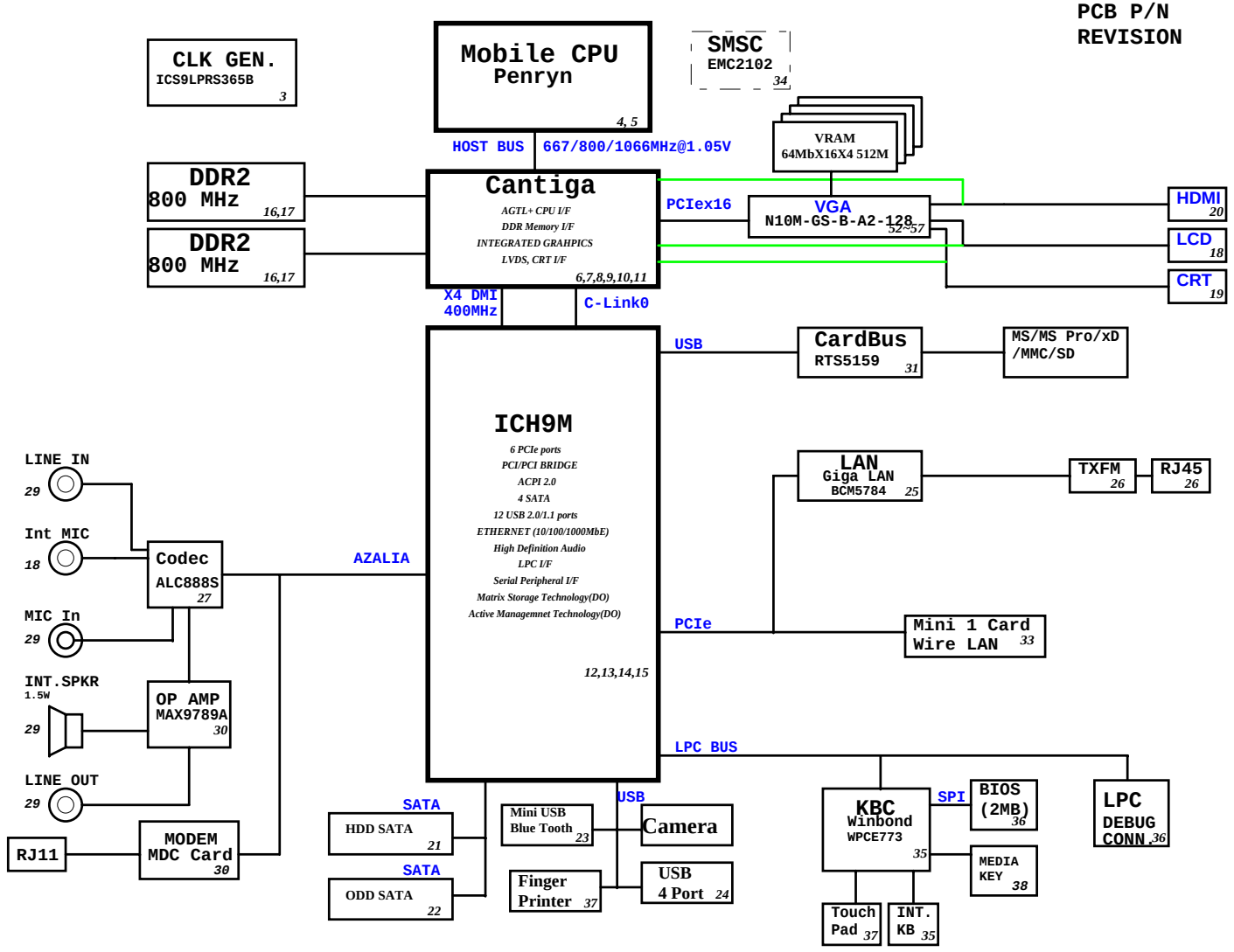
JV71-MV Block Diagram

Project code: 91.4FX01.001
PCB P/N : 48.4FX01.0SA
REVISION : 09242 -1



SYSTEM DC/DC
ISL62392 42

INPUTS	OUTPUTS
DCBATOUT	5V_S5(6A) 3D3V_S5(7A) 5V_AUX_S5 3D3V_AUX_S5

SYSTEM DC/DC
TPS51124 43

INPUTS	OUTPUTS
DCBATOUT	1D05V_S0(9A) 1D5V_S3(12A)

RT9026 44

1D5V_S3	DDR_VREF_S3 (1.2A)

RT9018 44

1D5V_S3	1D1V_S0(2A)

TPS51117 45

DCBATOUT	FBVDD(4A)

CHARGER
ISL88731A 47

INPUTS	OUTPUTS
DCBATOUT	BT+

CPU DC/DC
ISL6266A 41

INPUTS	OUTPUTS
DCBATOUT	VCC_CORE 38A

VGA_CORE
RT8202A 47

INPUTS	OUTPUTS
DCBATOUT	VGA_CORE 13A

GFXCORE
ISL6263A 46

INPUTS	OUTPUTS
DCBATOUT	VCC_GFXCORE (7A)

PCB STACKUP

TOP		L1
GND		L2
S		L3
S		L4
GND		L5
BOTTOM		L6

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Title: BLOCK DIAGRAM

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ICH9M Functional Strap Definitions

Signal	Usage/When Sampled	Comment
HDA_SDOUT	XOR Chain Entrance/ PCIE Port Config1 bit1, Rising Edge of PWROK	Allows entrance to XOR Chain testing when TP3 pulled low.When TP3 not pulled low at rising edge of PWROK,sets bit1 of RPC.PC(Config Registers: offset 224h). This signal has weak internal pull-down
HDA_SYNC	PCIE config1 bit0, Rising Edge of PWROK.	This signal has a weak internal pull-down. Sets bit0 of RPC.PC(Config Registers:Offset 224h)
GNT2#/ GPIO53	PCIE config2 bit2, Rising Edge of PWROK.	This signal has a weak internal pull-up. Sets bit2 of RPC.PC2(Config Registers:Offset 0224h)
GPIO20	Reserved	This signal should not be pulled high.
GNT1#/ GPIO51	ESI Strap (Server Only) Rising Edge of PWROK	ESI compatible mode is for server platforms only. This signal should not be pulled low for desttop and mobile.
GNT3#/ GPIO55	Top-Block Swap Override. Rising Edge of PWROK.	Sampled low:Top-Block Swap mode(inverts A16 for all cycles targeting FWH BIOS space). Note: Software will not be able to clear the Top-Swap bit until the system is rebooted without GNT3# being pulled down.
GNT0#: SPI_CS1#/ GPIO58	Boot BIOS Destination Selection 0:1. Rising Edge of PWROK.	Controllable via Boot BIOS Destination bit (Config Registers:Offset 3410h:bit 11:10). GNT0# is MSB, 01-SPI, 10-PCI, 11-LPC.
SPI_MOSI	Integrated TPM Enable, Rising Edge of CLPWROK	Sample low: the Integrated TPM will be disabled. Sample high: the MCH TPM enable strap is sampled low and the TPM Disable bit is clear, the Integrated TPM will be enable.
GPIO49	DMI Termination Voltage, Rising Edge of PWROK.	The signal is required to be low for desktop applications and required to be high for mobile applications.
SATALED#	PCI Express Lane Reversal. Rising Edge of PWROK.	Signal has weak internal pull-up. Sets bit 27 of MPC.LR(Device 28:Function 0:Offset D8)
SPKR	No Reboot. Rising Edge of PWROK.	If sampled high, the system is strapped to the "No Reboot" mode(ICH9 will disable the TCO Timer system reboot feature). The status is readable via the NO REBOOT bit.
TP3	XOR Chain Entrance. Rising Edge of PWROK.	This signal should not be pull low unless using XOR Chain testing.
GPIO33/ HDA_DOCK _EN#	Flash Descriptor Security Override Strap Rising Edge of PWROK	Sampled low:the Flash Descriptor Security will be overridden. If high,the security measures will be in effect.This should only be enabled in manufacturing environments using an external pull-up resister.

ICH9M Integrated Pull-up and Pull-down Resistors

SIGNAL	Resistor Type/Value
CL_CLK[1:0]	PULL-UP 20K
CL_DATA[1:0]	PULL-UP 20K
CL_RST0#	PULL-UP 20K
DPRSLPVR/GPIO16	PULL-DOWN 20K
ENERGY_DETECT	PULL-UP 20K
HDA_BIT_CLK	PULL-DOWN 20K
HDA_DOCK_EN#/GPIO33	PULL-UP 20K
HDA_RST#	PULL-DOWN 20K
HDA_SDIN[3:0]	PULL-DOWN 20K
HDA_SDOUT	PULL-DOWN 20K
HDA_SYNC	PULL-DOWN 20K
GLAN_DOCK#	The pull-up or pull-down active when configured for native GLAN_DOCK# functionality and determined by LAN controller
GNT[3:0]#/GPIO[55,53,51]	PULL-UP 20K
GPIO[20]	PULL-DOWN 20K
GPIO[49]	PULL-UP 20K
LDA[3:0]#/FHW[3:0]#	PULL-UP 20K
LAN_RXD[2:0]	PULL-UP 20K
LDRQ[0]	PULL-UP 20K
LDRQ[1]/GPIO23	PULL-UP 20K
PME#	PULL-UP 20K
PWRBTN#	PULL-UP 20K
SATALED#	PULL-UP 15K
SPI_CS1#/GPIO58/CLGPIO6	PULL-UP 20K
SPI_MOSI	PULL-DOWN 20K
SPI_MISO	PULL-UP 20K
SPKR	PULL-DOWN 20K
TACH_[3:0]	PULL-UP 20K
TP[3]	PULL-UP 20K
USB[11:0][P,N]	PULL-DOWN 15K

Cantiga chipset and ICH9M I/O controller Hub strapping configuration

Pin Name	Strap Description	Configuration
CFG[2:0]	FSB Frequency Select	000 = FSB1067 011 = FSB667 010 = FSB800 others = Reserved
CFG[4:3] CFG8 CFG[15:14] CFG[18:17]	Reserved	
CFG5	DMI x2 Select	0 = DMI x2 1 = DMI x4 (Default)
CFG6	iTPM Host Interface	0= The iTPM Host Interface is enabled(Note2) **1=The iTPM Host Interface is disalbed(default)**
CFG7	Intel Management engine Crypto strap	0 = Transport Layer Security (TLS) cipher suite with no confidentiality **1 = TLS cipher suite with confidentiality (default)**
CFG9	PCIE Graphics Lane	0 = Reverse Lanes,15->0,14->1 ect.. **1= Normal operation(Default):Lane Numbered in order**
CFG10	PCIE Loopback enable	0 = Enable (Note 3) **1= Disabled (default)**
CFG[13:12]	XOR/ALL	00 = Reserve 10 = XOR mode Enabled 01 = ALLZ mode Enabled (Note 3) **11 = Disabled (default)**
CFG16	FSB Dynamic ODT	0 = Dynamic ODT Disabled **1 = Dynamic ODT Enabled (Default)**
CFG19	DMI Lane Reversal	**0 = Normal operation(Default): Lane Numbered in Order** 1 = Reverse Lanes DMI x4 mode[MCH -> ICH]:(3->0,2->1,1->2and0->3) DMI x2 mode[MCH -> ICH]:(3->0,2->1)
CFG20	Digital Display Port (SDVO/DP/iHDMI) Concurrent with PCIe	**0 = Only Digital Display Port or PCIE is operational (Default)** 1 =Digital display Port and PCIe are operting simulataneously via the PEG port
SDVO_CTRLDATA	SDVO Present	**0 =No SDVO Card Present (Default)** 1 = SDVO Card Present
L_DDC_DATA	Local Flat Panel (LFP) Present	**0 = LFP Disabled (Default)** 1= LFP Card Present; PCIE disabled

NOTE:
1. All strap signals are sampled with respect to the leading edge of the (G)MCH Power OK (PWROK) signal.
2. iTPM can be disabled by a 'Soft-Strap' option in the Flash-decriptor section of the Firmware. This 'Soft-Strap' is activated only after enabling iTPM via CFG6.
Only one of the CFG10/CFG/12/CFG13 straps can be enabled at any time.

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Title: ***Reference***

Size: A3 | Document Number: **JV71** | Rev: **-2**

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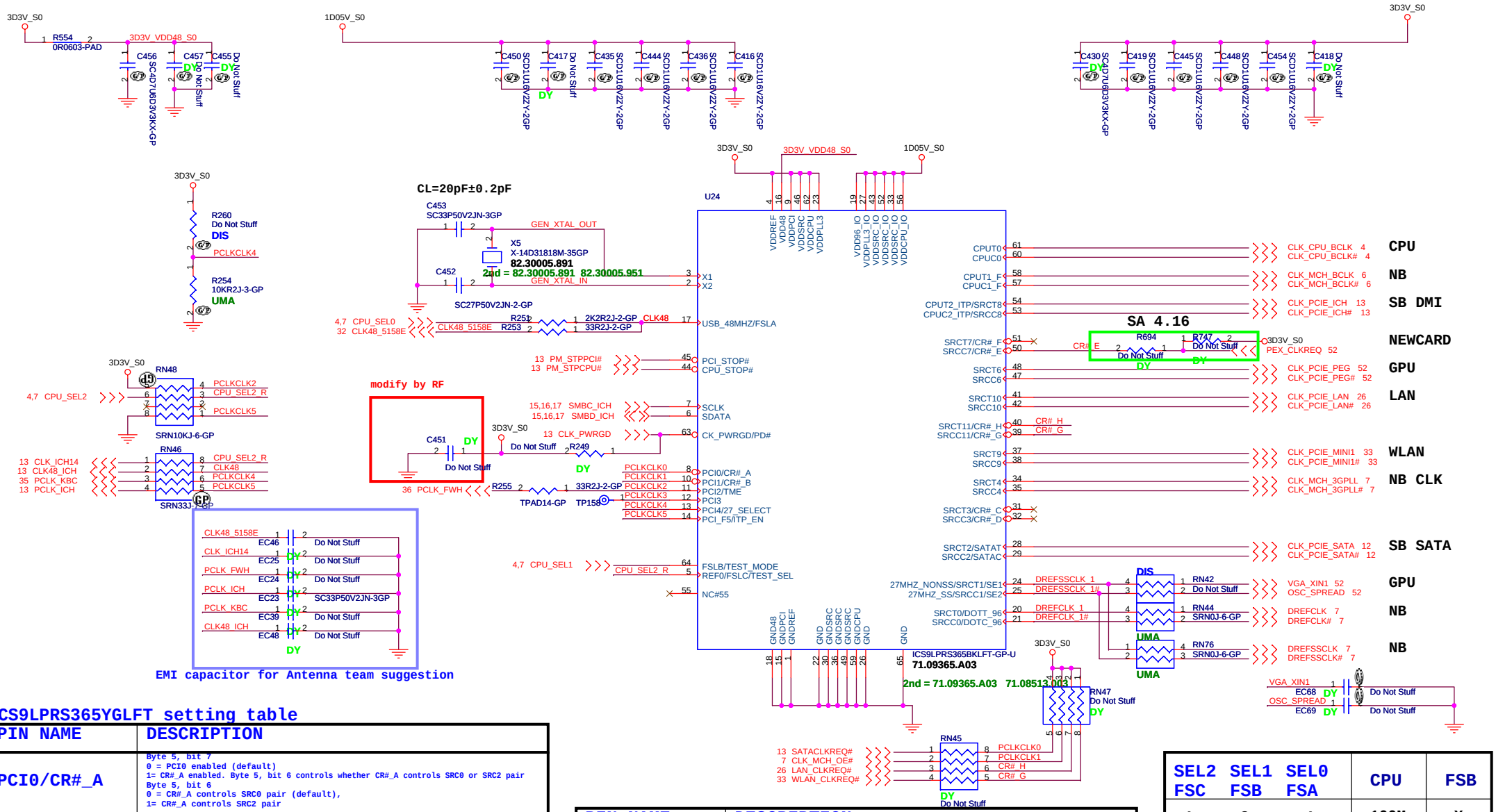

ICS9LPRS365YGLFT setting table

PIN NAME	DESCRIPTION
PCI0/CR#_A	Byte 5, bit 7 0 = PCI0 enabled (default) 1= CR#_A enabled. Byte 5, bit 6 controls whether CR#_A controls SRC0 or SRC2 pair Byte 5, bit 6 0 = CR#_A controls SRC0 pair (default), 1= CR#_A controls SRC2 pair
PCI1/CR#_B	Byte 5, bit 5 0 = PCI1 enabled (default) 1= CR#_B enabled. Byte 5, bit 6 controls whether CR#_B controls SRC1 or SRC4 pair Byte 5, bit 4 0 = CR#_B controls SRC1 pair (default) 1= CR#_B controls SRC4 pair
PCI2/TME	0 = Overclocking of CPU and SRC Allowed 1 = Overclocking of CPU and SRC NOT allowed
PCI3	
PCI4/27M_SEL	0 = Pin17 as SRC-1, Pin18 as SRC-1#, Pin13 as DOT96, Pin14 as DOT96# 1 = Pin17 as 27MHz, Pin 18 as 27MHz_SS, Pin13 as SRC-0, Pin14 as SRC-0#
PCI_F5/ITP_EN	0 =SRC8/SRC8# 1 = ITP/ITP#
SRCT3/CR#_C	Byte 5, bit 3 0 = SRC3 enabled (default) 1= CR#_C enabled. Byte 5, bit 2 controls whether CR#_C controls SRC0 or SRC2 pair Byte 5, bit 2 0 = CR#_C controls SRC0 pair (default), 1= CR#_C controls SRC2 pair

PIN NAME	DESCRIPTION
SRCC3/CR#_D	Byte 5, bit 1 0 = SRC3 enabled (default) 1= CR#_D enabled. Byte 5, bit 0 controls whether CR#_D controls SRC1 or SRC4 pair Byte 5, bit 0 0 = CR#_D controls SRC1 pair (default) 1= CR#_D controls SRC4 pair
SRCC7/CR#_E	Byte 6, bit 7 0 = SRC7# enabled (default) 1= CR#_F controls SRC6
SRCT7/CR#_F	Byte 6, bit 6 0 = SRC7 enabled (default) 1= CR#_F controls SRC8
SRCC11/CR#_G	Byte 6, bit 5 0 = SRC11# enabled (default) 1= CR#_G controls SRC9
SRCT11/CR#_H	Byte 6, bit 4 0 = SRC11 enabled (default) 1= CR#_H controls SRC10

SEL2 FSC	SEL1 FSB	SEL0 FSA	CPU	FSB
1	0	1	100M	X
0	0	1	133M	533M
0	1	1	166M	667M
0	1	0	200M	800M
0	0	0	266M	1067M

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Title: Clock Generator

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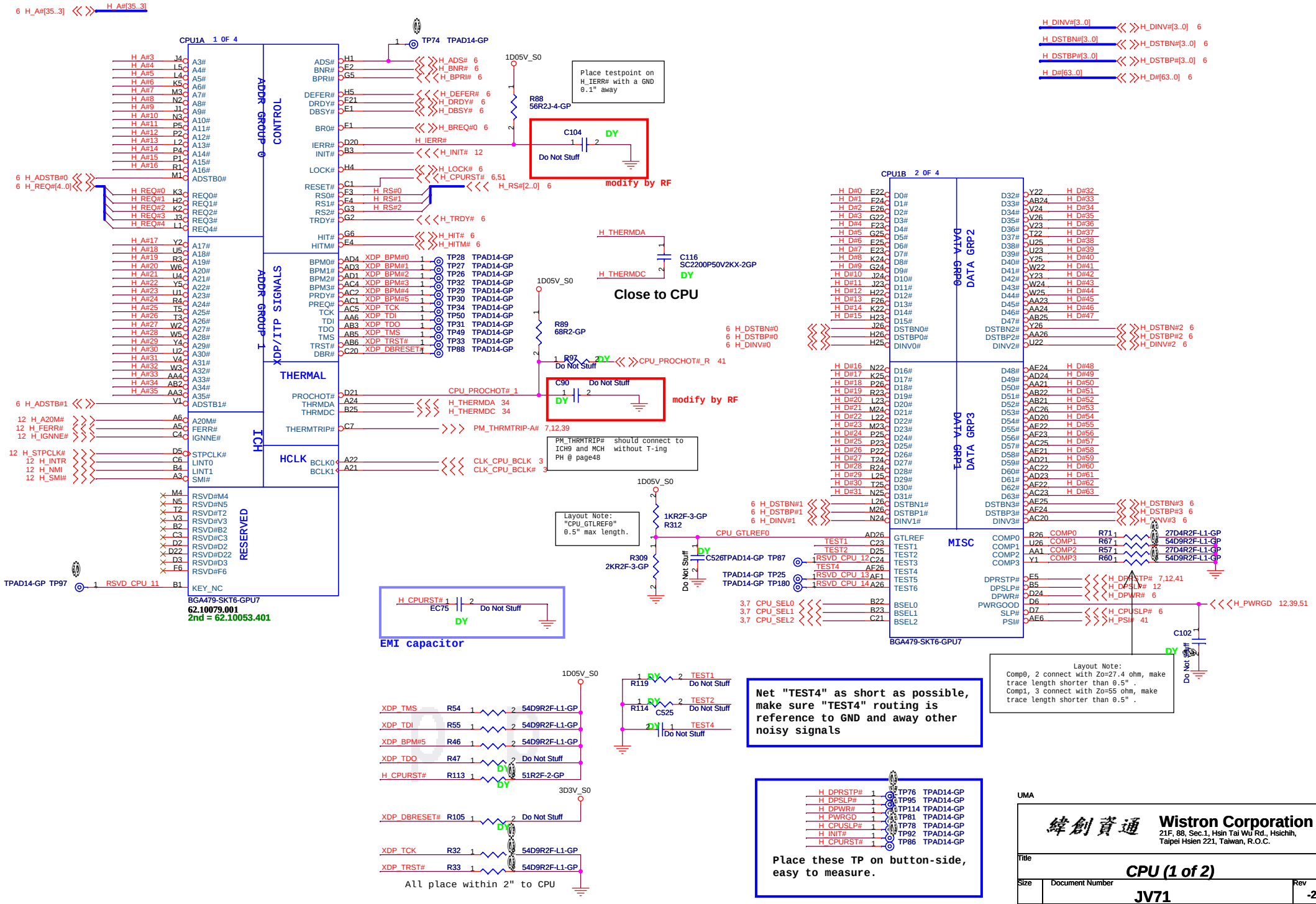
CPU1A 1 0F 4
ADDR GROUP 0
ADDR GROUP 1
CONTROL
XDP/ITP SIGNALS
THERMAL
HCLK
ICH
RESERVED
BGA479-SKT6-GPU7
62.10079.001
2nd = 62.10053.401
CPU1B 2 0F 4
DATA GRP2
DATA GRP0
DATA GRP1
DATA GRP3
MISC
BGA479-SKT6-GPU7
Close to CPU
modify by RF
EMI capacitor
Net "TEST4" as short as possible, make sure "TEST4" routing is reference to GND and away other noisy signals
Place these TP on button-side, easy to measure.
All place within 2" to CPU
Layout Note: Comp0, 2 connect with Zo=27.4 ohm, make trace length shorter than 0.5" . Comp1, 3 connect with Zo=55 ohm, make trace length shorter than 0.5" .
Place testpoint on H_IERR# with a GND 0.1" away
PM_THRMTRIP# should connect to ICH9 and MCH PH @ page48
Layout Note: "CPU_GTLREF0" 0.5" max length.
Do Not Stuff
DY
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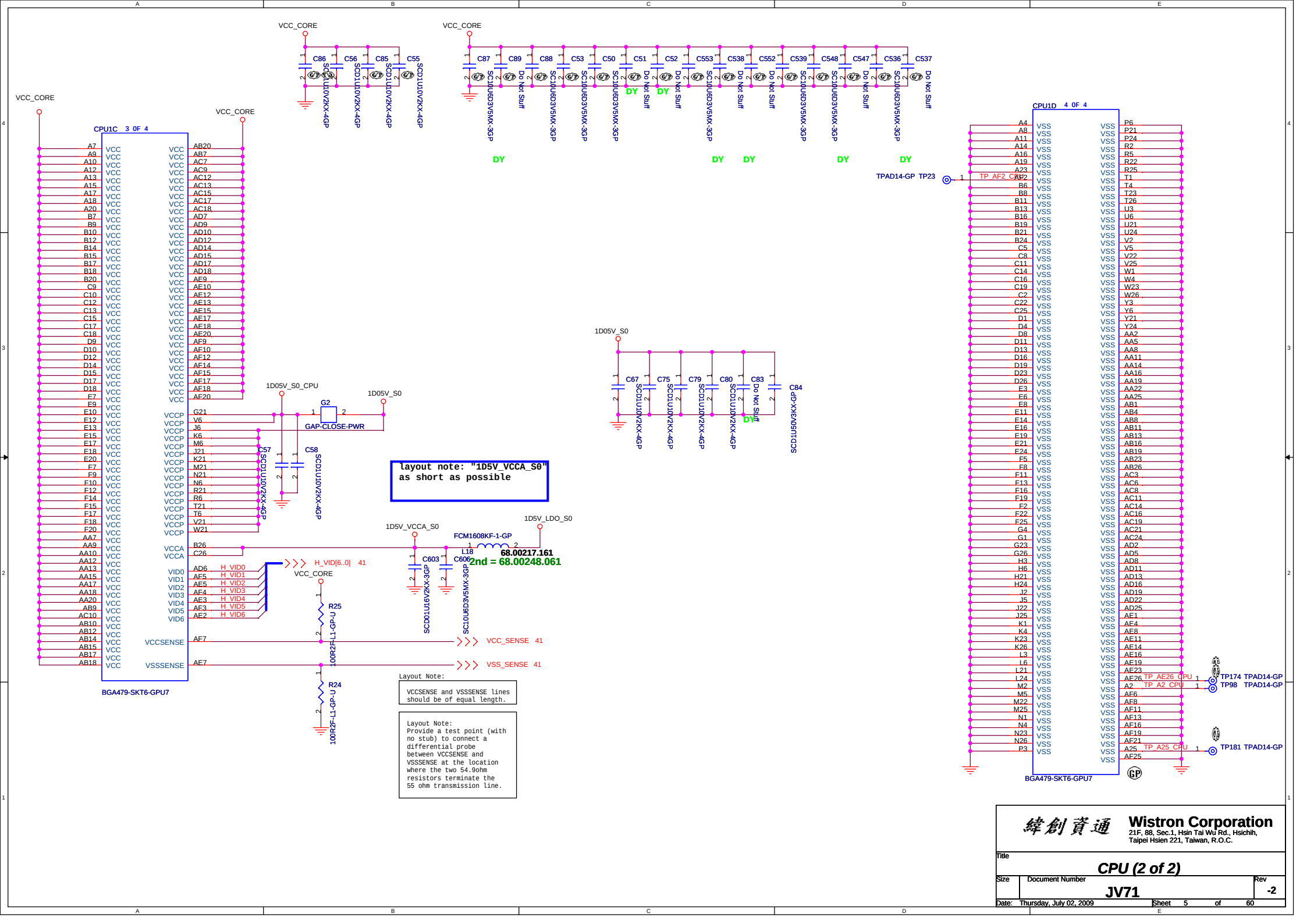

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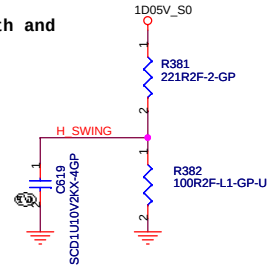
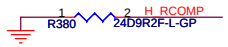
H_SWING routing Trace width and Spacing use 10 / 20 mil

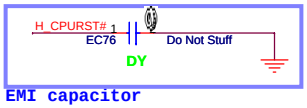
H_SWING Resistors and Capacitors close MCH 500 mil (MAX)



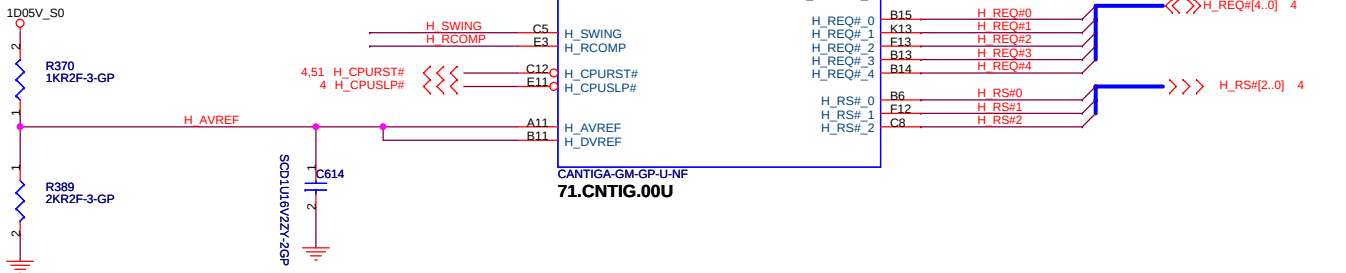
H_RCOMP routing Trace width and Spacing use 10 / 20 mil



Place them near to the chip (< 0.5")



EMI capacitor



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Title	***Cantiga (1 of 6)***	
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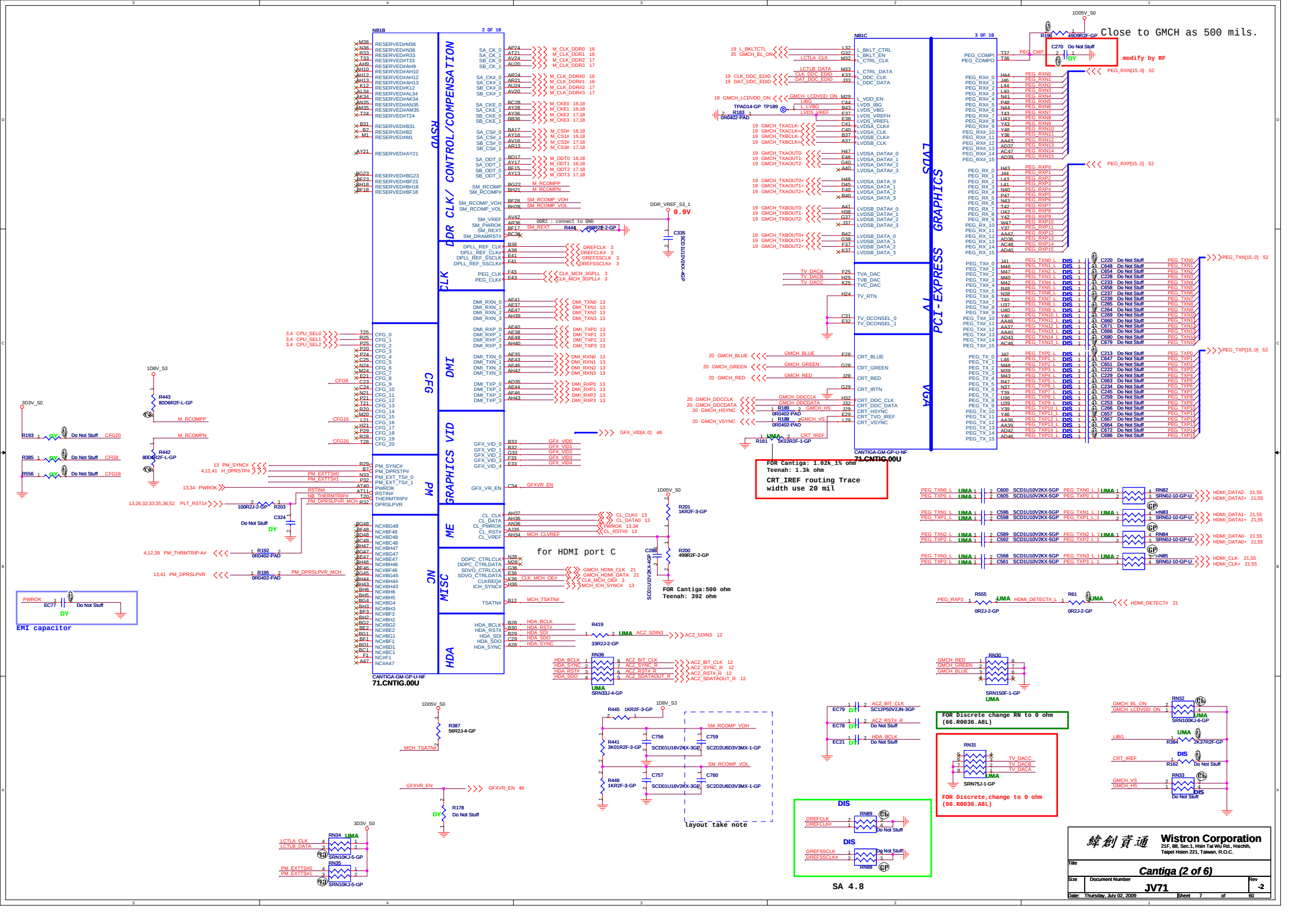
Close to GMCH as 500 mils.
modify by RF
FOR Cantiga 1.02k_1% ohm
Teenah: 1.3k ohm
CRT_IREF routing Trace width use 20 mil
for HDMI port C
FOR Cantiga:500 ohm
Teenah: 392 ohm
layout take note
FOR Discrete change RN to 0 ohm (66.R0036.A8L)
FOR Discrete,change to 0 ohm (66.R0036.A8L)
EMI capacitor
CANTIGA-GM-GP-U-NF
71.CNTIG.00U
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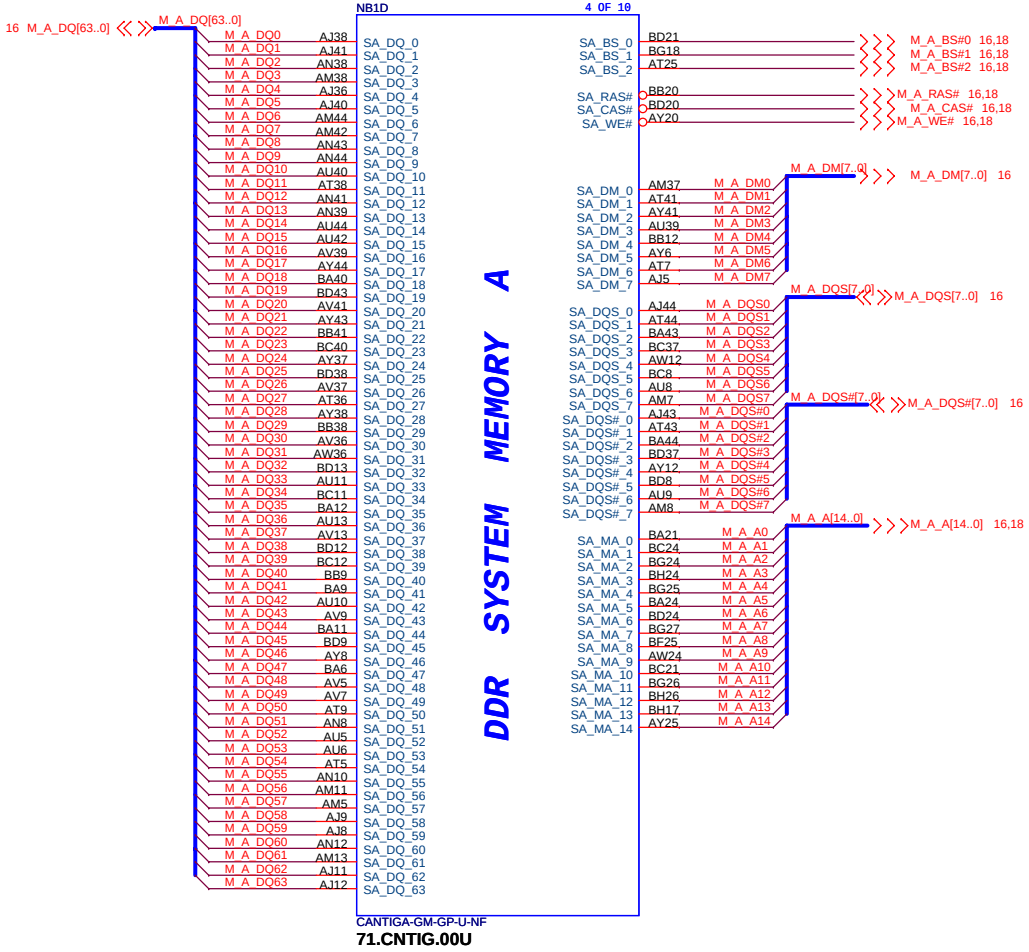
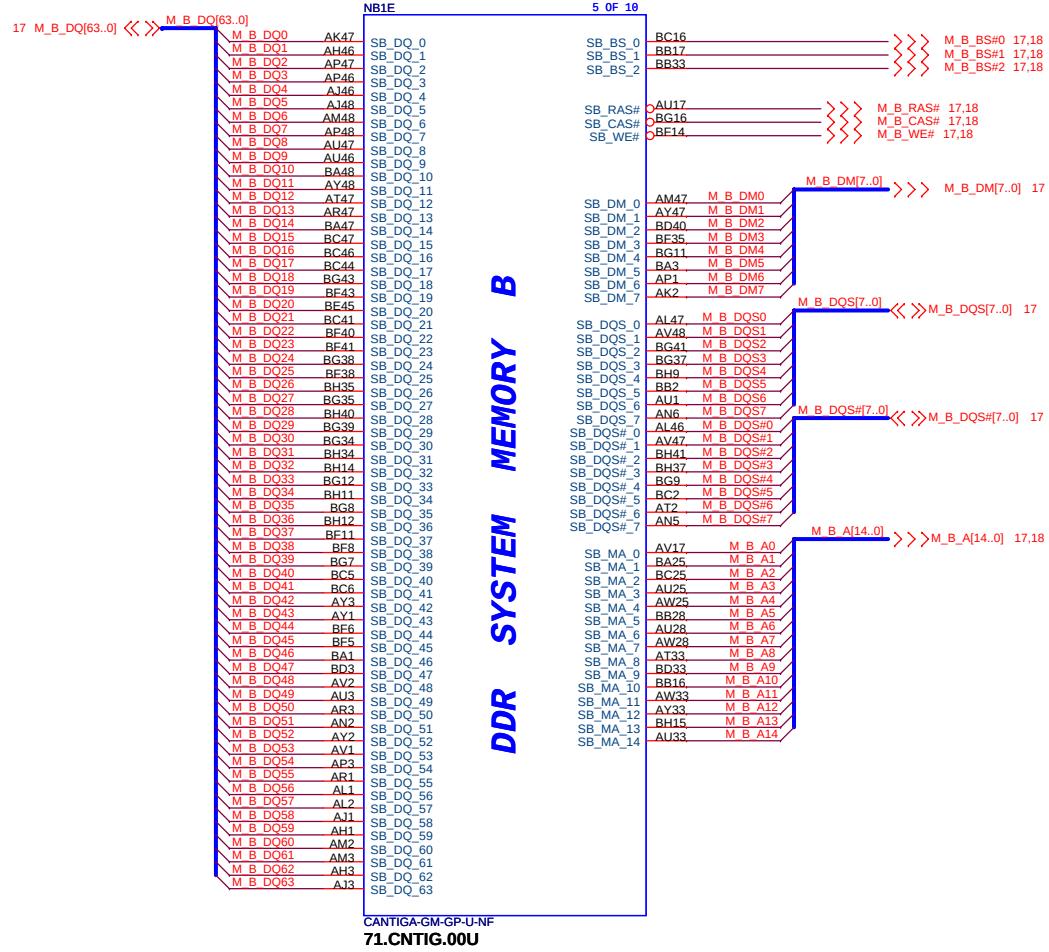
SA 4.8





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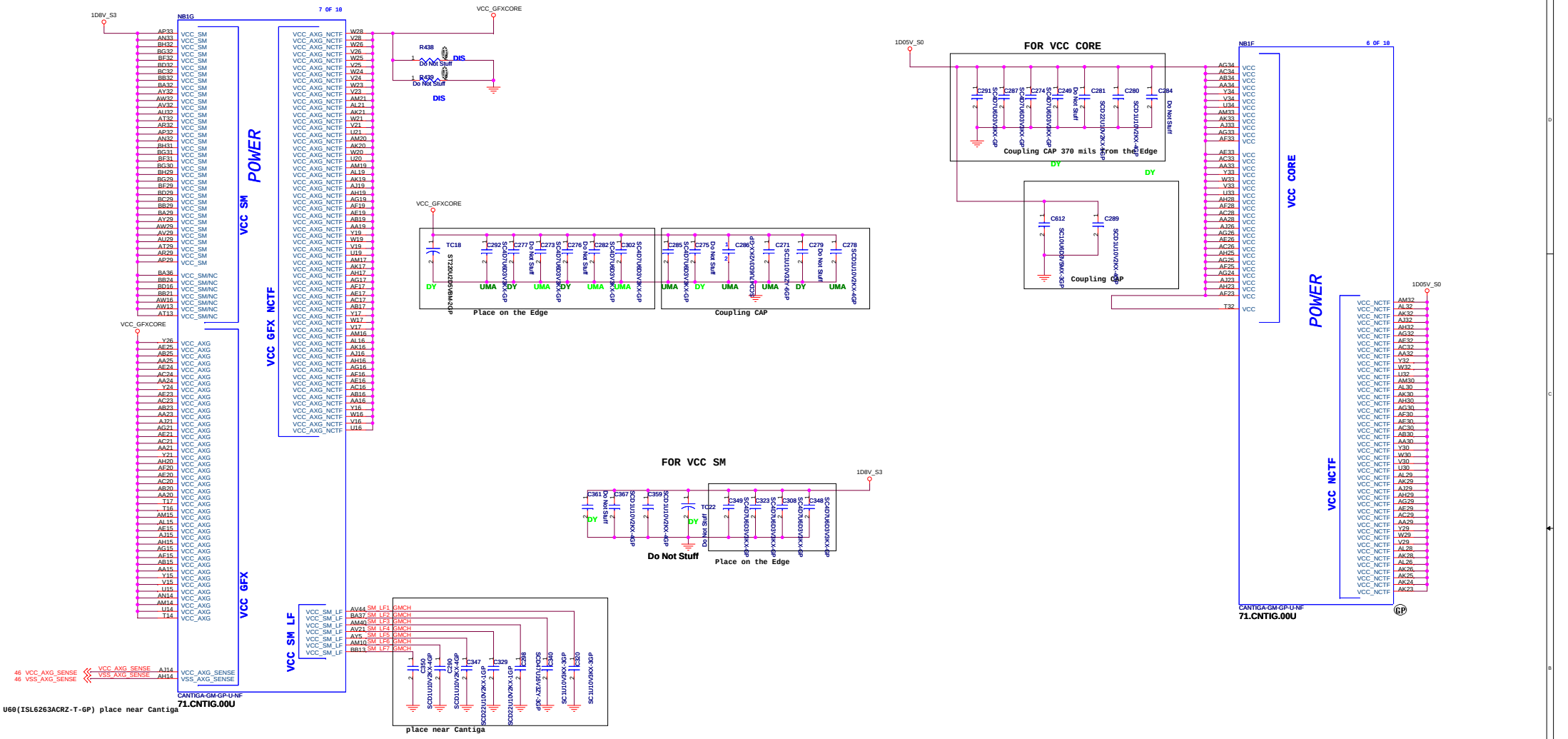

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Title	Cantiga (4 of 6)		
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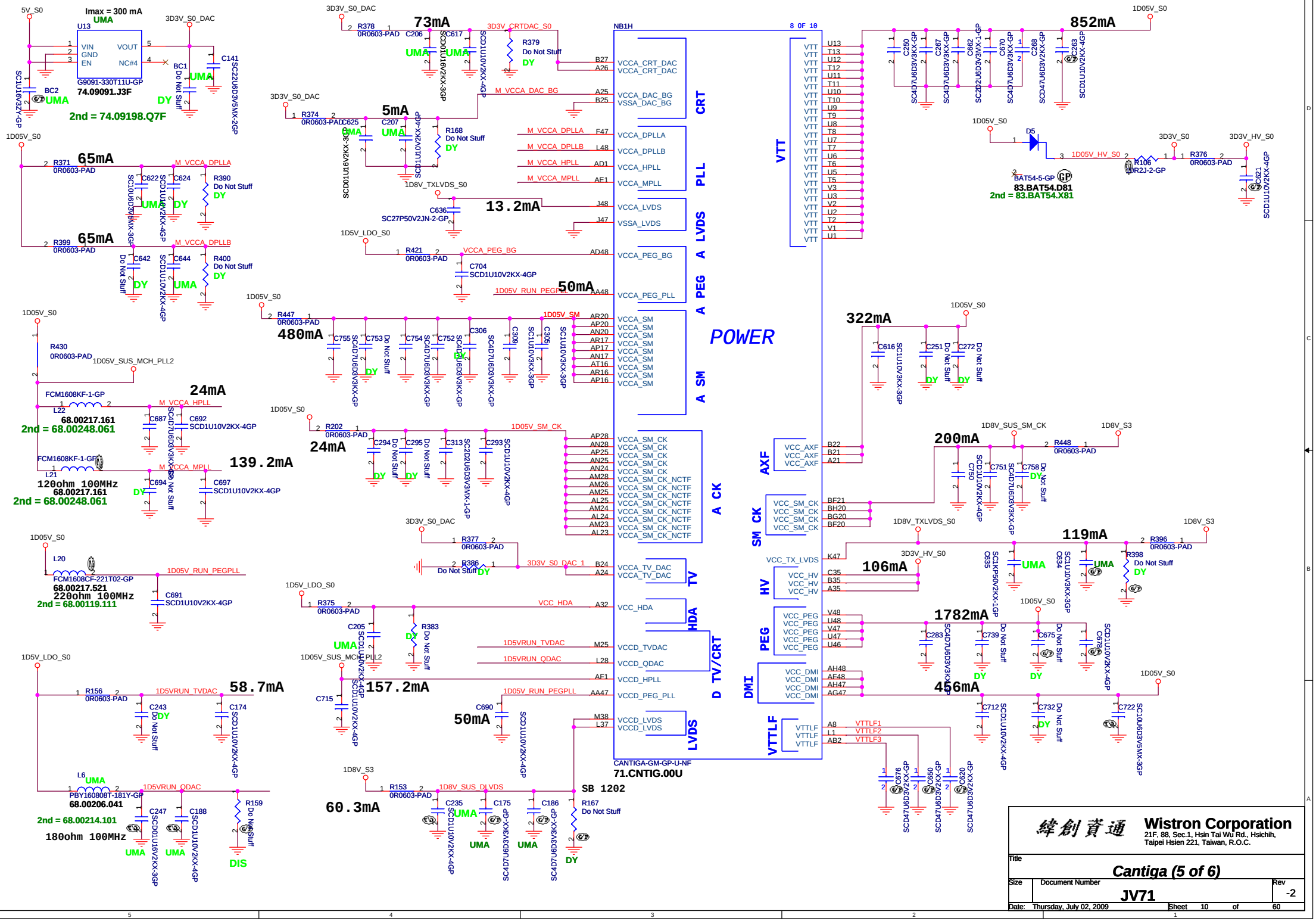
POWER
NB1H
CANTIGA-GM-GP-U-NF
71.CNTIG.00U
SB 1202
Imax = 300 mA
UMA
G9091-330T11U-GP
74.09091.J3F
2nd = 74.09198.Q7F
73mA
5mA
65mA
65mA
13.2mA
50mA
480mA
24mA
139.2mA
322mA
200mA
119mA
106mA
1782mA
456mA
852mA
24mA
58.7mA
157.2mA
50mA
60.3mA
68.00217.161
2nd = 68.00248.061
68.00217.521
2nd = 68.00119.111
68.00206.041
2nd = 68.00214.101
120ohm 100MHz
180ohm 100MHz
2nd = 83.BAT54.X81
CRT
PLL
A LVDS
A PEG
A SM
A CK
TV
HDA
D TV/CRT
LVDS
AXF
SM CK
HV
PEG
DMI
VTTLF
VTT
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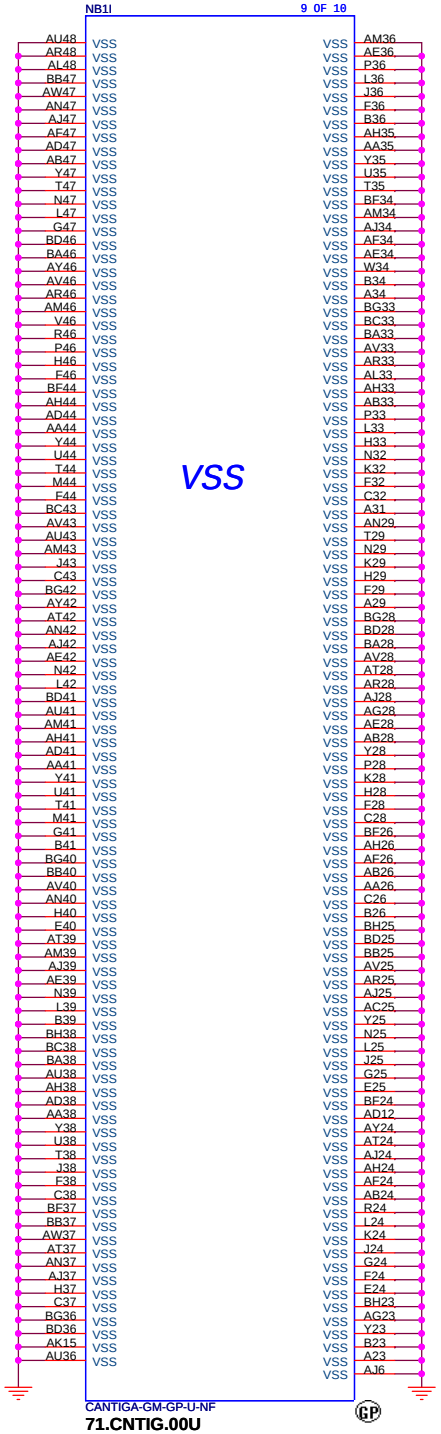

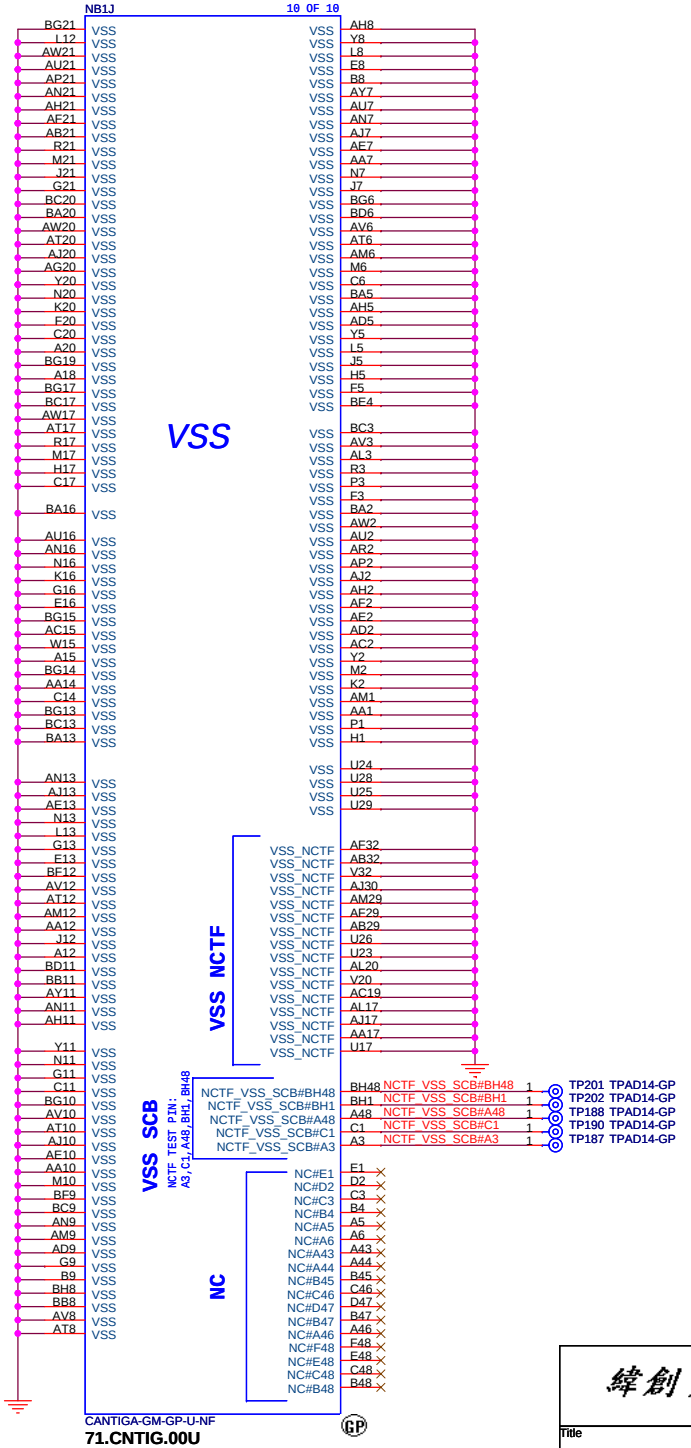

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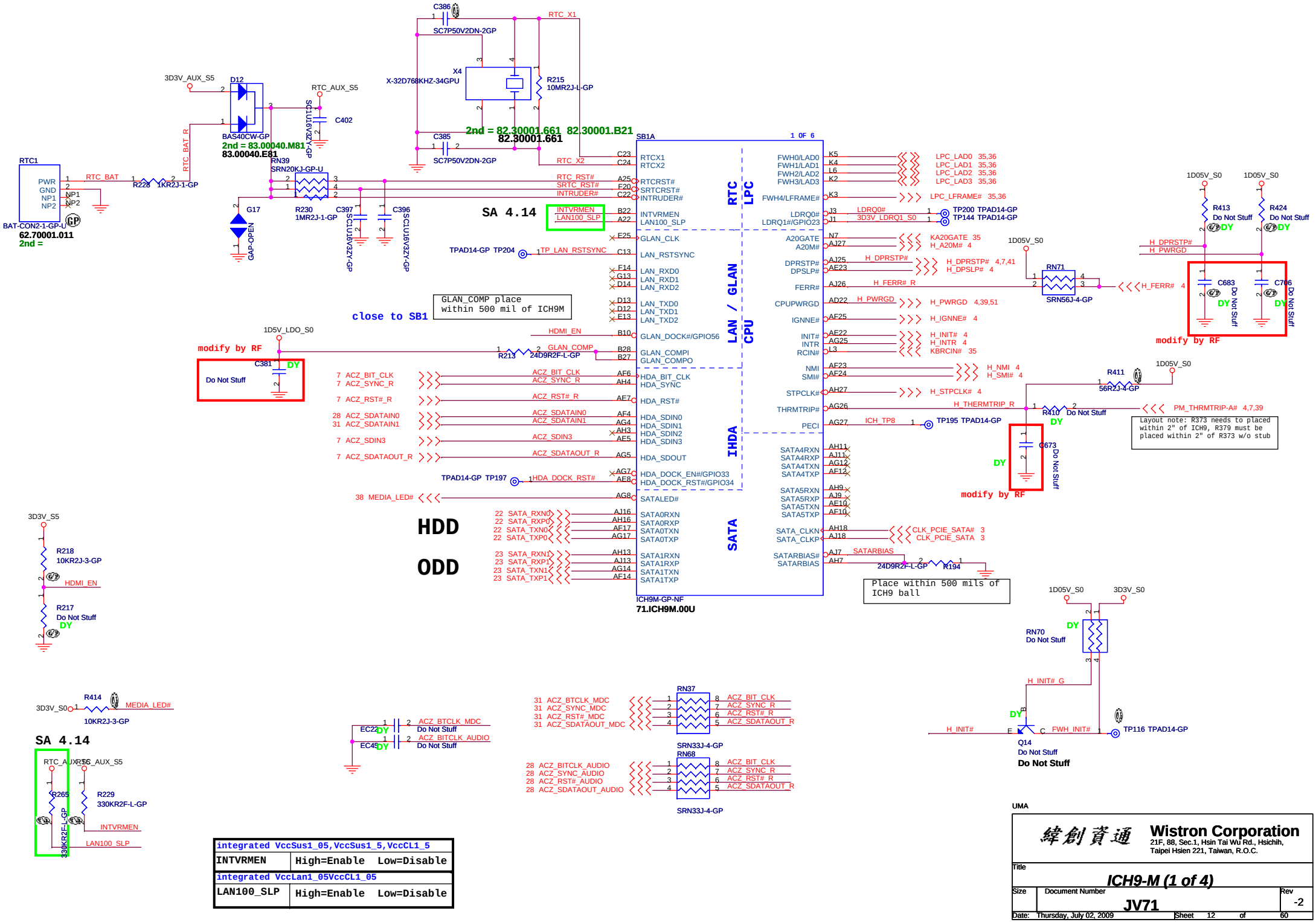
SB1A
1 OF 6
ICH9M-GP-NF
71.ICH9M.00U
RTC
LPC
LAN / GLAN
CPU
IHDA
SATA
SA 4.14
HDD
ODD
close to SB1
GLAN_COMP place within 500 mil of ICH9M
Place within 500 mils of ICH9 ball
modify by RF
Do Not Stuff
DY
2nd = 82.30001.661 82.30001.B21
82.30001.661
2nd = 83.00040.M81
83.00040.E81
62.70001.011
2nd =
Layout note: R373 needs to placed within 2" of ICH9, R379 must be placed within 2" of R373 w/o stub
integrated VccSus1_05,VccSus1_5,VccCL1_5
INTVRMEN High=Enable Low=Disable
integrated VccLan1_05VccCL1_05
LAN100_SLP High=Enable Low=Disable
UMA
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PCI_GNT#0 and SPI_CS1#
have weak internal Pull up

SB1B 2 OF 6

PCI

AD0 AD1 AD2 AD3 AD4 AD5 AD6 AD7 AD8 AD9 AD10 AD11 AD12 AD13 AD14 AD15 AD16 AD17 AD18 AD19 AD20 AD21 AD22 AD23 AD24 AD25 AD26 AD27 AD28 AD29 AD30 AD31

REQ0# GNT0# REQ1#/GPIO50 GNT1#/GPIO51 REQ2#/GPIO52 GNT2#/GPIO53 REQ3#/GPIO54 GNT3#/GPIO55

C/BE0# C/BE1# C/BE2# C/BE3#

IRDY# PAR PCIRST# DEVSEL# PERR# PLOCK# SERR# STOP# TRDY# FRAME#

PLTRST# PCICLK PME#

PCI_REQ#0 PCI_REQ#1 PCI_REQ#2 PCI_REQ#3 PCI_IRDY# PCI_DEVSEL# PCI_PERR# PCI_LOCK# PCI_SERR# PCI_STOP# PCI_TRDY# PCI_FRAME# PCI_RST# R1 R216 2 0R0402-PAD PLT_RST1# 7,26,32,33,35,36,52 PCLK_ICH 3

C388 Do Not Stuff DY

Interrupt I/F

INT_PIRQA# INT_PIRQB# INT_PIRQC# INT_PIRQD# J5 E1 J6 C4

PIRQA# PIRQB# PIRQC# PIRQD#

PIRQE#/GPIO2 PIRQF#/GPIO3 PIRQG#/GPIO4 PIRQH#/GPIO5

INT_PIRQE# INT_PIRQF# INT_PIRQG# INT_PIRQH#

ICH9M-GP-NF
71.ICH9M.00U

SB1C 3 OF 6

15,26,33 SMB_CLK
15,26,33 SMB_DATA

SMBCLK SMBDATA LINKALERT#/GPIO60/CLGPIO4 SMLINK0 SMLINK1

SMB_LINK_ALERT#

RI# PM_RI# TPAD14-GP TP199 PM_SUS_STAT# DBRESET#

SUS_STAT#/LPCPD# SYS_RESET#

7 PM_SYNC#

PMSYNC#/GPIO0

SMB_ALERT#

SMBALERT#/GPIO11

3 PM_STPPCI# 3 PM_STPCPU#

STP_PCI# STP_CPU#

35 PM_CLKRUN#

CLKRUN#

26 PCIE_WAKE# 35 INT_SERIRQ 34 THRM#

WAKE# SERIRQ THRM#

34,41 VGATE_PWRGD

VRMPWRGD

SST

TACH1/GPIO1 TACH2/GPIO6 TACH3/GPIO7 GPIO8 LAN_PHY_PWR_CTRL/GPIO12 ENERGY_DETECT/GPIO13 TACH0/GPIO17 GPIO18 GPIO20 SCLOCK/GPIO22 GPIO27 GPIO28 SATACLKREQ#/GPIO35 SLOAD/GPIO38 SDATAOUT0/GPIO39 SDATAOUT1/GPIO48 GPIO49 GPIO57/CLGPIO5

SPKR MCH_SYNC# TP3 PWM0 PWM1 PWM2

SMB

SATA GPIO

SATA0GP/GPIO21 SATA1GP/GPIO19 SATA4GP/GPIO36 SATA5GP/GPIO37

AH23 SATA0GP AF19 SATA1GP AE21 ICH_GPIO36 AD20 ICH_GPIO37

RN72 SRN10KJ-6-GP

Clocks

CLK14 CLK48

H1 AF3 P1

CLK_ICH14 3 CLK48_ICH 3 PM_SUS_CLK 34

SYS GPIO

SLP_S3# SLP_S4# SLP_S5#

C16 E16 G17 PM_SLP_S3# 28,34,35,39,43,44 PM_SLP_S4# 35,43,44 PM_SLP_S5# TP203 TPAD14-GP

S4_STATE#/GPIO26 C10 S4_STATE# TP207 TPAD14-GP

PWROK G20 PWROK 7,34

Power MGT

DPRSLPVR/GPIO16 M2 PM_DPRSLPVR 1 R211 R212 100R2J-2-GP DY Do Not Stuff PM_DPRSLPVR 7,41

BATLOW# B13 PM_BATLOW# R

PWRBTN# R3 PWRBTN# ICH D8 BAS16-1-GP PM_PWRBTN# 35,51

LAN_RST# D20

RSMRST# D22 RSMRST# SB

CK_PWRGD R5 CLK_PWRGD 3

CLPWROK R6 PWROK 7,34

SLP_M# B16 PM_SLP_M# 1 TP148 TPAD14-GP

CL_CLK0 CL_CLK1 F24 B19 CL_CLK0 7

CL_DATA0 CL_DATA1 F22 C19 CL_DATA0 7

CL_VREF0 CL_VREF1 C25 A19 CL_VREF0_ICH

CL_RST0# CL_RST1# F21 D18 CL_RST#0 7

GPIO24/MEM_LED A16 ICH_GPIO24 1 TP153 TPAD14-GP

GPIO10/SUS_PWR_ACK C18 SUSPWRACK

GPIO14/AC_PRESENT C11 AC_PRESENT

GPIO9/WOL_EN C20 ICH_GPIO9 1 TP206 TPAD14-GP

GPIO

Controller Link

MISC

83.00016.B11 2nd = 83.00016.F11

3D3V_S0 R404 10KR2J-3-GP GAP-OPEN G78

TPAD14-GP TP196 TPAD14-GP TP122 ICH9_GPIO20 CLK_SEL1 AJ22

TPAD14-GP TP193 FP_ID AG19 35 EC_TMR AH21 35 ECSCI#_1 AG21 35 ECSWI# A21

R221 DY ICH_TP7 A20 Do Not Stuff

PSW_CLR# AE18 K1

3 SATACLKREQ# TPAD14-GP TP198 TPAD14-GP TP194 SATACLKREQ# PCB_VER0_SB AE19 PCB_VER1_SB AG22 MIC_SEL_1 AF21 NO_iTPM AH24 A8

7 MCH_ICH_SYNC# TPAD14-GP TP205 ICH_TP3 M7 AJ24 B21 AH20 AJ20 AJ21

GPIO049 should be pulled down to GND only when using Teenah. When using Cantiga, this ball should be left as No Connect.

3D3V_S0 R226 3K24R2F-GP C409 SCD1U10V2KX-4GP R227 453R2F-1-GP 3D3V_S5

R220 100KR2J-1-GP 3D3V_S5

SA 4.14

RN73 SRN10KJ-6-GP

USB_OC#0 USB_OC#1 USB_OC#3

SB1D 4 OF 6

PCI-Express

PERN1 PERP1 PETP1 PETN1

PERN2 PERP2 PETN2 PETP2

PERN3 PERP3 PETN3 PETP3

PERN4 PERP4 PETN4 PETP4

PERN5 PERP5 PETN5 PETP5

PERN6/GLAN_RXN PERP6/GLAN_RXP PETN6/GLAN_TXN PETP6/GLAN_TXP

SPI_CLK SPI_CS0# SPI_CS1#/GPIO58/CLGPIO6 SPI_MOSI SPI_MISO

SPI

USB

OC0#/GPIO59 OC1#/GPIO40 OC2#/GPIO41 OC3#/GPIO42 OC4#/GPIO43 OC5#/GPIO29 OC6#/GPIO30 OC7#/GPIO31 OC8#/GPIO44 OC9#/GPIO45 OC10#/GPIO46 OC11#/GPIO47

USBRBIAS USBRBIAS#

Direct Media Interface

DMI0RXN DMI0RXP DMI0TXN DMI0TXP

DMI1RXN DMI1RXP DMI1TXN DMI1TXP

DMI2RXN DMI2RXP DMI2TXN DMI2TXP

DMI3RXN DMI3RXP DMI3TXN DMI3TXP

DMI_CLKN DMI_CLKP

DMI_ZCOMP DMI_IRCOMP

USBP0N USBP0P USBP1N USBP1P USBP2N USBP2P USBP3N USBP3P USBP4N USBP4P USBP5N USBP5P USBP6N USBP6P USBP7N USBP7P USBP8N USBP8P USBP9N USBP9P USBP10N USBP10P USBP11N USBP11P

ICH9M-GP-NF
71.ICH9M.00U

26 PCIE_RXN1 26 PCIE_RXP1 26 PCIE_TXN1 26 PCIE_TXP1

C363 SCD1U10V2KX-5GP C360 SCD1U10V2KX-5GP TXN1 TXP1

LAN

33 PCIE_RXN2 33 PCIE_RXP2 33 PCIE_TXN2 33 PCIE_TXP2

C369 SCD1U10V2KX-5GP C365 SCD1U10V2KX-5GP TXN2 TXP2

MINICARD1

DMI_RXN0 7 DMI_RXP0 7 DMI_TXN0 7 DMI_TXP0 7

DMI_RXN1 7 DMI_RXP1 7 DMI_TXN1 7 DMI_TXP1 7

DMI_RXN2 7 DMI_RXP2 7 DMI_TXN2 7 DMI_TXP2 7

DMI_RXN3 7 DMI_RXP3 7 DMI_TXN3 7 DMI_TXP3 7

CLK_PCIE_ICH# 3 CLK_PCIE_ICH 3

DMI_IRCOMP_R

R417 24D9R2F-L-GP 1D5V_LDO_S0

USBPN0 25 USBPP0 25 USBPN1 25 USBPP1 25 USBPN2 25 USBPP2 25 USBPN3 33 USBPP3 33 USBPN4 19 USBPP4 19

USBPN6 37 USBPP6 37 USBPN7 24 USBPP7 24

USBPN9 25 USBPP9 25

USBPN11 32 USBPP11 32

SA 4.14

25 USB_OC#0 25 USB_OC#1 25 USB_OC#9

USB_OC#0 USB_OC#1 USB_OC#3 USB_OC#4 USB_OC#5 USB_OC#6 USB_OC#7 USB_OC#8 USB_OC#9 USB_OC#10 USB_OC#11

USB_RBIAS_PN AG2 AG1 R415 22D6R2F-L1-GP

SPI_ICH_CS1# F23

These R need close SB within 600 mils

EMI capacitor

EC81 DY VGATE_PWRGD Do Not Stuff

EC80 DY CLK_PWRGD Do Not Stuff

RP1 SRN10KJ-L3-GP

PM_RI# PM_BATLOW# R ECSWI# PCIE_WAKE# SMB_ALERT# DBRESET# SUSPWRACK SMB_LINK_ALERT#

RP3 SRN8K2J-2-GP-U

PCI_TRDY# INT_PIRQG# PCI_REQ#0 INT_PIRQH# INT_PIRQB# PCI_PERR# PCI_REQ#3 PCI_IRDY#

RP4 SRN8K2J-2-GP-U

INT_PIRQD# PCI_LOCK# PCI_FRAME# PCI_REQ#2 PCI_DEVSEL# PCI_REQ#1 PCI_STOP#

RP2 SRN8K2J-2-GP-U

INT_PIRQC# INT_PIRQF# INT_SERIRQ PM_CLKRUN# INT_PIRQA# INT_PIRQE# ECSCI#_1 PCI_SERR#

RP5 SRN10KJ-L3-GP

USB_OC#4 USB_OC#9 USB_OC#5 USB_OC#8 USB_OC#7 USB_OC#10 USB_OC#6 USB_OC#11

RN40 SRN10KJ-5-GP

DY R222 Do Not Stuff AC_PRESENT RSMRST#_SB

35 RSMRST#_KBC D11 BAT54-5-GP R224 100KR2J-1-GP

83.BAT54.D81

2nd = 83.BAT54.X81

USB	
Pair	Device
0	USB2
1	USB3
2	USB4
3	MINI1
4	CCD
5	NC
6	Finger Print
7	Blue Tooth
8	NC
9	USB1
10	NC
11	Cardreader

No Reboot Strap

SPKR	LOW = Defaule High=No Reboot

SA 4.14

MIC_SEL_1 DY R405 Do Not Stuff

ACZ_SPKR R434 DY Do Not Stuff

3D3V_S0

NO_iTPM PWROK RN38 SRN10KJ-5-GP

SPI_ICH_CS1# R225 DY Do Not Stuff

BOOT BIOS Strap

PCI_GNT#0	SPI_CS#1	BOOT BIOS Location
0	1	SPI
1	0	PCI
1	1	LPC(Default)

A16 swap override strap

PCI_GNT#3	low = A16 swap override enable high = default

UMA

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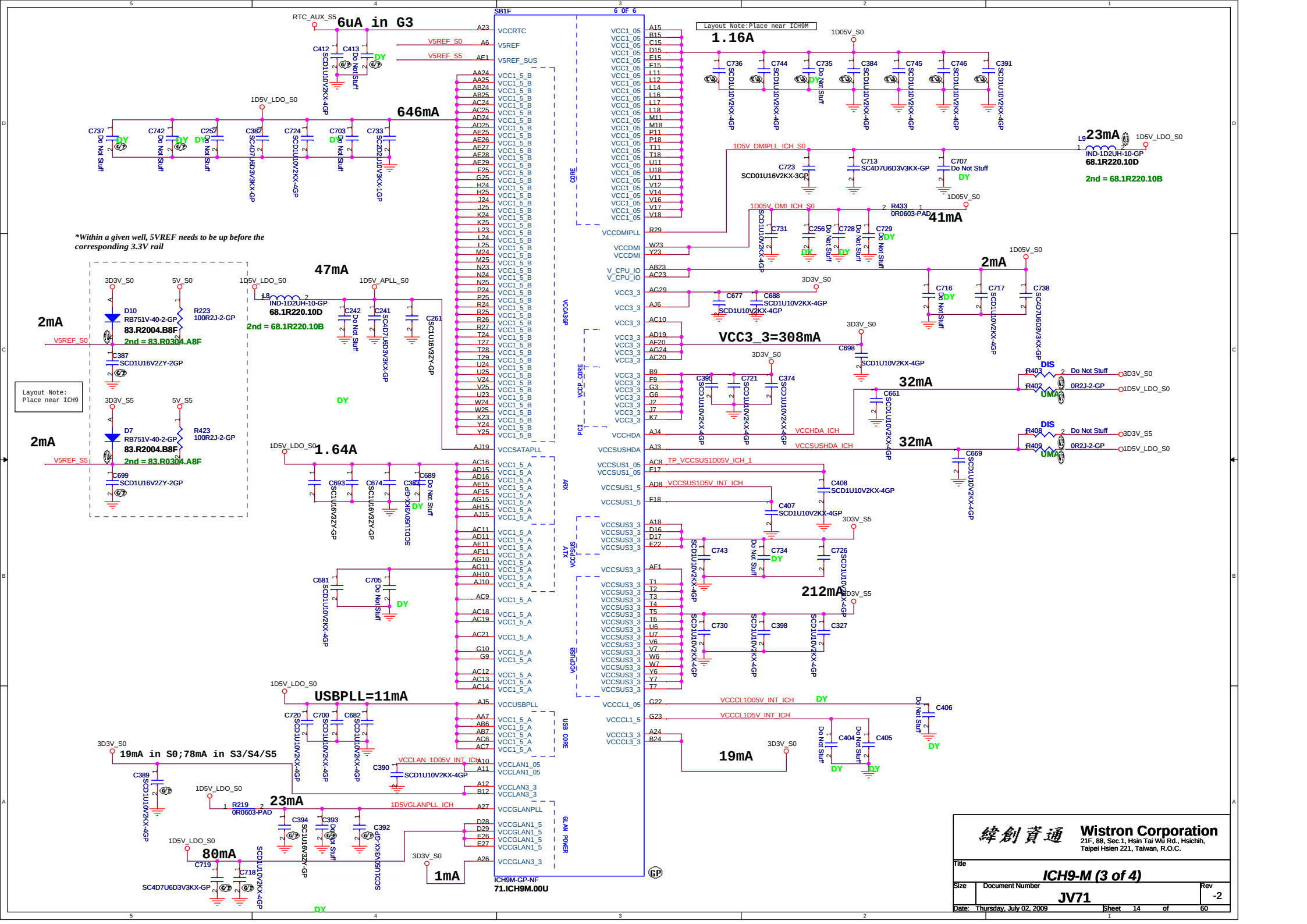
Title: ICH9-M (2 of 4)

Size: | Document Number: JV71 | Rev: -2

Date: Thursday, July 02, 2009 Sheet 13 of 60


SB1F
6 OF 6
ICH9M-GP-NF
71.ICH9M.00U
RTC_AUX_S5
6uA in G3
V5REF_S0
V5REF_S5
1D5V_LDO_S0
646mA
*Within a given well, 5VREF needs to be up before the corresponding 3.3V rail
47mA
1D5V_APLL_S0
IND-1D2UH-10-GP
68.1R220.10D
2nd = 68.1R220.10B
2mA
3D3V_S0
5V_S0
D10
RB751V-40-2-GP
R223
100R2J-2-GP
83.R2004.B8F
2nd = 83.R0304.A8F
3D3V_S5
5V_S5
D7
R423
Layout Note:
Place near ICH9
1.64A
USBPLL=11mA
19mA in S0;78mA in S3/S4/S5
23mA
80mA
1mA
1.16A
Layout Note:Place near ICH9M
1D05V_S0
1D05V_DMIPLL_ICH_S0
1D05V_DMI_ICH_S0
R433
0R0603-PAD
41mA
2mA
VCC3_3=308mA
32mA
DIS
UMA
212mA
VCCHDA_ICH
VCCSUSHDA_ICH
TP_VCCSUS1D05V_ICH_1
VCCSUS1D5V_INT_ICH
VCCCL1D05V_INT_ICH
19mA
1D5VGLANPLL_ICH
VCCLAN_1D05V_INT_ICH
CORE
VCCA3GP
VCCP_CORE
PCI
ARX
VCCP5IS
ATX
VCCP5IS
USB CORE
GLAN POWER
Wistron Corporation
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Title
ICH9-M (3 of 4)
Size
Document Number
JV71
Rev
-2
Date: Thursday, July 02, 2009
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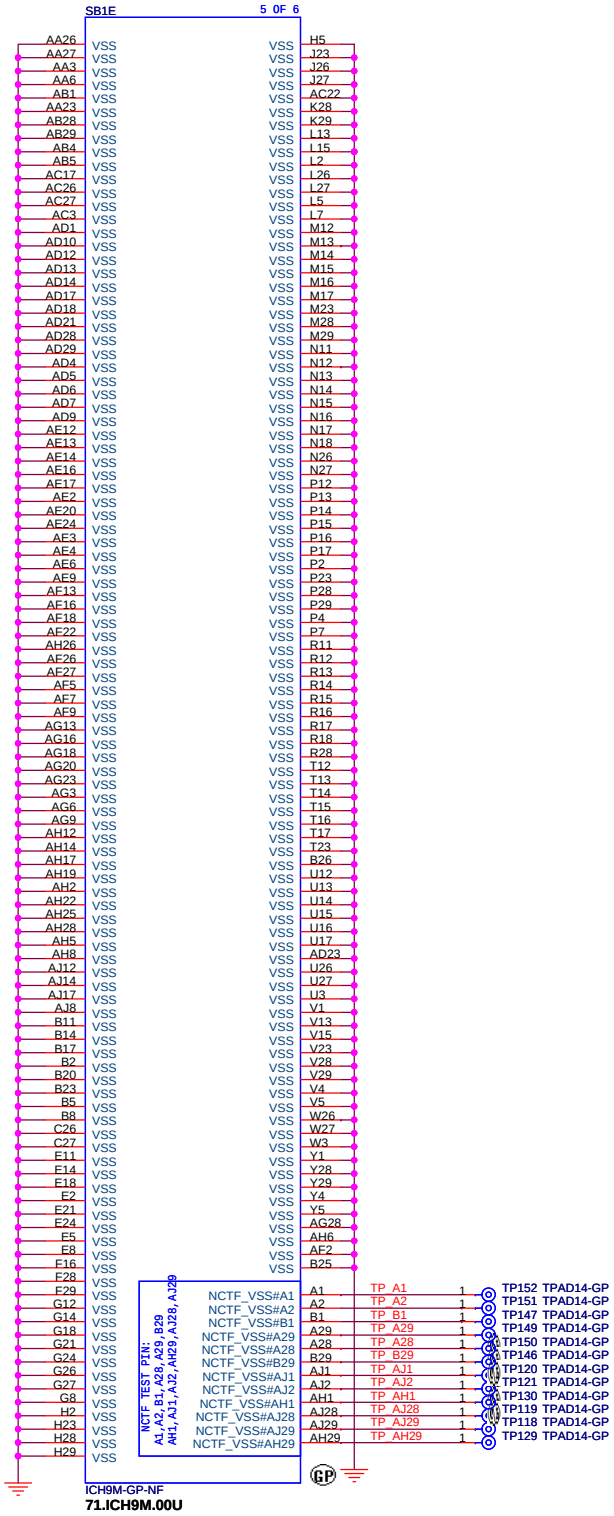

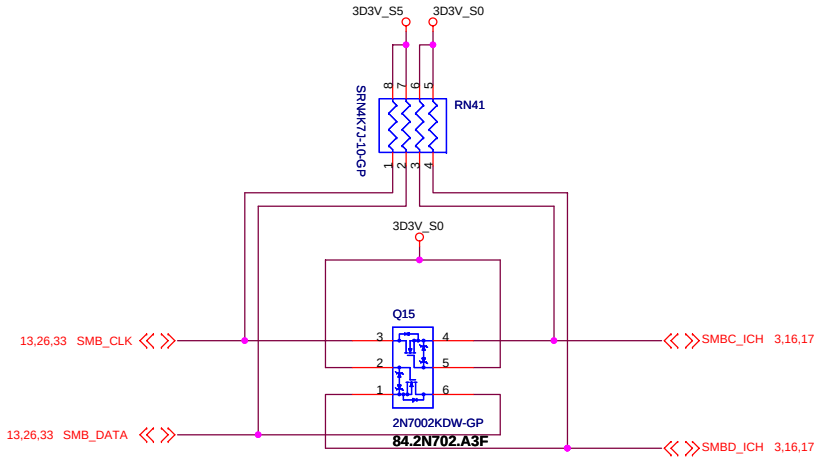

SMBUS

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Title: *ICH9-M (4 of 4)*

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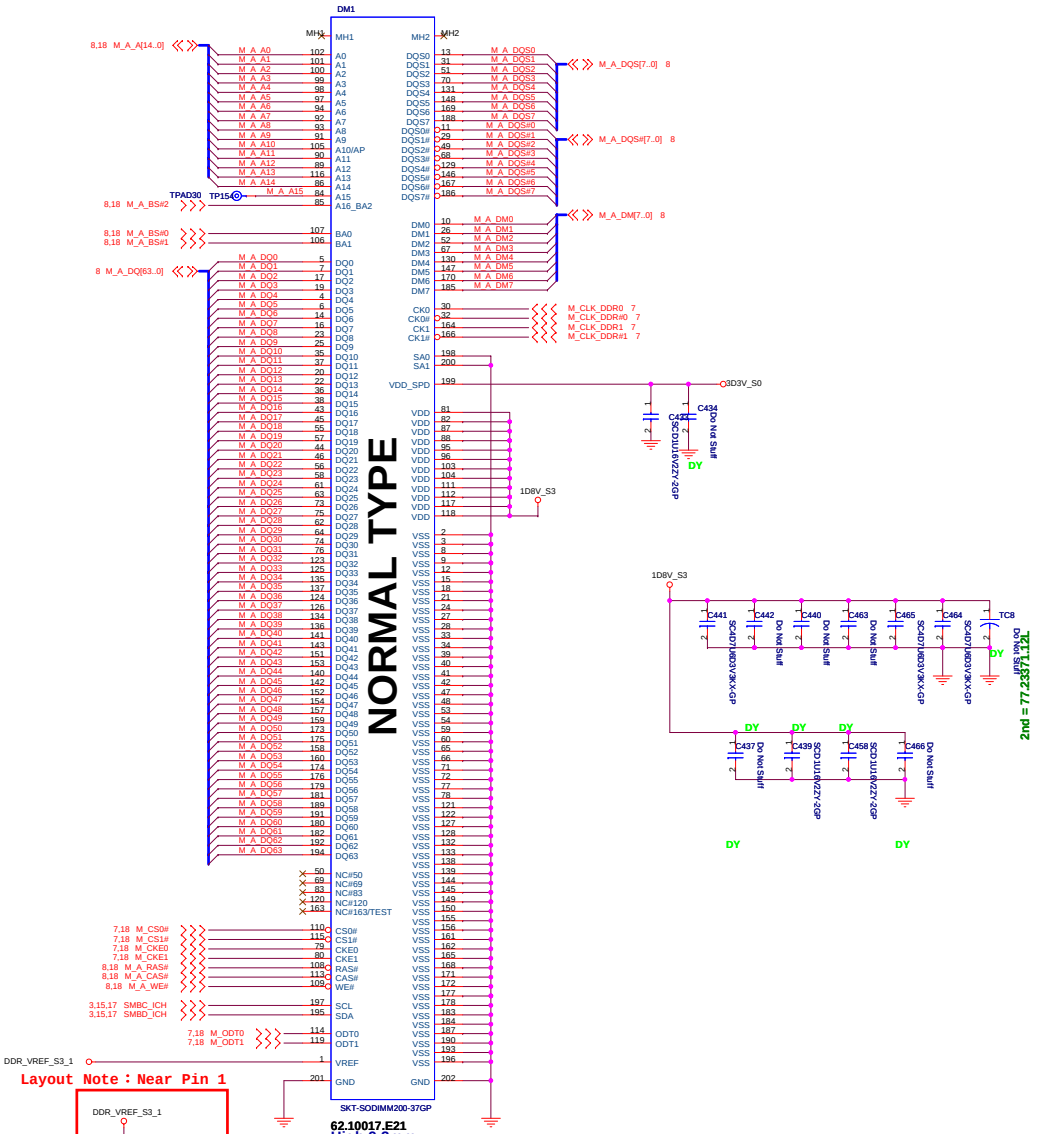
DDR2 SOCKET_1



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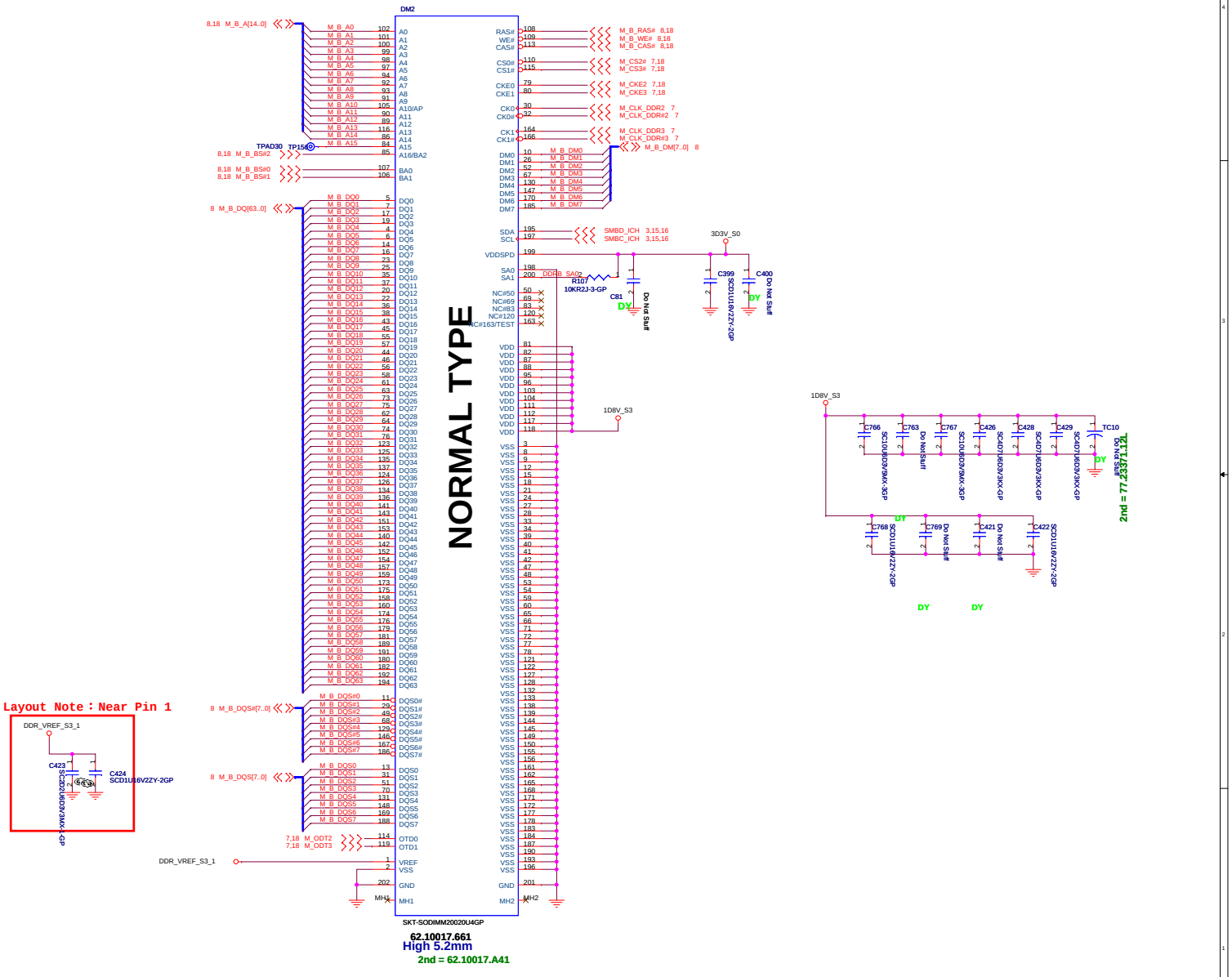
Title	DDR3 Socket		
Size	Document Number	JV71	Rev -2
Date: Thursday, July 02, 2009	Sheet 16 of 60		

DDR2 SOCKET_2



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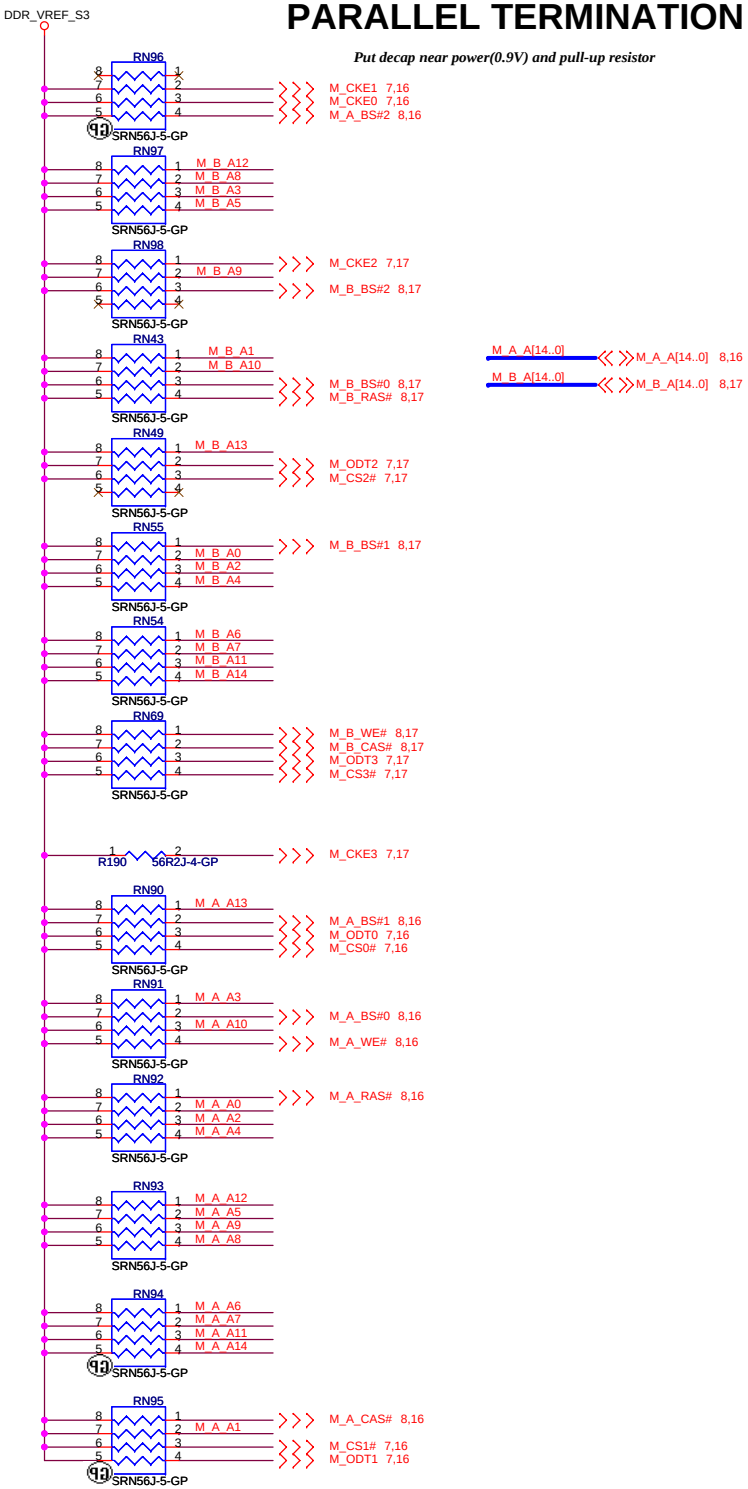
Title: DDR3 Socket2	
Size:	Document Number: JV71 Rev: -2
Date: Thursday, July 02, 2009	Sheet 17 of 60

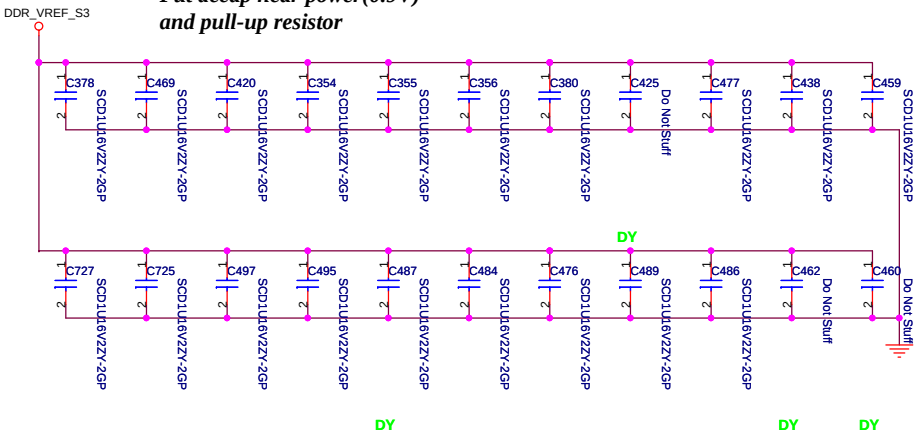
PARALLEL TERMINATION

Put decap near power(0.9V) and pull-up resistor



Decoupling Capacitor

Put decap near power(0.9V) and pull-up resistor



UMA

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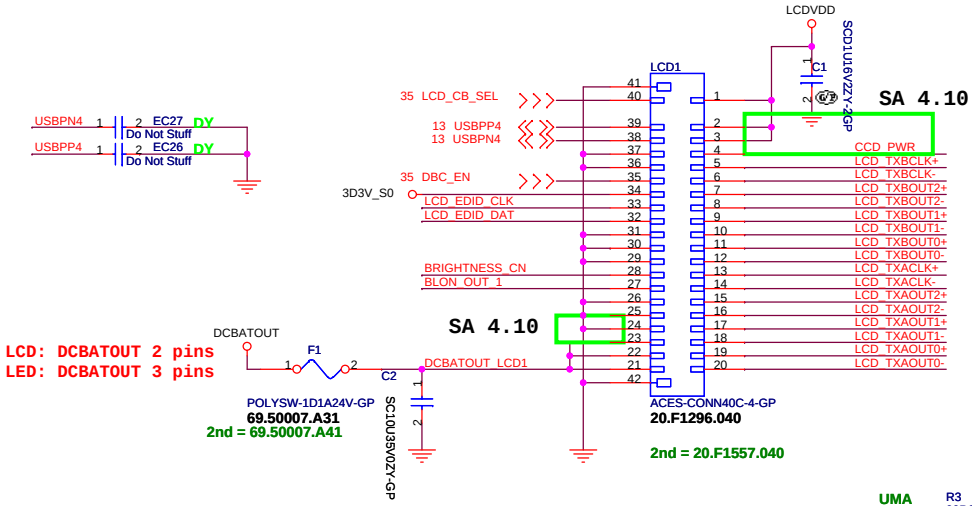
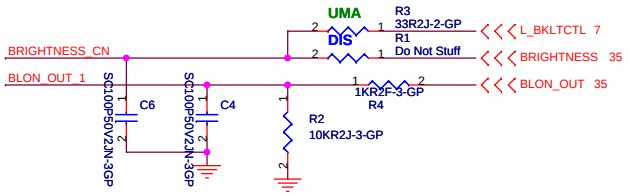
Title: ***DDR 2 Termination Resistor***

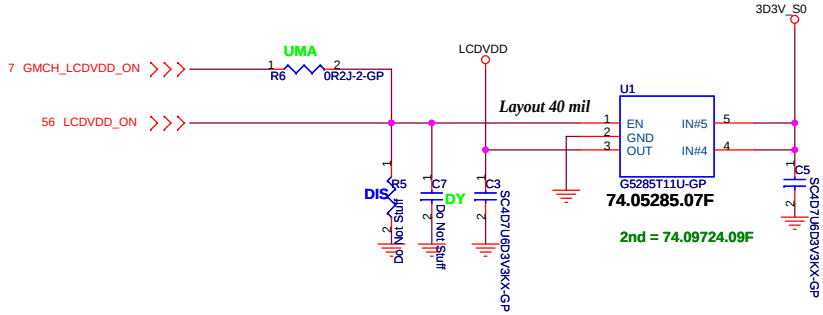
Size	Document Number	Rev
	JV71	-2

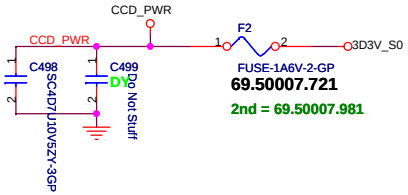
Date: Thursday, July 02, 2009 Sheet 18 of 60

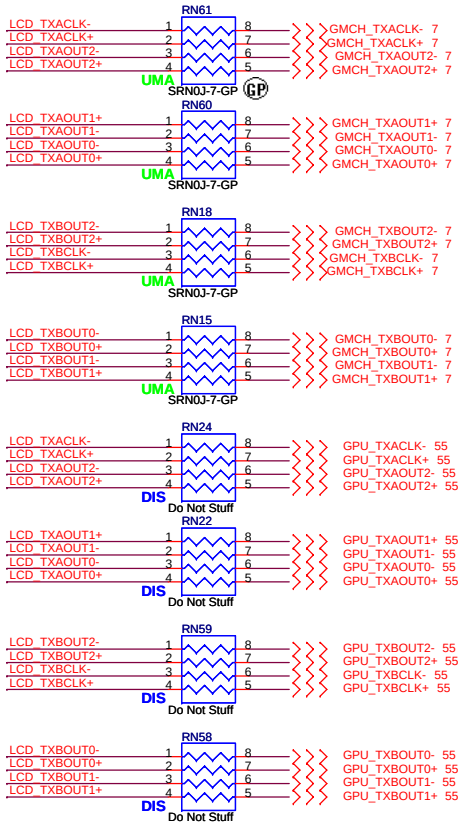
LCD/INVERTER/CCD CONN

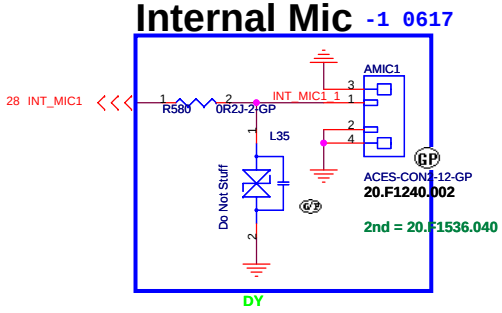


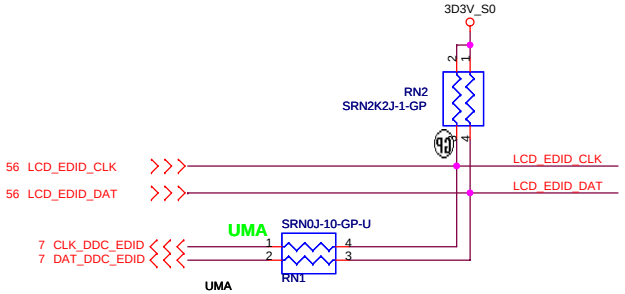












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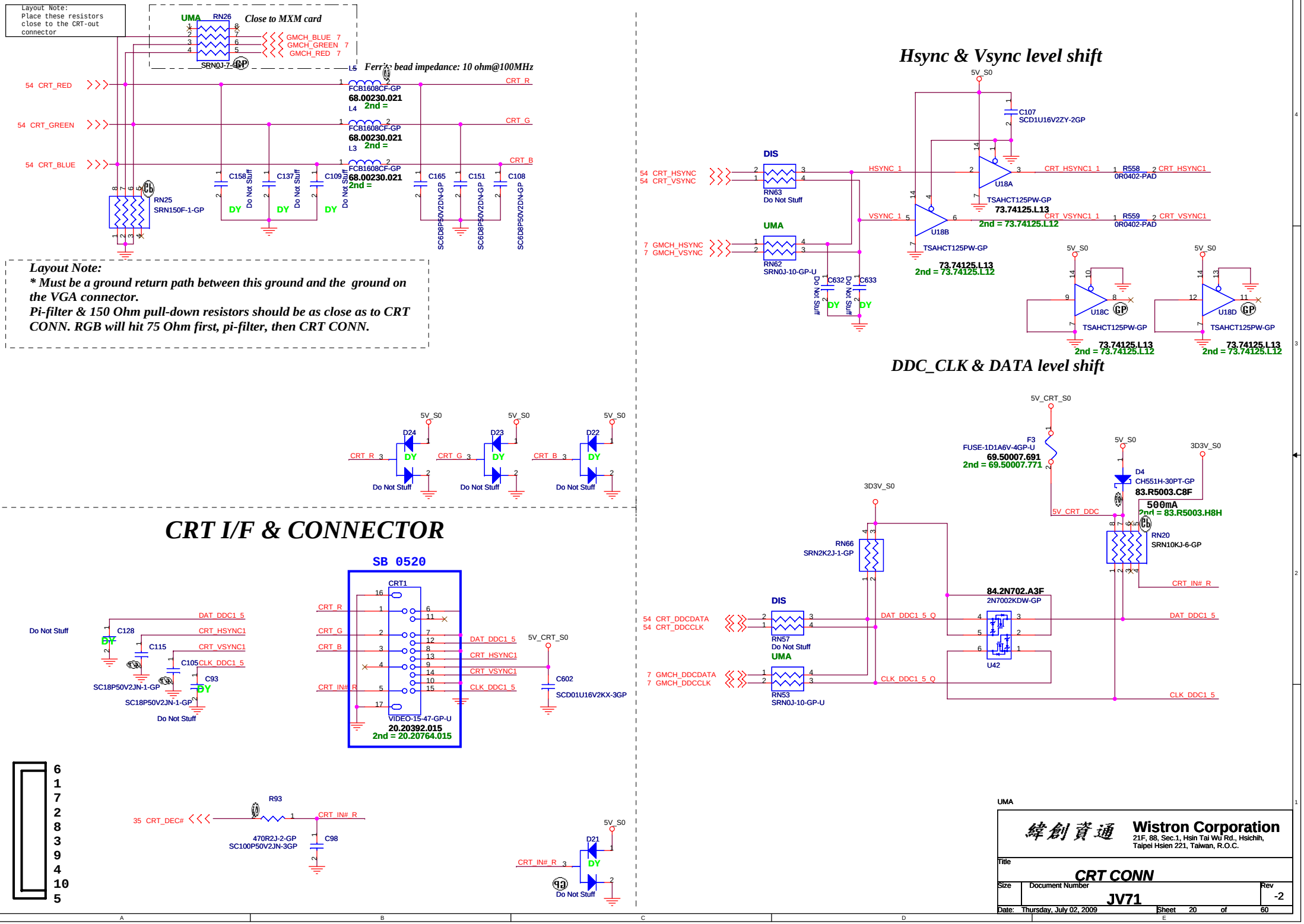
Title	**LCD CONN**	
Size	Document Number **JV71**	Rev -2
Date: Thursday, July 02, 2009	Sheet 19 of 60	


Layout Note:
Place these resistors close to the CRT-out connector
UMA
RN26
Close to MXM card
GMCH_BLUE 7
GMCH_GREEN 7
GMCH_RED 7
SRN0J-7-GP
Ferrite bead impedance: 10 ohm@100MHz
54 CRT_RED
54 CRT_GREEN
54 CRT_BLUE
L5
L4
L3
FCB1608CF-GP
68.00230.021
2nd =
CRT_R
CRT_G
CRT_B
RN25
SRN150F-1-GP
C158
C137
C109
C165
C151
C108
Do Not Stuff
DY
SC6D8P50V2DN-GP
Layout Note:
* Must be a ground return path between this ground and the ground on the VGA connector.
Pi-filter & 150 Ohm pull-down resistors should be as close as to CRT CONN. RGB will hit 75 Ohm first, pi-filter, then CRT CONN.
Hsync & Vsync level shift
5V_S0
C107
SCD1U16V2ZY-2GP
DIS
54 CRT_HSYNC
54 CRT_VSYNC
RN63
HSYNC_1
VSYNC_1
U18A
U18B
TSAHCT125PW-GP
73.74125.L13
2nd = 73.74125.L12
CRT_HSYNC1_1
CRT_VSYNC1_1
R558
R559
0R0402-PAD
CRT_HSYNC1
CRT_VSYNC1
UMA
7 GMCH_HSYNC
7 GMCH_VSYNC
RN62
SRN0J-10-GP-U
C632
C633
U18C
U18D
DDC_CLK & DATA level shift
5V_CRT_S0
F3
FUSE-1D1A6V-4GP-U
69.50007.691
2nd = 69.50007.771
3D3V_S0
D4
CH551H-30PT-GP
83.R5003.C8F
500mA
2nd = 83.R5003.H8H
5V_CRT_DDC
RN20
SRN10KJ-6-GP
CRT_IN#_R
RN66
SRN2K2J-1-GP
84.2N702.A3F
2N7002KDW-GP
U42
54 CRT_DDCDATA
54 CRT_DDCCLK
RN57
DAT_DDC1_5_Q
CLK_DDC1_5_Q
7 GMCH_DDCDATA
7 GMCH_DDCCLK
RN53
SRN0J-10-GP-U
DAT_DDC1_5
CLK_DDC1_5
D24
D23
D22
CRT_R_3
CRT_G_3
CRT_B_3
CRT I/F & CONNECTOR
SB 0520
CRT1
VIDEO-15-47-GP-U
20.20392.015
2nd = 20.20764.015
C128
C115
C105
C93
SC18P50V2JN-1-GP
DAT_DDC1_5
CRT_HSYNC1
CRT_VSYNC1
CLK_DDC1_5
C602
SCD01U16V2KX-3GP
R93
35 CRT_DEC#
470R2J-2-GP
SC100P50V2JN-3GP
C98
D21
CRT_IN#_R_3
6 1 7 2 8 3 9 4 10 5
UMA
緯創資通
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
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Title
CRT CONN
Size
Document Number
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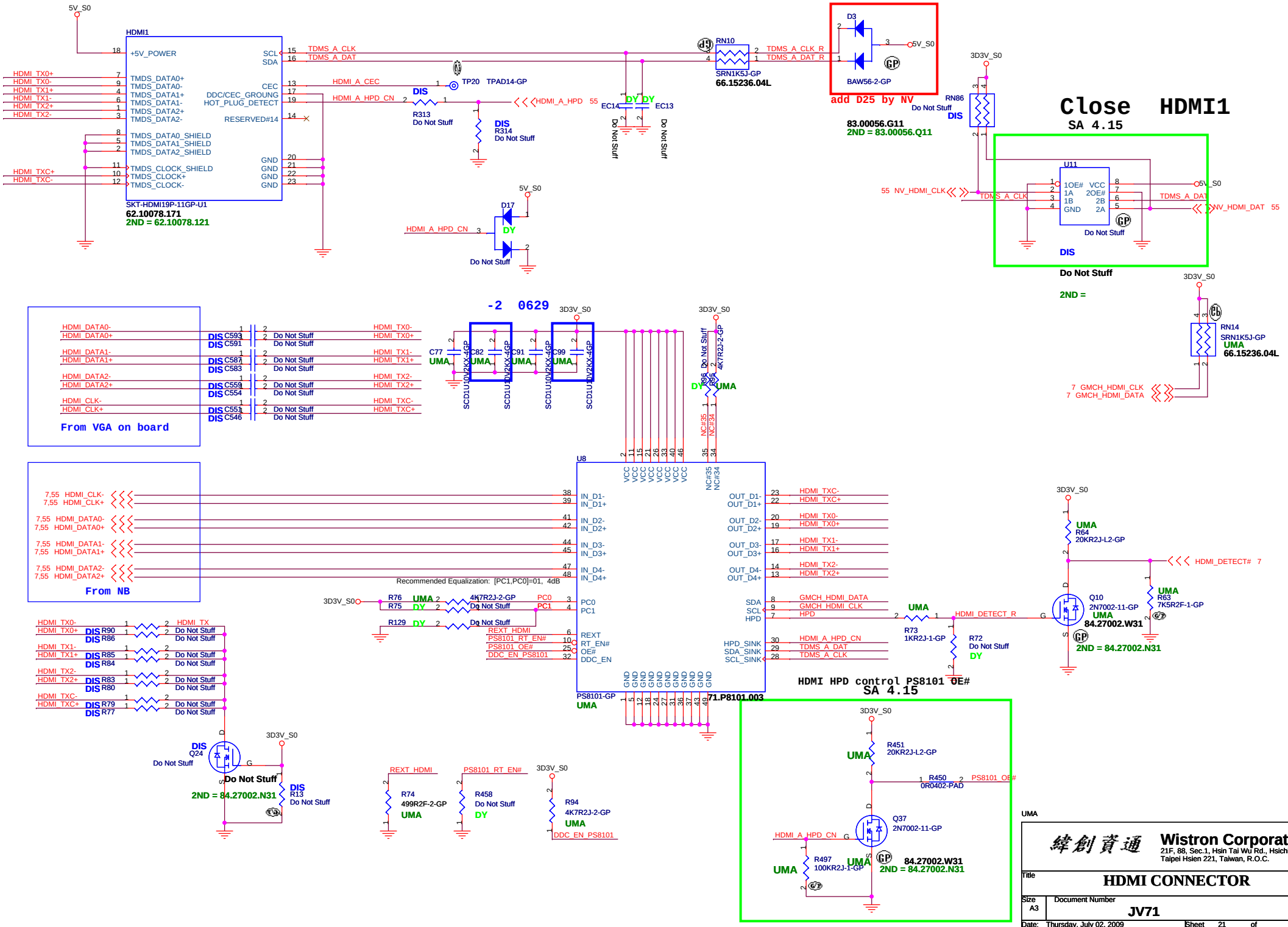
HDMI1
SKT-HDMI19P-11GP-U1
62.10078.171
2ND = 62.10078.121
TP20 TPAD14-GP
RN10
SRN1K5J-GP
66.15236.04L
D3
BAW56-2-GP
add D25 by NV
83.00056.G11
2ND = 83.00056.Q11
RN86
Do Not Stuff
DIS
Close HDMI1
SA 4.15
U11
Do Not Stuff
DIS
Do Not Stuff
2ND =
RN14
SRN1K5J-GP
UMA
66.15236.04L
-2 0629
From VGA on board
From NB
U8
PS8101-GP
UMA
71.P8101.003
Recommended Equalization: [PC1,PC0]=01, 4dB
HDMI HPD control PS8101 OE#
SA 4.15
Q24
Do Not Stuff
2ND = 84.27002.N31
Q10
2N7002-11-GP
UMA
84.27002.W31
2ND = 84.27002.N31
Q37
2N7002-11-GP
UMA
84.27002.W31
2ND = 84.27002.N31
UMA
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.
Title
HDMI CONNECTOR
Size A3
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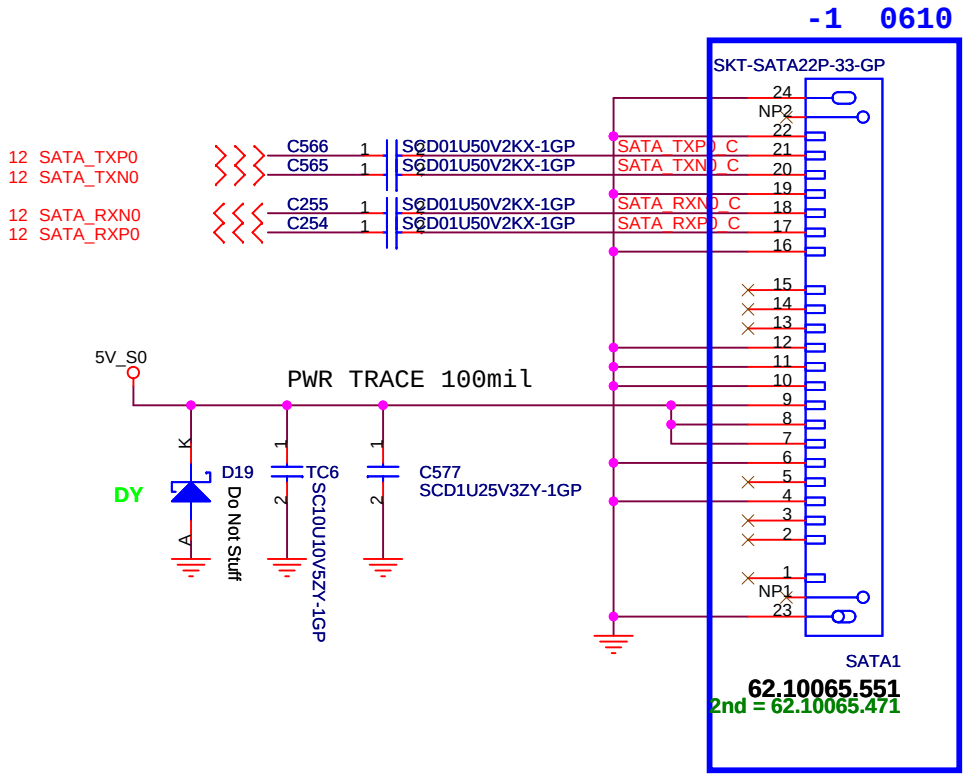
SATA Connector



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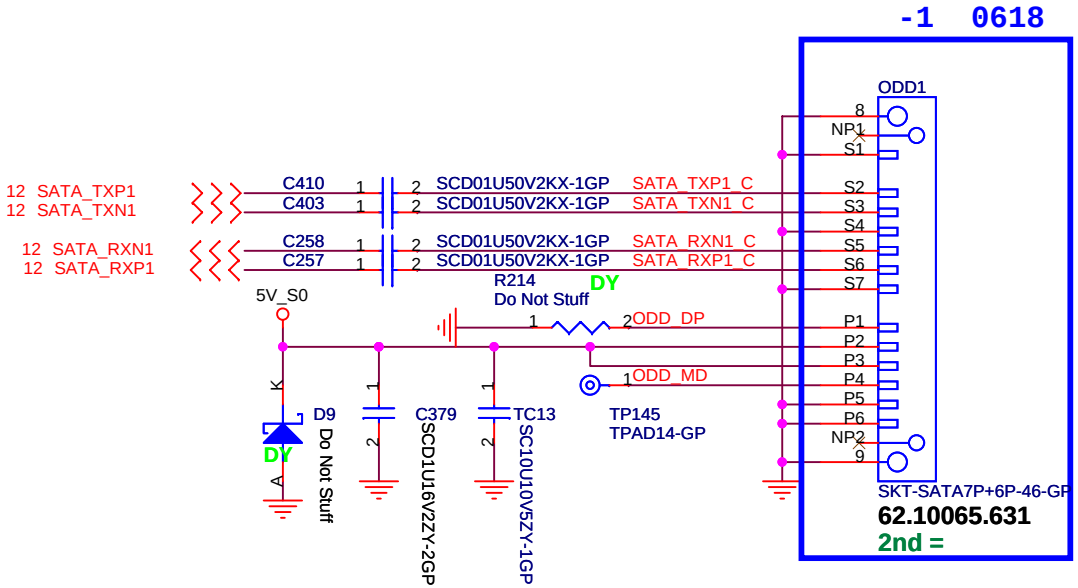
Title	HDD CONN	
Size	Document Number JV71	Rev -2
Date: Thursday, July 02, 2009	Sheet 22 of 60	

ODD Connector



UMA

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Title	***ODD***	
Size	Document Number **JV71**	Rev -2
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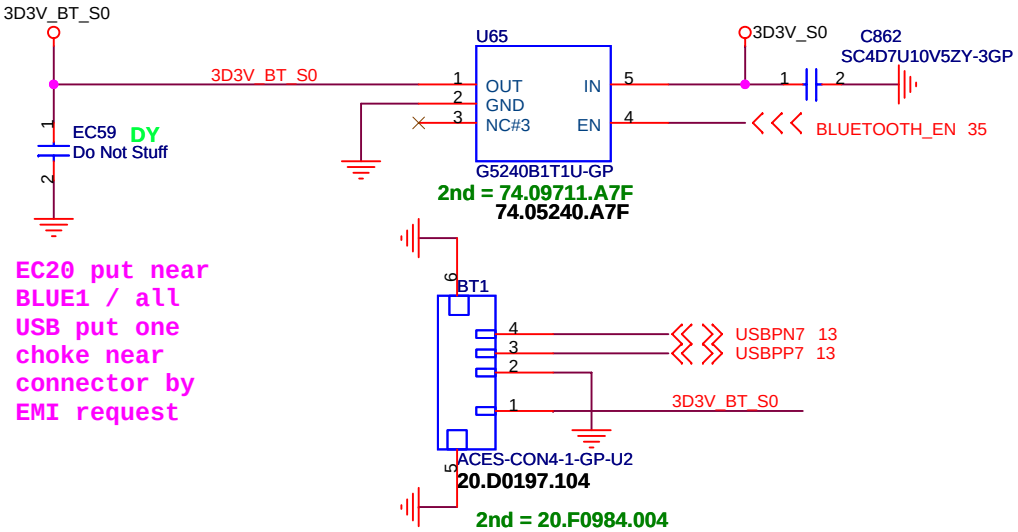
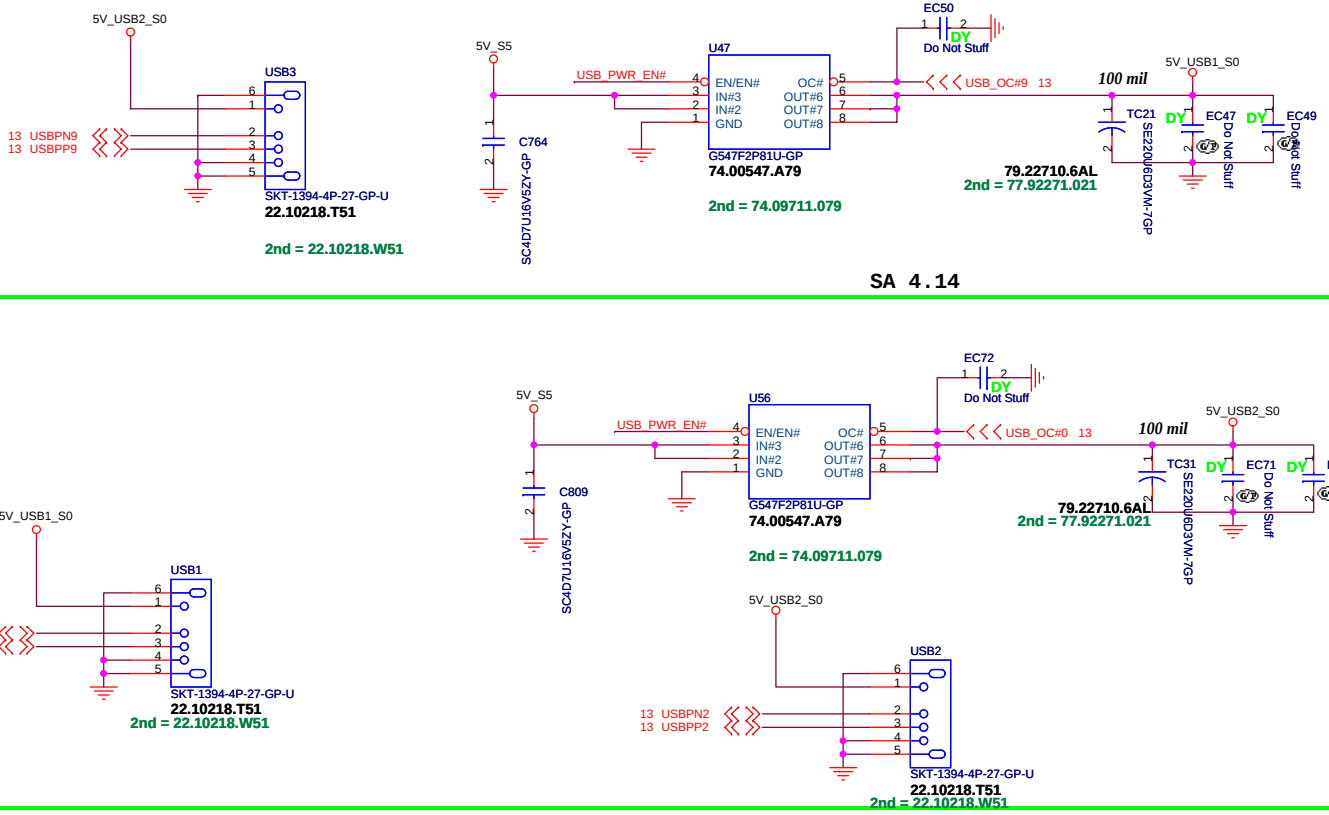
BLUETOOTH MODULE



UMA

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: ***BLUETOOTH***		
Size	Document Number: **JV71**	Rev: -2
Date: Thursday, July 02, 2009	Sheet 24 of 60	



UMA

緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title		
USB CONN		
Size	Document Number	Rev
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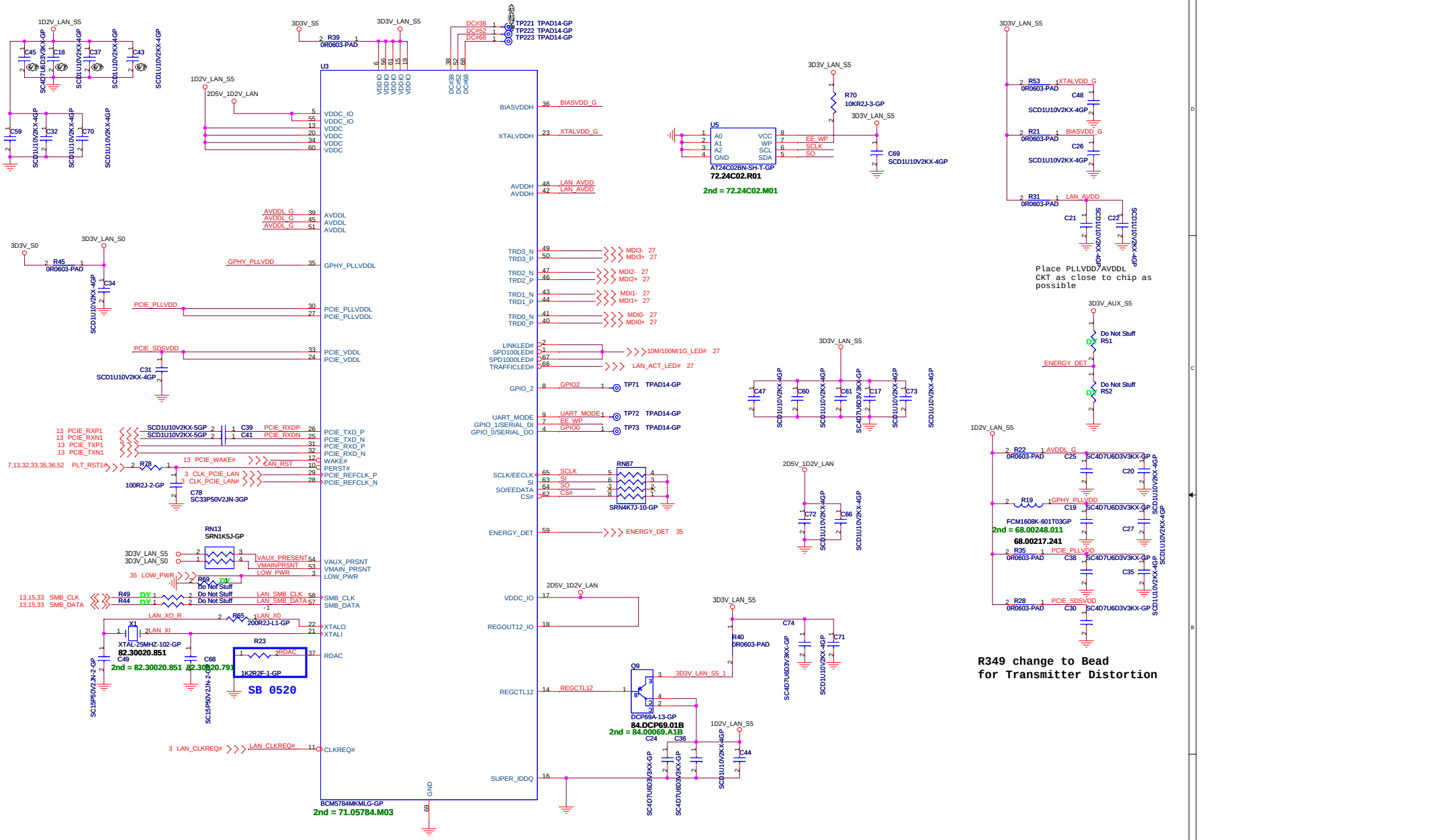
U3
BCM5784MKMLG-GP
2nd = 71.05784.M03
U5
AT24C02BN-SH-T-GP
72.24C02.R01
2nd = 72.24C02.M01
RN87
SRN4K7J-10-GP
RN13
SRN1K5J-GP
Q9
DCP69A-13-GP
84.DCP69.01B
2nd = 84.00069.A1B
X1
XTAL-25MHZ-102-GP
82.30020.851
2nd = 82.30020.851 82.30020.791
SB 0520
Place PLLVDD/AVDDL CKT as close to chip as possible
R349 change to Bead for Transmitter Distortion
UMA
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.
Title
BCM5764
Size Custom
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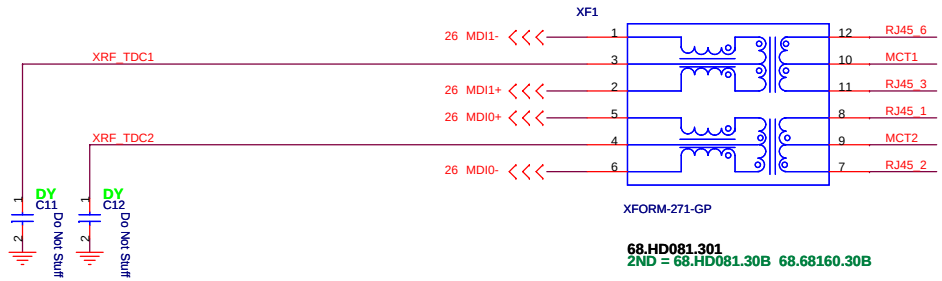
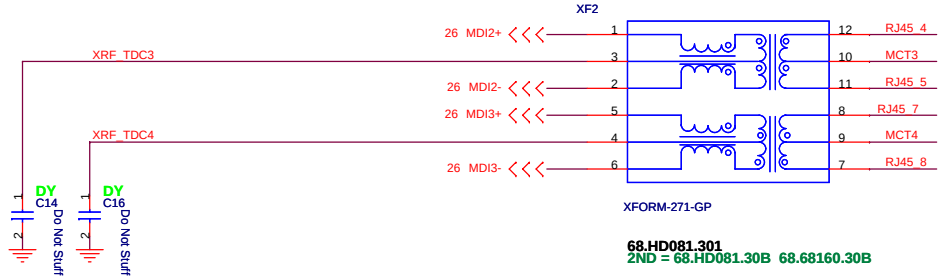
LAN Connector

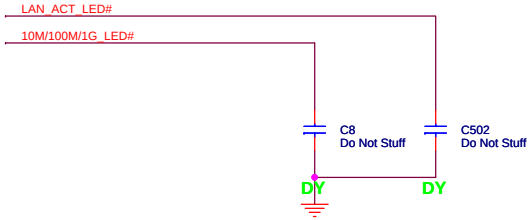
1.route on bottom as differential pairs.
2.Tx+/Tx- are pairs. Rx+/Rx- are pairs.
3.No vias, No 90 degree bends.
4.pairs must be equal lengths.
5.6mil trace width,12mil separation.
6.36mil between pairs and any other trace.
7.Must not cross ground moat,except
RJ-45 moat.

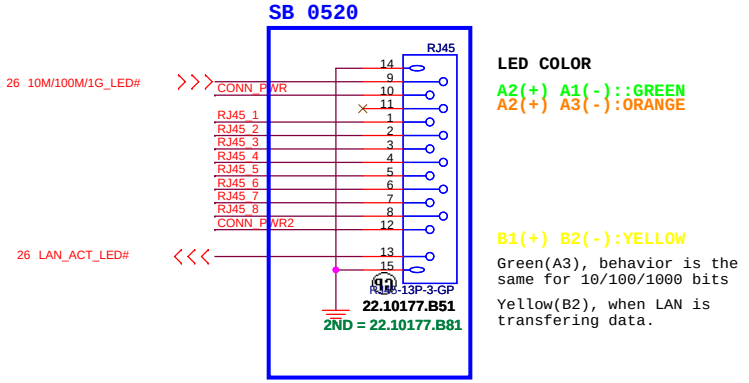
LAN Connector

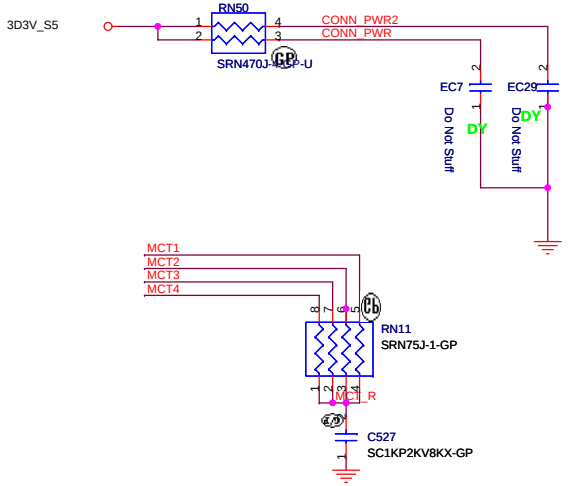
GIGA Lan Transformer











UMA

緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: **LAN CONN**		
Size: A3	Document Number: JV71	Rev: -2
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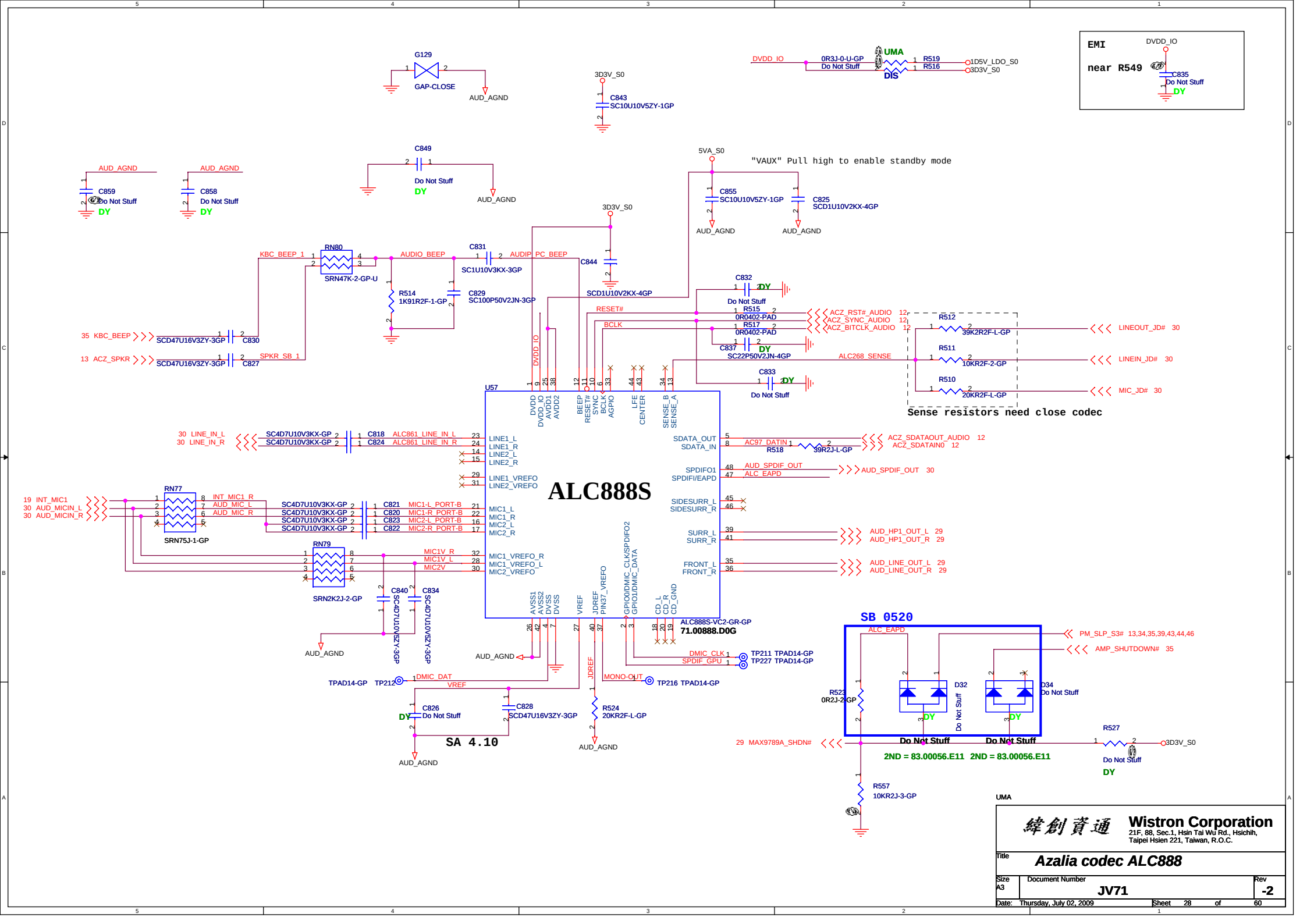
EMI
near R549
DVDD_IO
C835
Do Not Stuff
DY
G129
GAP-CLOSE
AUD_AGND
3D3V_S0
C843
SC10U10V5ZY-1GP
DVDD_IO
0R3J-0-U-GP
Do Not Stuff
UMA
DIS
R519
R516
1D5V_LDO_S0
3D3V_S0
C849
Do Not Stuff
DY
5VA_S0
"VAUX" Pull high to enable standby mode
C855
SC10U10V5ZY-1GP
C825
SCD1U10V2KX-4GP
C859
C858
C831
SC1U10V3KX-3GP
C844
SCD1U10V2KX-4GP
C832
Do Not Stuff
KBC_BEEP_1
RN80
SRN47K-2-GP-U
AUDIO_BEEP
AUDIP_PC_BEEP
R514
1K91R2F-1-GP
C829
SC100P50V2JN-3GP
RESET#
BCLK
R515
0R0402-PAD
R517
0R0402-PAD
ACZ_RST#_AUDIO 12
ACZ_SYNC_AUDIO 12
ACZ_BITCLK_AUDIO 12
C837
SC22P50V2JN-4GP
ALC268_SENSE
C833
Do Not Stuff
R512
39K2R2F-L-GP
R511
10KR2F-2-GP
R510
20KR2F-L-GP
LINEOUT_JD# 30
LINEIN_JD# 30
MIC_JD# 30
Sense resistors need close codec
35 KBC_BEEP
13 ACZ_SPKR
SCD47U16V3ZY-3GP
C830
C827
SPKR_SB_1
U57
ALC888S
DVDD
DVDD_IO
AVDD1
AVDD2
BEEP
RESET#
SYNC
BCLK
AGPIO
LFE
CENTER
SENSE_B
SENSE_A
30 LINE_IN_L
30 LINE_IN_R
SC4D7U10V3KX-GP
C818
C824
ALC861_LINE_IN_L
ALC861_LINE_IN_R
LINE1_L
LINE1_R
LINE2_L
LINE2_R
LINE1_VREFO
LINE2_VREFO
SDATA_OUT
SDATA_IN
AC97_DATIN
R518
39R2J-L-GP
ACZ_SDATAOUT_AUDIO 12
ACZ_SDATAIN0 12
SPDIFO1
SPDIFI/EAPD
AUD_SPDIF_OUT
ALC_EAPD
AUD_SPDIF_OUT 30
SIDESURR_L
SIDESURR_R
SURR_L
SURR_R
AUD_HP1_OUT_L 29
AUD_HP1_OUT_R 29
FRONT_L
FRONT_R
AUD_LINE_OUT_L 29
AUD_LINE_OUT_R 29
19 INT_MIC1
30 AUD_MICIN_L
30 AUD_MICIN_R
RN77
SRN75J-1-GP
INT_MIC1_R
AUD_MIC_L
AUD_MIC_R
C821
C820
C823
C822
MIC1-L_PORT-B
MIC1-R_PORT-B
MIC2-L_PORT-B
MIC2-R_PORT-B
MIC1_L
MIC1_R
MIC2_L
MIC2_R
RN79
SRN2K2J-2-GP
MIC1V_R
MIC1V_L
MIC2V
MIC1_VREFO_R
MIC1_VREFO_L
MIC2_VREFO
C840
C834
SC4P47U50V-3GP
SC4D7U10V3ZY-3GP
AVSS1
AVSS2
DVSS
DVSS
VREF
JDREF
PIN37_VREFO
GPIO0/DMIC_CLK/SPDIFO2
GPIO1/DMIC_DATA
CD_L
CD_R
CD_GND
ALC888S-VC2-GR-GP
71.00888.D0G
AUD_AGND
DMIC_CLK
SPDIF_GPU
TP211 TPAD14-GP
TP227 TPAD14-GP
TPAD14-GP
TP212
DMIC_DAT
VREF
MONO-OUT
TP216 TPAD14-GP
C826
Do Not Stuff
C828
SCD47U16V3ZY-3GP
R524
20KR2F-L-GP
SA 4.10
SB 0520
ALC_EAPD
PM_SLP_S3# 13,34,35,39,43,44,46
AMP_SHUTDOWN# 35
R523
0R2J-2-GP
D32
Do Not Stuff
D34
Do Not Stuff
29 MAX9789A_SHDN#
R527
3D3V_S0
Do Not Stuff
DY
2ND = 83.00056.E11
2ND = 83.00056.E11
R557
10KR2J-3-GP
UMA
緯創資通
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.
Title
Azalia codec ALC888
Size
A3
Document Number
JV71
Rev
-2
Date: Thursday, July 02, 2009
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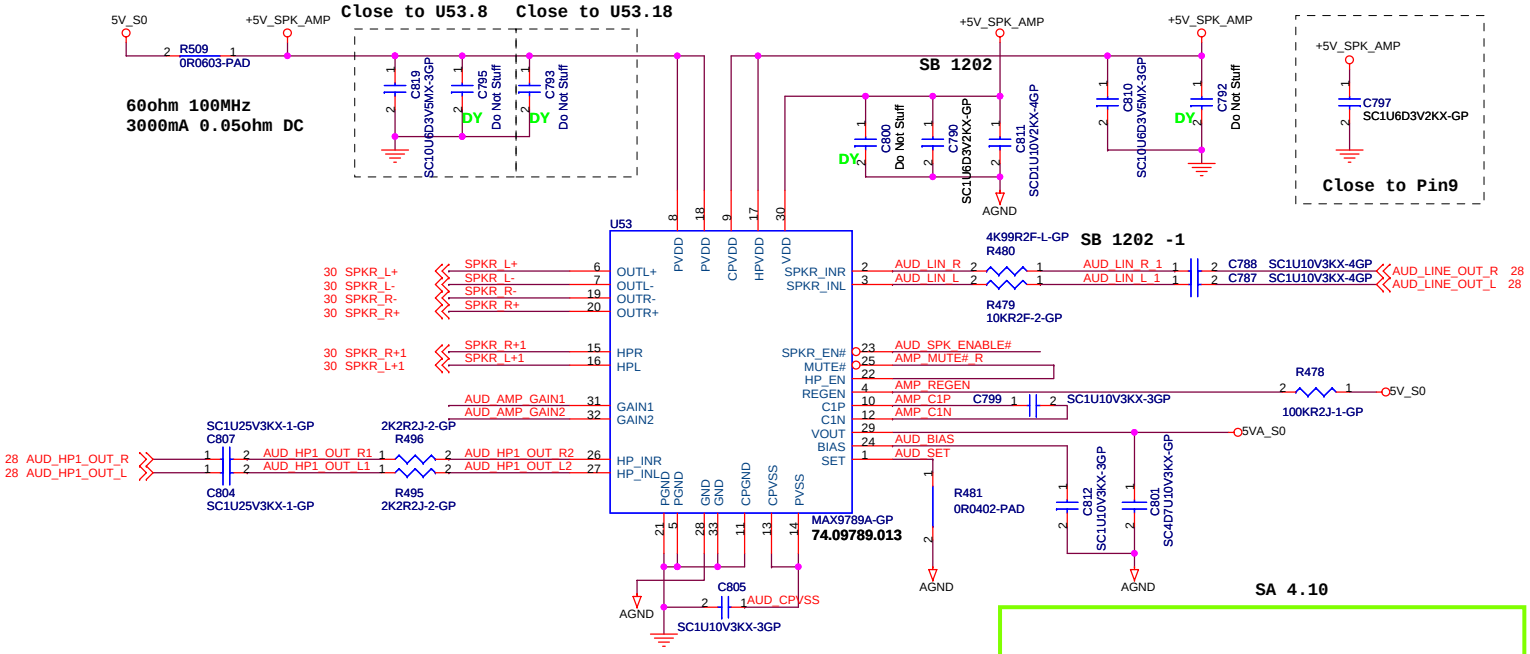
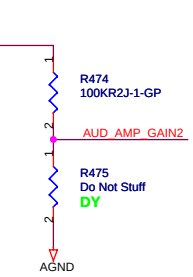
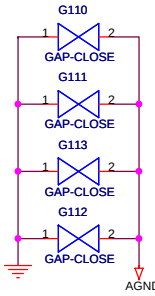
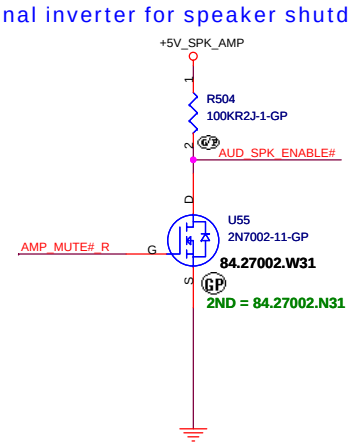




GAIN1	GAIN2	GAIN
0	0	6dB
0	1	10dB
1	0	15.6dB
1	1	21.6dB





UMA

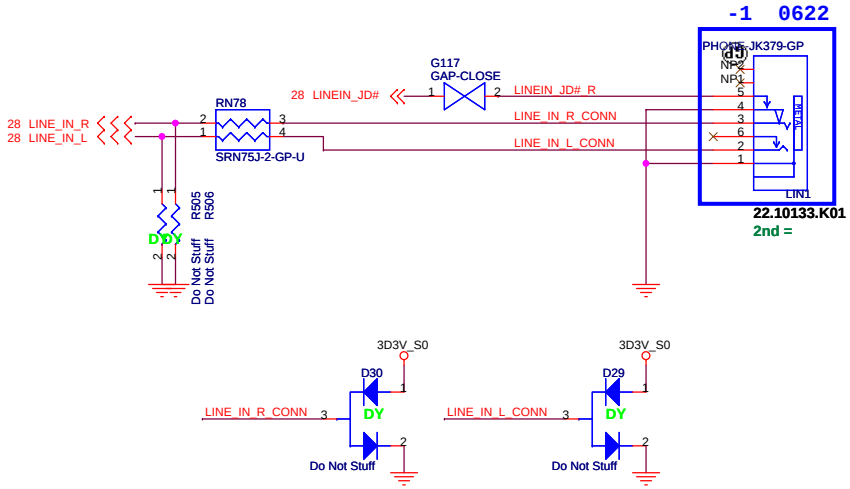
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: AUDIO AMP

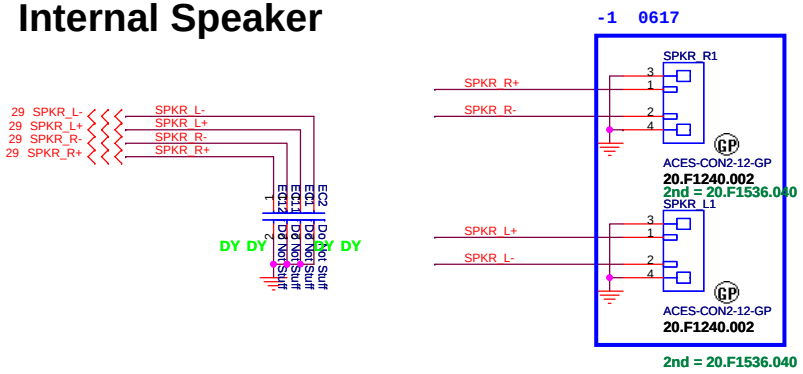
Size | Document Number: JV71 | Rev: -2

Date: Thursday, July 02, 2009 | Sheet 29 of 60

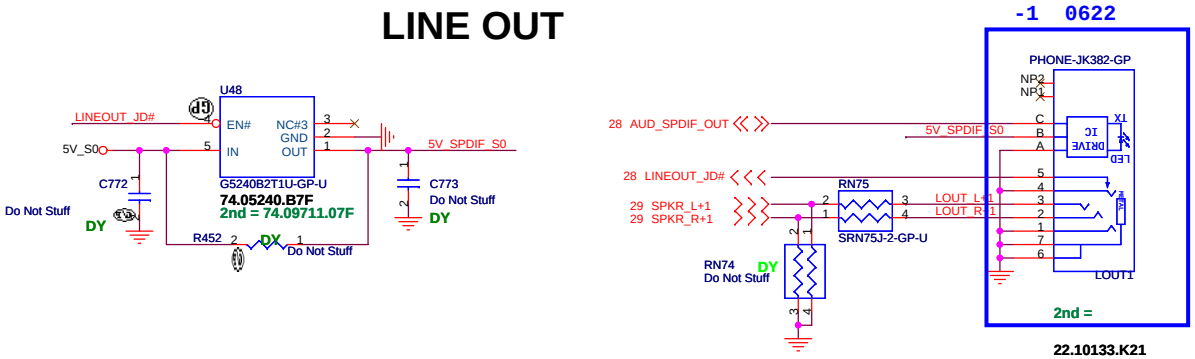
LINE IN

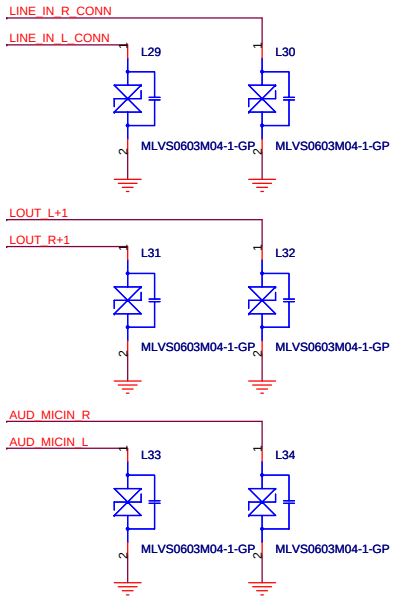


Internal Speaker

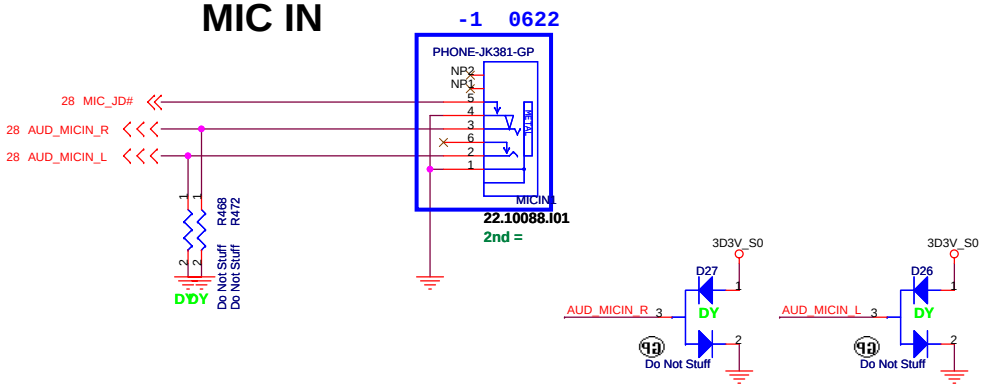


LINE OUT





MIC IN



UMA

緯創資通	**Wistron Corporation** 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title	*AUDIO jack*	
Size	Document Number JV71	Rev -2
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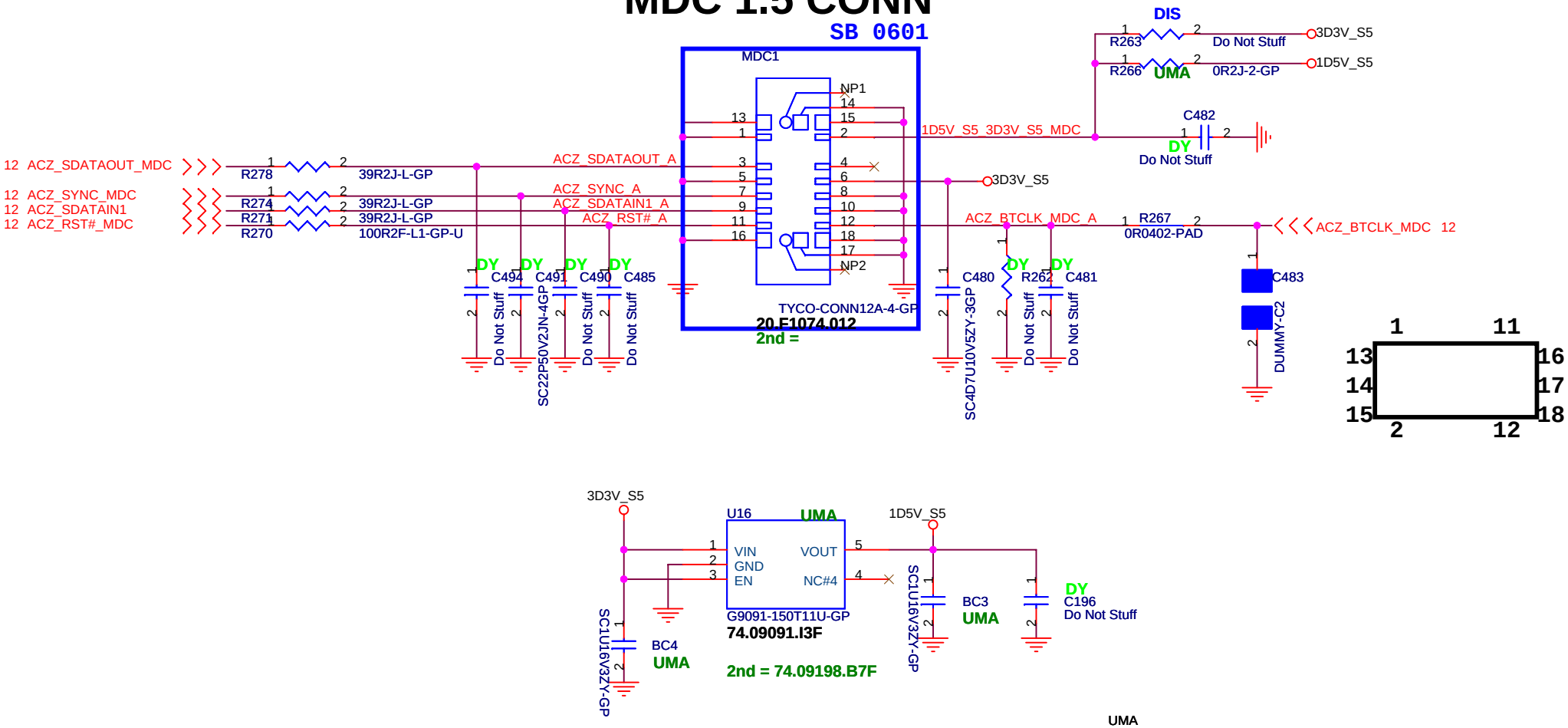
MDC 1.5 CONN

SB 0601



UMA

緯創資通	**Wistron Corporation** 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title	***MDC***	
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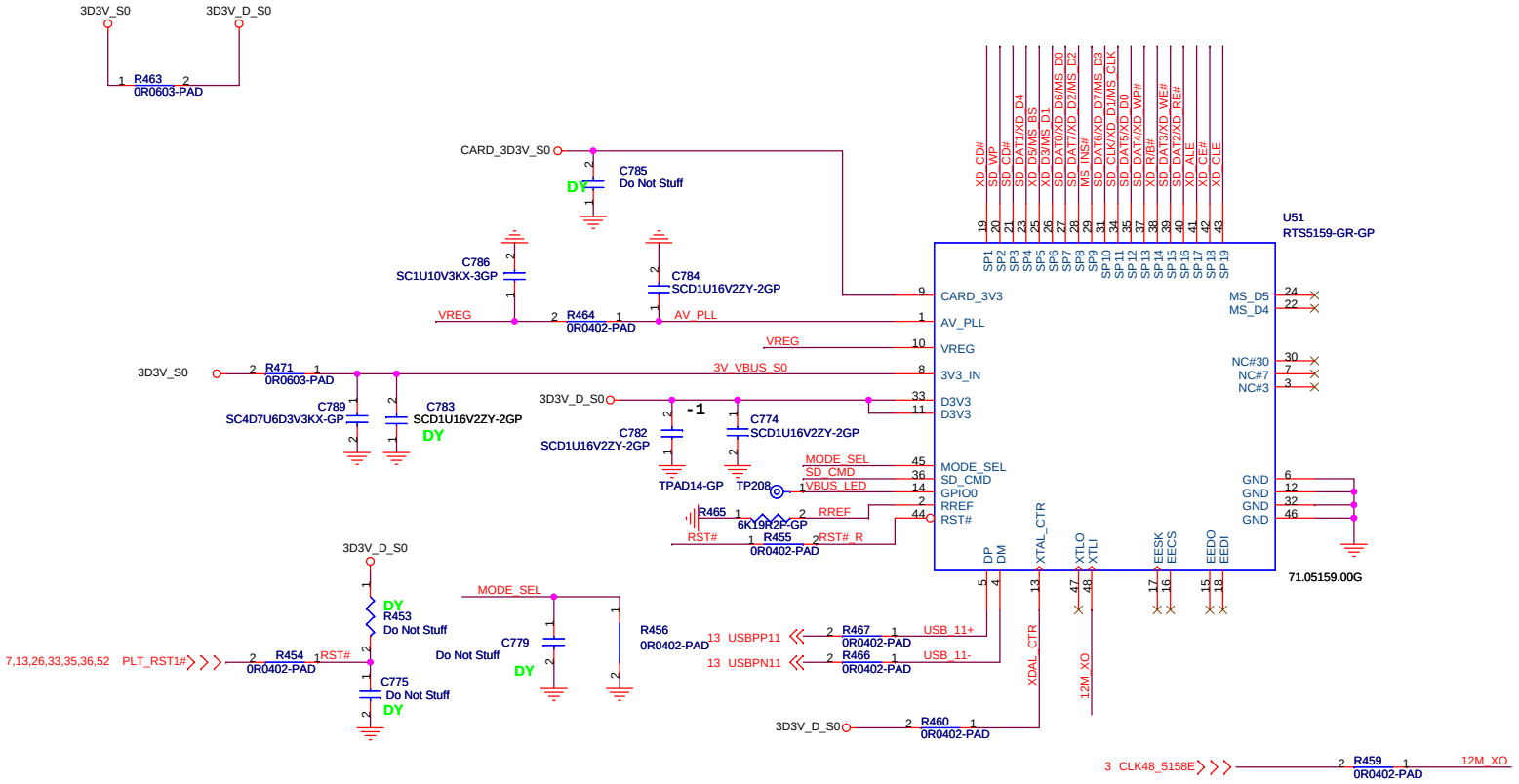

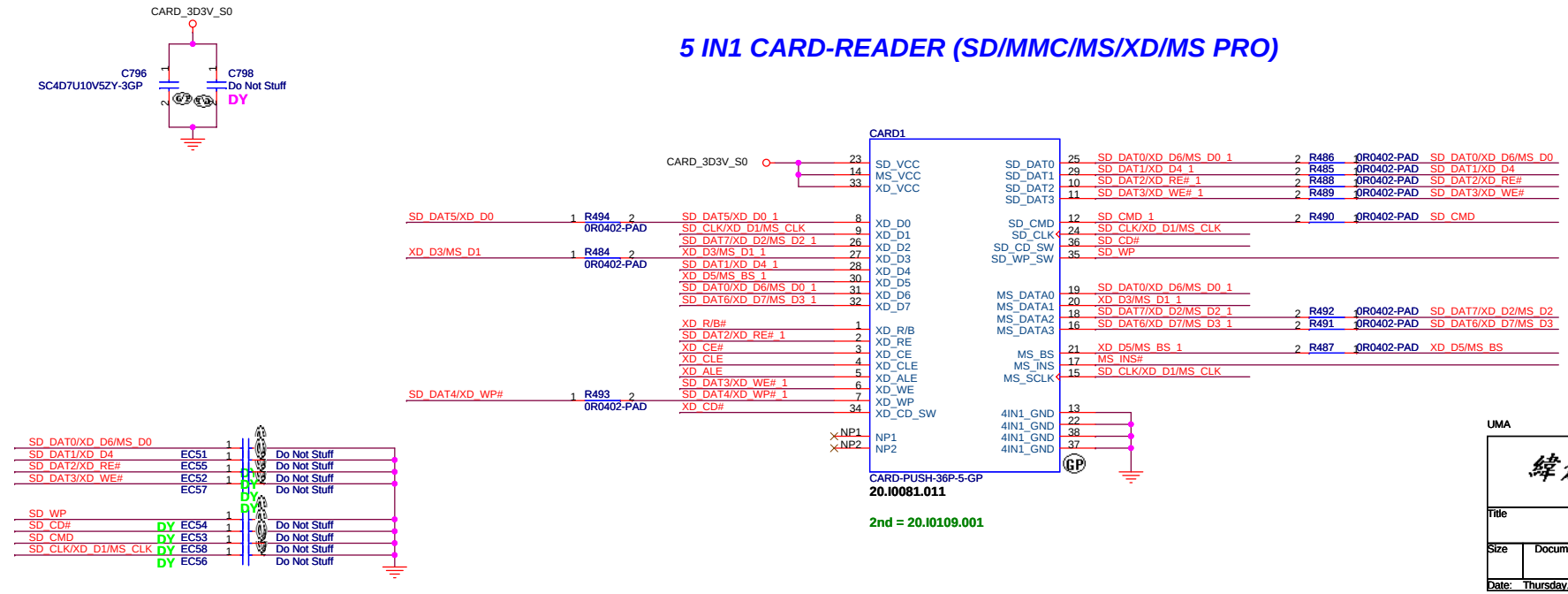

UMA

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: Cardreader RTS5159

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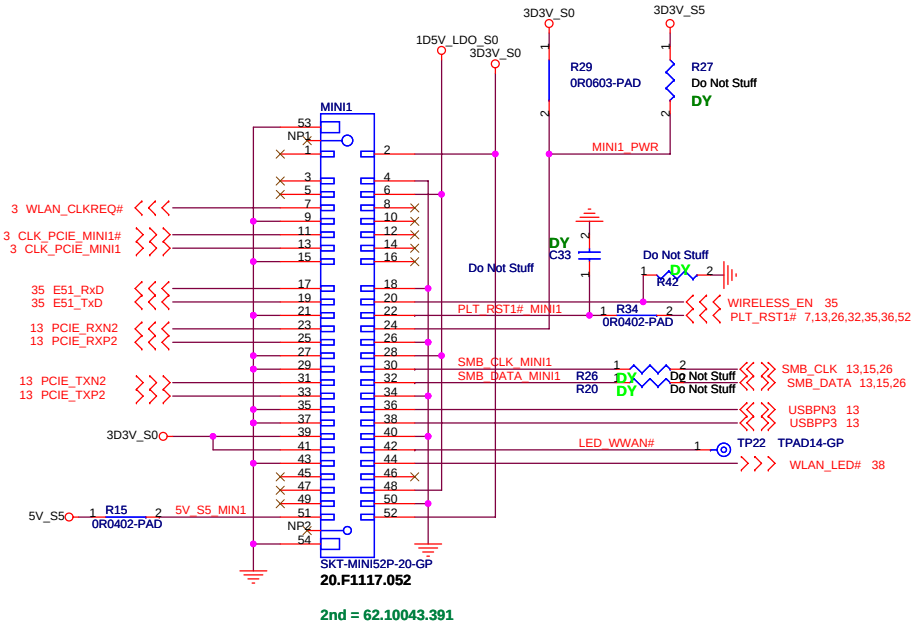
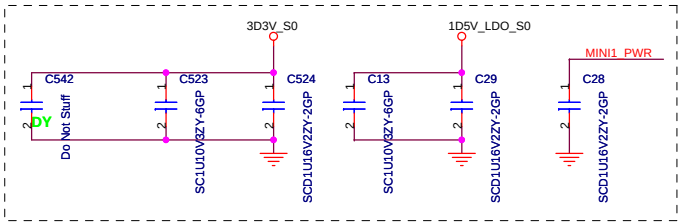
Mini Card Connector(WLAN)
Support debug-card



Place near MINI1



Mini Card Connector

UMA

緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: MINI CARD		
Size: A3	Document Number: JV71	Rev: -2
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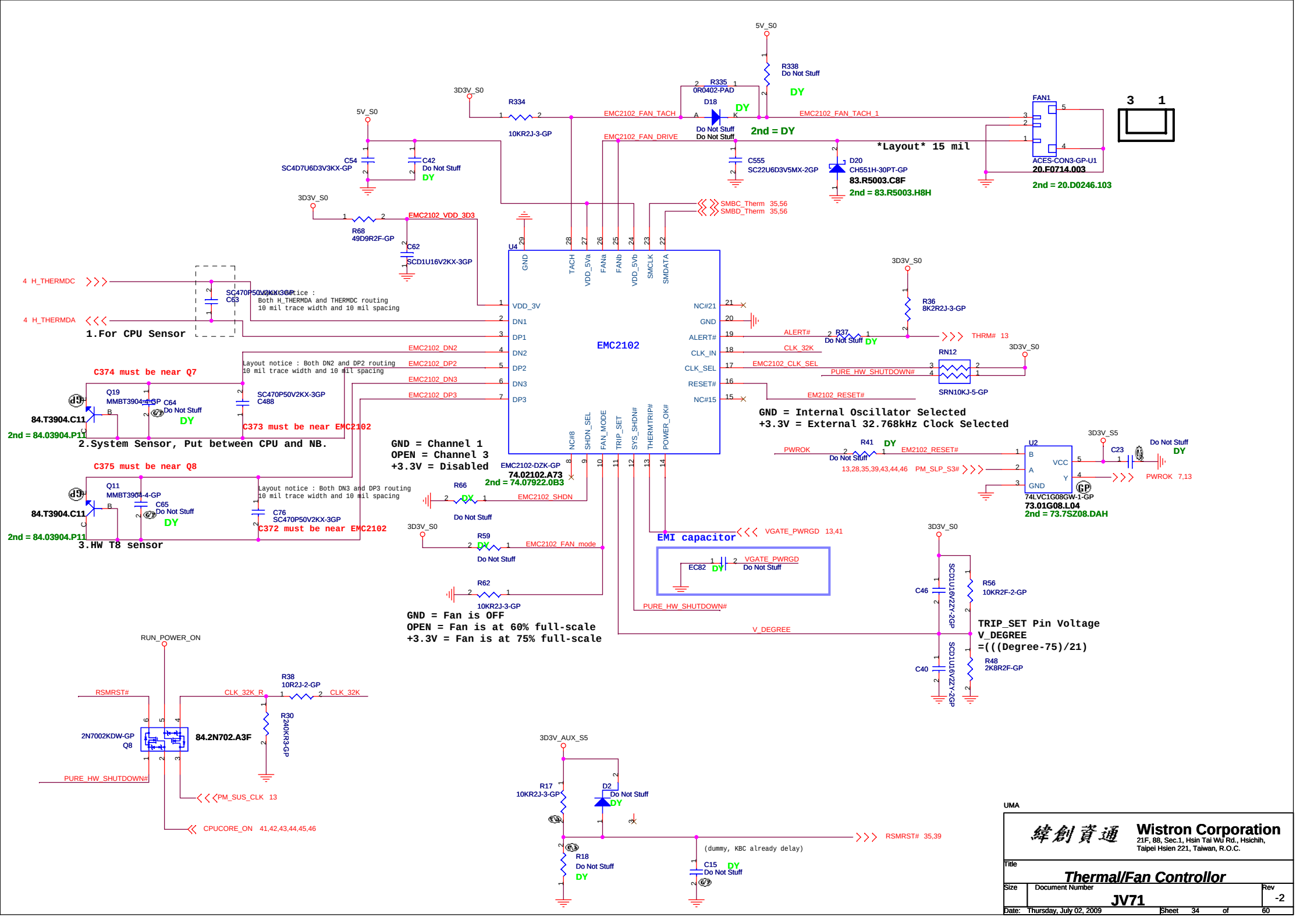
5V_S0
R338
Do Not Stuff
DY
3D3V_S0
R334
10KR2J-3-GP
R335
0R0402-PAD
D18
DY
EMC2102_FAN_TACH
EMC2102_FAN_TACH_1
Do Not Stuff
Do Not Stuff
2nd = DY
EMC2102_FAN_DRIVE
FAN1
Layout 15 mil
ACES-CON3-GP-U1
20.F0714.003
2nd = 20.D0246.103
C54
SC4D7U6D3V3KX-GP
C42
Do Not Stuff
DY
C555
SC22U6D3V5MX-2GP
D20
CH551H-30PT-GP
83.R5003.C8F
2nd = 83.R5003.H8H
3D3V_S0
R68
49D9R2F-GP
EMC2102_VDD_3D3
C62
SCD1U16V2KX-3GP
SMBC_Therm 35,56
SMBD_Therm 35,56
U4
GND
TACH
VDD_5Va
FANa
FANb
VDD_5Vb
SMCLK
SMDATA
4 H_THERMDC
4 H_THERMDA
SC470P50V2KX-3GP
C63
Layout notice :
Both H_THERMDA and THERMDC routing
10 mil trace width and 10 mil spacing
1.For CPU Sensor
VDD_3V
DN1
DP1
DN2
DP2
DN3
DP3
EMC2102
NC#21
GND
ALERT#
CLK_IN
CLK_SEL
RESET#
NC#15
3D3V_S0
R36
8K2R2J-3-GP
R37
Do Not Stuff
DY
ALERT#
THRM# 13
CLK_32K
EMC2102_CLK_SEL
PURE_HW_SHUTDOWN#
RN12
SRN10KJ-5-GP
EM2102_RESET#
GND = Internal Oscillator Selected
+3.3V = External 32.768kHz Clock Selected
EMC2102_DN2
EMC2102_DP2
EMC2102_DN3
EMC2102_DP3
Layout notice : Both DN2 and DP2 routing
10 mil trace width and 10 mil spacing
C374 must be near Q7
Q19
MMBT3904-4-GP
C64
Do Not Stuff
DY
84.T3904.C11
2nd = 84.03904.P11
SC470P50V2KX-3GP
C488
C373 must be near EMC2102
2.System Sensor, Put between CPU and NB.
GND = Channel 1
OPEN = Channel 3
+3.3V = Disabled
NC#8
SHDN_SEL
FAN_MODE
TRIP_SET
SYS_SHDN#
THERMTRIP#
POWER_OK#
EMC2102-DZK-GP
74.02102.A73
2nd = 74.07922.0B3
PWROK
R41
DY
Do Not Stuff
EM2102_RESET#
13,28,35,39,43,44,46 PM_SLP_S3#
U2
VCC
GND
74LVC1G08GW-1-GP
73.01G08.L04
2nd = 73.7S08.DAH
3D3V_S5
C23
Do Not Stuff
DY
PWROK 7,13
C375 must be near Q8
Q11
MMBT3904-4-GP
C65
Do Not Stuff
DY
84.T3904.C11
2nd = 84.03904.P11
3.HW T8 sensor
Layout notice : Both DN3 and DP3 routing
10 mil trace width and 10 mil spacing
C76
SC470P50V2KX-3GP
C372 must be near EMC2102
R66
DY
Do Not Stuff
EMC2102_SHDN
3D3V_S0
R59
DY
Do Not Stuff
EMC2102_FAN_mode
R62
10KR2J-3-GP
EMI capacitor
VGATE_PWRGD 13,41
EC82
DY
VGATE_PWRGD
Do Not Stuff
PURE_HW_SHUTDOWN#
V_DEGREE
GND = Fan is OFF
OPEN = Fan is at 60% full-scale
+3.3V = Fan is at 75% full-scale
3D3V_S0
C46
SCD1U16V2ZY-2GP
R56
10KR2F-2-GP
TRIP_SET Pin Voltage
V_DEGREE
=(((Degree-75)/21)
C40
SCD1U16V2ZY-2GP
R48
2K8R2F-GP
RUN_POWER_ON
RSMRST#
CLK_32K_R
R38
10R2J-2-GP
CLK_32K
2N7002KDW-GP
Q8
84.2N702.A3F
R30
240KR3-GP
PURE_HW_SHUTDOWN#
PM_SUS_CLK 13
CPUCORE_ON 41,42,43,44,45,46
3D3V_AUX_S5
R17
10KR2J-3-GP
D2
Do Not Stuff
DY
R18
Do Not Stuff
DY
C15
Do Not Stuff
DY
(dummy, KBC already delay)
RSMRST# 35,39
UMA
緯創資通
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.
Title
Thermal/Fan Controllor
Size
Document Number
JV71
Rev
-2
Date: Thursday, July 02, 2009
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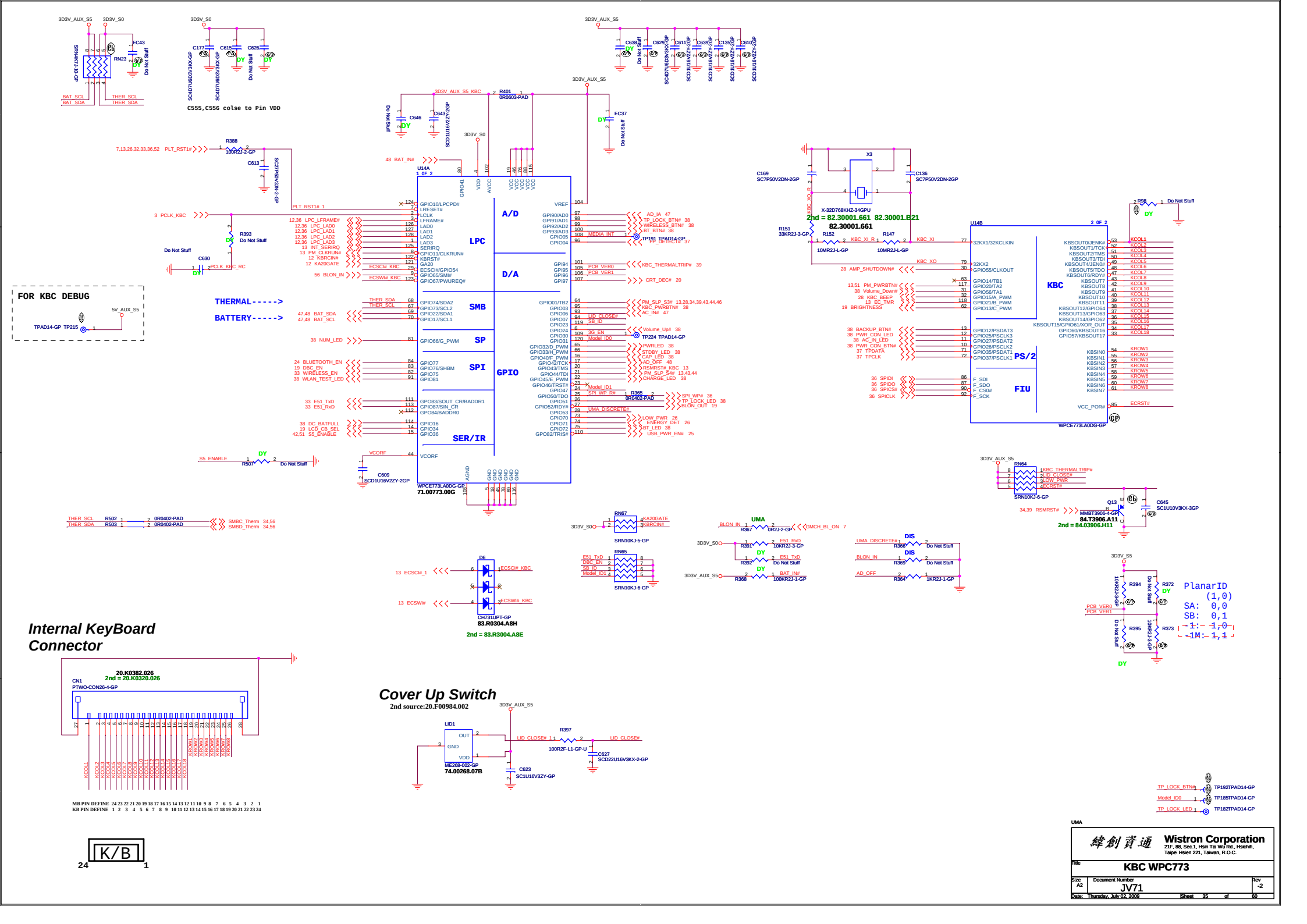

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: KBC WPC773

Size	Document Number	Rev
A2	JV71	-2

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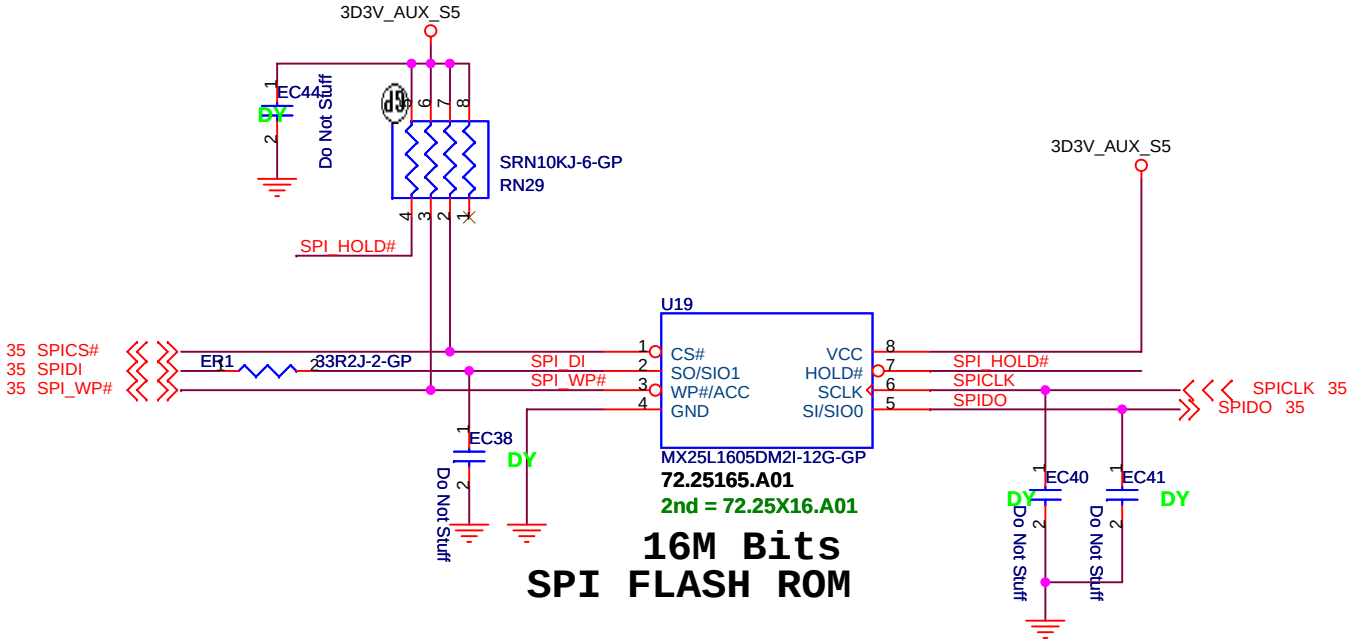
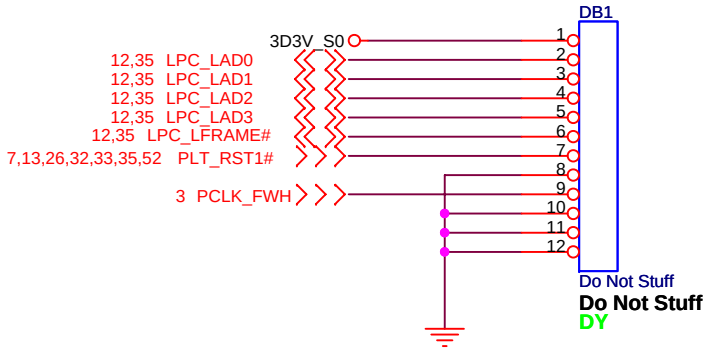


GOLDEN FINGER FOR DEBUG BOARD



UMA

緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

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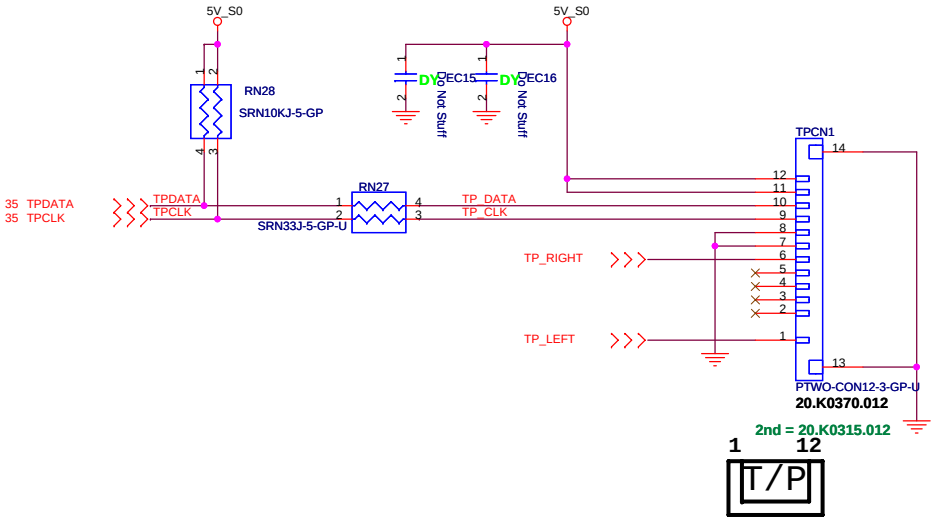
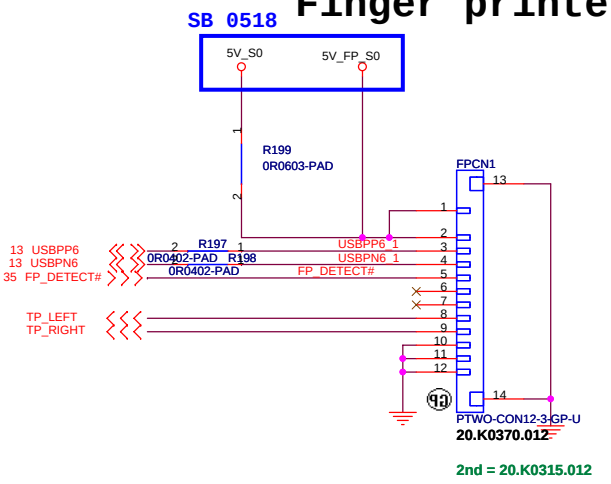
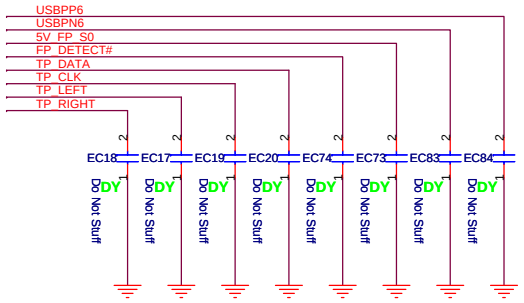
TOUCH PAD



Finger printer





UMA

緯創資通 Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.		
Title: Touch PAD and FP		
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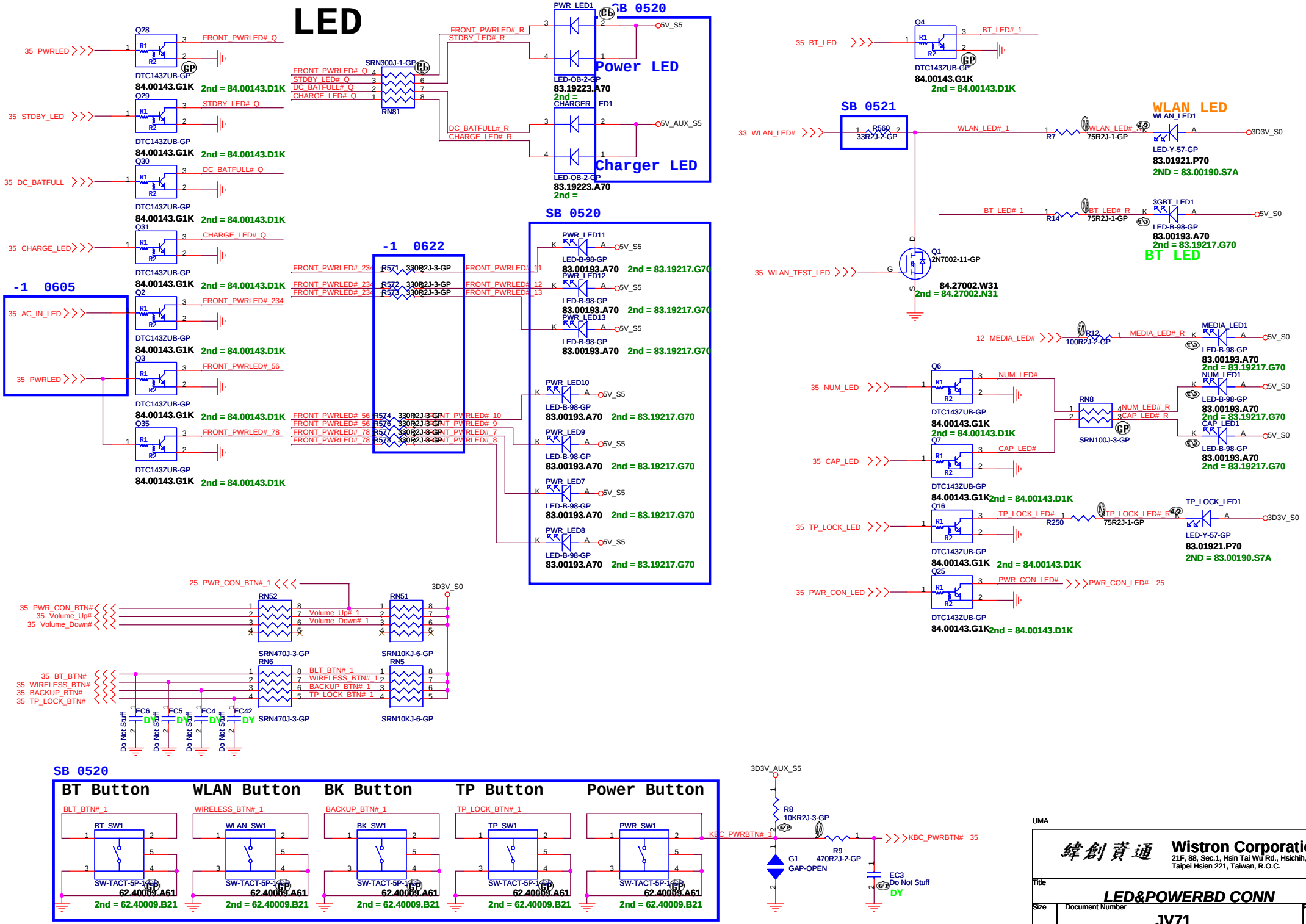
LED


SB 0520
Power LED
Charger LED
SB 0521
WLAN LED
BT LED
-1 0605
-1 0622
SB 0520
BT Button
WLAN Button
BK Button
TP Button
Power Button
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.
LED&POWERBD CONN
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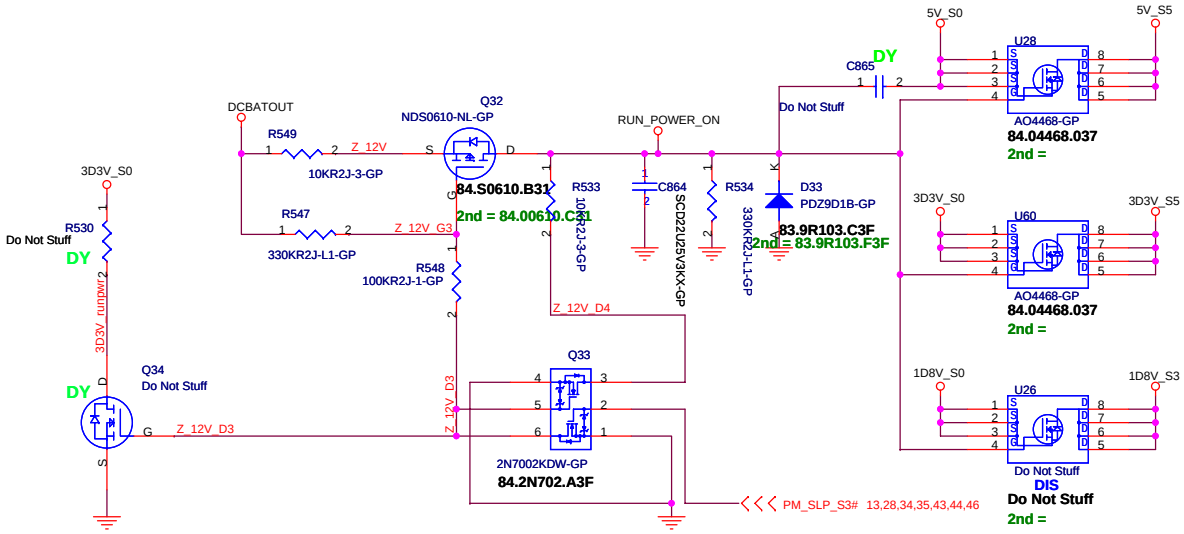
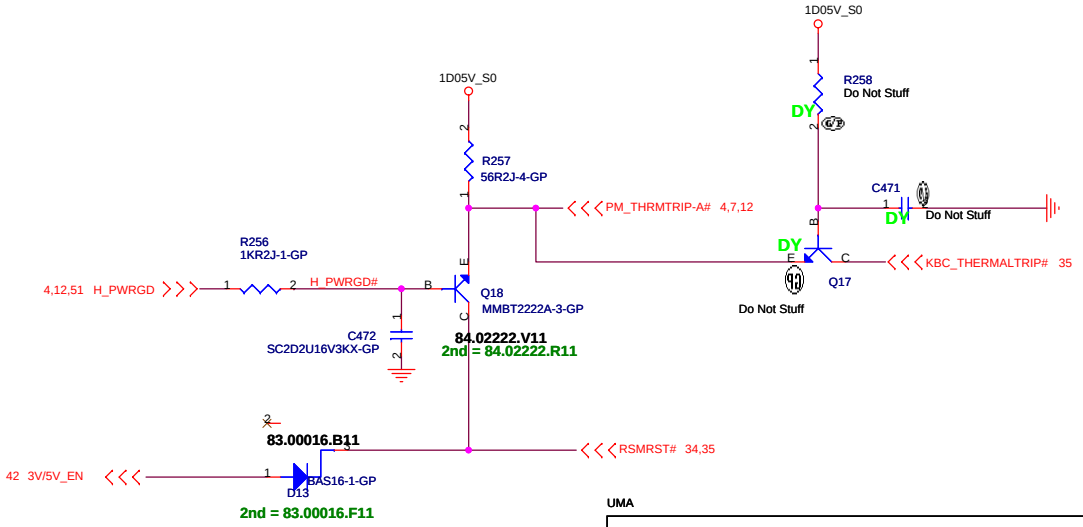
Run Power





UMA

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Title	RUN POWER and 3D3V_AUX_S5	
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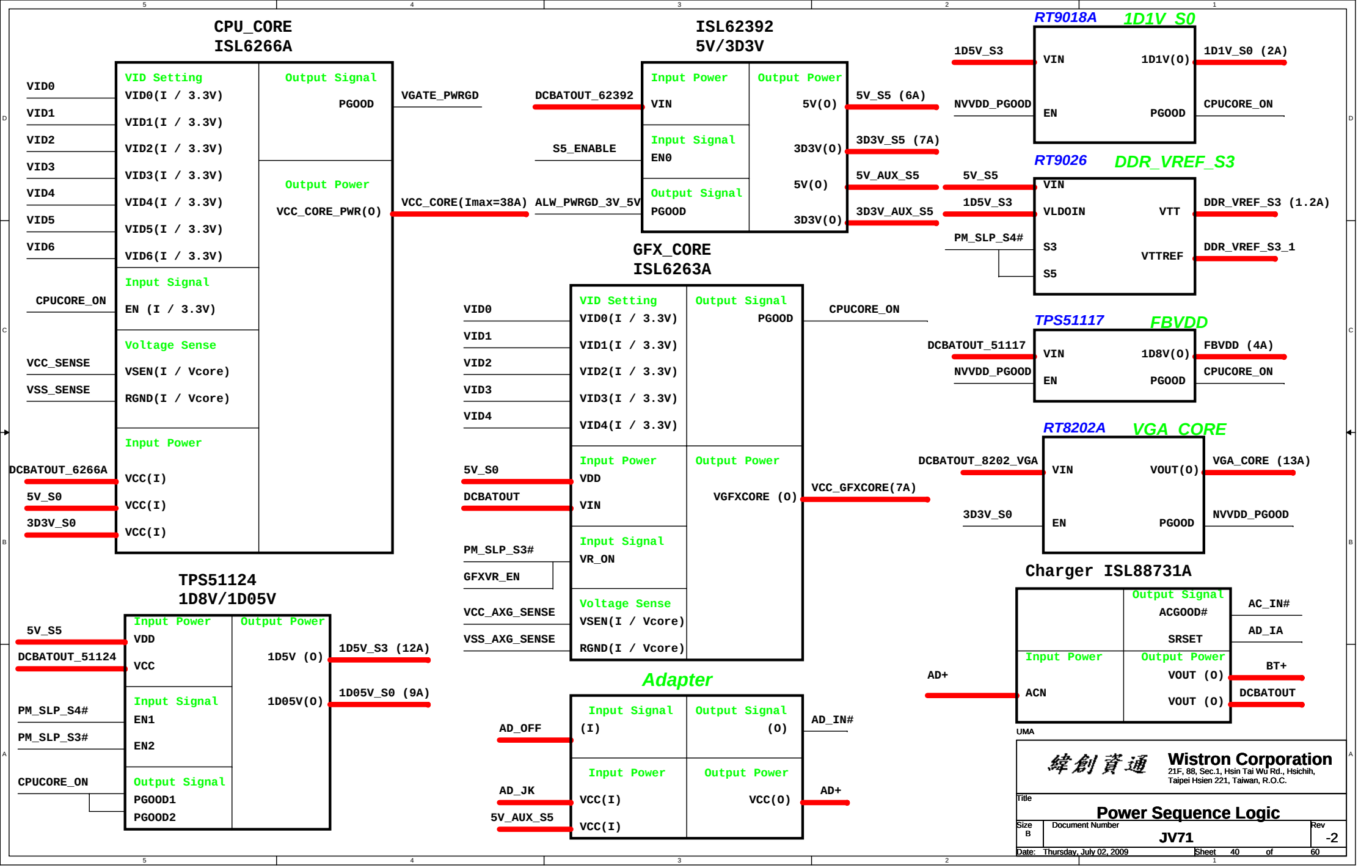
CPU_CORE
ISL6266A
VID Setting
VID0(I / 3.3V)
VID1(I / 3.3V)
VID2(I / 3.3V)
VID3(I / 3.3V)
VID4(I / 3.3V)
VID5(I / 3.3V)
VID6(I / 3.3V)
Input Signal
EN (I / 3.3V)
Voltage Sense
VSEN(I / Vcore)
RGND(I / Vcore)
Input Power
VCC(I)
VCC(I)
VCC(I)
Output Signal
PGOOD
Output Power
VCC_CORE_PWR(O)
VID0
VID1
VID2
VID3
VID4
VID5
VID6
CPUCORE_ON
VCC_SENSE
VSS_SENSE
DCBATOUT_6266A
5V_S0
3D3V_S0
VGATE_PWRGD
VCC_CORE(Imax=38A)
ISL62392
5V/3D3V
Input Power
VIN
Input Signal
EN0
Output Signal
PGOOD
Output Power
5V(O)
3D3V(O)
5V(O)
3D3V(O)
DCBATOUT_62392
S5_ENABLE
ALW_PWRGD_3V_5V
5V_S5 (6A)
3D3V_S5 (7A)
5V_AUX_S5
3D3V_AUX_S5
RT9018A
1D1V_S0
VIN
EN
1D1V(O)
PGOOD
1D5V_S3
NVVDD_PGOOD
1D1V_S0 (2A)
CPUCORE_ON
RT9026
DDR_VREF_S3
VIN
VLDOIN
S3
S5
VTT
VTTREF
5V_S5
1D5V_S3
PM_SLP_S4#
DDR_VREF_S3 (1.2A)
DDR_VREF_S3_1
GFX_CORE
ISL6263A
VID Setting
VID0(I / 3.3V)
VID1(I / 3.3V)
VID2(I / 3.3V)
VID3(I / 3.3V)
VID4(I / 3.3V)
Input Power
VDD
VIN
Input Signal
VR_ON
Voltage Sense
VSEN(I / Vcore)
RGND(I / Vcore)
Output Signal
PGOOD
Output Power
VGFXCORE (O)
VID0
VID1
VID2
VID3
VID4
5V_S0
DCBATOUT
PM_SLP_S3#
GFXVR_EN
VCC_AXG_SENSE
VSS_AXG_SENSE
CPUCORE_ON
VCC_GFXCORE(7A)
TPS51117
FBVDD
VIN
EN
1D8V(O)
PGOOD
DCBATOUT_51117
NVVDD_PGOOD
FBVDD (4A)
CPUCORE_ON
RT8202A
VGA_CORE
VIN
EN
VOUT(O)
PGOOD
DCBATOUT_8202_VGA
3D3V_S0
VGA_CORE (13A)
NVVDD_PGOOD
TPS51124
1D8V/1D05V
Input Power
VDD
VCC
Input Signal
EN1
EN2
Output Signal
PGOOD1
PGOOD2
Output Power
1D5V (O)
1D05V(O)
5V_S5
DCBATOUT_51124
PM_SLP_S4#
PM_SLP_S3#
CPUCORE_ON
1D5V_S3 (12A)
1D05V_S0 (9A)
Adapter
Input Signal
(I)
Input Power
VCC(I)
VCC(I)
Output Signal
(O)
Output Power
VCC(O)
AD_OFF
AD_JK
5V_AUX_S5
AD_IN#
AD+
Charger ISL88731A
Input Power
ACN
Output Signal
ACGOOD#
SRSET
Output Power
VOUT (O)
VOUT (O)
AD+
AC_IN#
AD_IA
BT+
DCBATOUT
UMA
緯創資通
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.
Title
Power Sequence Logic
Size
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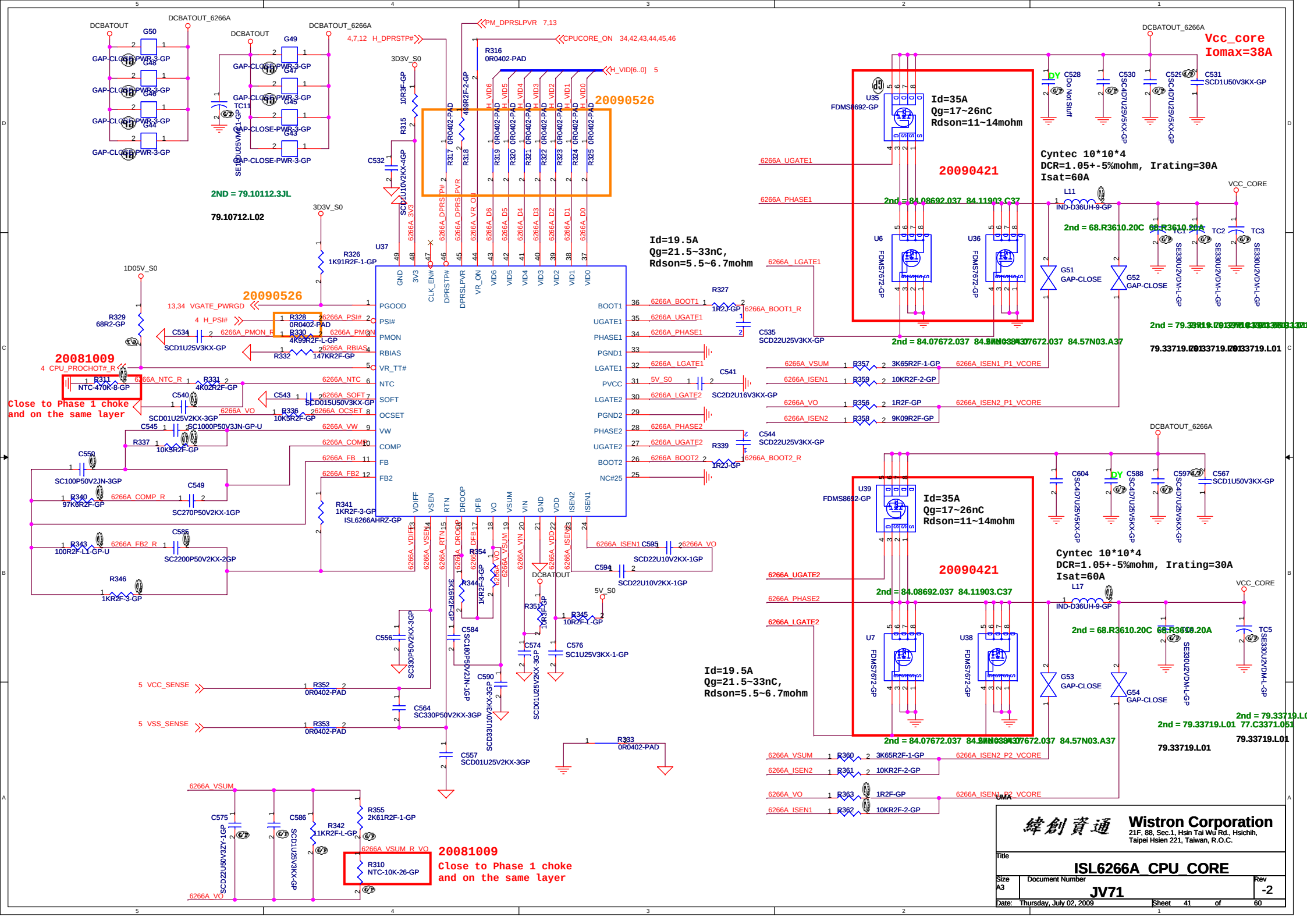
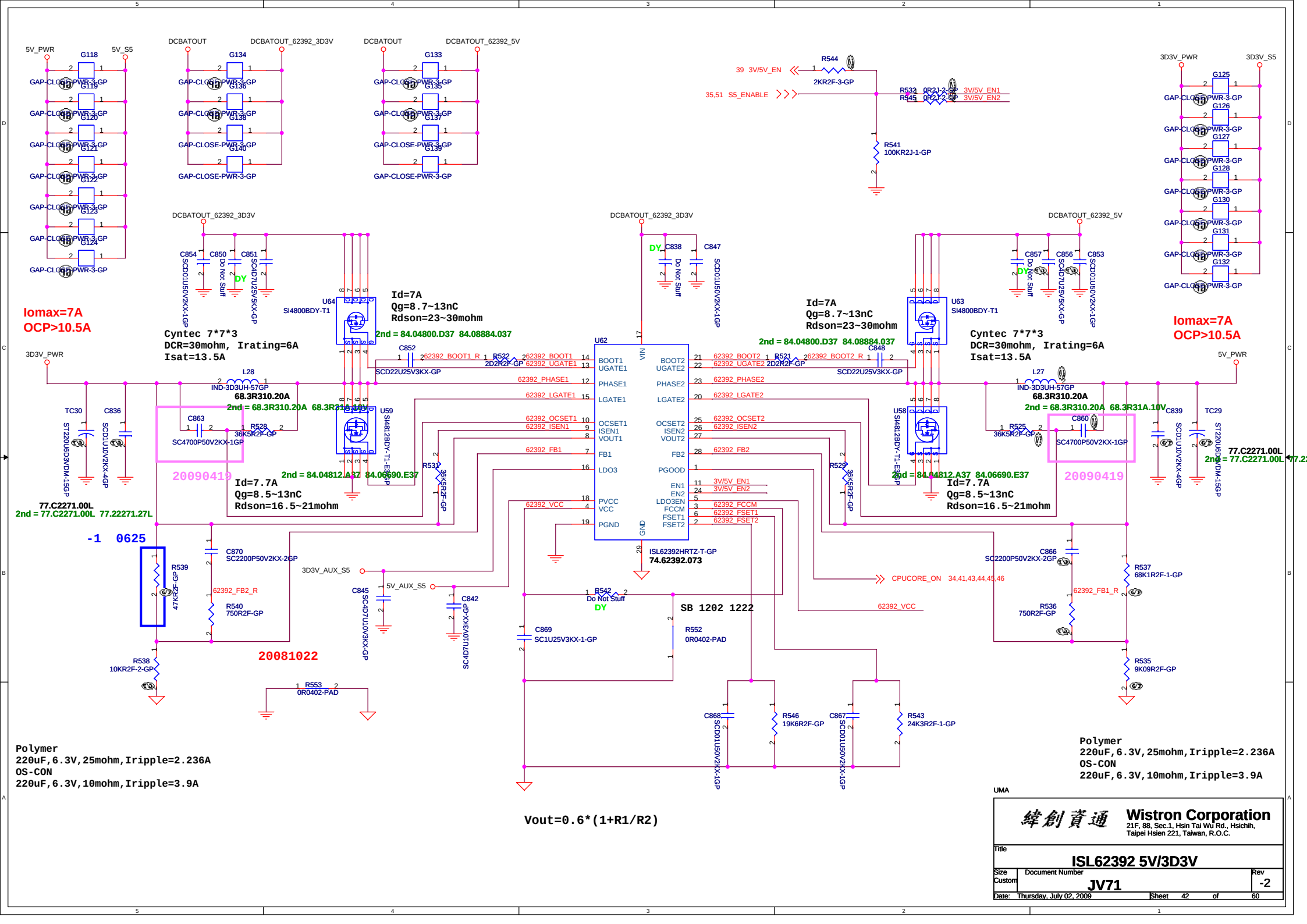

Vcc_core
Iomax=38A
Id=35A
Qg=17~26nC
Rdson=11~14mohm
20090421
Cyntec 10*10*4
DCR=1.05+-5%mohm, Irating=30A
Isat=60A
Id=19.5A
Qg=21.5~33nC,
Rdson=5.5~6.7mohm
20090526
20081009
Close to Phase 1 choke
and on the same layer
2ND = 79.10112.3JL
79.10712.L02
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.
ISL6266A_CPU_CORE
JV71
Thursday, July 02, 2009


5V_PWR
5V_S5
DCBATOUT
DCBATOUT_62392_3D3V
DCBATOUT_62392_5V
3D3V_PWR
3D3V_S5
G118
G119
G120
G121
G122
G123
G124
G134
G136
G138
G140
G133
G135
G137
G139
G125
G126
G127
G128
G130
G131
G132
GAP-CLOSE-PWR-3-GP
R544
2KR2F-3-GP
39 3V/5V_EN
35,51 S5_ENABLE
R532 0R2J-2-GP
R545 0R2J-2-GP
3V/5V_EN1
3V/5V_EN2
R541
100KR2J-1-GP
Iomax=7A
OCP>10.5A
Cyntec 7*7*3
DCR=30mohm, Irating=6A
Isat=13.5A
Id=7A
Qg=8.7~13nC
Rdson=23~30mohm
2nd = 84.04800.D37 84.08884.037
U64
SI4800BDY-T1
U63
SI4800BDY-T1
U62
ISL62392HRTZ-T-GP
74.62392.073
L28
L27
IND-3D3UH-57GP
68.3R310.20A
2nd = 68.3R310.20A 68.3R31A.10V
U59
U58
SI4812BDY-T1-E3-GP
2nd = 84.04812.A37 84.06690.E37
Id=7.7A
Qg=8.5~13nC
Rdson=16.5~21mohm
20090419
77.C2271.00L
2nd = 77.C2271.00L 77.22271.27L
-1 0625
20081022
SB 1202 1222
CPUCORE_ON 34,41,43,44,45,46
Vout=0.6*(1+R1/R2)
Polymer
220uF,6.3V,25mohm,Iripple=2.236A
OS-CON
220uF,6.3V,10mohm,Iripple=3.9A
UMA
緯創資通
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.
Title
ISL62392 5V/3D3V
Size
Custom
Document Number
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-2
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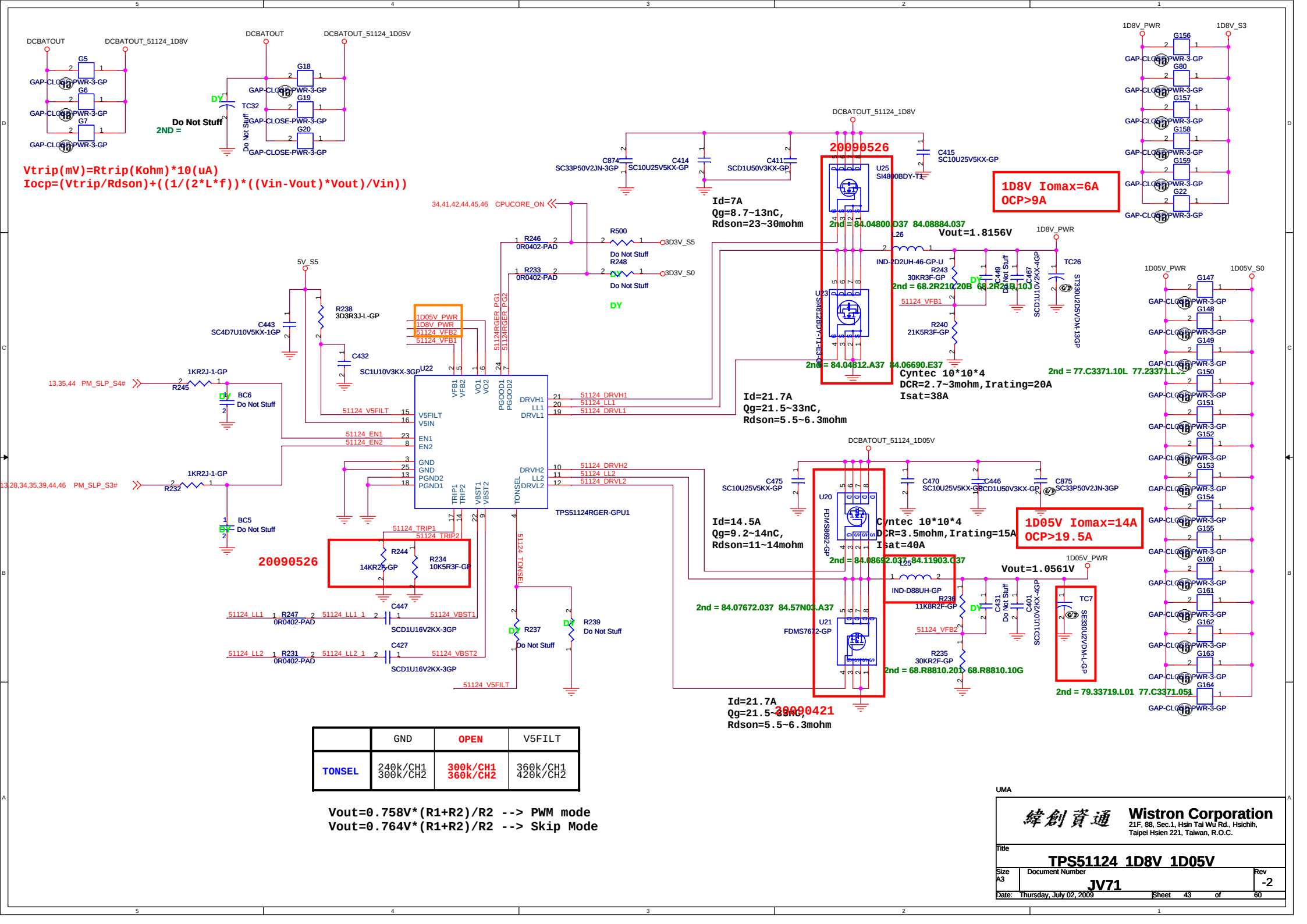
DCBATOUT
DCBATOUT_51124_1D8V
DCBATOUT_51124_1D05V
Do Not Stuff
2ND =
Vtrip(mV)=Rtrip(Kohm)*10(uA)
Iocp=(Vtrip/Rdson)+((1/(2*L*f))*((Vin-Vout)*Vout)/Vin))
1D8V_PWR
1D8V_S3
1D05V_PWR
1D05V_S0
5V_S5
3D3V_S5
3D3V_S0
CPUCORE_ON
PM_SLP_S4#
PM_SLP_S3#
TPS51124RGER-GPU1
20090526
20090421
Id=7A
Qg=8.7~13nC,
Rdson=23~30mohm
1D8V Iomax=6A
OCP>9A
Vout=1.8156V
Cyntec 10*10*4
DCR=2.7~3mohm,Irating=20A
Isat=38A
Id=21.7A
Qg=21.5~33nC,
Rdson=5.5~6.3mohm
Id=14.5A
Qg=9.2~14nC,
Rdson=11~14mohm
Cyntec 10*10*4
DCR=3.5mohm,Irating=15A
Isat=40A
1D05V Iomax=14A
OCP>19.5A
Vout=1.0561V
Id=21.7A
Qg=21.5~33nC,
Rdson=5.5~6.3mohm
Vout=0.758V*(R1+R2)/R2 --> PWM mode
Vout=0.764V*(R1+R2)/R2 --> Skip Mode
TONSEL
GND
OPEN
V5FILT
240k/CH1
300k/CH2
300k/CH1
360k/CH2
360k/CH1
420k/CH2
UMA
緯創資通
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.
Title
TPS51124 1D8V 1D05V
Size
A3
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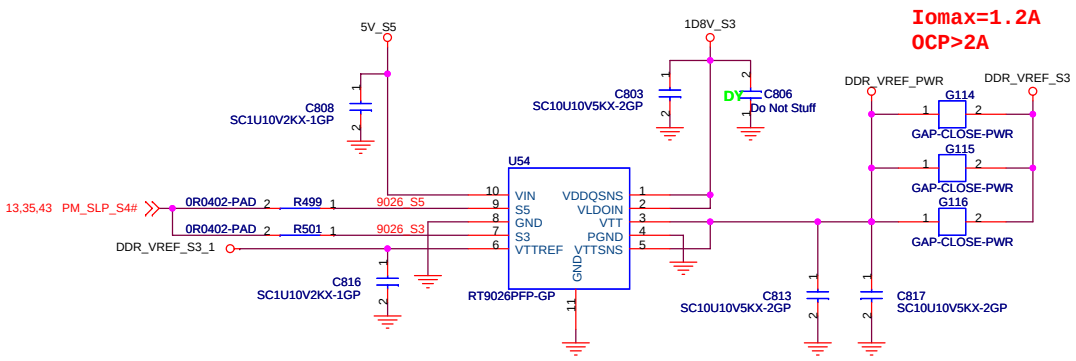

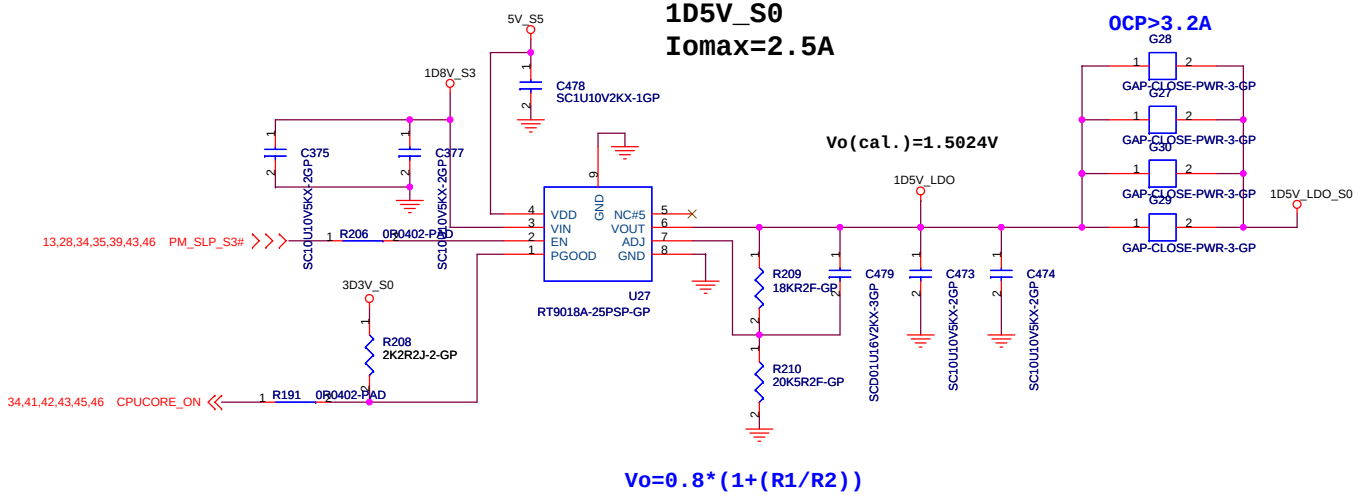

UMA

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21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title	0D75V	
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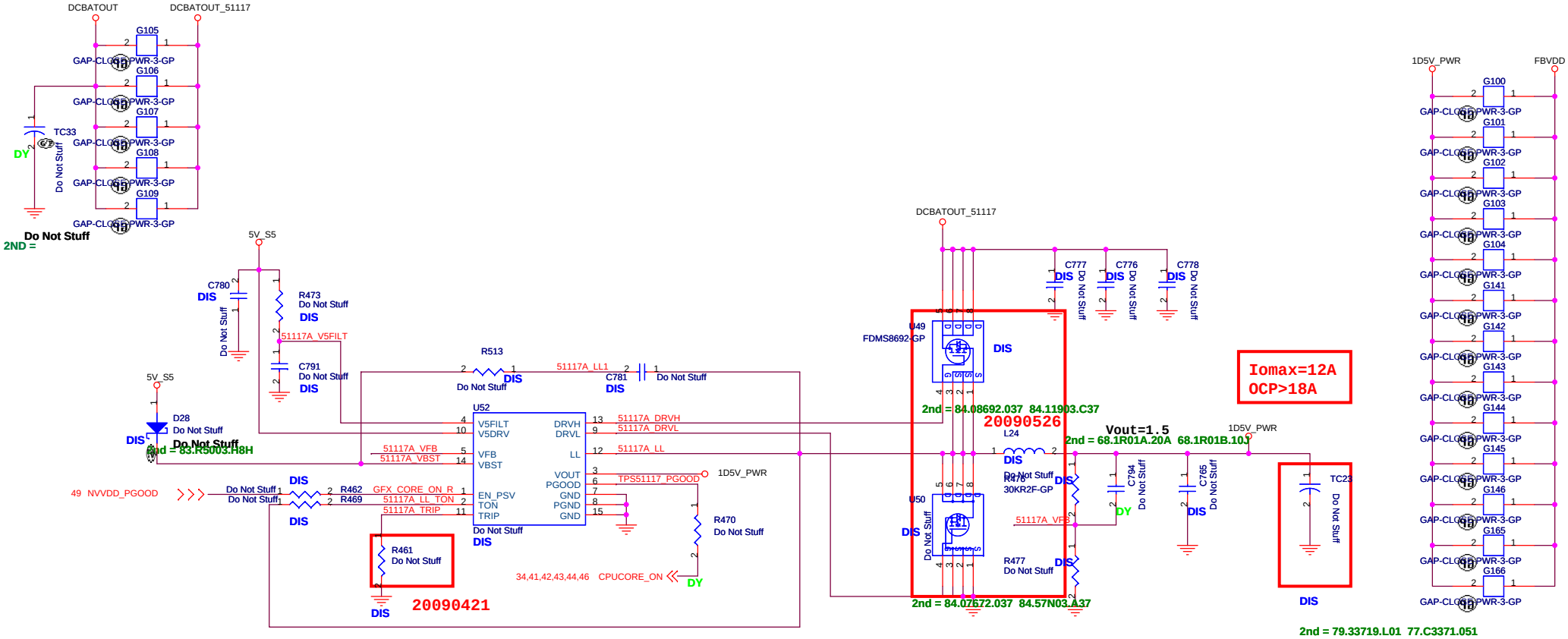

Vout=0.75V*(R1+R2)/R2

UMA

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21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: TPS51117_1D8V

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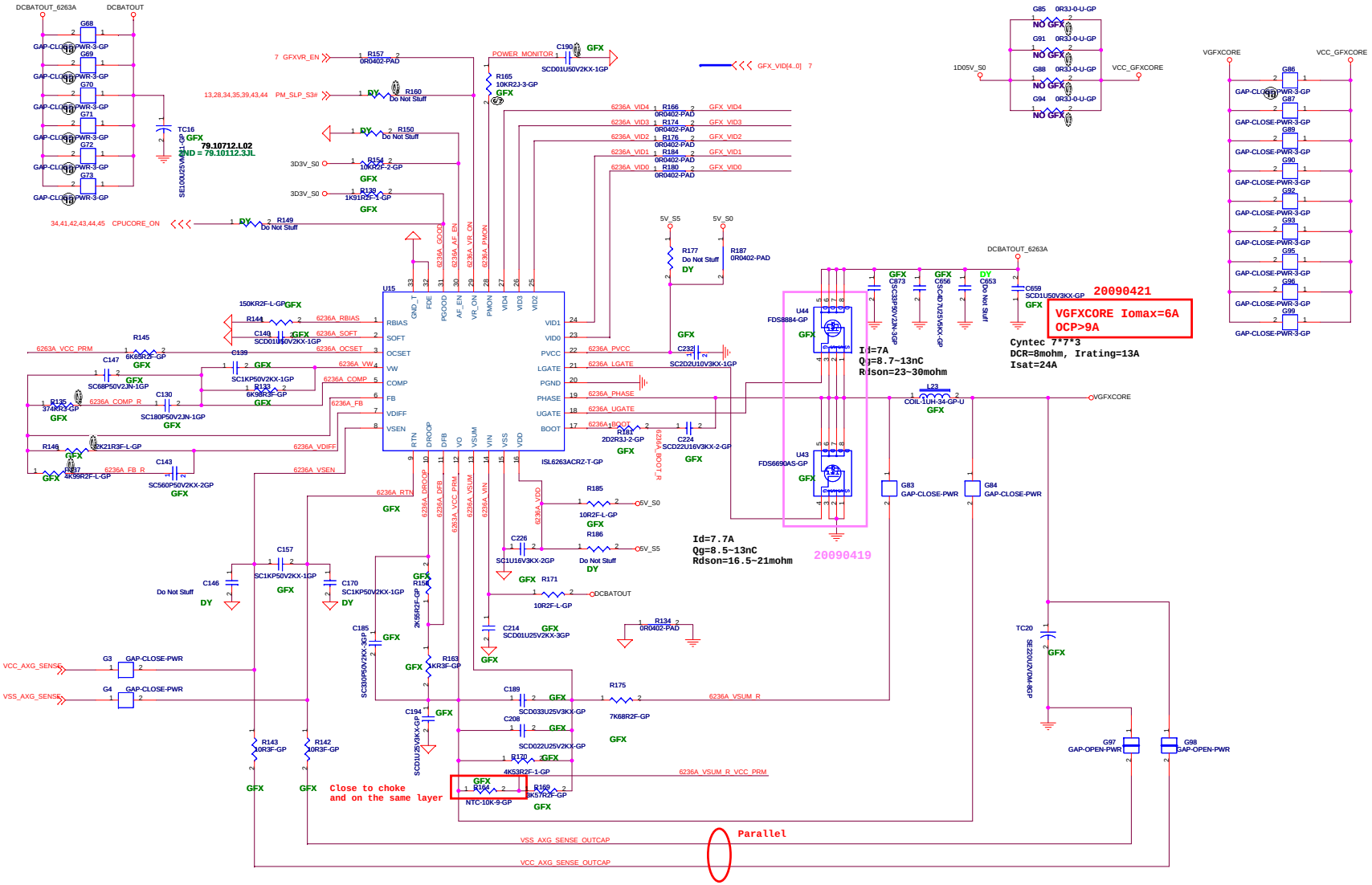

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Taipei Hsien 221, Taiwan, R.O.C.

Title: ISL6263A_GFX CORE

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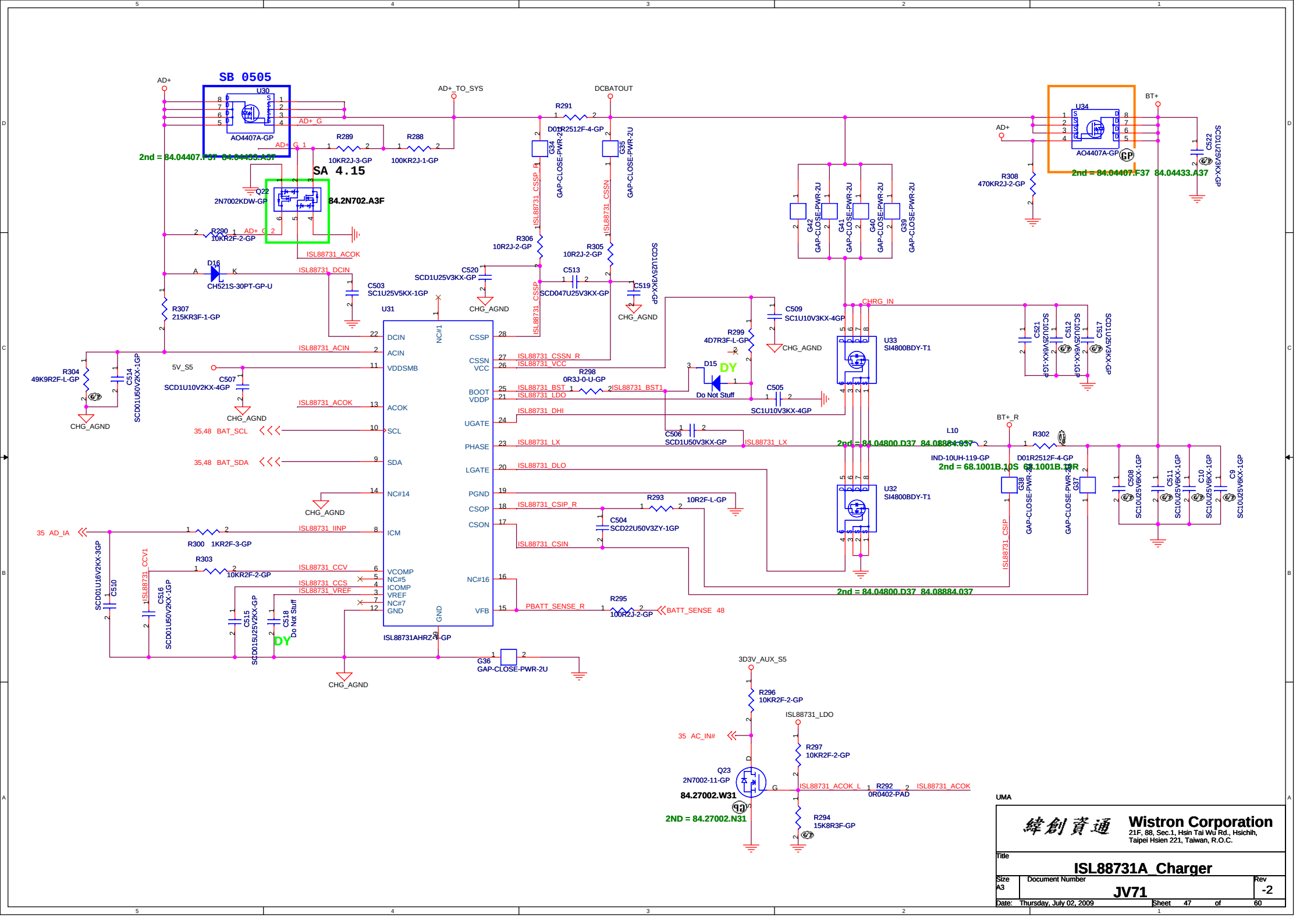
SB 0505
SA 4.15
84.2N702.A3F
2nd = 84.04407.F37 84.04433.A37
2nd = 84.04800.D37 84.08884.037
2nd = 68.1001B.10S 68.1001B.10R
2ND = 84.27002.N31
ISL88731AHRZ-T-GP
AO4407A-GP
2N7002KDW-GP
2N7002-11-GP
CH521S-30PT-GP-U
IND-10UH-119-GP
SI4800BDY-T1
D01R2512F-4-GP
GAP-CLOSE-PWR-2U
Do Not Stuff
DY
CHG_AGND
AD+
AD+_TO_SYS
DCBATOUT
BT+
BT+_R
CHRG_IN
3D3V_AUX_S5
5V_S5
35,48 BAT_SCL
35,48 BAT_SDA
35 AD_IA
35 AC_IN#
BATT_SENSE 48
DCIN
ACIN
VDDSMB
ACOK
SCL
SDA
NC#14
ICM
VCOMP
NC#5
ICOMP
VREF
NC#7
GND
NC#16
VFB
CSSP
CSSN
VCC
BOOT
VDDP
UGATE
PHASE
LGATE
PGND
CSOP
CSON
NC#1
ISL88731_ACOK
ISL88731_DCIN
ISL88731_ACIN
ISL88731_CSSN_R
ISL88731_VCC
ISL88731_BST
ISL88731_BST1
ISL88731_LDO
ISL88731_DHI
ISL88731_LX
ISL88731_DLO
ISL88731_CSIP_R
ISL88731_CSIN
ISL88731_IINP
ISL88731_CCV
ISL88731_CCS
ISL88731_VREF
PBATT_SENSE_R
ISL88731_CCV1
ISL88731_CSIP
ISL88731_ACOK_L
R291 D01R2512F-4-GP
R289 10KR2J-3-GP
R288 100KR2J-1-GP
R290 10KR2F-2-GP
R306 10R2J-2-GP
R305 10R2J-2-GP
R307 215KR3F-1-GP
R304 49K9R2F-L-GP
R299 4D7R3F-L-GP
R298 0R3J-0-U-GP
R300 1KR2F-3-GP
R303 10KR2F-2-GP
R293 10R2F-L-GP
R295 100R2J-2-GP
R296 10KR2F-2-GP
R297 10KR2F-2-GP
R294 15K8R3F-GP
R292 0R0402-PAD
R308 470KR2J-2-GP
R302
L10
C503 SC1U25V5KX-1GP
C504 SCD22U50V3ZY-1GP
C505 SC1U10V3KX-4GP
C506 SCD1U50V3KX-GP
C507 SCD1U10V2KX-4GP
C509 SC1U10V3KX-4GP
C510 SCD01U16V2KX-3GP
C513 SCD047U25V3KX-GP
C514 SCD01U50V2KX-1GP
C515 SCD015U25V2KX-GP
C516 SCD01U50V2KX-1GP
C518 Do Not Stuff
C520 SCD1U25V3KX-GP
C519 SCD1U25V3KX-GP
C522 SCD1U25V3KX-GP
C521 SC10U25V6KX-1GP
C512 SC10U25V6KX-1GP
C517 SCD1U25V3KX-GP
C508 SC10U25V6KX-1GP
C511 SC10U25V6KX-1GP
C10 SC10U25V6KX-1GP
C9 SC10U25V6KX-1GP
G34 G35 G36 G37 G38 G39 G40 G41 G42 GAP-CLOSE-PWR-2U
Q22 84.2N702.A3F
Q23 84.27002.W31
U30 U31 U32 U33 U34
UMA
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.
Title
ISL88731A_Charger
Size A3
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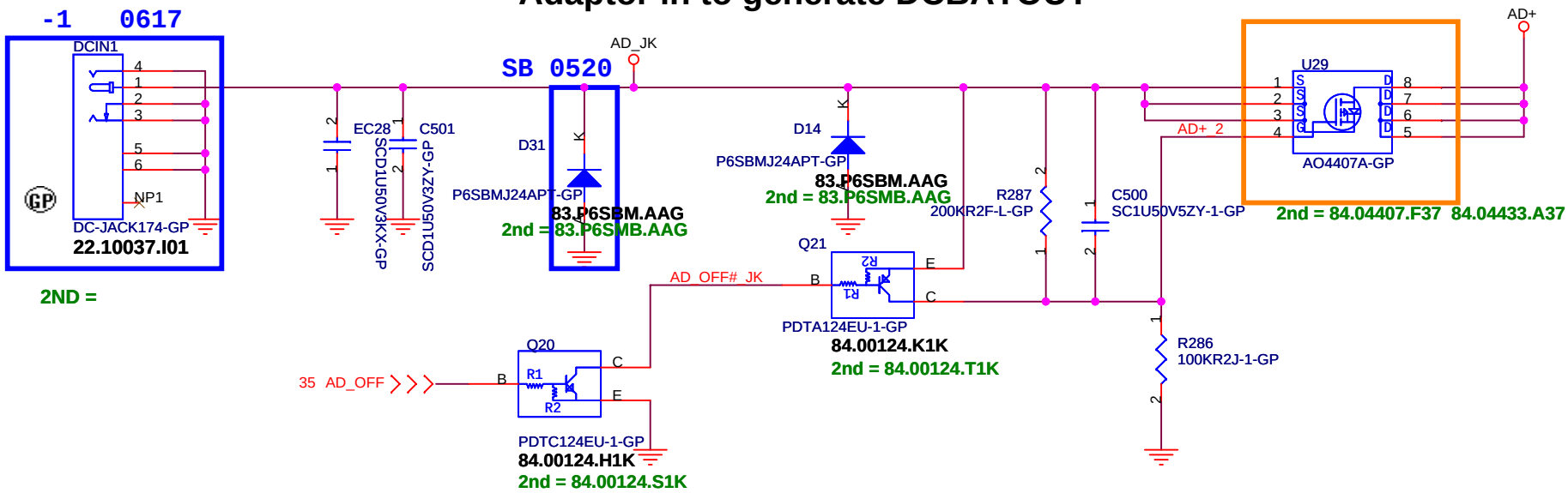
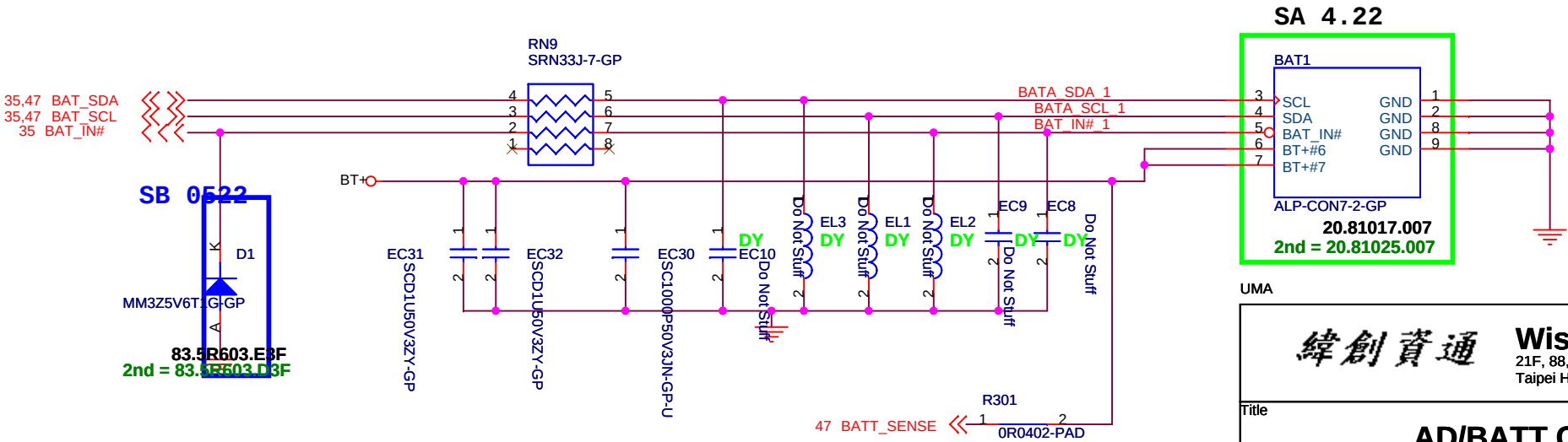
Adaptor in to generate DCBATOUT



BATTERY CONNECTOR



UMA

緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title	AD/BATT CONN	
Size	Document Number: JV71	Rev: -2
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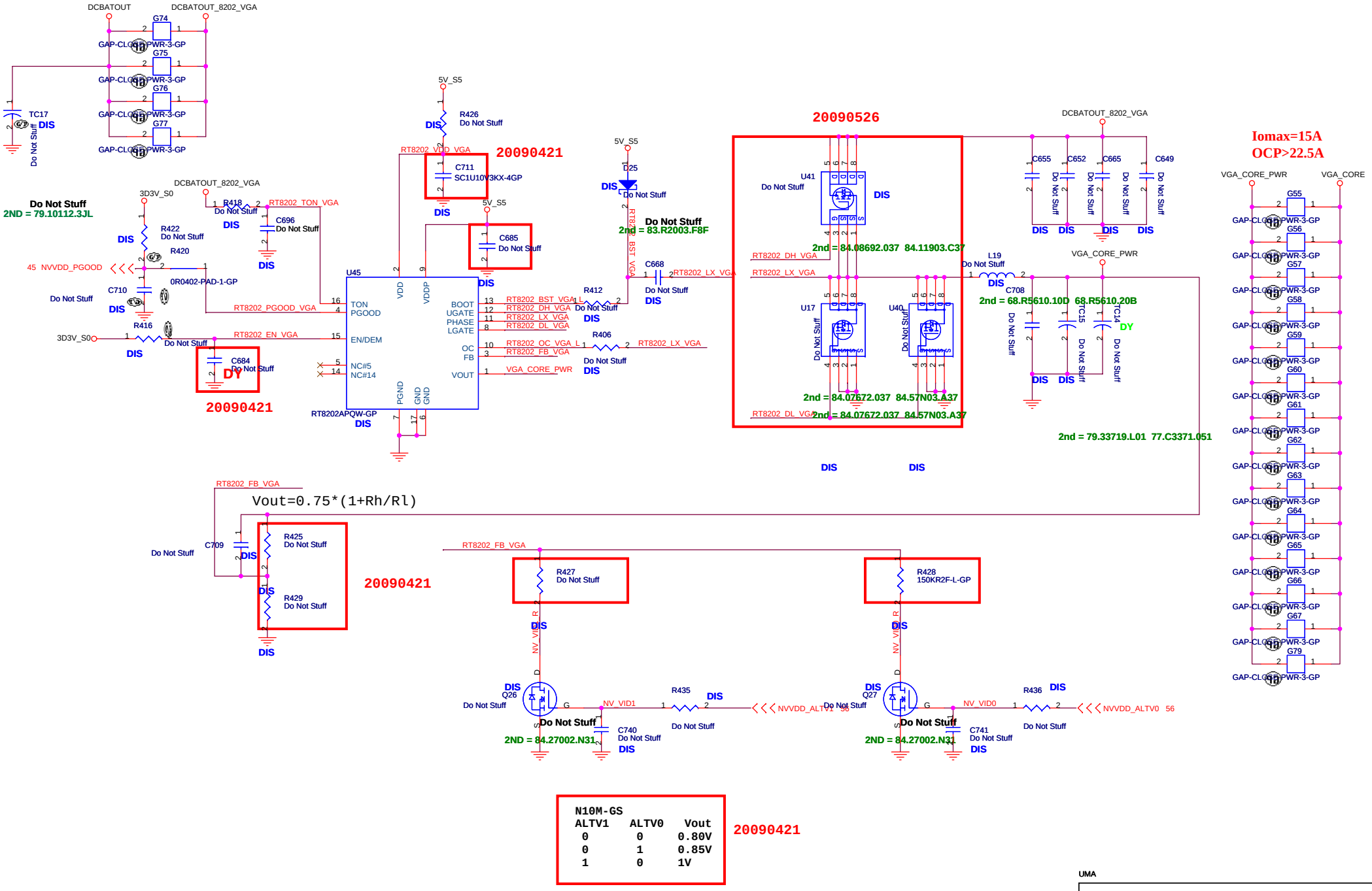

UMA

緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: **RT8202A VGA CORE**

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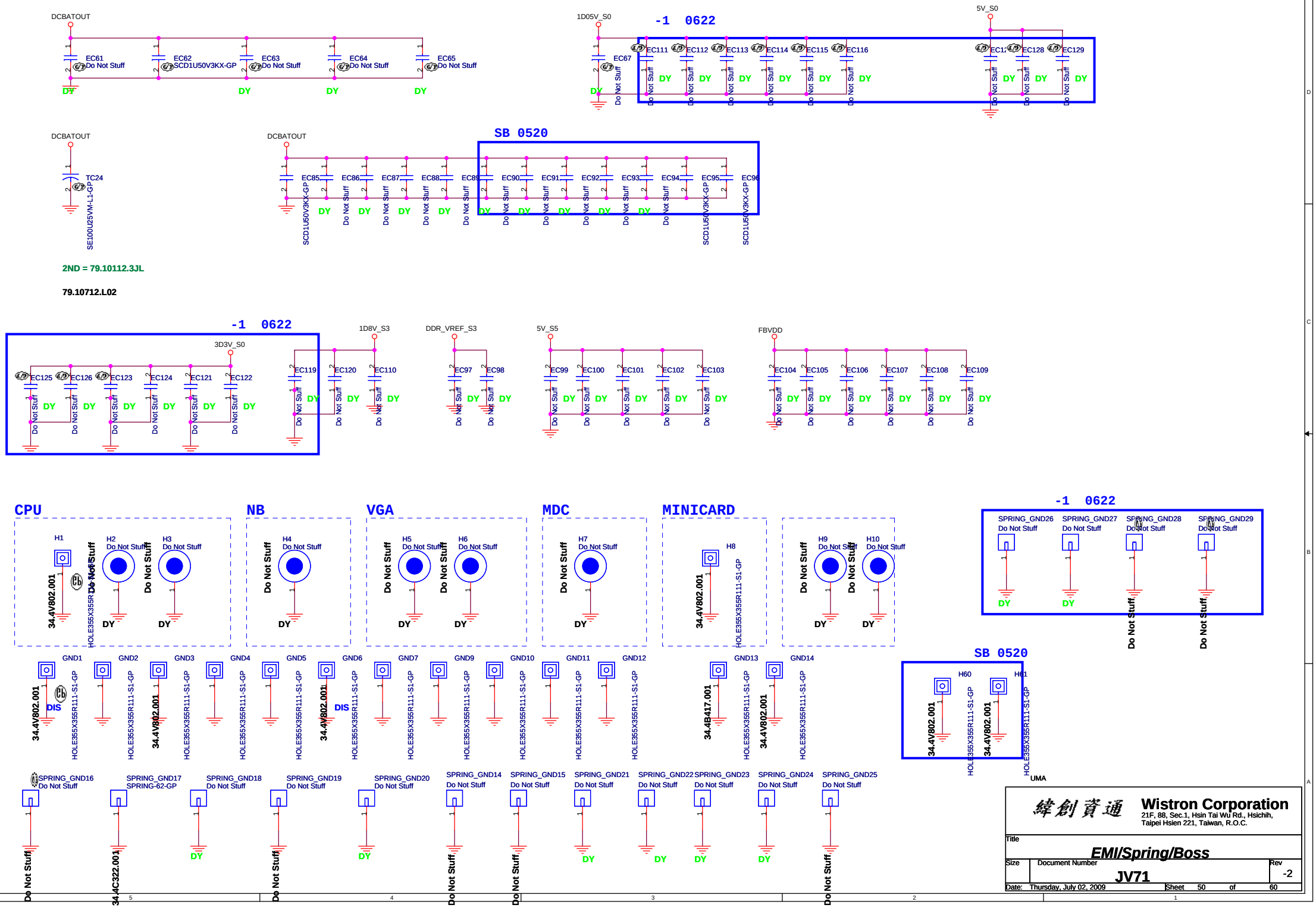
DCBATOUT
EC61 Do Not Stuff
EC62 SCD1U50V3KX-GP
EC63 Do Not Stuff
EC64 Do Not Stuff
EC65 Do Not Stuff
1D05V_S0
-1 0622
EC67 Do Not Stuff
EC111 EC112 EC113 EC114 EC115 EC116
5V_S0
EC127 EC128 EC129
DCBATOUT
TC24
SE100U25VM-L1-GP
DCBATOUT
SB 0520
EC85 EC86 EC87 EC88 EC89 EC90 EC91 EC92 EC93 EC94 EC95 EC96
SCD1U50V3KX-GP
2ND = 79.10112.3JL
79.10712.L02
-1 0622
3D3V_S0
EC125 EC126 EC123 EC124 EC121 EC122
1D8V_S3
EC119 EC120 EC110
DDR_VREF_S3
EC97 EC98
5V_S5
EC99 EC100 EC101 EC102 EC103
FBVDD
EC104 EC105 EC106 EC107 EC108 EC109
CPU
NB
VGA
MDC
MINICARD
H1 H2 H3 H4 H5 H6 H7 H8 H9 H10
Do Not Stuff
34.4V802.001
HOLE355X355R111-S1-GP
-1 0622
SPRING_GND26 SPRING_GND27 SPRING_GND28 SPRING_GND29
GND1 GND2 GND3 GND4 GND5 GND6 GND7 GND9 GND10 GND11 GND12 GND13 GND14
34.4B417.001
SB 0520
H60 H61
SPRING_GND16 SPRING_GND17 SPRING-62-GP SPRING_GND18 SPRING_GND19 SPRING_GND20 SPRING_GND14 SPRING_GND15 SPRING_GND21 SPRING_GND22 SPRING_GND23 SPRING_GND24 SPRING_GND25
34.4C322.001
UMA
緯創資通
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.
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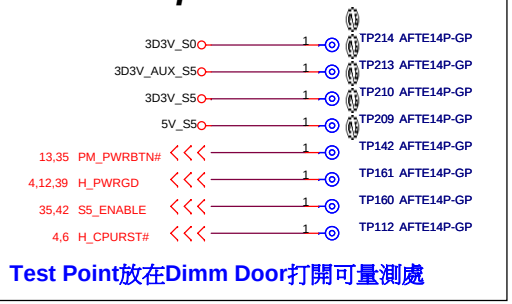
Check test point



Test Point放在Dimm Door打開可量測處

UMA

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21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

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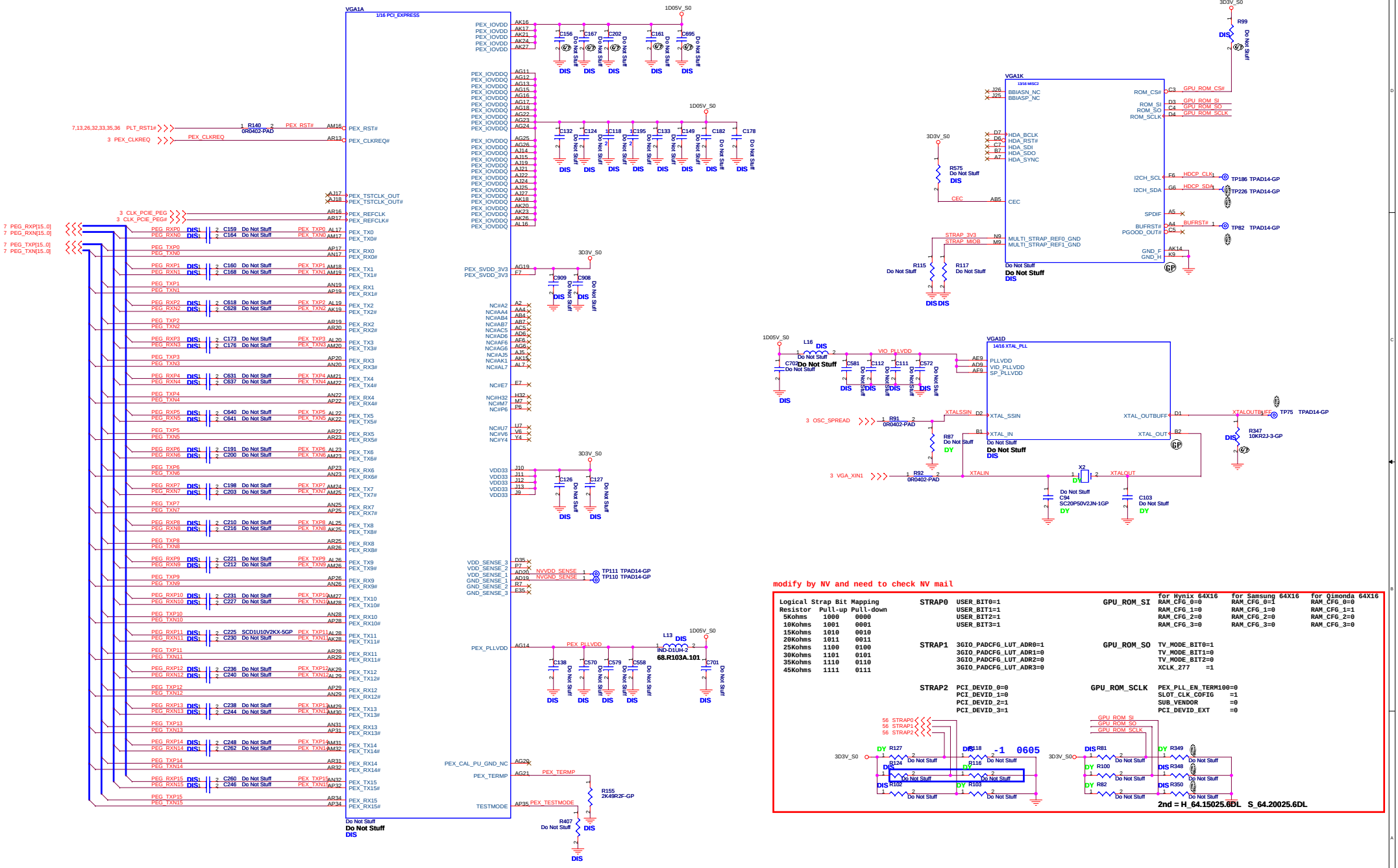
VGA1A
1/16 PCI_EXPRESS
PEX_RST#
PEX_CLKREQ#
PEX_TSTCLK_OUT
PEX_REFCLK
PEX_REFCLK#
PEX_TX0
PEX_RX0
PEX_TX1
PEX_RX1
PEX_TX2
PEX_RX2
PEX_TX3
PEX_RX3
PEX_TX4
PEX_RX4
PEX_TX5
PEX_RX5
PEX_TX6
PEX_RX6
PEX_TX7
PEX_RX7
PEX_TX8
PEX_RX8
PEX_TX9
PEX_RX9
PEX_TX10
PEX_RX10
PEX_TX11
PEX_RX11
PEX_TX12
PEX_RX12
PEX_TX13
PEX_RX13
PEX_TX14
PEX_RX14
PEX_TX15
PEX_RX15
PEX_PLLVDD
PEX_CAL_PU_GND_NC
PEX_TERMP
TESTMODE
Do Not Stuff
DIS
VGA1K
VGA1D
14/16 XTAL_PLL
modify by NV and need to check NV mail
Logical Strap Bit Mapping
Resistor Pull-up Pull-down
5Kohms 1000 0000
10Kohms 1001 0001
15Kohms 1010 0010
20Kohms 1011 0011
25Kohms 1100 0100
30Kohms 1101 0101
35Kohms 1110 0110
45Kohms 1111 0111
STRAP0
USER_BIT0=1
USER_BIT1=1
USER_BIT2=1
USER_BIT3=1
STRAP1
3GIO_PADCFG_LUT_ADR0=1
3GIO_PADCFG_LUT_ADR1=0
3GIO_PADCFG_LUT_ADR2=0
3GIO_PADCFG_LUT_ADR3=0
STRAP2
PCI_DEVID_0=0
PCI_DEVID_1=0
PCI_DEVID_2=1
PCI_DEVID_3=1
GPU_ROM_SI
for Hynix 64X16 RAM_CFG_0=0 RAM_CFG_1=0 RAM_CFG_2=0 RAM_CFG_3=0
for Samsung 64X16 RAM_CFG_0=1 RAM_CFG_1=1 RAM_CFG_2=0 RAM_CFG_3=0
for Qimonda 64X16 RAM_CFG_0=0 RAM_CFG_1=1 RAM_CFG_2=0 RAM_CFG_3=0
GPU_ROM_SO
TV_MODE_BIT0=1
TV_MODE_BIT1=0
TV_MODE_BIT2=0
XCLK_277 =1
GPU_ROM_SCLK
PEX_PLL_EN_TERM100=0
SLOT_CLK_COFIG =1
SUB_VENDOR =0
PCI_DEVID_EXT =0
2nd = H_64.15025.6DL S_64.20025.6DL
UMA
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.
Title
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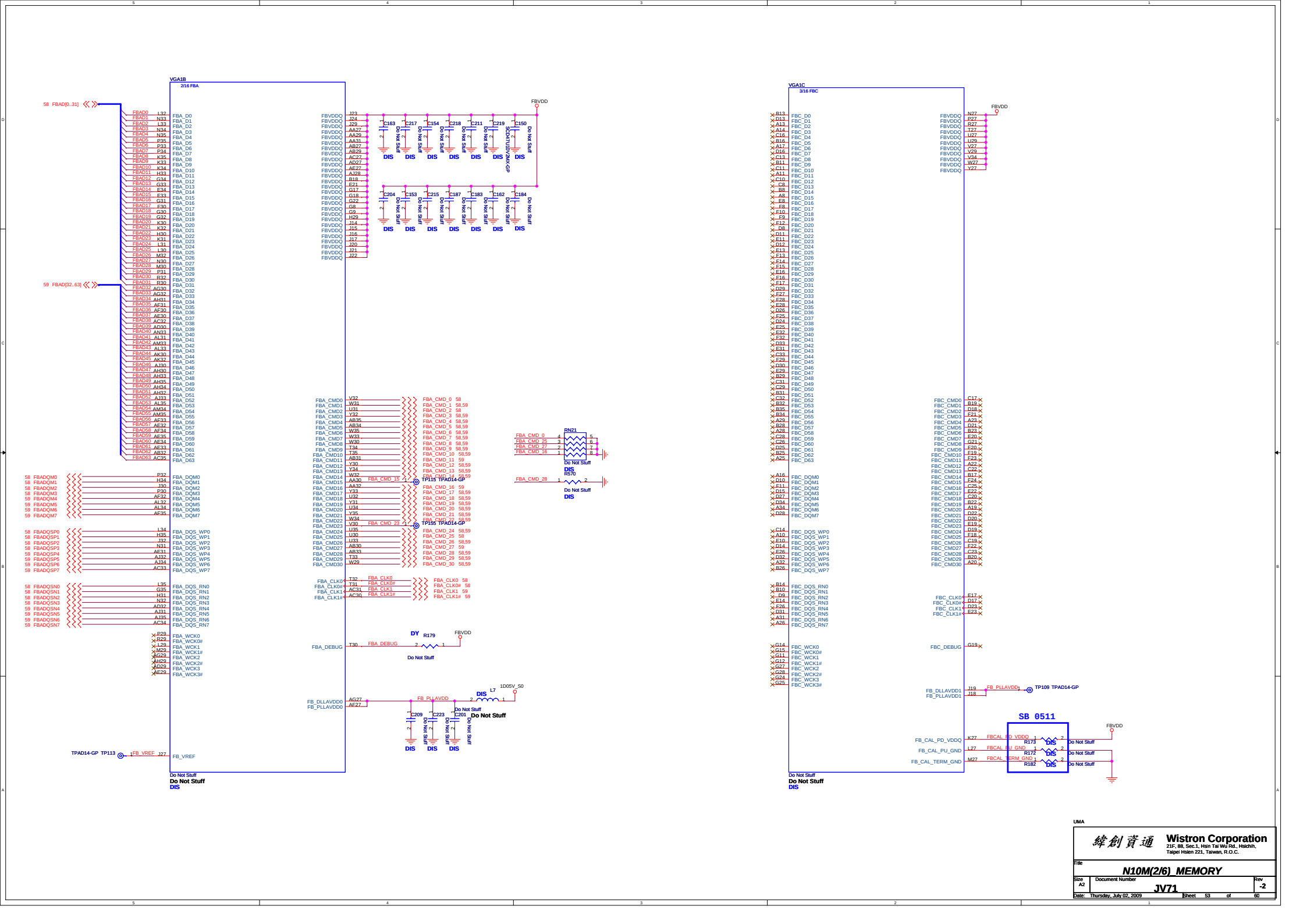
VGA1B
2/16 FBA
VGA1C
3/16 FBC
FBVDD
Do Not Stuff
DIS
SB 0511
TP109 TPAD14-GP
TP115 TPAD14-GP
TP195 TPAD14-GP
TPAD14-GP TP113
RN21
R570
R179
L7
1D05V_S0
UMA
緯創資通
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.
Title
N10M(2/6)_MEMORY
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A2
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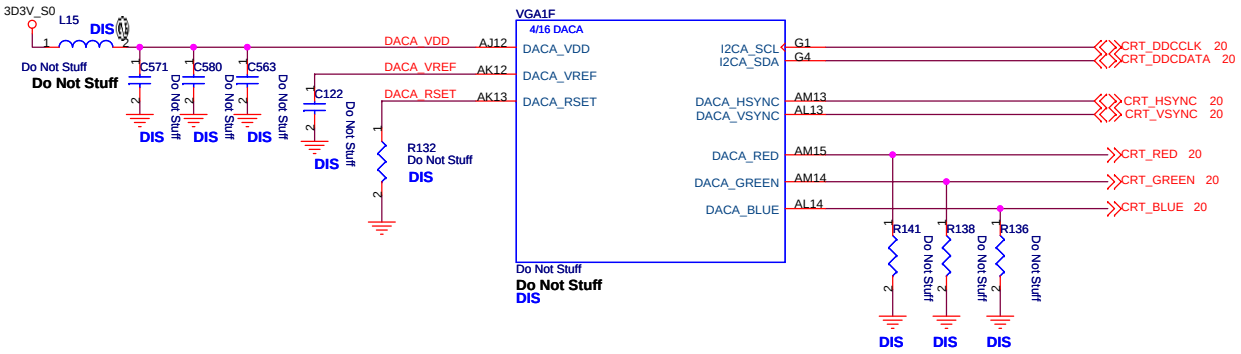

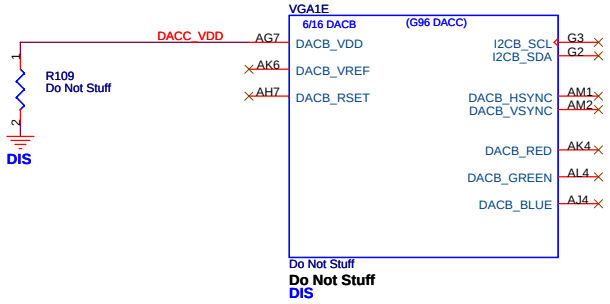

UMA

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Taipei Hsien 221, Taiwan, R.O.C.

Title: ***N10M(3/6) DAC***

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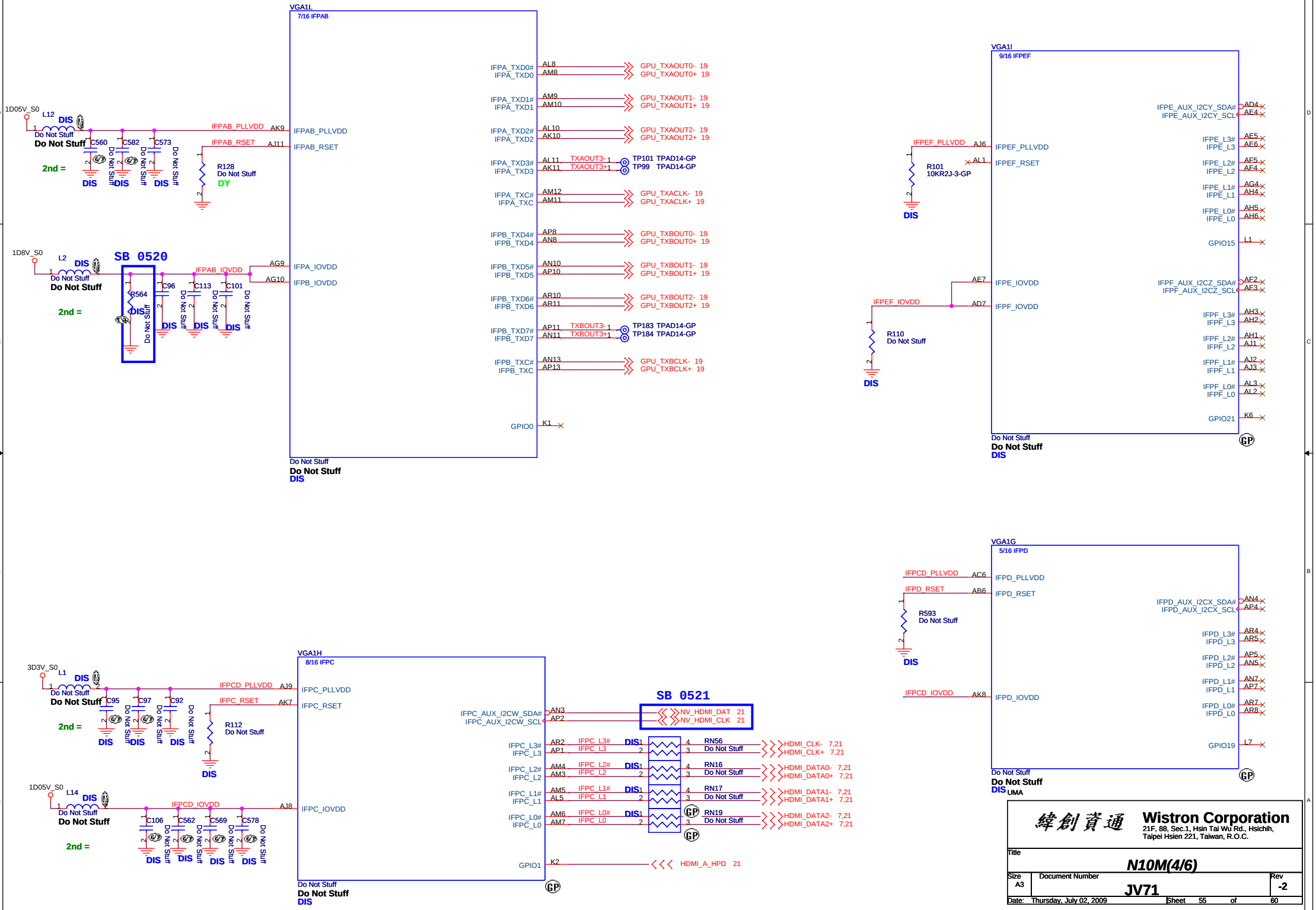
VGA1L
7/16 IFPAB
1D05V_S0
L12
DIS
Do Not Stuff
Do Not Stuff
C560
C582
C573
2nd =
DIS
IFPAB_PLLVDD
AK9
IFPAB_RSET
AJ11
R128
Do Not Stuff
DY
1D8V_S0
L2
SB 0520
IFPAB_IOVDD
AG9
AG10
R564
C96
C113
C101
IFPA_IOVDD
IFPB_IOVDD
IFPA_TXD0#
IFPA_TXD0
AL8
AM8
GPU_TXAOUT0- 19
GPU_TXAOUT0+ 19
IFPA_TXD1#
IFPA_TXD1
AM9
AM10
GPU_TXAOUT1- 19
GPU_TXAOUT1+ 19
IFPA_TXD2#
IFPA_TXD2
AL10
AK10
GPU_TXAOUT2- 19
GPU_TXAOUT2+ 19
IFPA_TXD3#
IFPA_TXD3
AL11
AK11
TXAOUT3-
TXAOUT3+
TP101 TPAD14-GP
TP99 TPAD14-GP
IFPA_TXC#
IFPA_TXC
AM12
AM11
GPU_TXACLK- 19
GPU_TXACLK+ 19
IFPB_TXD4#
IFPB_TXD4
AP8
AN8
GPU_TXBOUT0- 19
GPU_TXBOUT0+ 19
IFPB_TXD5#
IFPB_TXD5
AN10
AP10
GPU_TXBOUT1- 19
GPU_TXBOUT1+ 19
IFPB_TXD6#
IFPB_TXD6
AR10
AR11
GPU_TXBOUT2- 19
GPU_TXBOUT2+ 19
IFPB_TXD7#
IFPB_TXD7
AP11
AN11
TXBOUT3-
TXBOUT3+
TP183 TPAD14-GP
TP184 TPAD14-GP
IFPB_TXC#
IFPB_TXC
AN13
AP13
GPU_TXBCLK- 19
GPU_TXBCLK+ 19
GPIO0
K1
Do Not Stuff
DIS
VGA1I
9/16 IFPEF
IFPEF_PLLVDD
AJ6
IFPEF_RSET
AL1
R101
10KR2J-3-GP
IFPEF_IOVDD
AE7
AD7
R110
Do Not Stuff
IFPE_IOVDD
IFPF_IOVDD
IFPE_AUX_I2CY_SDA#
IFPE_AUX_I2CY_SCL
AD4
AE4
IFPE_L3#
IFPE_L3
AE5
AE6
IFPE_L2#
IFPE_L2
AF5
AF4
IFPE_L1#
IFPE_L1
AG4
AH4
IFPE_L0#
IFPE_L0
AH5
AH6
GPIO15
L1
IFPF_AUX_I2CZ_SDA#
IFPF_AUX_I2CZ_SCL
AF2
AF3
IFPF_L3#
IFPF_L3
AH3
AH2
IFPF_L2#
IFPF_L2
AH1
AJ1
IFPF_L1#
IFPF_L1
AJ2
AJ3
IFPF_L0#
IFPF_L0
AL3
AL2
GPIO21
K6
Do Not Stuff
Do Not Stuff
DIS
GP
3D3V_S0
L1
DIS
Do Not Stuff
Do Not Stuff
C95
C97
C92
2nd =
IFPCD_PLLVDD
AJ9
IFPC_RSET
AK7
R112
Do Not Stuff
1D05V_S0
L14
C106
C562
C569
C578
IFPCD_IOVDD
AJ8
VGA1H
8/16 IFPC
IFPC_PLLVDD
IFPC_RSET
IFPC_IOVDD
IFPC_AUX_I2CW_SDA#
IFPC_AUX_I2CW_SCL
AN3
AP2
SB 0521
NV_HDMI_DAT 21
NV_HDMI_CLK 21
IFPC_L3#
IFPC_L3
AR2
AP1
RN56
Do Not Stuff
HDMI_CLK- 7,21
HDMI_CLK+ 7,21
IFPC_L2#
IFPC_L2
AM4
AM3
RN16
Do Not Stuff
HDMI_DATA0- 7,21
HDMI_DATA0+ 7,21
IFPC_L1#
IFPC_L1
AM5
AL5
RN17
Do Not Stuff
HDMI_DATA1- 7,21
HDMI_DATA1+ 7,21
IFPC_L0#
IFPC_L0
AM6
AM7
RN19
Do Not Stuff
HDMI_DATA2- 7,21
HDMI_DATA2+ 7,21
GPIO1
K2
HDMI_A_HPD 21
VGA1G
5/16 IFPD
IFPCD_PLLVDD
AC6
IFPD_RSET
AB6
R593
Do Not Stuff
IFPCD_IOVDD
AK8
IFPD_PLLVDD
IFPD_RSET
IFPD_IOVDD
IFPD_AUX_I2CX_SDA#
IFPD_AUX_I2CX_SCL
AN4
AP4
IFPD_L3#
IFPD_L3
AR4
AR5
IFPD_L2#
IFPD_L2
AP5
AN5
IFPD_L1#
IFPD_L1
AN7
AP7
IFPD_L0#
IFPD_L0
AR7
AR8
GPIO19
L7
UMA
緯創資通
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.
Title
N10M(4/6)
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A3
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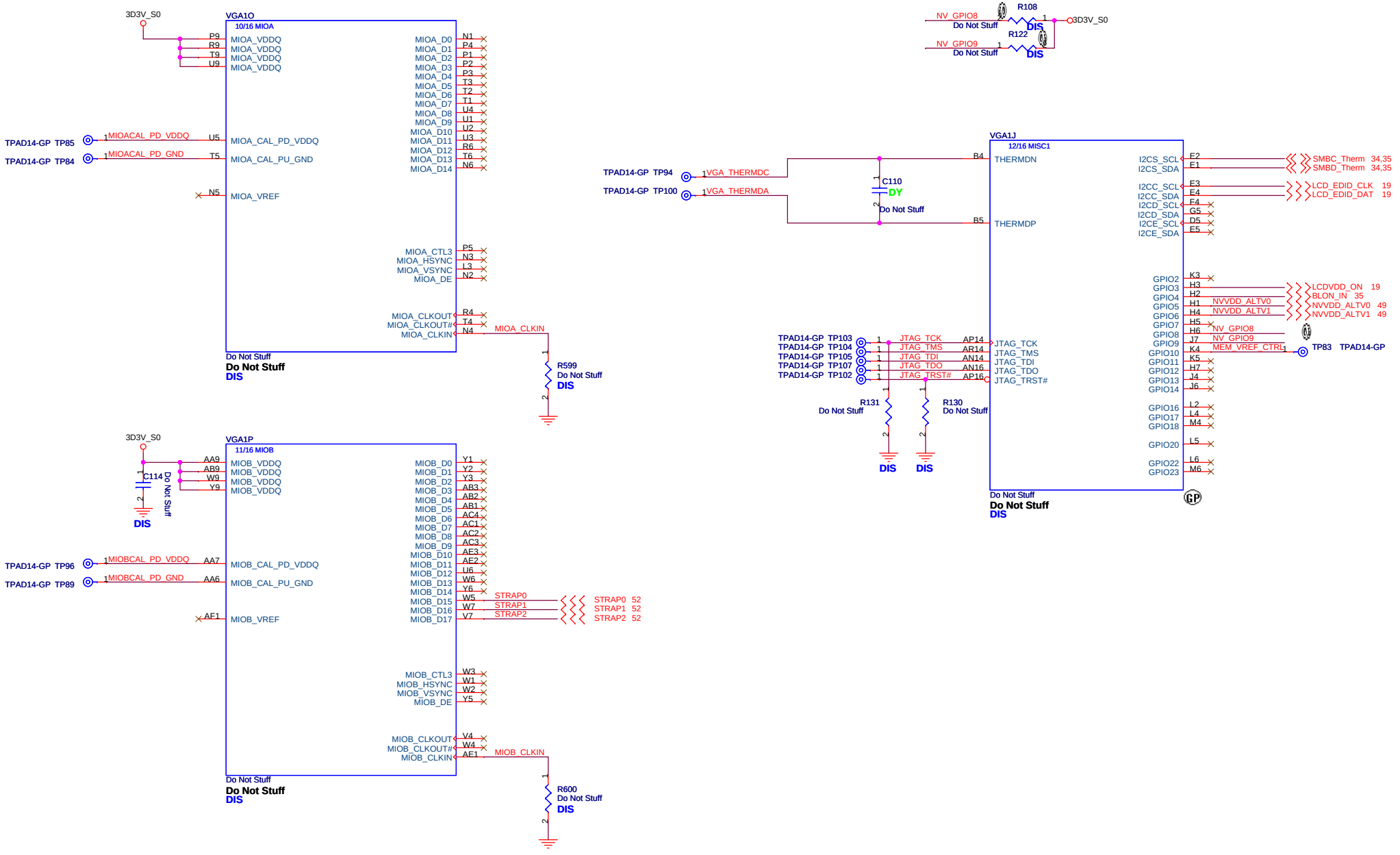

UMA

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Taipei Hsien 221, Taiwan, R.O.C.

Title: ***N10M(5/6) MIO/ GPIO***

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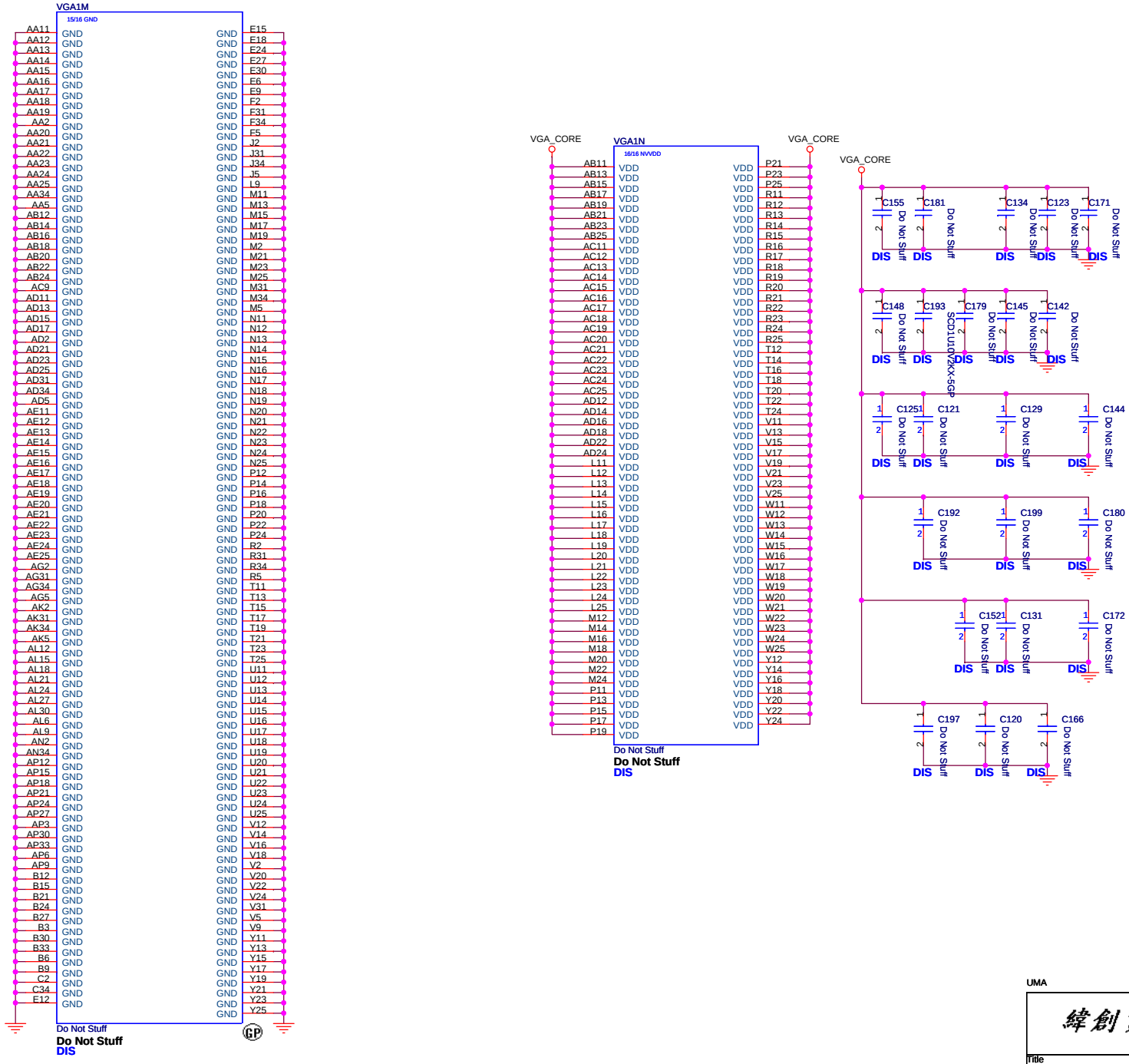

UMA

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Taipei Hsien 221, Taiwan, R.O.C.

Title: ***N10M(6/6) POWER***

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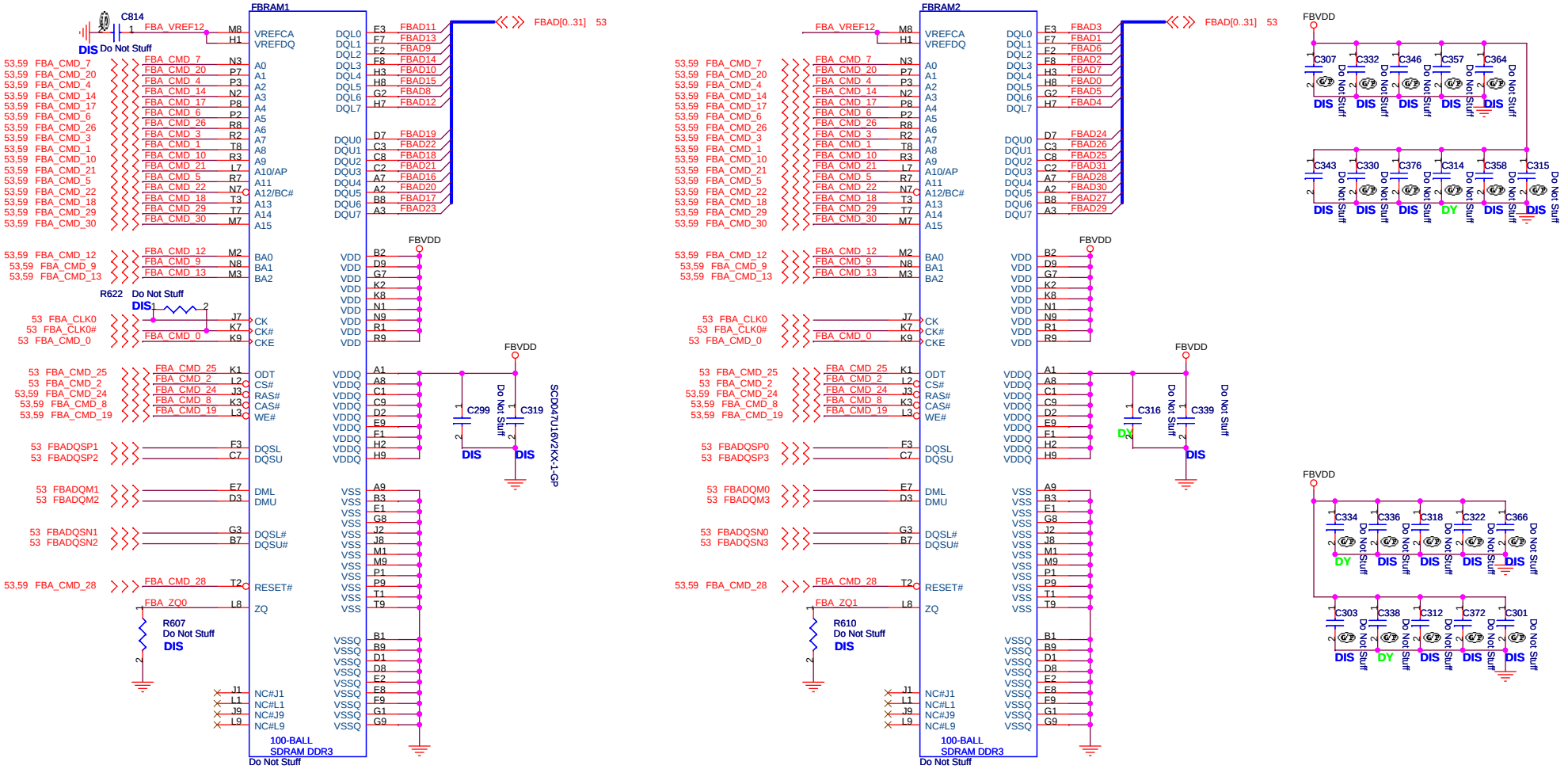


2ND = H_72.51G63.C0U S_72.41164.H0U

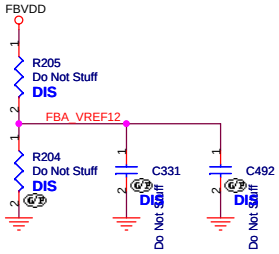
DIS

2ND = H_72.51G63.C0U S_72.41164.H0U

DIS

FB CMD mapping Mode C-N10M
<Mirror Mode>

DDR3 Power consumption 1.5V@800MHz
Hynix :IDD4W=220.4mA
Samsung :IDD7=150.4mA (calcurated)



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Title: ***VRAM(1/2)***

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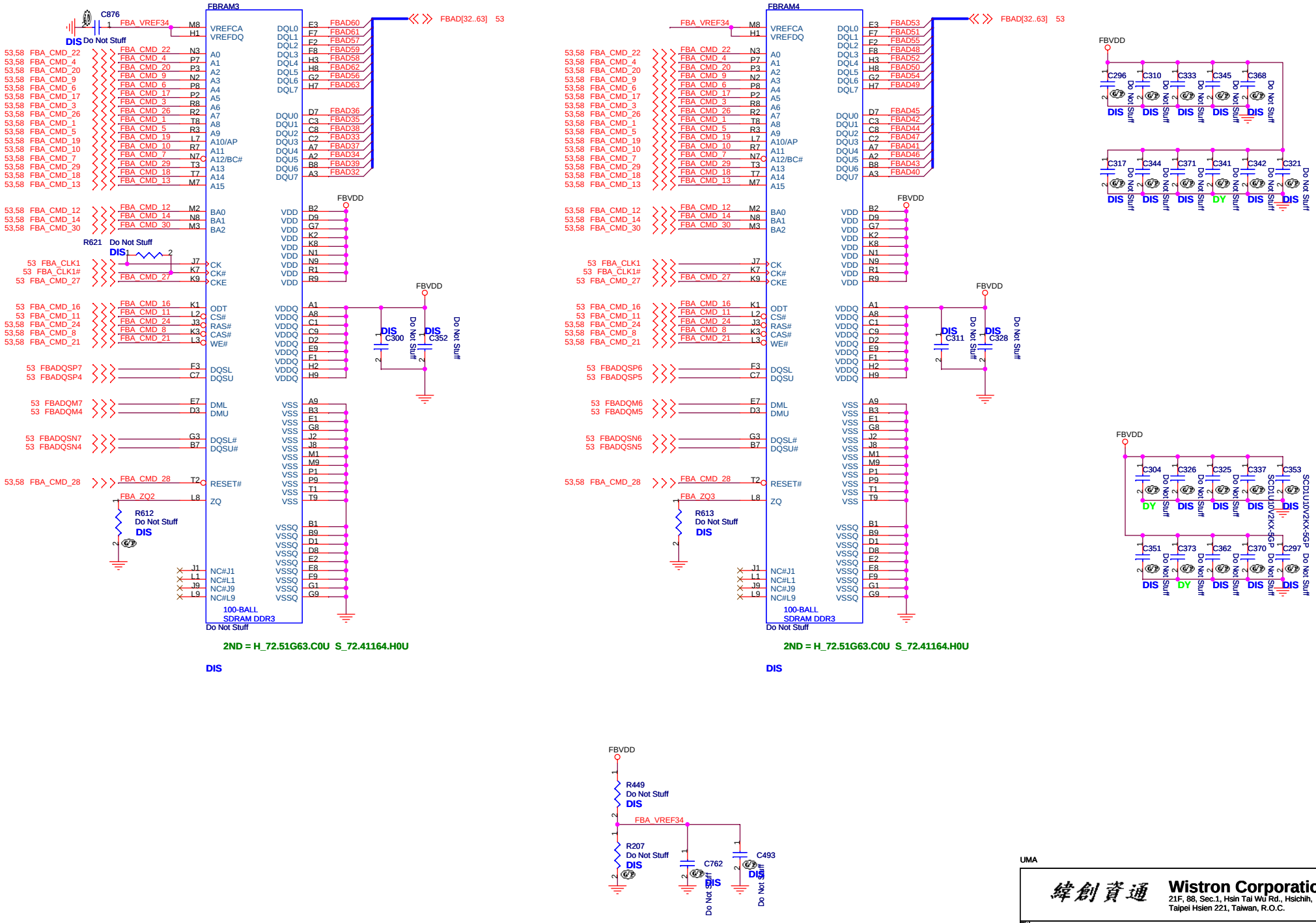
FBRAM3
FBRAM4
C876
DIS
Do Not Stuff
FBA_VREF34
FBAD[32..63] 53
FBVDD
R621
FBA_CLK1
FBA_CLK1#
FBA_CMD_27
FBA_CMD_16
FBA_CMD_11
FBA_CMD_24
FBA_CMD_8
FBA_CMD_21
FBADQSP7
FBADQSP4
FBADQM7
FBADQM4
FBADQSN7
FBADQSN4
FBA_CMD_28
FBA_ZQ2
R612
FBADQSP6
FBADQSP5
FBADQM6
FBADQM5
FBADQSN6
FBADQSN5
FBA_ZQ3
R613
C300
C352
C311
C328
100-BALL
SDRAM DDR3
2ND = H_72.51G63.C0U S_72.41164.H0U
C296
C310
C333
C345
C368
C317
C344
C371
C341
C342
C321
DY
C304
C326
C325
C337
C353
SCD1U10V2KX-5GP
C351
C373
C362
C370
C297
R449
R207
C762
C493
UMA
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.
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UMA

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21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: ***HISTORY***

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