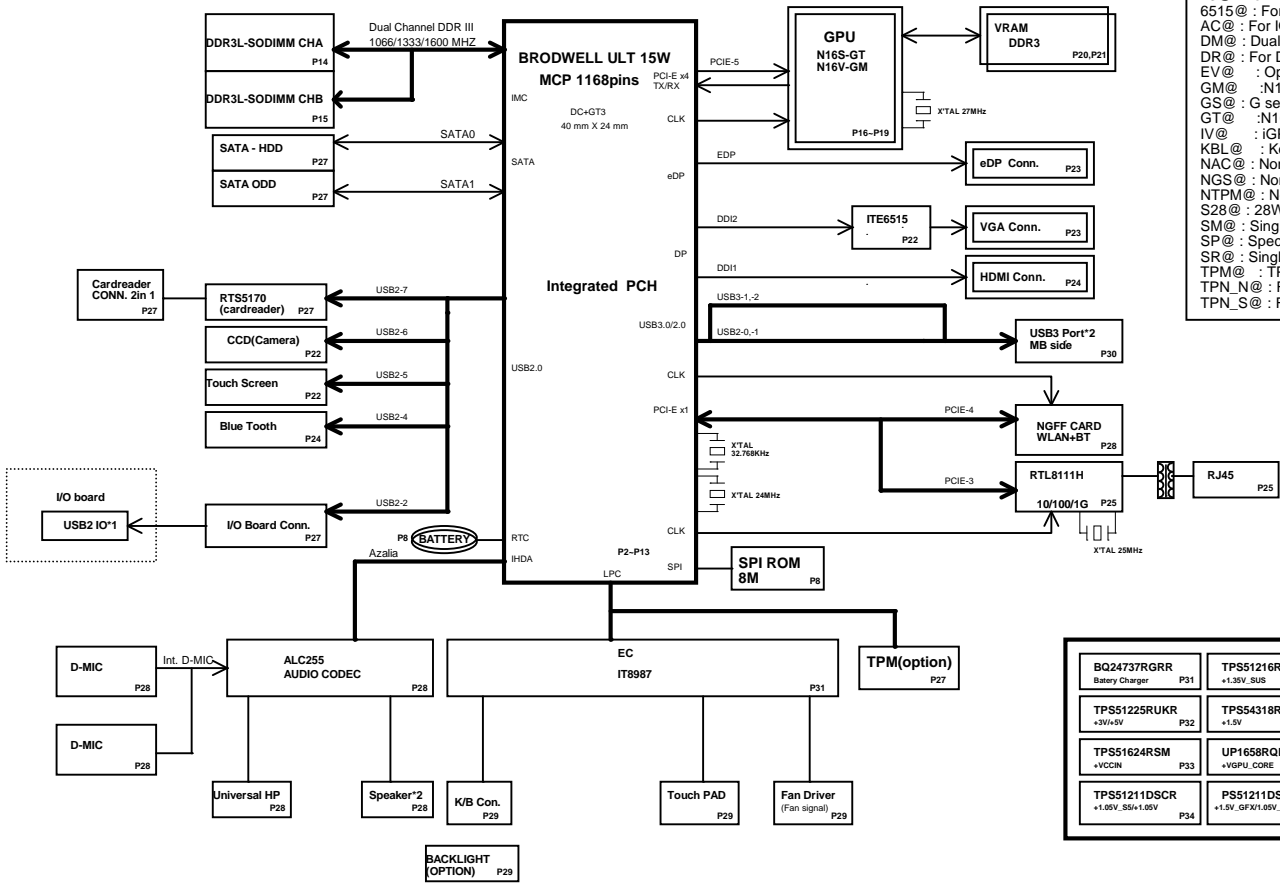


ZRT/ZRTA GDDR3 BWD ULT SYSTEM BLOCK DIAGRAM

BOM

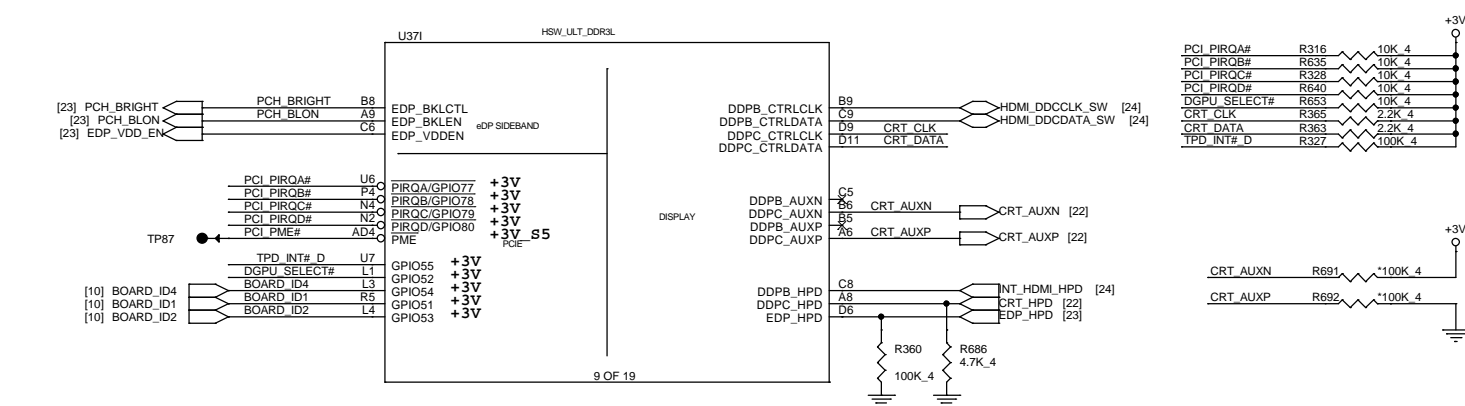
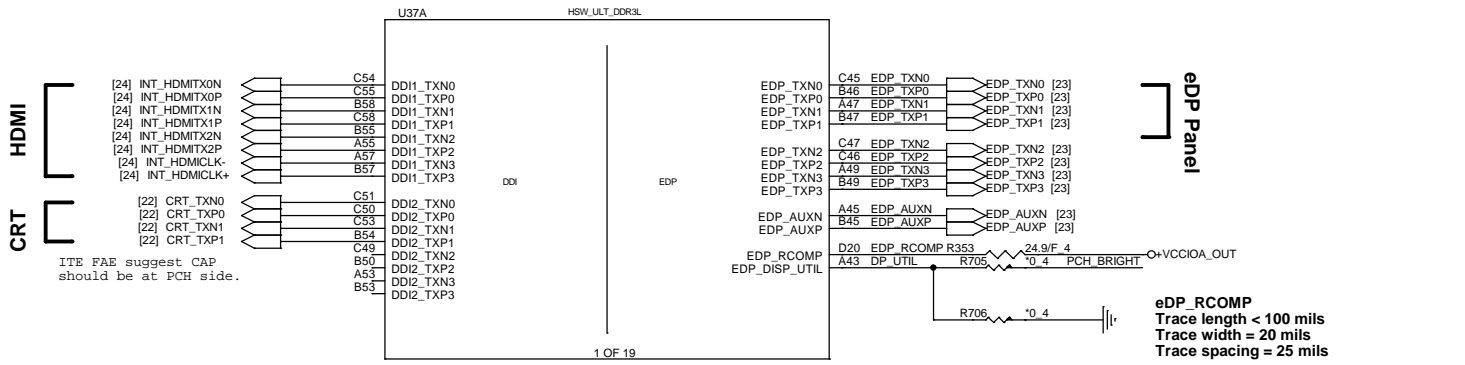


- 15@ : For 15W CPU
- 28@ : For 28W CPU
- 6515@ : For 6515 stuff
- AC@ : For IOAC
- DM@ : Dual MIC
- DR@ : For Dual Rank
- EV@ : Optimus
- GM@ : N16V-GM /WO GC6
- GS@ : G sensor
- GT@ : N16S-GT /GC6
- IV@ : iGPU
- KBL@ : Keyboard backlight
- NAC@ : Non IOAC
- NGS@ : Non G sensor
- NTPM@ : Non TPM
- S28@ : 28W Change BOM
- SM@ : Single MIC
- SP@ : Special
- SR@ : Single Rank
- TPM@ : TPM
- TPN_N@ : For TPM 2.0
- TPN_S@ : For TPM 1.2

BQ24737RGR	TPS51216RUKR	Thermal Protection Discharger
Battery Charger P31	+1.30V_SUS P35	P36
TPS51225RUKR	TPS54318RTER	
+3V/+5V P32	+1.5V P36	
TPS51624RSM	UP1658RQKF	
+VCCIN P33	+VGPU_CORE P37	
TPS51211DSCR	PS51211DSCR	
+1.00V_S5/+1.00V P34	+1.5V_GFX/+1.00V_GFX/+3V_GFX P38	

Haswell ULT (DISPLAY, eDP)

Laptopblue



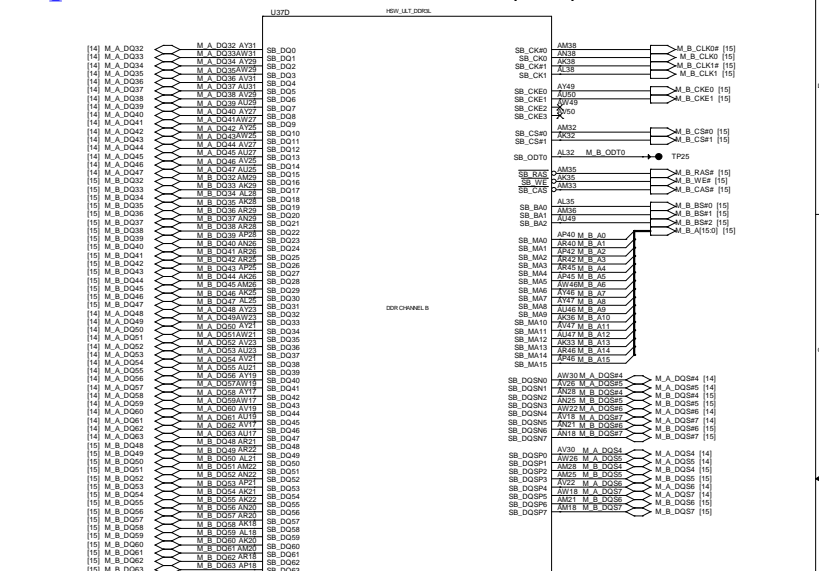
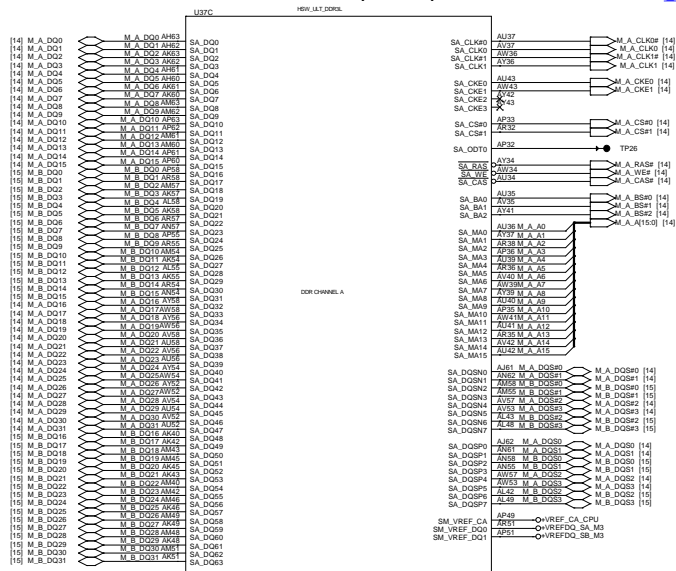
Quanta Computer Inc.


PROJECT : ZRT/ZRTA

Size	Document Number	Rev
	Haswell 3/5 (DDI/eDP)	3A
Date:	Wednesday, February 11, 2015	Sheet 2 of 44

Haswell ULT (DDR3L)

Haswell Processor (DDR3)




Quanta Computer Inc.
 PROJECT : ZRT / ZRTA

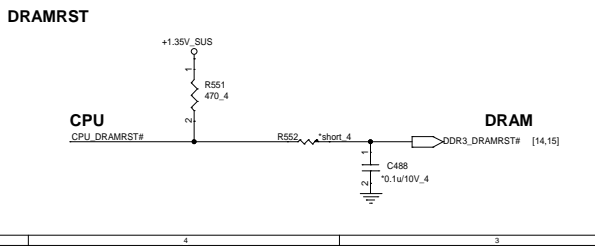
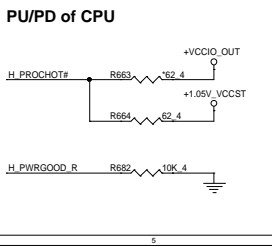
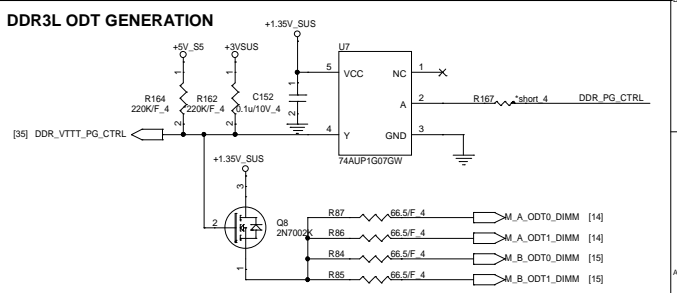
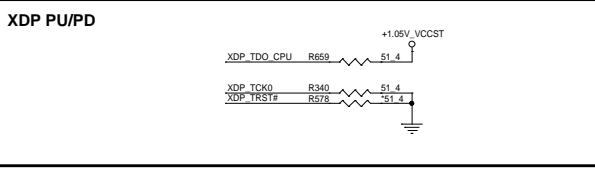
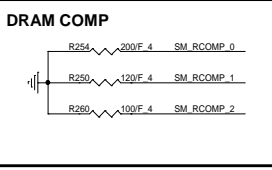
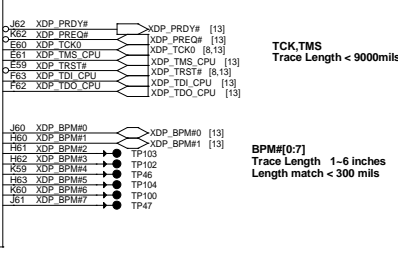
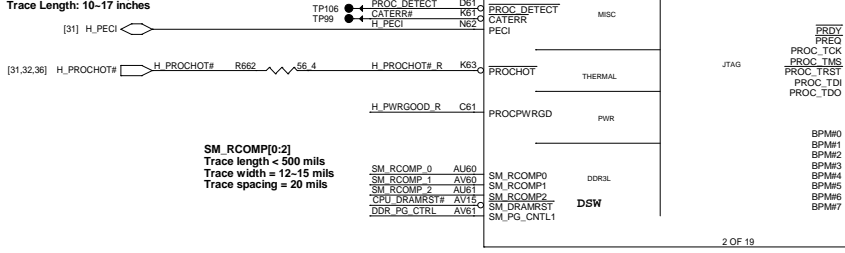
Rev	3A
Date:	Wednesday, February 11, 2015
Esheet	3 of 44

Haswell ULT (SIDE BAND)

H_PECI (50ohm)
 Route on microstrip only
 Spacing >18 mils
 Trace Length: 0.4-6.125 inches

H_PWRGOOD (50ohm)
 Trace Length: 1-11.25 inches

CPU_PLTRST# (50ohm)
 Trace Length: 10-17 inches



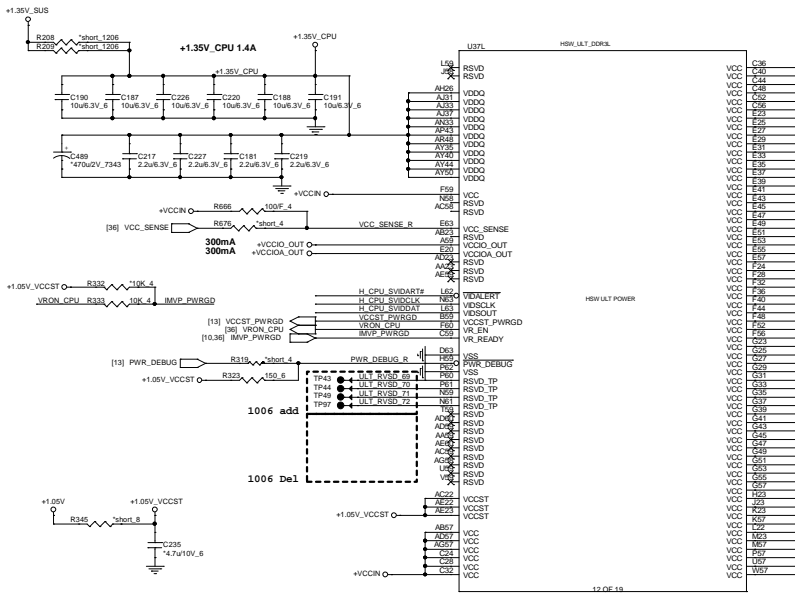
Quanta Computer Inc.
PROJECT : ZRT / ZRTA

Size	Document Number	Rev
	Haswell 1/5 (PEG/DMI/FDI)	3A
	Date: Wednesday, February 11, 2015	Sheet 4 of 44

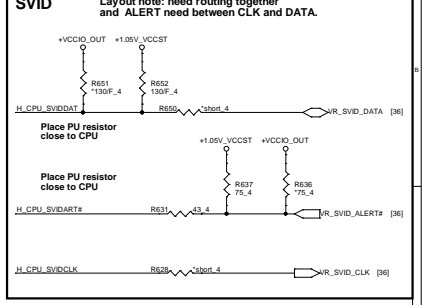
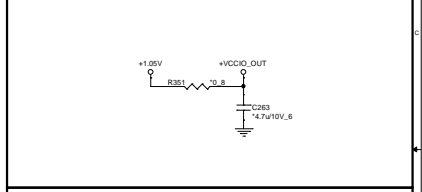
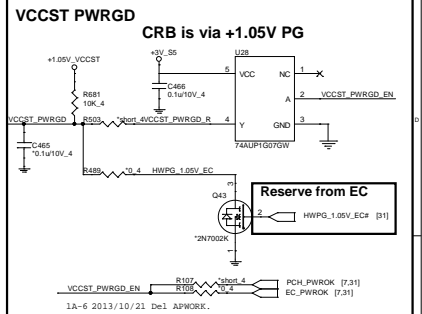
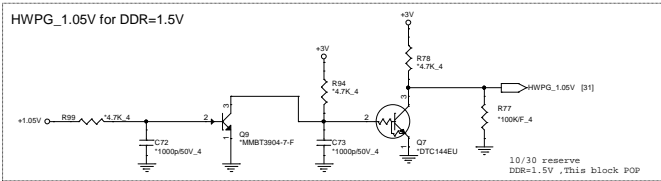
Laptopblue

VDDQ Output Decoupling Recommendations		
330uFx2	7343	BOT socket side
22uF x11	0805	5 on TOP, 6 on BOT inside socket cavity
10uF x10	0805	5 on TOP, 5 on BOT inside socket cavity

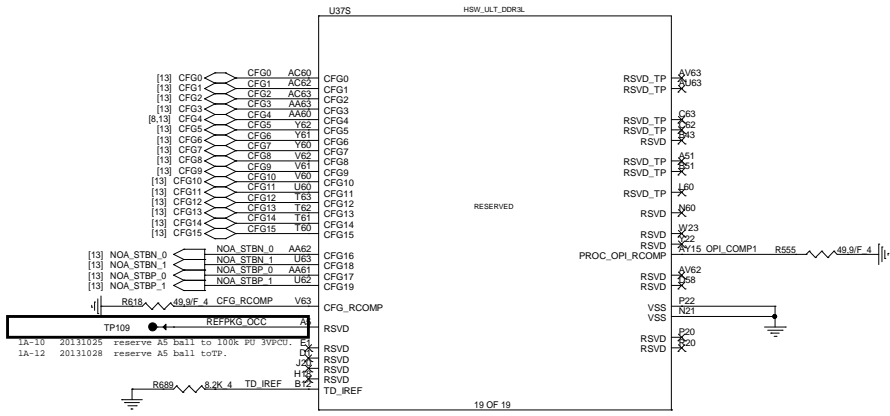
Haswell ULT (POWER)



VCC Output Decoupling Recommendations		
470uF x4	7343	TOP socket side
22uF x8	0805	4 on TOP, 4 on BOT near socket edge
22uF x11	0805	TOP, inside socket cavity
10uF x11	0805	BOT, inside socket cavity




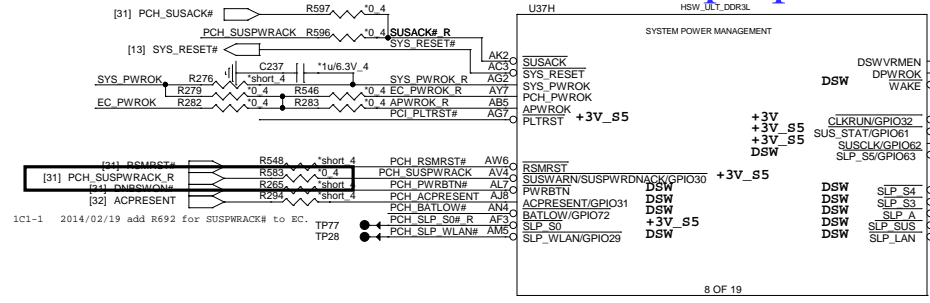
Quanta Computer Inc.
PROJECT : ZRT / ZRTA
Document Number: Haswell 45 (POWER)
 Date: Wednesday, February 11, 2015 11:20:15 AM Sheet: 5 of 44



Processor Strapping

	1	0	
CFG0 EAR-STALL/NOT STALL RESET SEQUENCE AFTER PCU PLL IS LOCKED	(DEFAULT) NORMAL OPERATION; NO STALL	STALL	CFG0 R289 ~1K 4
CFG1 PCH/ PCH LESS MODE SELECTION	(DEFAULT) NORMAL OPERATION	PCH-LESS MODE	CFG1 R606 ~1K 4
CFG3 PHYSICAL_DEBUG_ENABLED (DFX PRIVACY)	DISABLED NO PHYSICAL DISPLAY PORT ATTACHED TO EMBEDDED DISPLAY PORT	ENABLED AN EXTERNAL DISPLAY PORT DEVICE IS CONNECTED TO THE EMBEDDED DISPLAY PORT	CFG3 R610 ~1K 4
CFG 8 ALLOW THE USE OF NOA ON LOCKED UNITS	DISABLED/DEFAULT; IN THIS CASE, NOA WILL BE DISABLED IN LOCKED UNITS AND ENABLED IN UN-LOCKED UNITS	ENABLED; NOA WILL BE AVAILABLE REGARDLESS OF THE LOCKING OF THE UNIT	CFG8 R614 ~1K 4
CFG9 NO SVID PROTOCOL CAPABLE VR CONNECTED	VRS SUPPORTING SVID PROTOCOL ARE PRESENT	NO VR SUPPORTING SVID IS PRESENT. THE CHIP WILL NOT GENERATE (OR RESPOND TO) SVID ACTIVITY	CFG9 R619 ~1K 4
CFG10 SAFE MODE BOOT	POWER FEATURES ACTIVATED DURING RESET	POWER FEATURES (ESPECIALLY CLOCK GATING) ARE NOT ACTIVATED	CFG10 R295 ~1K 4

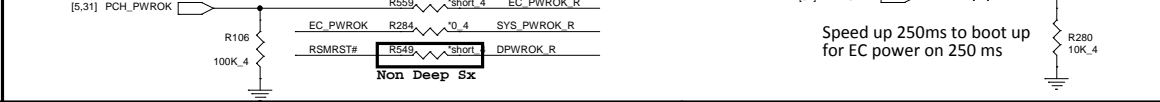
 **Quanta Computer Inc.**
PROJECT : ZRT / ZRTA
Haswell 5/5 (CFG/GND)
 Date: Wednesday, February 11, 2015 Sheet 6 of 44



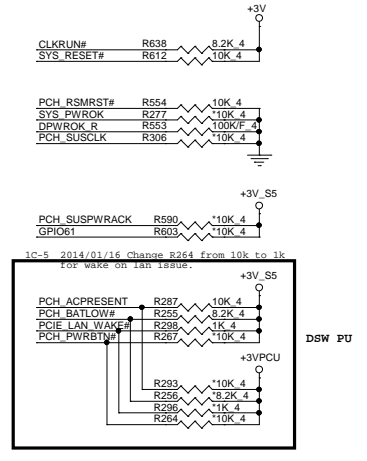
IC1-1 2014/02/19 add R692 for SUSPWACK# to EC.

IC-5 2014/01/16 Change R264 from 10K to 1K for wake on lan issue.

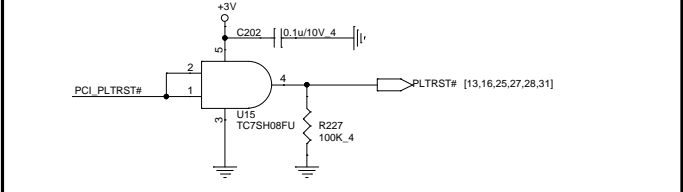
Power Sequence



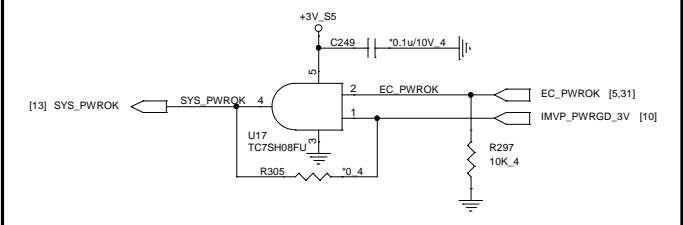
PCH PM PU/PD



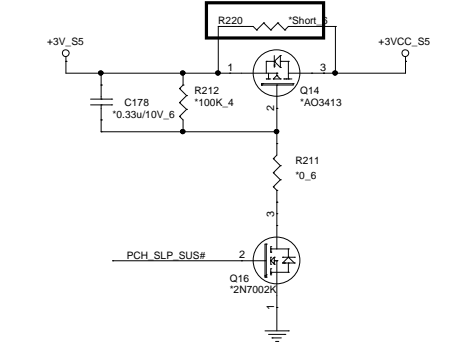
PLTRST# Buffer



SYSPWOK



Deep Sx Circuit



Quanta Computer Inc.
PROJECT : ZRT / ZRTA

Size	Document Number	Rev
	LPT 1/6 (DM/BD/VGA)	3A

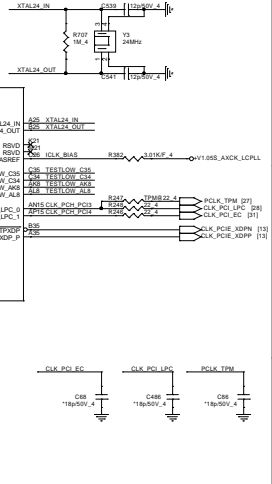
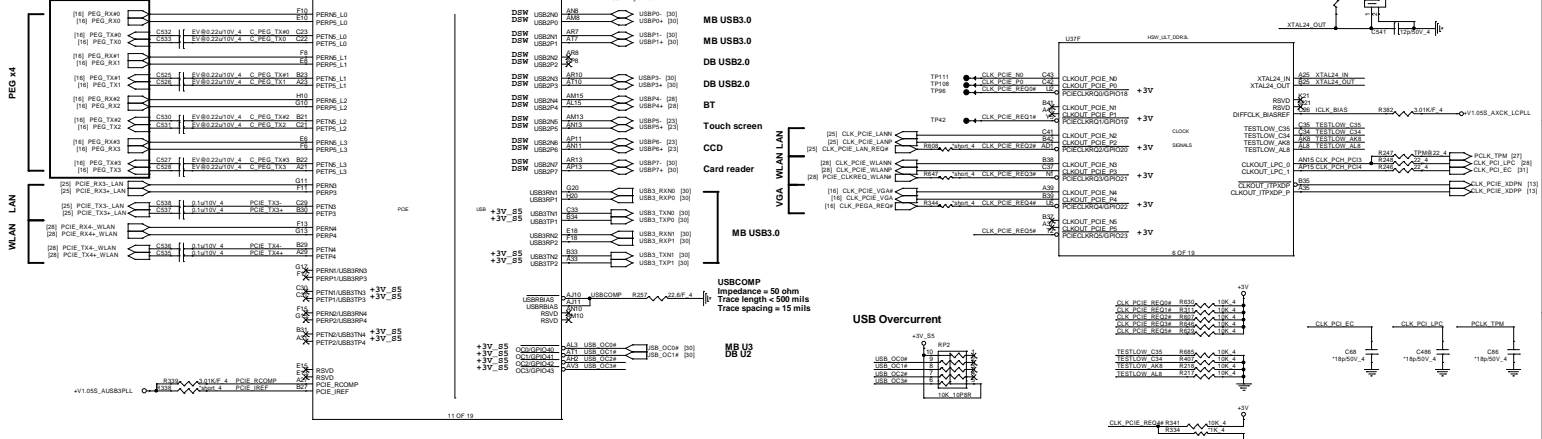
Date: Wednesday, February 11, 2015 Sheet 7 of 46

1A-6 2013/10/21 several P8G lan for layout.

1A-8 2013/10/21 Swap P82 to normal mode.

1A-1 2013/10/15 following up acer define and swap USB3 and USB2

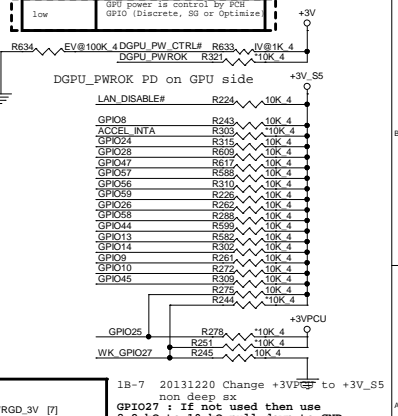
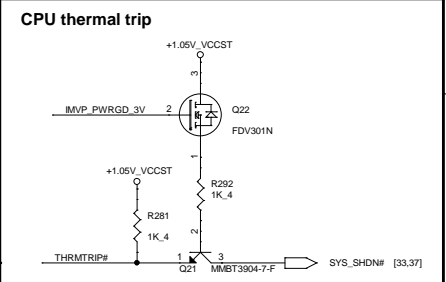
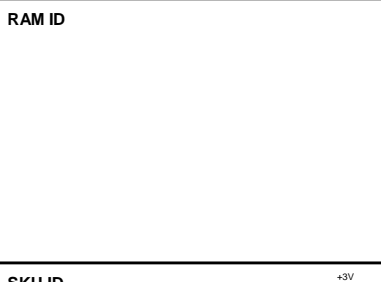
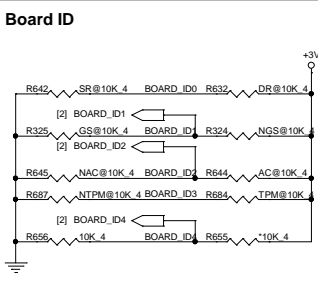
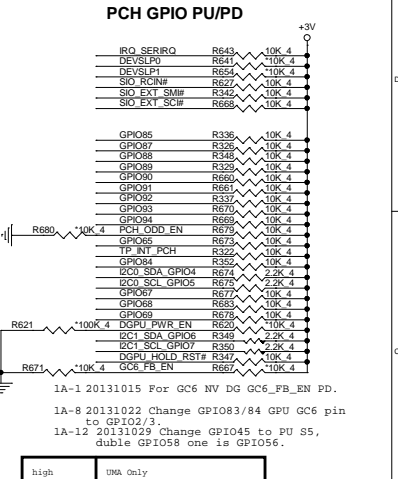
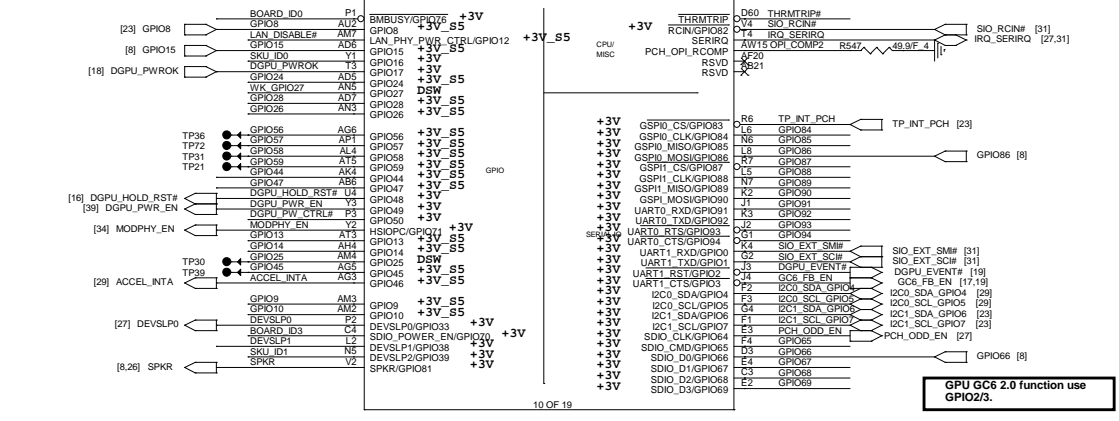
USB2 port.



Quanta Computer Inc.
PROJECT : ZRT/ZRTA
LPT 3/6 (PCIE/USB/CLK)
 Date: Wednesday, 1 February 11, 2015 Page: 9 of 24

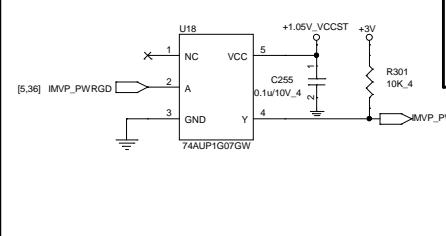
Haswell ULT PCH (GPIO,CPU/Misc,NCIF)

GPIO#	High	Low
[23] GPIO8	Touch panel	No touch panel



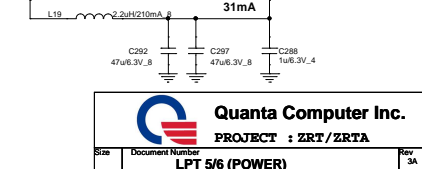
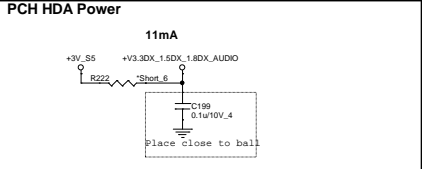
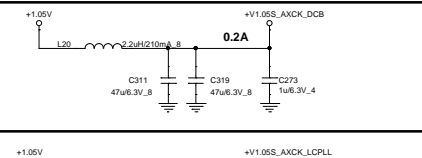
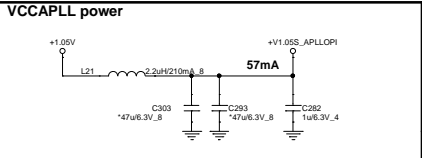
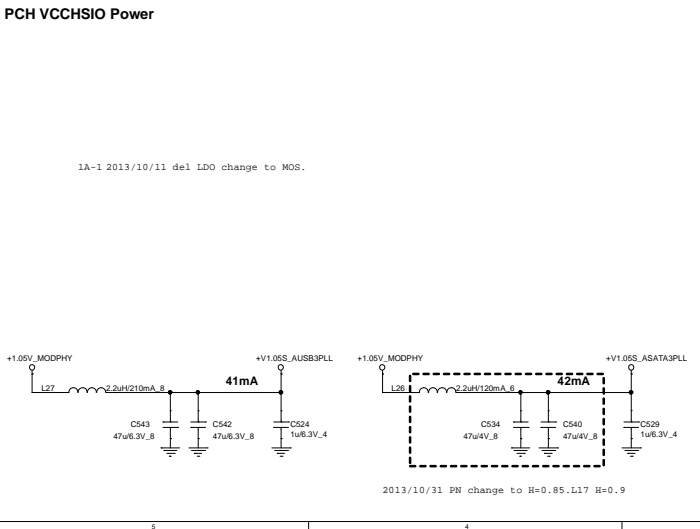
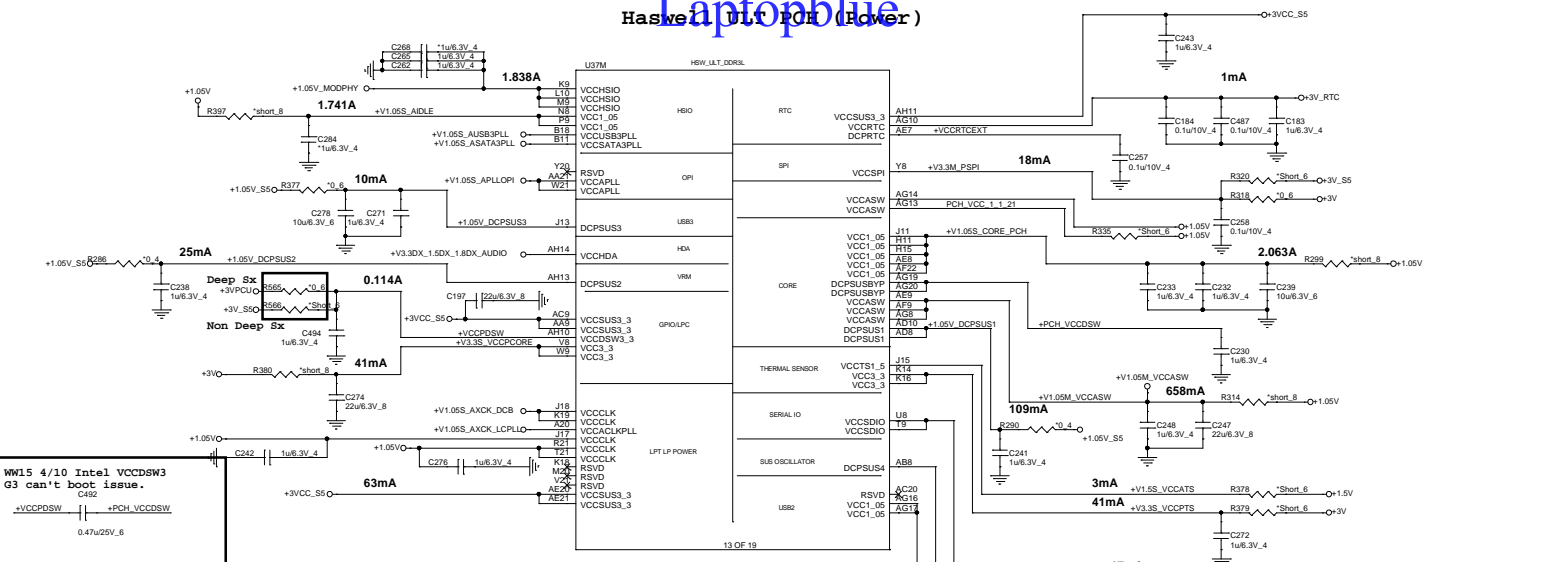
BOARD_ID#	Low	High
BOARD_ID0	single rank SKU	Dual rank SKU
BOARD_ID1	Reserved (Default)	Reserve
BOARD_ID2	No IOAC	IOAC
BOARD_ID3	No TPM	TPM
BOARD_ID4	Non-Dolly (Default)	Dolly


SKU_ID#	SKU_ID#	VIA H/W signal	Setup Menu	UMA boot	GPU boot	UMA+GPU boot
UMA Only	0	0	UMA	Hidden	UMA boot	
dGPU Only	0	1	GPU	Hidden	GPU boot	
Switchable (Flex)	1	0	UMA+GPU	dGPU/S0	UMA boot	
Optimize (MaxLess)	1	1	UMA	UMA/S0	UMA boot	



Quanta Computer Inc.
PROJECT : ZRT/ZRTA

Size: Document Number **LPT 4/6 (GPIO/MISC)** Rev 3A
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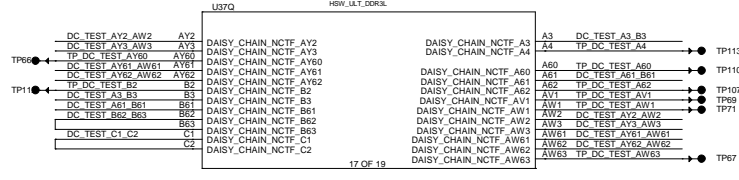
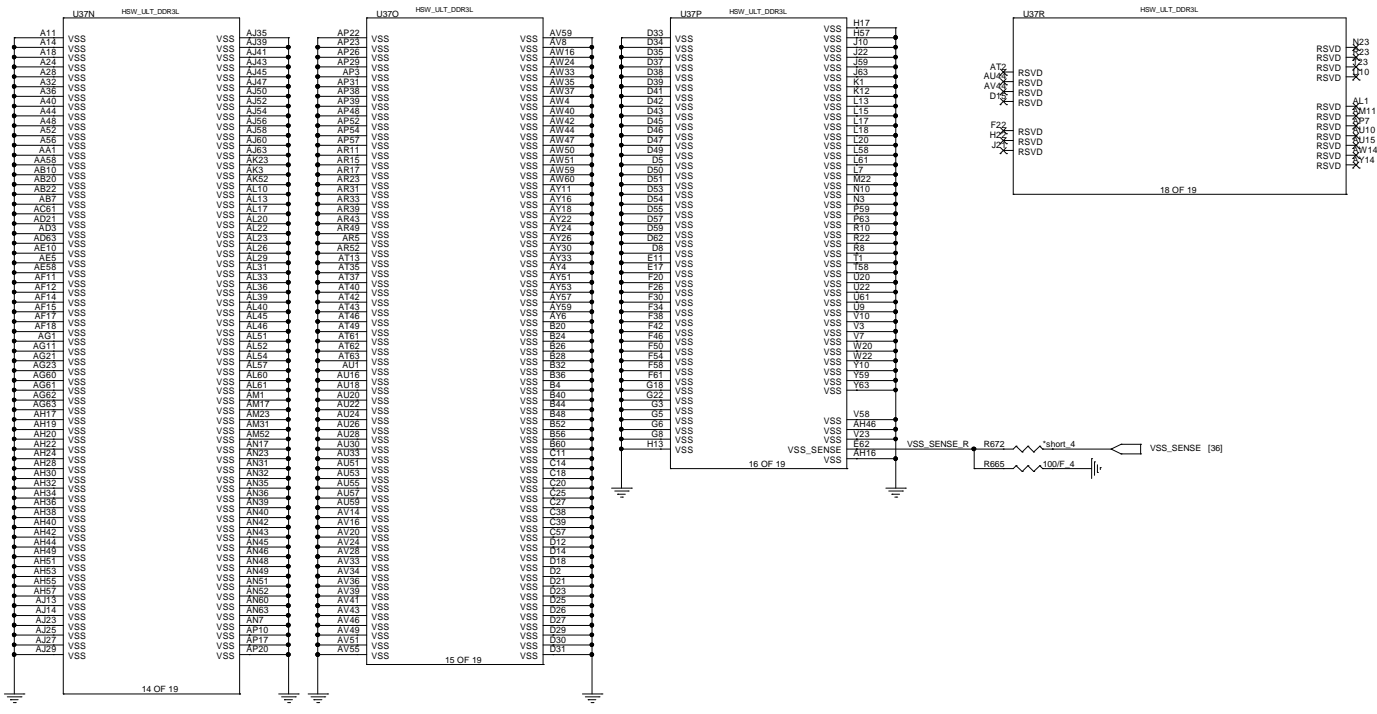




Quanta Computer Inc.
PROJECT : ZRT / ZRTA

Size	Document Number	Rev	3A
LPT 5/6 (POWER)			
Date:	Wednesday, February 11, 2015	Sheet	11 of 44

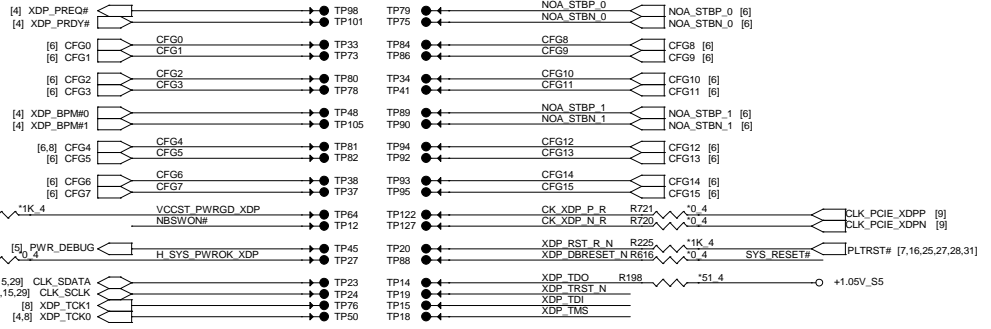
Haswell ULT (GND)



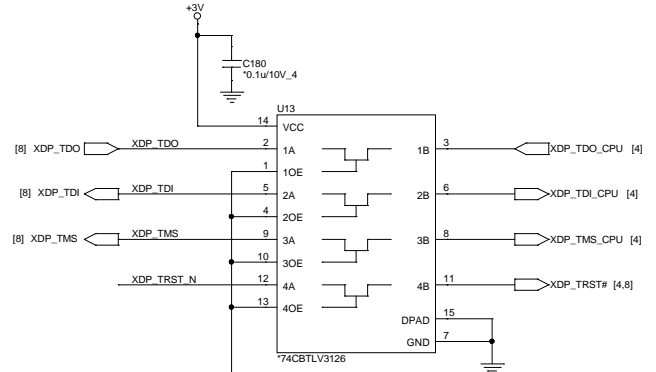
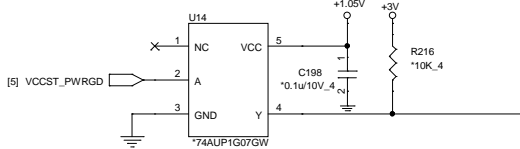
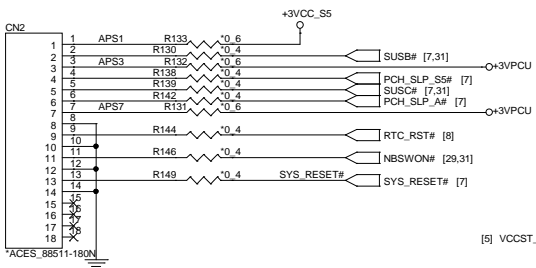
Quanta Computer Inc.
PROJECT : ZRT/ZRTA

Size	Document Number	Rev
	LPT 6/6 (GND)	3A
Date	Wednesday, February 11, 2016	Sheet 12 of 44

Laptopblue

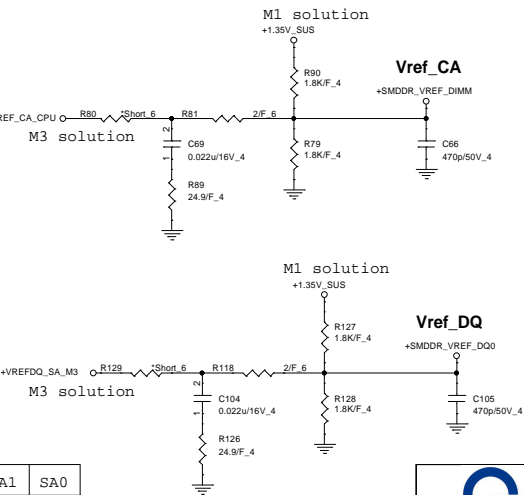
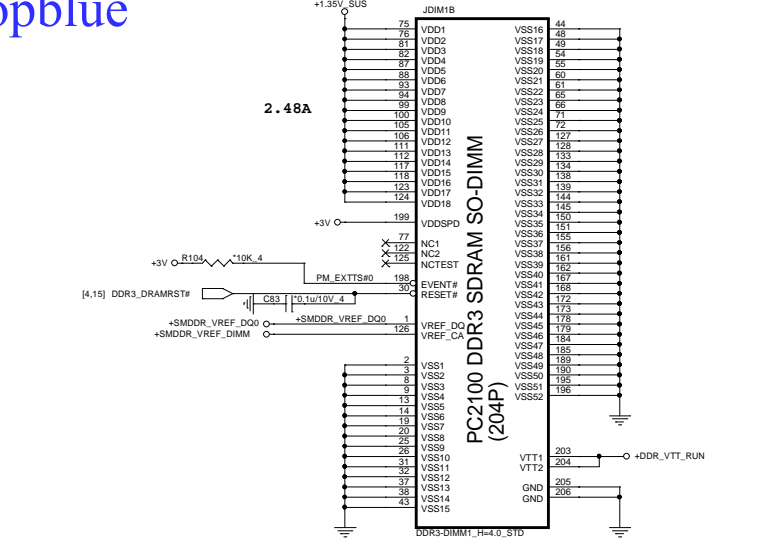
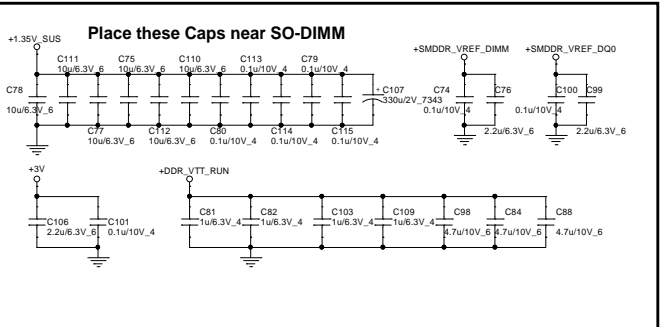
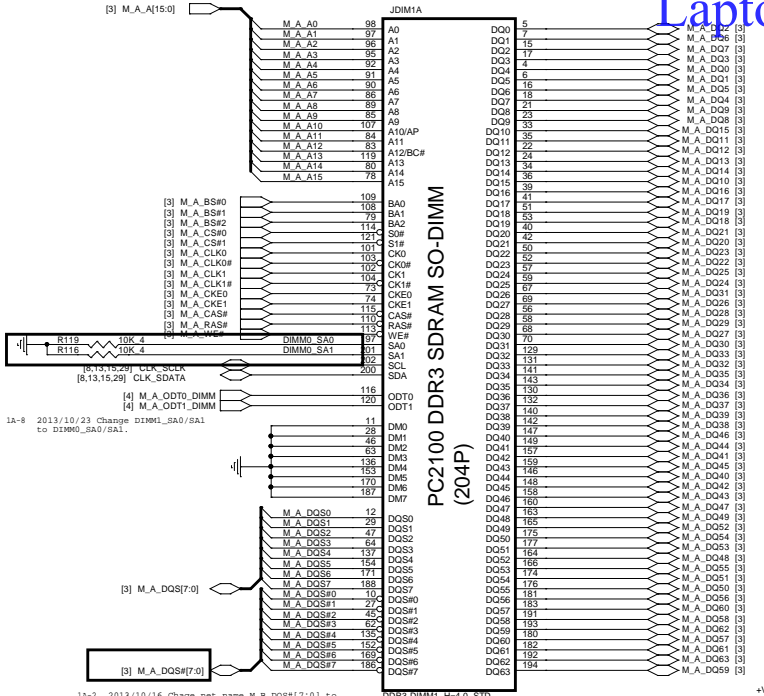


APS



Quanta Computer Inc.
PROJECT : ZRT/ZRTA

Size	Document Number	Rev
	CPU/PCH XDP	3A
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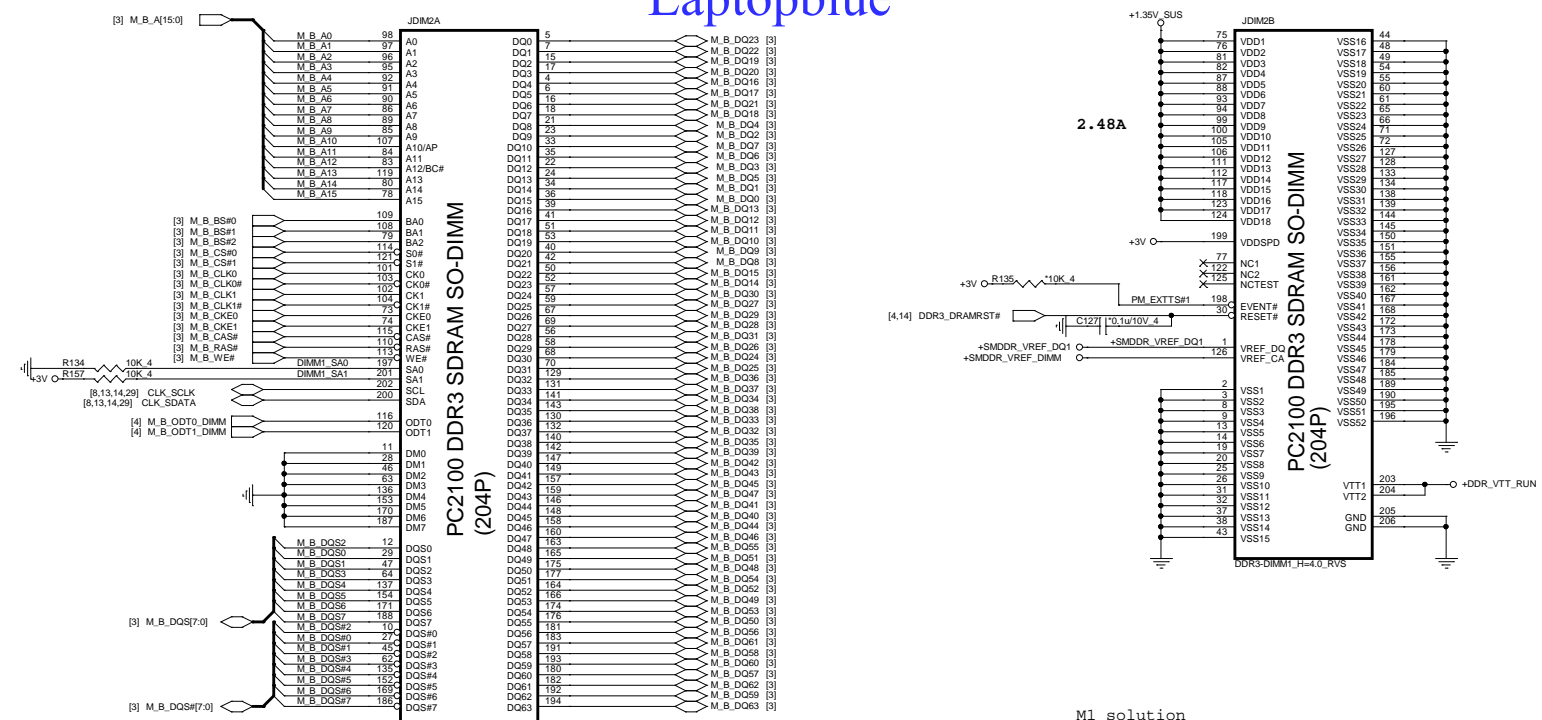


	SA1	SA0
CHA	0	0
CHB	1	0

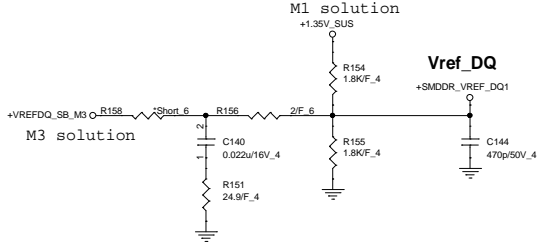
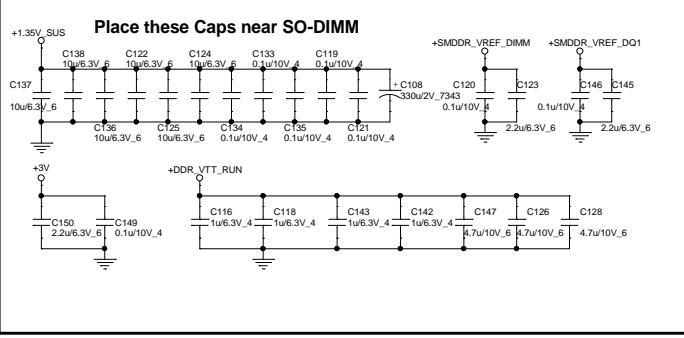
Quanta Computer Inc.
PROJECT : ZRT / ZRTA

Size	Document Number	Rev
	DDR3 MEMORY SO-DIMM A	3A
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Laptopblue



1A-22013/10/16 Swap M_B_DQS2/M_B_DQS3 and swap M_B_DQS#2/M_B_DQS#3.



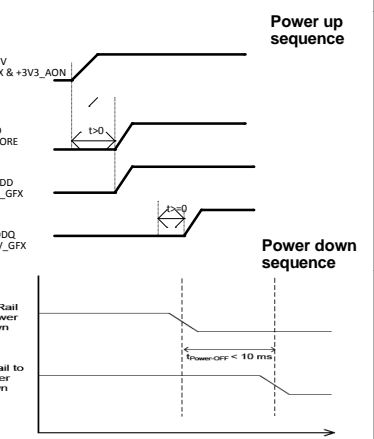
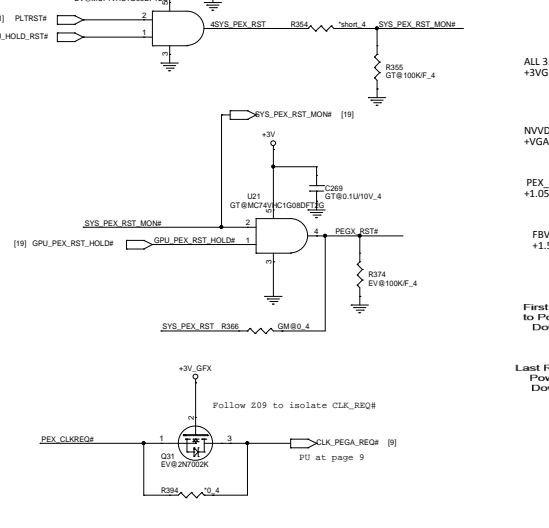
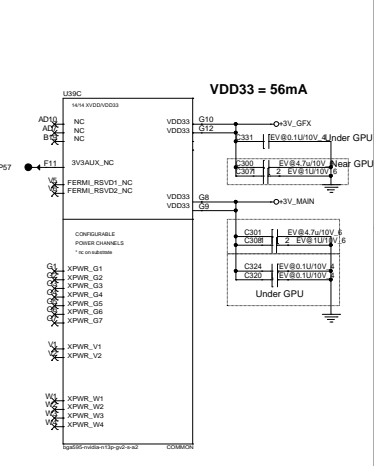
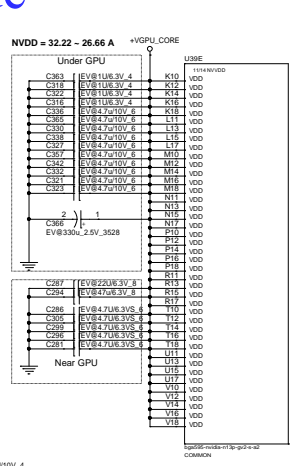
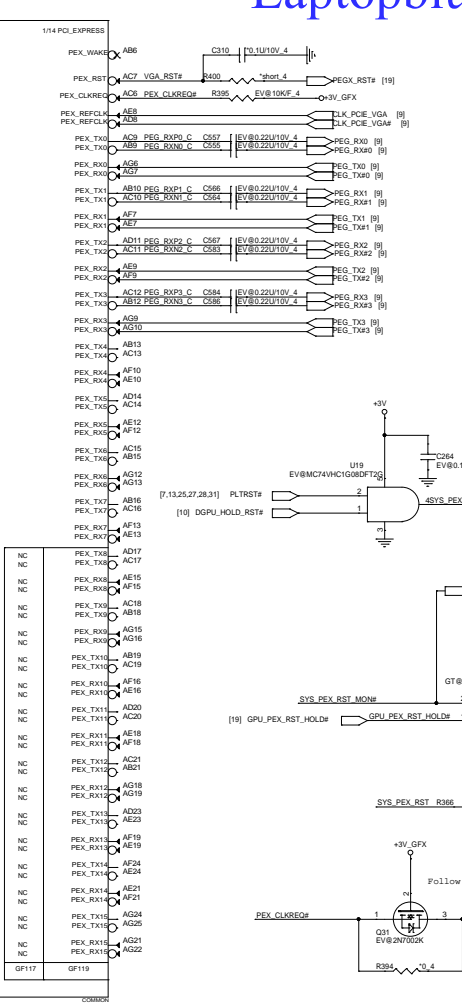
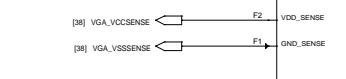
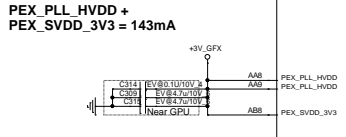
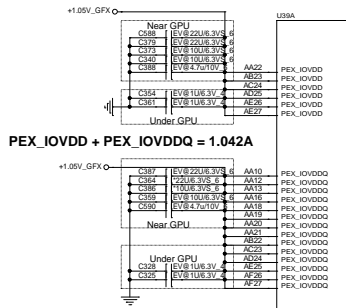
	SA1	SA0
CHA	0	0
CHB	1	0



Quanta Computer Inc.
PROJECT : ZRT/ZRTA

Size: _____ Document Number: _____ Rev: 3A
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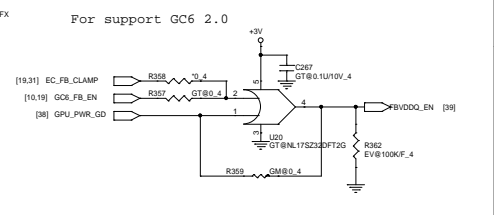
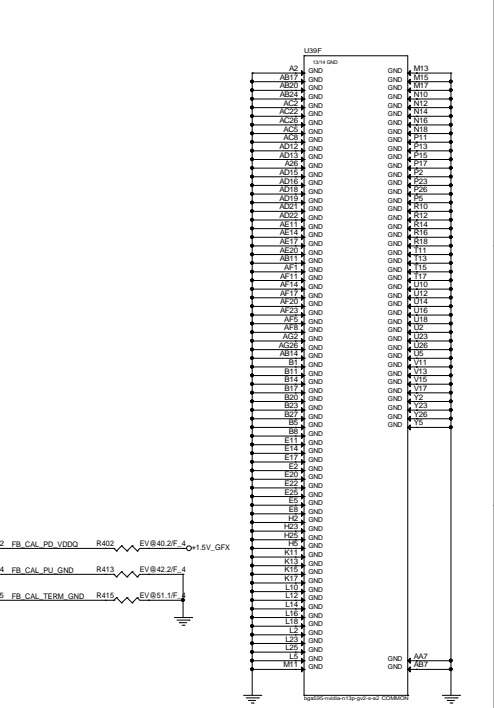
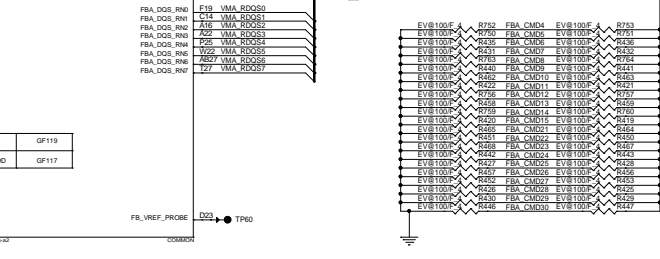
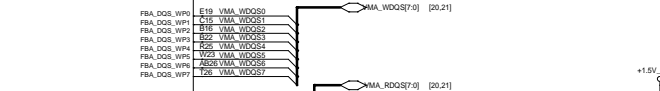
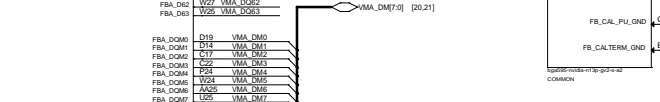
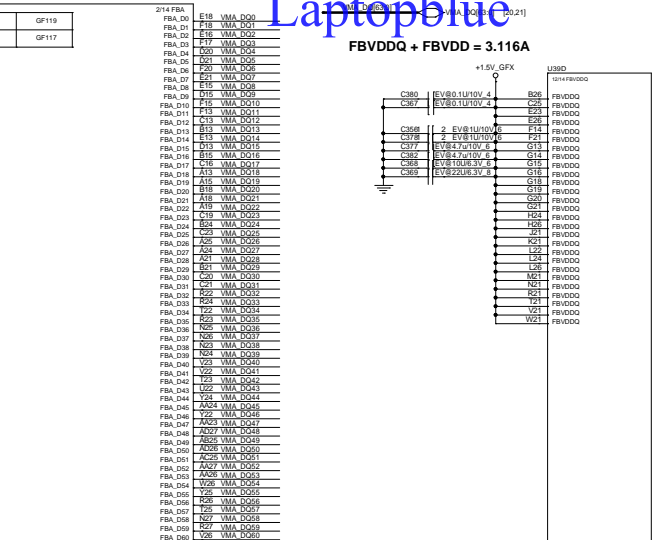
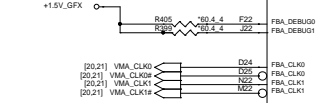
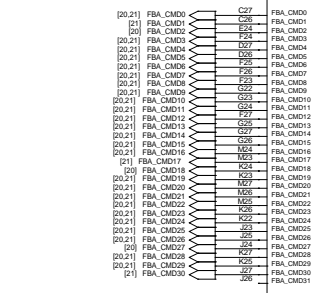
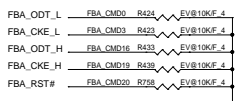
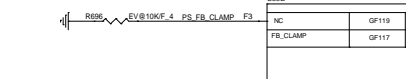
Laptopblue



Quanta Computer Inc.
PROJECT : ZRT / ZRTA

Doc: N165-GT (PCIE I/F) NVDD
 Date: Wednesday, February 11, 2015
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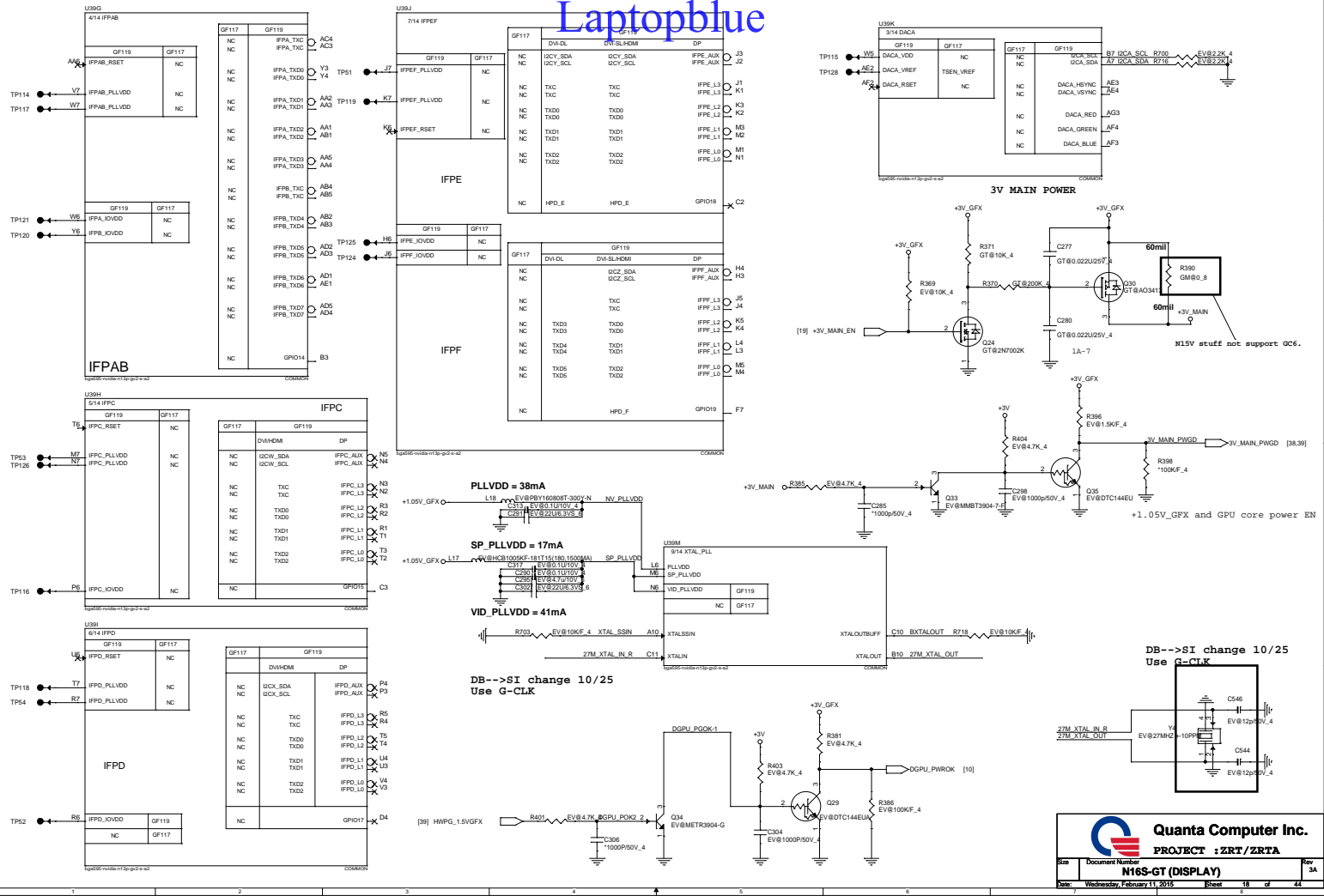
FBVDDQ + FBVDD = 3.116A



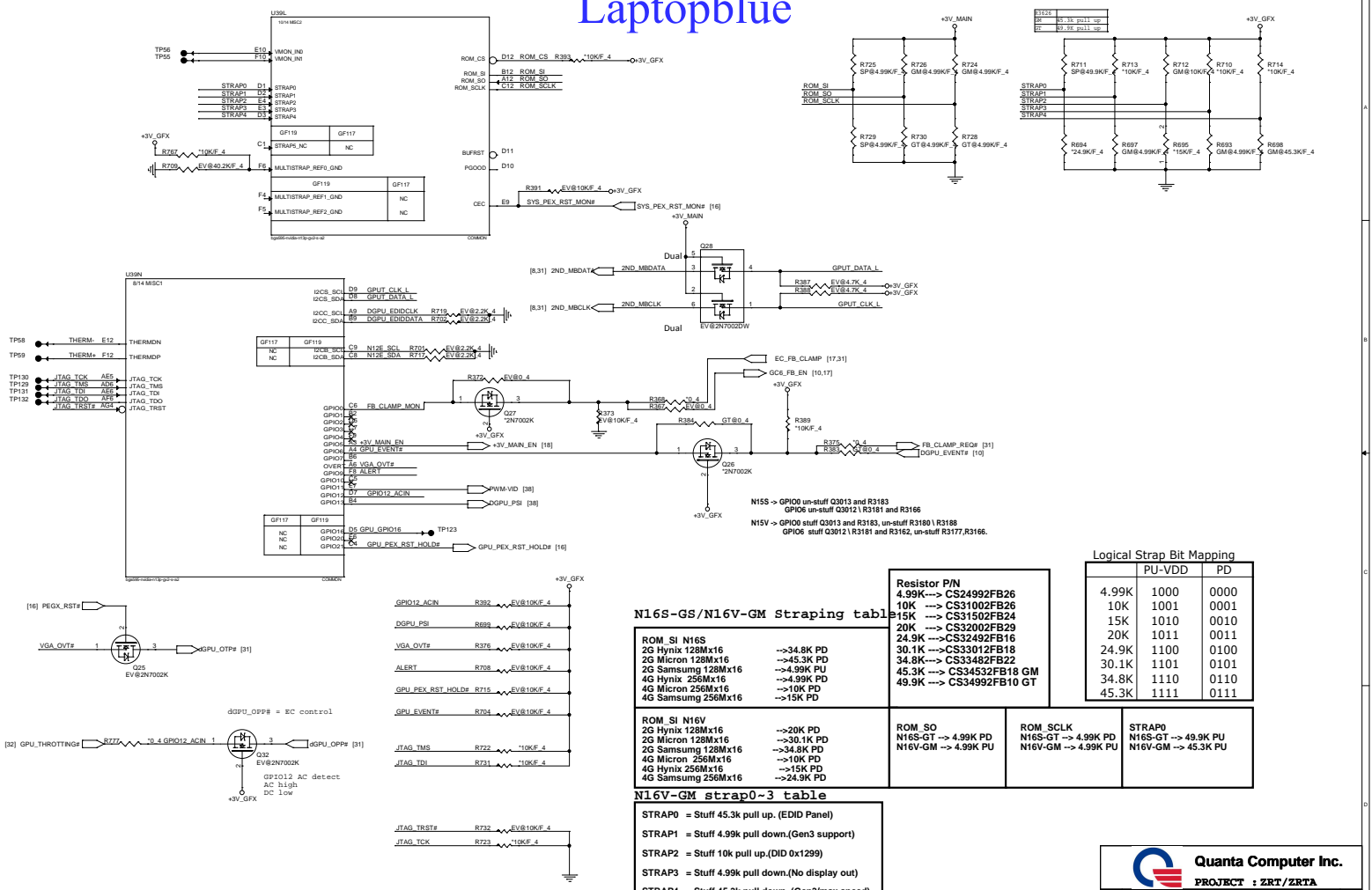
Quanta Computer Inc.
PROJECT : ZRT / ZRTA

Size Document Number: **N6S-GT (MEMORY/GND)** Rev 3A
Date: Wednesday, February 11, 2015 Sheet 17 of 44

Laptopblue



Laptopblue



N16S-GS/N16V-GM Strapping table

Component	Value	Part
ROM_SI N16S		
2G Hynix 128Mx16	-->	34.8K PD
2G Micron 128Mx16	-->	45.3K PD
2G Samsung 128Mx16	-->	4.99K PU
4G Hynix 256Mx16	-->	4.99K PD
4G Micron 256Mx16	-->	10K PD
4G Samsung 256Mx16	-->	15K PD
ROM_SO		
N16S-GT	->	4.99K PD
N16V-GM	->	4.99K PU
ROM_SCLK		
N16S-GT	->	4.99K PD
N16V-GM	->	4.99K PU
STRAP0		
N16S-GT	->	49.9K PU
N16V-GM	->	45.3K PU

Logical Strap Bit Mapping

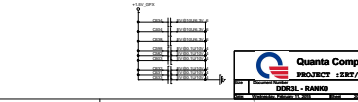
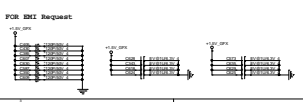
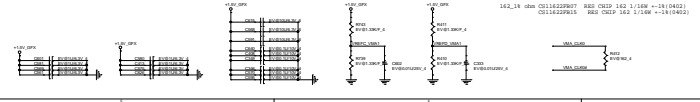
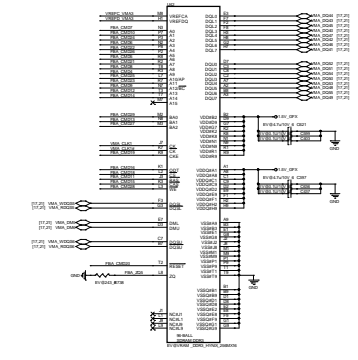
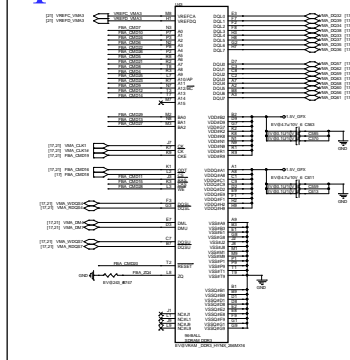
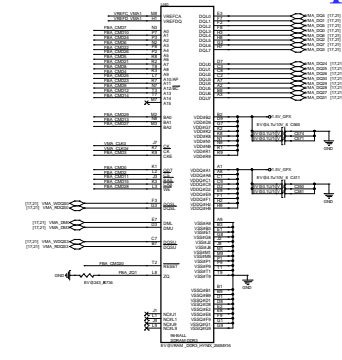
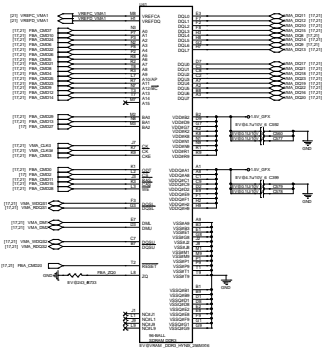
PU-VDD	PD
4.99K	1000
10K	1001
15K	1010
20K	1011
24.9K	1100
30.1K	1101
34.8K	1110
45.3K	1111

N16V-GM strap0-3 table

- STRAP0 = Stuff 45.3k pull up. (EDID Panel)
- STRAP1 = Stuff 4.99k pull down.(Gen3 support)
- STRAP2 = Stuff 10k pull up.(DID 0x1299)
- STRAP3 = Stuff 4.99k pull down.(No display out)
- STRAP4 = Stuff 45.3k pull down. (Gen3/max speed)

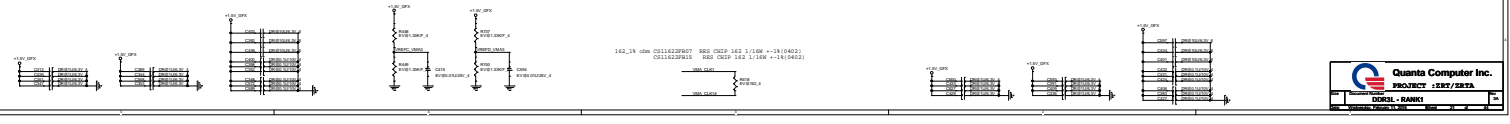
Quanta Computer Inc.
PROJECT : ZRT/ZRTA
Date: Wednesday, February 11, 2014 ESheet 19 of 44
Rev 3A

Laptopblue

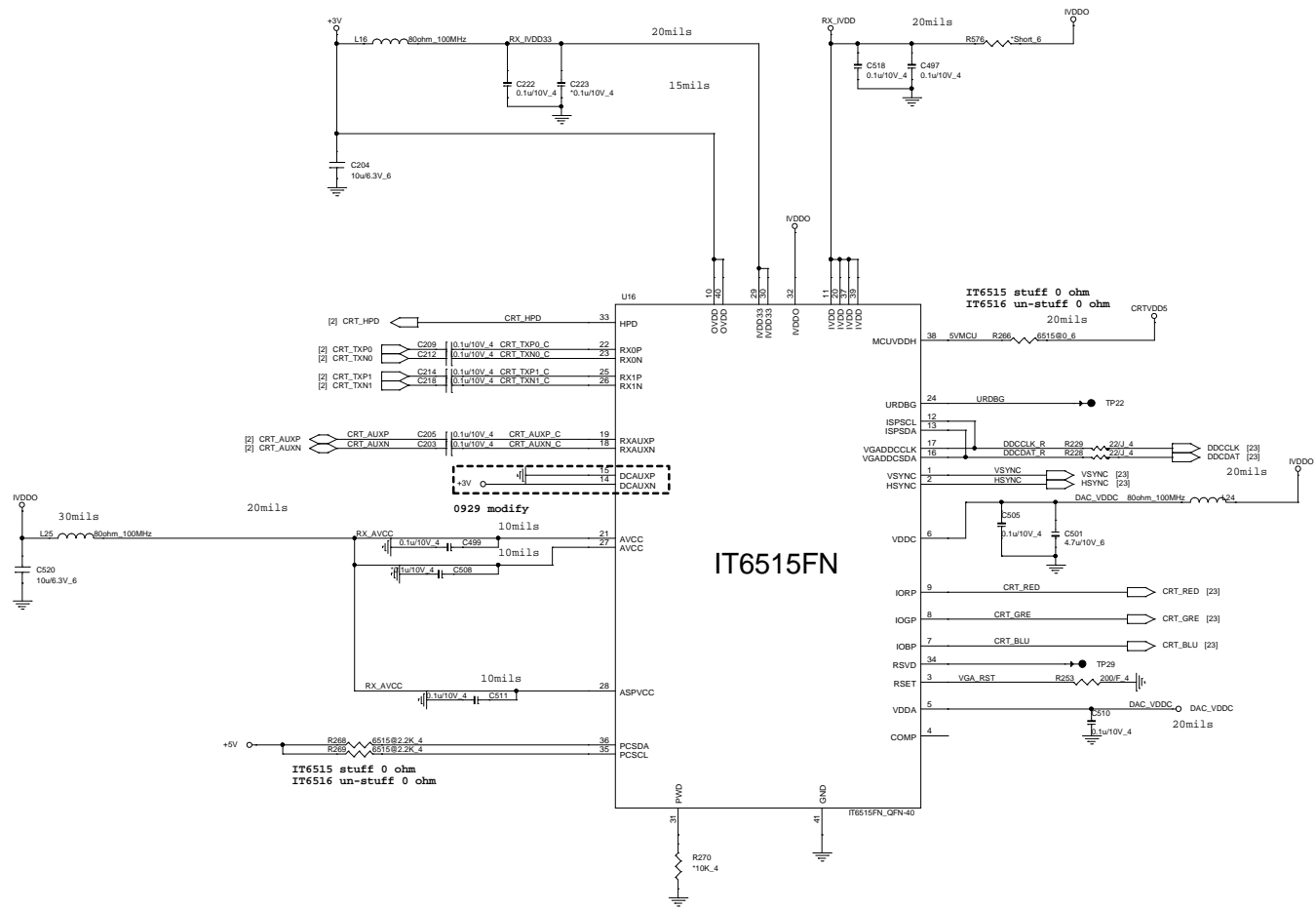


Quanta Computer Inc.
 PROJECT :REV:ZETA
 DORAL-RAVING

Laptopblue

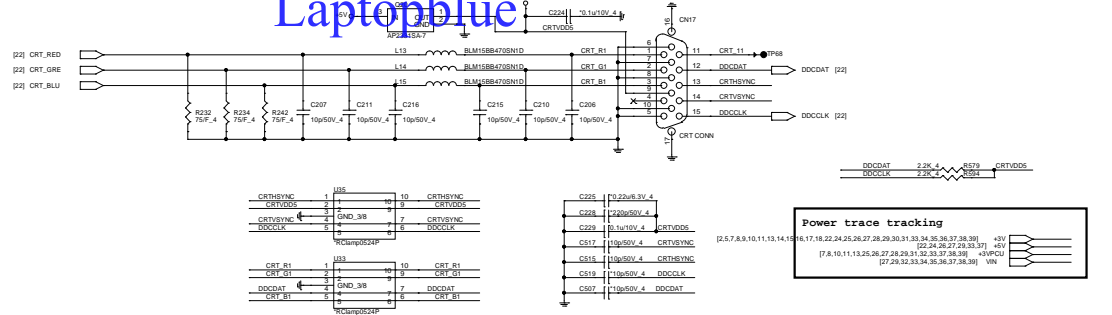
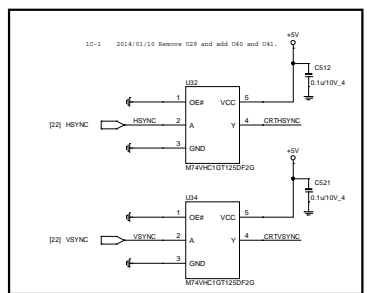


Laptopblue

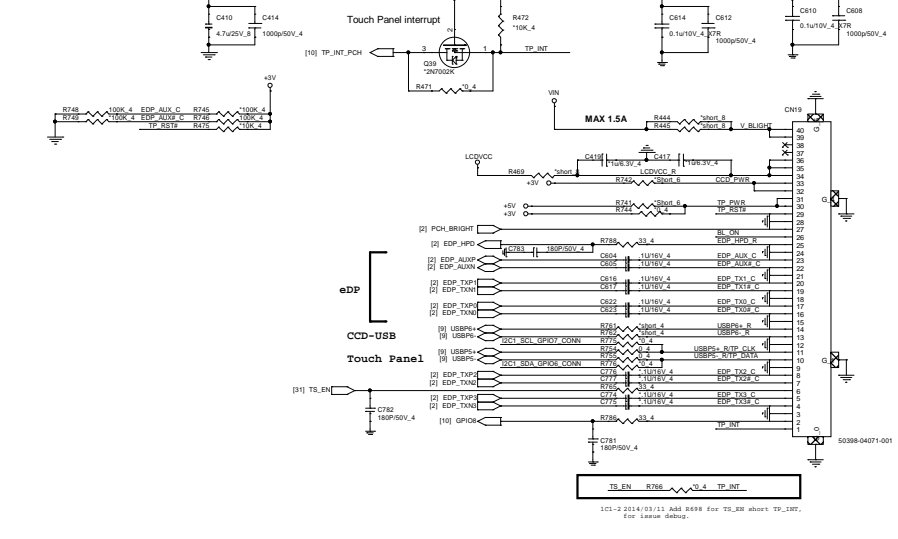


[2,5,7,8,9,10,11,13,14,15,16,17,18,23,24,25,26,27,28,29,30,31,33,34,35,36,37,38,39] +3V
 [23,24,26,27,29,33,37] +5V

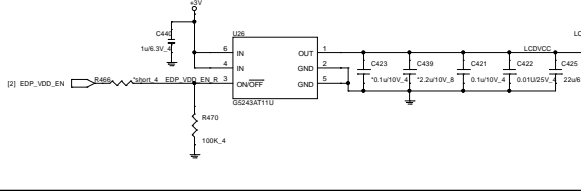
		Quanta Computer Inc.	
		PROJECT : ZRT/ZRTA	
Size	Document Number	Rev	
	DP to VGA IT6165	3A	
Date:	Wednesday, February 11, 2015	Sheet	22 of 44



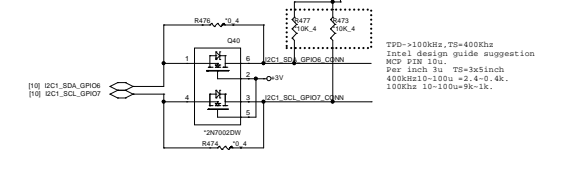
LCD CONNECTOR



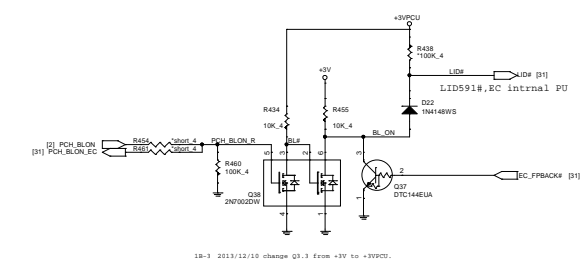
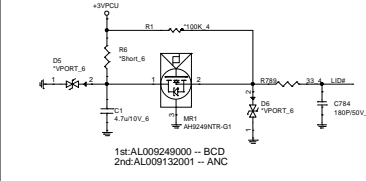
LCD Power



Touch screen level shift I2C(reserve)



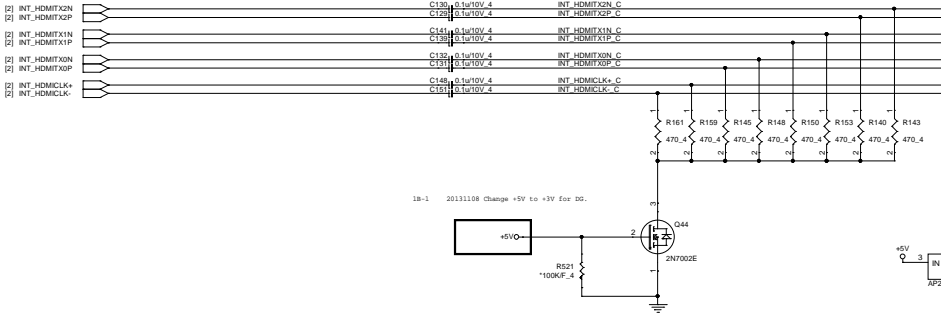
Hall Sensor (HSR)



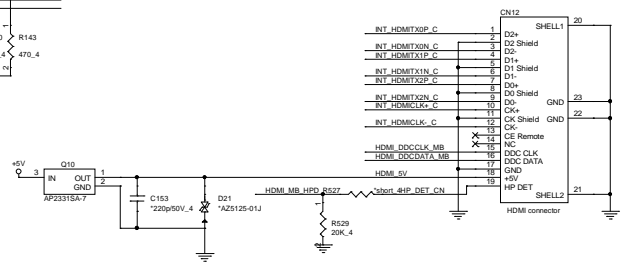
HDMI

Laptopblue

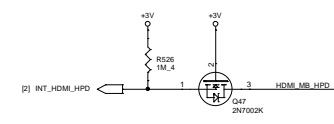
From PCH



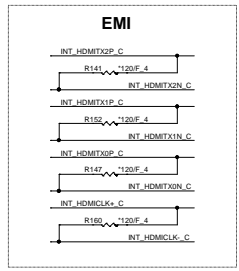
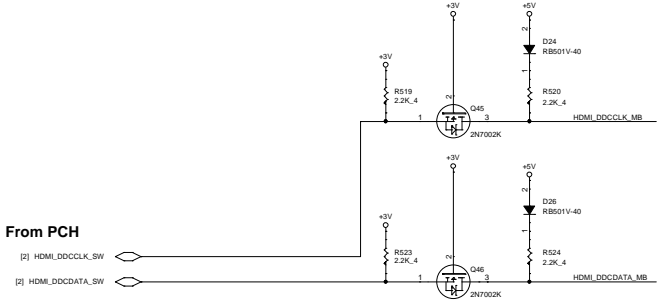
HDMI connector



HDMI-detect



I2C



Power trace tracking

[2,5,7,8,9,10,11,13,14,15] 6,17,18,22,23,25,26,27,28,29,30,31,33,34,35,36,37,38,39] +3V

[23,26,27,29,33,37] +5V

Quanta Computer Inc.

PROJECT : ZRT/ZRTA

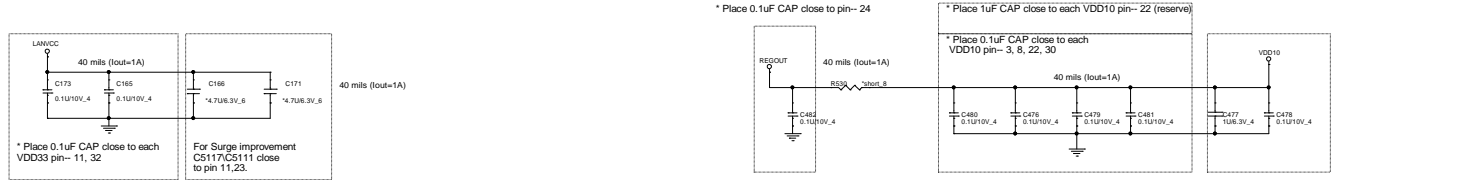
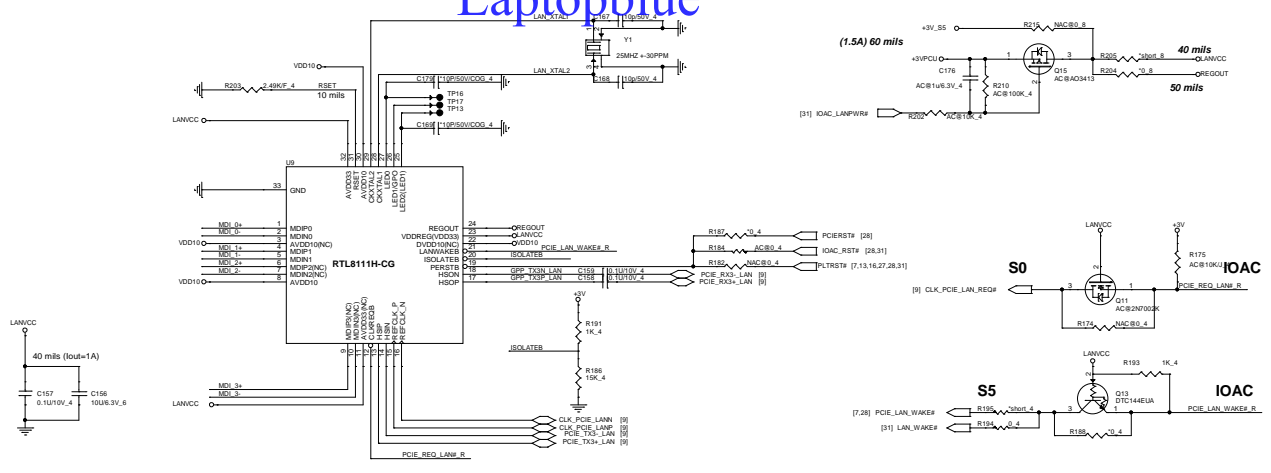
HDMI (PS8101)

Size: _____ Document Number: _____ Rev: 1A

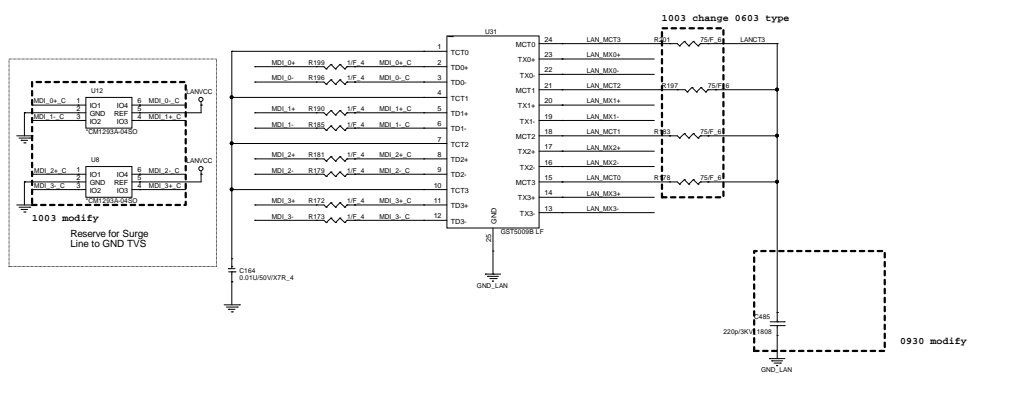
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LAN

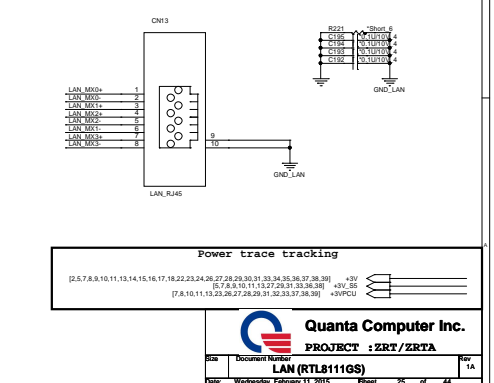
Laptopblue



Transformer

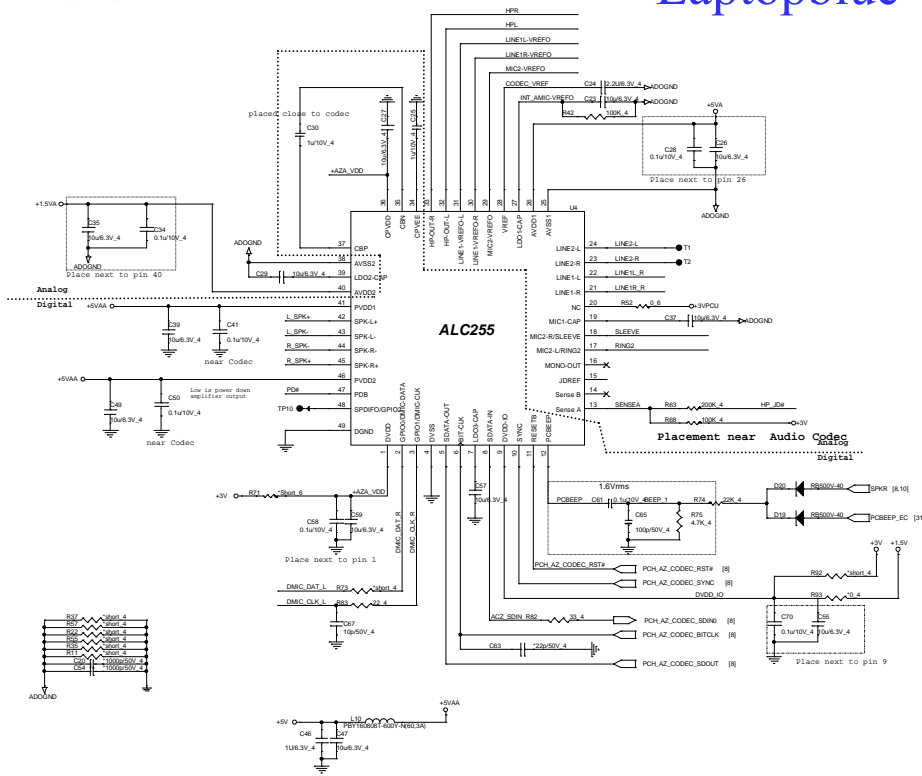


RJ45 Connector

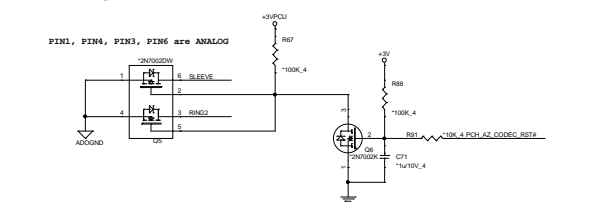


Quanta Computer Inc.
PROJECT : ZRT/ZRTA
LAN (RTL8111GS)
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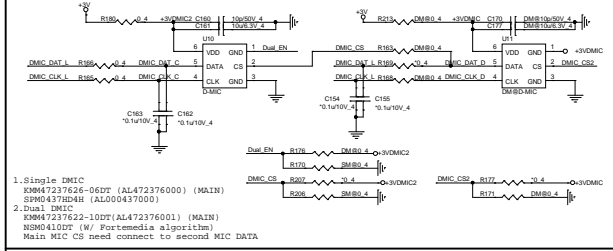
Codec(ADO)



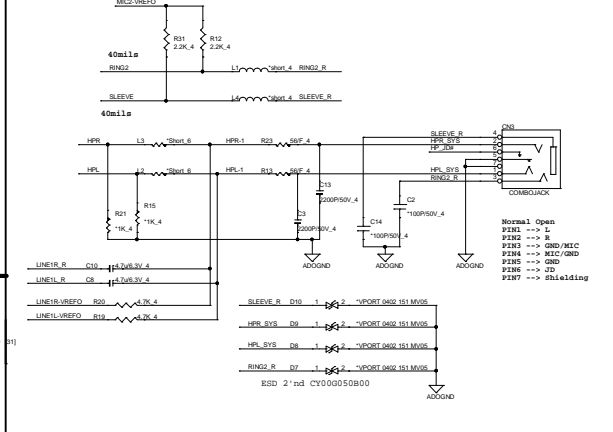
Grounding circuit(ADO)



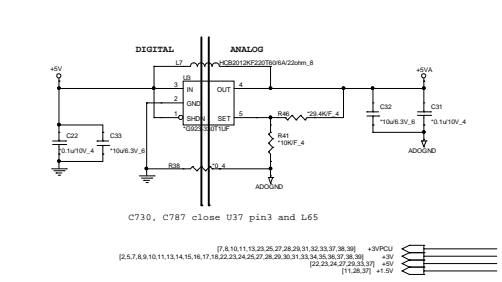
D-Mic



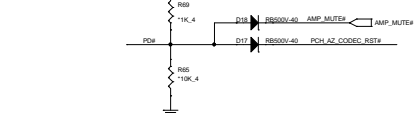
Universal Audio Jack



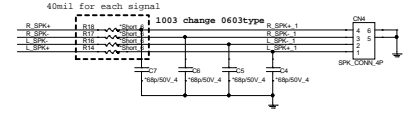
Codec PWR 5V(ADO)



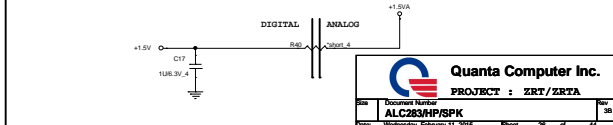
Mute(ADO)



Internal Speaker



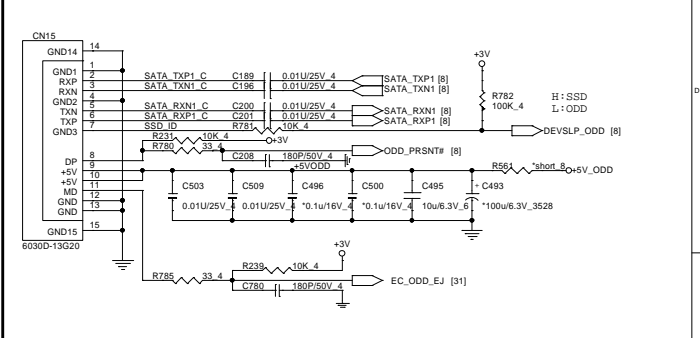
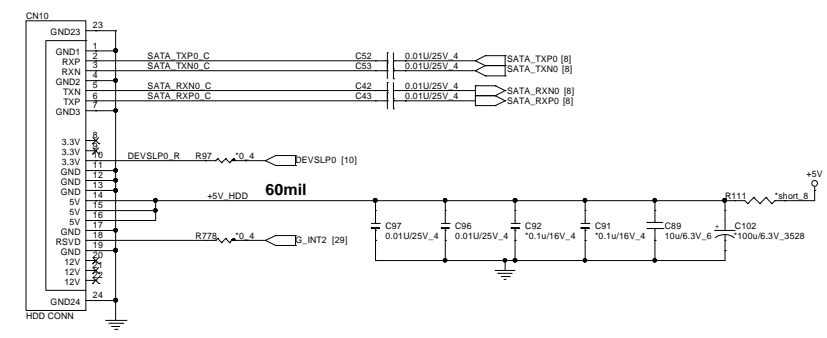
Codec PWR 3V/1.5V(ADO)



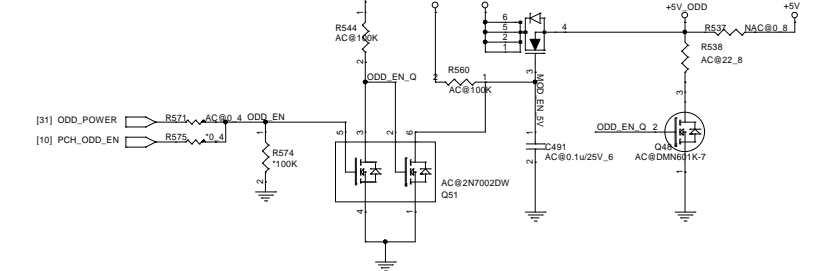
Quanta Computer Inc.
PROJECT : ZRT / ZRTA
ALC255/HP/SPK
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2.5" SATA HDD (HDD)

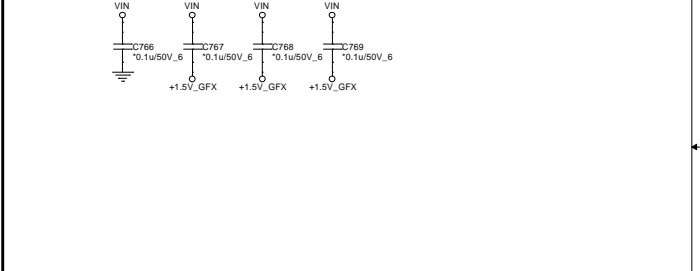
Laptop SATA ODD Connector(ODD)



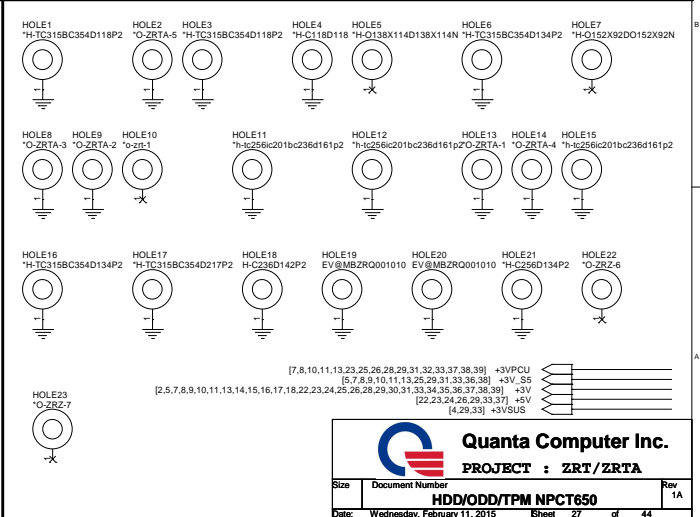
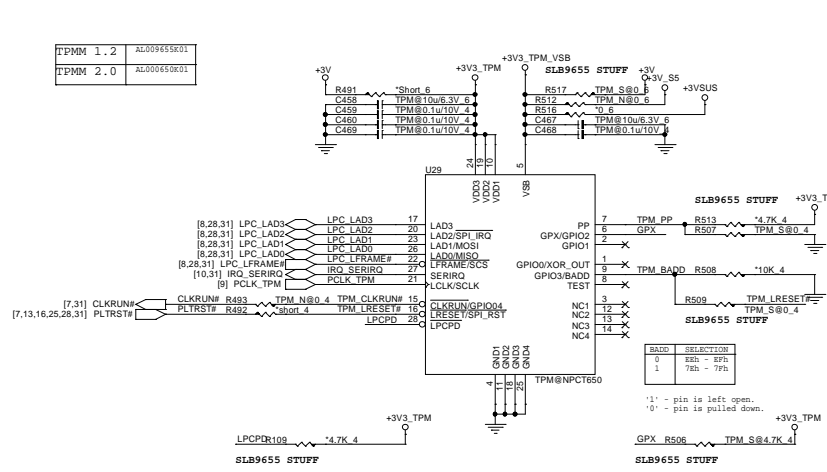
ODD Power (ODD)



EMI

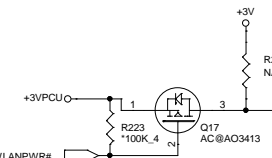
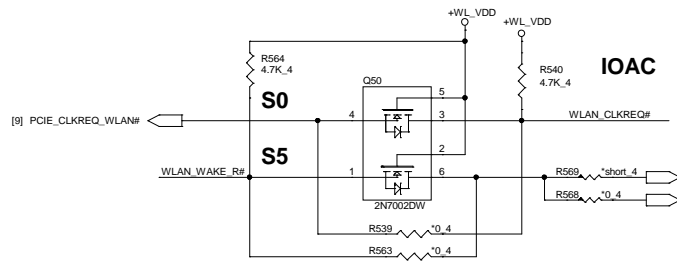
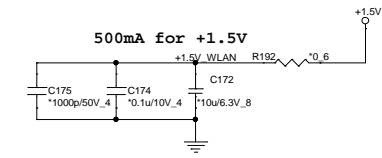
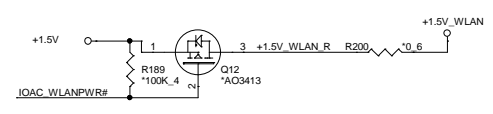
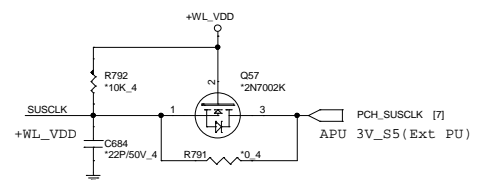
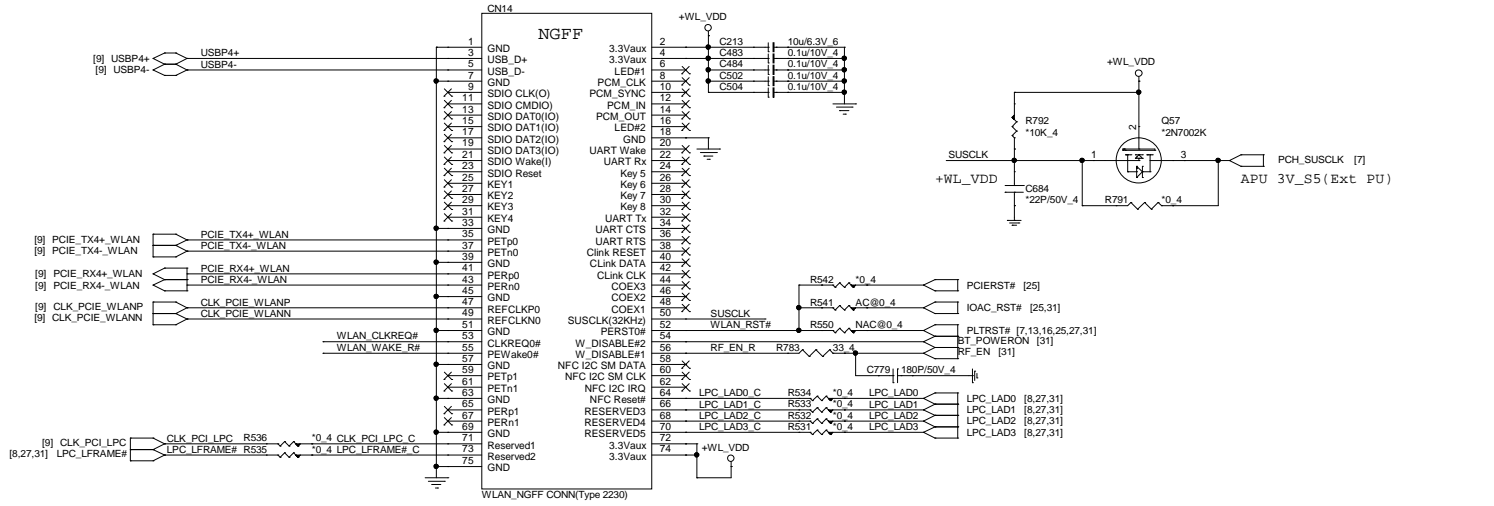


TPM NPCT650 (TPM)



Quanta Computer Inc.
PROJECT : ZRT/ZRTA

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	HDD/ODD/TPM NPCT650	1A
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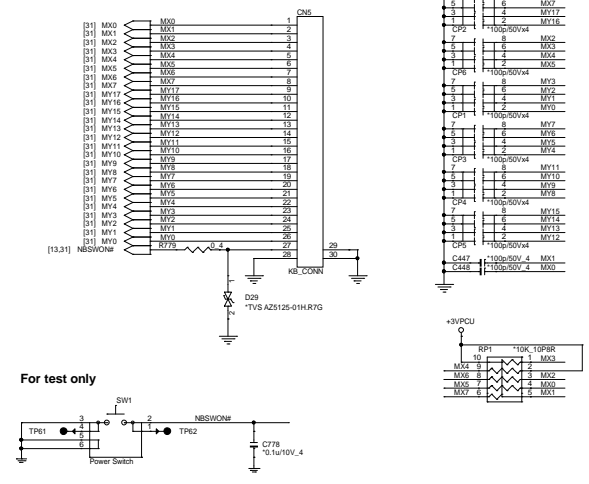


Low	Mini card +3V power enable
High	Mini card +3V power disable

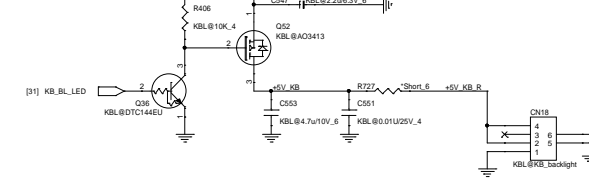
High	Mini card +3V power disable
------	-----------------------------

Quanta Computer Inc.
PROJECT : ZRT/ZRTA
Mini-Card/WL/3G/SIM
 Date: Wednesday, February 11, 2015 Sheet 28 of 44

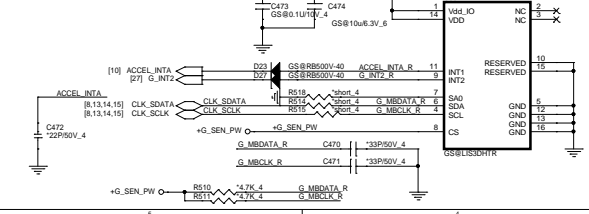
K/B (KBC)



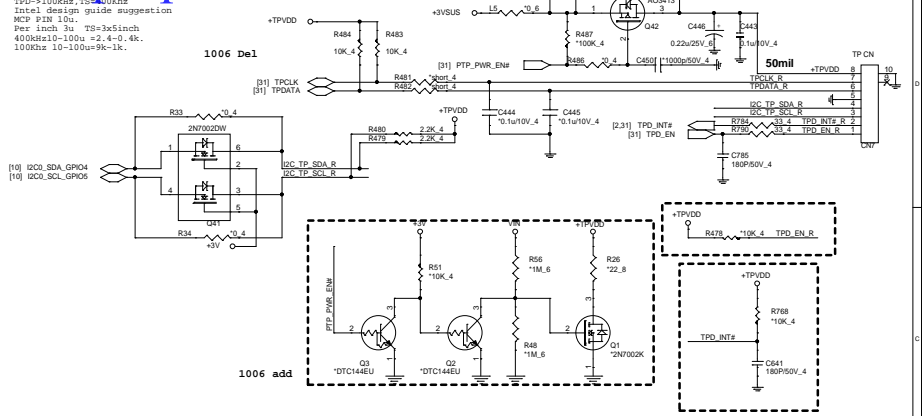
KB_BL LED (KBL)



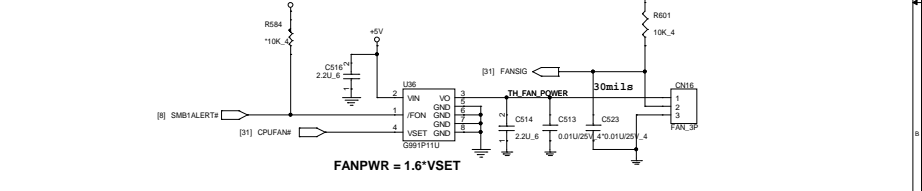
G-sensor(ACS)



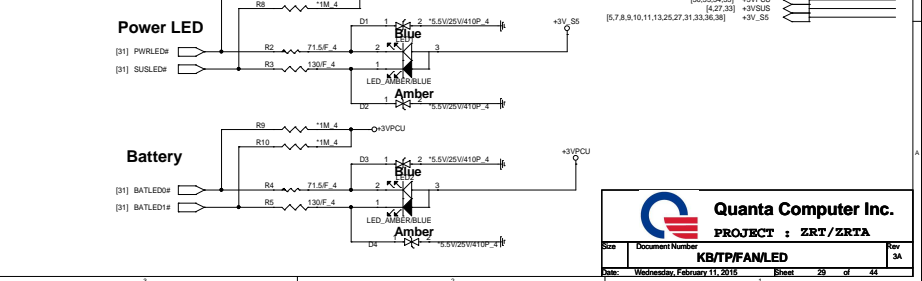
TOUCHPAD BOARD CONN (TPD I2C/PS2 co-lay)



CPU FAN (THM)



POWER LED (UIF)

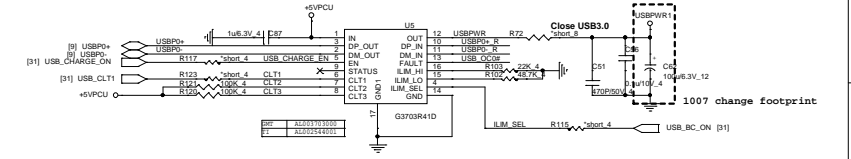
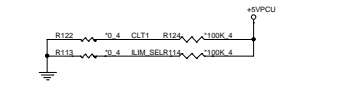
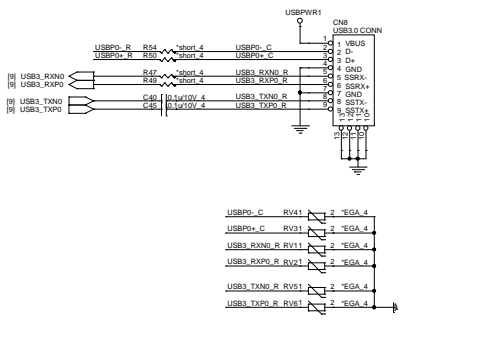


Quanta Computer Inc. PROJECT : ZRT / ZRTA		Document Number	Rev
		KB/TP/FAN/LED	3A
Date	Wednesday, February 11, 2015	Sheet	29 of 44

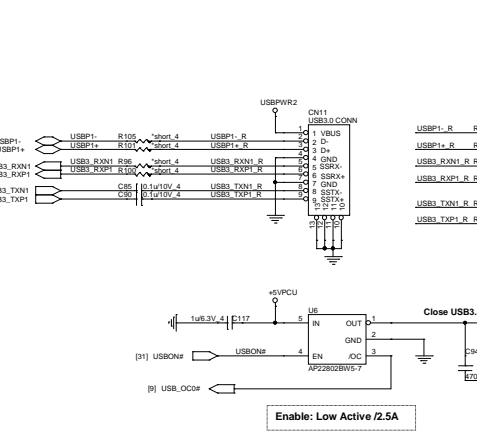
USB Charger for USB3.0 Port0 (UBC)

CTL1	CTL2	CTL3	ILIM_SEL	MODE	Current Limit Setting	Status	Output	Notice
0	0	0	0	Discharge	NA	OFF	OUT hold low	
0	0	0	1	Discharge	NA	OFF		
0	0	1	0	DCP_Auto	ILIM_HI	OFF	Data lines disconnected	
0	0	1	1	DCP_Auto	ILIM_HI	DCP	Data lines disconnected	USB Charger function active
0	1	0	0	SRP1	ILIM_LO	OFF	Data lines cop-iced	
0	1	0	1	SRP1	ILIM_HI	OFF	Data lines disconnected	
0	1	1	0	DCP_Auto	ILIM_LO	OFF	Data lines disconnected	
0	1	1	1	DCP_Auto	ILIM_HI	DCP	Data lines disconnected	Load Detect Function active
1	0	0	0	DCP_Overload	ILIM_LO	OFF	Device forced to stay in DCP BC 1.2	
1	0	0	1	DCP_Overload	ILIM_HI	OFF	Changing mode	
1	0	1	0	DCP_Overload	ILIM_LO	OFF	Device forced to stay in DCP divider1	
1	0	1	1	DCP_Overload	ILIM_HI	OFF	Changing mode	
1	1	0	0	SRP1	ILIM_LO	OFF	Data lines connected	
1	1	0	1	SRP1	ILIM_HI	OFF	Data lines connected	
1	1	1	0	SRP2	ILIM_LO	OFF	Data lines connected	
1	1	1	1	SRP2	ILIM_HI	DCP	Data lines disconnected	Load Detect Function active

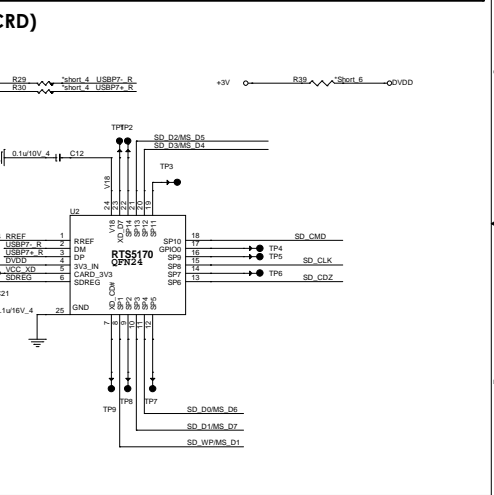
USB 3.0 Connector(UB3)



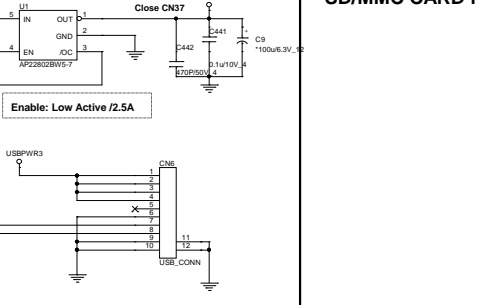
USB 3.0 Connector(UB3)



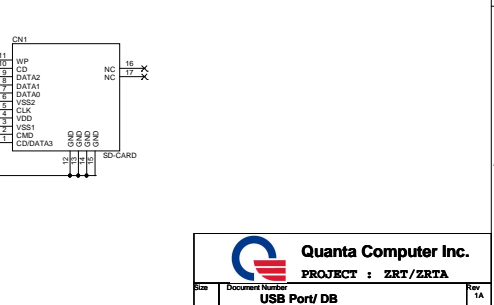
Card Reader (CRD)



USB IO D/B (UB2)



SD/MMC CARD READER (CRD)



Quanta Computer Inc.

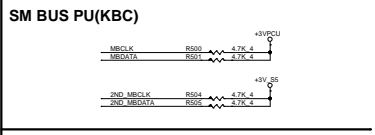
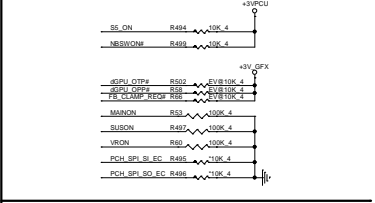
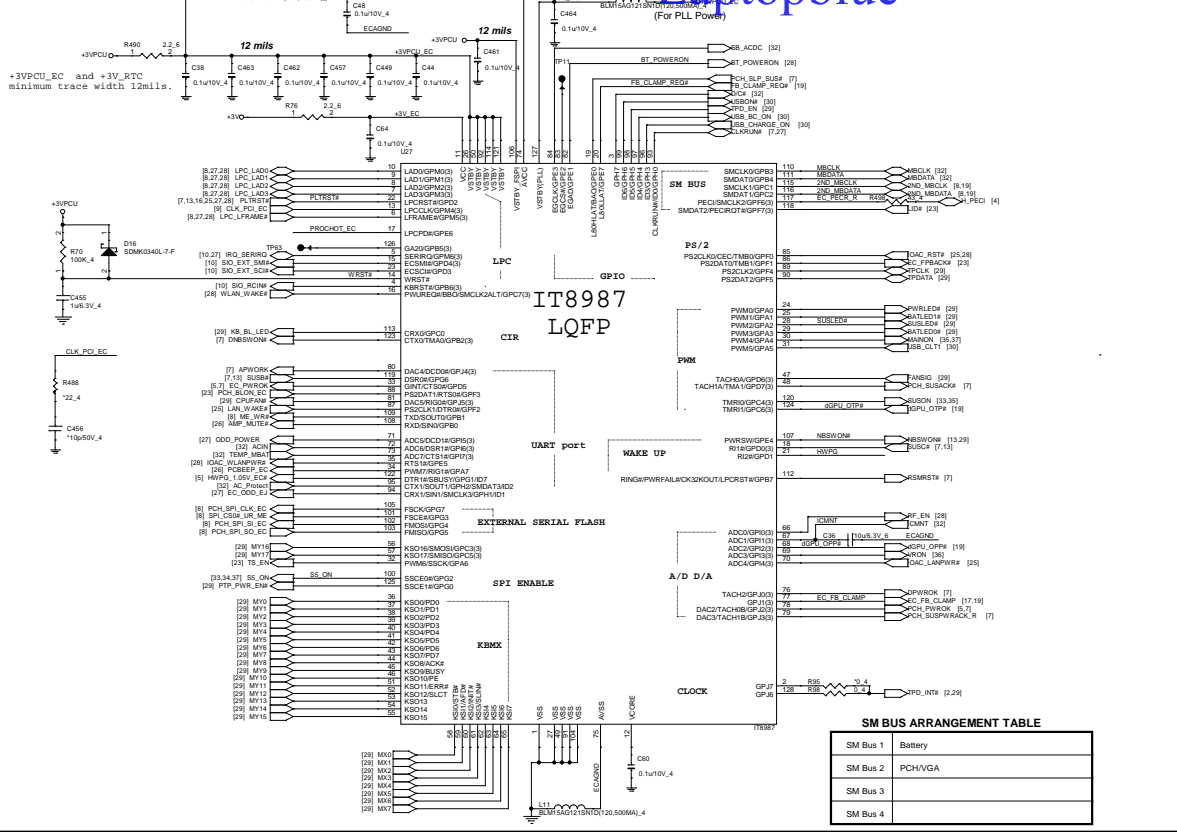
PROJECT : ZRT/ZRTA

Doc. No. **USB Port/DB**

Date: **Wednesday, February 11, 2015**

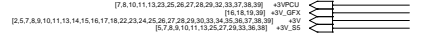
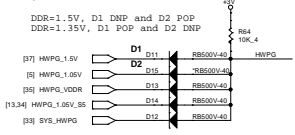
Rev. **1A**

EC(KBC)

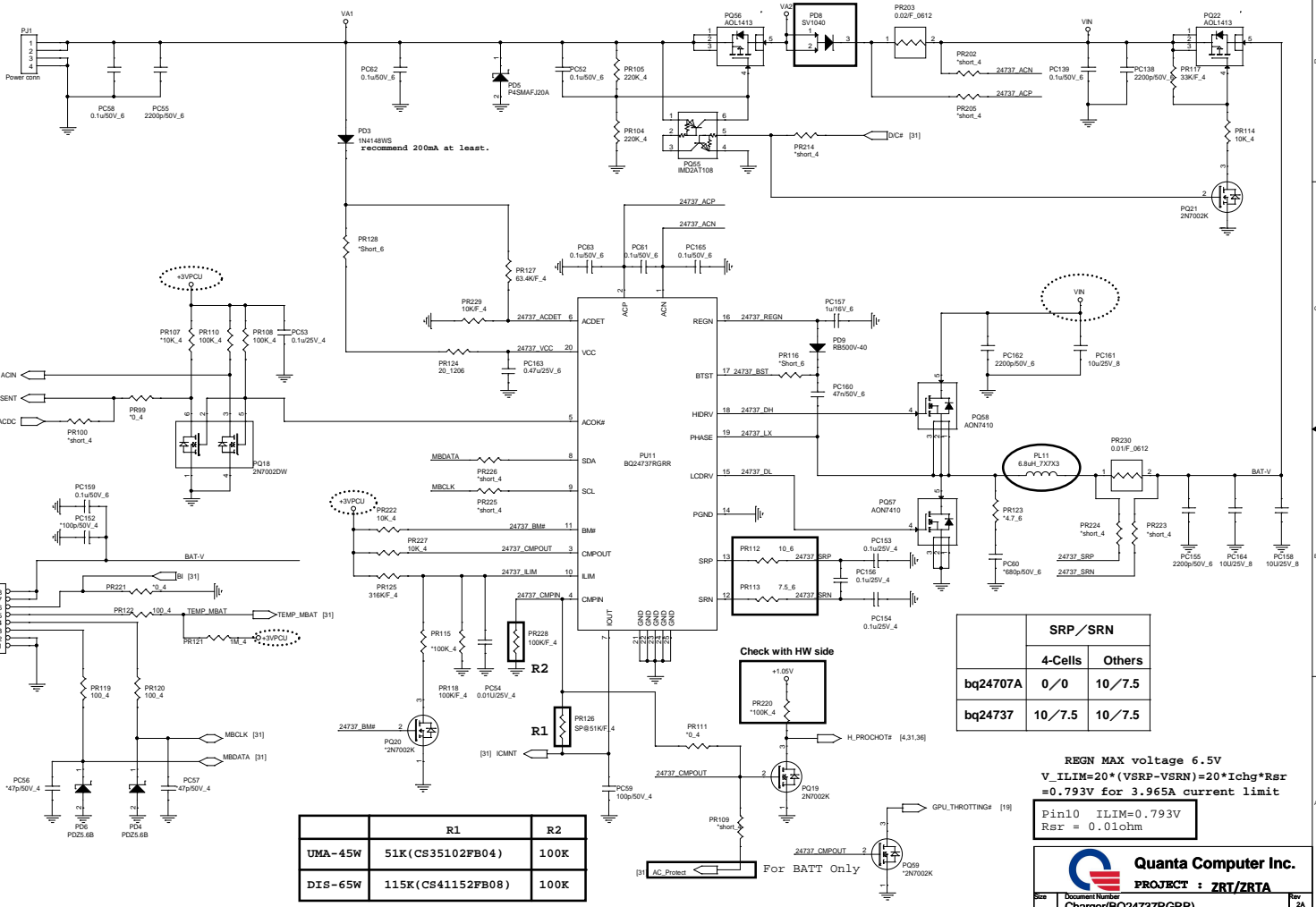


SM Bus	Component
SM Bus 1	Battery
SM Bus 2	PCH/VGA
SM Bus 3	
SM Bus 4	

HWPG(KBC)



Quanta Computer Inc.
PROJECT : ZRT/ZRTA
KBC IT8587
Date: Wednesday, February 11, 2015 Page: 31 of 44



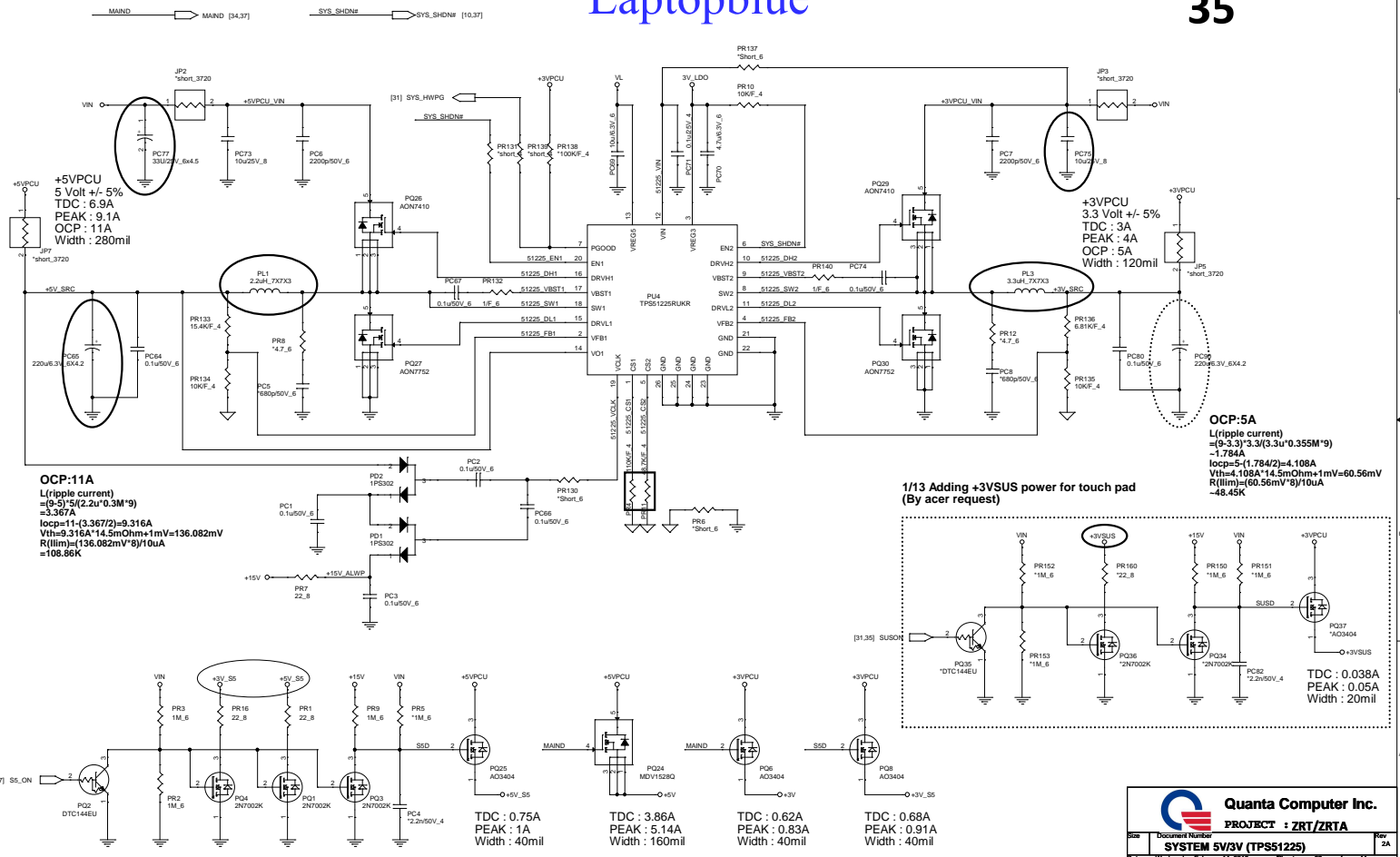
	R1	R2
UMA-45W	51K (CS35102FB04)	100K
DIS-65W	115K (CS41152FB08)	100K

	SRP / SRN	
	4-Cells	Others
bq24707A	0 / 0	10 / 7.5
bq24737	10 / 7.5	10 / 7.5

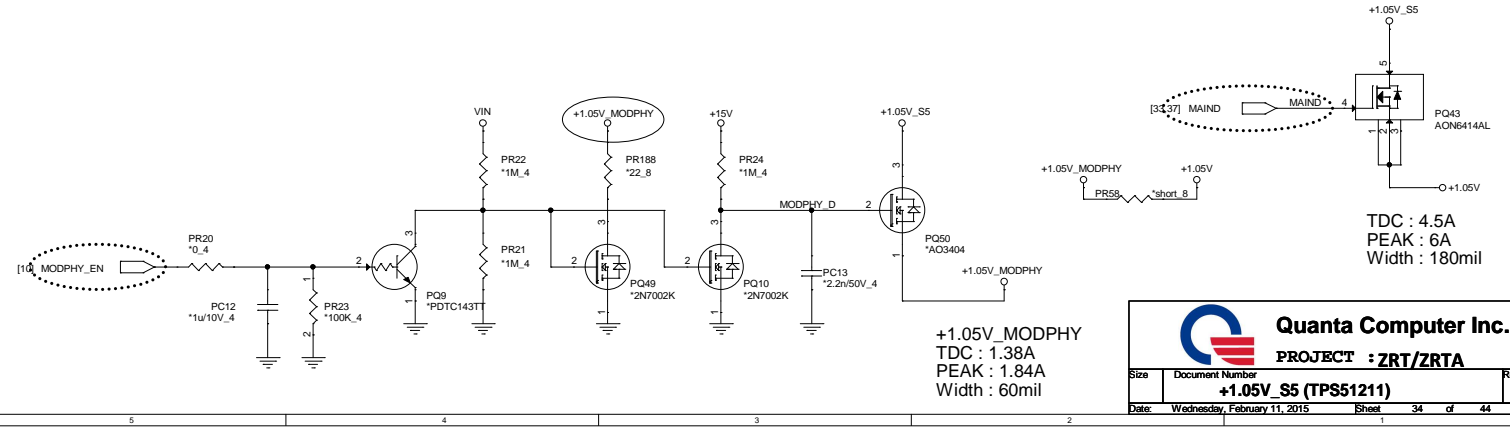
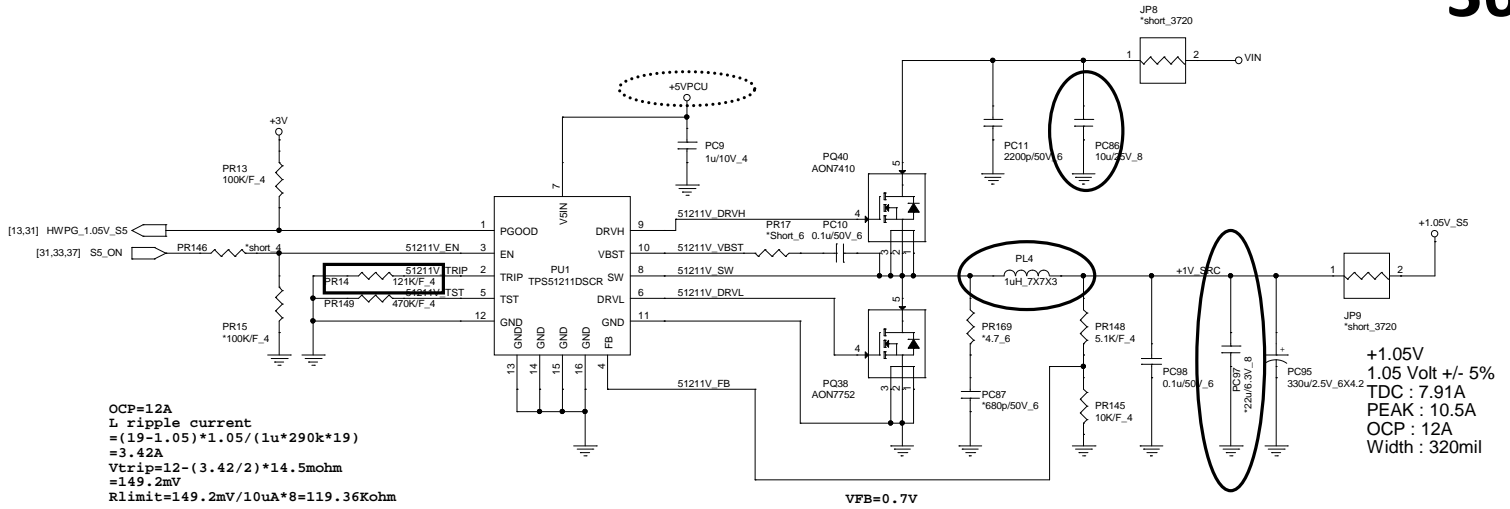
REGN MAX voltage 6.5V
 $V_{ILIM} = 20 * (V_{SRP} - V_{SRN}) = 20 * I_{chg} * R_{sr}$
 $= 0.793V$ for 3.965A current limit
 Pin10 ILIM = 0.793V
 $R_{sr} = 0.01ohm$

Quanta Computer Inc.
PROJECT : ZRT/ZRTA

Doc: _____
 Document Number: **Charger(BQ24737RGRR)**
 Date: **Wednesday, February 11, 2015** Sheet **32** of **41**



Quanta Computer Inc.
PROJECT : ZRT/ZRTA
SYSTEM 5V/3V (TPSS1225)
Date: Wednesday, February 11, 2010 10:21 AM
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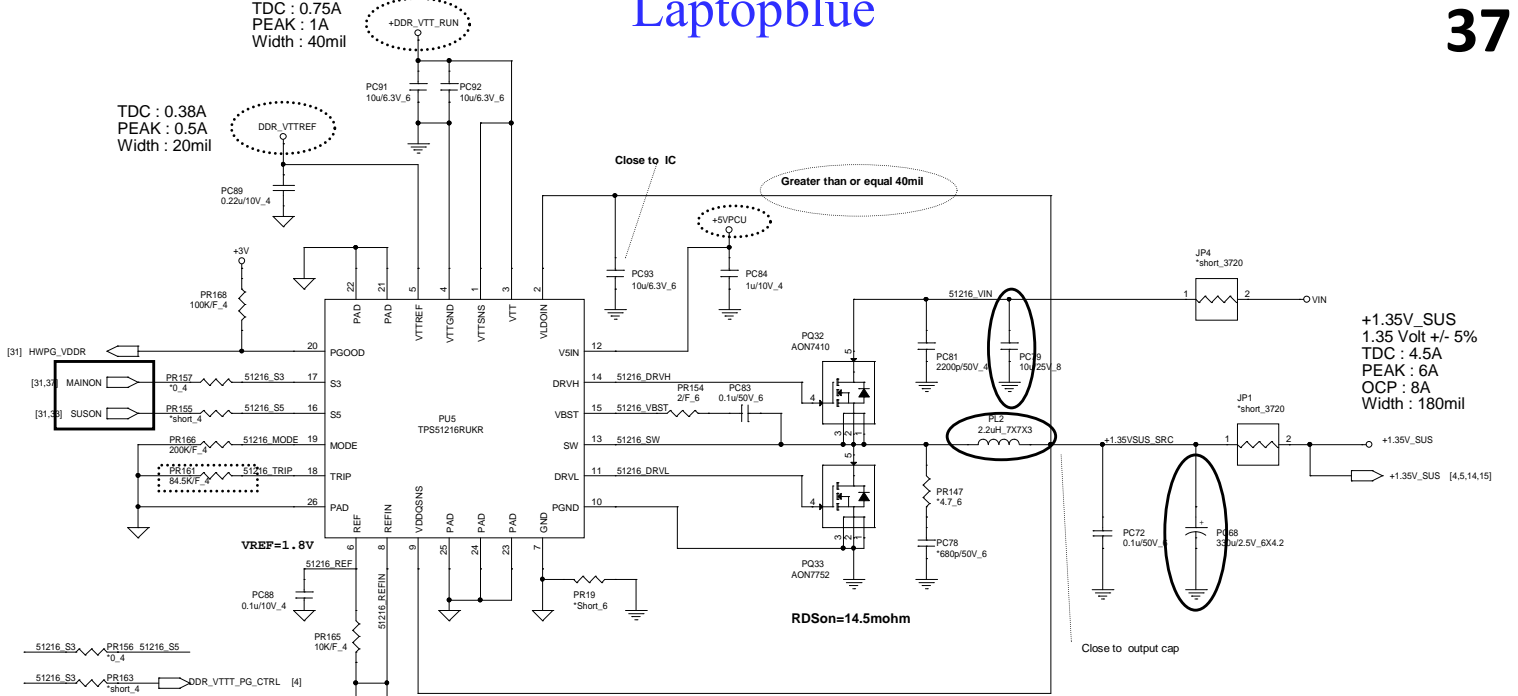
Quanta Computer Inc.

PROJECT : ZRT/ZRTA

Size	Document Number	Rev
	+1.05V_S5 (TPS51211)	2A
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TDC : 0.75A
PEAK : 1A
Width : 40mil

TDC : 0.38A
PEAK : 0.5A
Width : 20mil



+1.35V_SUS
1.35 Volt +/- 5%
TDC : 4.5A
PEAK : 8A
OCP : 8A
Width : 180mil

RDSON=14.5mohm

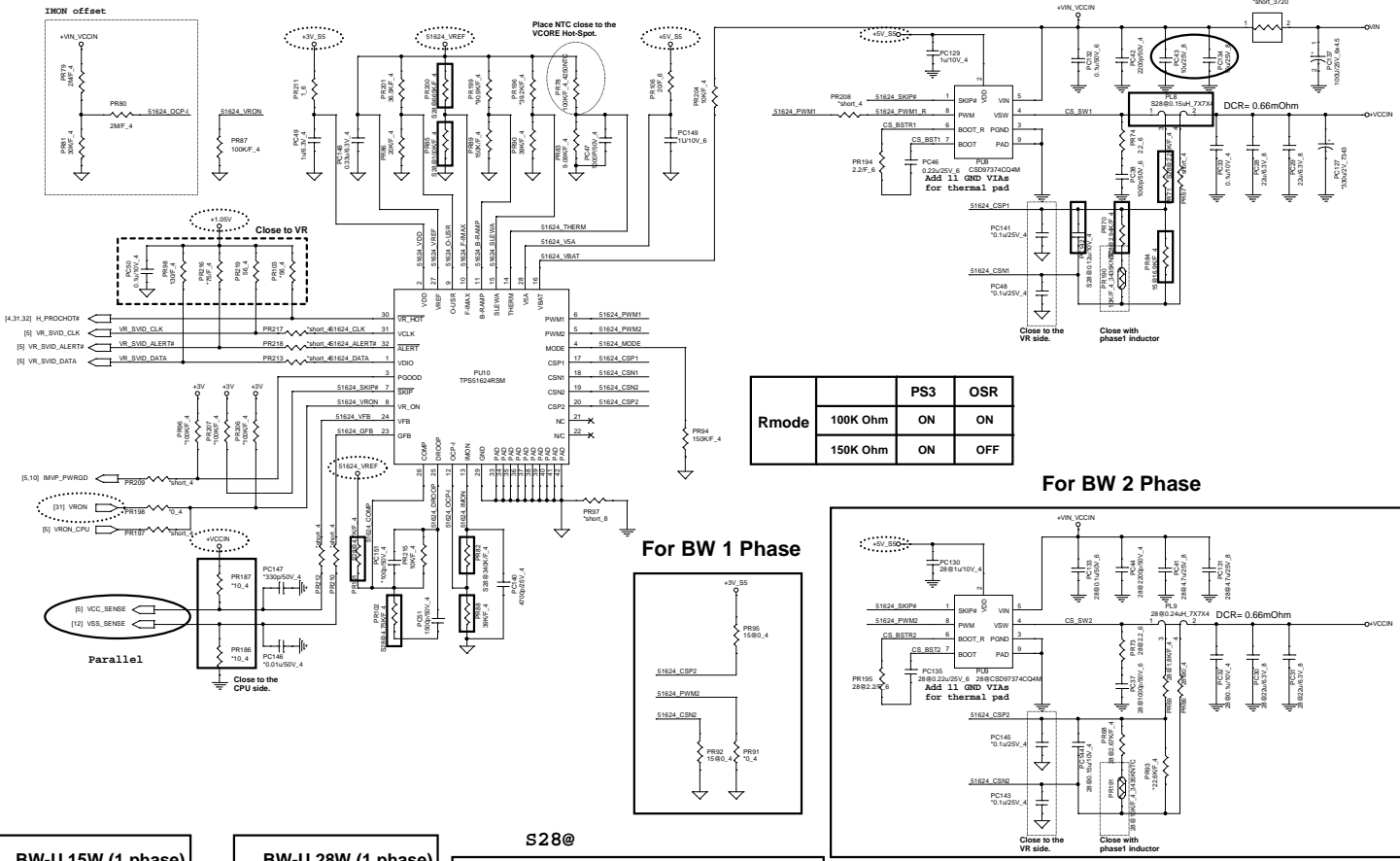
Mode	Frequency	Discharge mode
200K	400K	Tracking Discharge
100K	300K	Tracking Discharge

	S3	S5	+1.35VSUS	REF	VTT
S0	1	1	ON	ON	ON
S3 (mainon off)	0	1	ON	ON	OFF
S4/S5	0	0	OFF	OFF	OFF

OCP=8A
L ripple current
=(19-1.35)*1.35/(2.2u*400k*19)
=1.425A
Vtrip=8-(1.425/2)*14.5mohm
=105.668mV
Rlimit=105.668mV/10uA*8=84.53Kohm

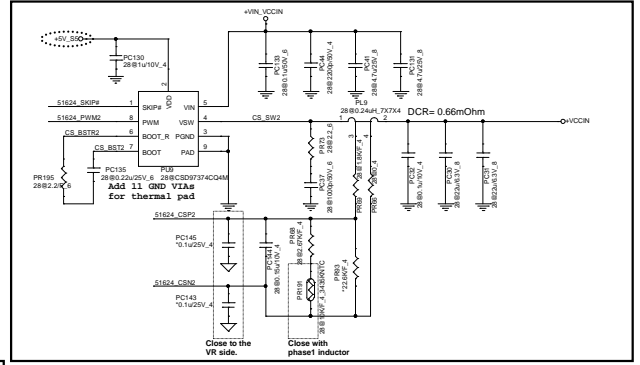
DDR=1.35V
PRB4=10K/F_4
PRB6=30.1K/F_4

Quanta Computer Inc.
PROJECT : ZRT/ZRTA
Size Document Number Raw
DDR 1.35V(TPS51216) 2A
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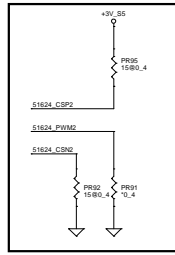


Rmode	PS3	OSR
100K Ohm	ON	ON
150K Ohm	ON	OFF

For BW 2 Phase



For BW 1 Phase



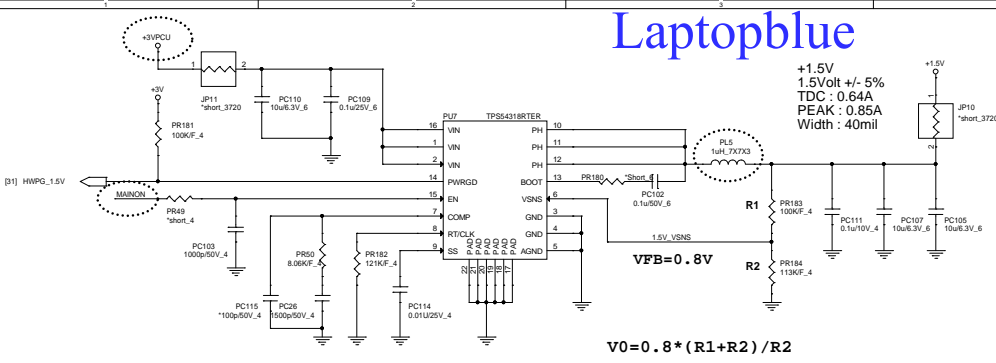
S28@

BW-U 28W 2 phase			
Location	Value	Location	Value
PL8	CV+24P0MZ00	PR85	CS35622FB10
PR71	CS21822FB14	PR101	CS22372FB11
PR82	CS41502FB18	PR102	CS31002FB26
PR70	CS22672FB12	PR200	CS42942FB13
PC142	CH4152K9B02		
Block 1.	Stuff		

PL9 0,24uH_7X7X4
 PR84 - PR93 *22.6K/F_4
 PR92 - PR95 *0_4
 PC143 - PC145 *0.1u/25V_4

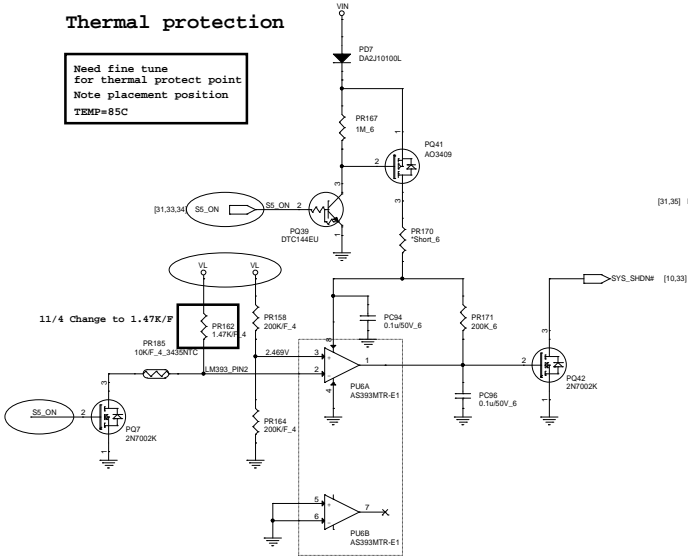
BW-U 15W (1 phase)
 Icc TDC PL2 : 14A
 Icc Max : 32A
 OCP : 37A
 Fsw : 1.2MHz
VCORE LL :
 R_DC_LL : - 2.0mV/A
 R_AC_LL : - 7.0mV/A

BW-U 28W (1 phase)
 Icc TDC PL2 : 19A
 Icc Max : 40A
 OCP : 47A
 Fsw : 800KHz
VCORE LL :
 R_DC_LL : - 2.0mV/A
 R_AC_LL : - 7.0mV/A

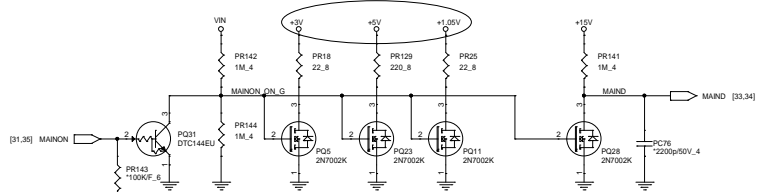


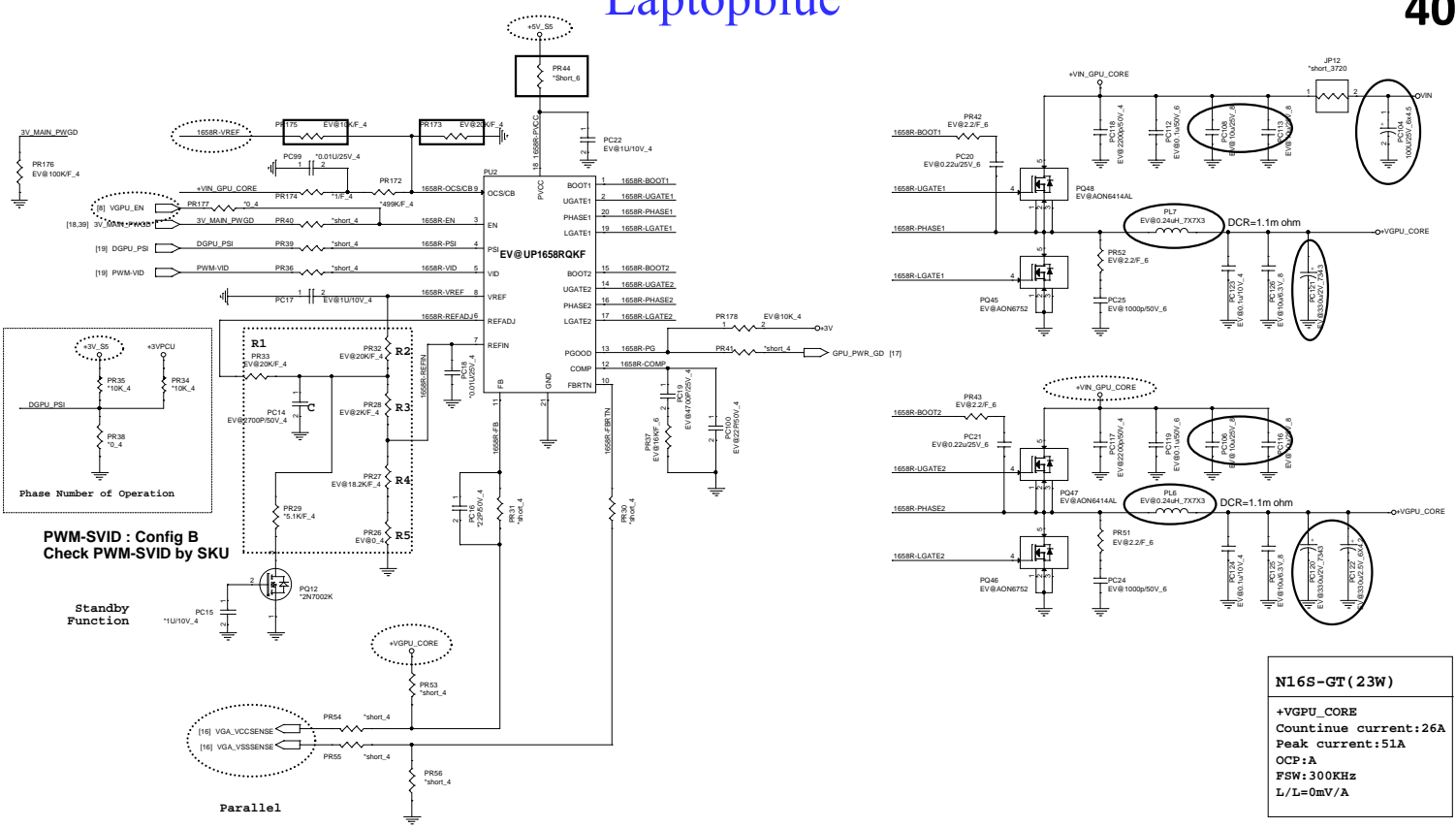
Thermal protection

Need fine tune
for thermal protect point
Note placement position
TEMP=85C



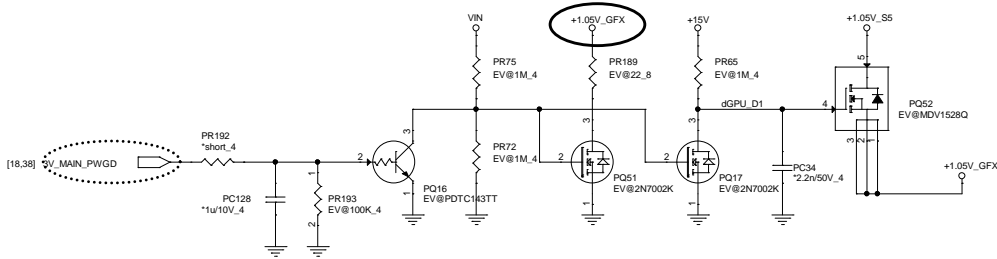
For EC control thermal protection (output 3.3V)



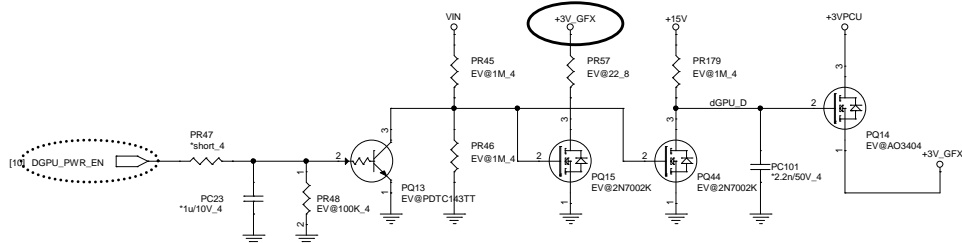


Quanta Computer Inc.
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+VGPU_CORE(UP1642PQAG)
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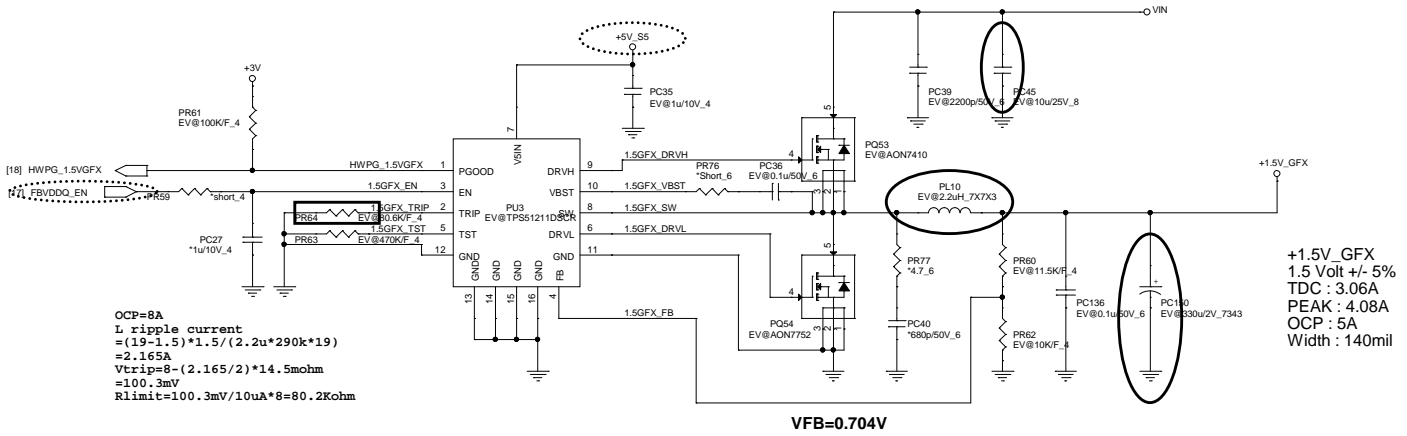
[16,17,18] +1.05V_GFX
 [17,20,21,27] +1.5V_GFX
 [16,18,19,31] +3V_GFX



+1.05V_GFX
 TDC : 1.57A
 PEAK : 2.1A
 Width : 80mil




+3V_GFX
 TDC : 0.05A
 PEAK : 0.06A
 Width : 20mil



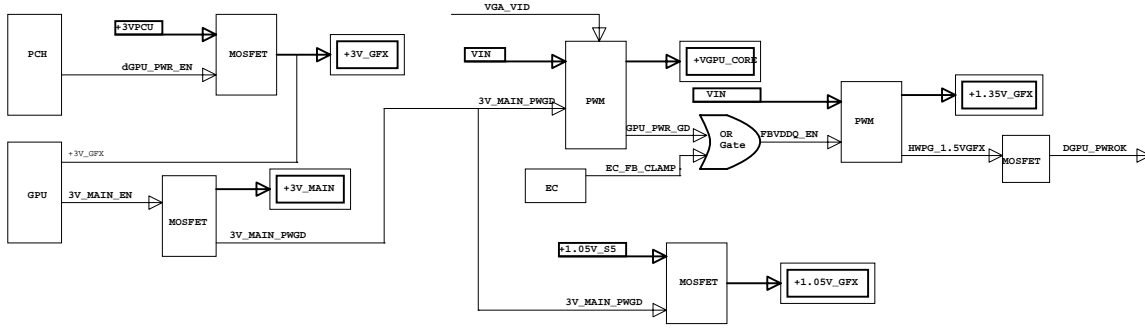
OCP=8A
 L ripple current
 $= (19-1.5) * 1.5 / (2.2u * 290k * 19)$
 $= 2.165A$
 $V_{trip} = 8 - (2.165 / 2) * 14.5mohm$
 $= 100.3mV$
 $R_{limit} = 100.3mV / 10uA * 8 = 80.2Kohm$

+1.5V_GFX
 1.5 Volt +/- 5%
 TDC : 3.06A
 PEAK : 4.08A
 OCP : 5A
 Width : 140mil

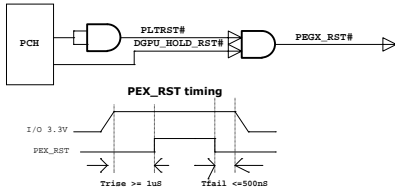
VFB=0.704V

 Quanta Computer Inc. PROJECT : ZRT/ZRTA		
Size	Document Number	Rev
	+1.5V_GFX+1.05V_GFX+3V_GFX	2A
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VGA power up sequence



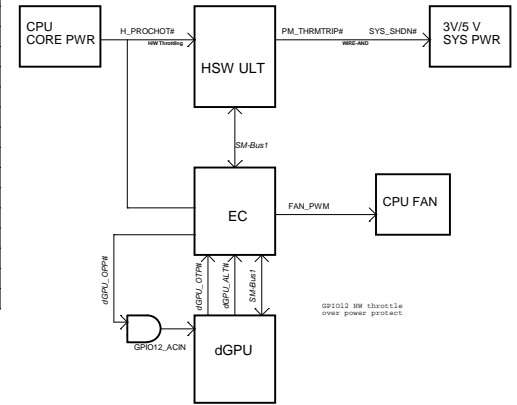
VGA Reset



Power States

POWER PLANE	VOLTAGE	DESCRIPTION	CONTROL SIGNAL	ACTIVE IN
VIN	+10V--+19V	MAIN POWER	ALWAYS	ALWAYS
+3V_RTC	+3V--+3.3V	RTC POWER	ALWAYS	ALWAYS
+3VPCU	+3.3V	EC POWER	ALWAYS	ALWAYS
+5VPCU	+5V	USB CHARGE POWER	ALWAYS	ALWAYS
+15V	+15V	CHARGE PUMP POWER	ALWAYS	ALWAYS
+3V_SS	+3.3V	LANBT POWER	SS_ON	S0-S5
+5V_SS	+5V	USB POWER	SS_ON	S0-S5
+5V	+5V	HDD/SPK/HDMI POWER	MAINON	S0
+3V	+3.3V	PCH/GPU/Peripheral component POWER	MAINON	S0
+1.35V/SUS	+1.35V	CPU/SODIMM/MD POWER	SUSON	S0-S3
+DDR_VIT_RUN	+0.675V	SODIMM/MD Termination POWER	MAINON	S0
LCDVCC	+3.3V	LCD POWER	LVDS_VDDEN	S0
+1.5V	+1.5V	MINI CARD/NEW CARD POWER	MAINON	S0
+1.05V	+1.05V	PCH CORE VCCST POWER	MAINON	S0
+VCCIN	variation	CPU CORE POWER	VRON	S0
+3V_GFX	variation	External GPU POWER	dGPU_PWR_EN	S0
+1.05V_GFX	+3.3V	External GPU POWER	3V_MAIN_EN	S0
+VGPU_CORE	+1.35V	External GPU POWER	3V_MAIN_EN	S0
+1.35V_GFX	+1.05V	External GPU POWER	FBVDDQ_EN	S0

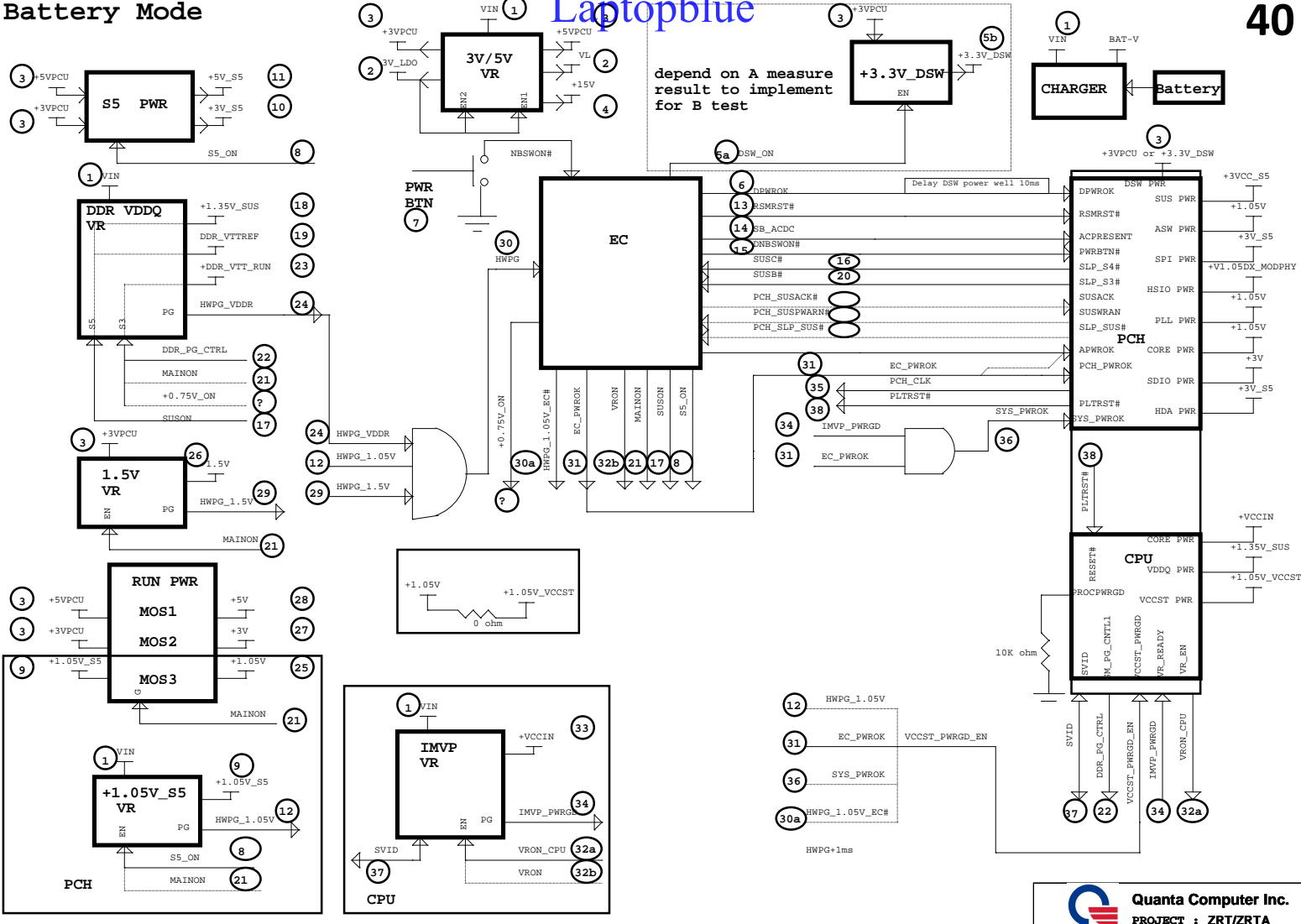
Thermal Follow Chart

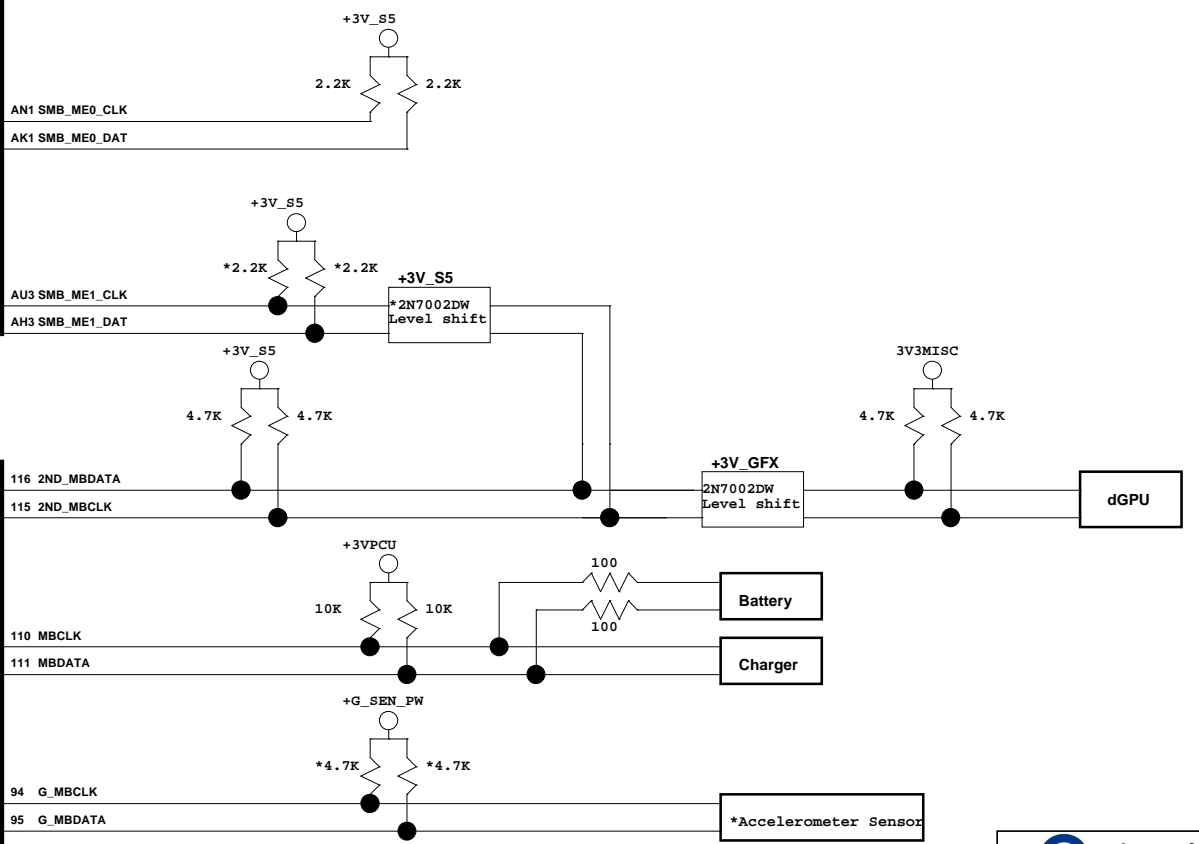
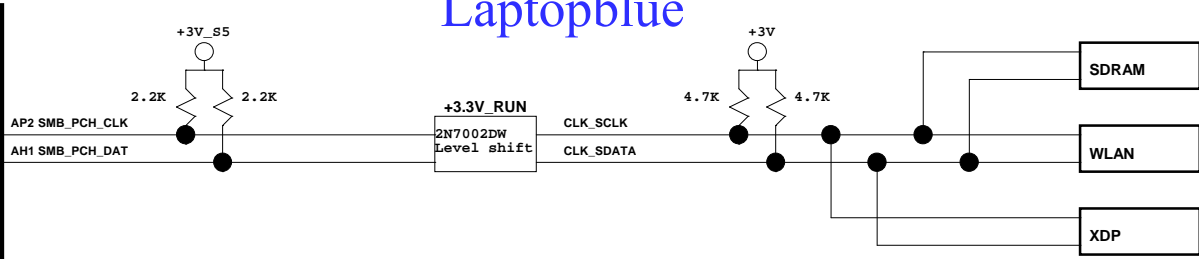
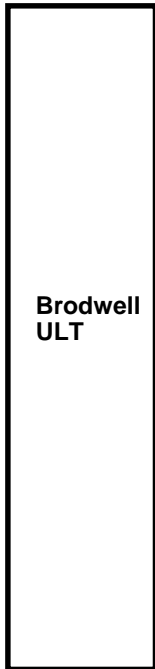


dGPU_CORE# EC notify SW throttle over power protect
 dGPU_CORE# Vth threshold -> before EC over temperature protect

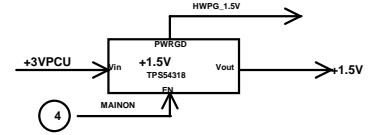
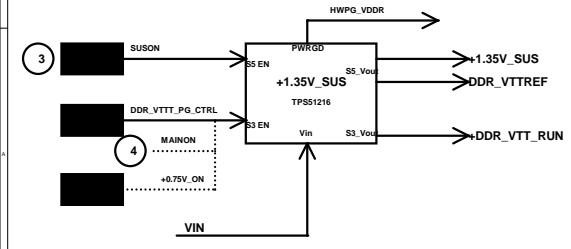
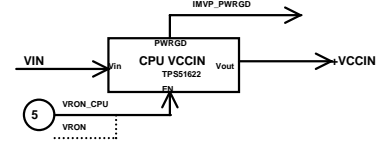
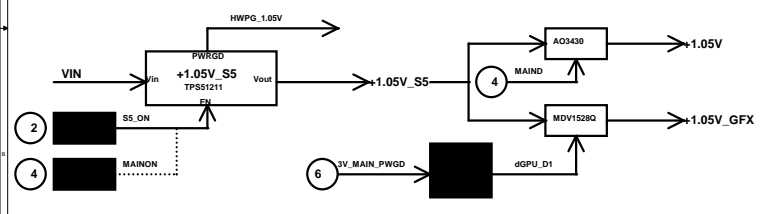
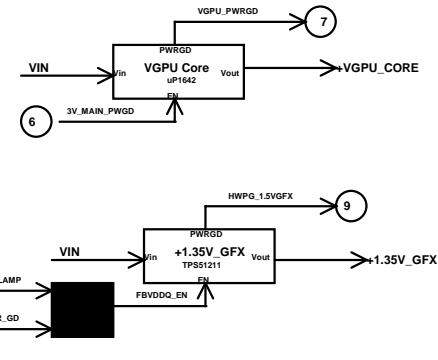
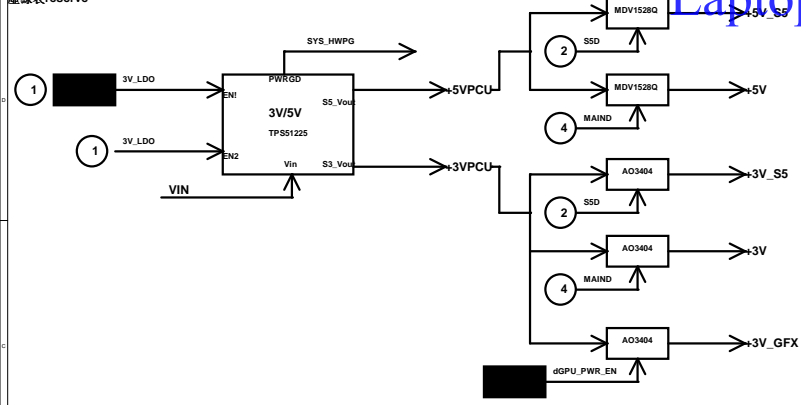
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Battery Mode





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PROJECT : ZRT/ZRTA
Block Diagram
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CHANGE LIST

Model	Version	Change List
ZQ0	1A-1	<ol style="list-style-type: none"> 1 2013/10/15 change pin define and add pwm IC.(page31) 2 2013/10/15 Change VGA ITE solution to NXP.(page 23) 3 2013/10/15 power board CN change to 6pin.(Page 23) 4 2013/10/15 U5017.12 change 27M crystal to VGA IC.(Page 23) 5 2013/10/15 U5017.14 add power rail +3V_RTC.(page23) 6 2013/10/15 strap0 R672 DG 50k PU.(Page 19) 7 2013/10/15 Change AND gat to Q63 D-MOS.(Page 19) 8 2013/10/15 change pin define and add pwm IC U17.(Page 46) 9 2013/10/15 for GC6 stuff R228(R1013;R226)R1012.un-stuff Q24(Q26;R227)R1011. (Page19) 10 20131015 For GC6 NV DG GC6_FB_EN PD.(Page10) 11 2013/10/15 following up acer define and swap USB3 and USB2 port.(Page9) 12 2013/10/15 swap CAP C8579/C8580 to Vrefo and resistor R5214/R5215 to Line in.(Page30) 13 2013/10/15 U27.30/U27.31 del fan Pwm signal.(Page32) 14 20131015 change LVDS(USB3;RJ45;FAN;TPD;USB DB CN;DC-IN CN;Power Button;Cardreader;KB BLK CN;Power board, footprint.
	1A-2	<ol style="list-style-type: none"> 1 2013/10/16 JDIM5 Swap M_B_DQS2/M_B_DQS3 and swap M_B_DQS#2/M_B_DQS#3.(page15) 2 2013/10/16 JDIM6 Chage net name M_B_DQS#[7:0] to M_A_DQS#[7:0].(page14) 3 2013/10/16 Add RTC charge circuit.(page8) 4 2013/10/16 BT1.1 Chage +3V_RTC_0 to VCCTC_2.(page8) 5 2013/10/15 change power rail from +3V_RTC_0 to VCCTC_2.(page23)