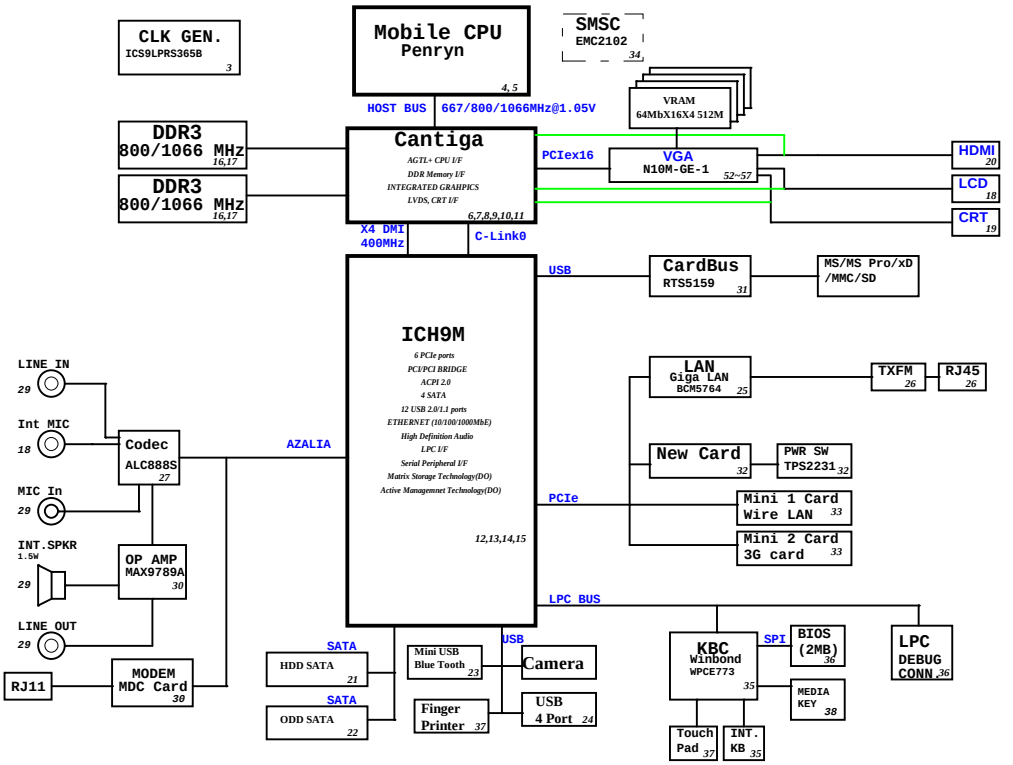
JV50 Block Diagram

Project code: 91.4CG01.001
PCB P/N : 48.4CG01.0SA
REVISION : 08245-SA



PCB STACKUP

TOP		L1
GND		L2
S		L3
S		L4
GND		L5
BOTTOM		L6

SYSTEM DC/DC ISL62392 42	
INPUTS	OUTPUTS
DCBATOUT	5V_S5(6A) 3D3V_S5(7A) 5V_AUX_S5 3D3V_AUX_S5

SYSTEM DC/DC TPS51124 43	
INPUTS	OUTPUTS
DCBATOUT	1D05V_S0(9A) 1D5V_S3(12A)

RT9026 44	
1D5V_S3	DDR_VREF_S3 (1.2A)

RT9018 44	
1D5V_S3	1D1V_S0(2A)

TPS51117 45	
DCBATOUT	FBVDD(4A)

CHARGER ISL88731A 47	
INPUTS	OUTPUTS
DCBATOUT	BT+

CPU DC/DC ISL6266A 41	
INPUTS	OUTPUTS
DCBATOUT	VCC_CORE 38A

VGA_CORE RT8202A 47	
INPUTS	OUTPUTS
DCBATOUT	VGA_CORE 13A

GFXCORE ISL6263A 46	
INPUTS	OUTPUTS
DCBATOUT	VCC_GFXCORE (7A)

JV50

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Title: BLOCK DIAGRAM

Size	Document Number	Rev
A2	JV50	SB

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ICH9M Functional Strap Definitions

Signal	Usage/When Sampled	Comment
HDA_SDOUT	XOR Chain Entrance/ PCIE Port Config1 bit1, Rising Edge of PWROK	Allows entrance to XOR Chain testing when TP3 pulled low.When TP3 not pulled low at rising edge of PWROK,sets bit1 of RPC.PC(Config Registers: offset 224h). This signal has weak internal pull-down
HDA_SYNC	PCIE config1 bit0, Rising Edge of PWROK.	This signal has a weak internal pull-down. Sets bit0 of RPC.PC(Config Registers:Offset 224h)
GNT2#/ GPIO53	PCIE config2 bit2, Rising Edge of PWROK.	This signal has a weak internal pull-up. Sets bit2 of RPC.PC2(Config Registers:Offset 0224h)
GPIO20	Reserved	This signal should not be pulled high.
GNT1#/ GPIO51	ESI Strap (Server Only) Rising Edge of PWROK	ESI compatible mode is for server platforms only. This signal should not be pulled low for desttop and mobile.
GNT3#/ GPIO55	Top-Block Swap Override. Rising Edge of PWROK.	Sampled low:Top-Block Swap mode(inverts A16 for all cycles targeting FWH BIOS space). Note: Software will not be able to clear the Top-Swap bit until the system is rebooted without GNT3# being pulled down.
GNT0#: SPI_CS1#/ GPIO58	Boot BIOS Destination Selection 0:1. Rising Edge of PWROK.	Controllable via Boot BIOS Destination bit (Config Registers:Offset 3410h:bit 11:10). GNT0# is MSB, 01-SPI, 10-PCI, 11-LPC.
SPI_MOSI	Integrated TPM Enable, Rising Edge of CLPWROK	Sample low: the Integrated TPM will be disabled. Sample high: the MCH TPM enable strap is sampled low and the TPM Disable bit is clear, the Integrated TPM will be enable.
GPIO49	DMI Termination Voltage, Rising Edge of PWROK.	The signal is required to be low for desktop applications and required to be high for mobile applications.
SATALED#	PCI Express Lane Reversal. Rising Edge of PWROK.	Signal has weak internal pull-up. Sets bit 27 of MPC.LR(Device 28:Function 0:Offset D8)
SPKR	No Reboot. Rising Edge of PWROK.	If sampled high, the system is strapped to the "No Reboot" mode(ICH9 will disable the TCO Timer system reboot feature). The status is readable via the NO REBOOT bit.
TP3	XOR Chain Entrance. Rising Edge of PWROK.	This signal should not be pull low unless using XOR Chain testing.
GPIO33/ HDA_DOCK _EN#	Flash Descriptor Security Override Strap Rising Edge of PWROK	Sampled low:the Flash Descriptor Security will be overridden. If high,the security measures will be in effect.This should only be enabled in manufacturing environments using an external pull-up resister.

ICH9M Integrated Pull-up and Pull-down Resistors

SIGNAL	Resistor Type/Value
CL_CLK[1:0]	PULL-UP 20K
CL_DATA[1:0]	PULL-UP 20K
CL_RST0#	PULL-UP 20K
DPRSLPVR/GPIO16	PULL-DOWN 20K
ENERGY_DETECT	PULL-UP 20K
HDA_BIT_CLK	PULL-DOWN 20K
HDA_DOCK_EN#/GPIO33	PULL-UP 20K
HDA_RST#	PULL-DOWN 20K
HDA_SDIN[3:0]	PULL-DOWN 20K
HDA_SDOUT	PULL-DOWN 20K
HDA_SYNC	PULL-DOWN 20K
GLAN_DOCK#	The pull-up or pull-down active when configured for native GLAN_DOCK# functionality and determined by LAN controller
GNT[3:0]#/GPIO[55,53,51]	PULL-UP 20K
GPIO[20]	PULL-DOWN 20K
GPIO[49]	PULL-UP 20K
LDA[3:0]#/FHW[3:0]#	PULL-UP 20K
LAN_RXD[2:0]	PULL-UP 20K
LDRQ[0]	PULL-UP 20K
LDRQ[1]/GPIO23	PULL-UP 20K
PME#	PULL-UP 20K
PWRBTN#	PULL-UP 20K
SATALED#	PULL-UP 15K
SPI_CS1#/GPIO58/CLGPIO6	PULL-UP 20K
SPI_MOSI	PULL-DOWN 20K
SPI_MISO	PULL-UP 20K
SPKR	PULL-DOWN 20K
TACH_[3:0]	PULL-UP 20K
TP[3]	PULL-UP 20K
USB[11:0][P,N]	PULL-DOWN 15K

Cantiga chipset and ICH9M I/O controller Hub strapping configuration

Pin Name	Strap Description	Configuration
CFG[2:0]	FSB Frequency Select	000 = FSB1067 011 = FSB667 010 = FSB800 others = Reserved
CFG[4:3] CFG8 CFG[15:14] CFG[18:17]	Reserved	
CFG5	DMI x2 Select	0 = DMI x2 1 = DMI x4 (Default)
CFG6	iTPM Host Interface	0= The iTPM Host Interface is enabled(Note2) **1=The iTPM Host Interface is disalbed(default)**
CFG7	Intel Management engine Crypto strap	0 = Transport Layer Security (TLS) cipher suite with no confidentiality **1 = TLS cipher suite with confidentiality (default)**
CFG9	PCIE Graphics Lane	0 = Reverse Lanes,15->0,14->1 ect.. **1= Normal operation(Default):Lane Numbered in order**
CFG10	PCIE Loopback enable	0 = Enable (Note 3) **1= Disabled (default)**
CFG[13:12]	XOR/ALL	00 = Reserve 10 = XOR mode Enabled 01 = ALLZ mode Enabled (Note 3) **11 = Disabled (default)**
CFG16	FSB Dynamic ODT	0 = Dynamic ODT Disabled **1 = Dynamic ODT Enabled (Default)**
CFG19	DMI Lane Reversal	**0 = Normal operation(Default): Lane Numbered in Order** 1 = Reverse Lanes DMI x4 mode[MCH -> ICH]:(3->0,2->1,1->2and0->3) DMI x2 mode[MCH -> ICH]:(3->0,2->1)
CFG20	Digital Display Port (SDVO/DP/iHDMI) Concurrent with PCIe	**0 = Only Digital Display Port or PCIE is operational (Default)** 1 =Digital display Port and PCIe afe operting simulataneously via the PEG port
SDVO_CTRLDATA	SDVO Present	**0 =No SDVO Card Present (Default)** 1 = SDVO Card Present
L_DDC_DATA	Local Flat Panel (LFP) Present	**0 = LFP Disabled (Default)** 1= LFP Card Present; PCIE disabled

NOTE:
1. All strap signals are sampled with respect to the leading edge of the (G)MCH Power OK (PWROK) signal.
2. iTPM can be disabled by a 'Soft-Strap' option in the Flash-decriptor section of the Firmware. This 'Soft-Strap' is activated only after enabling iTPM via CFG6. Only one of the CFG10/CFG/12/CFG13 straps can be enabled at any time.

JV50

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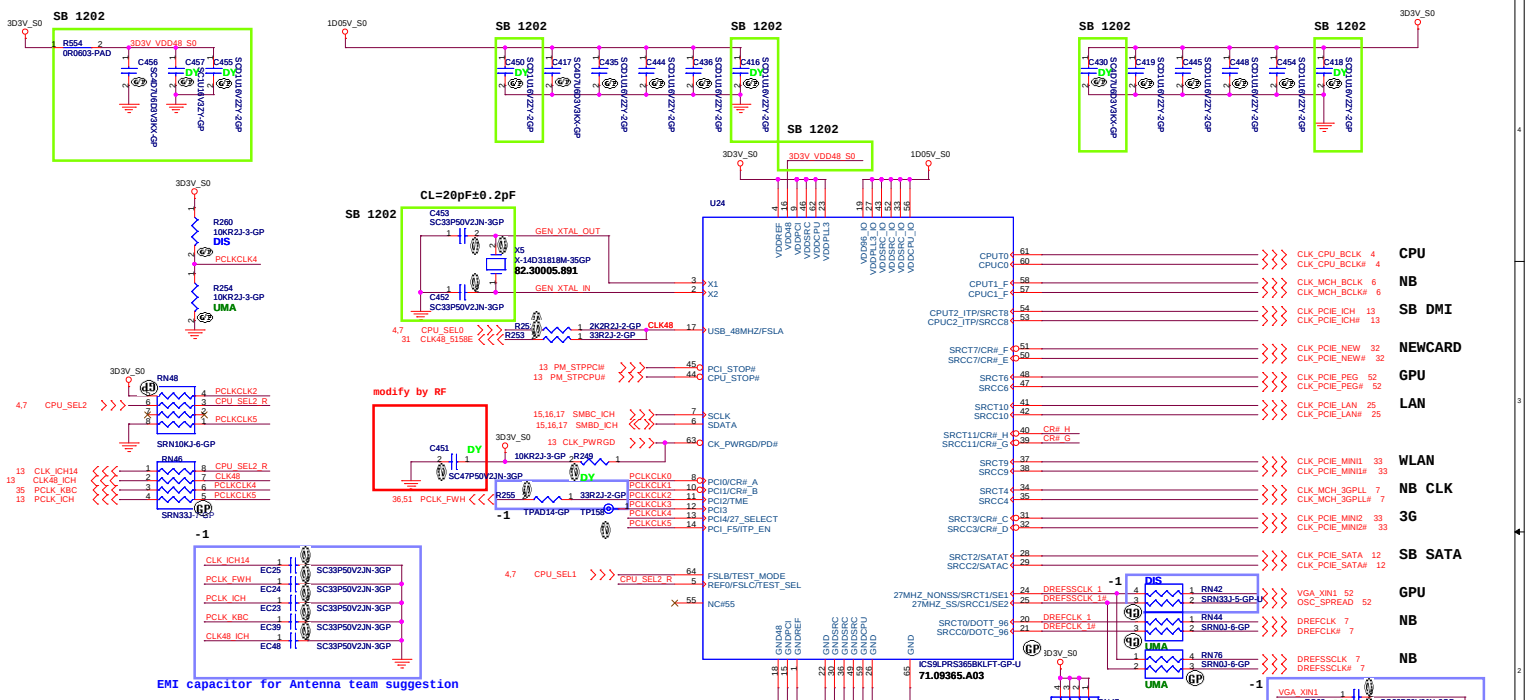
Title: Reference

Size	Document Number	Rev
A3	JV50	SB

Date: Thursday, January 08, 2009 Sheet 2 of 60



ICS9LPRS365YGLFT setting table

PIN NAME	DESCRIPTION
PCI0/CR#_A	Byte 5, bit 7 0 = PCI0 enabled (default) 1= CR#_A enabled. Byte 5, bit 6 controls whether CR#_A controls SRC0 or SRC2 pair Byte 5, bit 6 0 = CR#_A controls SRC0 pair (default), 1= CR#_A controls SRC2 pair
PCI1/CR#_B	Byte 5, bit 5 0 = PCI1 enabled (default) 1= CR#_B enabled. Byte 5, bit 6 controls whether CR#_B controls SRC1 or SRC4 pair Byte 5, bit 4 0 = CR#_B controls SRC1 pair (default) 1= CR#_B controls SRC4 pair
PCI2/TME	0 = Overclocking of CPU and SRC Allowed 1 = Overclocking of CPU and SRC NOT allowed
PCI3	
PCI4/27M_SEL	0 = Pin17 as SRC-1, Pin18 as SRC-1#, Pin13 as DOT96, Pin14 as DOT96# 1 = Pin17 as 27MHz, Pin 18 as 27MHz_SS, Pin13 as SRC-0, Pin14 as SRC-0#
PCI_F5/ITP_EN	0 =SRC8/SRC8# 1 = ITP/ITP#
SRCT3/CR#_C	Byte 5, bit 3 0 = SRC3 enabled (default) 1= CR#_C enabled. Byte 5, bit 2 controls whether CR#_C controls SRC0 or SRC2 pair Byte 5, bit 2 0 = CR#_C controls SRC0 pair (default), 1= CR#_C controls SRC2 pair

PIN NAME	DESCRIPTION
SRCC3/CR#_D	Byte 5, bit 1 0 = SRC3 enabled (default) 1= CR#_D enabled. Byte 5, bit 0 controls whether CR#_D controls SRC1 or SRC4 pair Byte 5, bit 0 0 = CR#_D controls SRC1 pair (default) 1= CR#_D controls SRC4 pair
SRCC7/CR#_E	Byte 6, bit 7 0 = SRC7# enabled (default) 1= CR#_F controls SRC6
SRCT7/CR#_F	Byte 6, bit 6 0 = SRC7 enabled (default) 1= CR#_F controls SRC8
SRCC11/CR#_G	Byte 6, bit 5 0 = SRC11# enabled (default) 1= CR#_G controls SRC9
SRCT11/CR#_H	Byte 6, bit 4 0 = SRC11 enabled (default) 1= CR#_H controls SRC10

SEL2 FSC	SEL1 FSB	SEL0 FSA	CPU	FSB
1	0	1	100M	X
0	0	1	133M	533M
0	1	1	166M	667M
0	1	0	200M	800M
0	0	0	266M	1067M

JV50

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Title: Clock Generator

Size	Document Number	Rev
	JV50	SB

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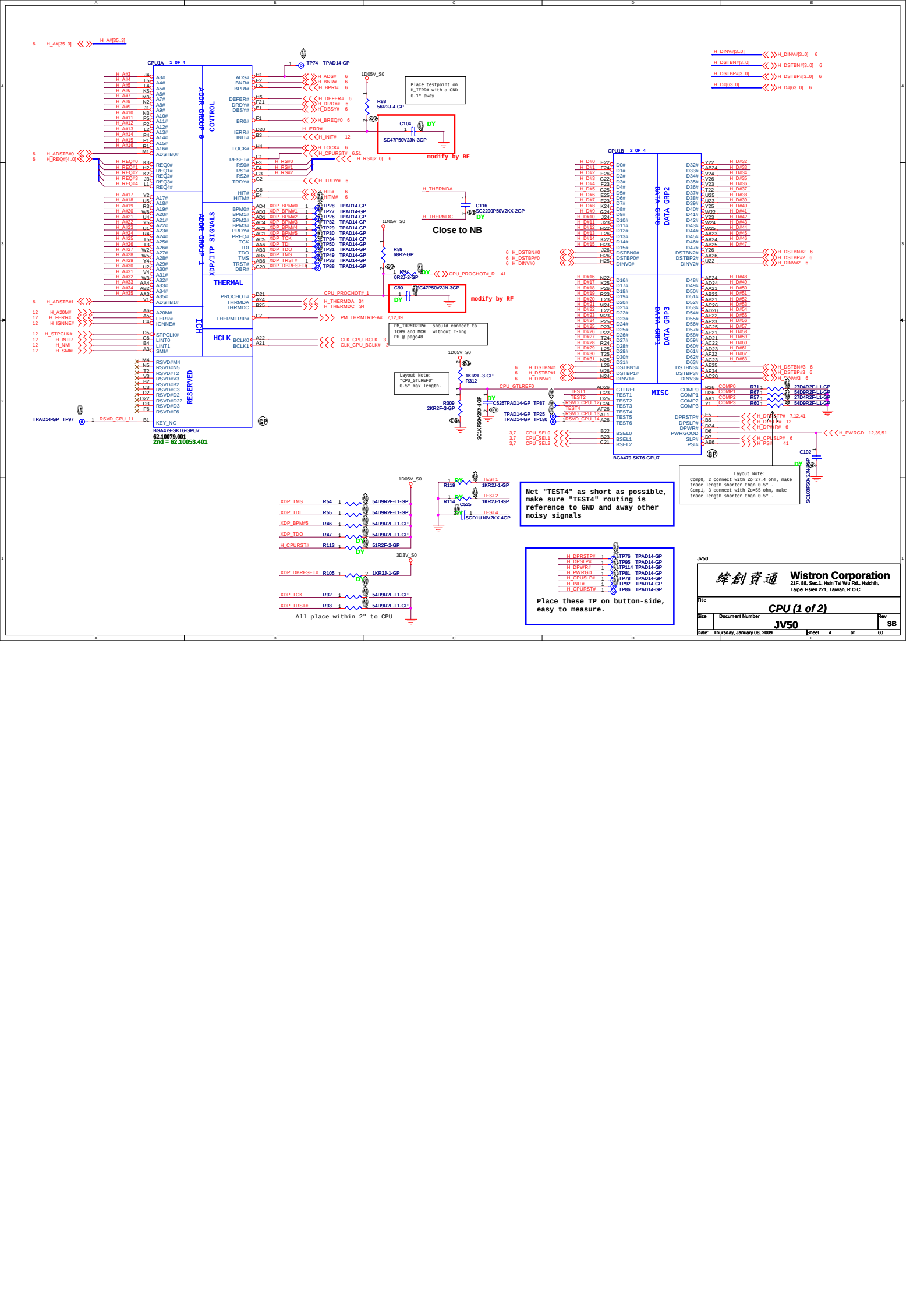
CPU1A 1 OF 4
ADDR GROUP 0
CONTROL
ADDR GROUP 1
XDP/ITP SIGNALS
THERMAL
ICH
HCLK
RESERVED
BGA479-SKT6-GPU7
62.10079.001
2nd = 62.10053.401
CPU1B 2 OF 4
DATA GRP2
DATA GRP1
DATA GRP3
MISC
BGA479-SKT6-GPU7
Close to NB
modify by RF
modify by RF
Net "TEST4" as short as possible, make sure "TEST4" routing is reference to GND and away other noisy signals
Place these TP on button-side, easy to measure.
All place within 2" to CPU
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CPU (1 of 2)
JV50
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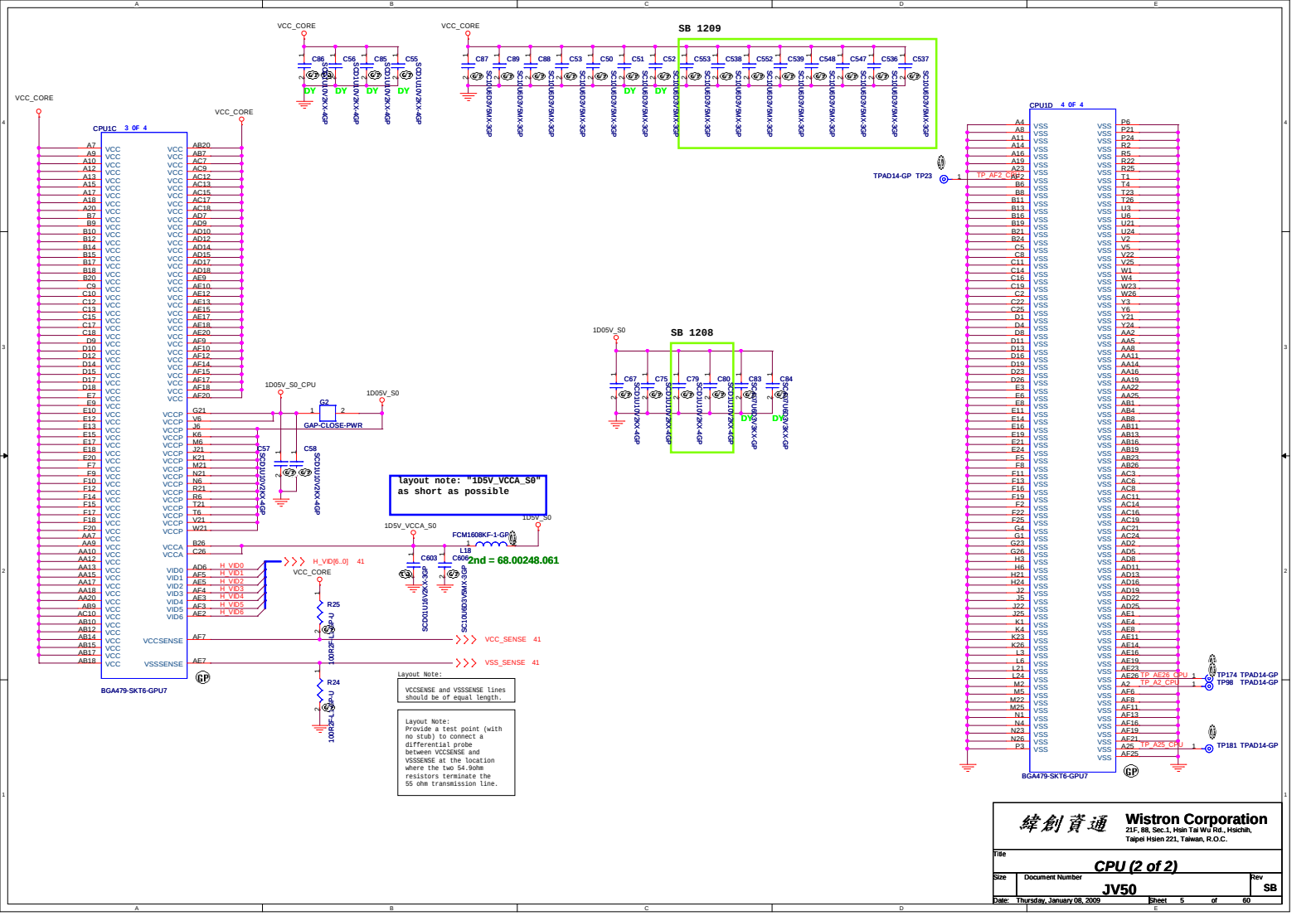

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Title	CPU (2 of 2)	
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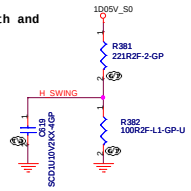
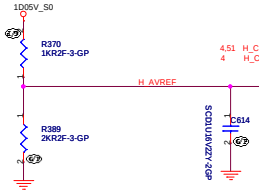
H_SWING routing Trace width and Spacing use 10 / 20 mil

H_SWING Resistors and Capacitors close MCH 500 mil (MAX)



H_RCOMP routing Trace width and Spacing use 10 / 20 mil

Place them near to the chip (< 0.5")



JV50

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Title	***Cantiga (1 of 6)***	
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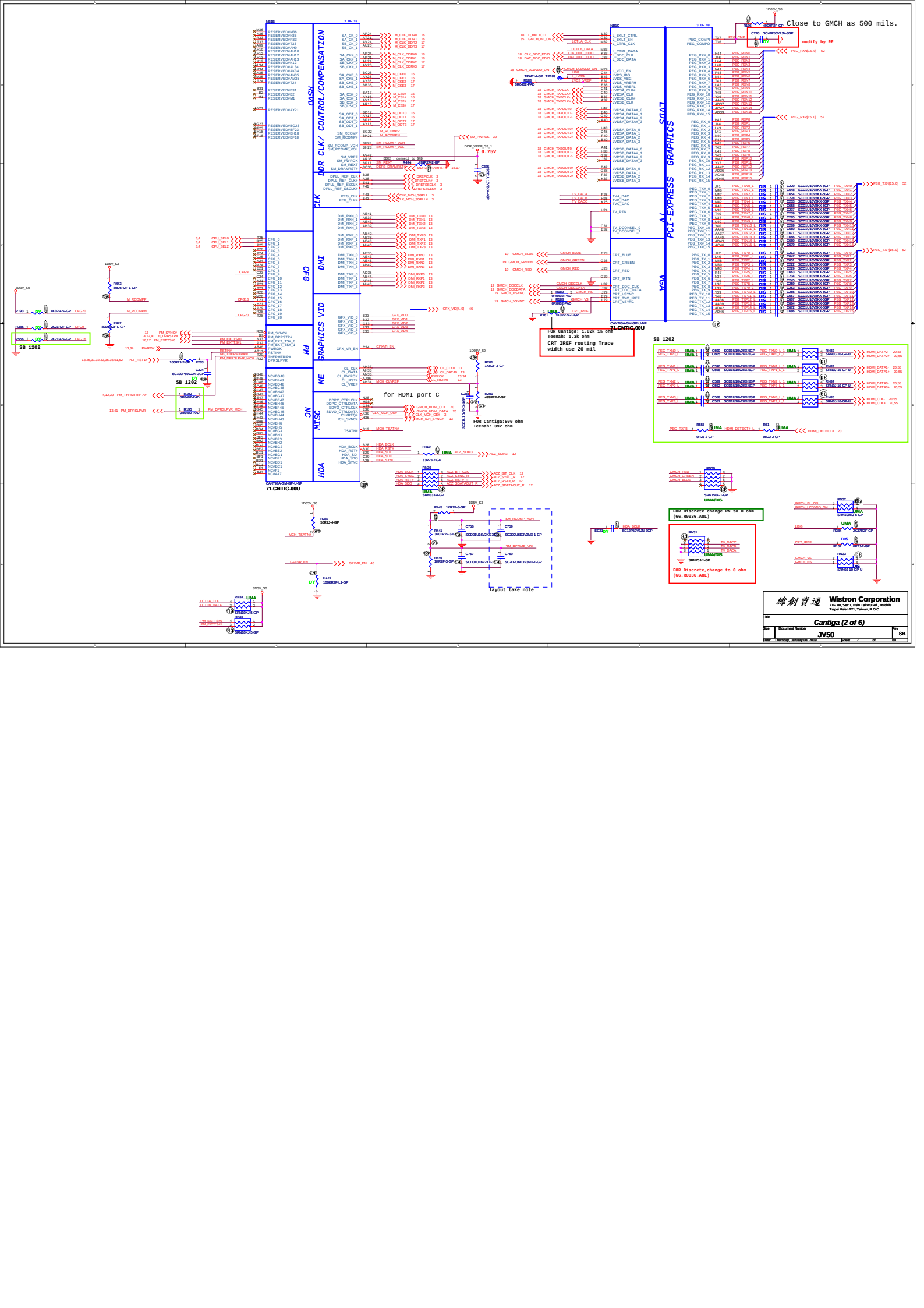
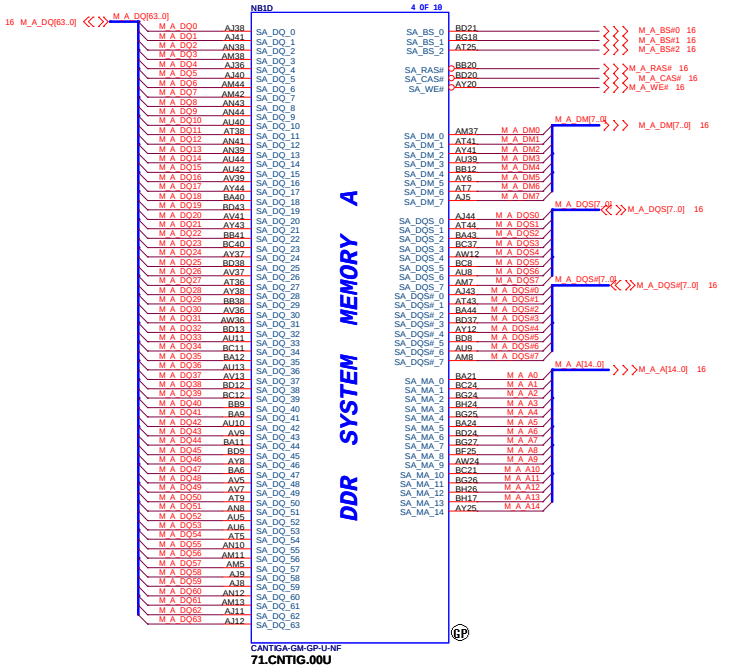
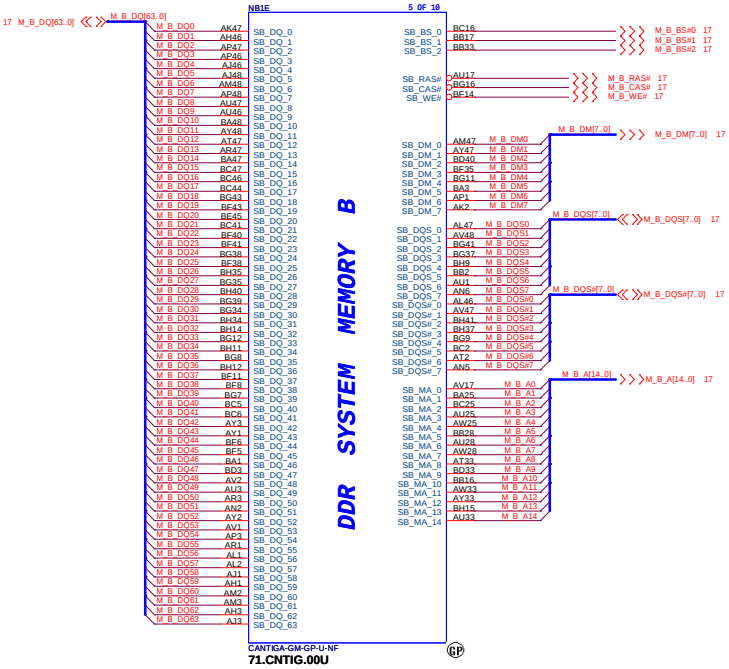

Close to GMCH as 500 mils.
modify by RF
SB 1202
71.CNTIG.00U
CANTIGA-GM-GP-U-NF
for HDMI port C
FOR Cantiga:500 ohm
Teenah: 392 ohm
FOR Cantiga: 1.02k 1% ohm
Teenah: 1.3k ohm
CRT_IREF routing Trace
width use 20 mil
FOR Discrete change RN to 0 ohm
(66.R0036.ABL)
FOR Discrete,change to 0 ohm
(66.R0036.ABL)
layout take note
Wistron Corporation
Cantiga (2 of 6)
JV50
SB





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Title: Cantiga (3 of 6)			
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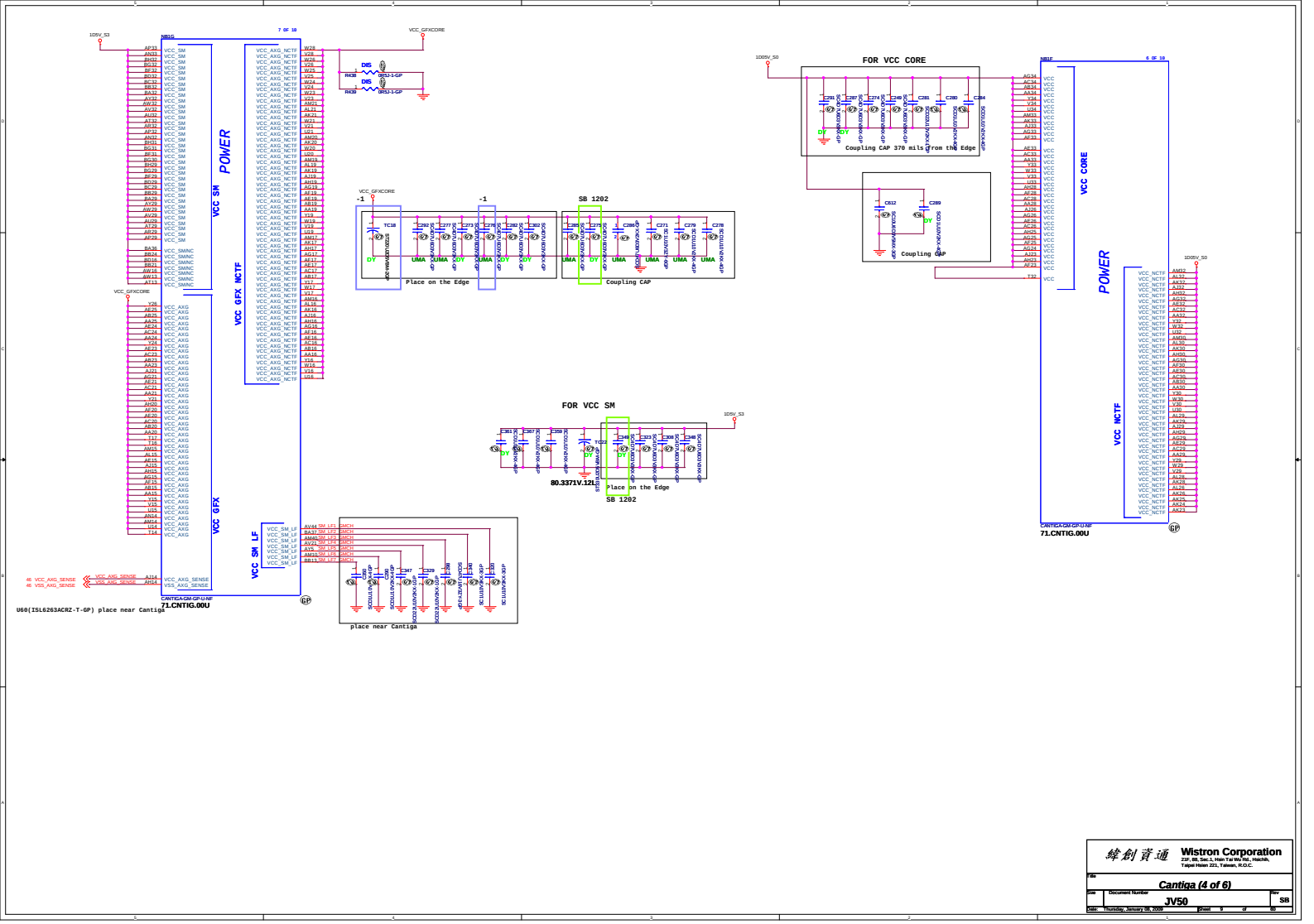

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Title: Cantiga (4 of 6)			
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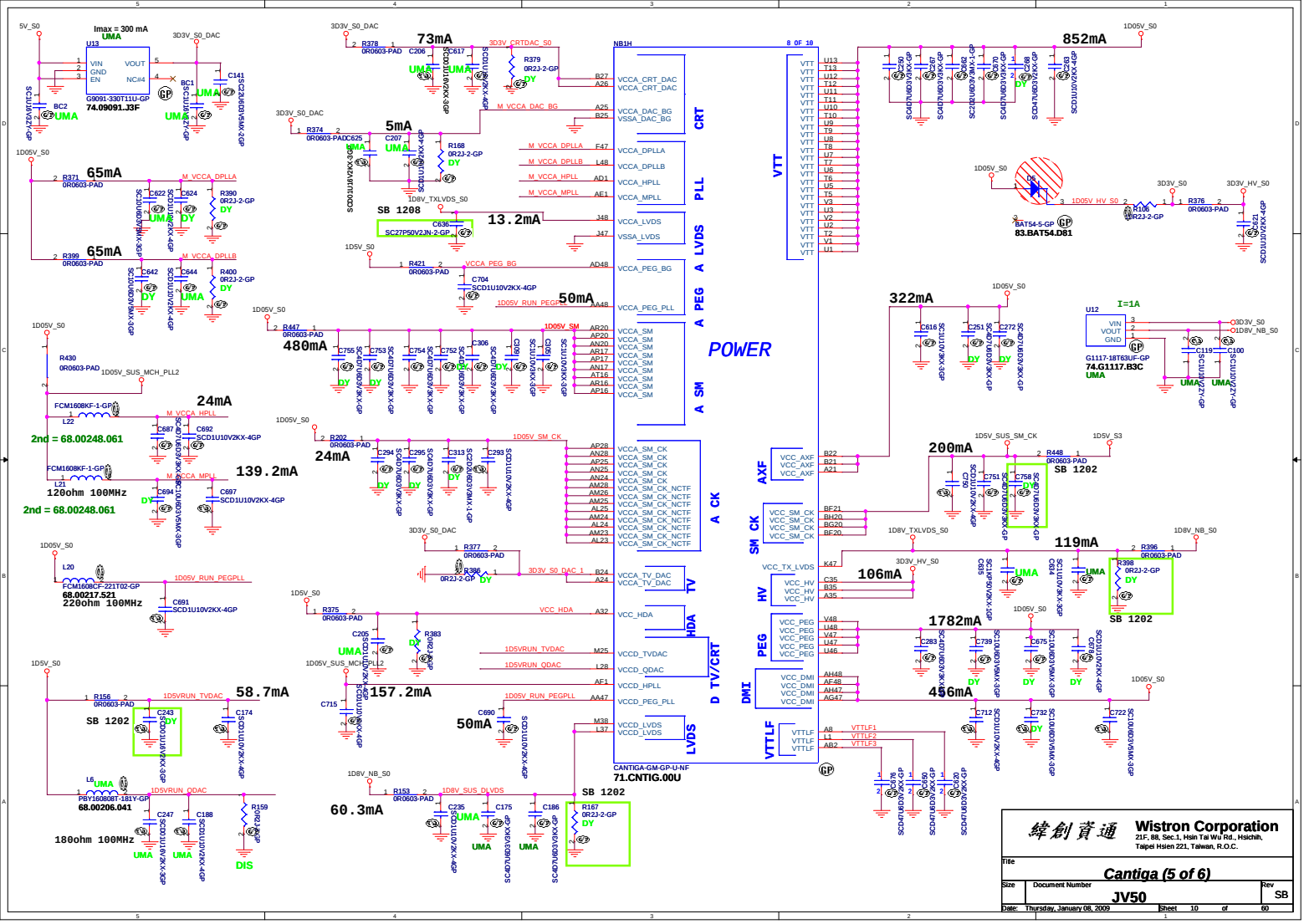
POWER
CRT
PLL
A LVDS
A PEG
A SM
A CK
TV
HDA
D TV/CRT
LVDS
AXF
SM CK
HV
PEG
DMI
VTTLF
VTT
NB1H
CANTIGA-GM-GP-U-NF
71.CNTIG.00U
Imax = 300 mA
UMA
G9091-330T11U-GP
74.09091.J3F
73mA
5mA
65mA
65mA
13.2mA
50mA
480mA
24mA
139.2mA
58.7mA
157.2mA
50mA
60.3mA
852mA
322mA
200mA
119mA
106mA
1782mA
456mA
SB 1208
SB 1202
SB 1202
SB 1202
SB 1202
24mA
2nd = 68.00248.061
2nd = 68.00248.061
68.00217.521
220ohm 100MHz
120ohm 100MHz
180ohm 100MHz
68.00206.041
83.BAT54.D81
G1117-18T63UF-GP
74.G1117.B3C
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Cantiga (5 of 6)
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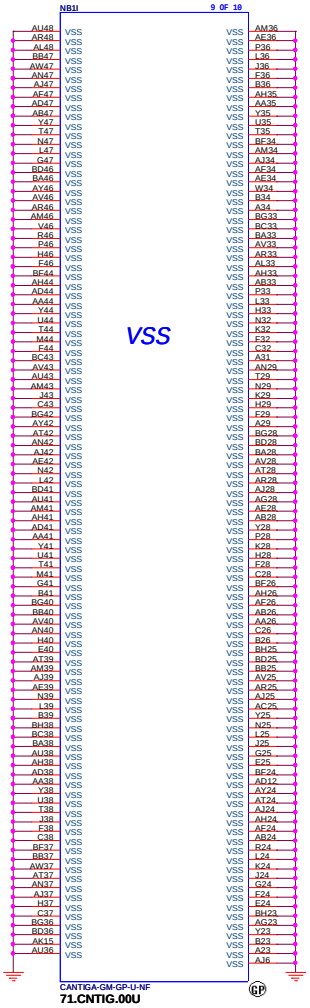

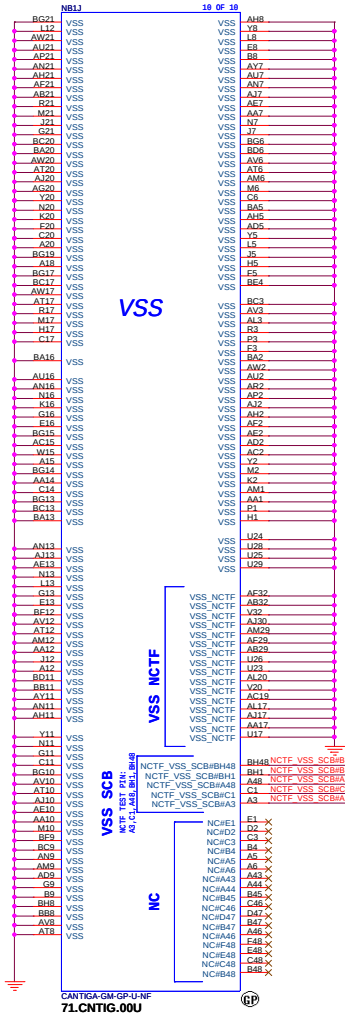

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Title	***Cantiga (6 of 6)***
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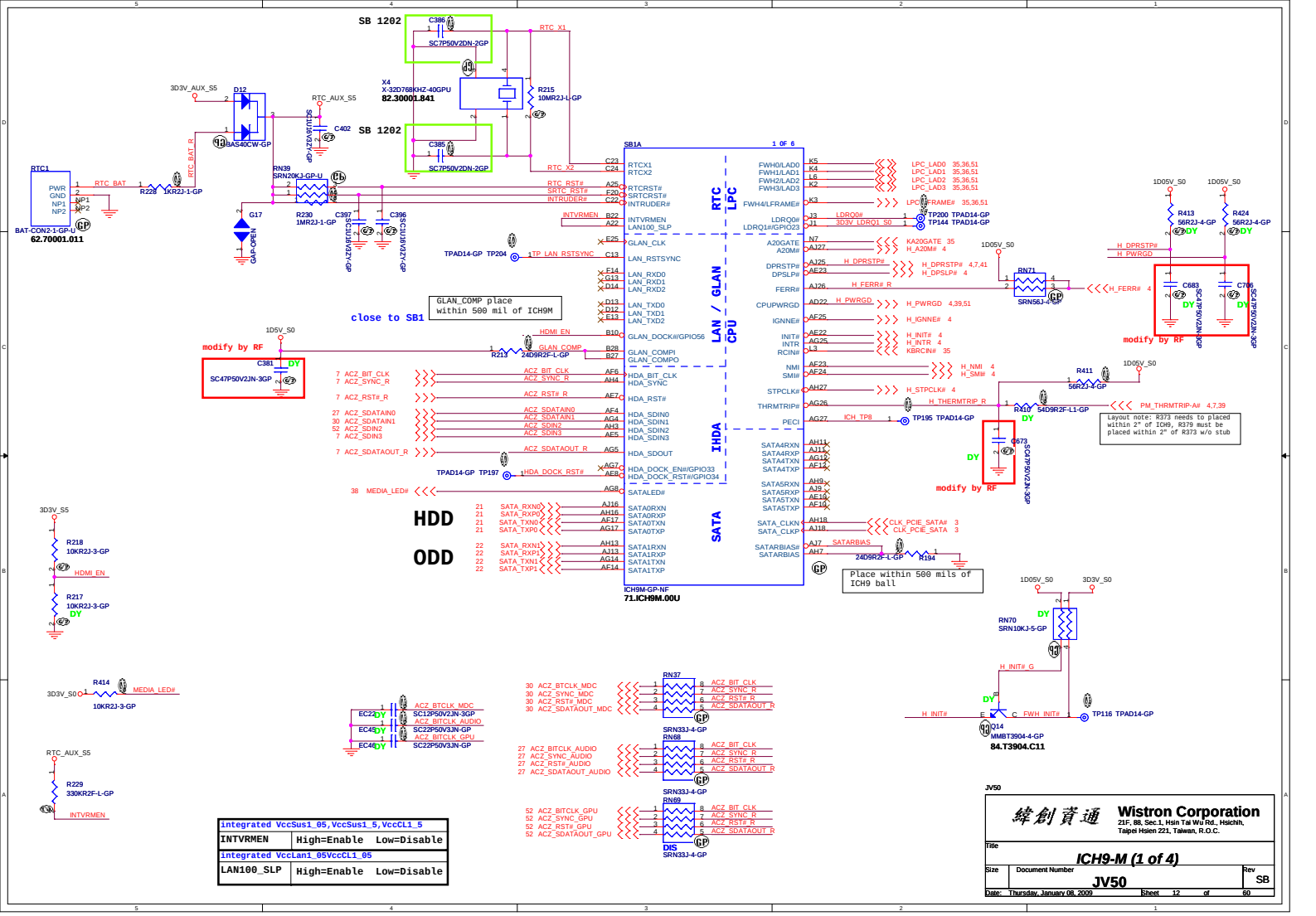
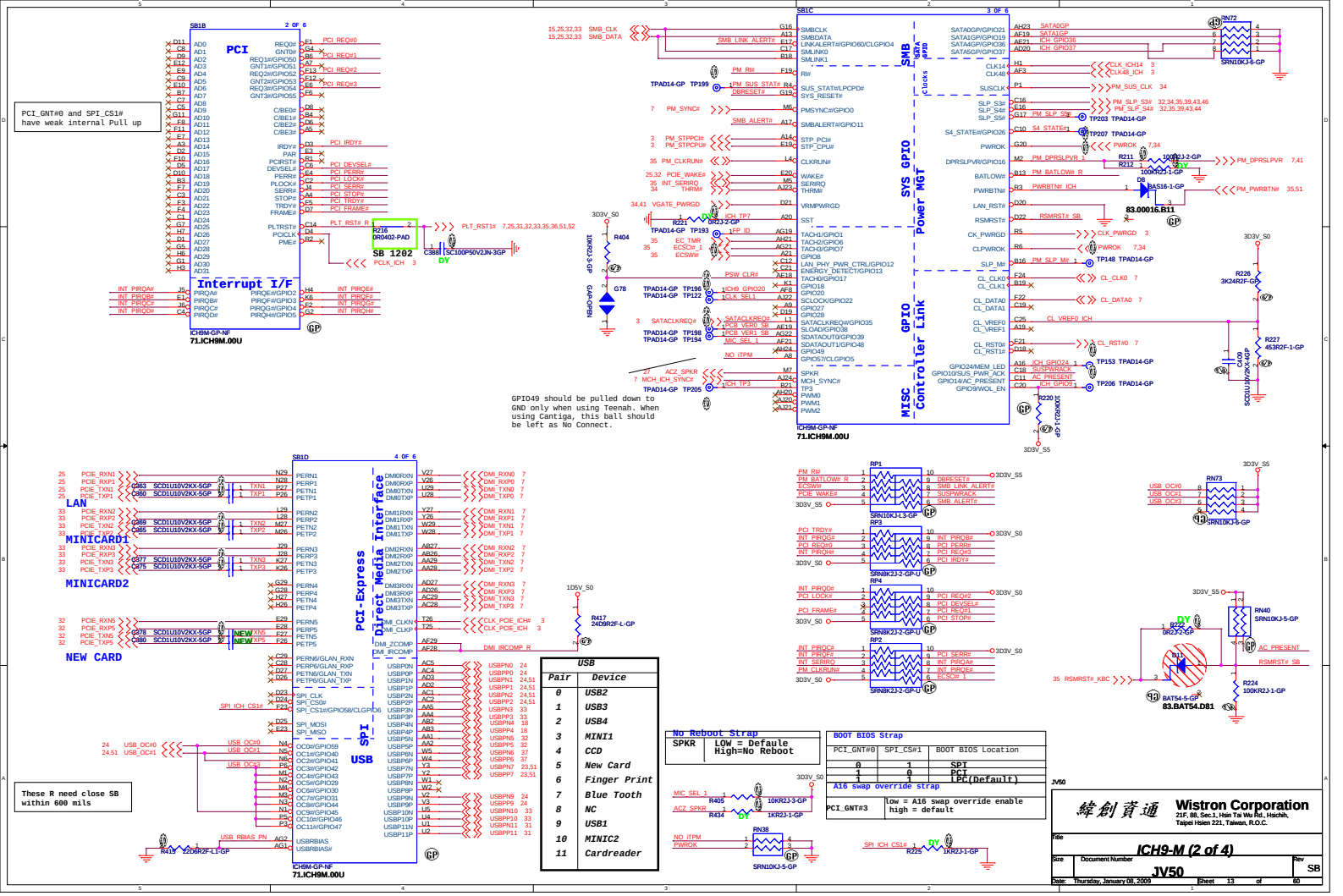

SB 1202
C386
SC7P50V2DN-2GP
RTC_X1
X4
X-32D768KHZ-40GPU
82.30001.841
R215
10MR2J-L-GP
SB 1202
C385
SC7P50V2DN-2GP
RTC_X2
3D3V_AUX_S5
D12
BAS40CW-GP
RTC_AUX_S5
C402
SC1U10V2ZY-GP
RTC_BAT_R
RTC1
BAT-CON2-1-GP
62.70001.011
RTC_BAT
R228
1KR2J-1-GP
RN39
SRN20KJ-GP-U
R230
1MR2J-1-GP
C397
SC1U10V2ZY-GP
C396
SC1U10V2ZY-GP
G17
GLP-OPEN
RTC_RST#
SRTC_RST#
INTRUDER#
INTVRMEN
TPAD14-GP TP204
TP_LAN_RSTSYNC
SB1A
1 OF 6
RTC
LPC
LAN / GLAN
CPU
IHDA
SATA
RTCX1
RTCX2
RTCRST#
SRTCRST#
INTRUDER#
INTVRMEN
LAN100_SLP
GLAN_CLK
LAN_RSTSYNC
LAN_RXD0
LAN_RXD1
LAN_RXD2
LAN_TXD0
LAN_TXD1
LAN_TXD2
GLAN_DOCK#/GPIO56
GLAN_COMPI
GLAN_COMPO
HDA_BIT_CLK
HDA_SYNC
HDA_RST#
HDA_SDIN0
HDA_SDIN1
HDA_SDIN2
HDA_SDIN3
HDA_SDOUT
HDA_DOCK_EN#/GPIO33
HDA_DOCK_RST#/GPIO34
SATALED#
SATA0RXN
SATA0RXP
SATA0TXN
SATA0TXP
SATA1RXN
SATA1RXP
SATA1TXN
SATA1TXP
FWH0/LAD0
FWH1/LAD1
FWH2/LAD2
FWH3/LAD3
FWH4/LFRAME#
LDRQ0#
LDRQ1#/GPIO23
A20GATE
A20M#
DPRSTP#
DPSLP#
FERR#
CPUPWRGD
IGNNE#
INIT#
INTR
RCIN#
NMI
SMI#
STPCLK#
THRMTRIP#
PECI
SATA4RXN
SATA4RXP
SATA4TXN
SATA4TXP
SATA5RXN
SATA5RXP
SATA5TXN
SATA5TXP
SATA_CLKN
SATA_CLKP
SATARBIAS#
SATARBIAS
ICH9M-GP-NF
71.ICH9M.00U
LPC_LAD0 35,36,51
LPC_LAD1 35,36,51
LPC_LAD2 35,36,51
LPC_LAD3 35,36,51
LPC_FRAME# 35,36,51
TP200 TPAD14-GP
TP144 TPAD14-GP
KA20GATE 35
H_A20M# 4
H_DPRSTP# 4,7,41
H_DPSLP# 4
H_FERR# 4
H_PWRGD 4,39,51
H_IGNNE# 4
H_INIT# 4
H_INTR 4
KBRCIN# 35
H_NMI 4
H_SM# 4
H_STPCLK# 4
H_THERMTRIP# 4,7,39
TP195 TPAD14-GP
CLK_PCIE_SATA# 3
CLK_PCIE_SATA 3
24D9R2F-L-GP
R194
Place within 500 mils of ICH9 ball
GLAN_COMP place within 500 mil of ICH9M
close to SB1
HDMI_EN
R213
24D9R2F-L-GP
modify by RF
C381
SC47P50V2JN-3GP
ACZ_BIT_CLK
ACZ_SYNC_R
ACZ_RST#_R
ACZ_SDATAIN0
ACZ_SDATAIN1
ACZ_SDIN2
ACZ_SDIN3
ACZ_SDATAOUT_R
TPAD14-GP TP197
HDA_DOCK_RST#
MEDIA_LED#
HDD
ODD
SATA_RXN0
SATA_RXP0
SATA_TXN0
SATA_TXP0
SATA_RXN1
SATA_RXP1
SATA_TXN1
SATA_TXP1
1D05V_S0
RN71
SRN56J-4-GP
H_DPRSTP#
H_PWRGD
H_FERR#
R413
56R2J-4-GP
R424
56R2J-4-GP
C683
SC47P50V2JN-3GP
C706
SC47P50V2JN-3GP
modify by RF
R411
56R2J-4-GP
R410
54D9R2F-L1-GP
PM_THRMTRIP-A# 4,7,39
Layout note: R373 needs to placed within 2" of ICH9, R373 must be placed within 2" of R373 w/o stub
C673
SC47P50V2JN-3GP
modify by RF
3D3V_S5
R218
10KR2J-3-GP
HDMI_EN
R217
10KR2J-3-GP
DY
3D3V_S0
R414
10KR2J-3-GP
MEDIA_LED#
RTC_AUX_S5
R229
330KR2F-L-GP
INTVRMEN
EC22 DY
EC45 DY
EC46 DY
SC12P50V2JN-3GP
SC22P50V3JN-GP
SC22P50V3JN-GP
ACZ_BITCLK_MDC
ACZ_BITCLK_AUDIO
ACZ_BITCLK_GPU
RN37
RN68
RN69
SRN33J-4-GP
30 ACZ_BITCLK_MDC
30 ACZ_SYNC_MDC
30 ACZ_RST#_MDC
30 ACZ_SDATAOUT_MDC
27 ACZ_BITCLK_AUDIO
27 ACZ_SYNC_AUDIO
27 ACZ_RST#_AUDIO
27 ACZ_SDATAOUT_AUDIO
52 ACZ_BITCLK_GPU
52 ACZ_SYNC_GPU
52 ACZ_RST#_GPU
52 ACZ_SDATAOUT_GPU
ACZ_BIT_CLK
ACZ_SYNC_R
ACZ_RST#_R
ACZ_SDATAOUT_R
DIS
RN70
SRN10KJ-5-GP
H_INIT#_G
H_INIT#
FWH_INIT#
TP116 TPAD14-GP
Q14
MMBT3904-4-GP
84.T3904.C11
integrated VccSus1_05,VccSus1_5,VccCL1_5
INTVRMEN High=Enable Low=Disable
integrated VccLan1_05VccCL1_05
LAN100_SLP High=Enable Low=Disable
JV50
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.
Title
ICH9-M (1 of 4)
Size
Document Number
JV50
Rev
SB
Date: Thursday, January 08, 2009
Sheet 12 of 60


PCI_GNT#0 and SPI_CS1# have weak internal Pull up
SB1B
2 OF 6
PCI
Interrupt I/F
ICH9M-GP-NF
71.ICH9M.00U
SB 1202
SC1U10V2KX-3GP
PCLK_ICH
PLT_RST#
R216 0R402-PAD
GPIO49 should be pulled down to GND only when using Teenah. When using Cantiga, this ball should be left as No Connect.
SB1C
3 OF 6
SMB
SYS GPIO
Power MGT
GPIO
Controller Link
MISC
SATA0GP/GPIO21
SATA1GP/GPIO19
SATA4GP/GPIO36
SATA5GP/GPIO37
CLK14
CLK48
SUSCLK
SLP_S3#
SLP_S4#
SLP_S5#
S4_STATE#/GPIO26
PWROK
DPRSLPVR/GPIO16
BATLOW#
PWRBTN#
LAN_RST#
RSMRST#
CK_PWRGD
CLPWROK
SLP_M#
CL_CLK0
CL_CLK1
CL_DATA0
CL_DATA1
CL_VREF0
CL_VREF1
CL_RST0#
CL_RST1#
GPIO24/MEM_LED
GPIO10/SUS_PWR_ACK
GPIO14/AC_PRESENT
GPIO9/WOL_EN
TACH1/GPIO1
TACH2/GPIO6
TACH3/GPIO7
GPIO8
LAN_PHY_PWR_CTRL/GPIO12
ENERGY_DETECT/GPIO13
TACH0/GPIO17
GPIO18
GPIO20
SCLOCK/GPIO22
GPIO27
GPIO28
SATACLKREQ#/GPIO35
SLOAD/GPIO38
SDATAOUT0/GPIO39
SDATAOUT1/GPIO48
GPIO49
GPIO57/CLGPIO5
SPKR
MCH_SYNC#
TP3
PWM0
PWM1
PWM2
ICH9M-GP-NF
71.ICH9M.00U
83.00016.B11
BAS16-1-GP
SCD1U10V2KX-4GP
R227 453R2F-1-GP
R226 3K24R2F-GP
R211 100KR2J-2-GP
R212 100KR2J-1-GP
R220 10KR2J-4-GP
RN72 SRN10KJ-6-GP
RN73 SRN10KJ-6-GP
RP1 SRN10KJ-L3-GP
RP3 SRN8K2J-2-GP-U
RP4 SRN8K2J-2-GP-U
RP2 SRN8K2J-2-GP-U
RN40 SRN10KJ-5-GP
RN38 SRN10KJ-5-GP
R417 24D8R2F-L-GP
R405 10KR2J-3-GP
R434 1KR2J-1-GP
R225 1KR2J-GP
R224 100KR2J-1-GP
R222 0R2J-2-GP
BAT54-5-GP
83.BAT54.D81
SB1D
4 OF 6
PCI-Express
Direct Media Interface
SPI
USB
LAN
MINICARD1
MINICARD2
NEW CARD
ICH9M-GP-NF
71.ICH9M.00U
These R need close SB within 600 mils
R419 22D6R2F-L1-GP
USB
Pair
Device
0
USB2
1
USB3
2
USB4
3
MINI1
4
CCD
5
New Card
6
Finger Print
7
Blue Tooth
8
NC
9
USB1
10
MINIC2
11
Cardreader
No Reboot Strap
SPKR
LOW = Defaule
High=No Reboot
BOOT BIOS Strap
PCI_GNT#0
SPI_CS#1
BOOT BIOS Location
0
1
SPI
1
0
PCI
1
1
LPC(Default)
A16 swap override Strap
PCI_GNT#3
low = A16 swap override enable
high = default
JV50
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.
Title
ICH9-M (2 of 4)
Size
Document Number
JV50
Rev
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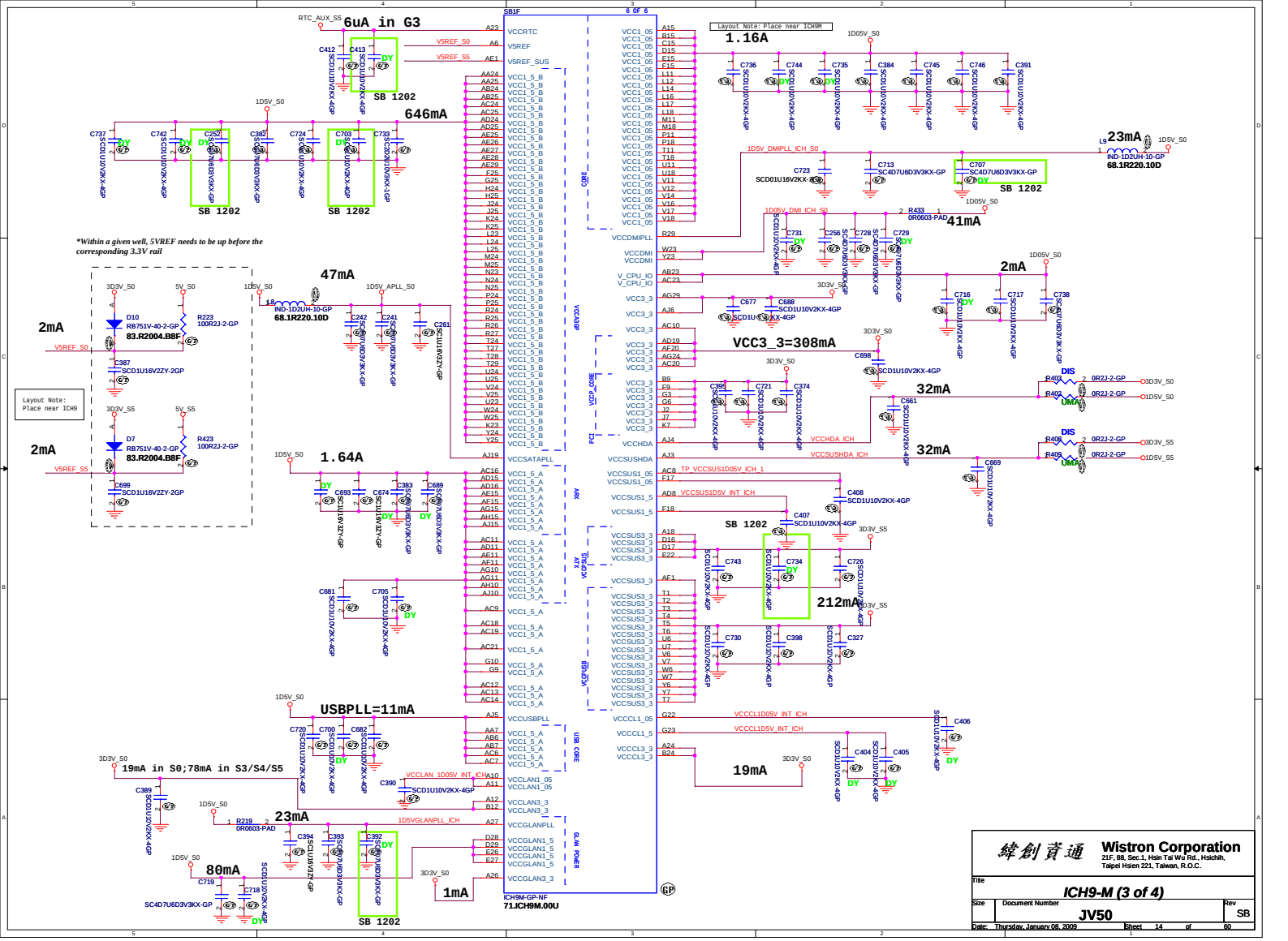
Date: Thursday, January 08, 2009
Sheet 13 of 60


6uA in G3
646mA
SB 1202
*Within a given well, 5VREF needs to be up before the corresponding 3.3V rail
47mA
2mA
2mA
1.64A
USBPLL=11mA
19mA in S0;78mA in S3/S4/S5
23mA
80mA
1mA
1.16A
23mA
41mA
2mA
VCC3_3=308mA
32mA
32mA
212mA
19mA
SB1F
6 OF 6
ICH9M-GP-NF
71.ICH9M.00U
Layout Note: Place near ICH9M
Layout Note: Place near ICH9
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.
ICH9-M (3 of 4)
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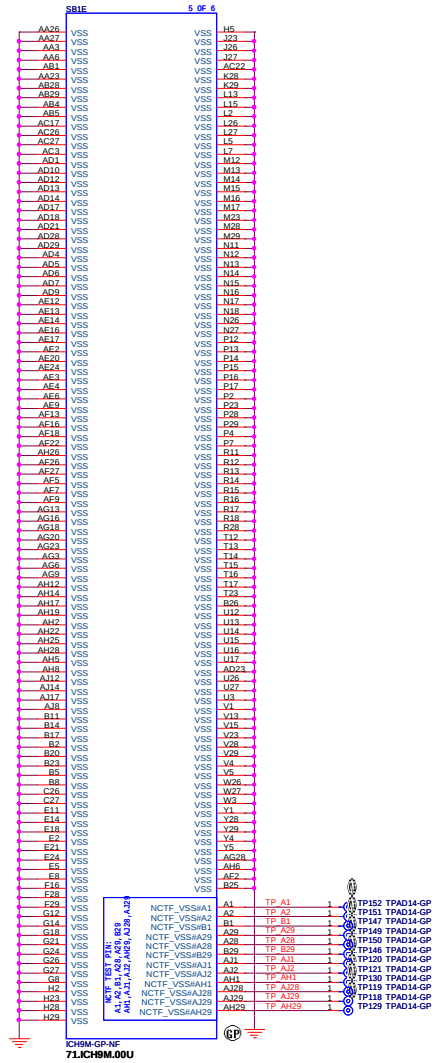
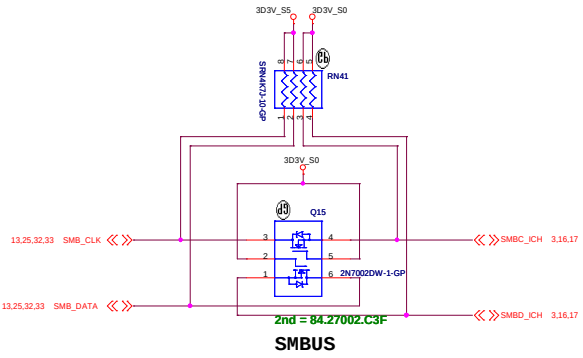
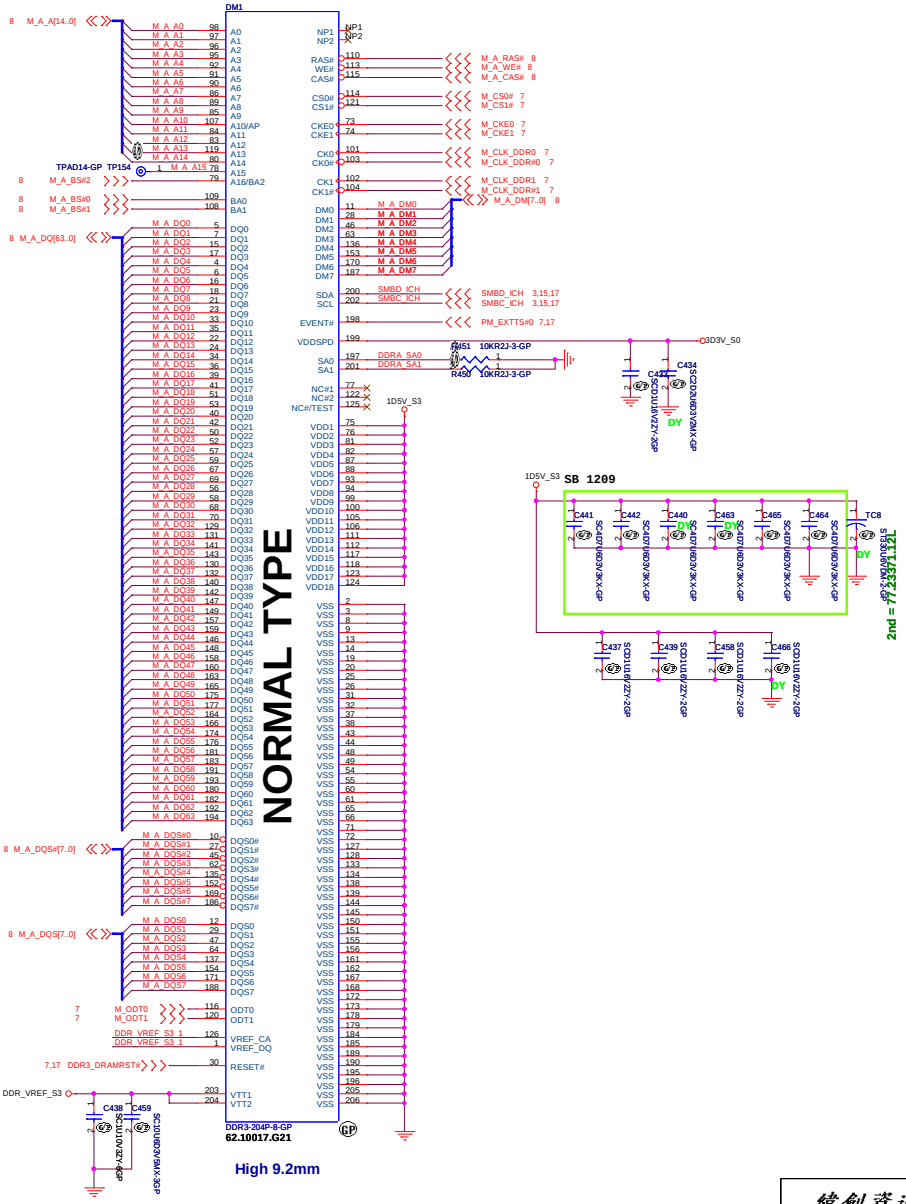
14
60



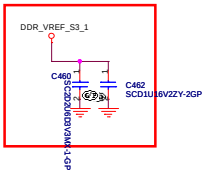


緯創資通 Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.			
Title: ICH9-M (4 of 4)			
Size	Document Number: JV50		Rev: SB
Date: Thursday, January 08, 2009	Sheet 15 of 60		

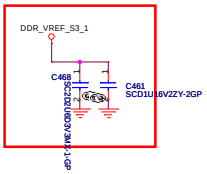
DDR3 SOCKET_1



Layout Note：Near Pin 126

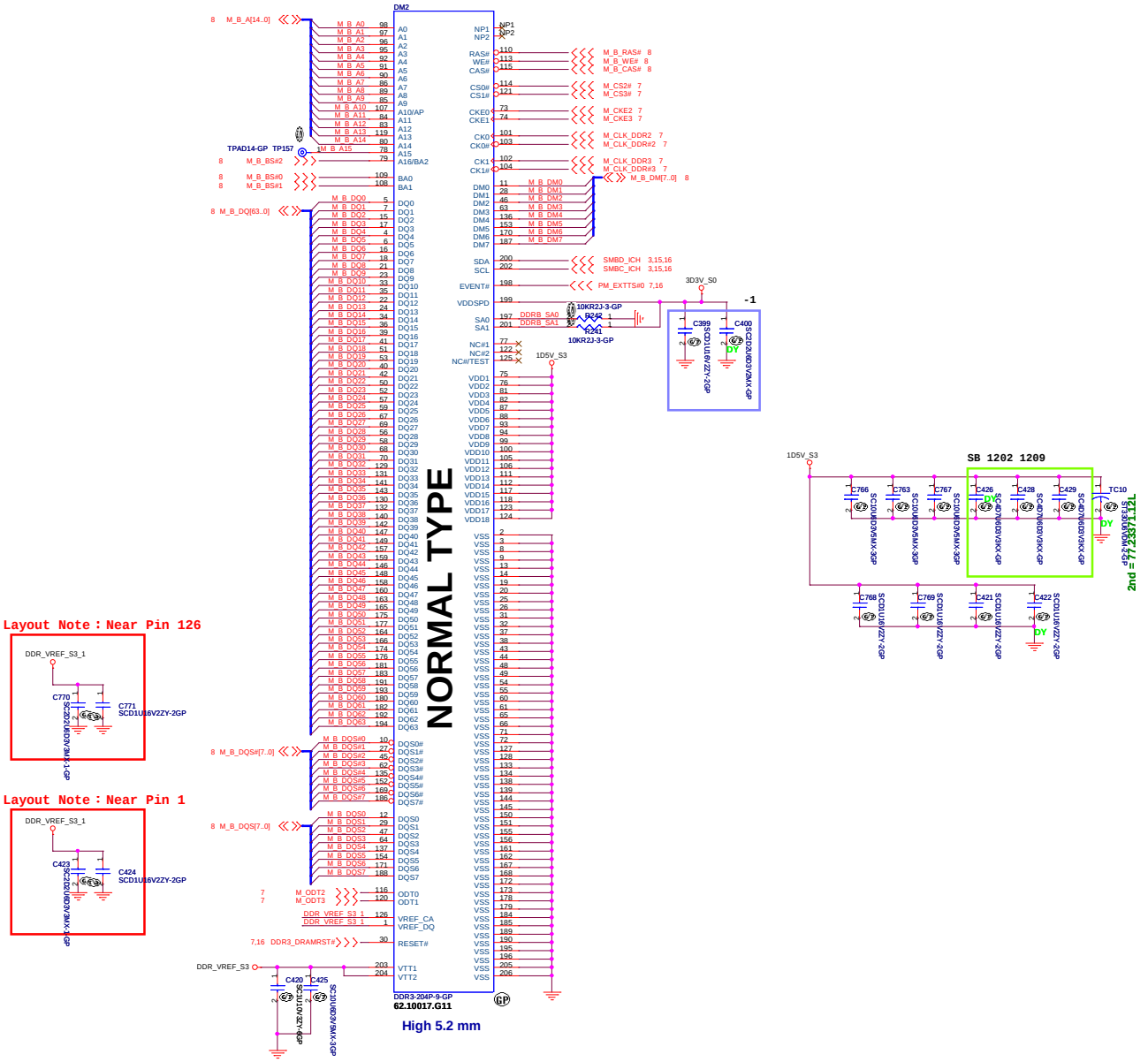


Layout Note：Near Pin 1



緯創資通 Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.			
Title: DDR3 Socket			
Size	Document Number: JV50		Rev: SB
Date: Thursday, January 08, 2009	Sheet 16 of 60		

DDR3 SOCKET_2



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Title: DDR3 Socket2			
Size	Document Number: JV50	Rev: SB	
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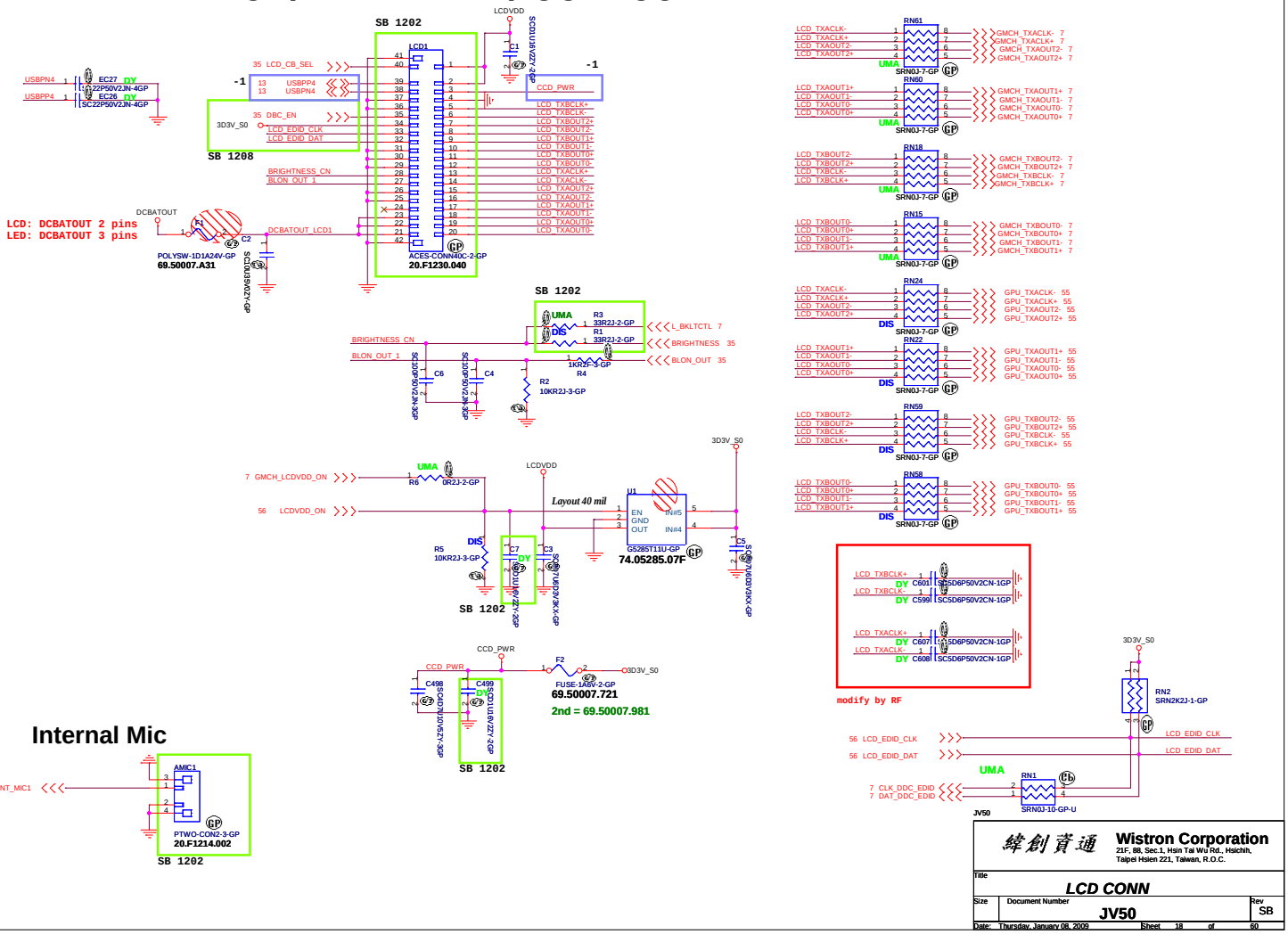
LCD/INVERTER/CCD CONN



緯創資通 Wistron Corporation
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Taipei Hsien 221, Taiwan, R.O.C.

Title: **LCD CONN**

Size	Document Number	Rev
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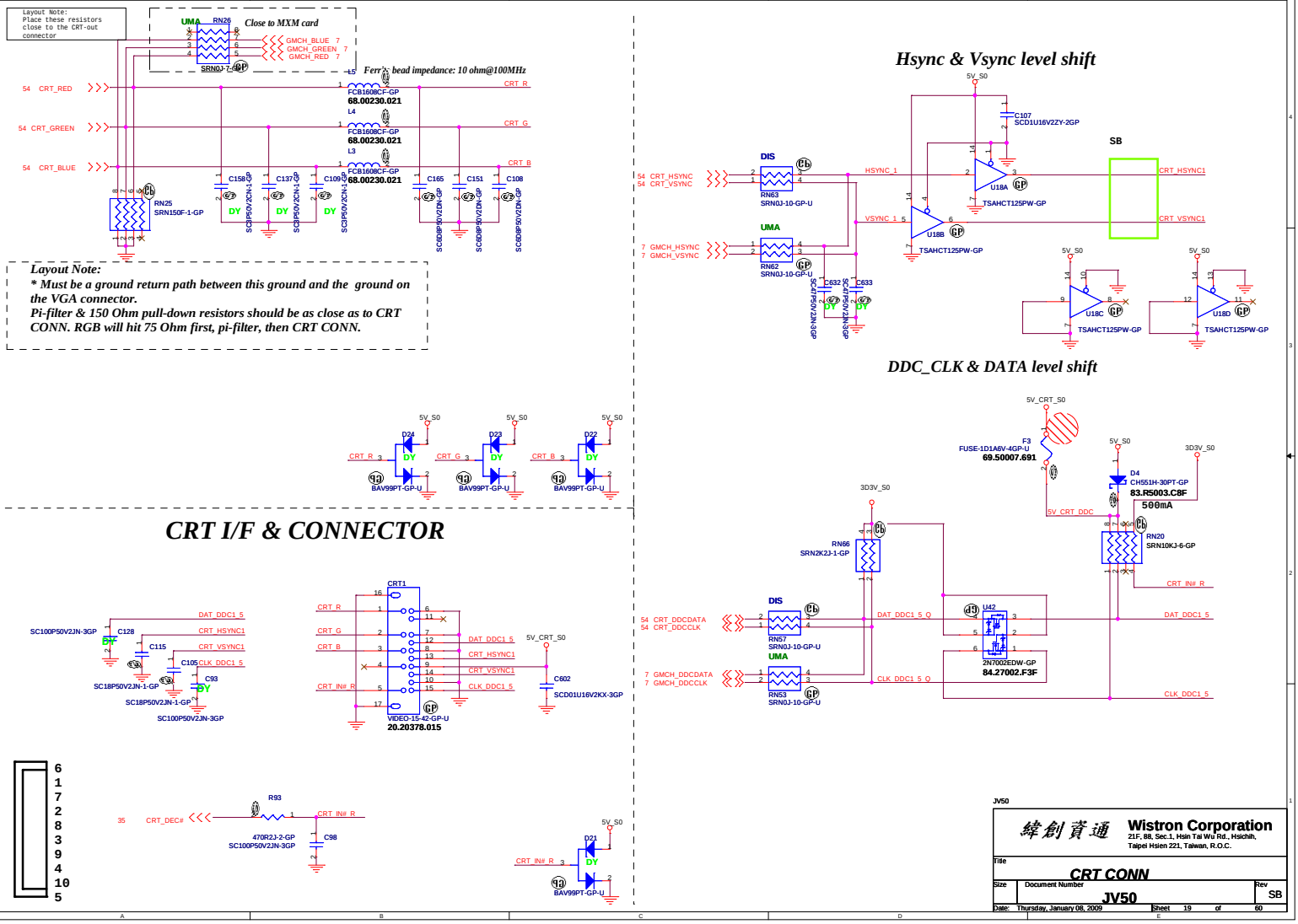
Layout Note:
Place these resistors close to the CRT-out connector
UMA
RN26
SRN0J-7-GP
Close to MXM card
GMCH_BLUE 7
GMCH_GREEN 7
GMCH_RED 7
54 CRT_RED
54 CRT_GREEN
54 CRT_BLUE
L5
L4
L3
FCB1608CF-GP
68.00230.021
Ferrite bead impedance: 10 ohm@100MHz
CRT_R
CRT_G
CRT_B
RN25
SRN150F-1-GP
C158
C137
C109
C165
C151
C108
DY
SC18P50V2CN-1-GP
SC680P50V2KN-GP
Layout Note:
* Must be a ground return path between this ground and the ground on the VGA connector.
Pi-filter & 150 Ohm pull-down resistors should be as close as to CRT CONN. RGB will hit 75 Ohm first, pi-filter, then CRT CONN.
Hsync & Vsync level shift
5V_S0
C107
SCD1U16V2ZY-2GP
SB
DIS
54 CRT_HSYNC
54 CRT_VSYNC
RN63
SRN0J-10-GP-U
HSYNC_1
VSYNC_1_5
U18A
U18B
TSAHCT125PW-GP
CRT_HSYNC1
CRT_VSYNC1
UMA
7 GMCH_HSYNC
7 GMCH_VSYNC
RN62
SRN0J-10-GP-U
C632
C633
SC47P50V2JN-3GP
SC18P50V2JN-3GP
U18C
U18D
DDC_CLK & DATA level shift
5V_CRT_S0
F3
FUSE-1D1A6V-4GP-U
69.50007.691
3D3V_S0
D4
CH551H-30PT-GP
83.R5003.C8F
500mA
5V_CRT_DDC
RN20
SRN10KJ-6-GP
CRT_IN# R
RN66
SRN2K2J-1-GP
54 CRT_DDCDATA
54 CRT_DDCCLK
RN57
SRN0J-10-GP-U
DAT_DDC1_5_Q
CLK_DDC1_5_Q
U42
2N7002EDW-GP
84.27002.F3F
7 GMCH_DDCDATA
7 GMCH_DDCCLK
RN53
SRN0J-10-GP-U
DAT_DDC1_5
CLK_DDC1_5
D24
D23
D22
CRT_R
CRT_G
CRT_B
BAV99PT-GP-U
CRT I/F & CONNECTOR
SC100P50V2JN-3GP
C128
C115
C105
C93
CRT_HSYNC1
CRT_VSYNC1
CLK_DDC1_5
DAT_DDC1_5
SC18P50V2JN-1-GP
SC100P50V2JN-3GP
CRT1
VIDEO-15-42-GP-U
20.20378.015
C602
SCD01U16V2KX-3GP
R93
35 CRT_DEC#
470R2J-2-GP
SC100P50V2JN-3GP
C98
D21
6 1 7 2 8 3 9 4 10 5
JV50
緯創資通
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.
Title
CRT CONN
Size
Document Number
JV50
Rev
SB
Date: Thursday, January 08, 2009
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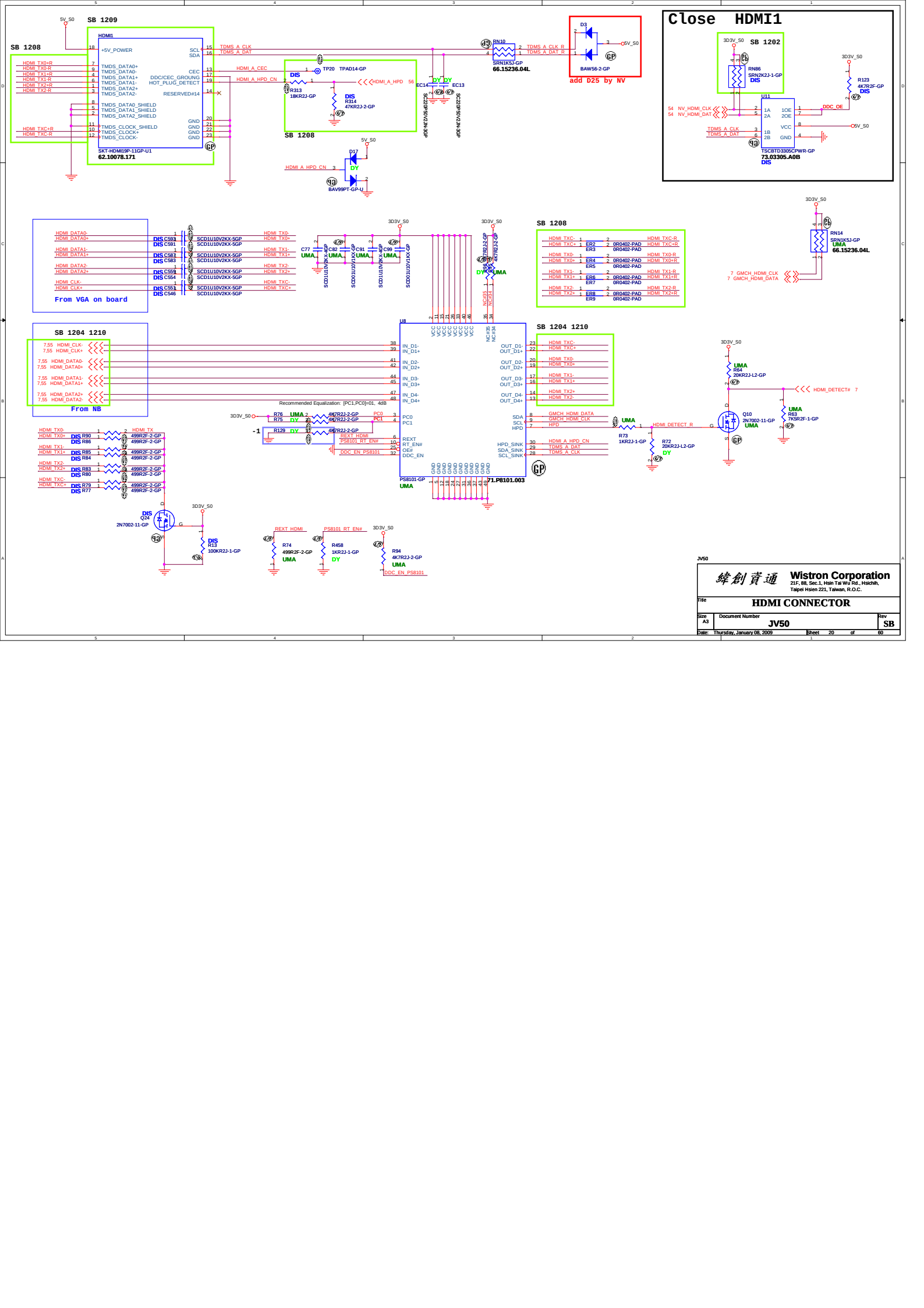
Close HDMI1
SB 1209
SB 1208
HDMI1
SKT-HDMI19P-11GP-U1
62.10078.171
TDMS_A_CLK
TDMS_A_DAT
HDMI_A_CEC
HDMI_A_HPD_CN
HDMI_A_HPD
TP20 TPAD14-GP
R313 18KR2J-GP
R314 47KR2J-2-GP
SC220P50V2JN-3GP
EC14
EC13
RN10
SRN1K5J-GP
66.15236.04L
TDMS_A_CLK_R
TDMS_A_DAT_R
D3
BAW56-2-GP
add D25 by NV
SB 1202
RN86
SRN2K2J-1-GP
R123
4K7R2F-GP
U11
TSCBTD3305CPWR-GP
73.03305.A0B
DDC_OE
NV_HDMI_CLK
NV_HDMI_DAT
D17
BAV99PT-GP-U
From VGA on board
From NB
SB 1204 1210
SB 1208
SCD1U10V2KX-5GP
C77
C82
C91
C99
U8
PS8101-GP
71.P8101.003
Recommended Equalization: [PC1,PC0]=01, 4dB
R76
R75
R129
REXT_HDMI
PS8101_RT_EN#
DDC_EN_PS8101
RN14
SRN1K5J-GP
66.15236.04L
HDMI_DETECT#
Q10
2N7002-11-GP
R64
20KR2J-L2-GP
R63
7K5R2F-1-GP
R73
1KR2J-1-GP
R72
20KR2J-L2-GP
Q24
R13
100KR2J-1-GP
R74
499R2F-2-GP
R458
1KR2J-1-GP
R94
4K7R2J-2-GP
3D3V_S0
5V_S0
JV50
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.
HDMI CONNECTOR
Size A3
Document Number JV50
Rev SB
Date: Thursday, January 08, 2009
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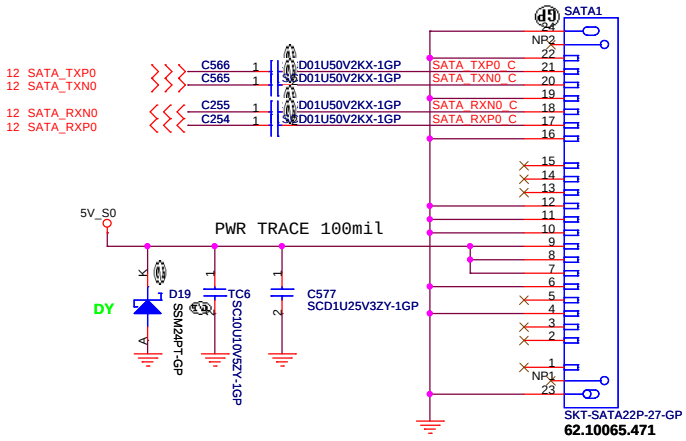
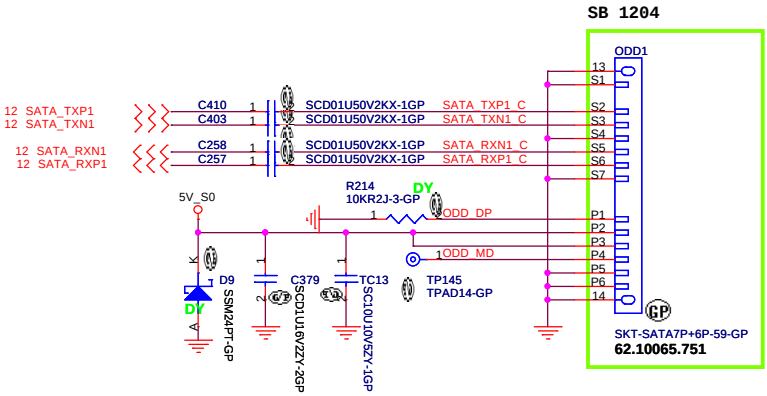
SATA Connector



JV50

緯創資通 Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.		
Title: *HDD CONN*		
Size	Document Number: JV50	Rev: SB
Date: Thursday, January 08, 2009	Sheet 21 of 60	

ODD Connector



JV50

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title		
ODD		
Size	Document Number	Rev
	JV50	SB
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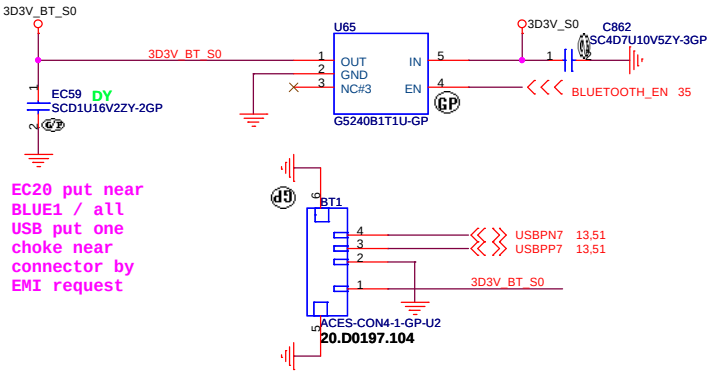
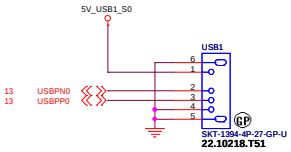
BLUETOOTH MODULE

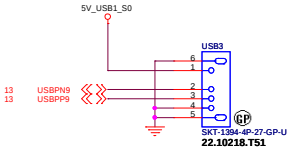


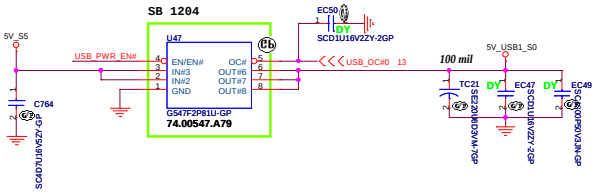
JV50

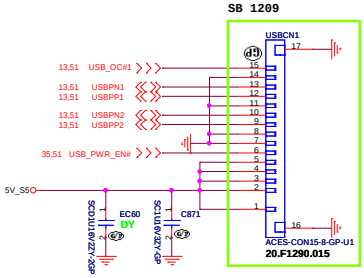
緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title	***BLUETOOTH***	
Size	Document Number **JV50**	Rev SB
Date: Thursday, January 08, 2009	Sheet 23 of 60	









JV50

緯創資通	**Wistron Corporation** 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.
Title	*USB CONN*
Size / Document Number	JV50 / Rev SB
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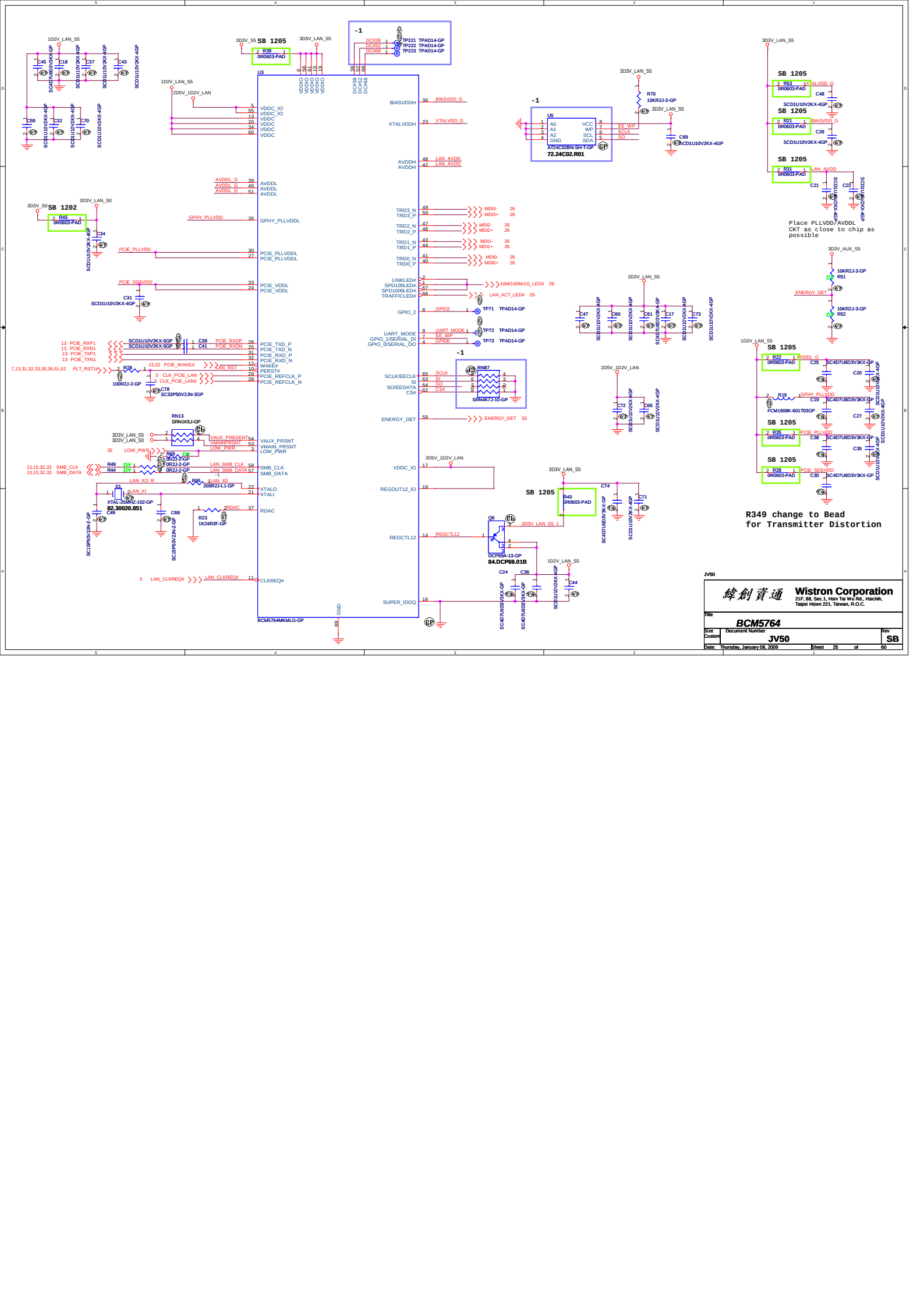
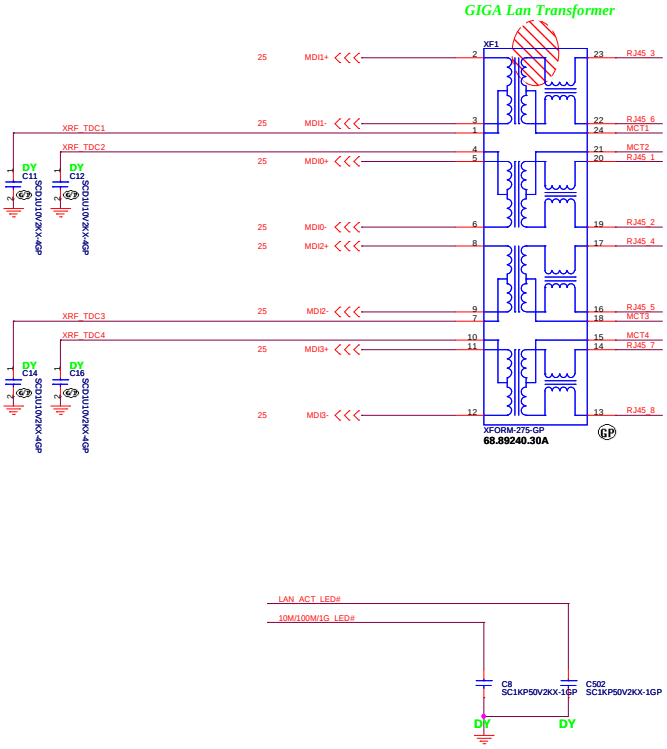

U3
BCM5764MKMLG-GP
SB 1205
SB 1202
Place PLLVDD/AVDDL CKT as close to chip as possible
R349 change to Bead for Transmitter Distortion
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.
BCM5764
JV50
Size: Custom
Document Number: JV50
Rev: SB
Date: Thursday, January 08, 2009
Sheet 25 of 60

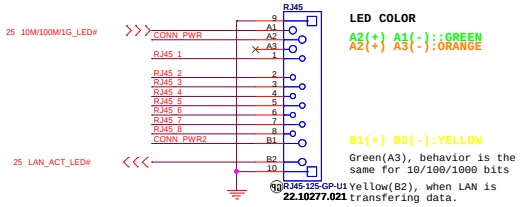
1.route on bottom as differential pairs.
2.Tx+/Tx- are pairs. Rx+/Rx- are pairs.
3.No vias, No 90 degree bends.
4.pairs must be equal lengths.
5.6mil trace width,12mil separation.
6.36mil between pairs and any other trace.
7.Must not cross ground moat,except
RJ-45 moat.

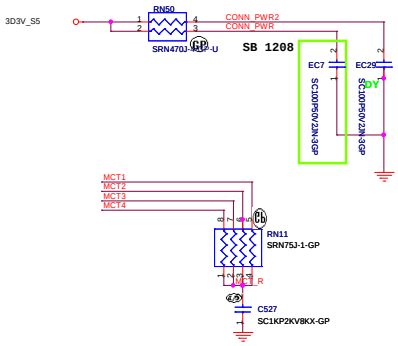
LAN Connector

LAN Connector

GIGA Lan Transformer







JV50

緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: **LAN CONN**

Size	Document Number	Rev
A3	JV50	SB

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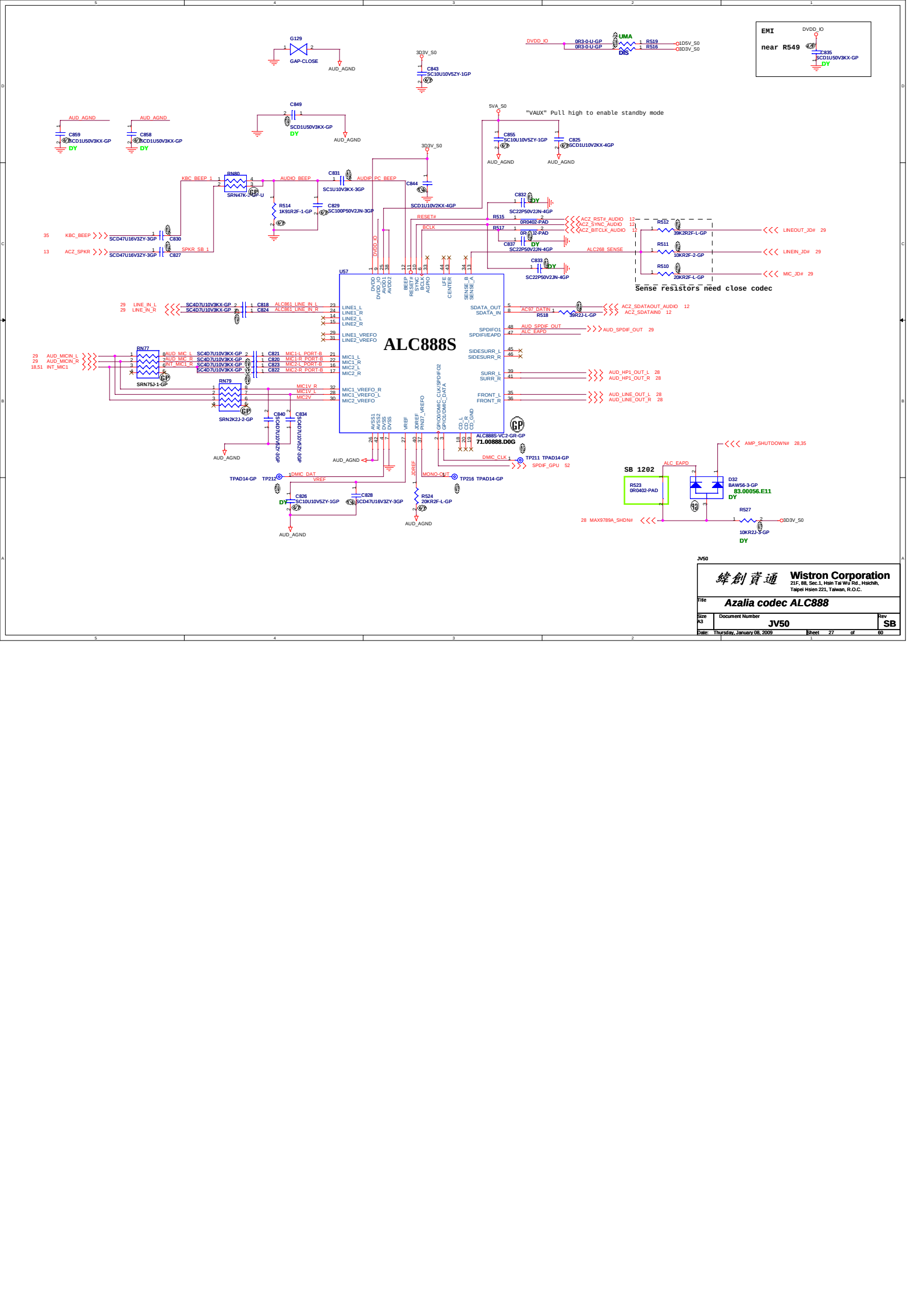
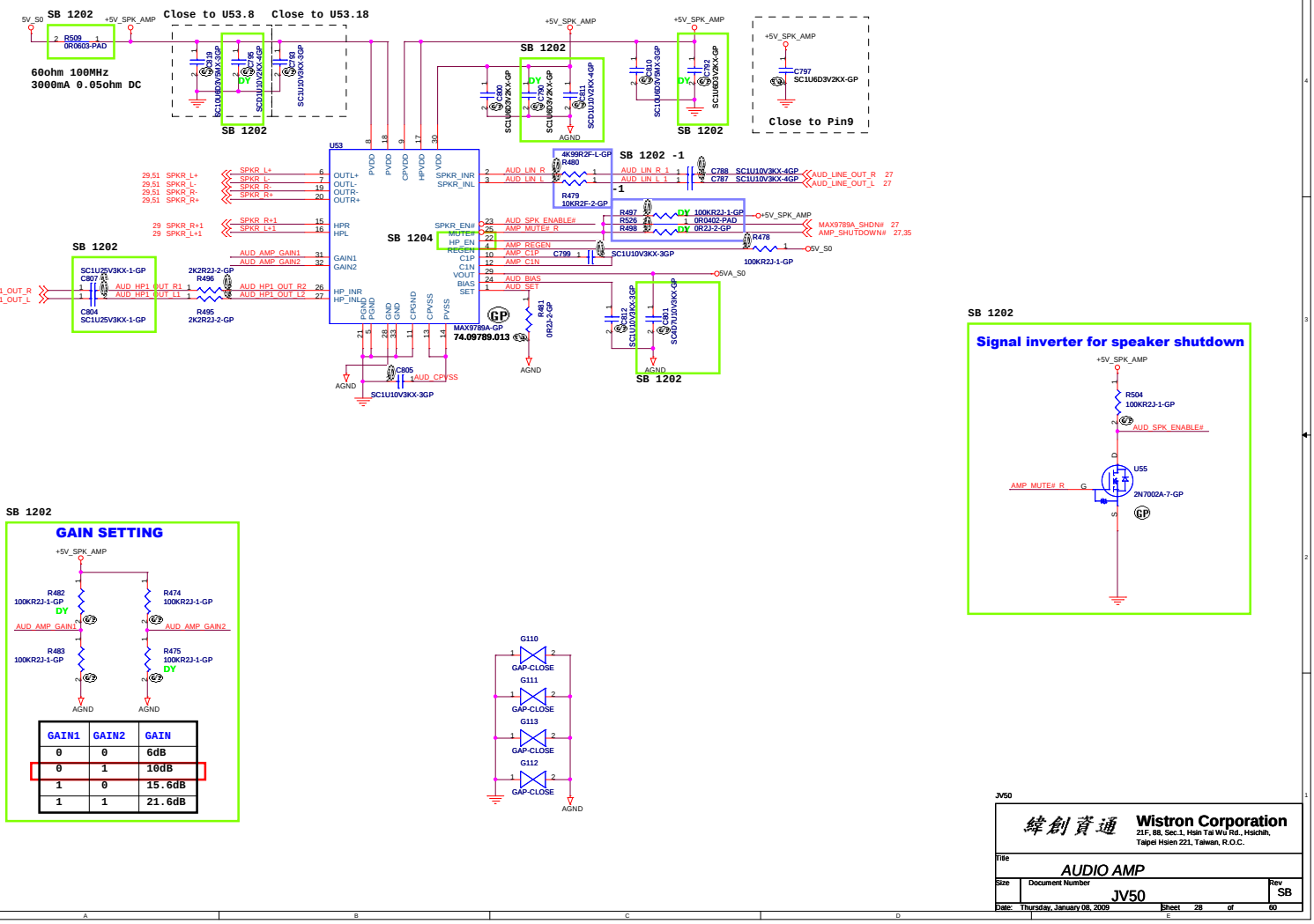
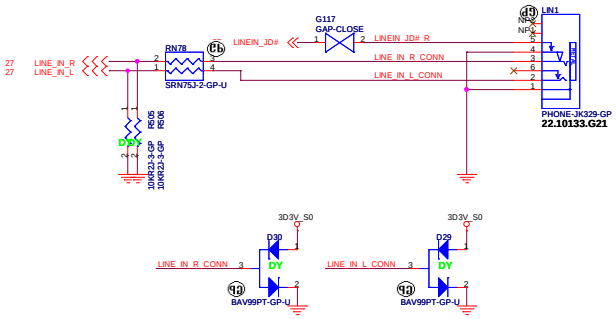


JV50

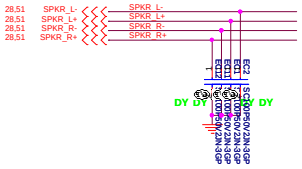
緯創資通	Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title	Azalia codec ALC888	
Size A3	Document Number JV50	Rev SB
Date: Thursday, January 08, 2009	Sheet 27 of 60	


SB 1202
Close to U53.8
Close to U53.18
60ohm 100MHz
3000mA 0.05ohm DC
SB 1202
SB 1202
SB 1202
Close to Pin9
SB 1204
SB 1202 -1
SB 1202
SB 1202
SB 1202
Signal inverter for speaker shutdown
SB 1202
GAIN SETTING
GAIN1 GAIN2 GAIN
0 0 6dB
0 1 10dB
1 0 15.6dB
1 1 21.6dB
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.
AUDIO AMP
JV50
Thursday, January 08, 2009

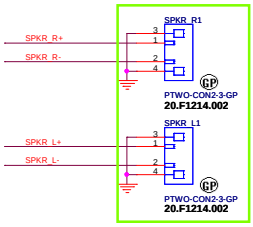
LINE IN



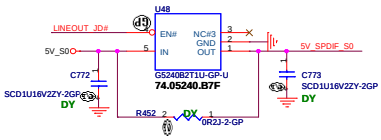
Internal Speaker

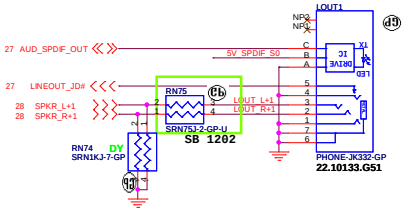


SB 1202

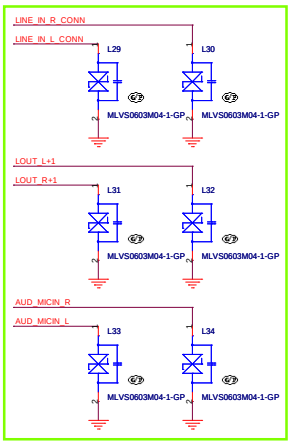


LINE OUT

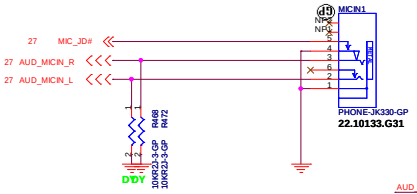


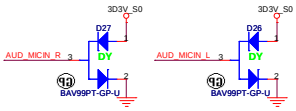


SB 1202



MIC IN

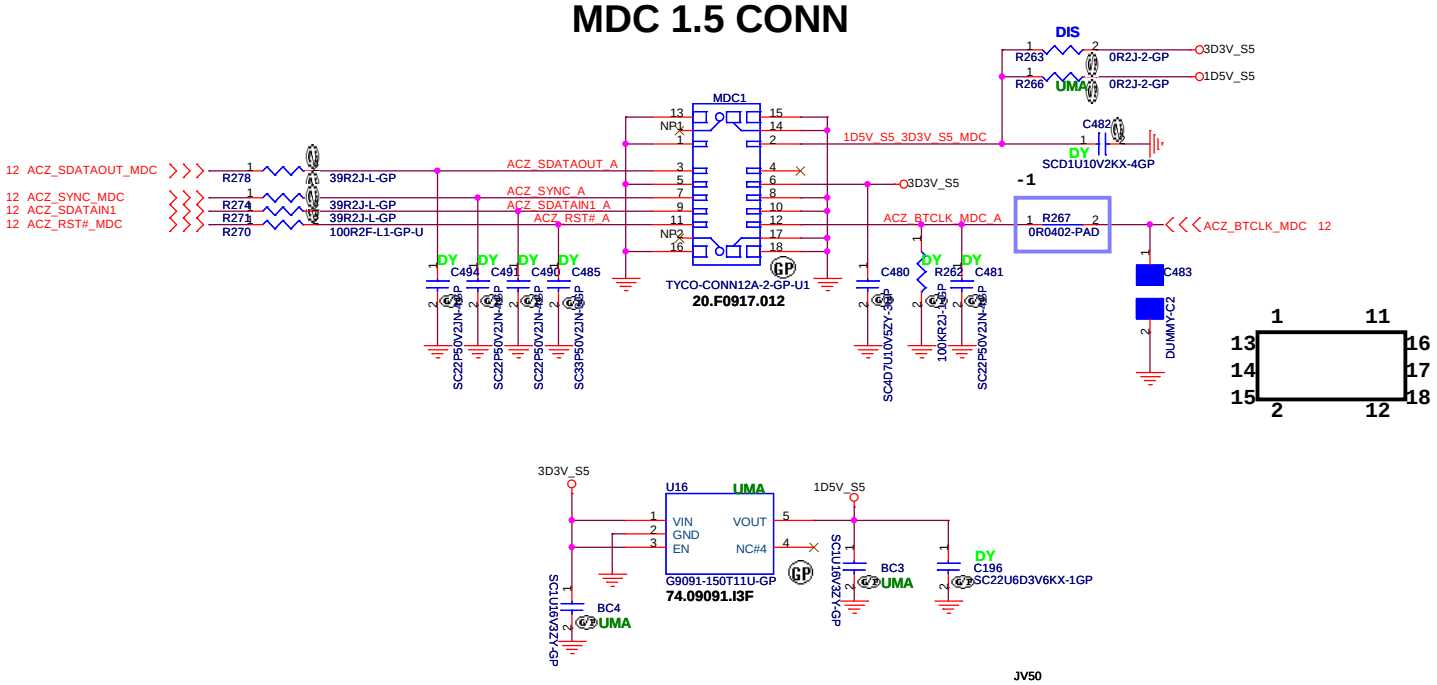




JV50

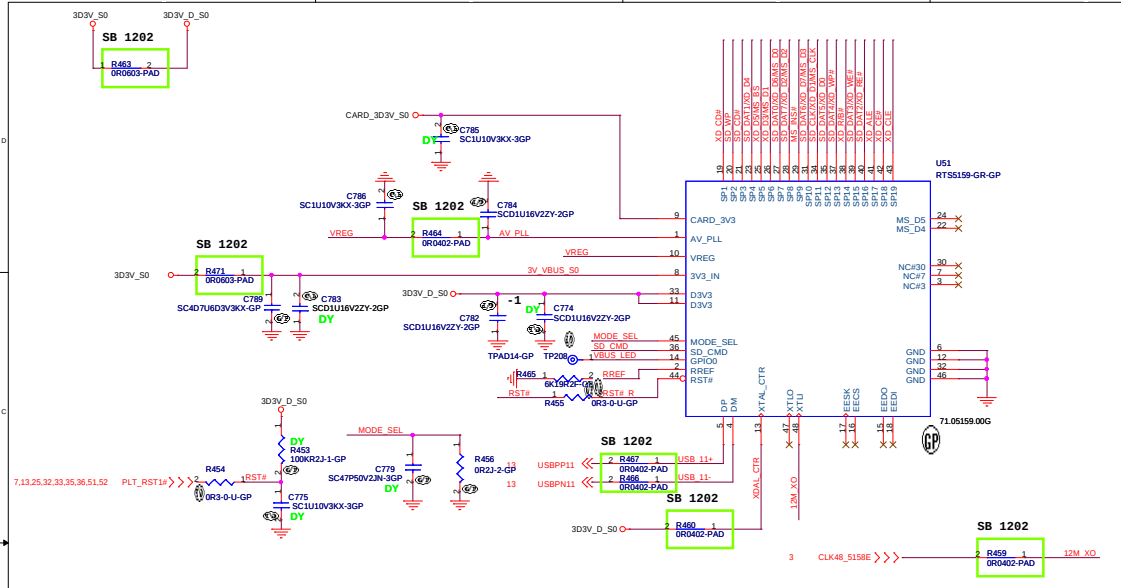
緯創資通 Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.		
Title: AUDIO jack		
Size	Document Number: JV50	Rev: SB
Date: Thursday, January 08, 2009	Sheet 29 of 60	

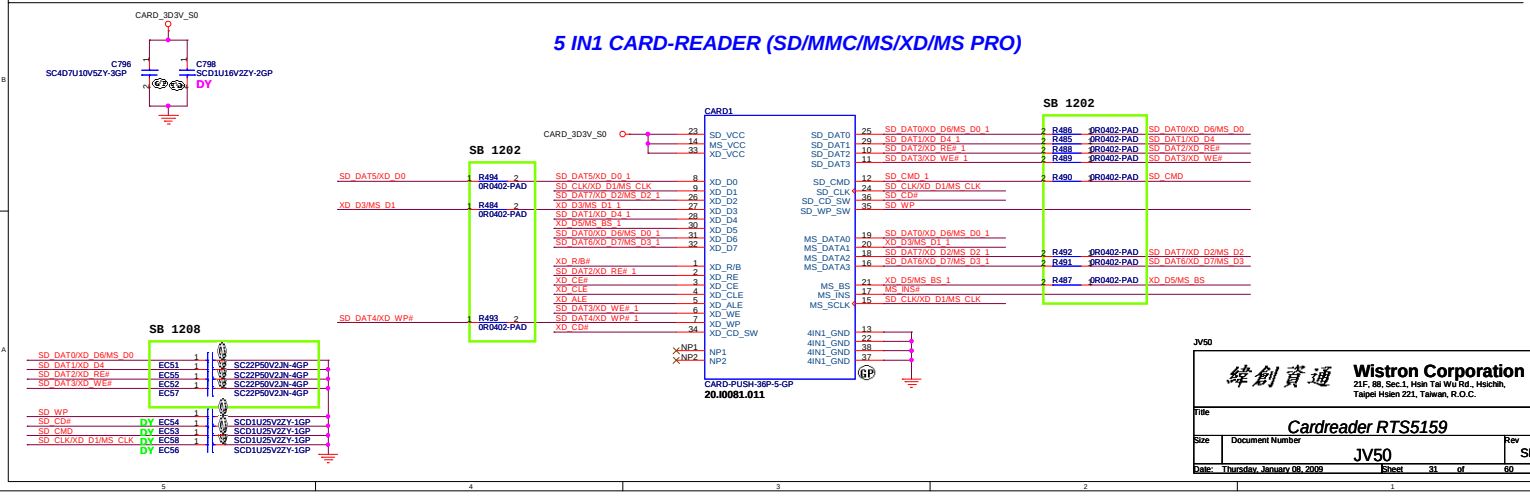
MDC 1.5 CONN



JV50

緯創資通	**Wistron Corporation** 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title	***MDC***	
Size	Document Number **JV50**	Rev SB
Date: Thursday, January 08, 2009	Sheet 30 of 60	





5 IN1 CARD-READER (SD/MMC/MS/XD/MS PRO)

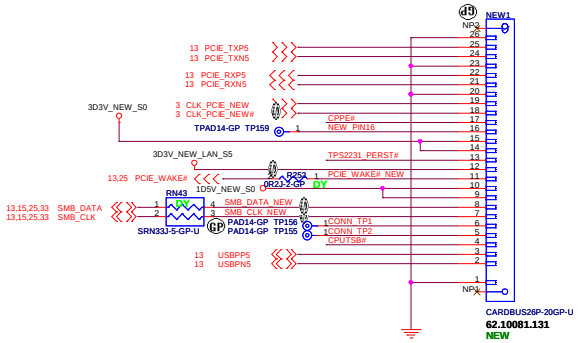
JV50

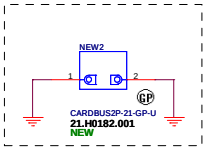
Wistron Corporation
21F., 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

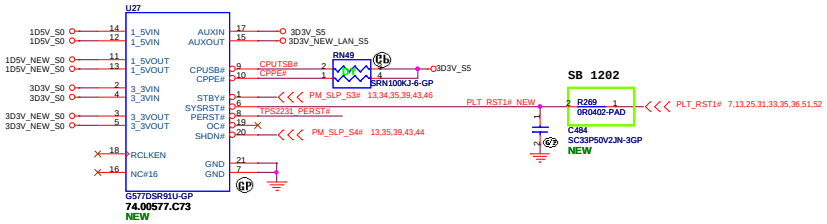
Title: *Cardreader RTS5159*

Size	Document Number	Rev
	JV50	SB

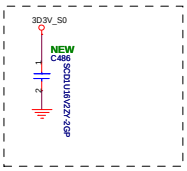
Date: Thursday, January 08, 2009 Sheet 31 of 60



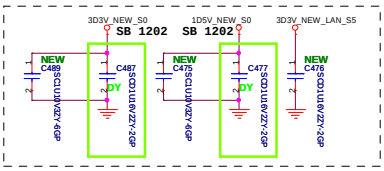




Place them Near to Chip



Place them Near to Connector



JV50

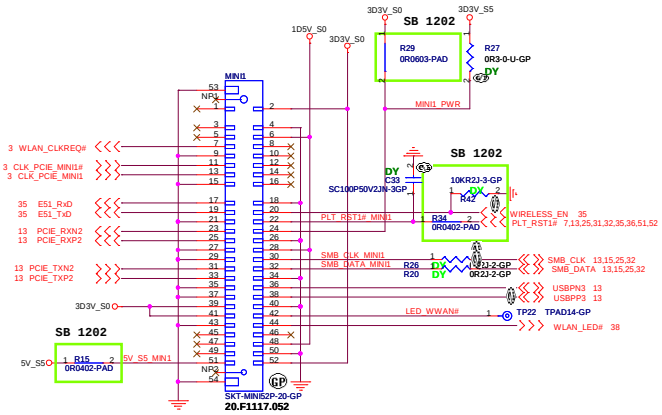
Wistron Corporation
21F., 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: **NEW CARD**

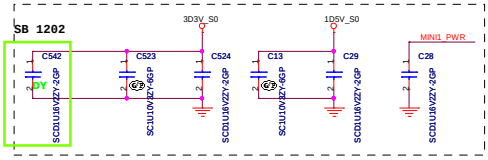
Size	Document Number	Rev
	JV50	SB

Date: Thursday, January 08, 2009 Sheet 32 of 60

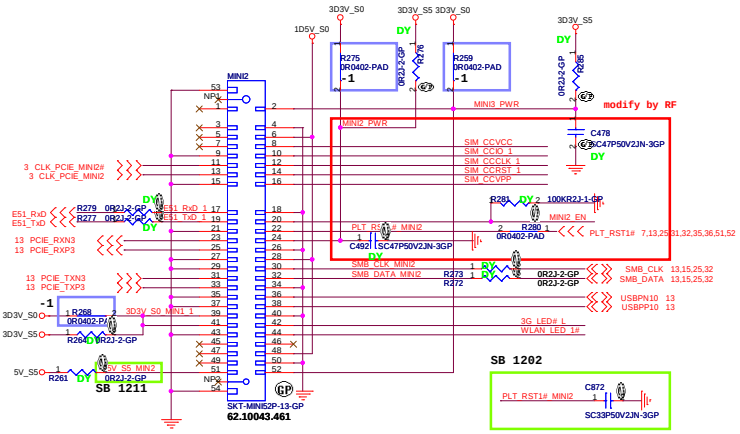
Mini Card Connector(WLAN)
Support debug-card

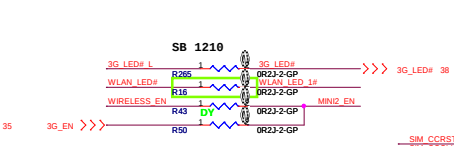


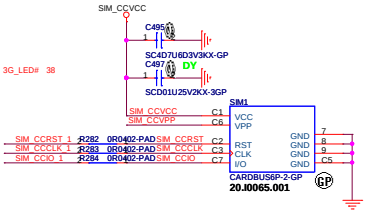
Place near MINI1



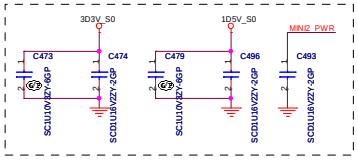
Mini Card Connector(Robson2 and 3G)





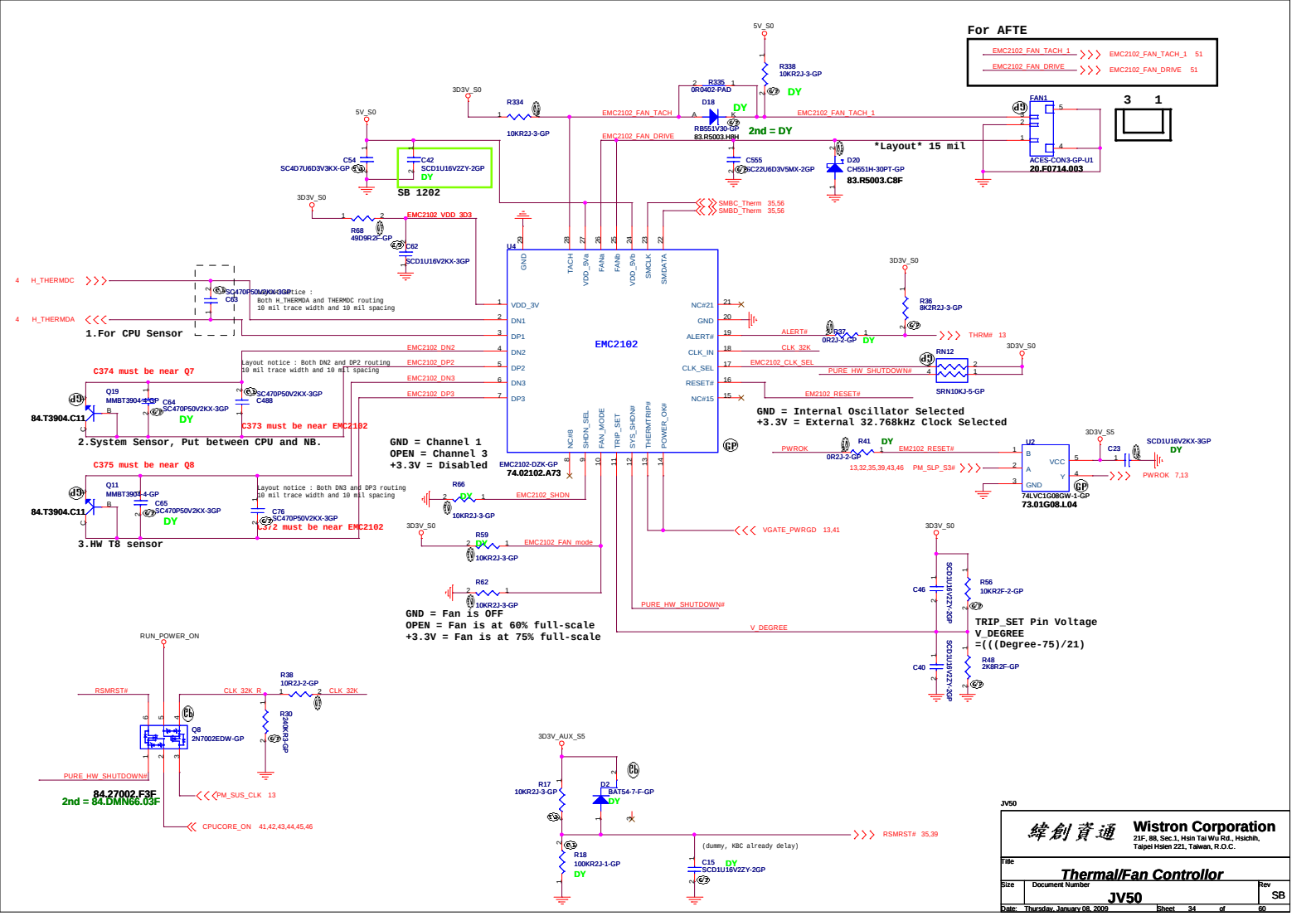


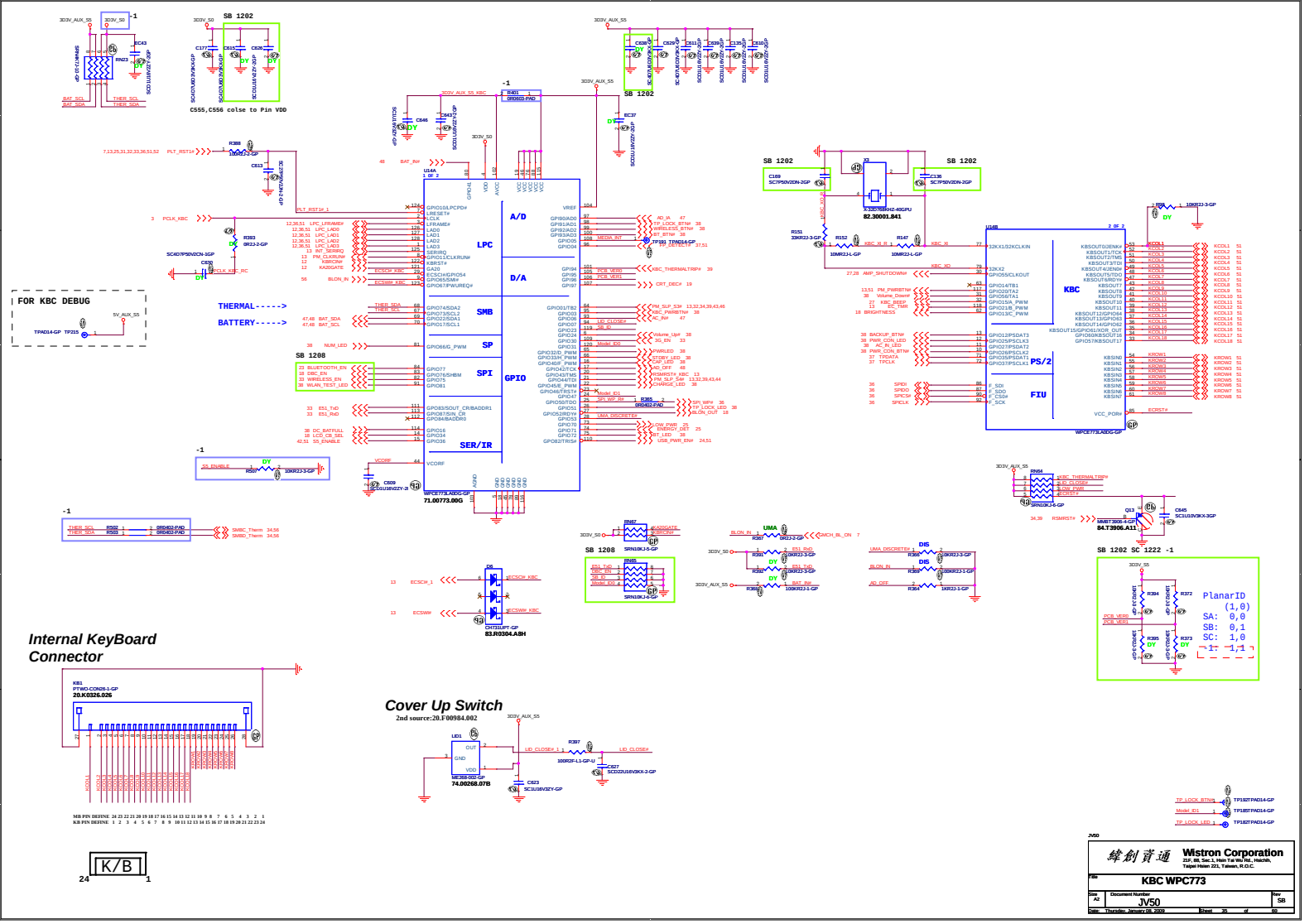
Place near MINIC2



JV50

緯創資通	Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title	MINI CARD	
Size A3	Document Number JV50	Rev SB
Date: Thursday, January 08, 2009	Sheet 33 of 60	


For AFTE
EMC2102_FAN_TACH_1
EMC2102_FAN_DRIVE
3 1
5V_S0
3D3V_S0
R338 10KR2J-3-GP
DY
R335 0R0402-PAD
D18
R8551V30-GP
83.R5003.H8H
2nd = DY
R334 10KR2J-3-GP
EMC2102_FAN_TACH
EMC2102_FAN_DRIVE
C555 SC22U6D3V5MX-2GP
D20 CH551H-30PT-GP
83.R5003.C8F
Layout 15 mil
FAN1
ACES-CON3-GP-U1
20.F0714.003
C54 SC4D7U6D3V3KX-GP
C42 SCD1U16V2ZY-2GP
SB 1202
R68 49D9R2F-GP
C62 SCD1U16V2KX-3GP
EMC2102_VDD_3D3
SMBC_Therm 35,56
SMBD_Therm 35,56
U4
EMC2102
GND
TACH
VDD_3V/A
FAN/I
FAN/I
VDD_3V/I
SMCLK
SMDATA
VDD_3V
DN1
DP1
DN2
DP2
DN3
DP3
NC#21
GND
ALERT#
CLK_IN
CLK_SEL
RESET#
NC#15
NC#8
SHDN_SEL
FAN_MODE
TRIP_SET
SYS_SHDN#
THERMTRIP#
POWER_OK#
EMC2102-DZK-GP
74.02102.A73
4 H_THERMDC
4 H_THERMDA
C63 SC470P50V2KX-3GP
Layout notice : Both H_THERMDA and THERMDC routing
10 mil trace width and 10 mil spacing
1.For CPU Sensor
EMC2102_DN2
EMC2102_DP2
EMC2102_DN3
EMC2102_DP3
Layout notice : Both DN2 and DP2 routing
10 mil trace width and 10 mil spacing
C374 must be near Q7
Q19 MMBT3904-4-GP
C64 SC470P50V2KX-3GP
C488 SC470P50V2KX-3GP
84.T3904.C11
DY
C373 must be near EMC2102
2.System Sensor, Put between CPU and NB.
C375 must be near Q8
Q11 MMBT3904-4-GP
C65 SC470P50V2KX-3GP
C76 SC470P50V2KX-3GP
84.T3904.C11
DY
372 must be near EMC2102
3.HW T8 sensor
Layout notice : Both DN3 and DP3 routing
10 mil trace width and 10 mil spacing
GND = Channel 1
OPEN = Channel 3
+3.3V = Disabled
R66 10KR2J-3-GP
EMC2102_SHDN
R59 10KR2J-3-GP
EMC2102_FAN_mode
R62 10KR2J-3-GP
GND = Fan is OFF
OPEN = Fan is at 60% full-scale
+3.3V = Fan is at 75% full-scale
R36 8K2R2J-3-GP
R37 0R2J-2-GP
DY
ALERT#
THRM# 13
CLK_32K
EMC2102_CLK_SEL
PURE_HW_SHUTDOWN#
RN12
SRN10KJ-5-GP
EM2102_RESET#
GND = Internal Oscillator Selected
+3.3V = External 32.768kHz Clock Selected
PWROK
R41 0R2J-2-GP
DY
EM2102_RESET#
13,32,35,39,43,46
PM_SLP_S3#
U2
74LVC1G08GW-1-GP
73.01G08.L04
3D3V_S5
C23
SCD1U16V2KX-3GP
DY
PWROK 7,13
VGATE_PWRGD 13,41
PURE_HW_SHUTDOWN#
V_DEGREE
C46 SCD1U16V2ZY-2GP
R56 10KR2F-2-GP
C40 SCD1U16V2ZY-2GP
R48 2K8R2F-GP
TRIP_SET Pin Voltage
V_DEGREE
=(((Degree-75)/21)
RUN_POWER_ON
RSMRST#
CLK_32K_R
R38 10R2J-2-GP
CLK_32K
R30 20KR3-GP
Q8 2N7002EDW-GP
PURE_HW_SHUTDOWN#
84.27002.F3F
2nd = 84.DMN66.03F
PM_SUS_CLK 13
CPUCORE_ON 41,42,43,44,45,46
3D3V_AUX_S5
R17 10KR2J-3-GP
D2 BAT54-7-F-GP
DY
R18 100KR2J-1-GP
DY
C15 SCD1U16V2ZY-2GP
DY
(dummy, KBC already delay)
RSMRST# 35,39
JV50
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.
Title
Thermal/Fan Controllor
Size
Document Number
JV50
Rev
SB
Date: Thursday, January 08, 2009
Sheet 34 of 60



Internal KeyBoard Connector

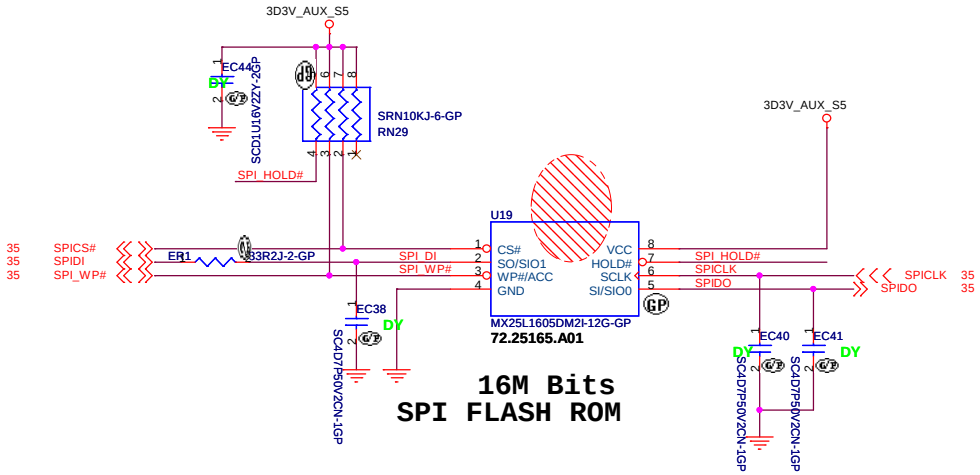
Cover Up Switch

2nd source:20.F00984.002

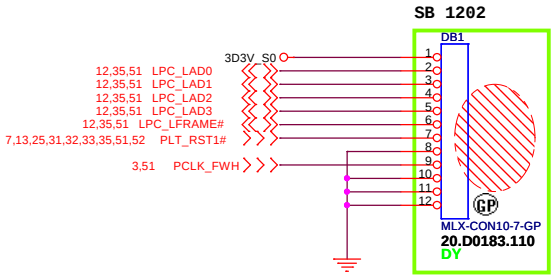
K/B

24 1

Wistron Corporation	21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.
Title: KBC WPC773	
Size: A2	Document Number: JV50
Rev: SB	
Date: Thursday, January 08, 2009	Sheet 35 of 60



GOLDEN FINGER FOR DEBUG BOARD



JV50

緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title	***BIOS***	
Size	Document Number **JV50**	Rev SB
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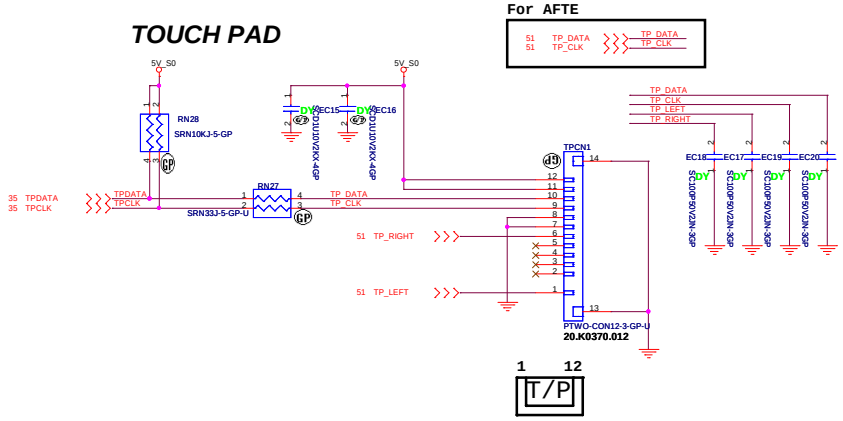
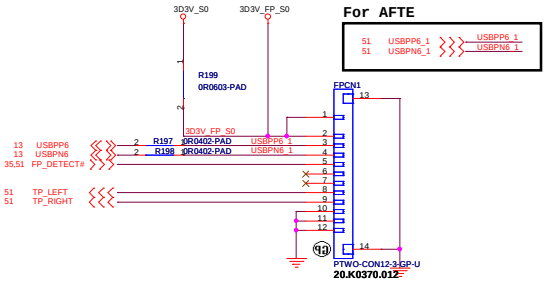
TOUCH PAD

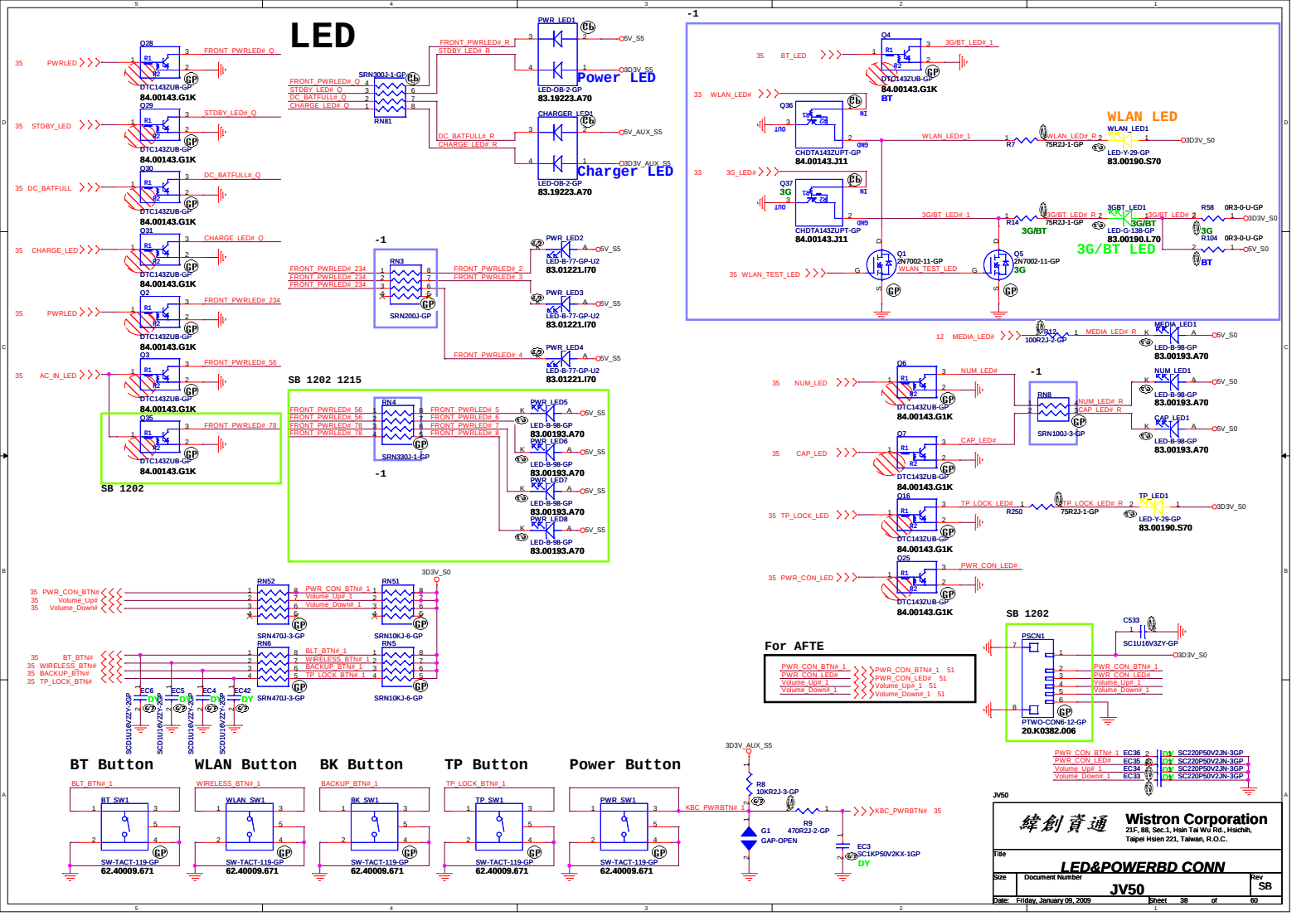


Finger printer



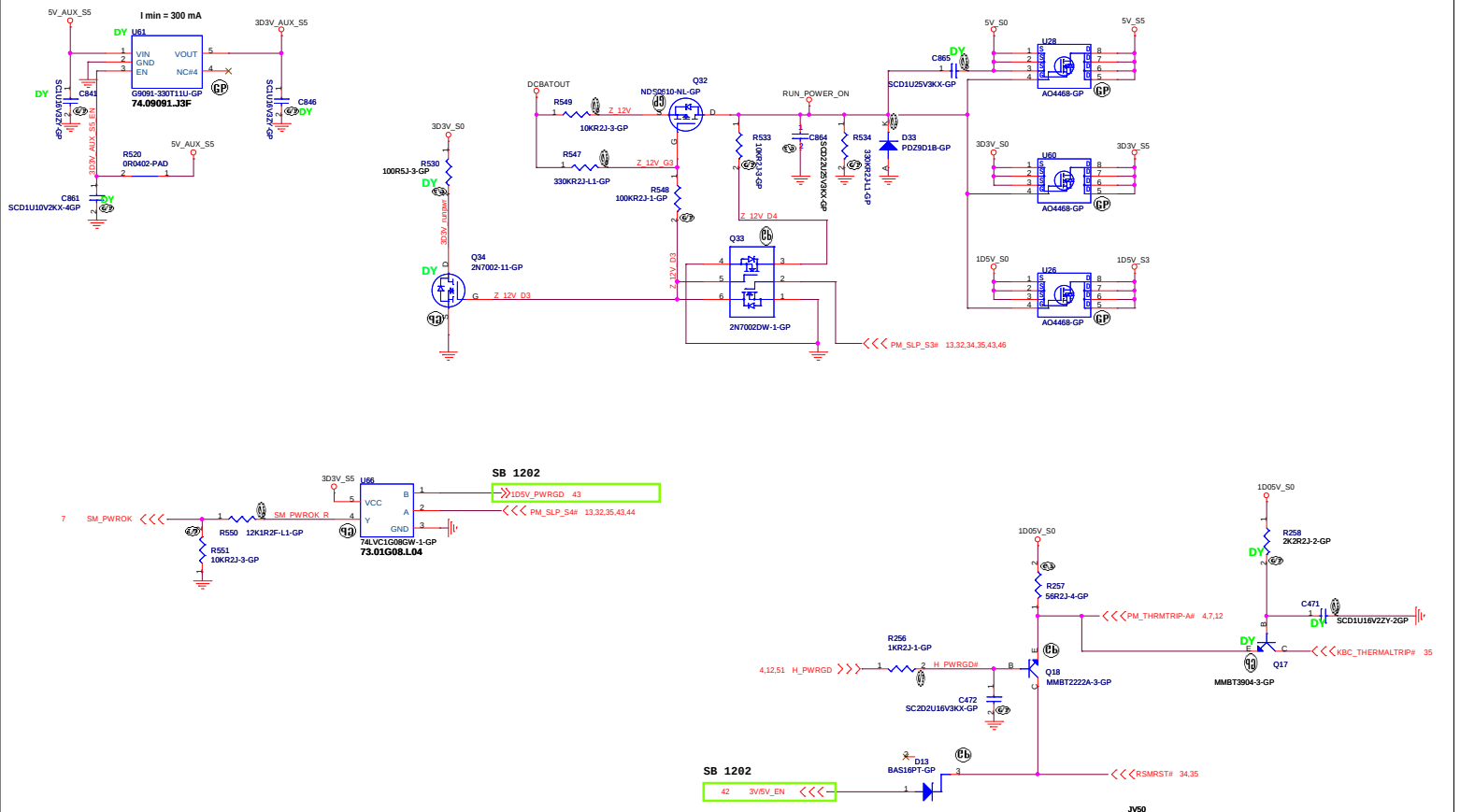
JV50

緯創資通	**Wistron Corporation** 21F., 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.
Title	*Touch PAD and FP*
Size	Document Number: JV50 — Rev: SB
Date: Thursday, January 08, 2009	Sheet 37 of 60


LED
Power LED
Charger LED
WLAN LED
3G/BT LED
SB 1202
For AFTE
BT Button
WLAN Button
BK Button
TP Button
Power Button
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.
LED&POWERBD CONN
JV50
Date: Friday, January 09, 2009
Sheet 38 of 60

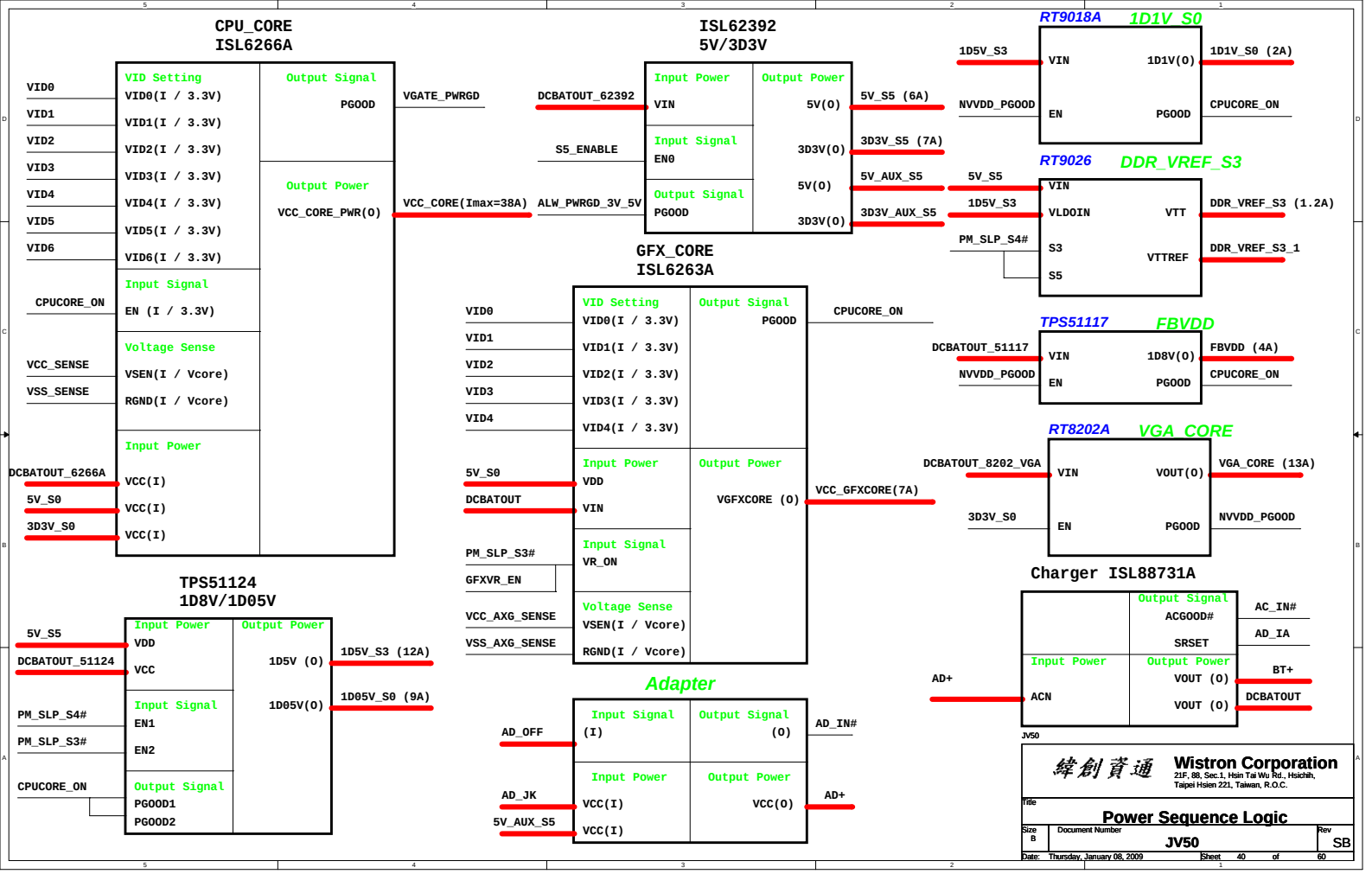
Aux Power 3D3V_AUX_S5

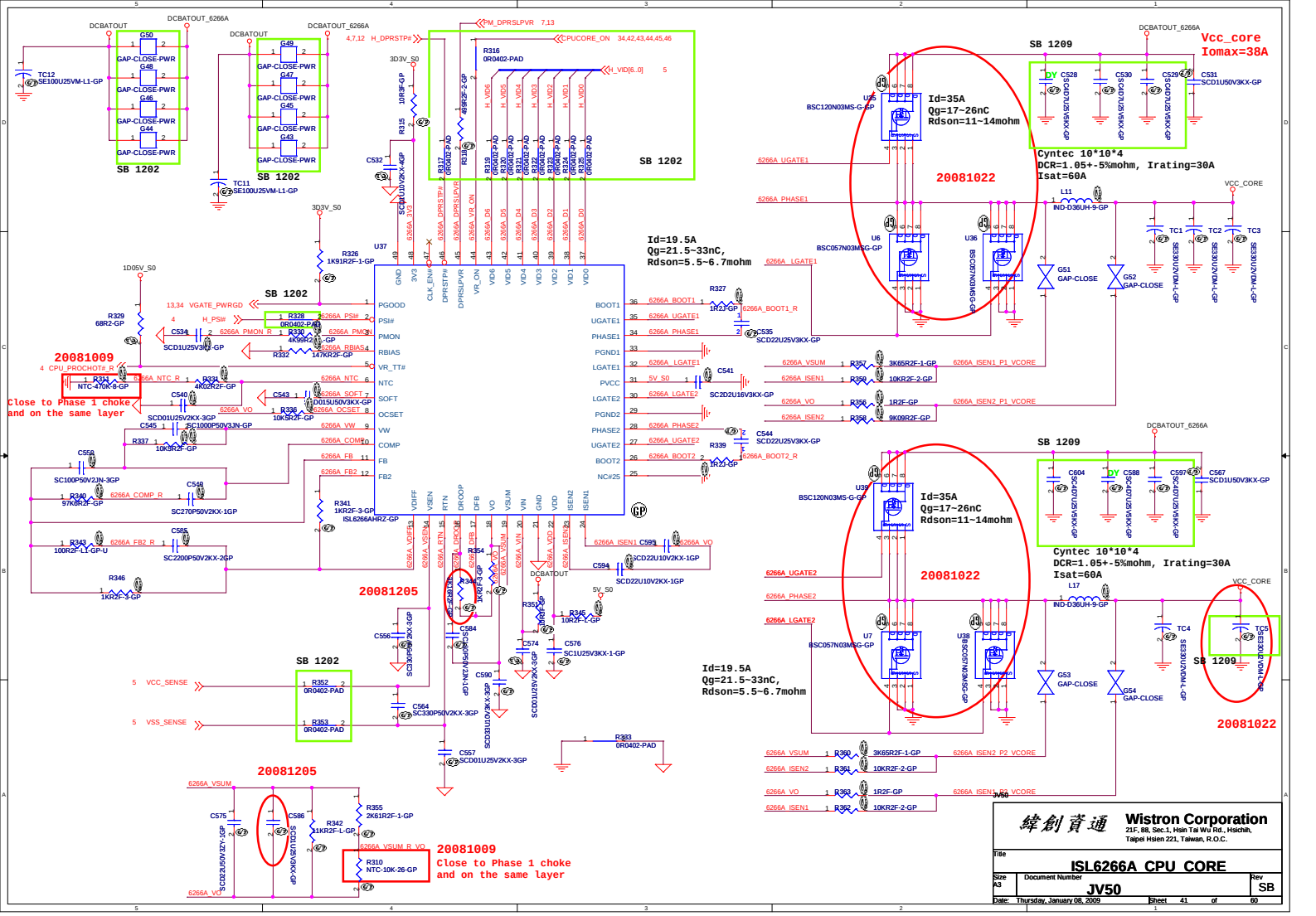
Run Power



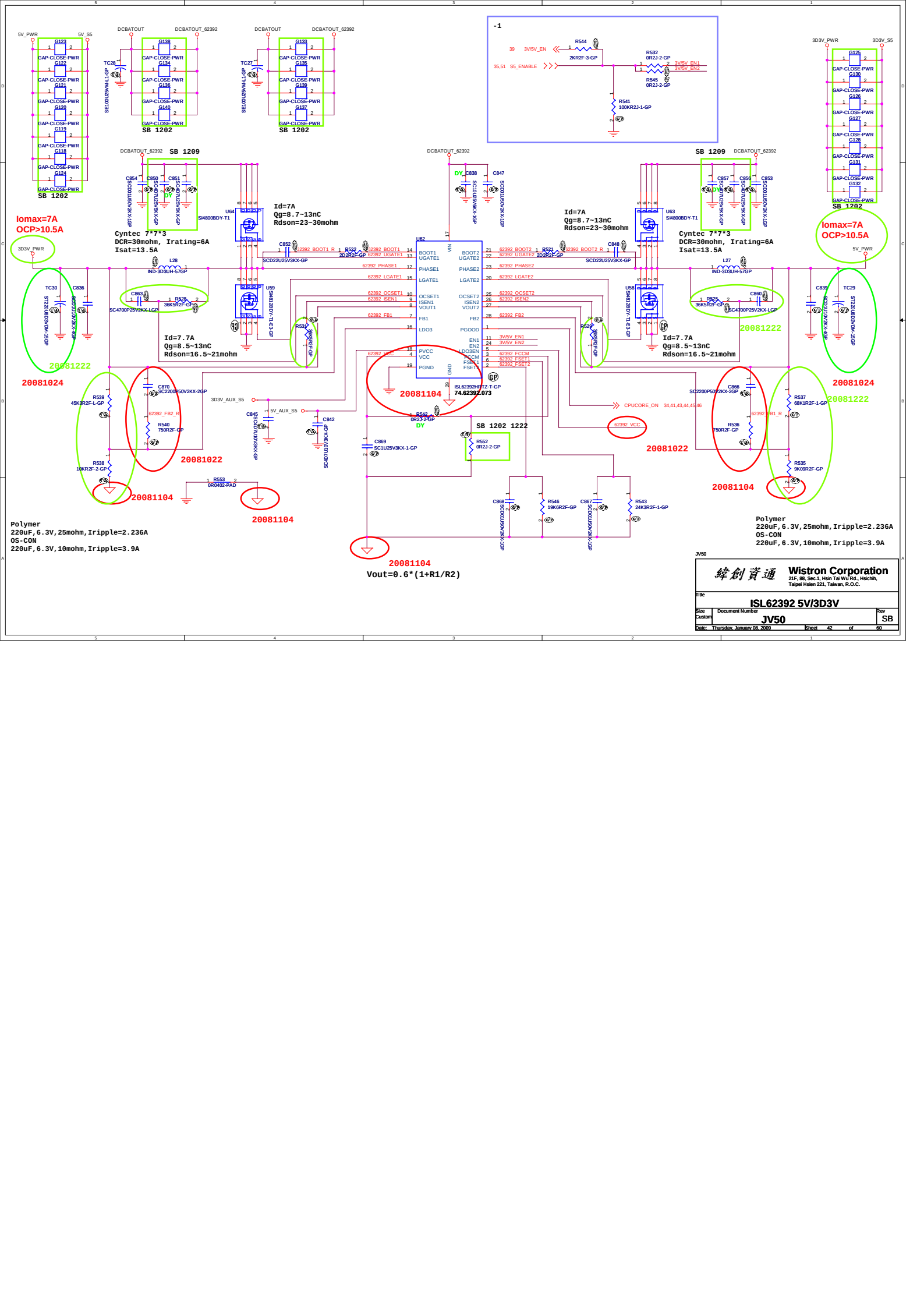
JV50

緯創資通 Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.		
Title: RUN POWER and 3D3V_AUX_S5		
Size	Document Number: JV50	Rev: SB
Date: Thursday, January 08, 2009	Sheet 39 of 60	


CPU_CORE
ISL6266A
VID Setting
VID0(I / 3.3V)
VID1(I / 3.3V)
VID2(I / 3.3V)
VID3(I / 3.3V)
VID4(I / 3.3V)
VID5(I / 3.3V)
VID6(I / 3.3V)
Input Signal
EN (I / 3.3V)
Voltage Sense
VSEN(I / Vcore)
RGND(I / Vcore)
Input Power
VCC(I)
VCC(I)
VCC(I)
Output Signal
PGOOD
Output Power
VCC_CORE_PWR(O)
VID0
VID1
VID2
VID3
VID4
VID5
VID6
CPUCORE_ON
VCC_SENSE
VSS_SENSE
DCBATOUT_6266A
5V_S0
3D3V_S0
VGATE_PWRGD
VCC_CORE(Imax=38A)
ISL62392
5V/3D3V
Input Power
VIN
Input Signal
EN0
Output Signal
PGOOD
Output Power
5V(O)
3D3V(O)
5V(O)
3D3V(O)
DCBATOUT_62392
S5_ENABLE
ALW_PWRGD_3V_5V
5V_S5 (6A)
3D3V_S5 (7A)
5V_AUX_S5
3D3V_AUX_S5
RT9018A
1D1V_S0
VIN
EN
1D1V(O)
PGOOD
1D5V_S3
NVVDD_PGOOD
1D1V_S0 (2A)
CPUCORE_ON
RT9026
DDR_VREF_S3
VIN
VLDOIN
S3
S5
VTT
VTTREF
5V_S5
1D5V_S3
PM_SLP_S4#
DDR_VREF_S3 (1.2A)
DDR_VREF_S3_1
GFX_CORE
ISL6263A
VID Setting
VID0(I / 3.3V)
VID1(I / 3.3V)
VID2(I / 3.3V)
VID3(I / 3.3V)
VID4(I / 3.3V)
Input Power
VDD
VIN
Input Signal
VR_ON
Voltage Sense
VSEN(I / Vcore)
RGND(I / Vcore)
Output Signal
PGOOD
Output Power
VGFXCORE (O)
VID0
VID1
VID2
VID3
VID4
5V_S0
DCBATOUT
PM_SLP_S3#
GFXVR_EN
VCC_AXG_SENSE
VSS_AXG_SENSE
CPUCORE_ON
VCC_GFXCORE(7A)
TPS51117
FBVDD
VIN
EN
1D8V(O)
PGOOD
DCBATOUT_51117
NVVDD_PGOOD
FBVDD (4A)
CPUCORE_ON
RT8202A
VGA_CORE
VIN
EN
VOUT(O)
PGOOD
DCBATOUT_8202_VGA
3D3V_S0
VGA_CORE (13A)
NVVDD_PGOOD
TPS51124
1D8V/1D05V
Input Power
VDD
VCC
Input Signal
EN1
EN2
Output Signal
PGOOD1
PGOOD2
Output Power
1D5V (O)
1D05V(O)
5V_S5
DCBATOUT_51124
PM_SLP_S4#
PM_SLP_S3#
CPUCORE_ON
1D5V_S3 (12A)
1D05V_S0 (9A)
Adapter
Input Signal
(I)
Input Power
VCC(I)
VCC(I)
Output Signal
(O)
Output Power
VCC(O)
AD_OFF
AD_JK
5V_AUX_S5
AD_IN#
AD+
Charger ISL88731A
Output Signal
ACGOOD#
SRSET
Input Power
ACN
Output Power
VOUT (O)
VOUT (O)
AD+
AC_IN#
AD_IA
BT+
DCBATOUT
JV50
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.
Title
Power Sequence Logic
Size
B
Document Number
JV50
Rev
SB
Date: Thursday, January 08, 2009
Sheet 40 of 60



Wistron Corporation	21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.
Title	ISL6266A CPU CORE
Size A3	Document Number JV50 Rev SB
Date: Thursday, January 08, 2009	Sheet 41 of 60


-1
R544 2KR2F-3-GP
R532 0R2J-2-GP
R545 0R2J-2-GP
R541 100KR2J-1-GP
39 3V/5V_EN
35,51 S5_ENABLE
3V/5V_EN1
3V/5V_EN2
SB 1202
SB 1209
DCBATOUT
DCBATOUT_62392
5V_PWR
5V_S5
3D3V_PWR
3D3V_S5
lomax=7A
OCP>10.5A
Cyntec 7*7*3
DCR=30mohm, Irating=6A
Isat=13.5A
Id=7A
Qg=8.7~13nC
Rdson=23~30mohm
Id=7.7A
Qg=8.5~13nC
Rdson=16.5~21mohm
U62
ISL62392HRTZ-T-GP
74.62392.073
20081104
20081222
20081024
20081022
20081104
SB 1202 1222
DY
CPUCORE_ON 34,41,43,44,45,46
62392_VCC
Vout=0.6*(1+R1/R2)
Polymer
220uF,6.3V,25mohm,Iripple=2.236A
OS-CON
220uF,6.3V,10mohm,Iripple=3.9A
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.
JV50
ISL62392 5V/3D3V
Size Custom
Document Number
Rev SB
Date: Thursday, January 08, 2009
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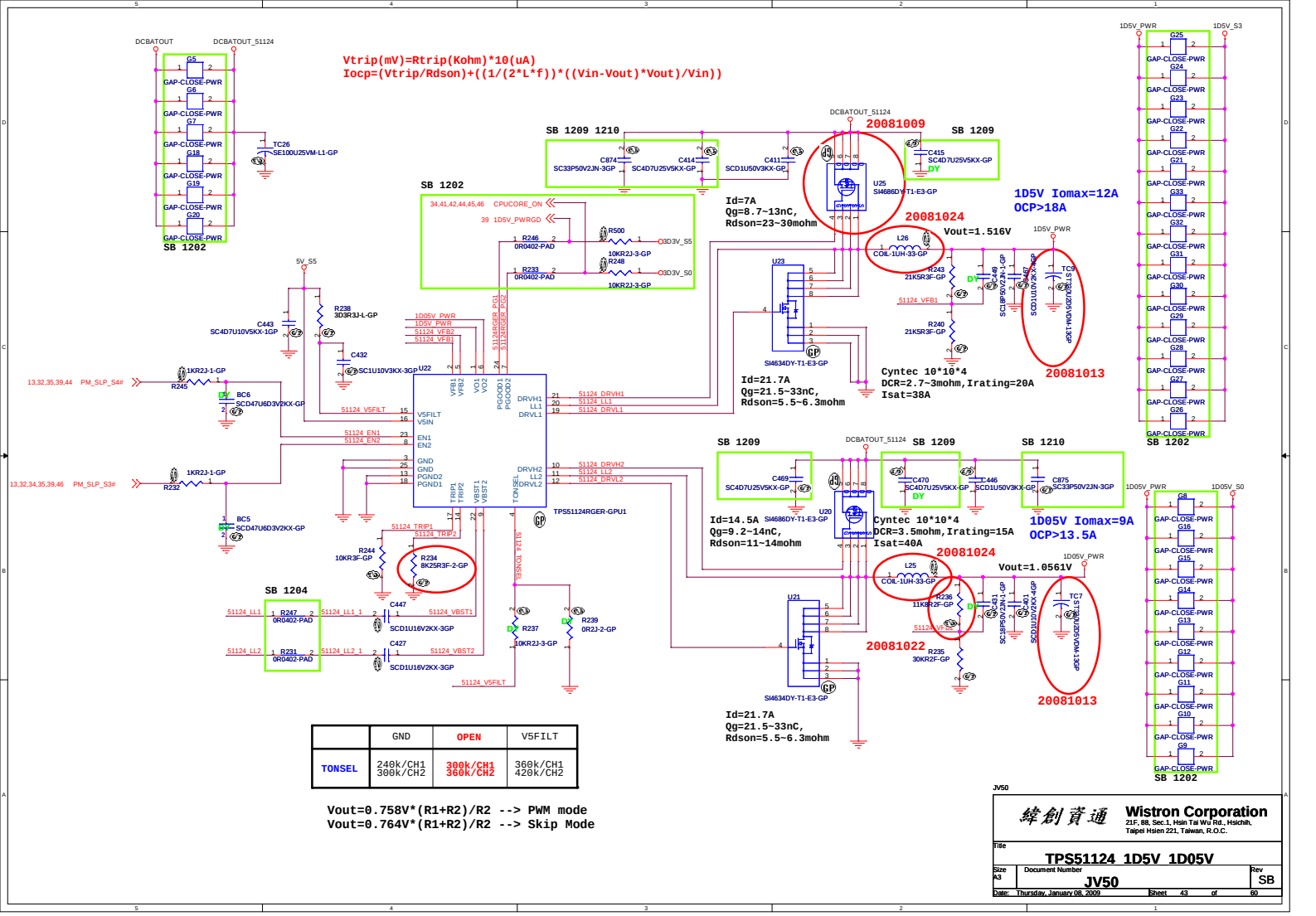
Vtrip(mV)=Rtrip(Kohm)*10(uA)
Iocp=(Vtrip/Rdson)+((1/(2*L*f))*((Vin-Vout)*Vout)/Vin))
SB 1202
SB 1209 1210
SB 1209
SB 1210
SB 1204
20081009
20081024
20081022
20081013
1D5V Iomax=12A
OCP>18A
1D5V Iomax=9A
OCP>13.5A
Vout=1.516V
Vout=1.0561V
Id=7A
Qg=8.7~13nC,
Rdson=23~30mohm
Id=21.7A
Qg=21.5~33nC,
Rdson=5.5~6.3mohm
Id=14.5A
Qg=9.2~14nC,
Rdson=11~14mohm
Id=21.7A
Qg=21.5~33nC,
Rdson=5.5~6.3mohm
Cyntec 10*10*4
DCR=2.7~3mohm,Irating=20A
Isat=38A
Cyntec 10*10*4
DCR=3.5mohm,Irating=15A
Isat=40A
TPS51124RGER-GPU1
Vout=0.758V*(R1+R2)/R2 --> PWM mode
Vout=0.764V*(R1+R2)/R2 --> Skip Mode
TONSEL
GND
OPEN
V5FILT
240k/CH1
300k/CH2
300k/CH1
360k/CH2
360k/CH1
420k/CH2
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.
TPS51124 1D5V 1D05V
JV50
SB
Thursday, January 08, 2009
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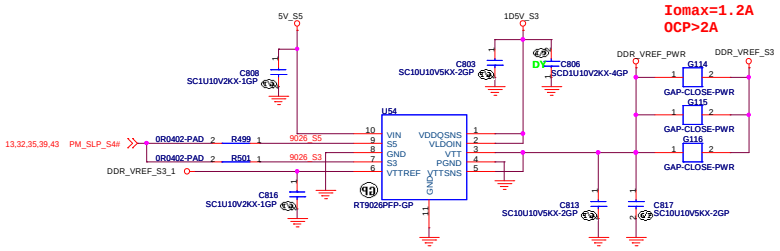
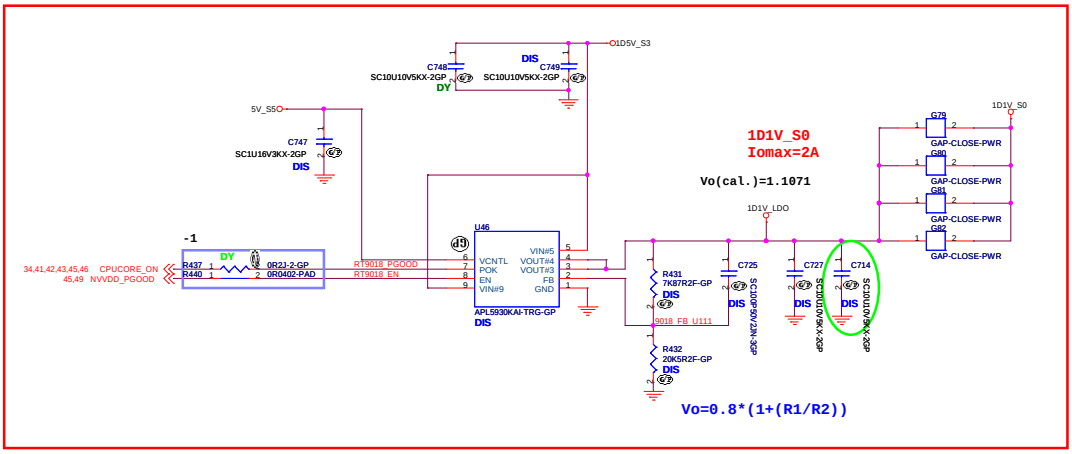
60

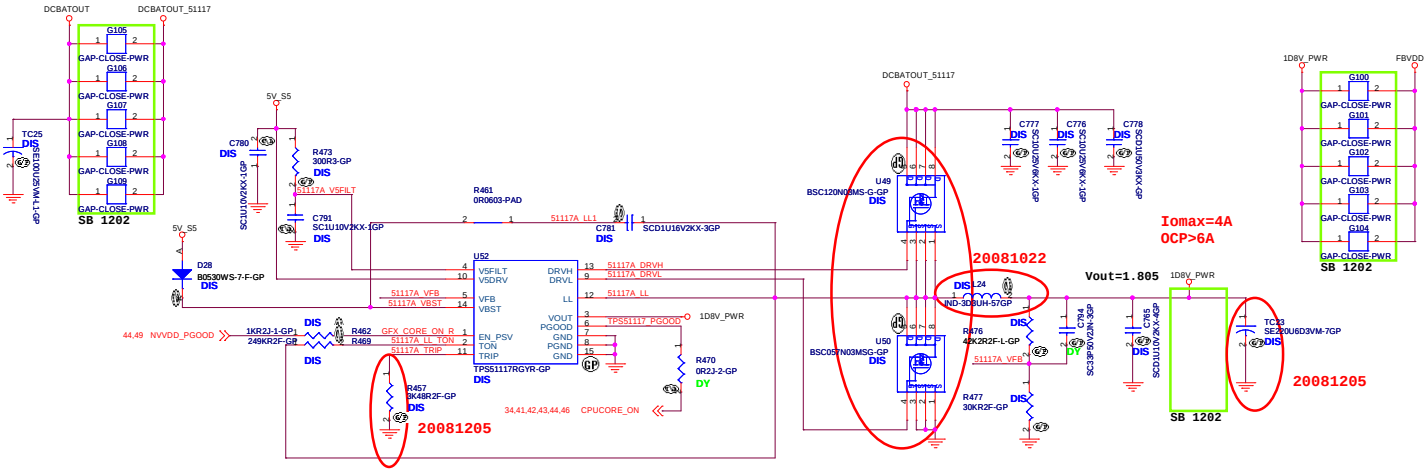




20090106

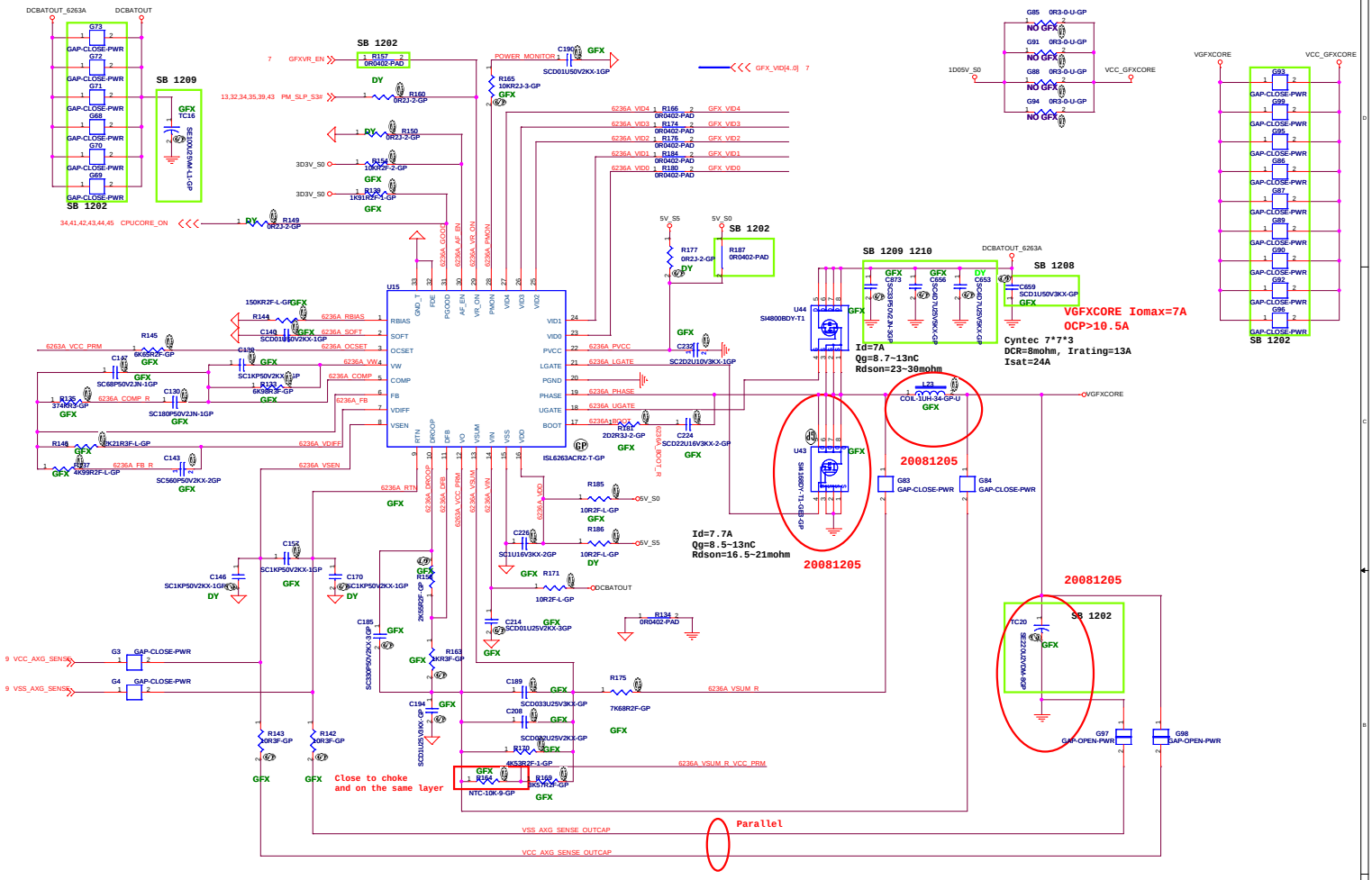
JV50

緯創資通 Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.		
Title: 0D75V/1D1V		
Size: A3	Document Number: JV50	Rev: SB
Date: Thursday, January 08, 2009	Sheet 44 of 60	



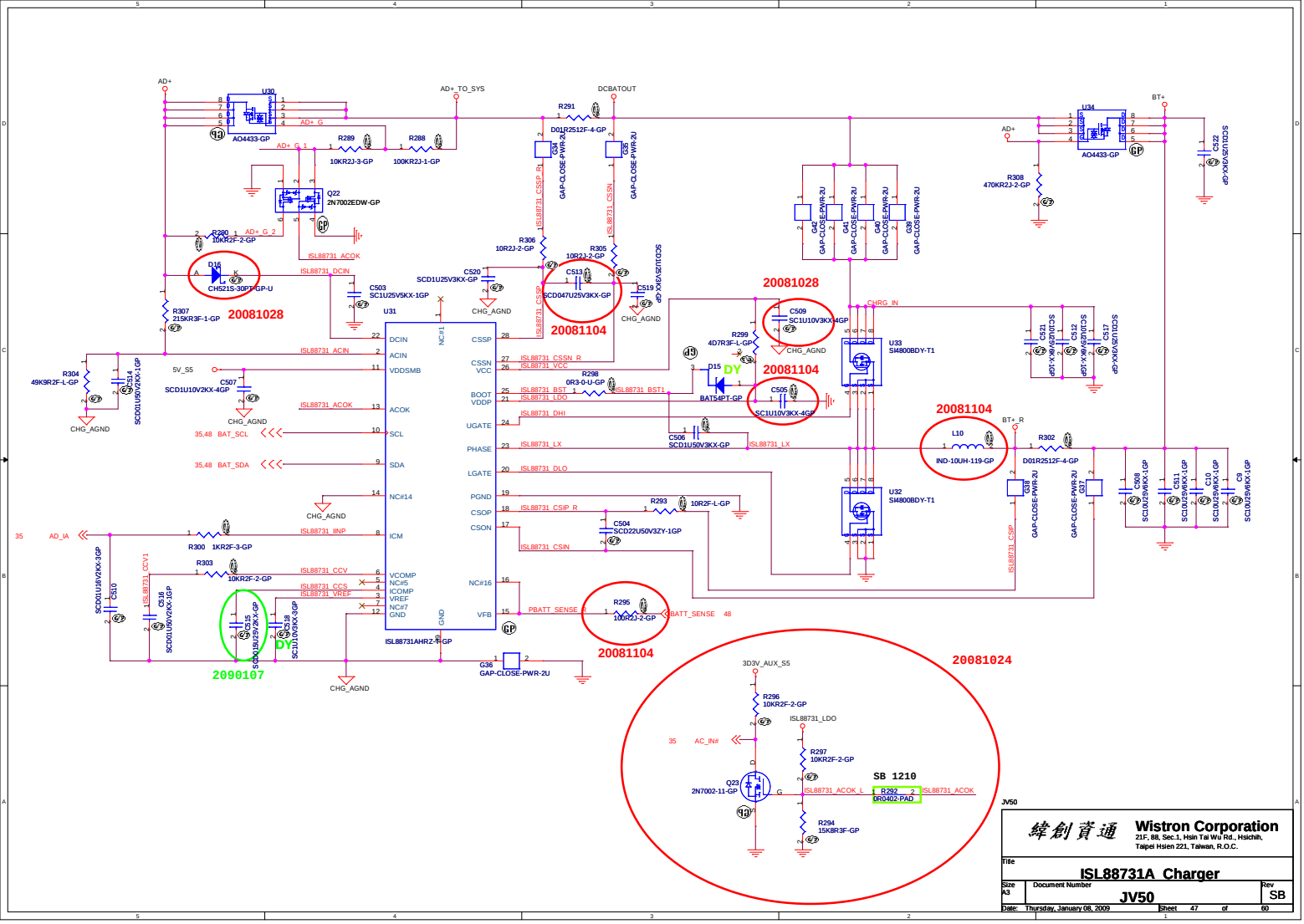
JV50

緯創資通 Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.		
Title: TPS51117 1D8V		
Size: A3	Document Number: JV50	Rev: SB
Date: Thursday, January 08, 2009	Sheet 45 of 60	



JV50

緯創資通	Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title	ISL6263A GFX CORE	
Size: Custom	Document Number: JV50	Rev: SB
Date: Thursday, January 08, 2009	Sheet 46 of 60	

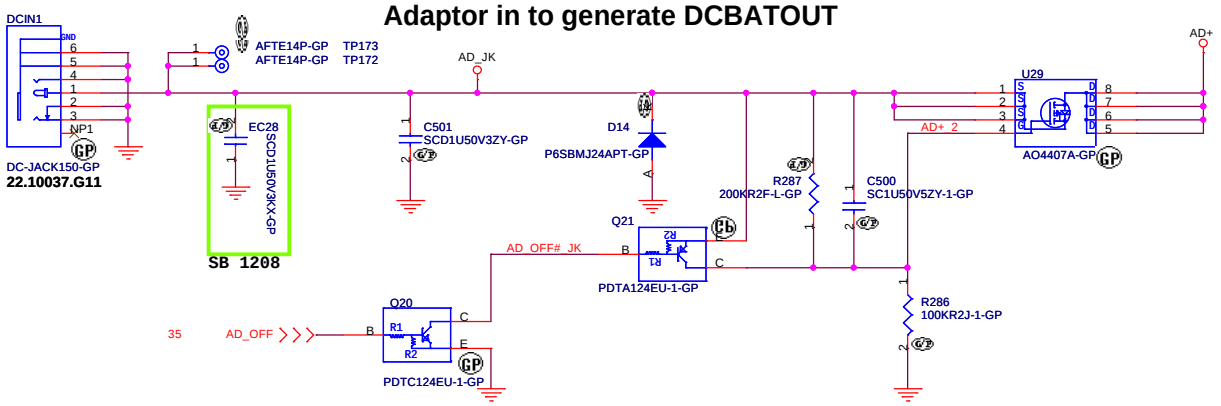


緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

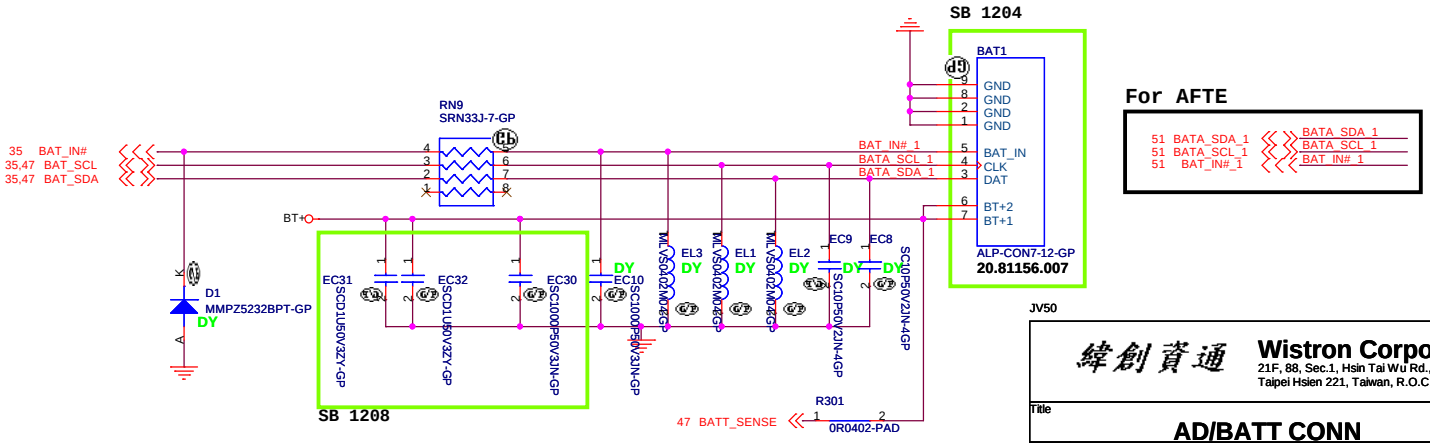
Title: ISL88731A Charger

Size	Document Number	Rev
A3	JV50	SB

Date: Thursday, January 08, 2009 Sheet 47 of 60



BATTERY CONNECTOR



For AFTE

51 BATA_SDA_1 — BATA_SDA_1
51 BATA_SCL_1 — BATA_SCL_1
51 BAT_IN#_1 — BAT_IN#_1

JV50

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: **AD/BATT CONN**

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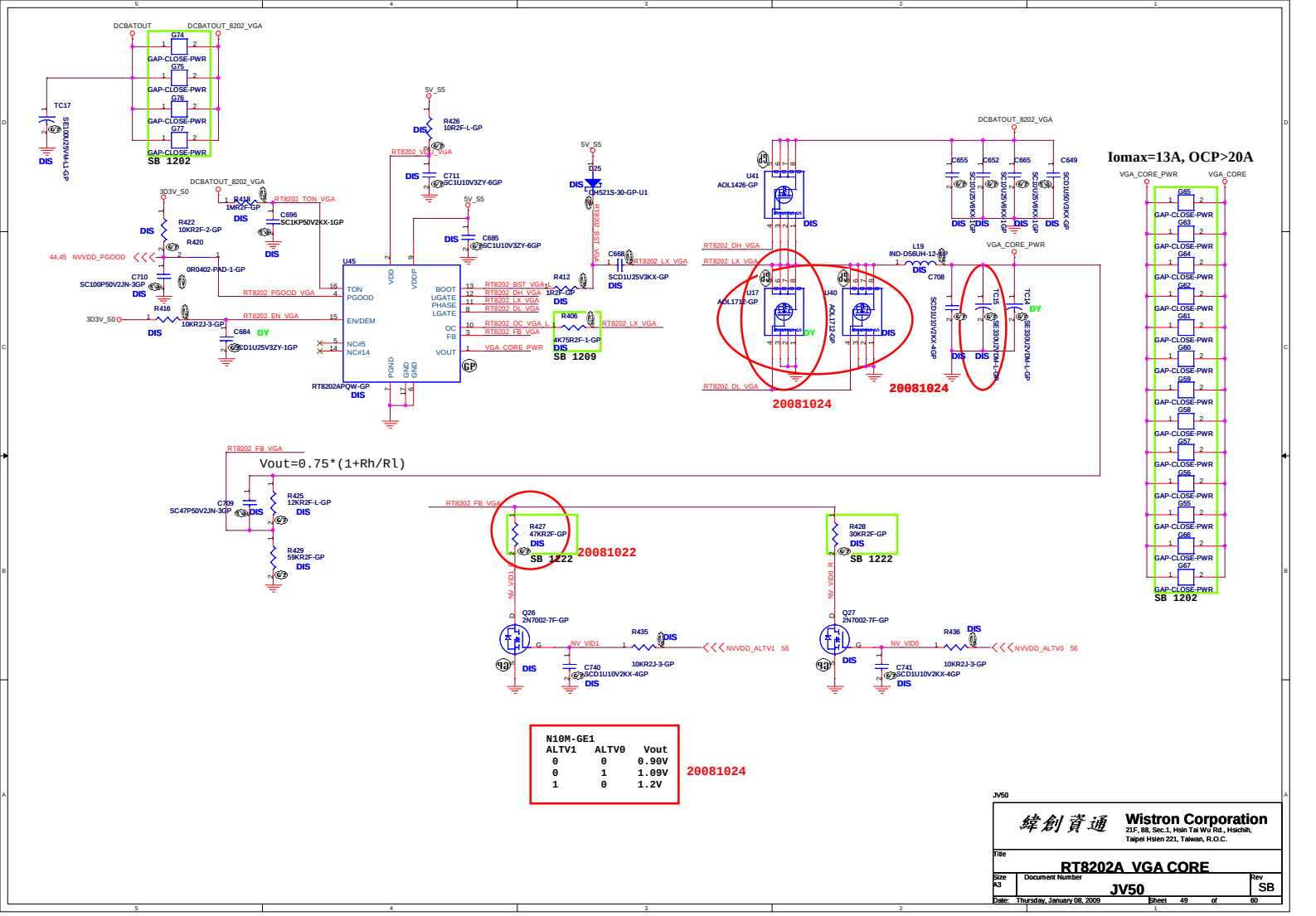
	JV50	SB

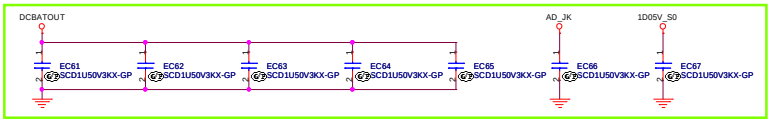
Date: Thursday, January 08, 2009 Sheet 48 of 60



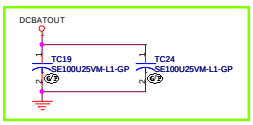
JV50

緯創資通	Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title	RT8202A_VGA CORE	
Size A3	Document Number JV50	Rev SB
Date: Thursday, January 08, 2009	Sheet 49 of 60	

SB 1208

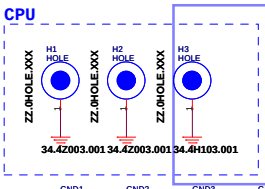


SB 1209

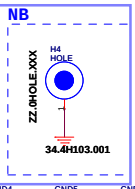


-1 0109

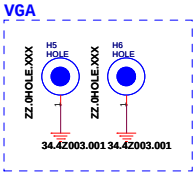
CPU



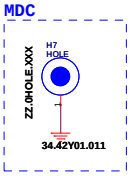
NB



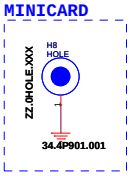
VGA

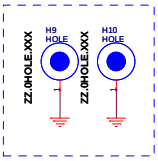


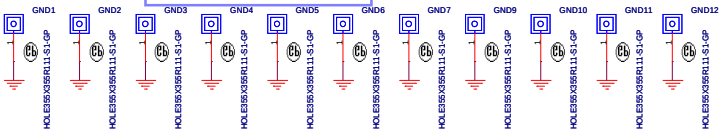
MDC

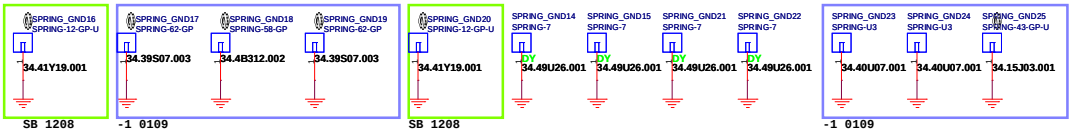


MINICARD









JV50

緯創資通 **Wistron Corporation**
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Taipei Hsien 221, Taiwan, R.O.C.

Title: ***EMI/Spring/Boss***

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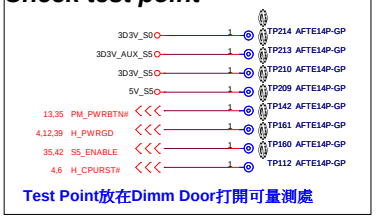
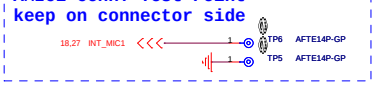
Check test point

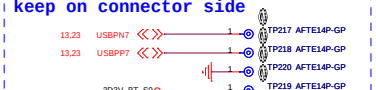


Test Point放在Dimm Door打開可量測處

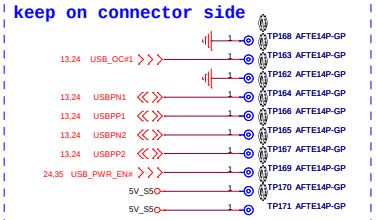
AMIC1 Conn. Test Point keep on connector side



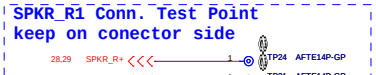
BT1 Conn. Test Point keep on connector side



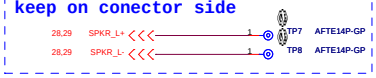
USBCN1 Conn. Test Point keep on connector side



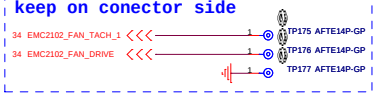
SPKR_R1 Conn. Test Point keep on conector side



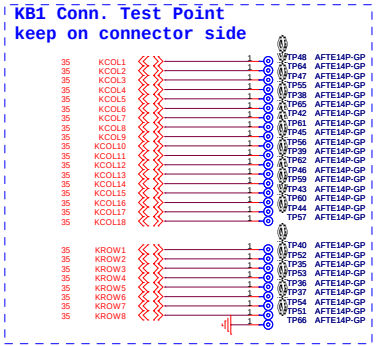
SPKR_L1 Conn. Test Point keep on conector side



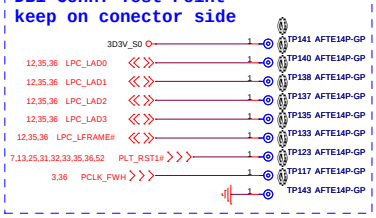
FAN1 Conn. Test Point keep on conector side



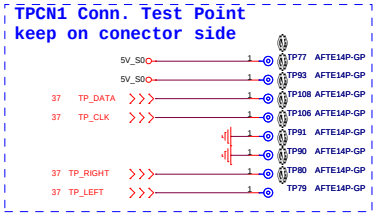
KB1 Conn. Test Point keep on connector side



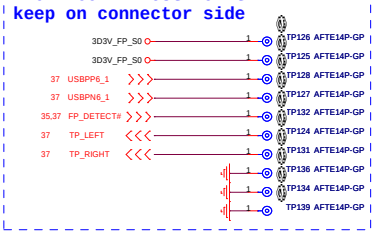
DB1 Conn. Test Point keep on conector side



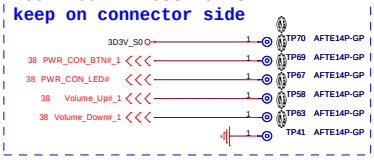
TPCN1 Conn. Test Point keep on conector side



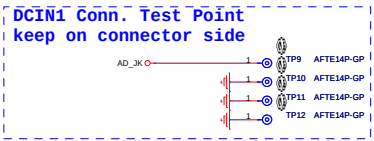
FPCN1 Conn. Test Point keep on connector side



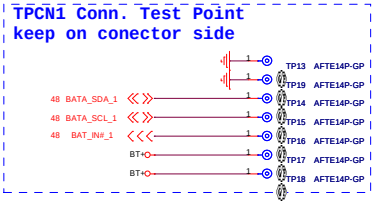
PSCN1 Conn. Test Point keep on connector side



DCIN1 Conn. Test Point keep on connector side



TPCN1 Conn. Test Point keep on conector side



JV50

緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: **AFTE TP**

Size	Document Number	Rev
A3	JV50	SB

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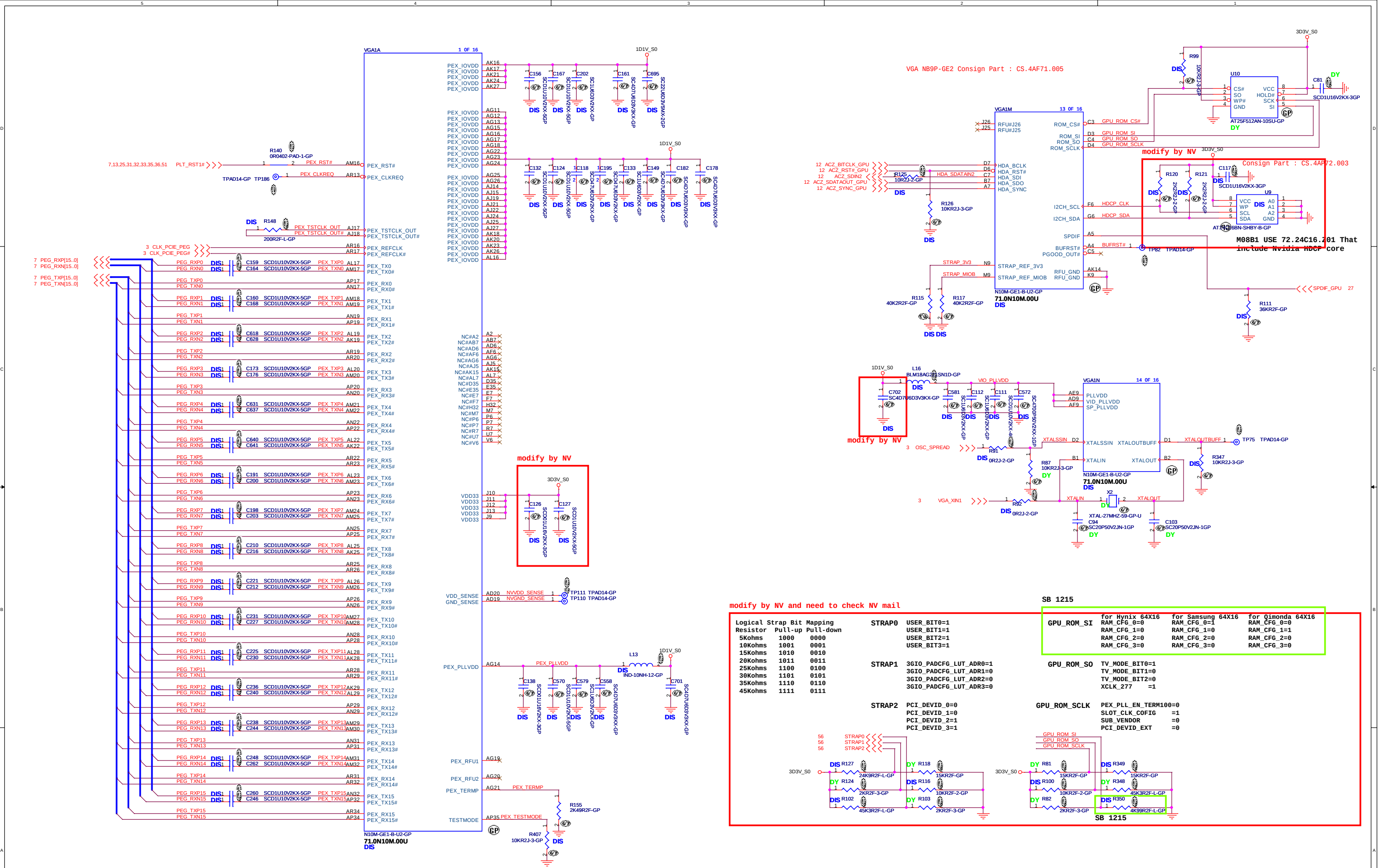

JV50

緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.

Title: **N10M(1/6)_PEG**

Size: A2 | Document Number: JV50 | Rev: SB

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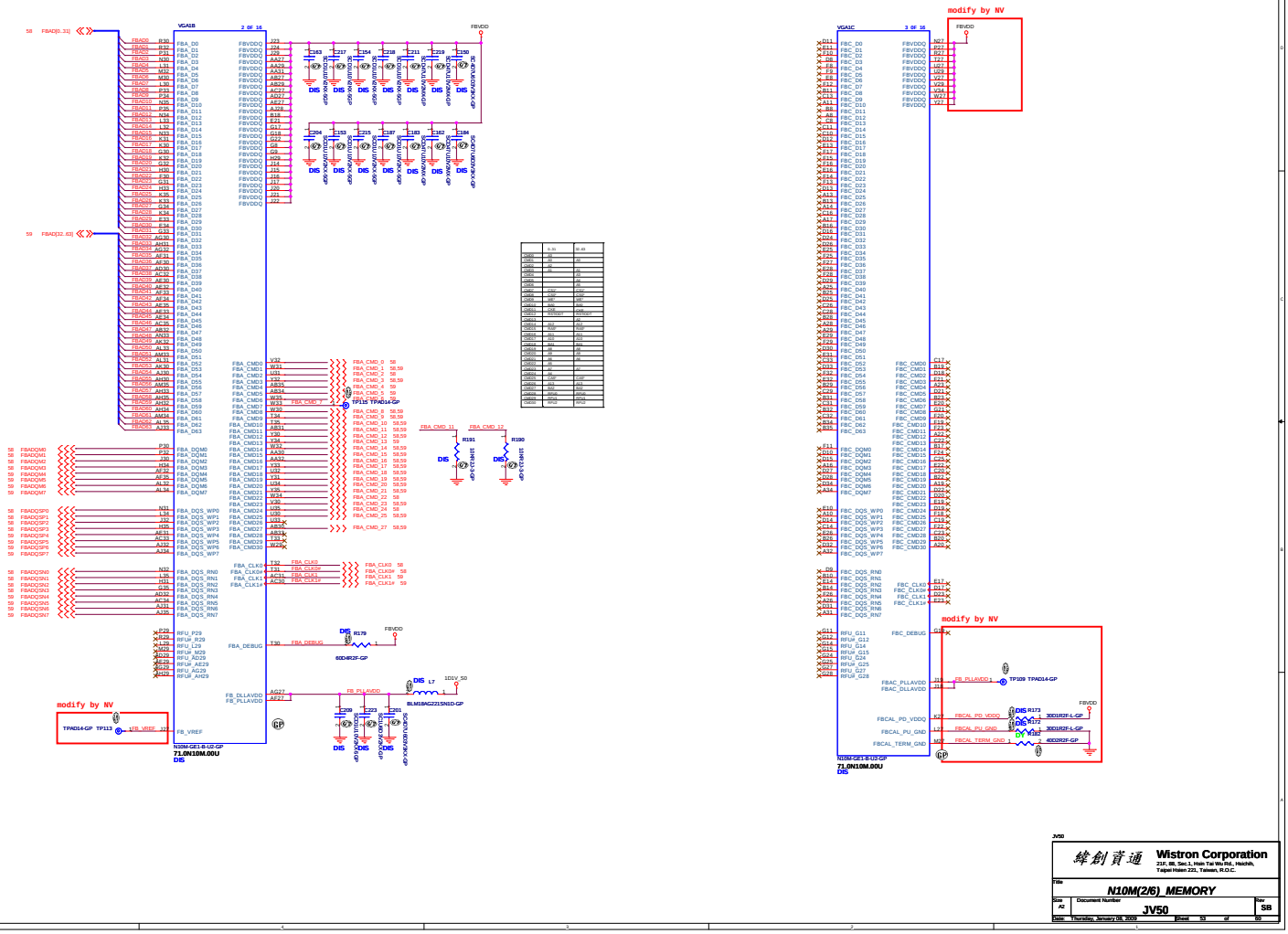

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: N10M(2/6) MEMORY

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A2	JV50	SB

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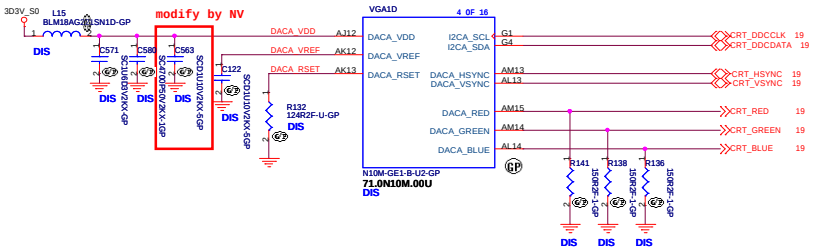
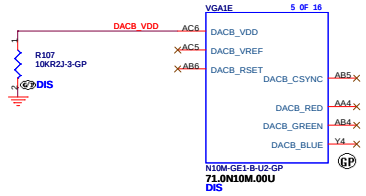
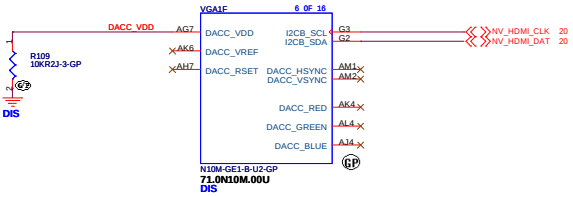
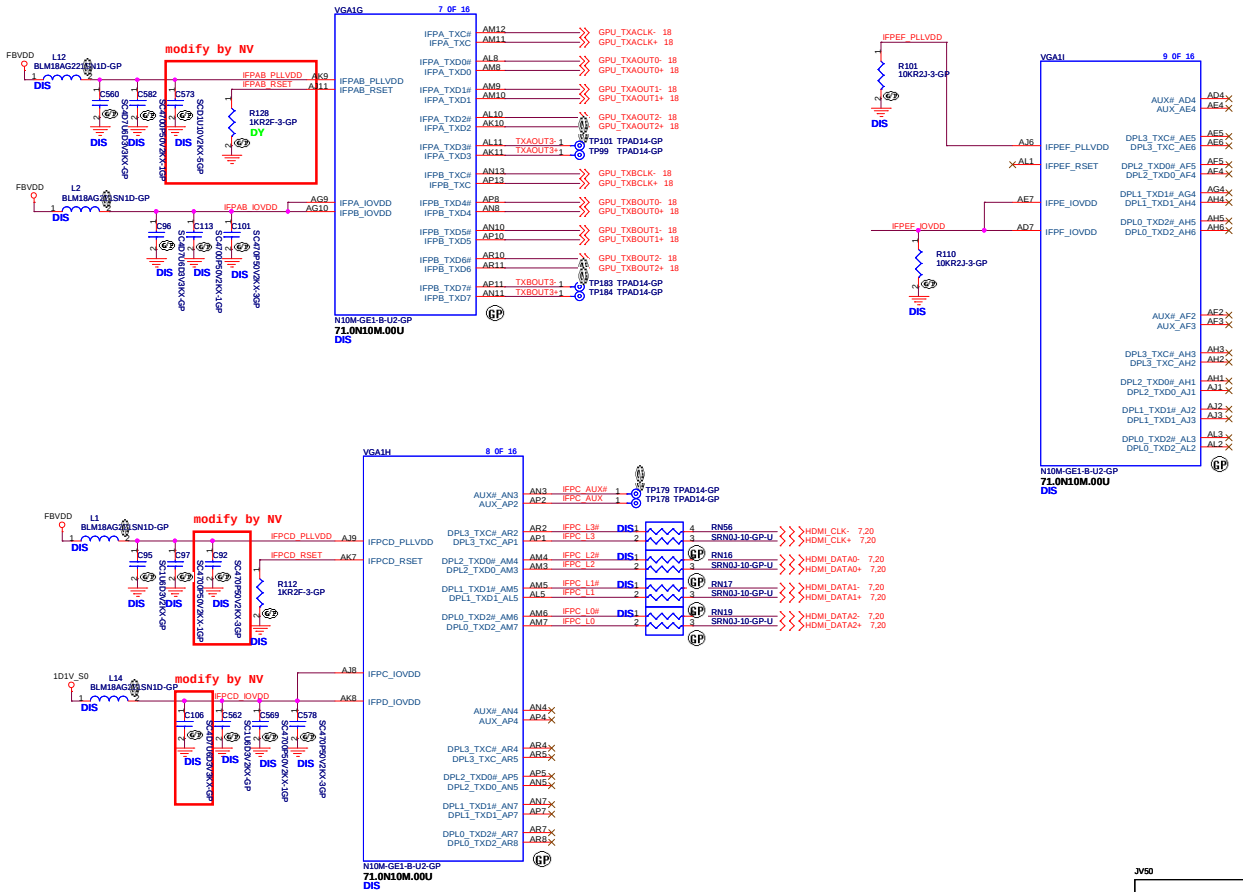






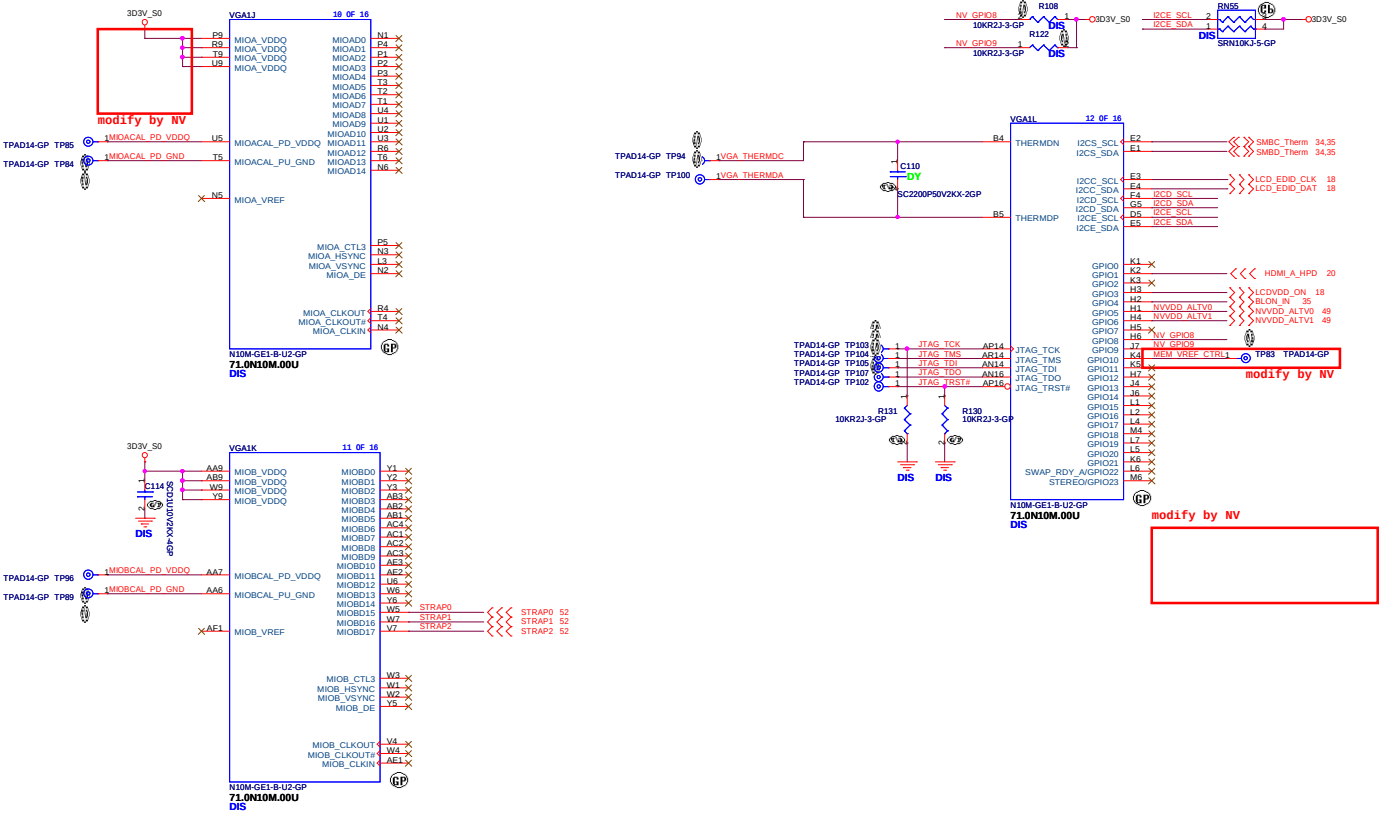
JV50

緯創資通	**Wistron Corporation** 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title	***N10M(3/6) DAC***	
Size: A3	Document Number: **JV50**	Rev: SB
Date: Thursday, January 08, 2009	Sheet 54 of 60	



JV50

緯創資通 Wistron Corporation 21F., 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.		
Title: N10M(4/6)		
Size: A3	Document Number: JV50	Rev: SB
Date: Thursday, January 08, 2009	Sheet 55 of 60	



JV50

緯創資通	**Wistron Corporation** 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title	***N10M(5/6) MIO/ GPIO***	
Size A3	Document Number **JV50**	Rev SB
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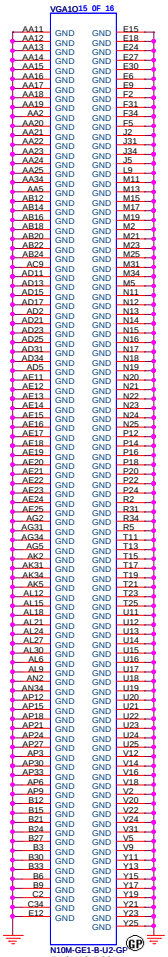

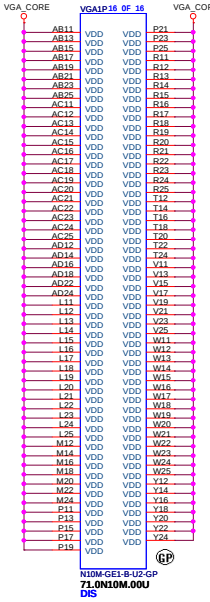

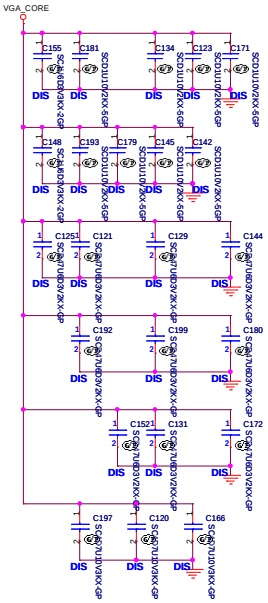

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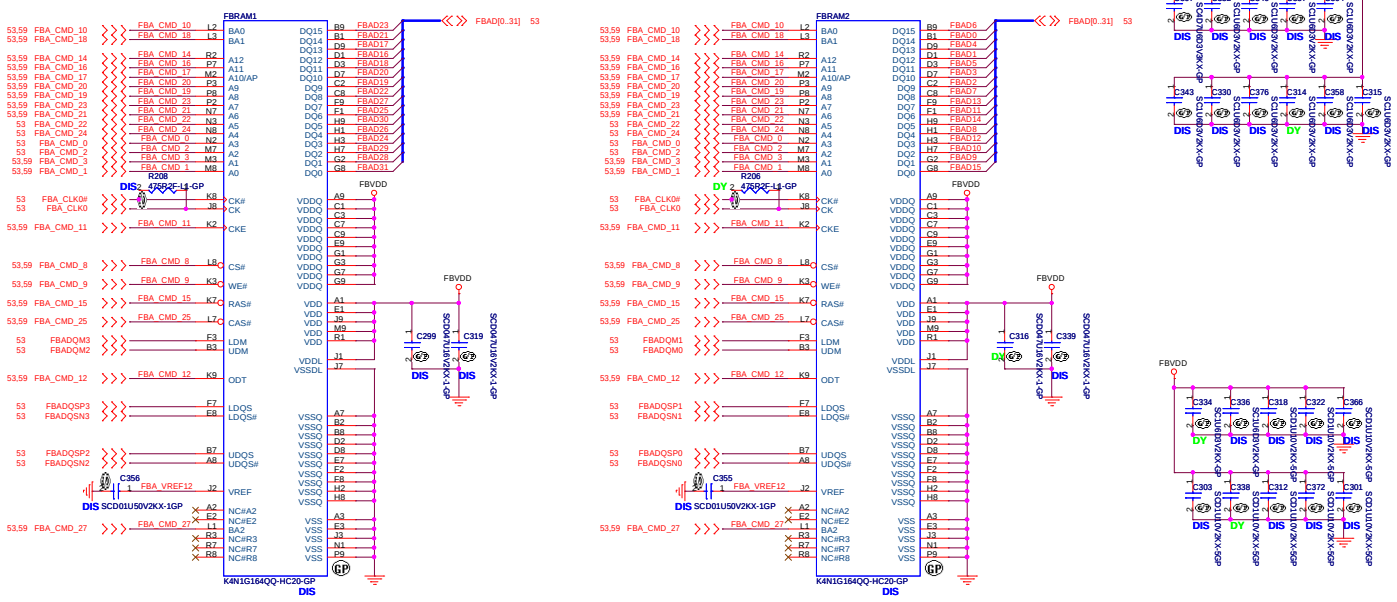
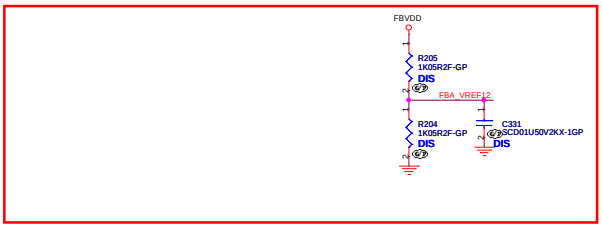
緯創資通	**Wistron Corporation** 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title	***N10M(6/6) POWER***	
Size: A3	Document Number: **JV50**	Rev: SB
Date: Thursday, January 08, 2009	Sheet 57 of 60	



modify by NV



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緯創資通	**Wistron Corporation** 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title	**VRAM(1/2)**	
Size A3	Document Number **JV50**	Rev **SB**
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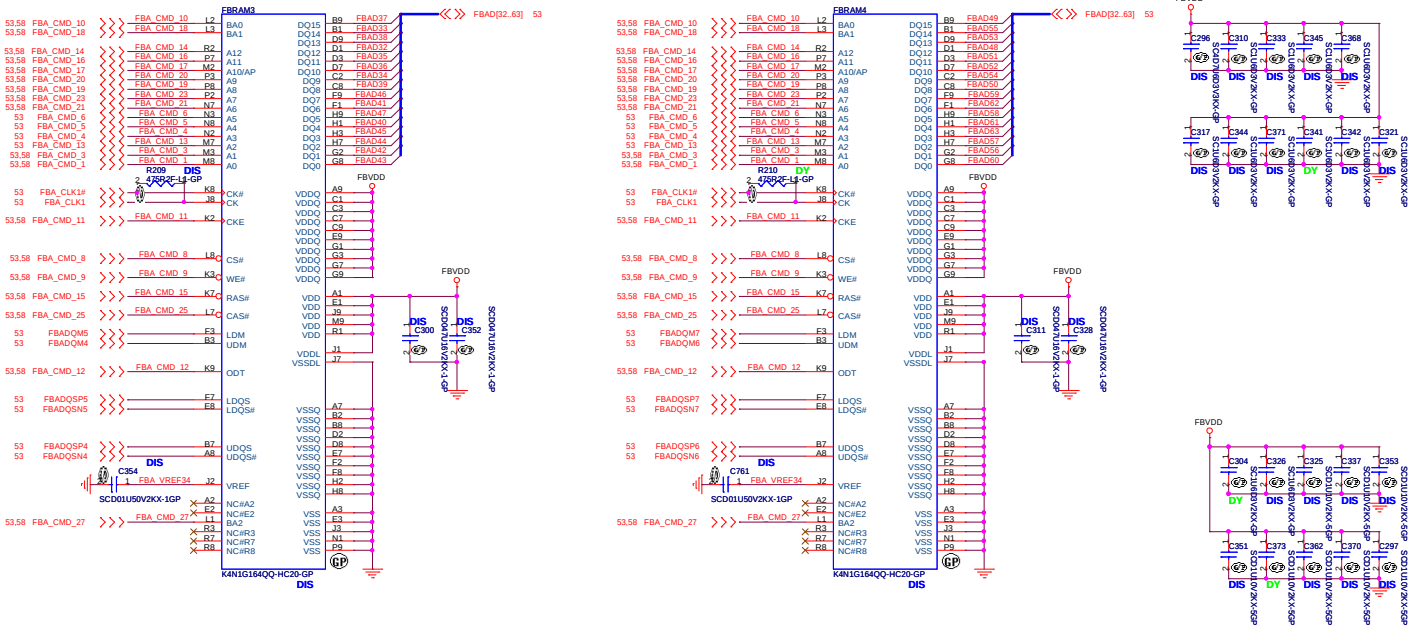
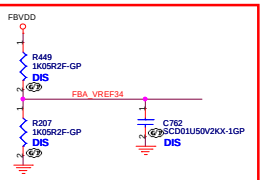


modify by NV



SB
All Component for NB9P-GE2

JV50

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: VRAM(2/2)

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12/02

Page3: change C452 C453 from 27P to 33P by vendor's request

Page33: add C872 33P for SIV

Page29: change SPKR_R1 SPKR_L1 from 20.F1396.002 to 20.F1214.002 by CE's request

Page18: change LCD1 from 20.F1296.040 to 20.F1230.040 by CE's request

Page24: change USBCN1 from 20.F1290.015 to 20.F1035.015 by CE's request

Page38: change PSCN1 from 20.K0356.006 to 20.K0382.006 by CE's request

Page18: change AMIC1 from 20.F1396.002 to 20.F1214.002 by CE's request

Page3: add R554 and change U24 pin16 from 3D3V_S0 to 3D3V_VDD48_S0

Page3: change C457 C450 C416 C430 C418 from mount to DY and change C456 from DY to mount

Page7: change R192 R195 from 0ohm resistor to 0ohm pad and add R555 RN82 RN83 RN84 RN85 for reflection

Page9: change C275 from UMA to DY and change C349 from mount to DY

Page10: change C243 C758 from mount to DY and change R167 R398 from DIS to DY

Page13: change R216 from 0ohm resistor to 0ohm pad

Page14: change C413 C252 C703 C392 C707 C734 from mount to DY

Page17: change C426 C429 from mount to DY

Page18: change C7 C499 from mount to DY and change R1 from mount to DIS and change R3 from DY to UMA

Page20: add RN86 for DIS HDMI SMbus

Page25: change R45 from 0ohm resistor to 0ohm pad

Page27: change R523 from 0ohm resistor to 0ohm pad

Page7: add R556 pull-low DY for A1 NB

Page28: change AGND & GND and change R509 from 0ohm resistor to 0ohm pad

Page28: change C795 C790 C792 from mount to DY and change R480 R479 from 0ohm to 6K2 and 8K2

Page28: combine C801 C802 two 1u to C801 4.7u

Page28: delete C815 C814 C809 R500 R503 R513 R507 R502 R508 D31 U56 and change U55 to 84.2N702.E31

Page28: change R474 from DY to mount and change R475 from mount to DY for 10dB

Page29: add L29 L30 L31 L32 L33 L34 for ESD

Page31: change R463 R464 R471 R467 R466 R460 R459 R494 R484 R493 R486 R485 R488 R489 R490 R492 R491 R487 from 0ohm resistor to 0ohm pad

Page32: change C487 C477 from mount to DY and change R269 from 0ohm resistor to 0ohm pad

Page12: change C385 C386 from 10p to 7p by vendor's request

Page35: change C136 C169 from 15p to 7p by vendor's request

Page33: change R15 R29 R34 from 0ohm resistor to 0ohm pad and change C542 from mount to DY

Page34: change C42 from mount to DY

Page35: change C615 C626 C638 R395 from mount to DY and change R394 from DY to mount for PCB version

Page36: change DB1 from mount to DY

Page38: add Q35 PWR_LED7 PWR_LED8 and change RN4 from 4P2R to 8P4R and change PWR_LED5 PWR_LED6 from 83.01221.I70 to 83.00193.A70 for LED type

Page39: change U66 pin1 from CPUCORE_ON to 1D5V_PWRGD and change D13 pin1 from S5_ENABLE to 3V/5V_EN

Page40: update power sequence logic

Page41: change G43-G50 from open gap to close gap and change R328 R352 R353 R317 R316 R319-R325 from 0ohm resistor to 0ohm pad

Page42: change R532 R545 R552 from 0ohm resistor to 0ohm pad and change G118-G128 G130-G140 from open gap to close gap

Page43: change R246 R233 from 0ohm resistor to 0ohm pad and change G5-G16 G18-G33 from open gap to close gap

Page43: change R246 pin2 from CPUCORE_ON to 1D5V_PWRGD and add R500 pull-high 10K 3D3V_S5

Page45: change G100-G109 from open gap to close gap

Page46: change R157 R187 from 0ohm resistor to 0ohm pad and change G68-G73 G86 G87 G89 G90 G92 G93 G95 G96 G99 from open gap to close gap

Page46: delete TC19 and change TC20 from DY to GFX

Page49: change G55-G67 G74-G77 from open gap to close gap

Page29: change RN75 from 47ohm to 75ohm

Page28: change C804 C807 from 4.7u to 1u 25V X5R

Page45: delete TC24

Page19: delete R104 R129

12/04

Page24: change U47 from 74.00545.A79 to 74.00547.A79

Page20: swap HDMI signals for routing

Page28: change U53 pin22 from AUD_HP1_EN to AMP_MUTE#_R

Page48: change BAT1 from 20.81094.007 to 20.81156.007

Page22: change ODD1 from 62.10065.541 to 62.10065.751

Page22: change R231 R247 from 0ohm resistor to 0ohm pad

12/05

Page25: change R39 R53 R21 R31 R22 R35 R28 from 0ohm resistor to 0ohm pad

Page46: change L23 from 68.R8210.10V to 68.1R01A.20B and change U43 from 84.04812.A37 to 84.04168.037 by power team's request

Page41: change R344 from 2K87 to 3K16 and change C586 from 0.47u to 0.1u by power team's request

Page41: change U35 U39 from 84.01426.037 to 84.12003.A37 and change U6 U7 U36 U38 from 84.01712.037 to 84.57N03.A37 by power team's request

Page45: change R457 from 11K to 3K48 and change TC23 from 390u to 220u by power team's request

12/08

Page26: change EC7 from DY to mount EMI's request

Page48: change EC28 EC30 EC31 EC32 from DY to mount EMI's request

Page31: change EC51 EC52 EC55 EC57 from 0.1u DY to 22p mount EMI's request

Page5: change C79 C80 from DY to mount EMI's request

Page46: change C659 from DY to GFX EMI's request

Page50: change SPRING_GND16-SPRING_GND20 from DY to mount EMI's request

Page50: add EC61-EC67 0.1u by EMI's request

Page20: change R313 R314 from 10K 100K to 18K 47K by NV's request

Page35: change U14 pin83 RN65 pin2 from SHBM to DBC_EN by annie's request

Page18: change LCD1 pin35 from NC to DBC_EN by annie's request

Page20: add ER1-ER8 0ohm pad by EMI's request

Page10: change C636 from 1000p DY to 27p mount by RF's request

12/09

Page49: change R406 from 6K2 to 4K75 by power team's request

Page46: change TC16 from mount to GFX

Page50: add TC19 TC24 100u

Page41: change C528 C529 530 C588 C597 C604 from 10u to 4.7u and change C528 C588 from mount to DY

Page46: change C656 C653 from 10u to 4.7u and change C653 from GFX to DY

Page42: change C856 C857 C851 C850 from 10u to 4.7u and change C857 C850 from mount to DY

Page41: change TC5 from DY to mount

Page5: change C553 C538 C552 C539 C547 C536 C548 C537 from DY to mount

Page17: change C426 C428 C429 from 10u to 4.7u and change C429 from DY to mount

Page16: change C440-C442 C463-C465 from 10u to 4.7u and change C440 from DY to mount and change C464 from DY to mount

Page20: change HDMI from 62.10078.161 to 62.10078.171 by CE's request

Page24: change USBCN1 from 20.F1035.015 to 20.F1290.015 by CE's request

12/10

Page46: add C873 33p GFX by RF's request

Page43: add C874 C875 33p by RF's request

Page20: swap U8 pin13 14 47 48

Page33: change R16 from DY to mount

Page47: change R292 from 0ohm resistor to 0ohm pad

12/11

Page33: change MINI2 pin 51 from 5V_S5_MIN1 to 5V_S5_MIN2

12/15

Page52: change VRAM strap R350

JV50

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21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.

Title: HISTORY

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12/22

Page49: change R427 from 30K 47K and R428 from 47K to 30K

SC

12/22

Page42: modify by power team's request

Page35: change R372 R395 from DY to mount and change R373 R394 from mount to DY

-1

01/06

Page17: change C400 from mount to DY and change C399 from DY to mount

Page30: change R267 from 39R to 0ohm pad

Page38: delete RN7 and add Q36 Q37

Page25: change U3 pin 38 52 from LAN_AVDD to TP and change U3 pin 68 from NC to TP

Page25: delete R58 and add RN87 and change U5 to 72.24C02.R01

Page3: change R255 from 22R to 33R and change RN42 from 0ohm to 33R

Page33: change R268 R275 R259 from 0ohm resistor to 0ohm pad

Page35: change R394 from DY to mount and change R395 from mount to DY

Page28: change R526 from 0ohm resistor to 0ohm pad

Page35: change R401 from 0ohm resistor to 0ohm pad

Page35: delete Q12 and add R502 R503

Page35: change RN23 pin 5 6 from 3D3V_AUX_S5 to 3D3V_S0

Page44: change U46 to APL5930 by power team's request

Page38: add 3G and BT option

Page28: change R479 from 8K2 to 10K and change R480 from 6K2 to 4K99 for audio speaker gain

Page28: merge CCD1 to LCD1

01/07

Page44: change R437 from 0ohm pad to 0ohm resistor

Page9: change TC18 from UMA to DY and change C276 from DY to mount

Page35: delete RN21 and add R507 10K DY

Page38: change RN4 to 330R and change RN8 to 100R and delete R10 and change RN3 to 8P4R 200R

Page47: change C515 to 78.15322.2FL by power team's request

Page3: mount 33p on EC23 EC24 EC25 EC39 EC48 for RF's request

Page3: add EC68 EC69 33p DY by RF's request

Page20: add R129 4K7 for diffierent vendor

01/08

Page42: change R541 from 200K to 100K and change R544 location

Page42: change R532 R545 from 0ohm pad to 0ohm resistor

01/09

Page38: change name from 3G/BT_LED1 to 3GBT_LED1

Page50: add SPRING_GND23 34.40U07.001, SPRING_GND24 34.40U07.001, SPRING_GND25 34.15J03.001

Page50: SPRING_GND17, SPRING_GND19 change from 34.41Y19.001 to 34.39S07.003

Page50: SPRING_GND18 change from 34.41Y19.001 to 34.4B312.002

JV50

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Title: HISTORY

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