


LCFC Confidential

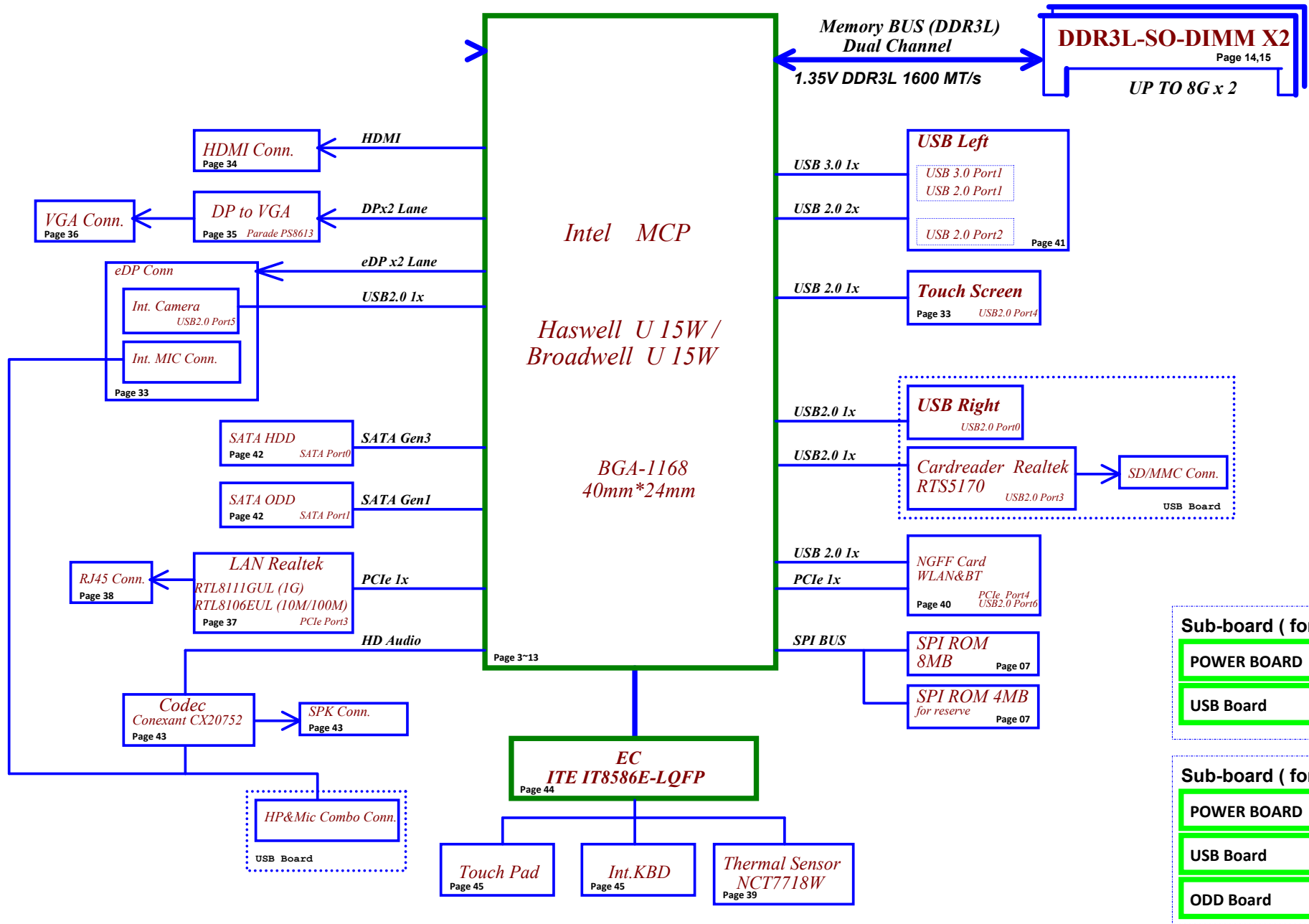
ACLU1/2 UMA M/B Schematics Document

Intel Haswell/Broadwell U-Processor

2013-12-05

REV: 1.0

Security Classification	LC Future Center Secret Data			Title		
Issued Date	2013/08/08	Deciphered Date	2013/08/05	Cover Page		
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Title		
Block Diagram		
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Voltage Rails (O --> Means ON , X --> Means OFF)

Power Plane / State	B+	+3VALW +5VALW	+3VALW_PCH	+1.35V	+5VS +3VS +1.5VS +1.35VS +1.05VS +0.675VS CPU_CORE
S0	O	O	O	O	O
S3	O	O	O	O	X
S3 Battery only	O	O	O	O	X
S5 S4/AC Only	O	O	O	X	X
S5 S4 Battery only	O	X	X	X	X
S5 S4 AC & Battery don't exist	X	X	X	X	X

STATE \ SIGNAL	SLP_S1#	SLP_S3#	SLP_S4#	SLP_S5#	+VALW	+V	+VS	Clock
Full ON	HIGH	HIGH	HIGH	HIGH	ON	ON	ON	ON
S1 (Power On Suspend)	LOW	HIGH	HIGH	HIGH	ON	ON	ON	LOW
S3 (Suspend to RAM)	LOW	LOW	HIGH	HIGH	ON	ON	OFF	OFF
S4 (Suspend to Disk)	LOW	LOW	LOW	HIGH	ON	OFF	OFF	OFF
S5 (Soft OFF)	LOW	LOW	LOW	LOW	ON	OFF	OFF	OFF

USB Port Table

USB 2.0 EHC11		USB 3.0 XHCI	
0	USB Port (Right Side)		
1	USB Port1 (Left Side)	1	USB Port1 (Left Side)
2	USB Port2 (Left Side)	2	
3	Cardreader	3	
4	TOUCH PANEL	4	
5	Camera		
6	NGFF(WLAN)		
7			

BOM Structure Table

BOM Structure	BTO Item
@	Not stuff
14@	For 14" part
15@	For 15" part
8111GUL@	8111GUL LAN Part
8106EUL@	8106EUL LAN Part
AOAC@	AOAC support part
GIGA@	GIGA LAN Part
JET@	For AMD Jet GPU part
ME@	ME part(connector, hole)
TS@	For support touch panel sku part

SMBUS Control Table

	SOURCE	BATT	IT8586E	SODIMM	WLAN WIMAX	Thermal Sensor	PCH	TP Module	charger
EC_SMB_CK1	IT8586E	V	V	X	X	X	X	X	V
EC_SMB_DA1	+3VALW	V	+3VALW	X	X	X	X	X	V
EC_SMB_CK2	IT8586E	X	V	X	X	V	V	X	X
EC_SMB_DA2	+3VS	X	+3VS	X	X	+3VS	+3VALW_PCH	X	X
PCH_SMB_CLK	PCH	X	X	V	V	X	V	X	X
PCH_SMB_DATA	+3VALW_PCH	X	X	+3VS	+3VS	X	+3VALW_PCH	X	X

PCIE PORT LIST

Port	Device
1	
2	
3	LAN
4	WLAN
5	
6	

EC SM Bus1 address EC SM Bus2 address PCH SM Bus address


Device		Device	Address	Device	Address
Smart Battery	0X16	Thermal Sensor NCT7718W	1001_100xb	DDR DIMMA	1010 000Xb
Charger	0001 0010 b	PCH	need to update	DDR DIMMB	1010 010Xb
				Wlan	Rsvd

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Title Notes List

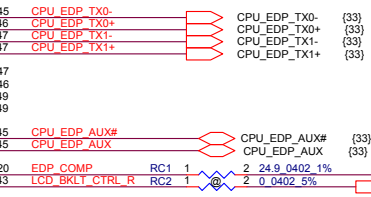
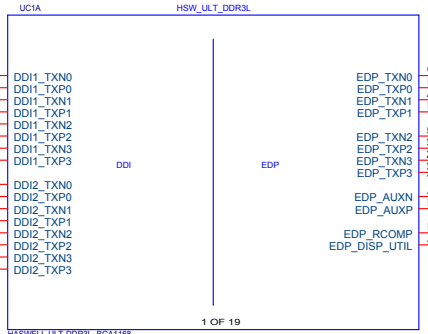
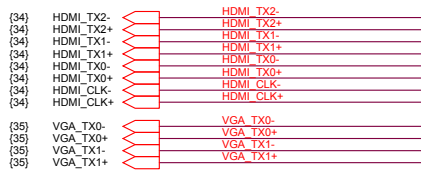


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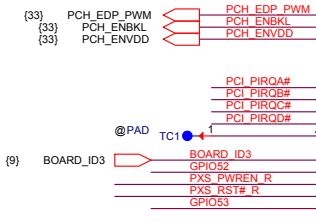
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HDMI D2
HDMI D1
HDMI D0
HDMI CLK
HDMI CLK

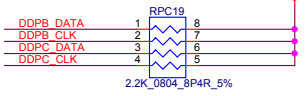
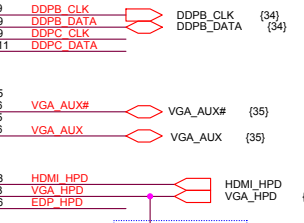
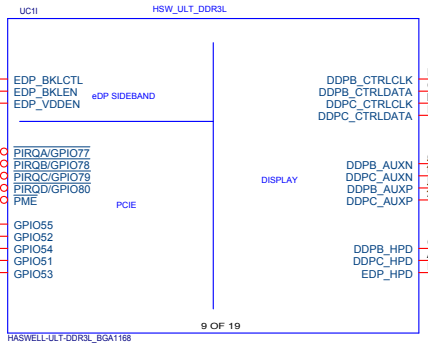
DP TO VGA Converter



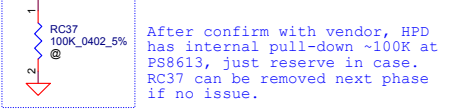
+VCCIOA_OUT & EDP_COMP :
Trace Width: 20mil
Space: 25mil
Max length: 100mil



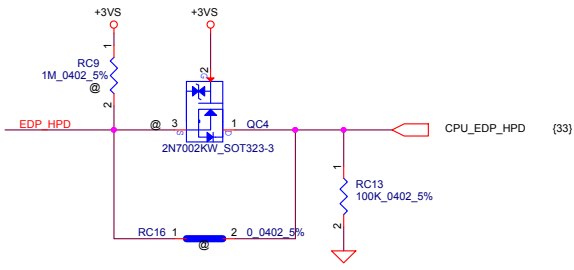
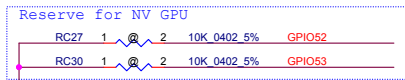
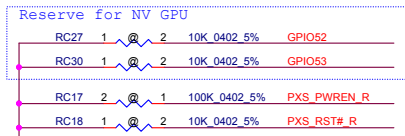
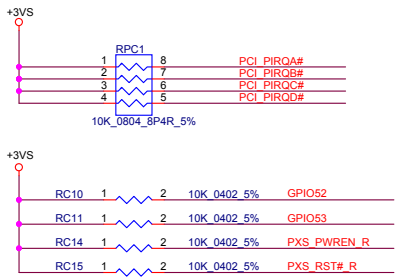
ACLU2: delete PXS_PWREN_R PXS_RST#_R PORT and RC7 RC8 RC10 RC13



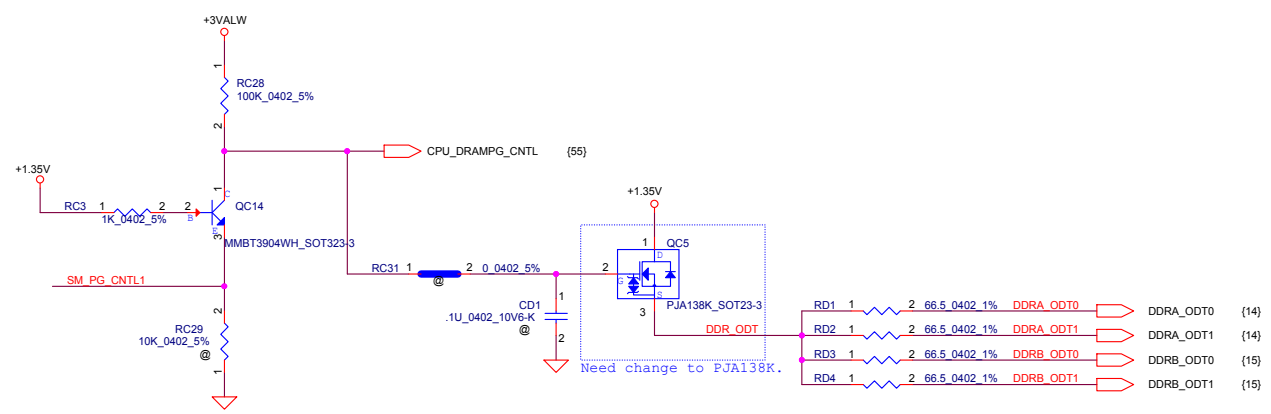
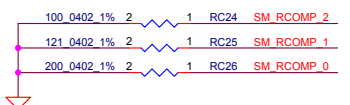
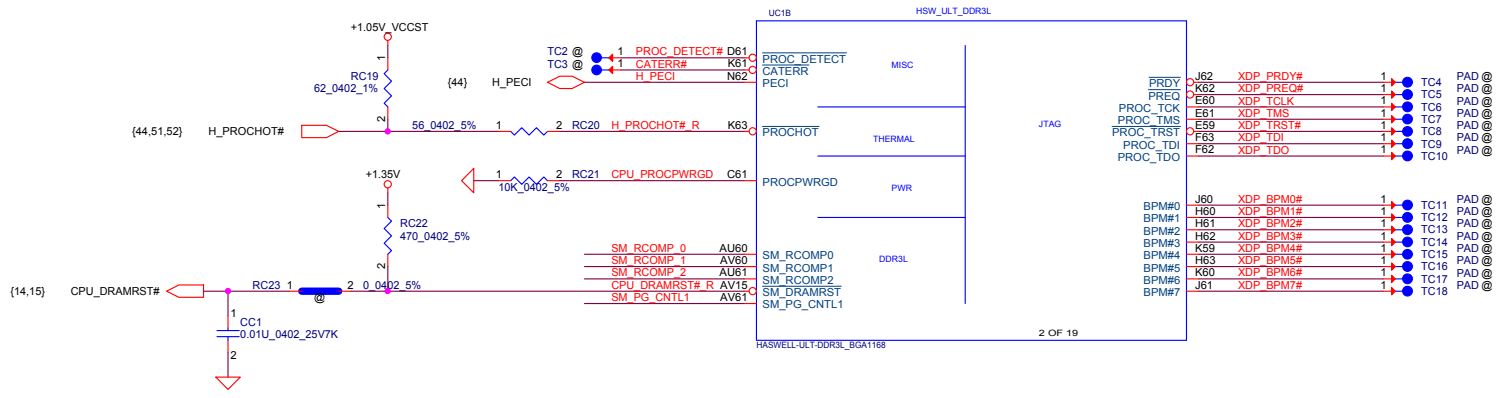
DDPx_CTRLDATA
The signal has a weak internal pull-down.
* H Port is detected.
L Port is not detected.



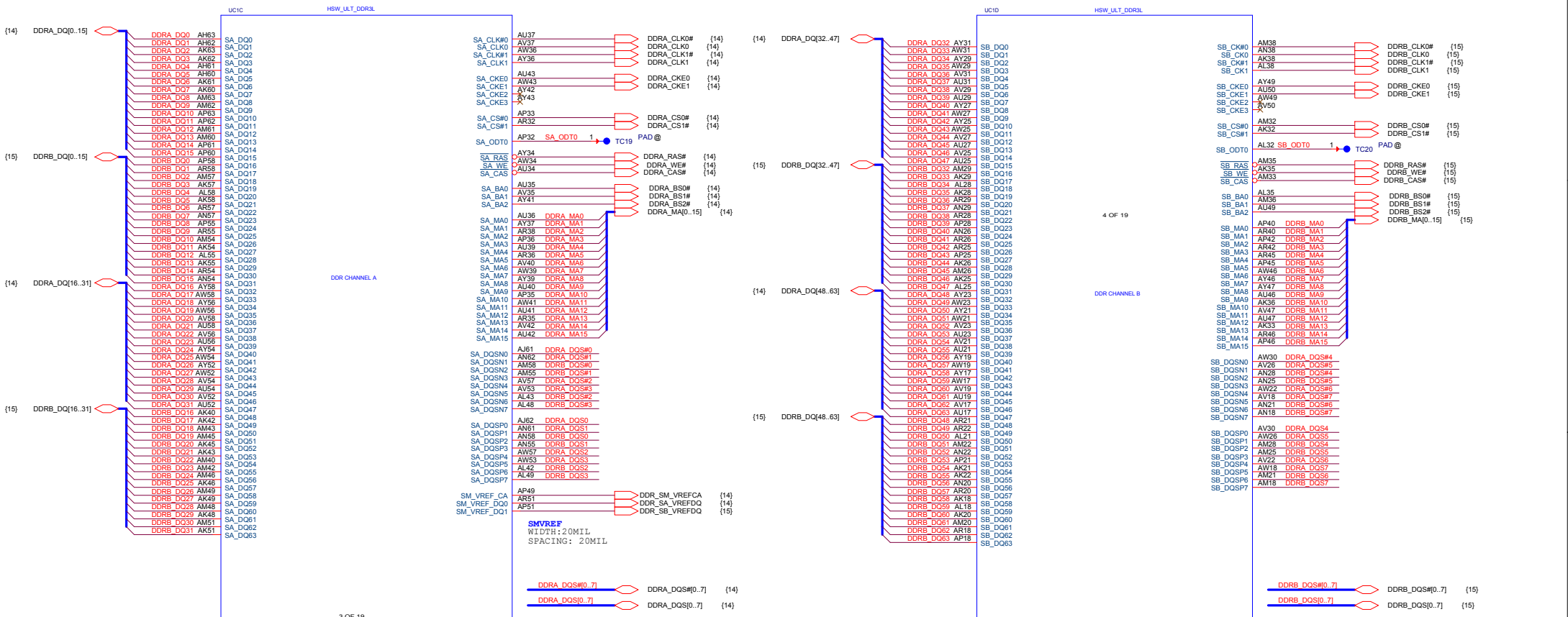
After confirm with vendor, HPD has internal pull-down ~100K at P88613, just reserve in case. RC37 can be removed next phase if no issue.




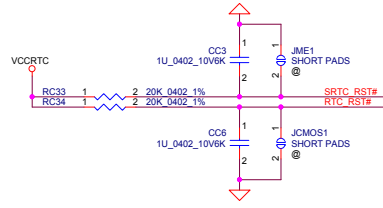
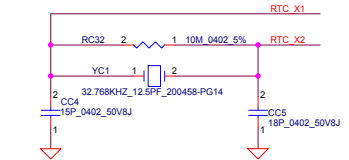
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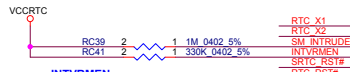
Security Classification	LC Future Center Secret Data		Title	 MCP (MISC, THERMAL, JTAG)
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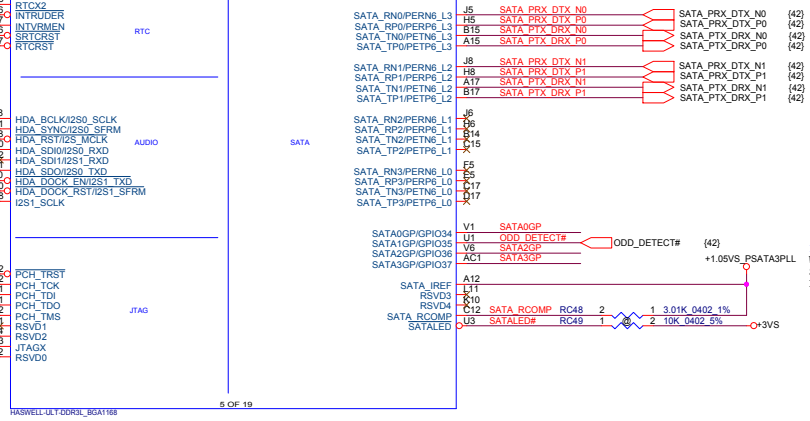
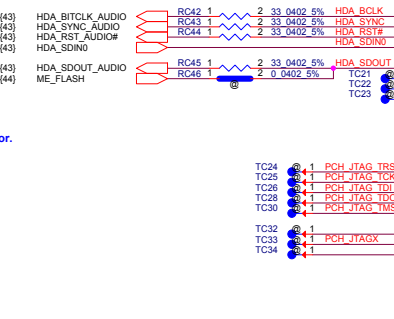
CRYSTAL
 1. Space 15MIL
 2. No trace under crystal
 3. Place on opposite side of MCP for temp influence



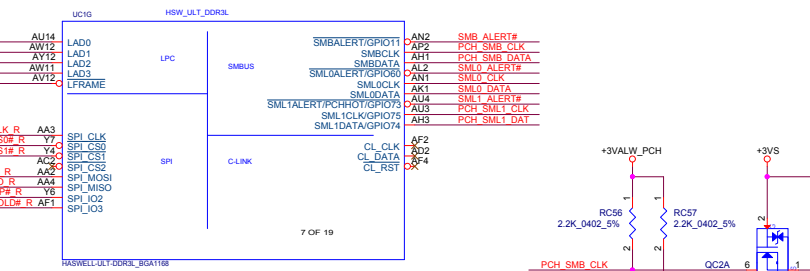
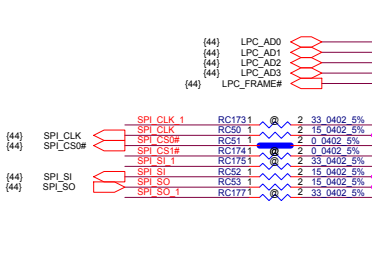
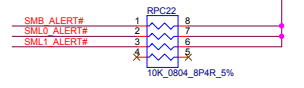
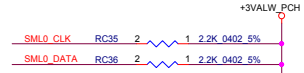
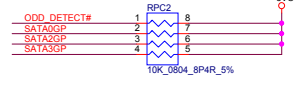
INTVRMEN
 H Integrated VRM enable (Default)
 L Integrated VRM disable
 (INTVRMEN should always be pull high.)



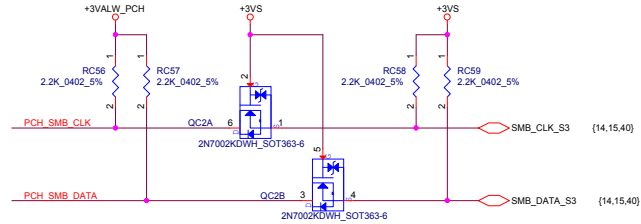
HDA_SDO This signal has a weak internal pull-down.
 0 = Enable security measures defined in the Flash Descriptor.
 1 = Disable Flash Descriptor Security(override). This strap should only be asserted high during external pull-up in manufacturing/debug environments ONLY.



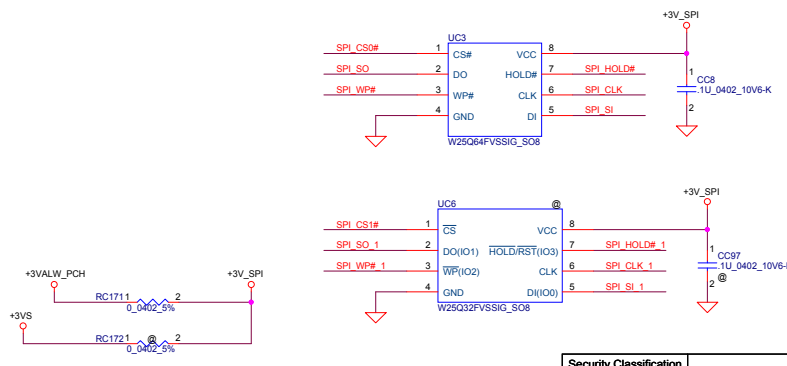
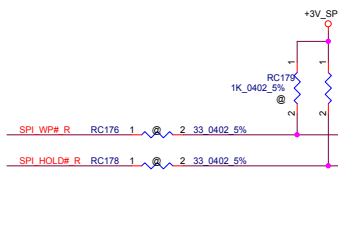
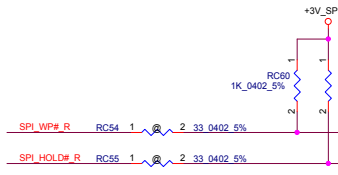
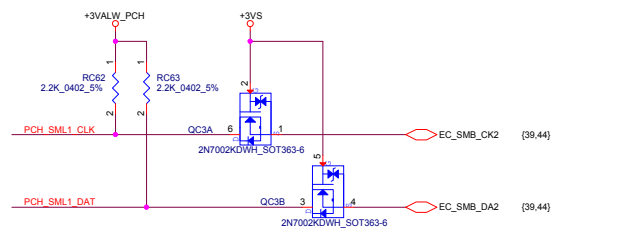
IREF6RCOMP
 Width: 12-15MIL
 Space: 12MIL
 Length: 500MIL



DIMM1, DIMM2, NGFF

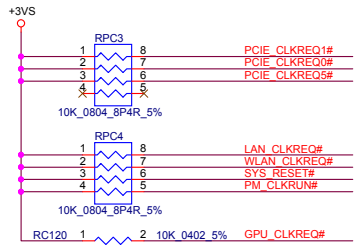


GPU, EC, Thermal Sensor

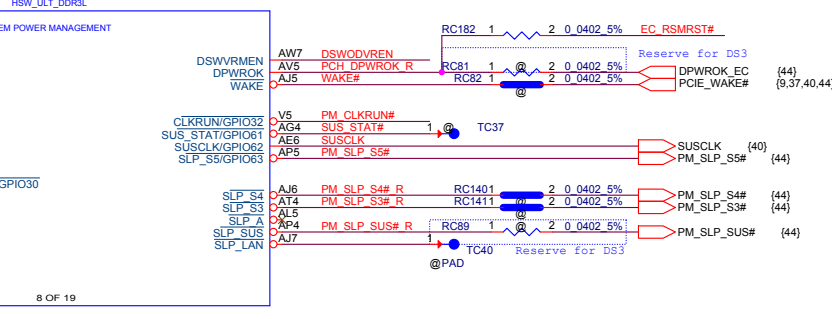
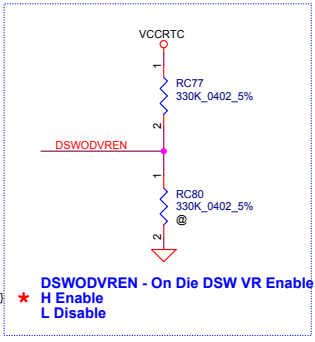
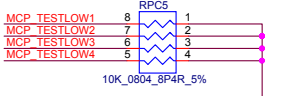
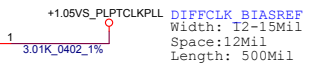
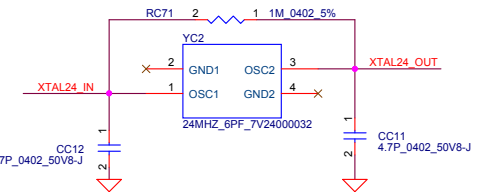
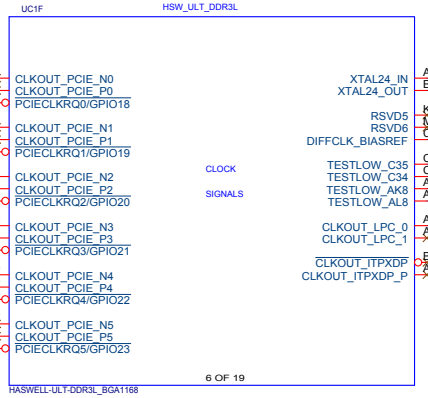
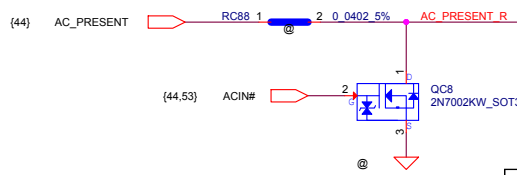
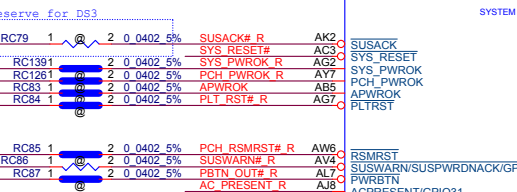
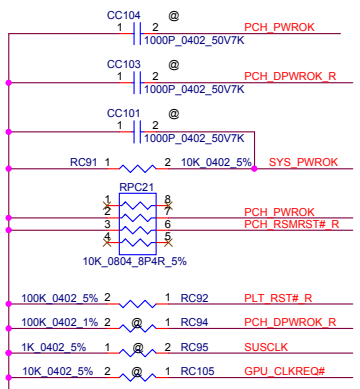
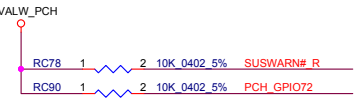
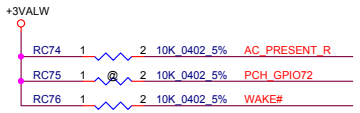


+3V_SPI
 1. If support DS3, connect to +3VS and don't support EC mirror code;
 2. If don't support DS3, connect to +3VALW_PCH and support EC mirror code.

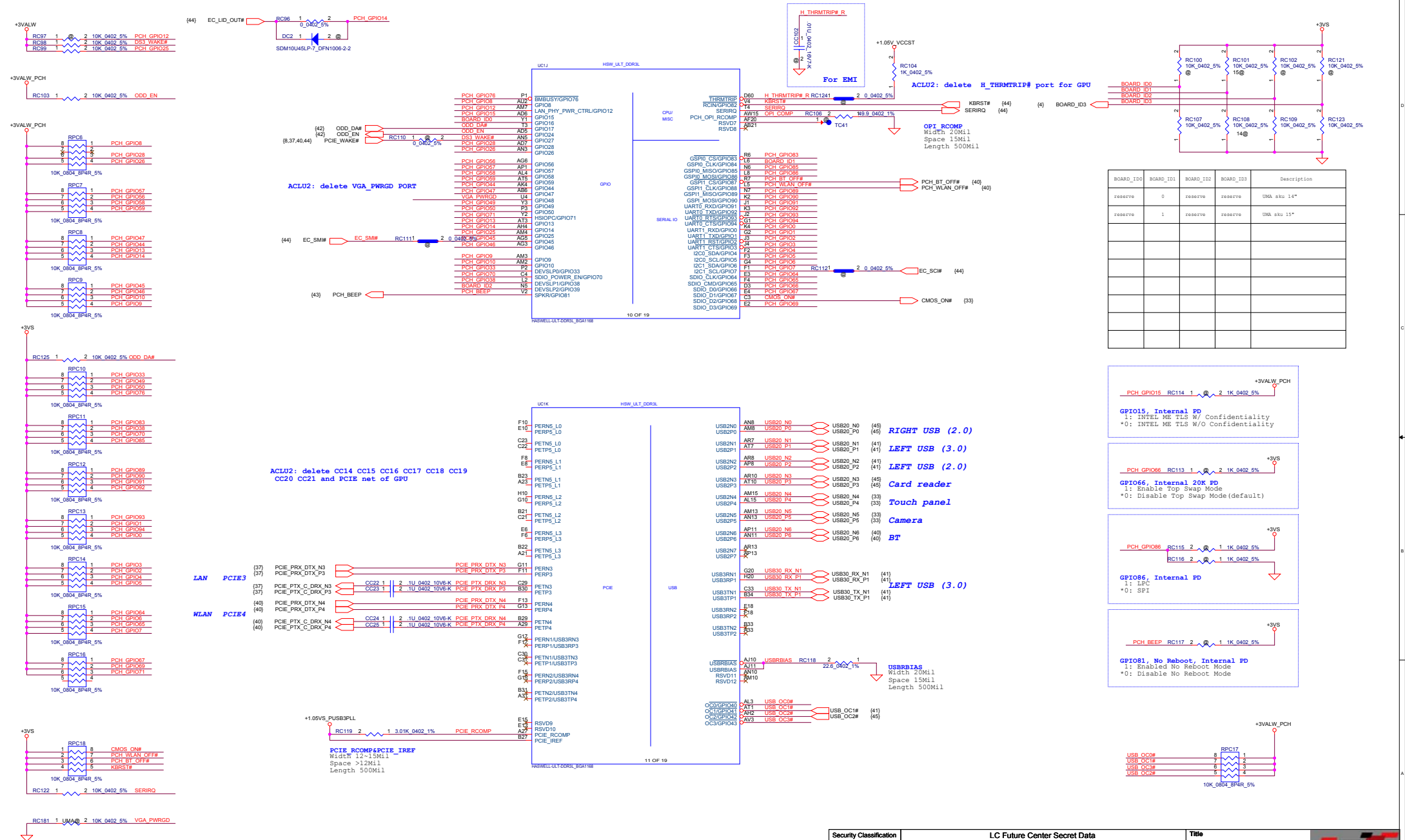
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PCIE CLK2 LAN (37) CLK_PCIE_LAN#
 (37) CLK_PCIE_LAN#
 (37) LAN_CLKREQ#
 PCIE CLK3 WLAN (40) CLK_PCIE_WLAN#
 (40) CLK_PCIE_WLAN#
 (40) WLAN_CLKREQ#
 PCIE CLK4 GPU

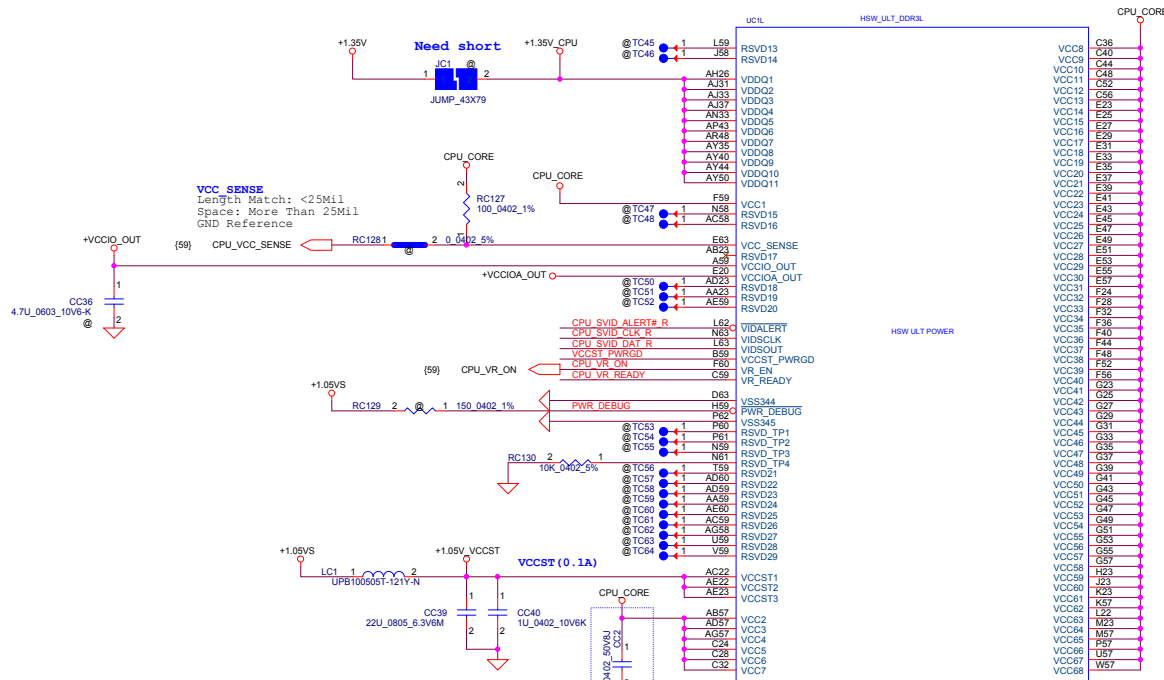


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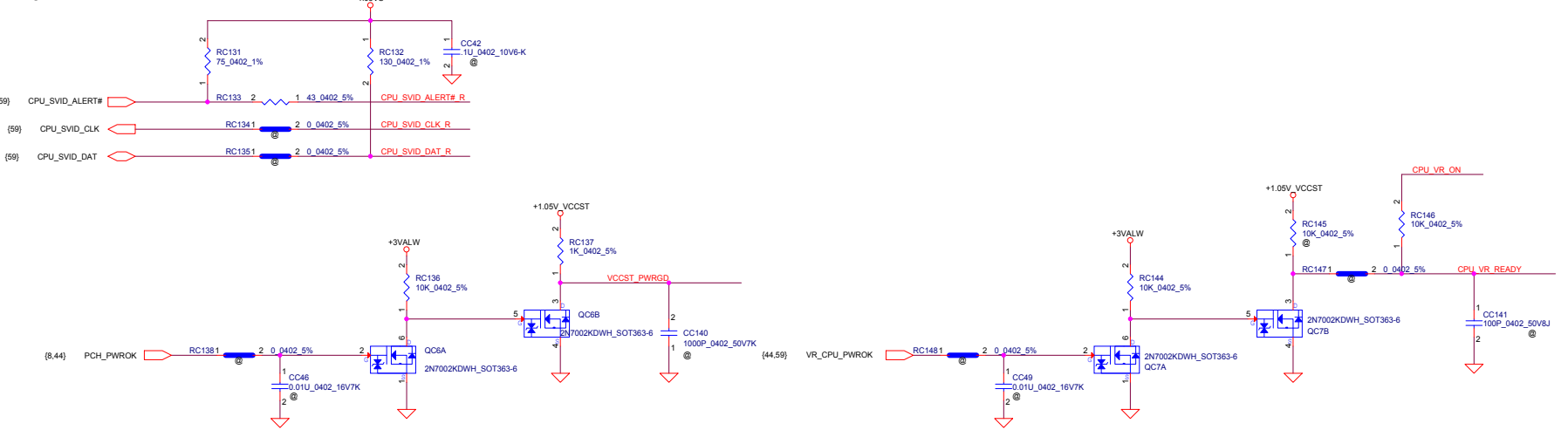


BOARD_ID0	BOARD_ID1	BOARD_ID2	BOARD_ID3	Description
reserve	0	reserve	reserve	DMA sku 14"
reserve	1	reserve	reserve	DMA sku 15"

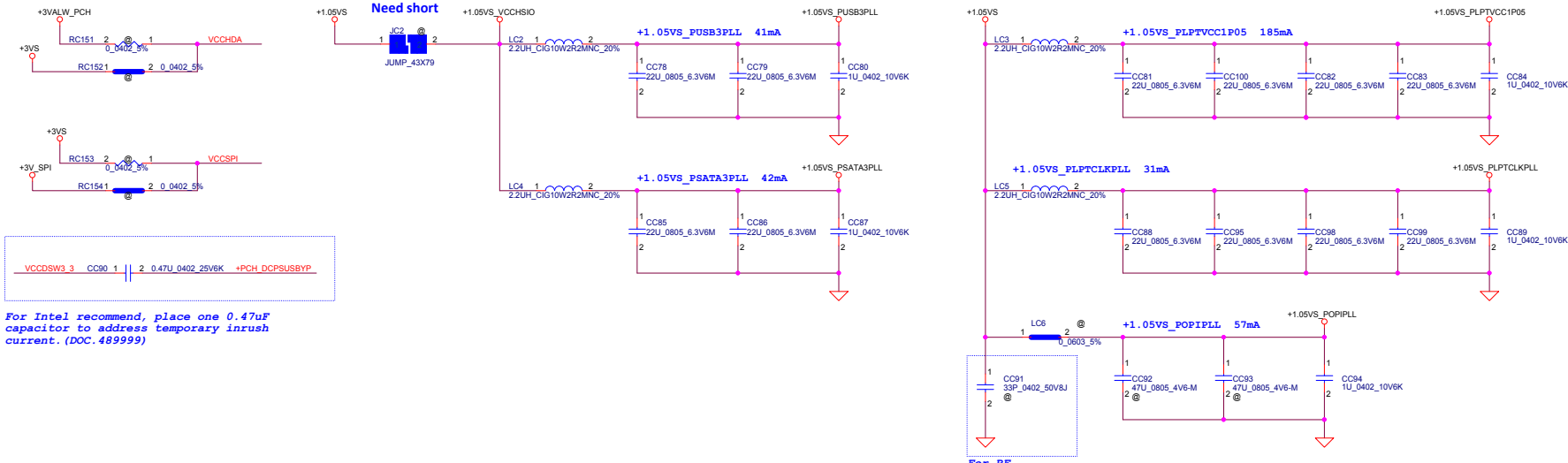
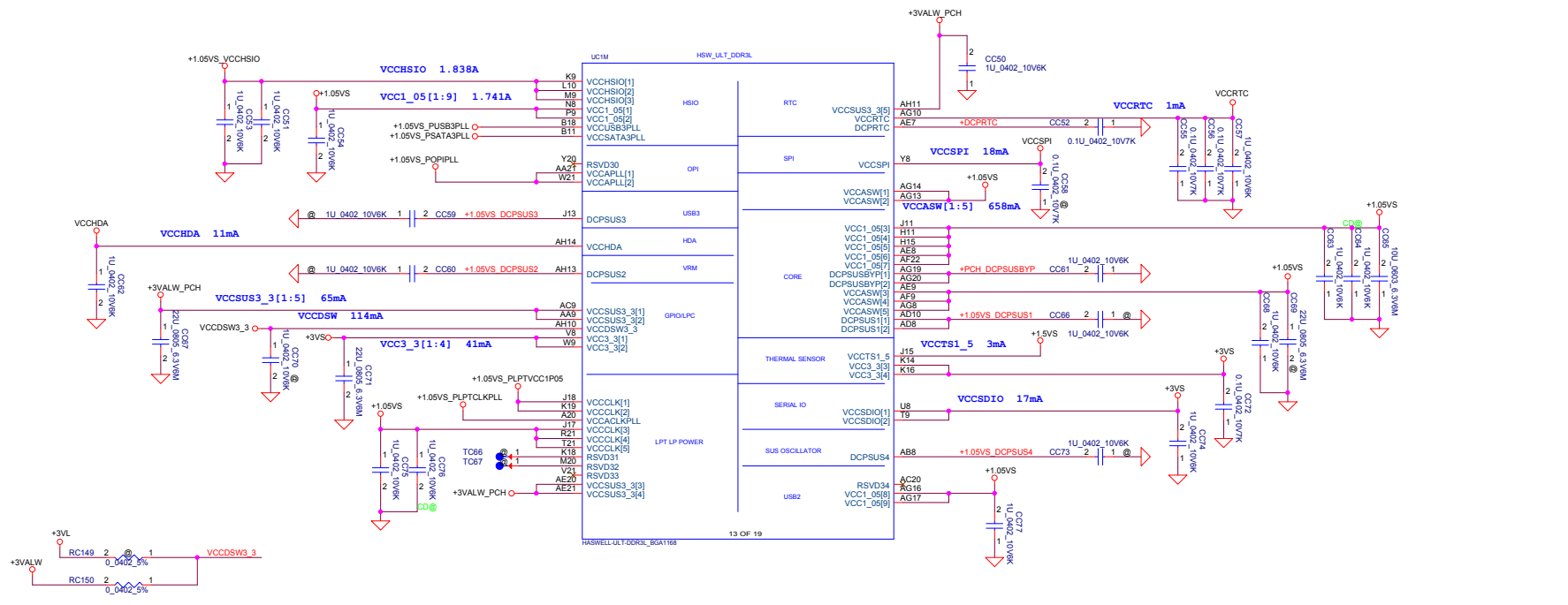
- PCH GPIO15** RC114 1 @ 2 1K 0402 5% +3VALW_PCH
GPIO15, Internal PD
 1: INTEL ME TLS W/ Confidentiality
 *0: INTEL ME TLS W/O Confidentiality
- PCH GPIO66** RC113 1 @ 2 1K 0402 5% +3VS
GPIO66, Internal 20K PD
 1: Enable Top Swap Mode
 *0: Disable Top Swap Mode(default)
- PCH GPIO68** RC115 2 @ 1 1K 0402 5% +3VS
 RC116 2 @ 1 1K 0402 5%
GPIO68, Internal PD
 1: LFC
 *0: SPI
- PCH BEEP** RC117 2 @ 1 1K 0402 5% +3VALW_PCH
GPIO81, No Reboot, Internal PD
 1: Enable No Reboot Mode
 *0: Disable No Reboot Mode



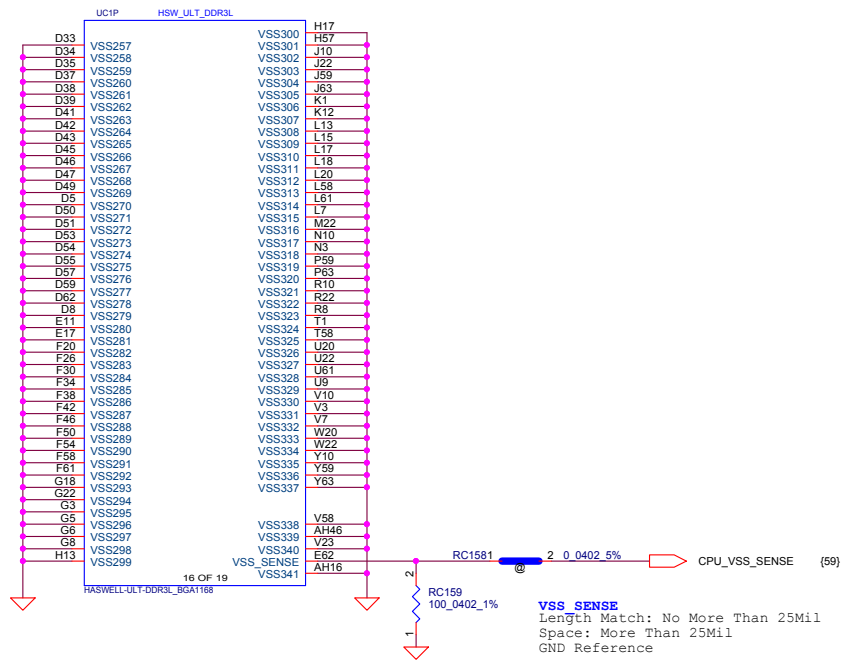
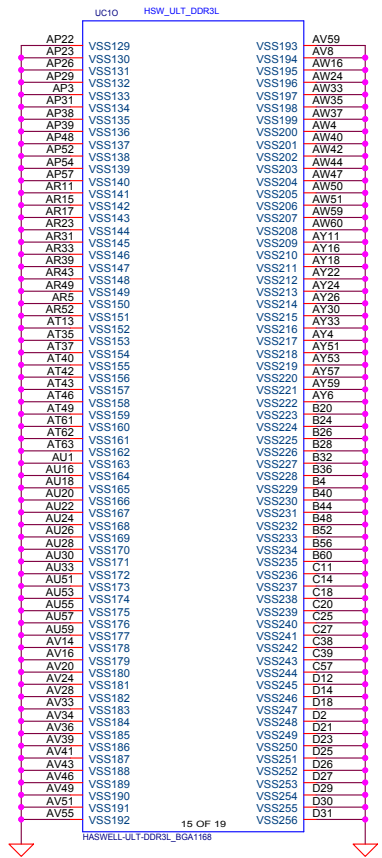
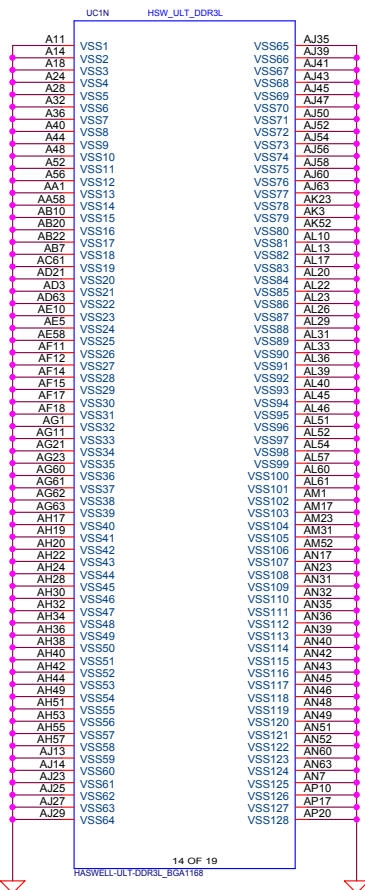
- SVID**
- 1, Stripline Line, No More Than 6000Mil
 - 2, Alert# Route Between CLK and Data
 - 3, CLK Length<Data Length<CLK Length + 2000Mil
 - 4, Space at least 18Mil




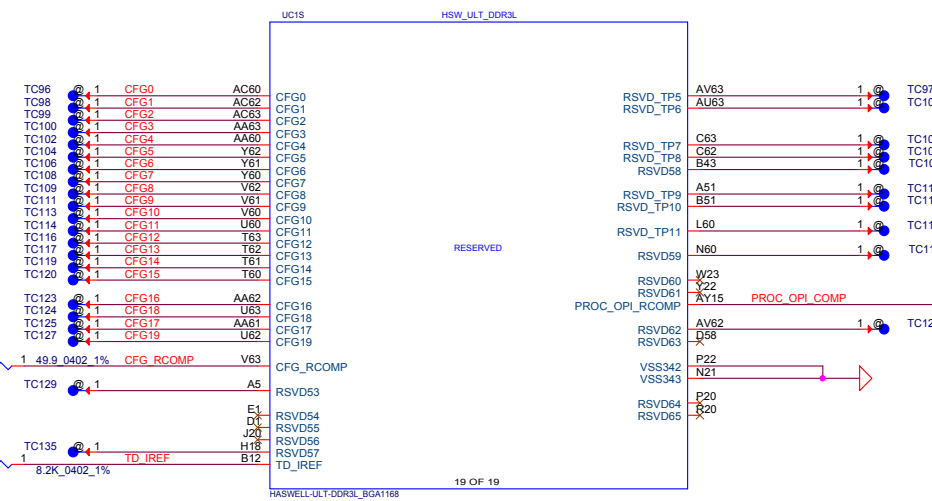
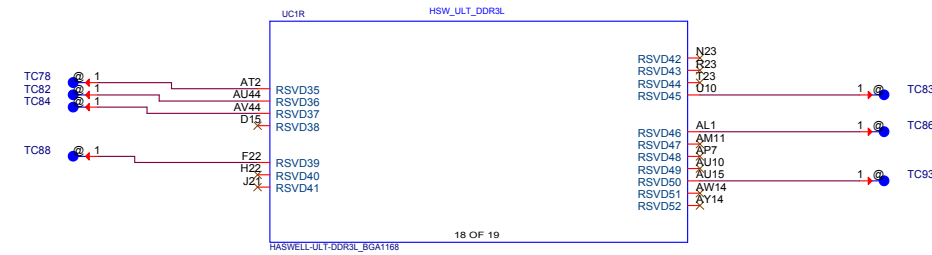
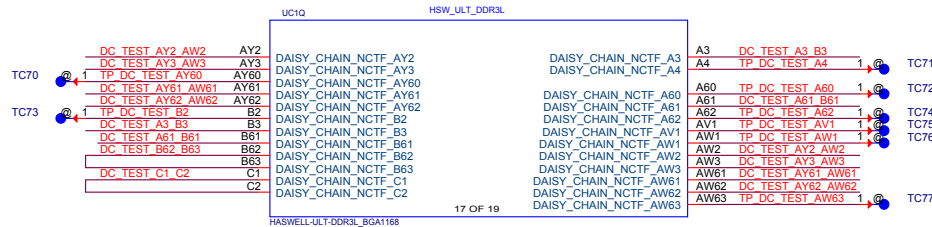
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For Intel recommend, place one 0.47uF capacitor to address temporary inrush current. (DOC. 489999)



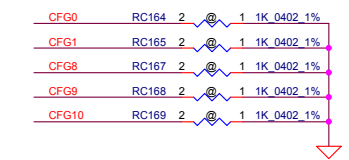
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CFG_RCOMP&TD_IREF
Width 20Mil
Space 15Mil
Length 500Mil

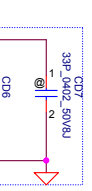
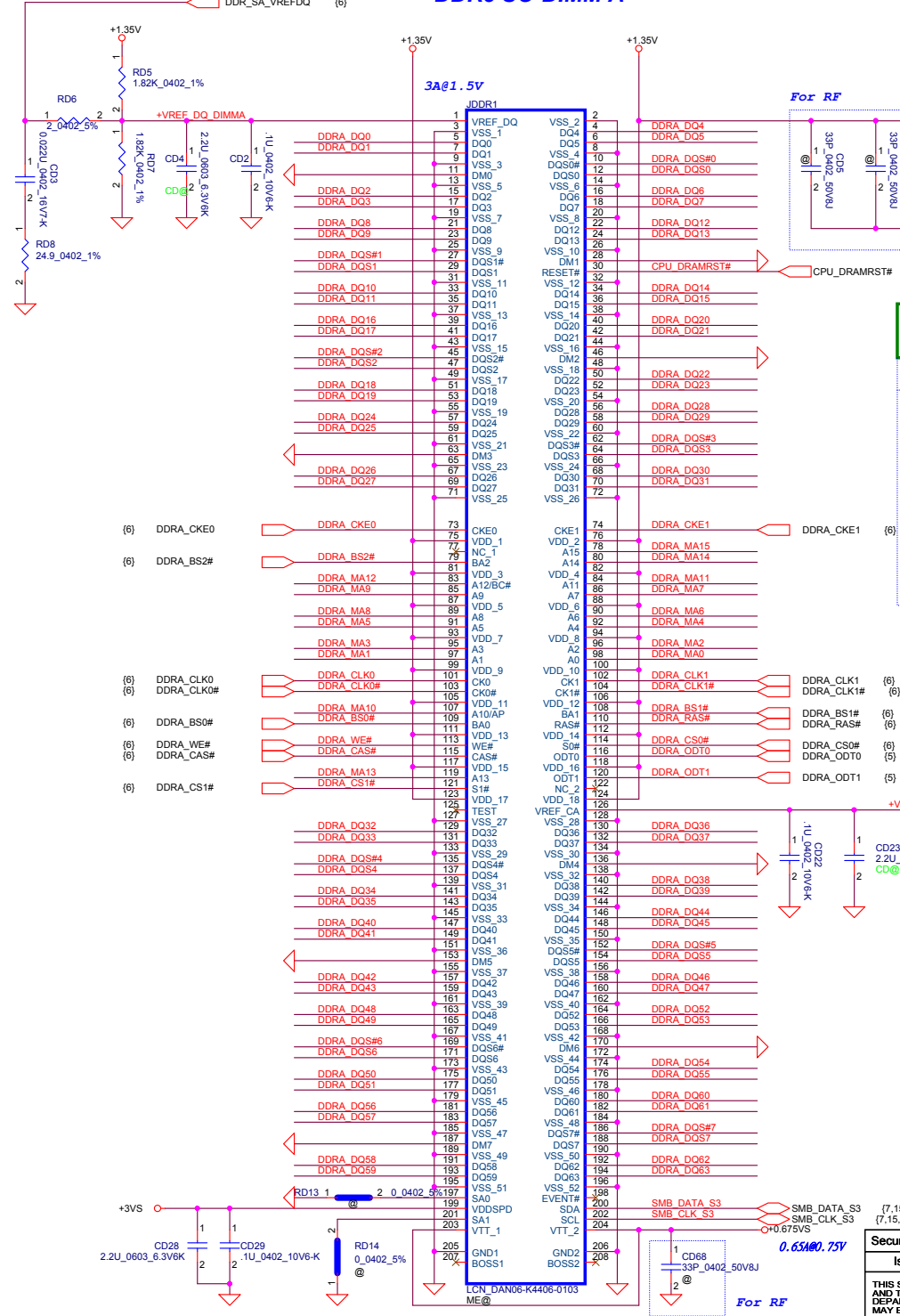
CFG3
*1: Disable
0: Enable, Set DFX Enabled BIT
In Debug Interface MSR

CFG4
*L: eDP enable
H: eDP disable



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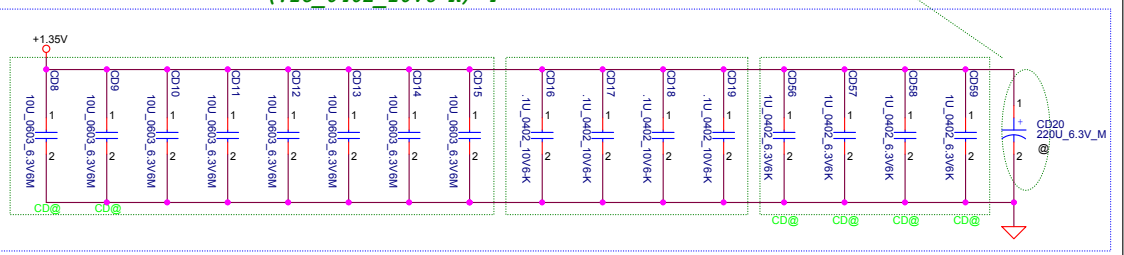
DDR3 SO-DIMM A



Layout Note:
Place near DIMM

- DDR3_A0[0..63] (6)
- DDR3_A1[0..7] (6)
- DDR3_A2[0..7] (6)
- DDR3_A3[0..15] (6)

OSCON (220uF_6.3V_4.2L_ESR17m)*1=(SF000002Y0J)
(10uF_0603_6.3V)*8
(1U_0402_6.3V)*4
(.1U_0402_10V6-K)*4

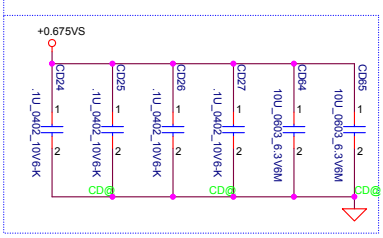


Note:
VREF trace width:20 mils at least
Spacing:20mils to other signal/planes
Place near DIMM socket

Trace width:20 mils
Space:20mils

Layout Note:
Place near DIMM

(10U_0603_6.3V)*2
(.1U_0402_10V)*4



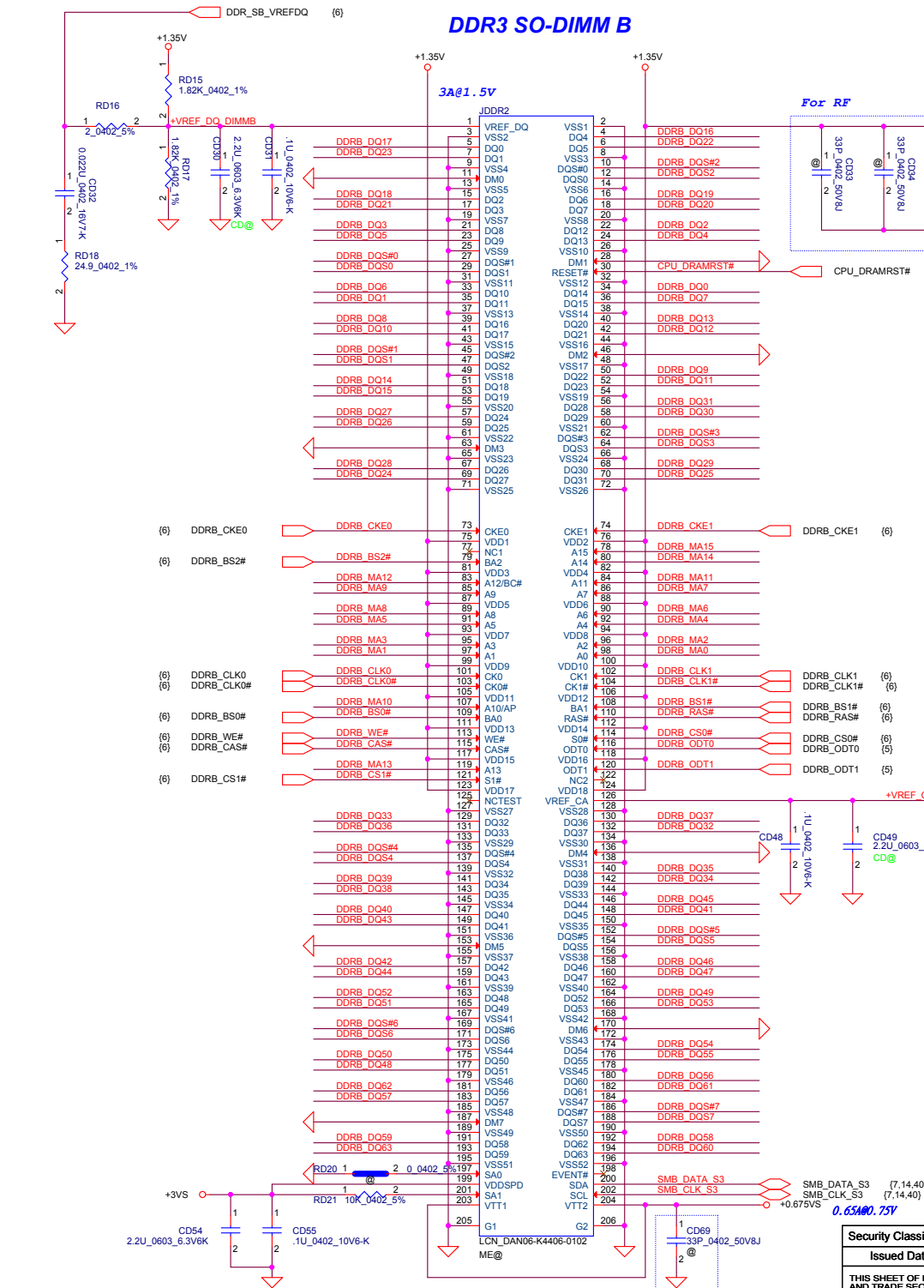
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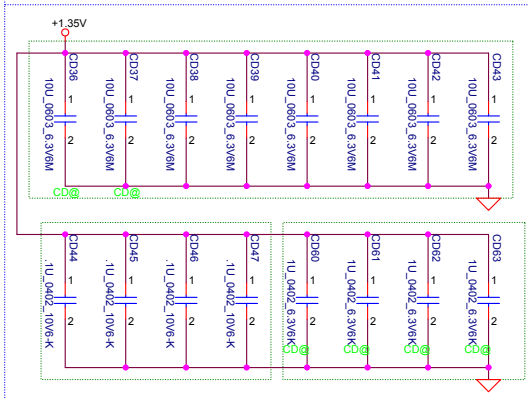
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Size	Document Number	
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DDR3 SO-DIMM B

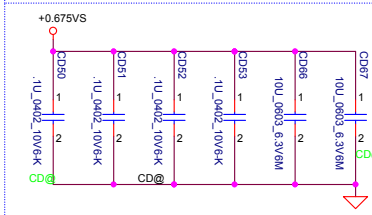
Swap Table



Layout Note:
Place near DIMM
(10uF_0603_6.3V)*8
(1U_0402_6.3V)*8
(.1U_0402_10V6-K)*4



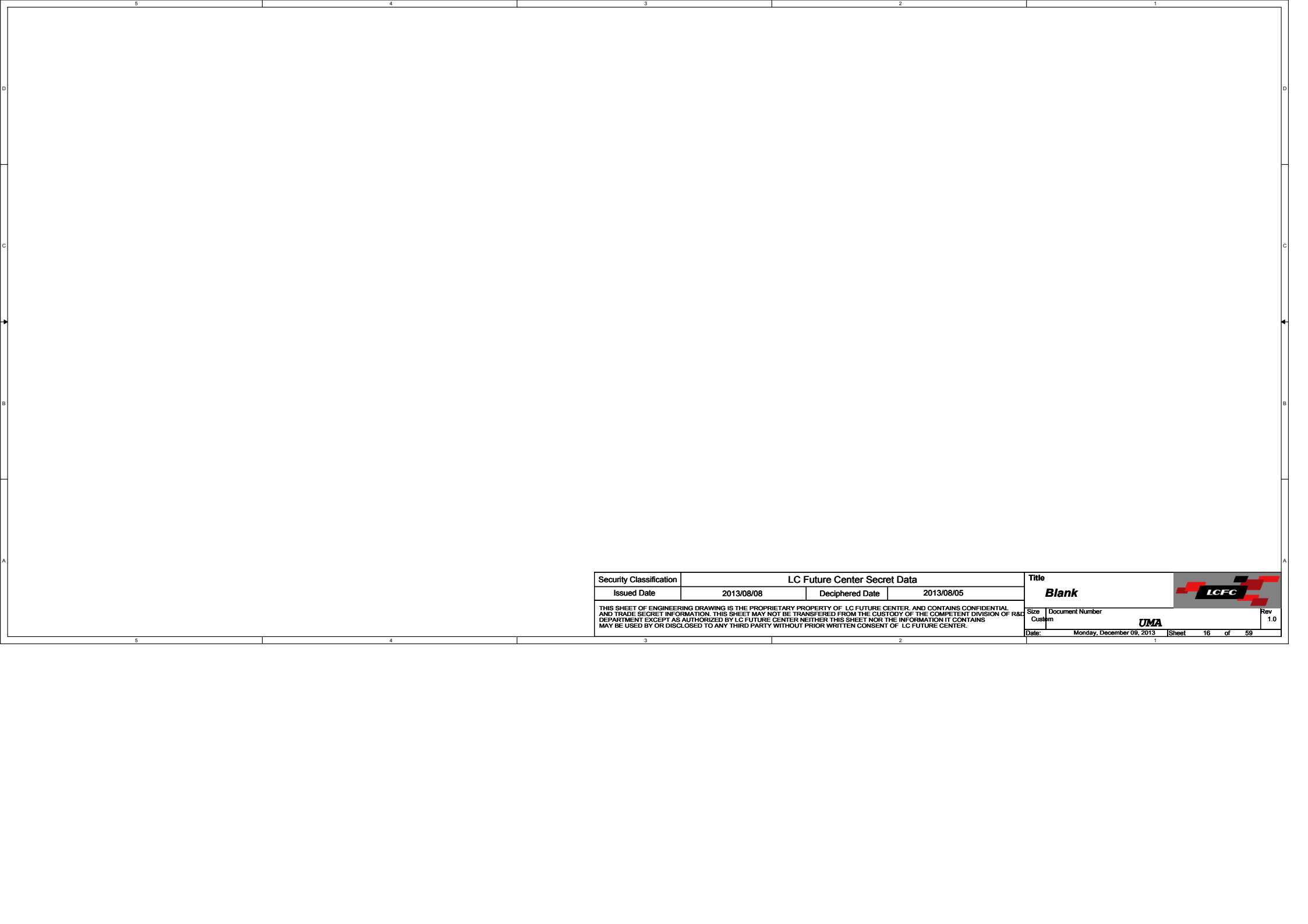
Layout Note:
Place near DIMM
(10U_0603_6.3V)*2
(.1U_0402_10V)*4




Pin Number	Pin Name	Net Name
5	DQ0	DDR8_DQ17
7	DQ1	DDR8_DQ23
15	DQ2	DDR8_DQ18
4	DQ3	DDR8_DQ21
17	DQ4	DDR8_DQ16
6	DQ5	DDR8_DQ22
16	DQ6	DDR8_DQ19
18	DQ7	DDR8_DQ20
10	DQS#0	DDR8_DQS#2
12	DQS#0	DDR8_DQS#2
21	DQ8	DDR8_DQ3
23	DQ9	DDR8_DQ5
33	DQ10	DDR8_DQ6
35	DQ11	DDR8_DQ1
22	DQ12	DDR8_DQ2
24	DQ13	DDR8_DQ4
34	DQ14	DDR8_DQ0
36	DQ15	DDR8_DQ7
27	DQS#1	DDR8_DQS#0
29	DQS#1	DDR8_DQS#0
39	DQ16	DDR8_DQ8
41	DQ17	DDR8_DQ10
51	DQ18	DDR8_DQ14
53	DQ19	DDR8_DQ15
40	DQ20	DDR8_DQ13
42	DQ21	DDR8_DQ12
50	DQ22	DDR8_DQ9
52	DQ23	DDR8_DQ11
45	DQS#2	DDR8_DQS#1
47	DQS#2	DDR8_DQS#1
57	DQ24	DDR8_DQ27
59	DQ25	DDR8_DQ26
67	DQ26	DDR8_DQ28
69	DQ27	DDR8_DQ24
56	DQ28	DDR8_DQ31
58	DQ29	DDR8_DQ30
68	DQ30	DDR8_DQ29
70	DQ31	DDR8_DQ25
62	DQS#3	DDR8_DQS#3
64	DQS#3	DDR8_DQS#3
129	DQ32	DDR8_DQ33
131	DQ33	DDR8_DQ36
141	DQ34	DDR8_DQ39
143	DQ35	DDR8_DQ38
130	DQ36	DDR8_DQ37
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140	DQ38	DDR8_DQ35
142	DQ39	DDR8_DQ34
135	DQS#4	DDR8_DQS#4
137	DQS#4	DDR8_DQS#4
147	DQ40	DDR8_DQ40
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160	DQ47	DDR8_DQ47
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154	DQS#5	DDR8_DQS#5
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176	DQ55	DDR8_DQ55
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183	DQ57	DDR8_DQ57
191	DQ58	DDR8_DQ59
193	DQ59	DDR8_DQ63
180	DQ60	DDR8_DQ56
182	DQ61	DDR8_DQ61
192	DQ62	DDR8_DQ58
194	DQ63	DDR8_DQ60
186	DQS#7	DDR8_DQS#7
188	DQS#7	DDR8_DQS#7



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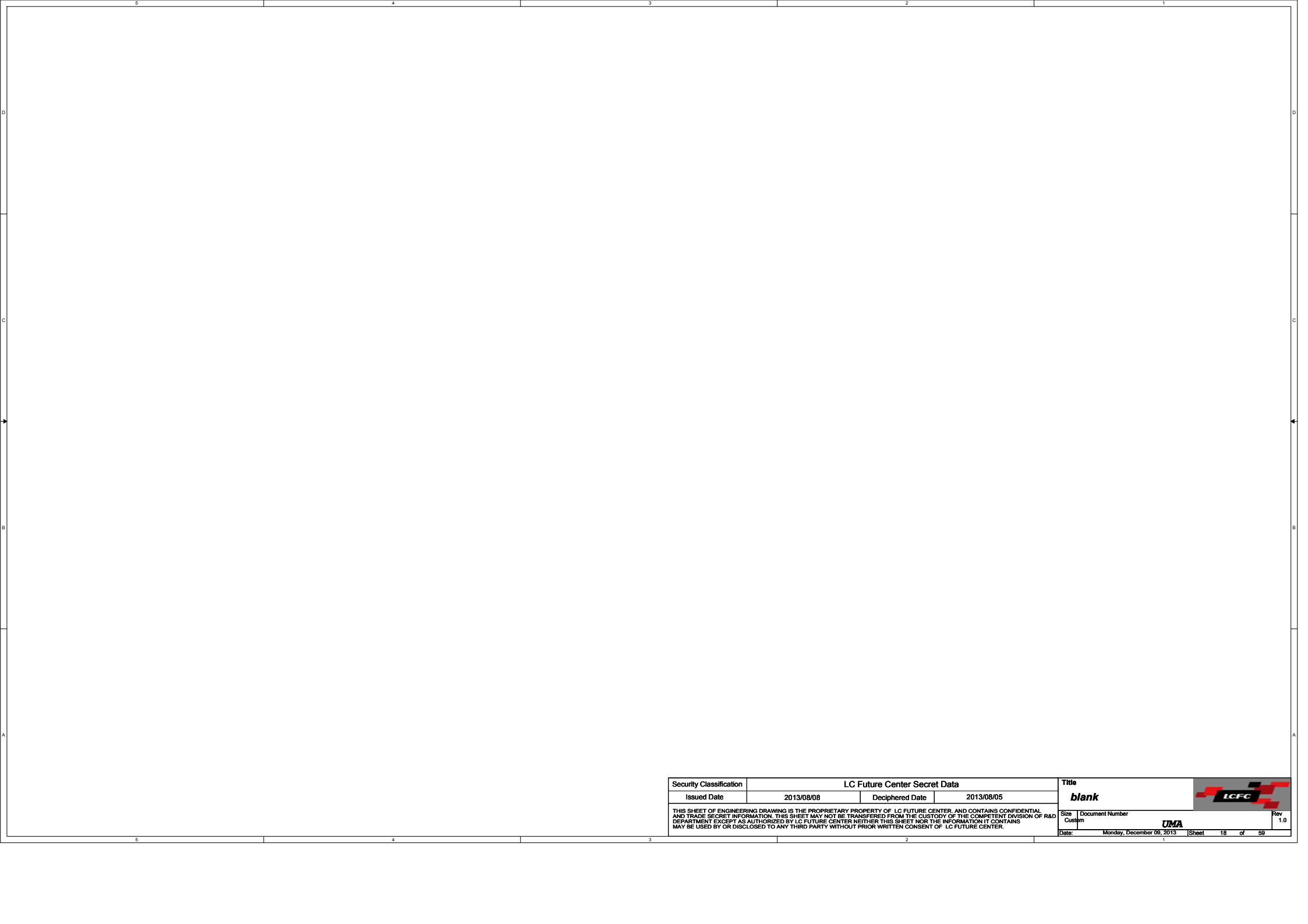
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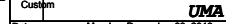
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Date:	Monday, December 09, 2013													
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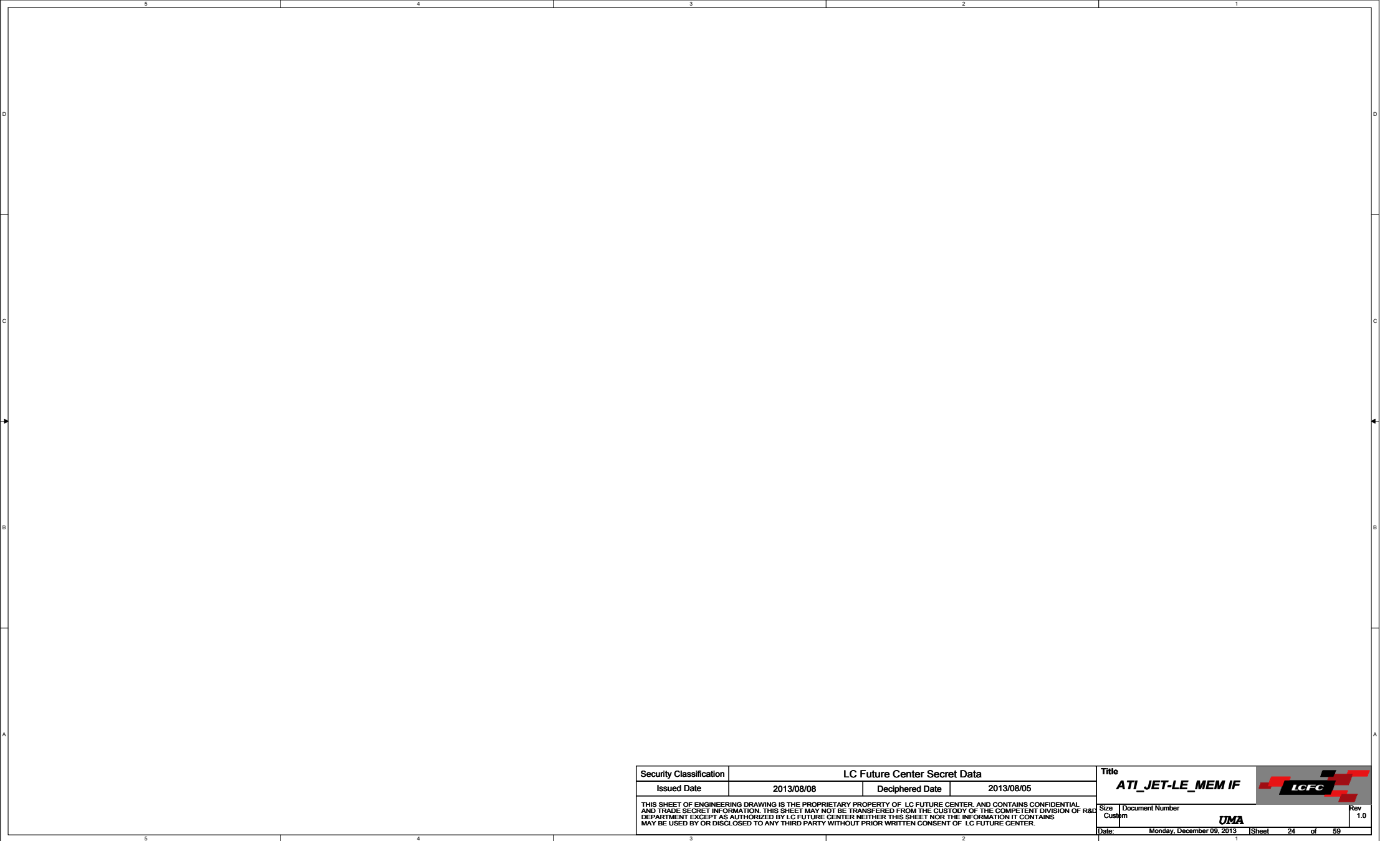
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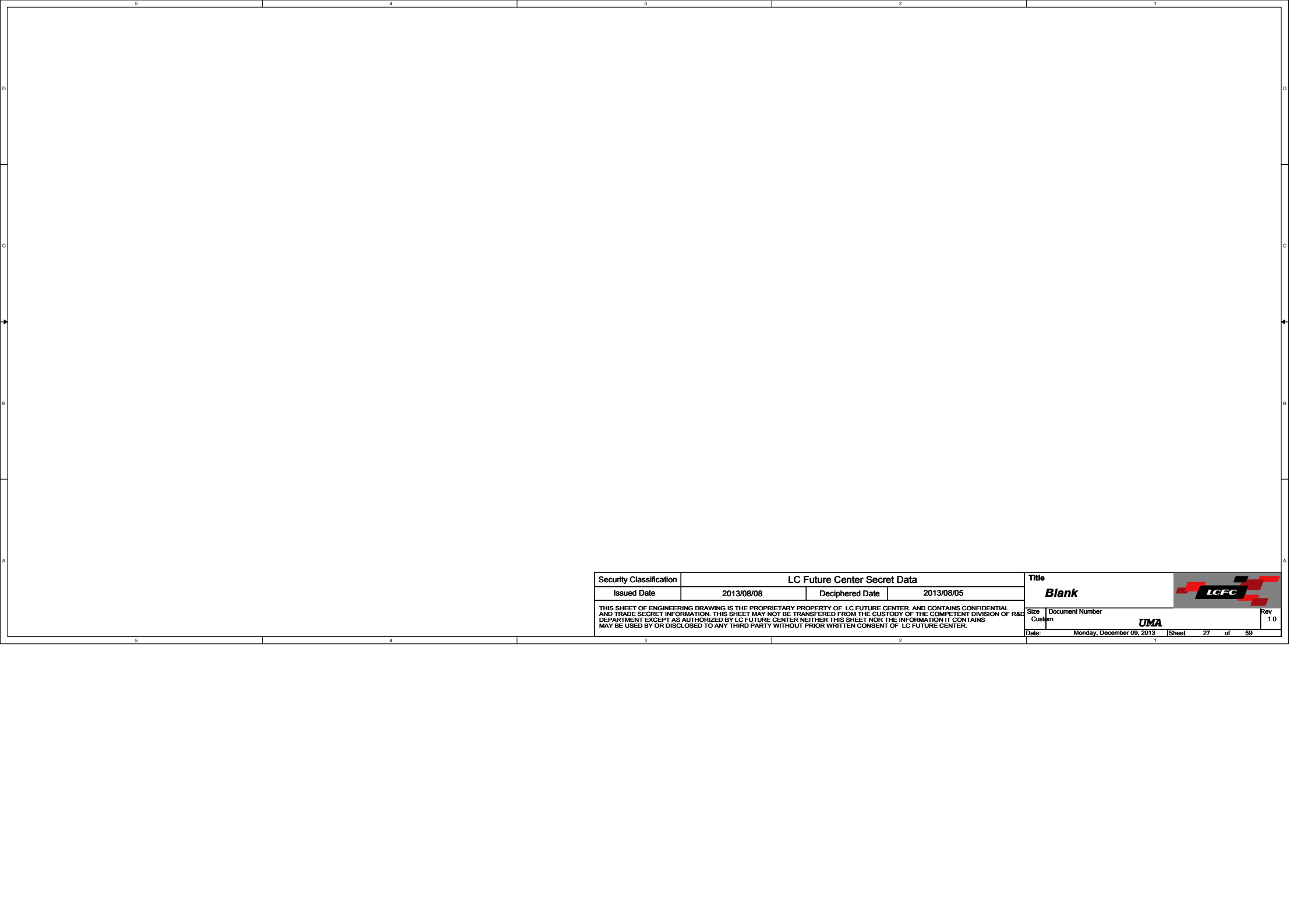
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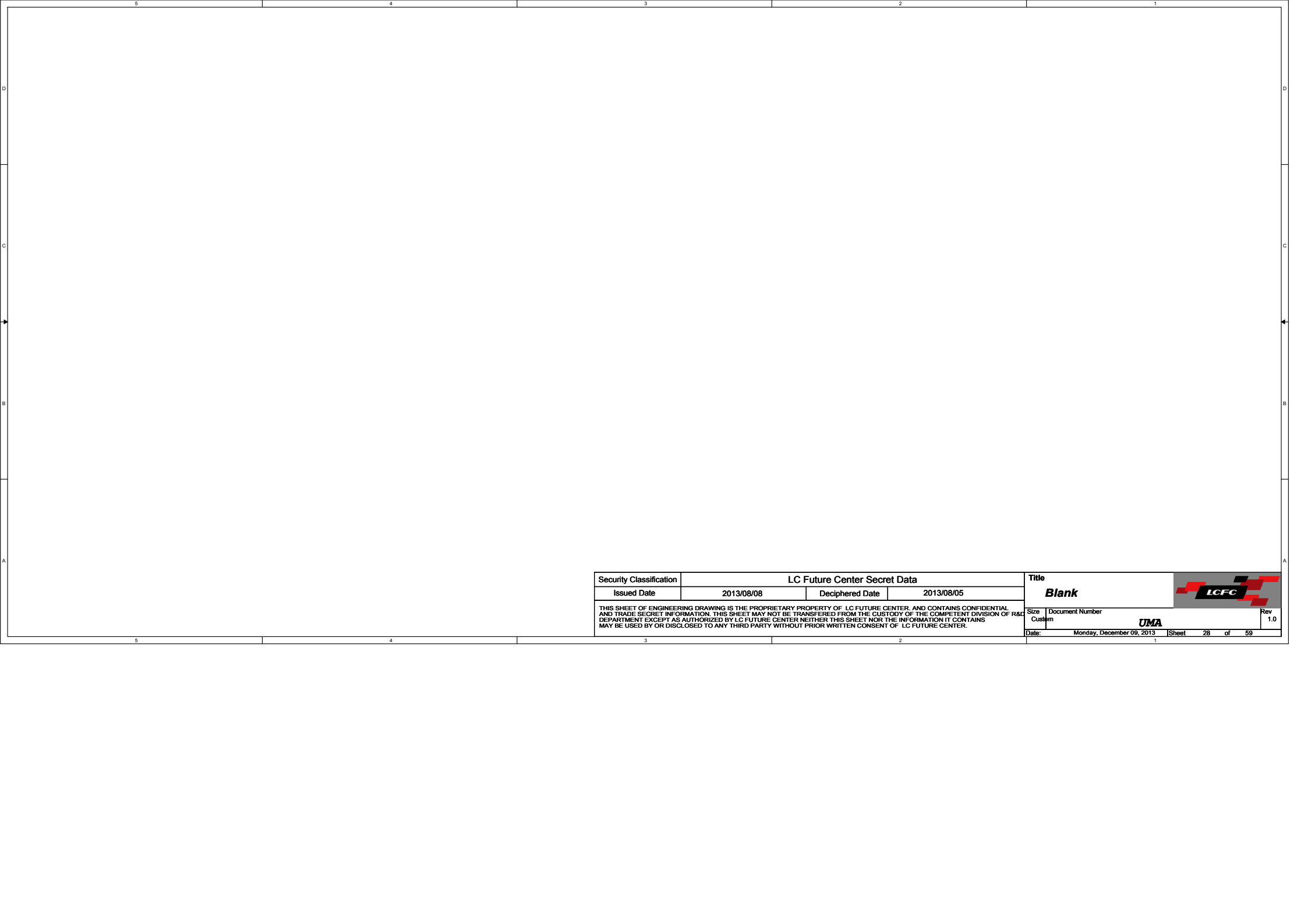
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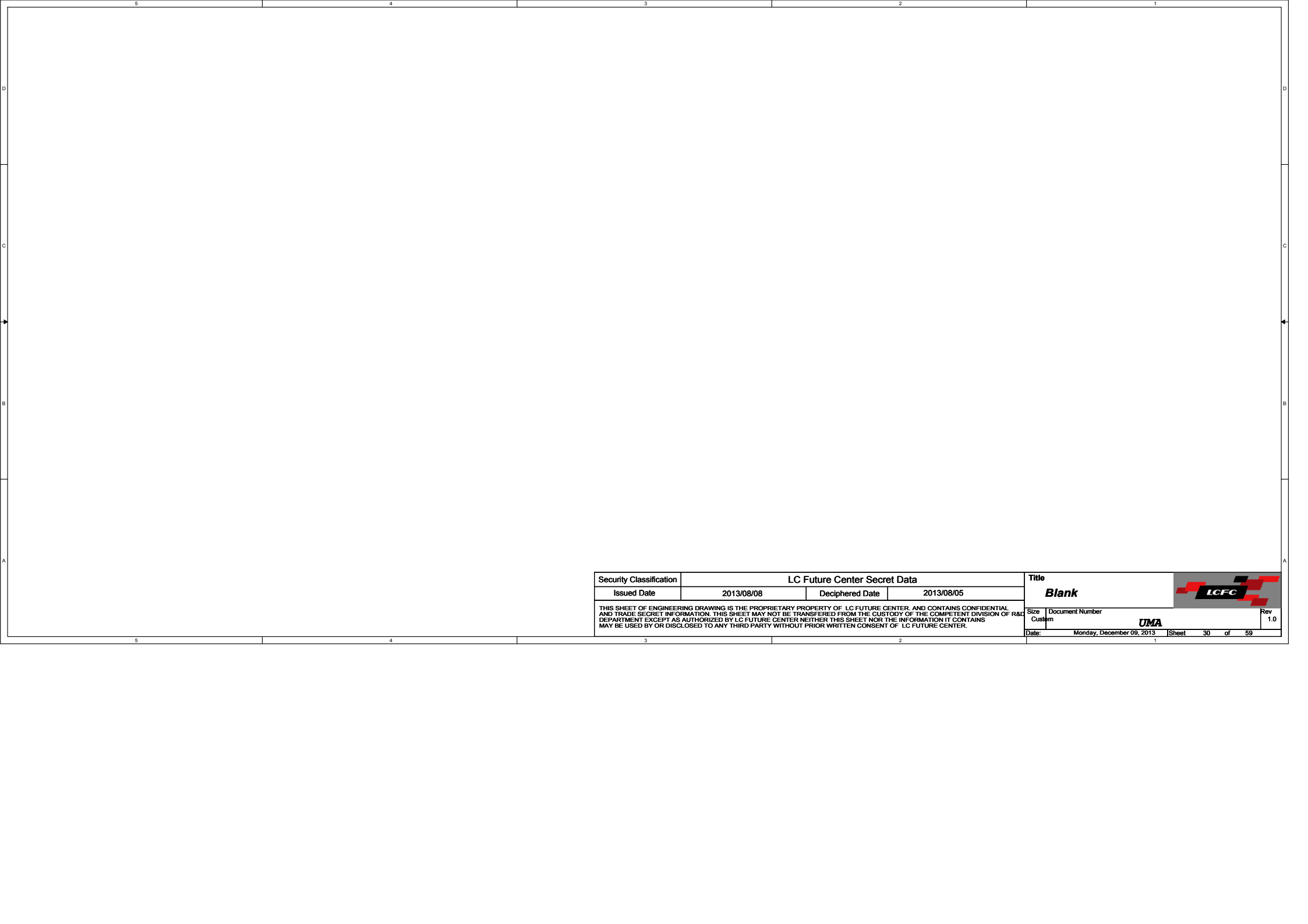



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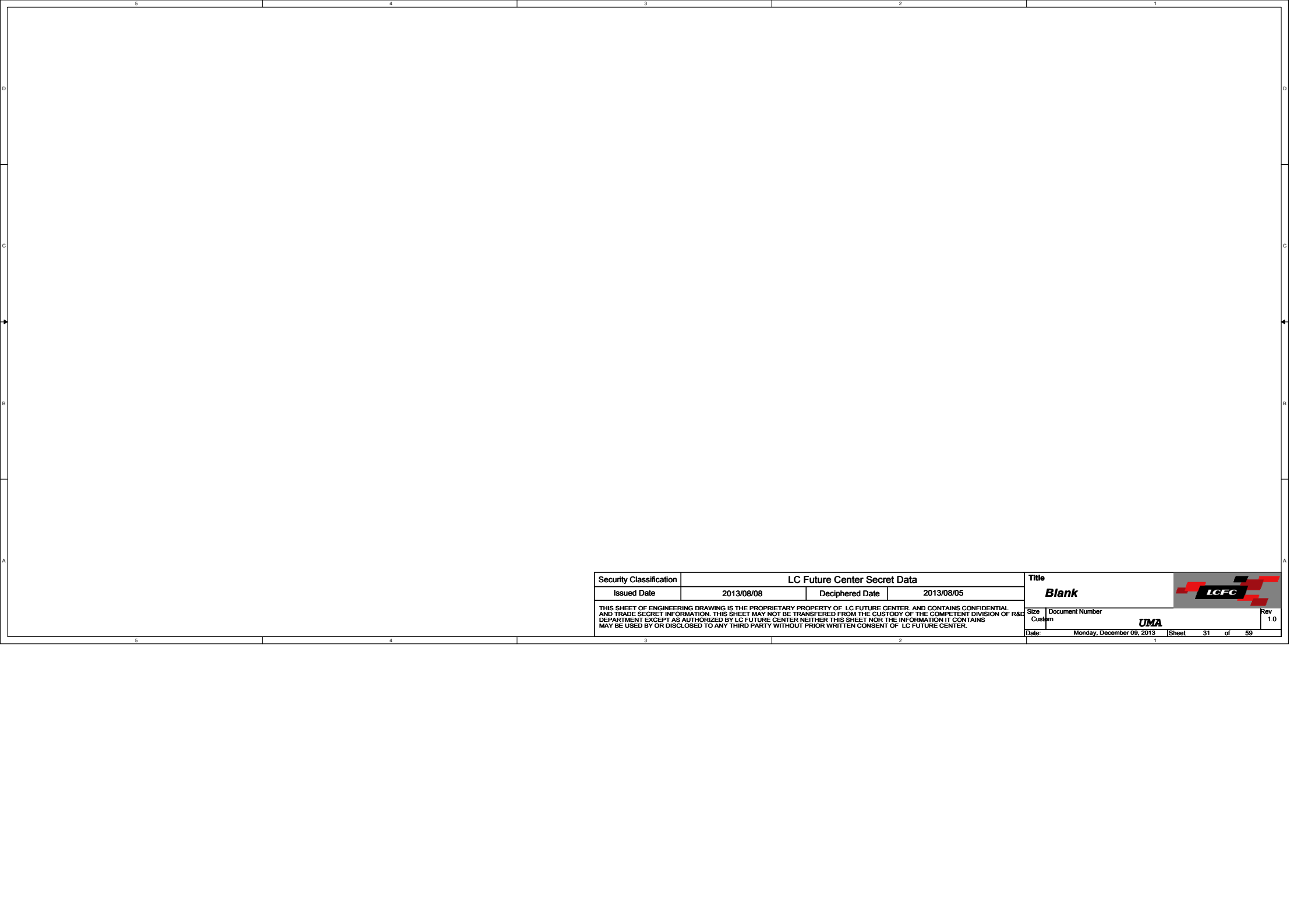



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				Date: Monday, December 09, 2013	Rev 1.0
				Sheet 28 of 59	

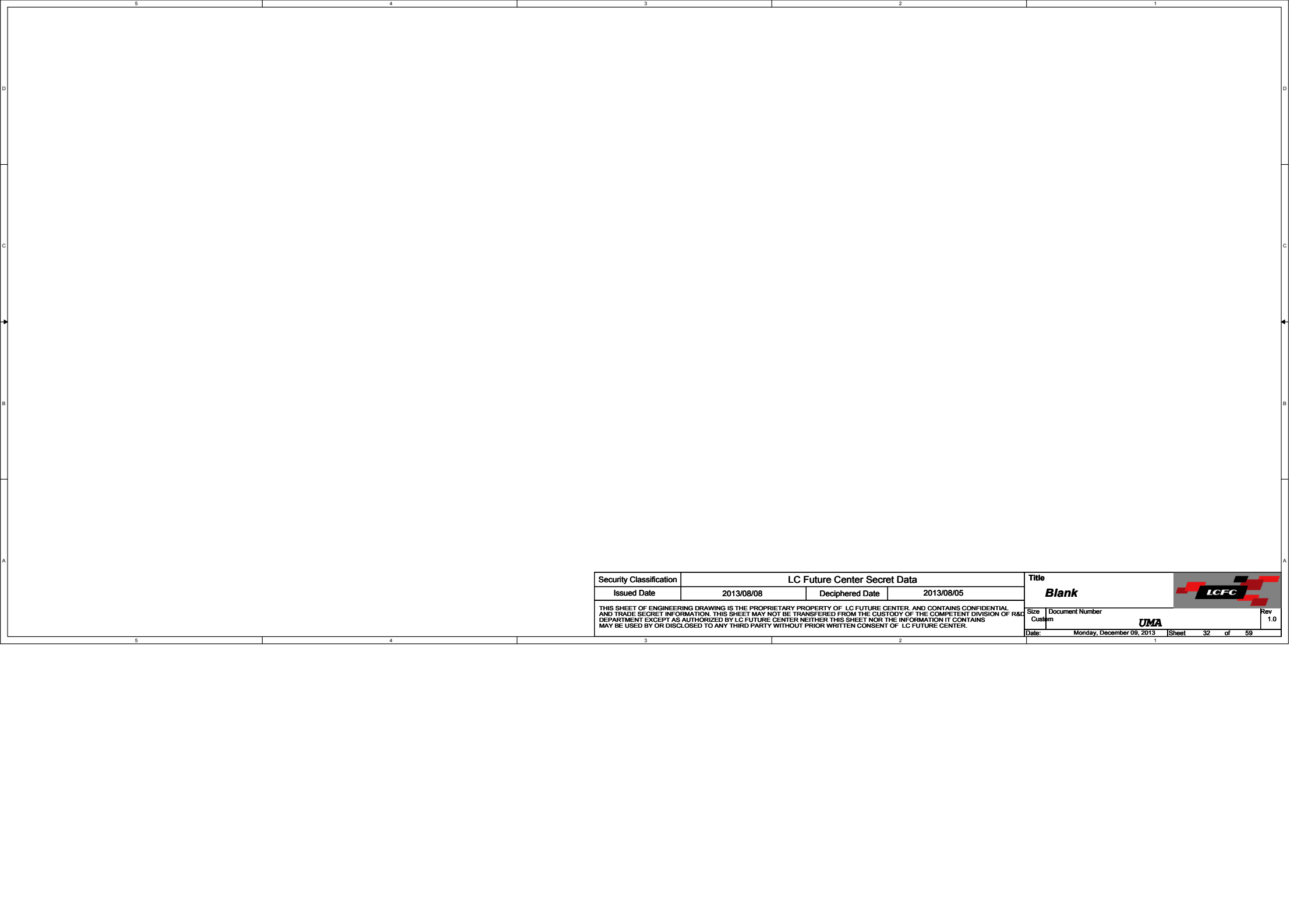
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A	B	C	D	A									
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Security Classification	LC Future Center Secret Data												
Issued Date	2013/08/08	Deciphered Date	2013/08/05										
<small>THIS SHEET OF ENGINEERING DRAWING IS THE PROPRIETARY PROPERTY OF LC FUTURE CENTER, AND CONTAINS CONFIDENTIAL AND TRADE SECRET INFORMATION. THIS SHEET MAY NOT BE TRANSFERRED FROM THE CUSTODY OF THE COMPETENT DIVISION OF R&D DEPARTMENT EXCEPT AS AUTHORIZED BY LC FUTURE CENTER. NEITHER THIS SHEET NOR THE INFORMATION IT CONTAINS MAY BE USED BY OR DISCLOSED TO ANY THIRD PARTY WITHOUT PRIOR WRITTEN CONSENT OF LC FUTURE CENTER.</small>				<table border="1"> <tr> <td>Size</td> <td>Document Number</td> <td>Rev</td> </tr> <tr> <td>Custom</td> <td>UMA</td> <td>1.0</td> </tr> </table>	Size	Document Number	Rev	Custom	UMA	1.0			
Size	Document Number	Rev											
Custom	UMA	1.0											
Date: Monday, December 09, 2013 Sheet 29 of 59													




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Issued Date	2013/08/08	Deciphered Date	2013/08/05		Title
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			Custom	UMA	1.0
			Date:	Monday, December 09, 2013	Sheet 30 of 59

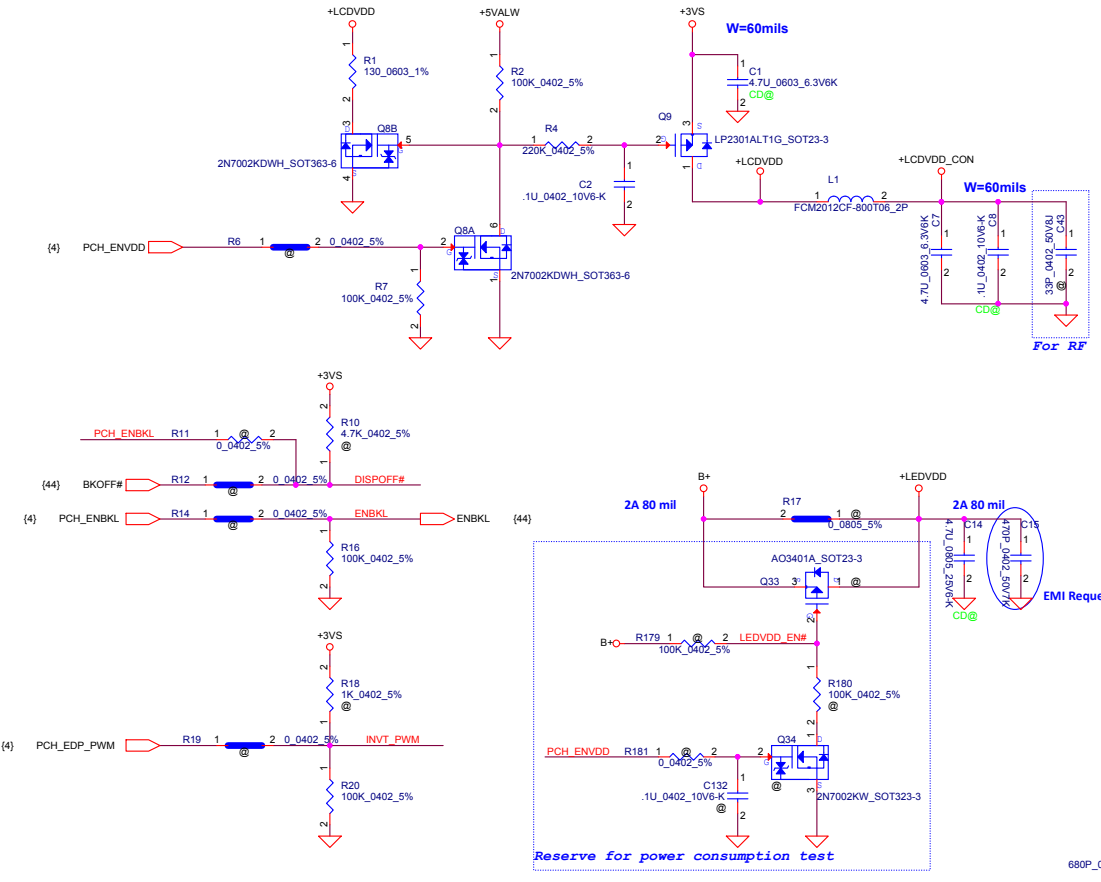


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Issued Date	2013/08/08	Deciphered Date	2013/08/05	Blank	
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				Date: Monday, December 09, 2013	Rev 1.0
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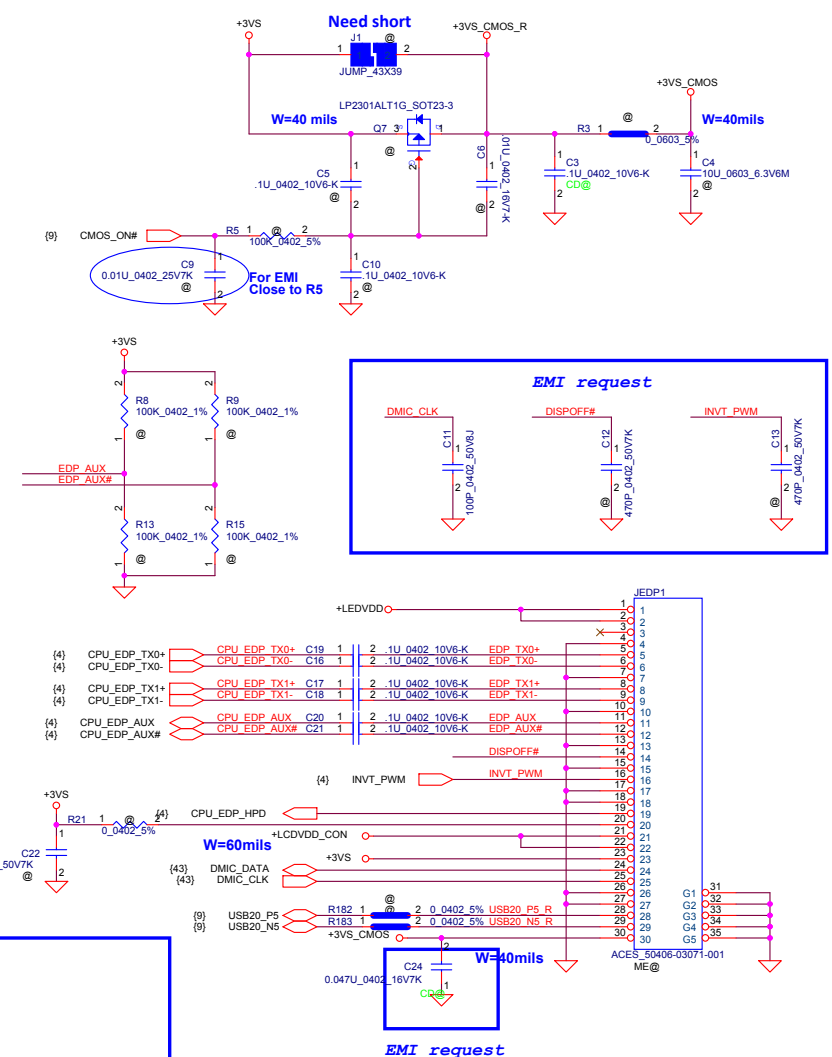


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				Date: Monday, December 09, 2013	Rev 1.0
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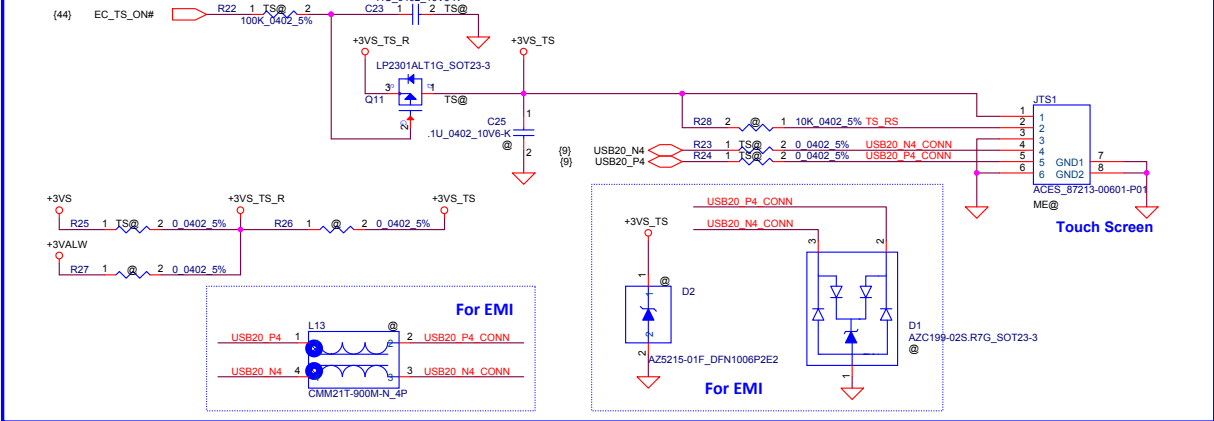
LCD POWER CIRCUIT



CMOS Camera



Touch Screen

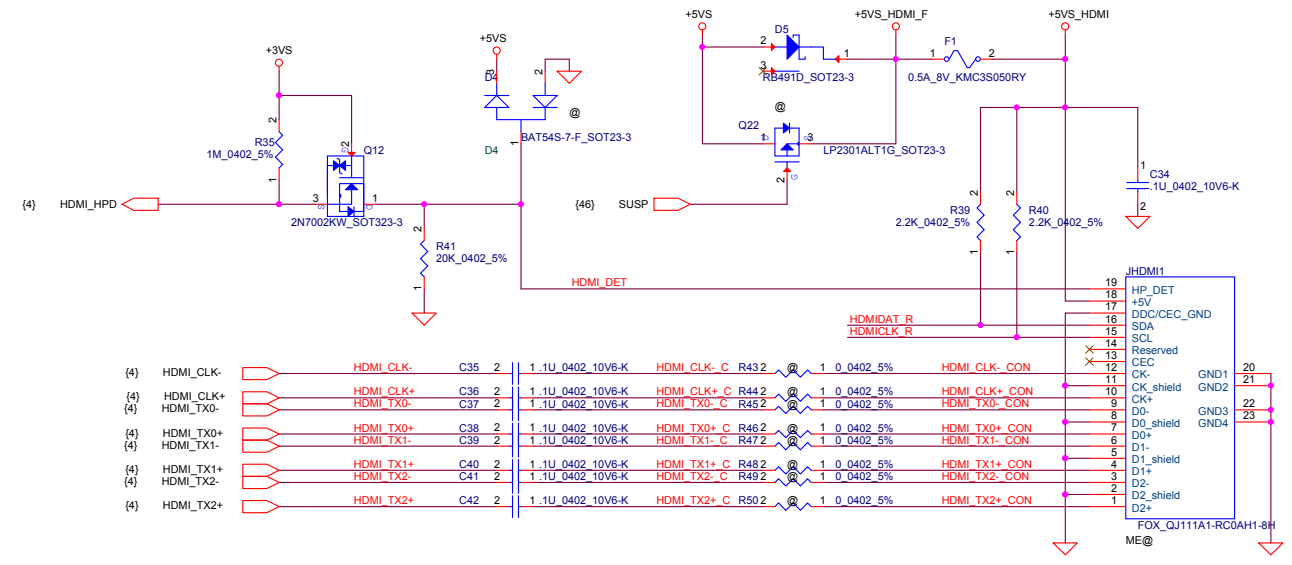
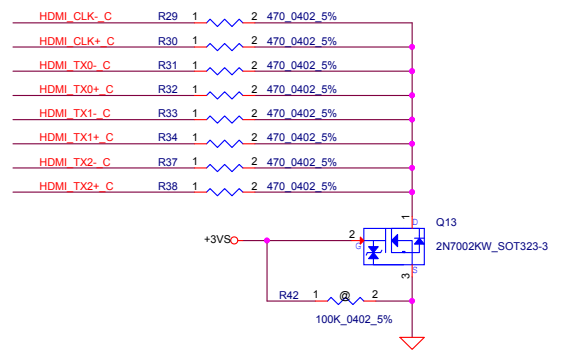
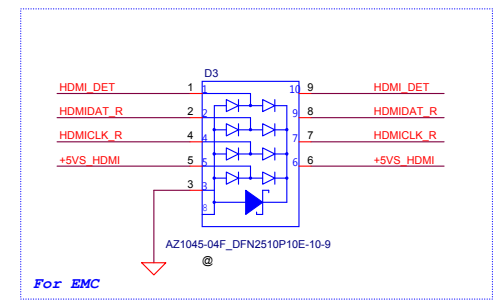
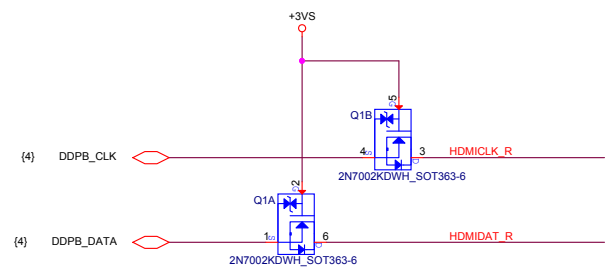
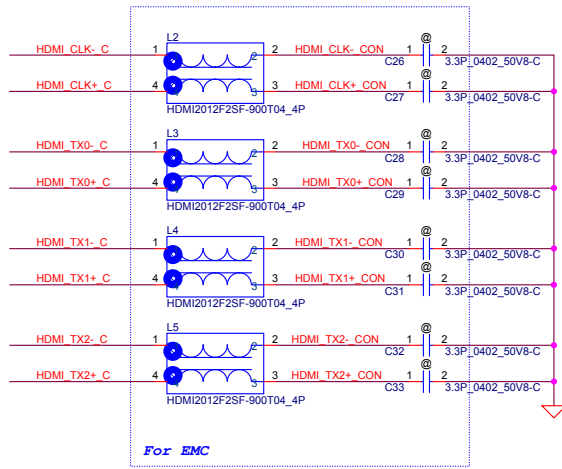


Security Classification		LC Future Center Secret Data		Title	
Issued Date		2013/08/08		eDP/ CMOS/Touch screen	
Deciphered Date		2013/08/05		Size	
				Document Number	
				Custom	
				Date	
				Monday, December 09, 2013	
				Sheet 33 of 59	
				Rev 1.0	

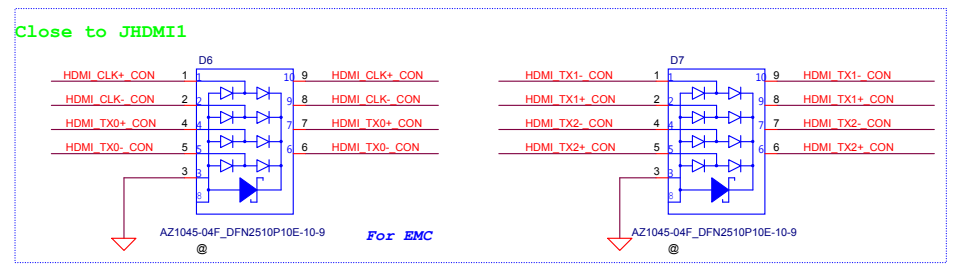
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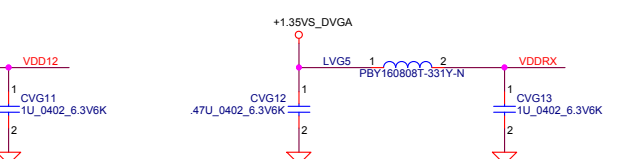
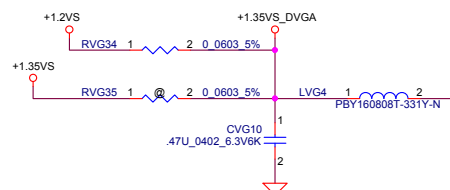
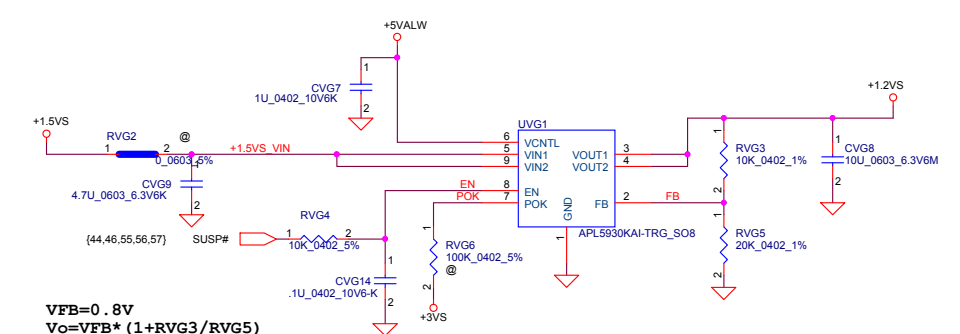
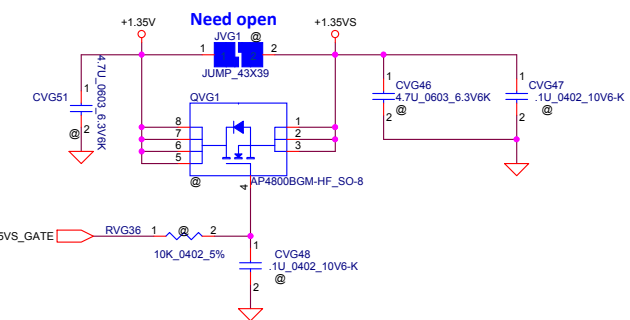
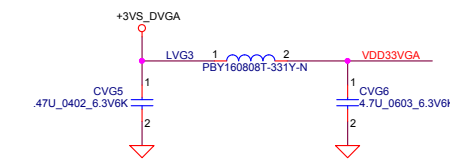
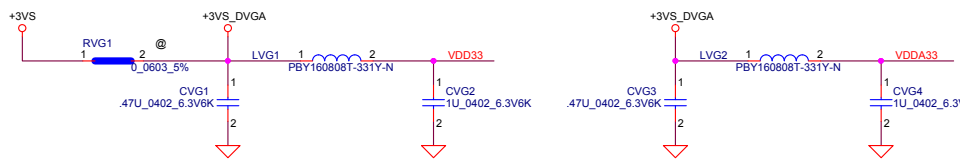
UMA



(4)	HDMI_CLK-	HDMI_CLK-	C35	2	1.1U_0402_10V6-K	HDMI_CLK- C	R43	2	@	1	0	0402_5%	HDMI_CLK- CON	
(4)	HDMI_CLK+	HDMI_CLK+	C36	2	1.1U_0402_10V6-K	HDMI_CLK+ C	R44	2	@	1	0	0402_5%	HDMI_CLK+ CON	
(4)	HDMI_TX0-	HDMI_TX0-	C37	2	1.1U_0402_10V6-K	HDMI_TX0- C	R45	2	@	1	0	0402_5%	HDMI_TX0- CON	
(4)	HDMI_TX0+	HDMI_TX0+	C38	2	1.1U_0402_10V6-K	HDMI_TX0+ C	R46	2	@	1	0	0402_5%	HDMI_TX0+ CON	
(4)	HDMI_TX1-	HDMI_TX1-	C39	2	1.1U_0402_10V6-K	HDMI_TX1- C	R47	2	@	1	0	0402_5%	HDMI_TX1- CON	
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(4)	HDMI_TX2-	HDMI_TX2-	C41	2	1.1U_0402_10V6-K	HDMI_TX2- C	R49	2	@	1	0	0402_5%	HDMI_TX2- CON	
(4)	HDMI_TX2+	HDMI_TX2+	C42	2	1.1U_0402_10V6-K	HDMI_TX2+ C	R50	2	@	1	0	0402_5%	HDMI_TX2+ CON	



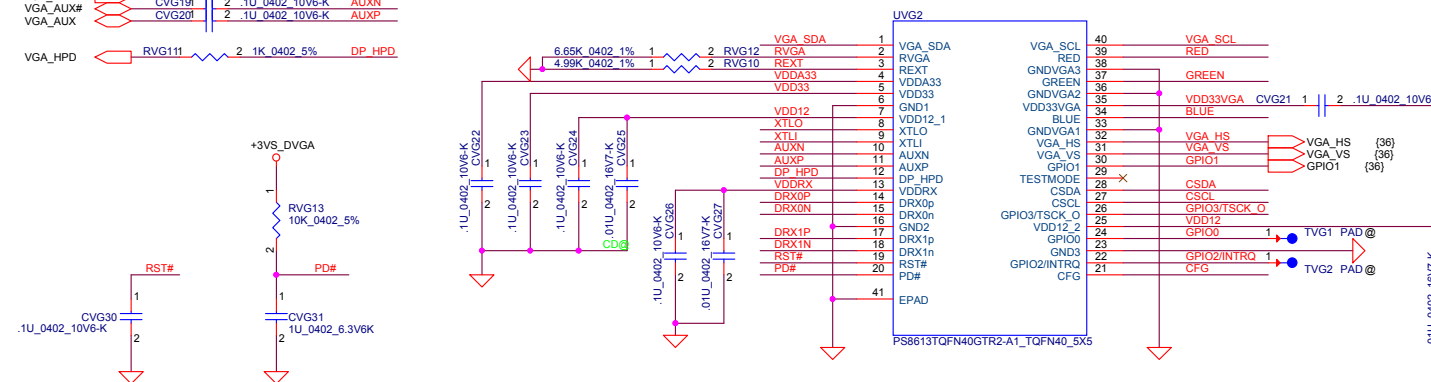
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Issued Date		2013/08/08		Deciphered Date		2013/08/05		Size		Document Number	
								Custom		UMA	
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Date: Monday, December 09, 2013								Sheet		34 of 59	



VFB=0.8V
 $V_o = VFB * (1 + RVG3 / RVG5)$
 OCP: Min 4A

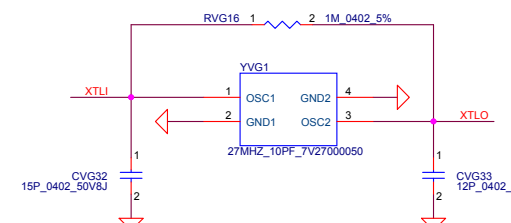
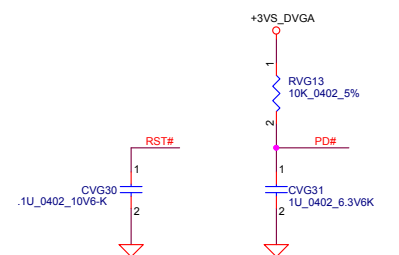
- (4) VGA_TX0- CVG151 2 .1U 0402 10V6-K DRX0N
- (4) VGA_TX0+ CVG151 2 .1U 0402 10V6-K DRX0P
- (4) VGA_TX1- CVG171 2 .1U 0402 10V6-K DRX1N
- (4) VGA_TX1+ CVG171 2 .1U 0402 10V6-K DRX1P
- (4) VGA_AUX# CVG151 2 .1U 0402 10V6-K AUXN
- (4) VGA_AUX CVG201 2 .1U 0402 10V6-K AUXP

- (4) VGA_HPD RVG111 2 1K 0402 5% DP_HPD



Initial code loading selection, internal pull down ~80kΩ:
 L: Loading initial code from internal MTP ROM
 H: No initial code loading, external I2C control is expected

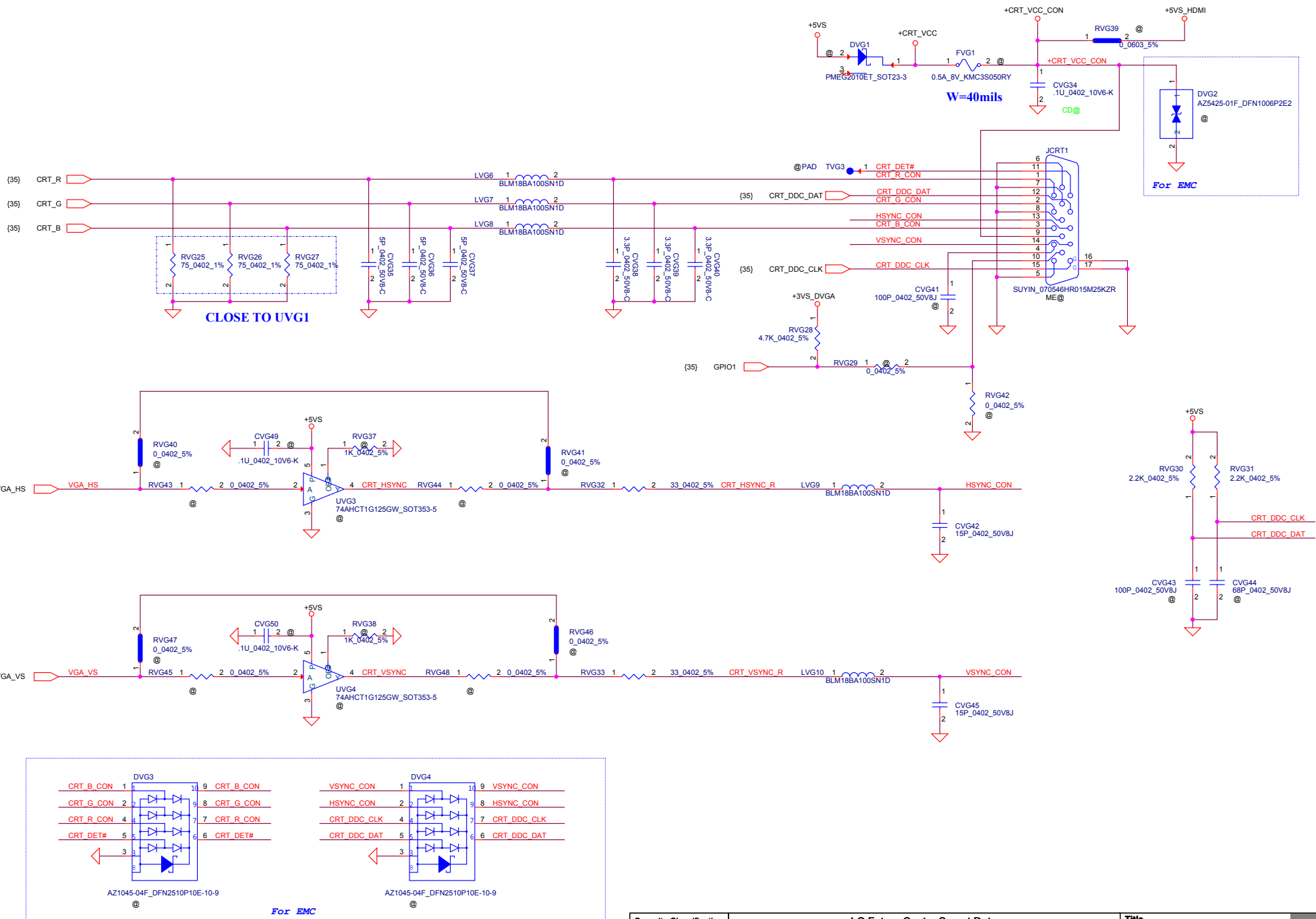
I2C address, 3-state inputs:
 L: 0x50h ~ 0x6Fh
 M: 0x90h ~ 0xAfh
 H: 0x30h ~ 0x4Fh



- RED RVG17 1 2 10 0402 5% CRT_R (36)
- GREEN RVG18 1 2 10 0402 5% CRT_G (36)
- BLUE RVG20 1 2 10 0402 5% CRT_B (36)
- VGA_SCL RVG231 2 0 0402 5% CRT_DDC_CLK (36)
- VGA_SDA RVG241 2 0 0402 5% CRT_DDC_DAT (36)

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CRT Connector



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		2013/08/05
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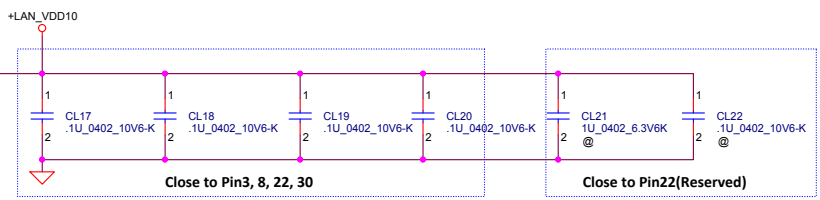
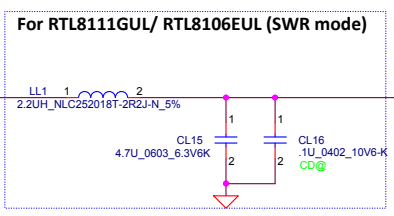
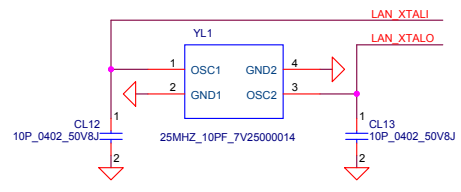
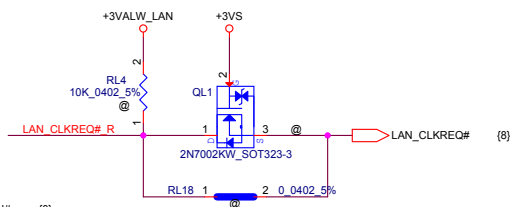
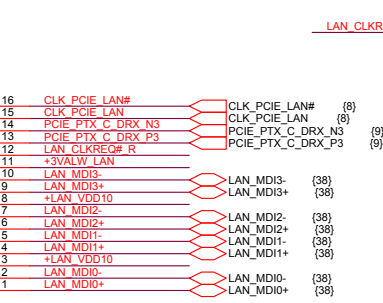
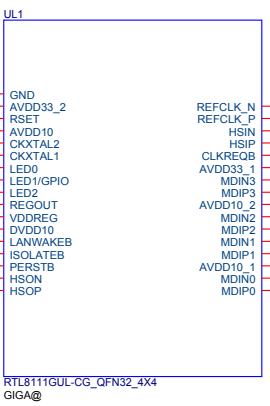
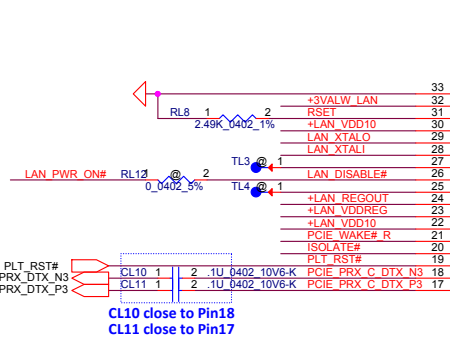
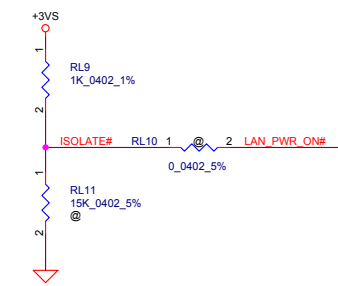
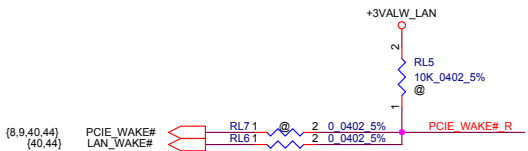
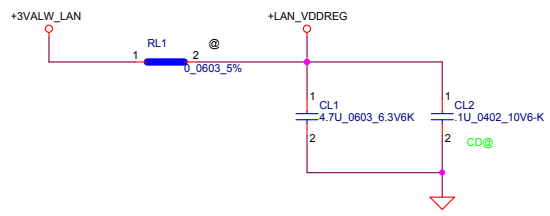
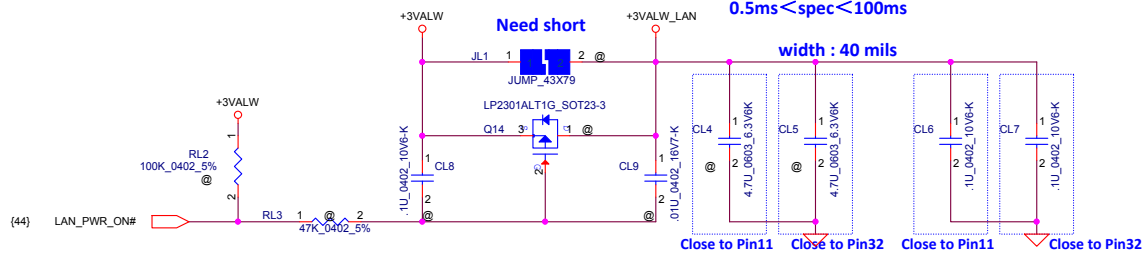
Title	Size	Document Number	Rev
CRT	Custom		1.0
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UMA

+3VALW TO +3VALW_LAN

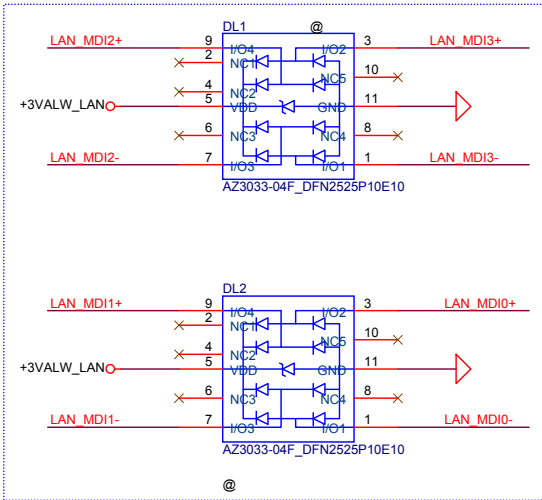
**+3VALW_LAN rising time (10%~90%):
0.5ms < spec < 100ms**



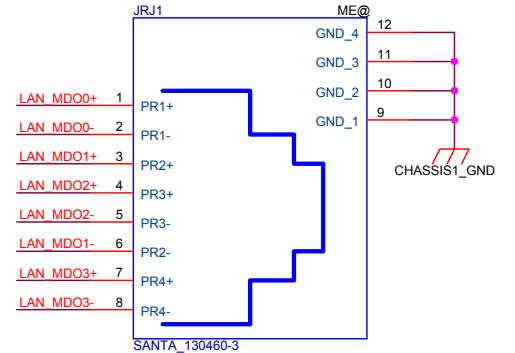
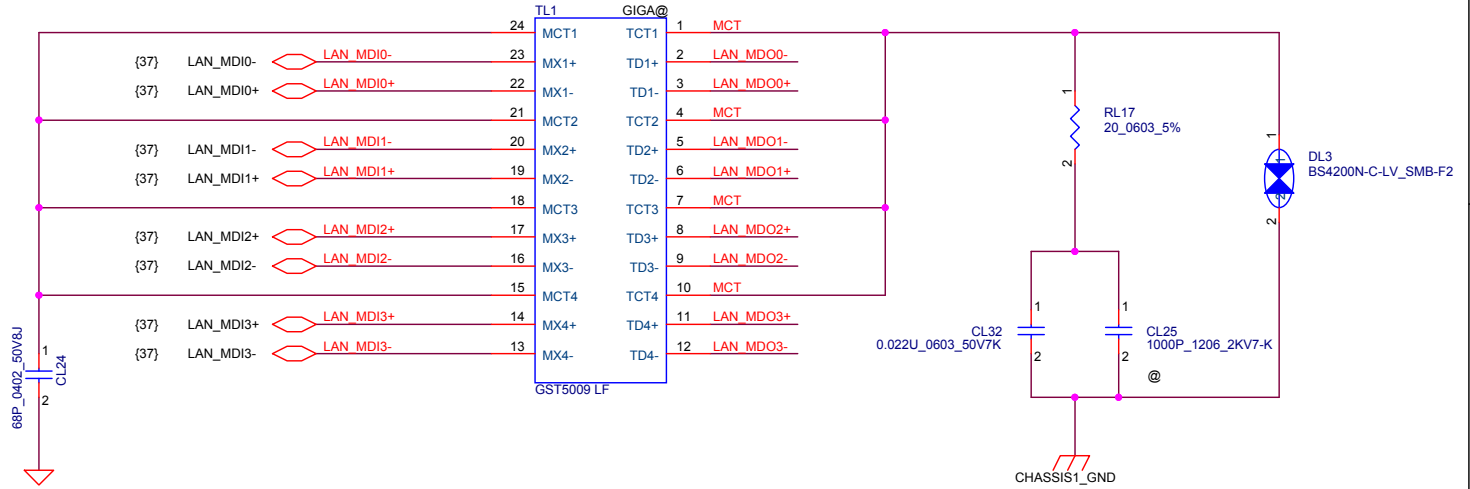
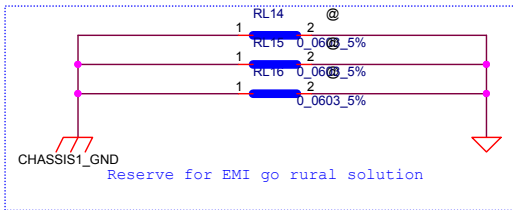
Layout Note: LL1 must be within 200mil to Pin36.
CL15, CL16 must be within 200mil to LL1.
+LAN_REGOUT: Width = 60mil

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Size Custom	Document Number	UMA		Rev	1.0
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DL1/DL2
1'S PN:SC300003M00

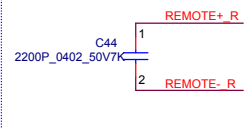


Place Close to TL1

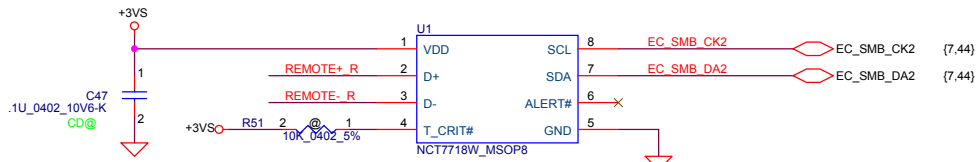


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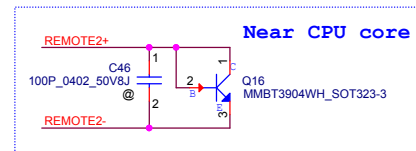
Close to U1



SMSC thermal sensor placed near DIMM



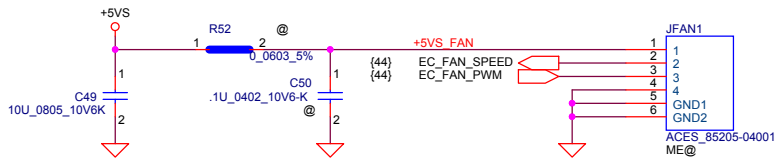
Address 1001_100xb



REMOTE2+ R176 1 @ 2 0.0402 5% REMOTE+ R
 REMOTE2- R177 1 @ 2 0.0402 5% REMOTE- R

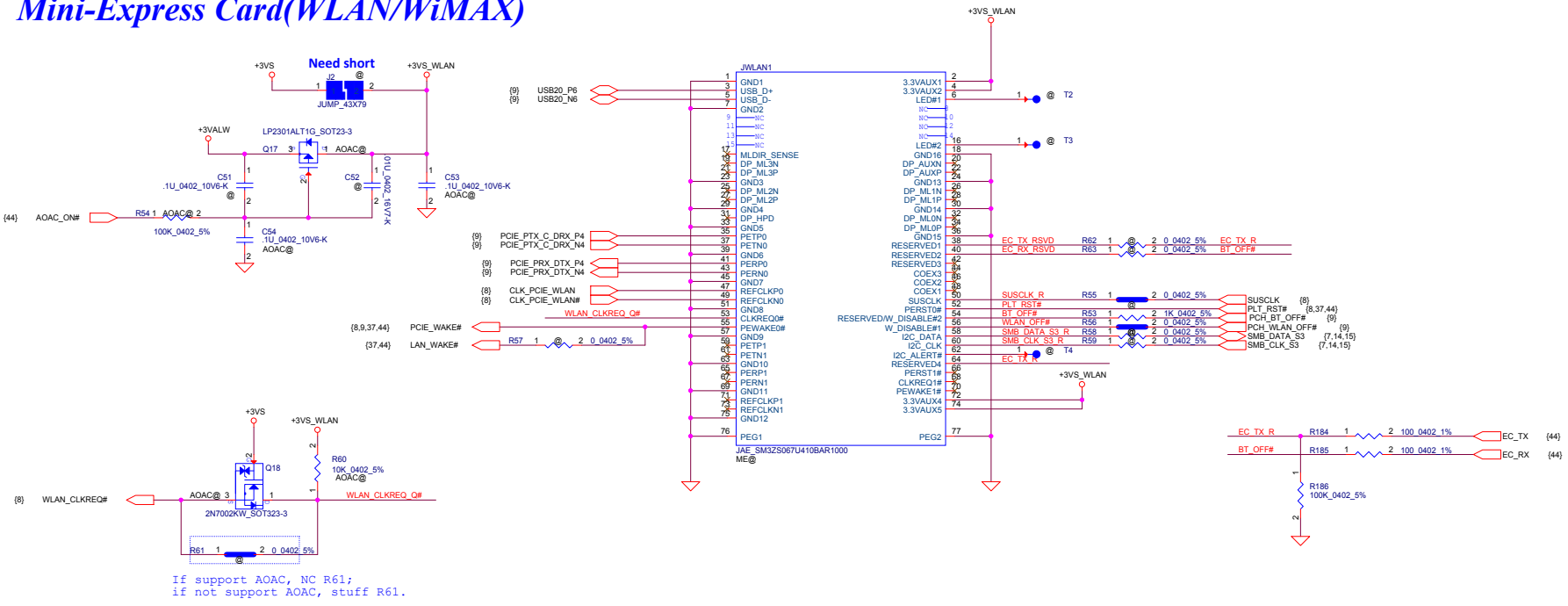
REMOTE+/- R, REMOTE1+/-, REMOTE2+/-:
 Trace width/space:10/10 mil
 Trace length:<8"


FAN Conn



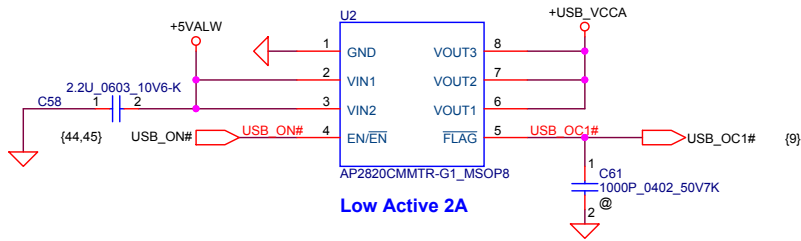
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Issued Date	2013/08/08	Deciphered Date	2013/08/05	
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Mini-Express Card(WLAN/WiMAX)

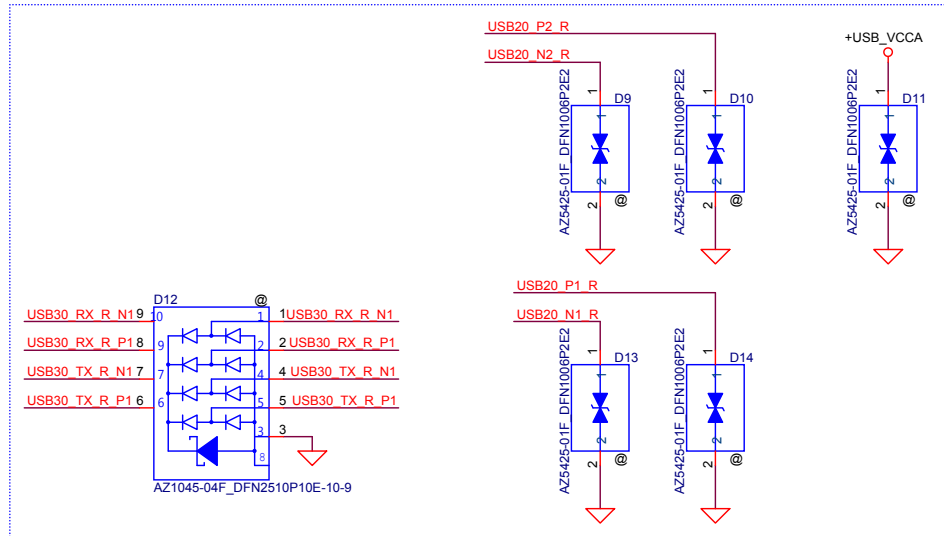
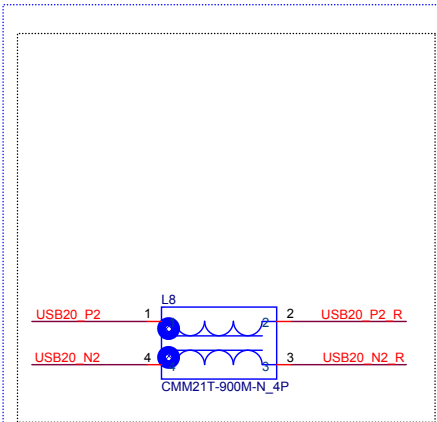
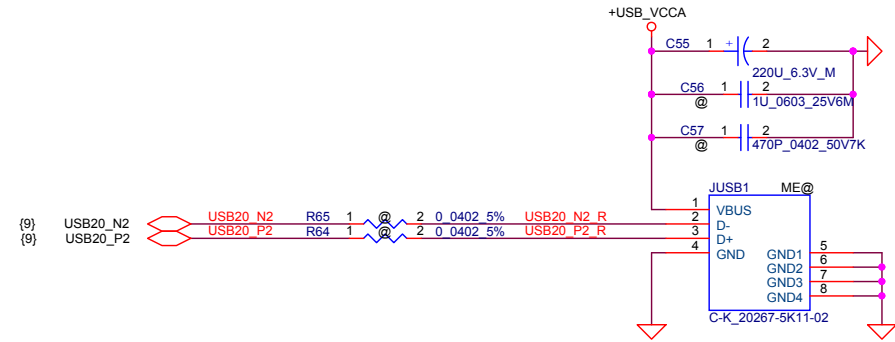


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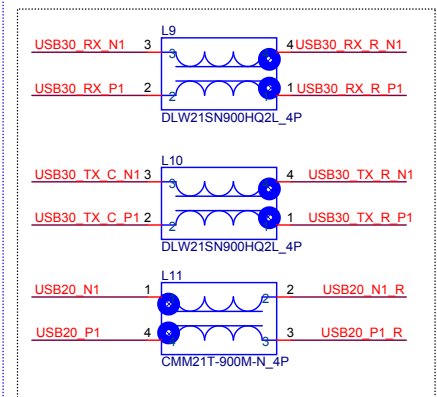
LEFT SIDE USB3.0 PORT X2



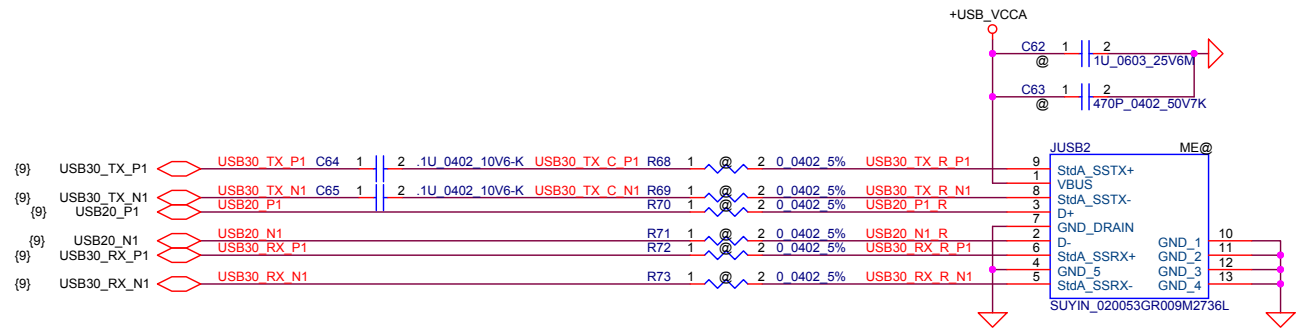
Low Active 2A



For EMC



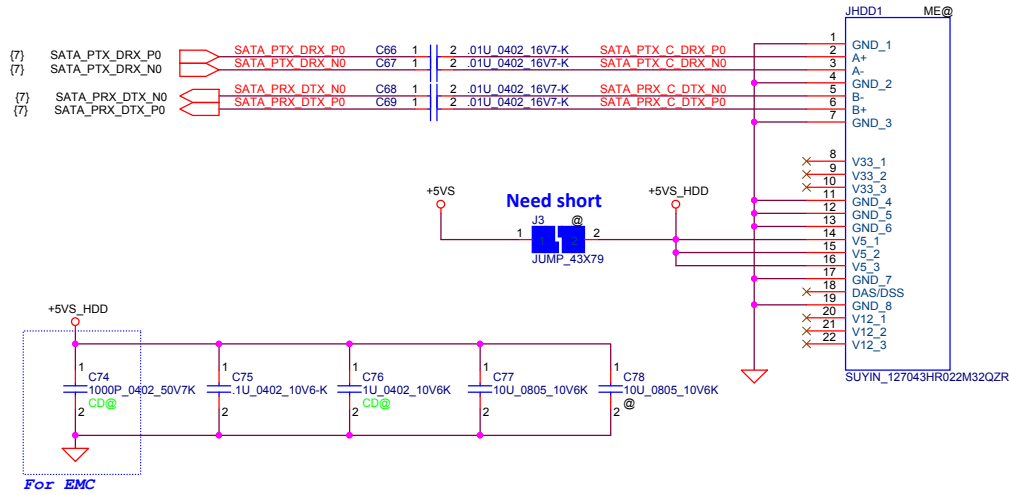
For EMC



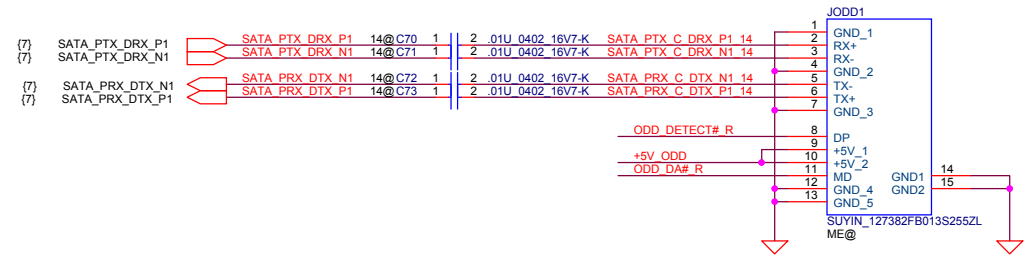
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Size	Document Number	
Custom		
Date:	Monday, December 09, 2013	Sheet 41 of 59

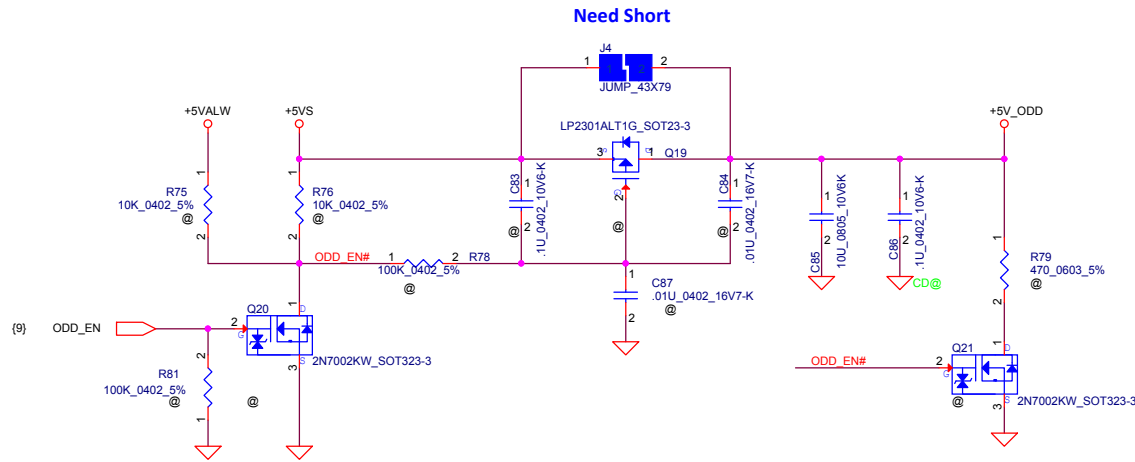
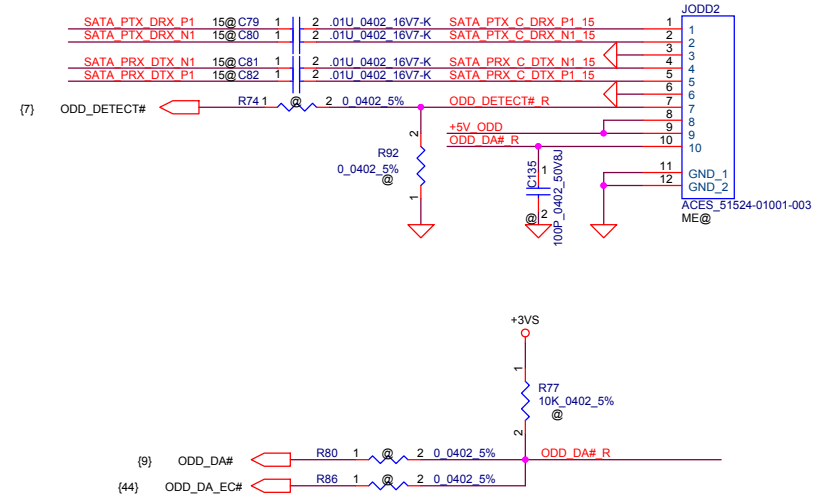
SATA HDD Conn.



FOR 14" SATA ODD Conn.

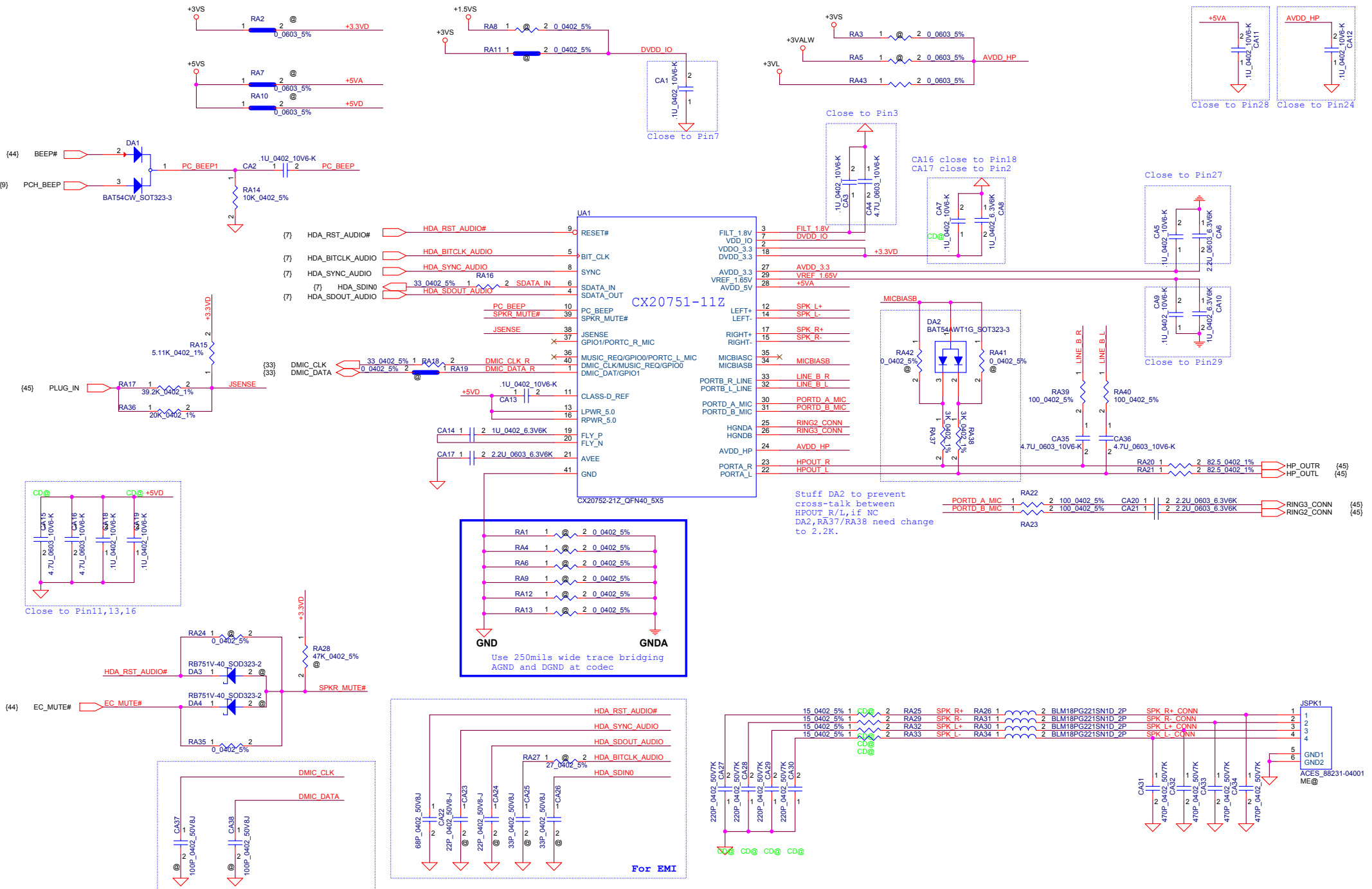


FOR 15" SATA ODD FFC Conn



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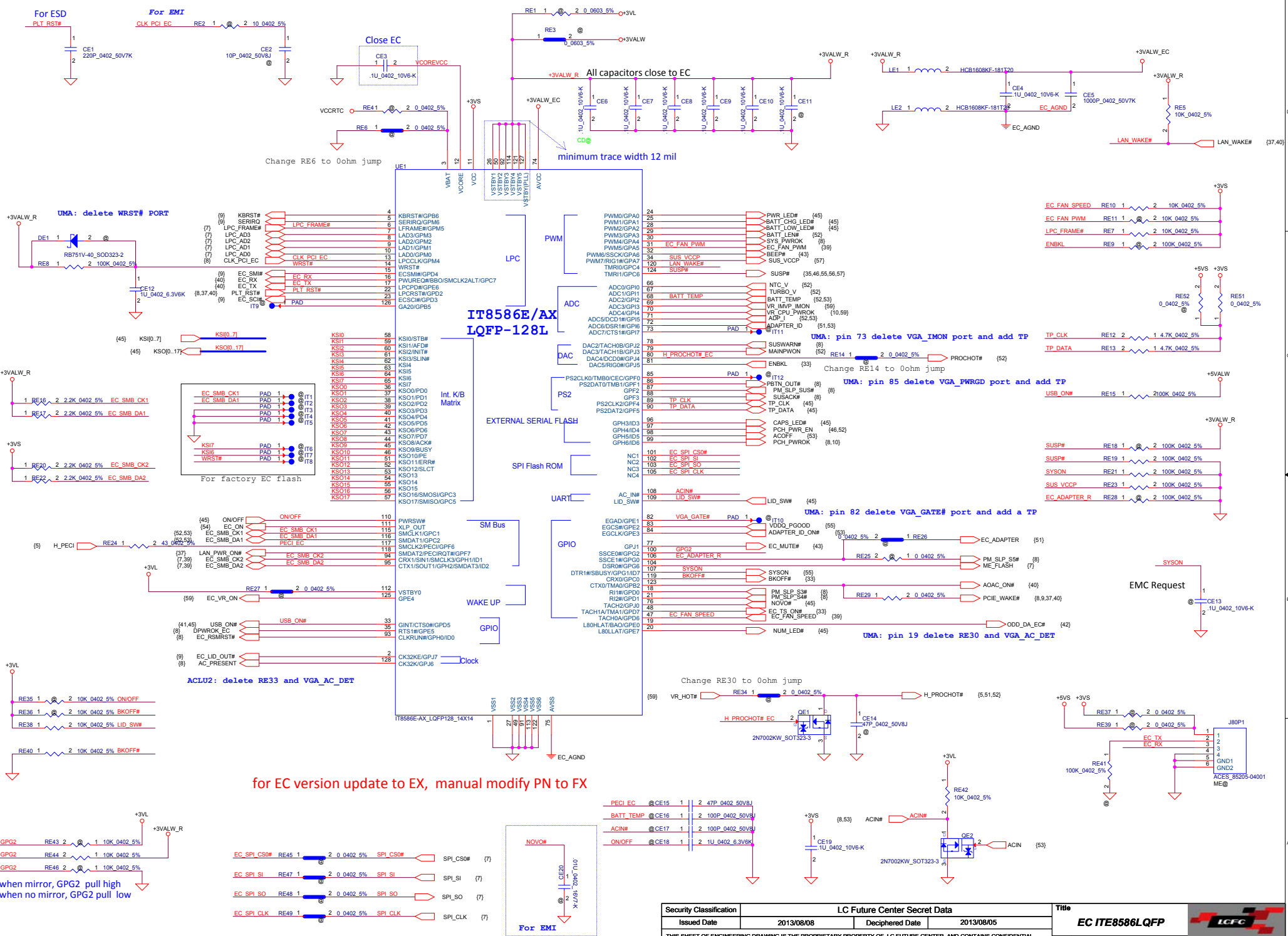
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Size	Document Number	Rev	1.0
Custom		UMA	
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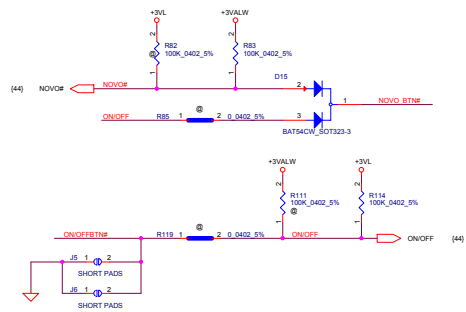
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Codec_CX20752		Document Number	Rev
Date: Monday, December 09, 2013		Sheet 43 of 59	1.0



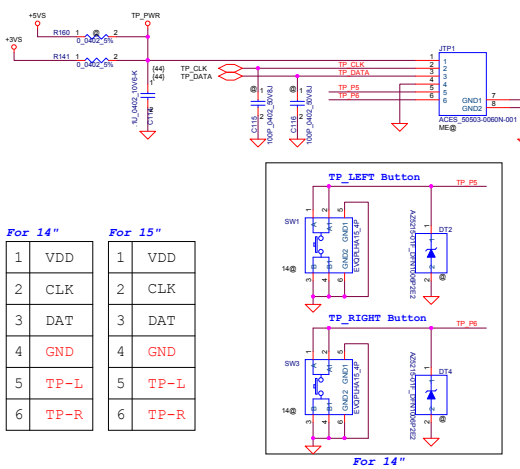


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Date	Monday, December 09, 2013	Sheet	44	of	59

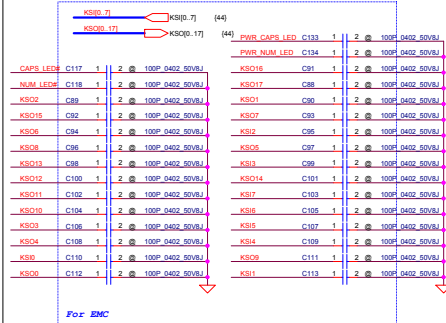
ON/OFF switch



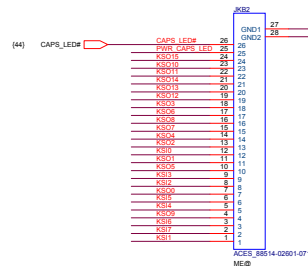
TP/B Connector



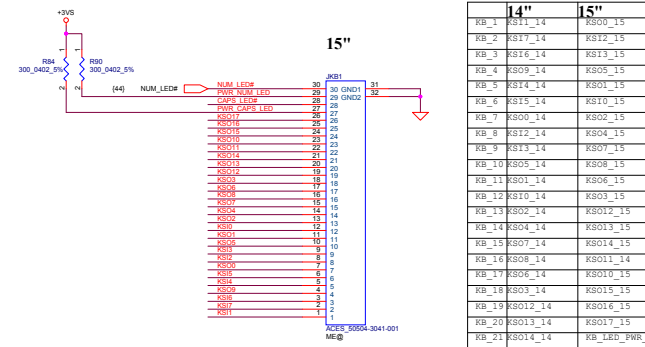
K/B Connector



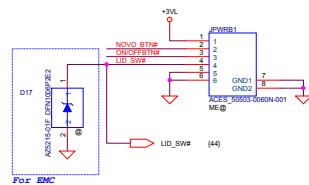
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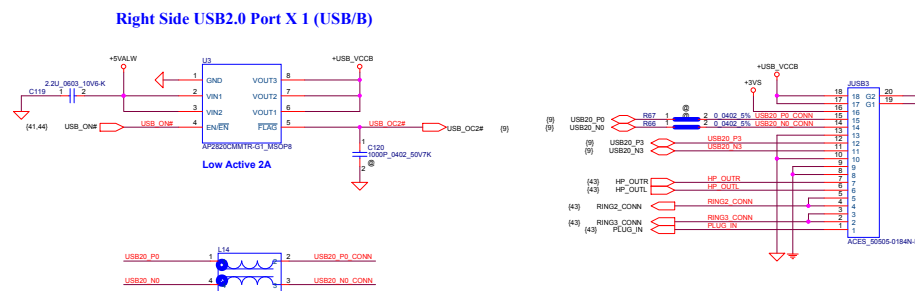
15"



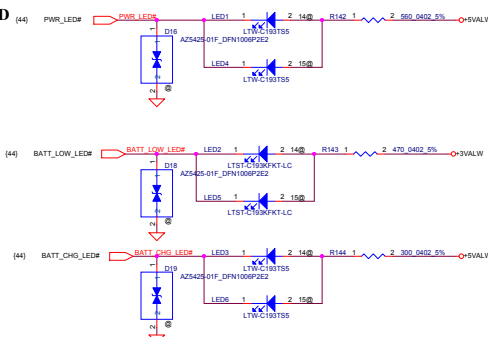
PWR/B Connector



USB I/O Connector

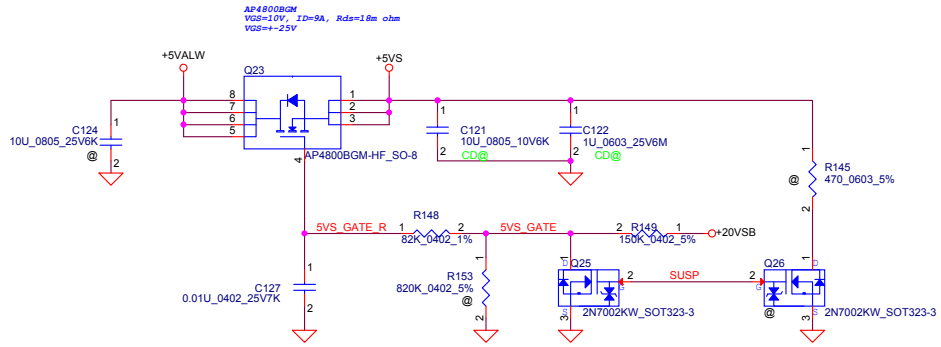


LED

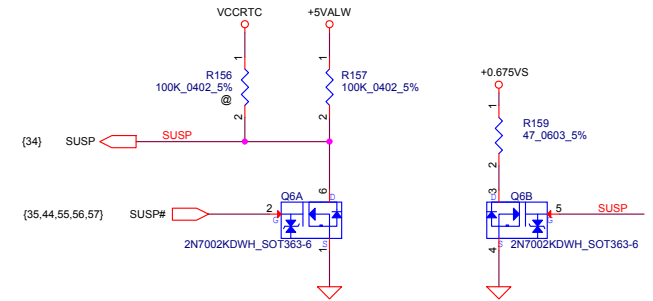
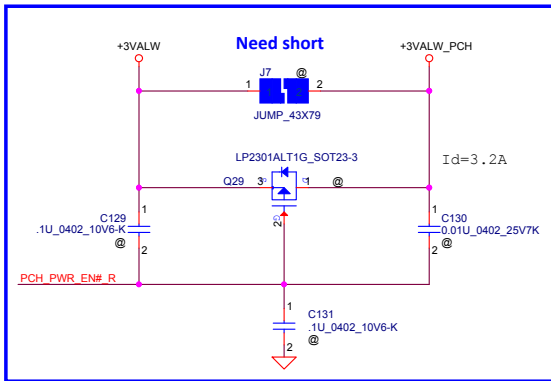
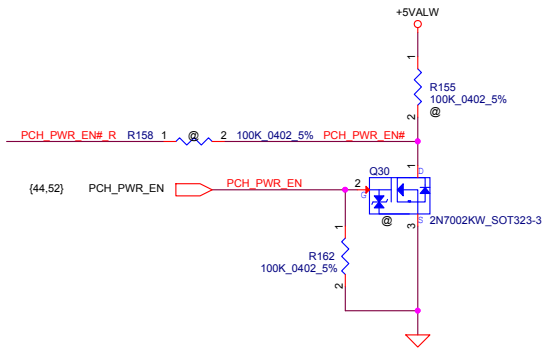
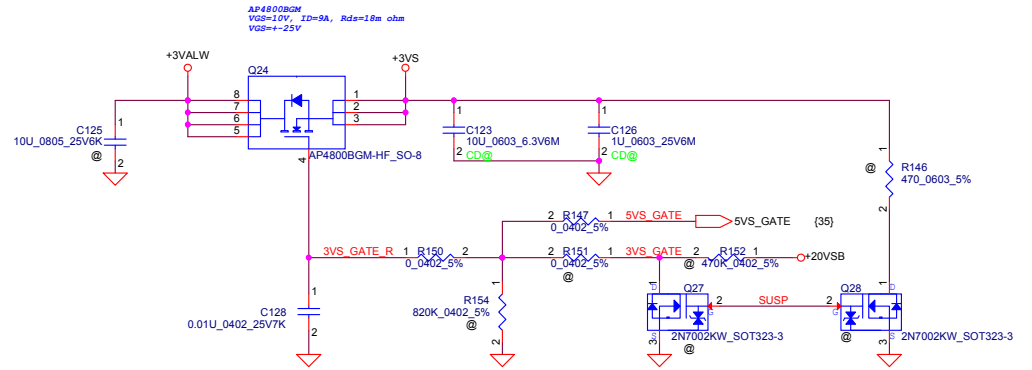



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Date:	Monday, December 09, 2013	Page	15	of	69

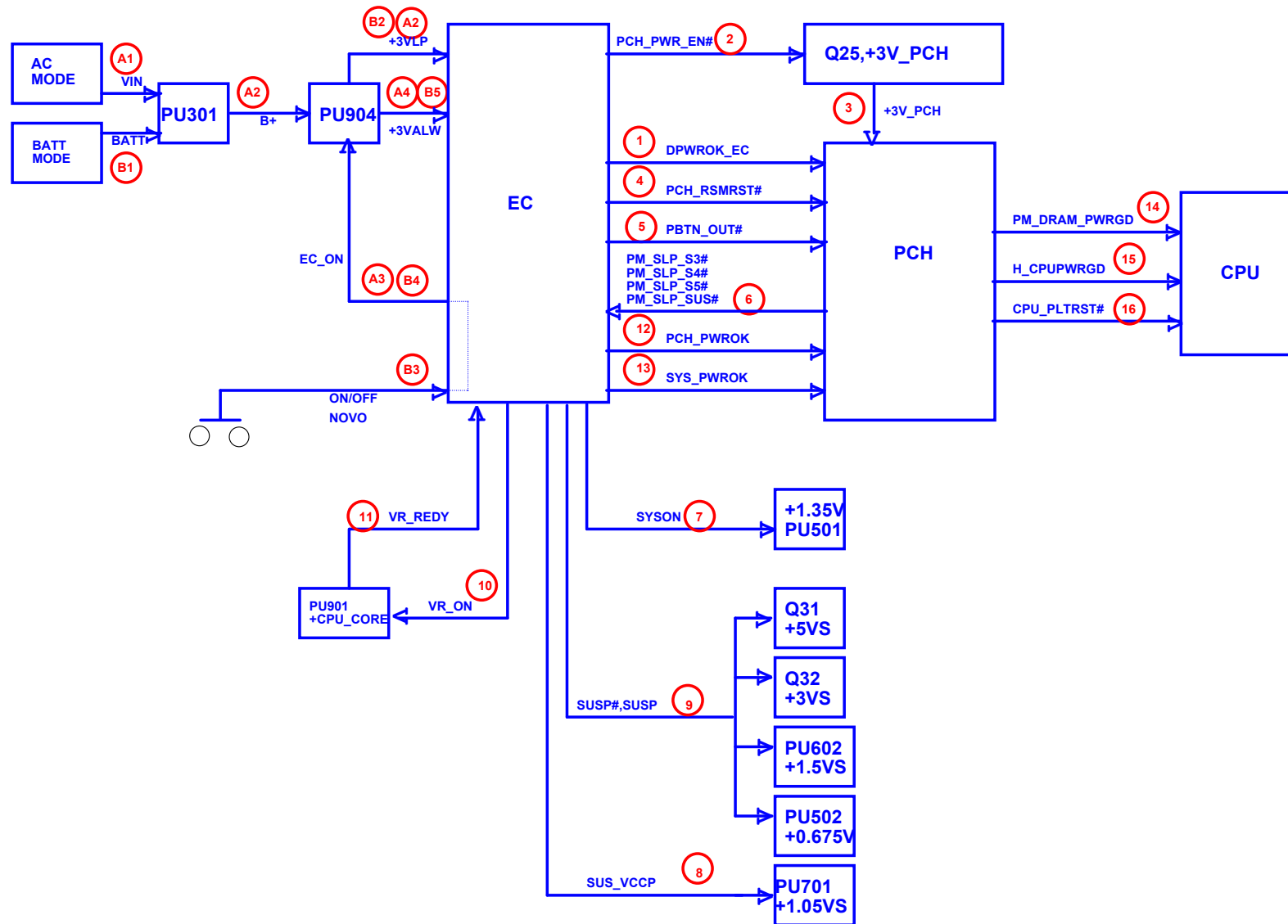
+5VALW to +5VS




+3VALW to +3VS




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					Rev 1.0

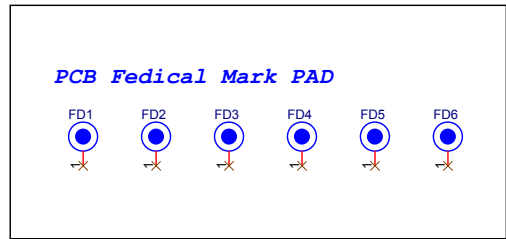
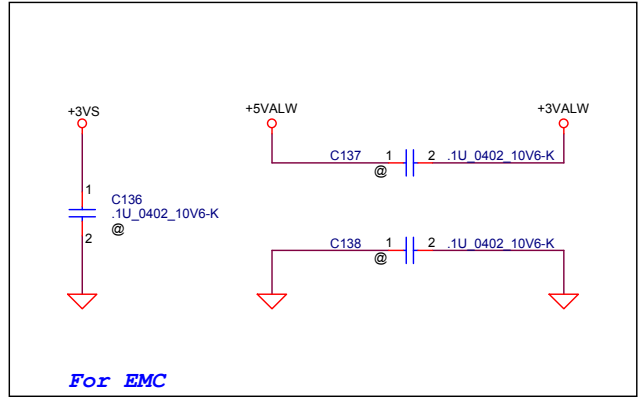
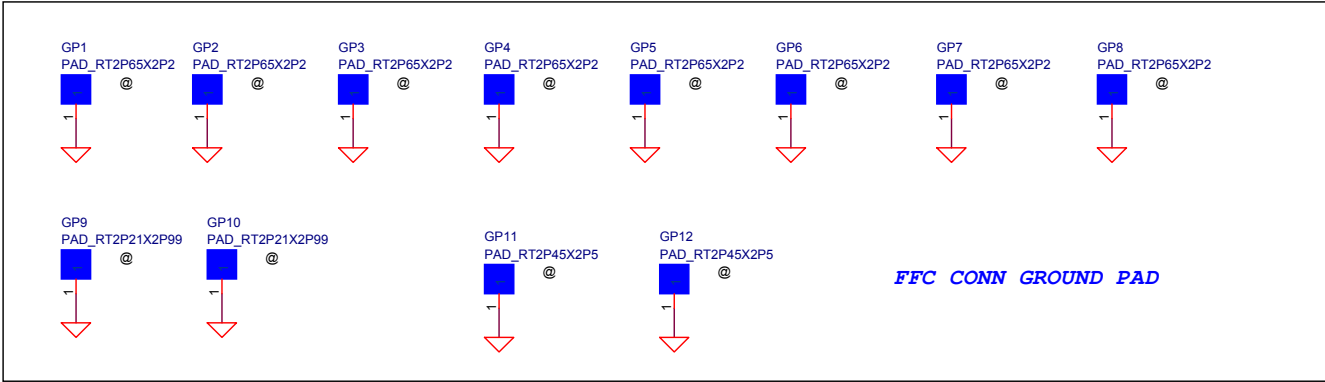
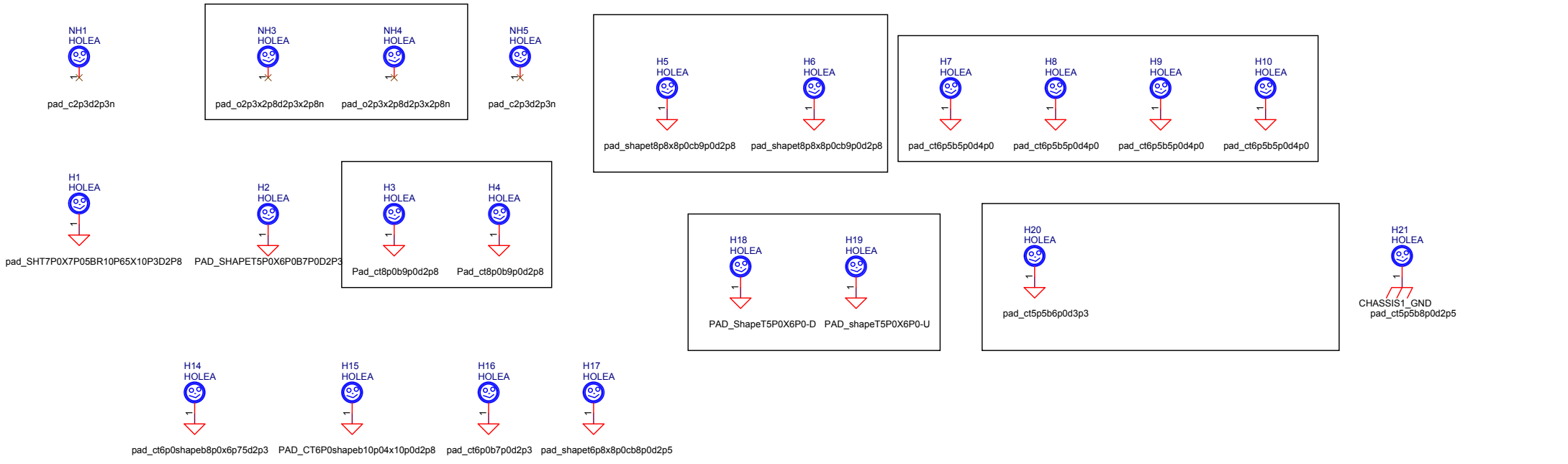



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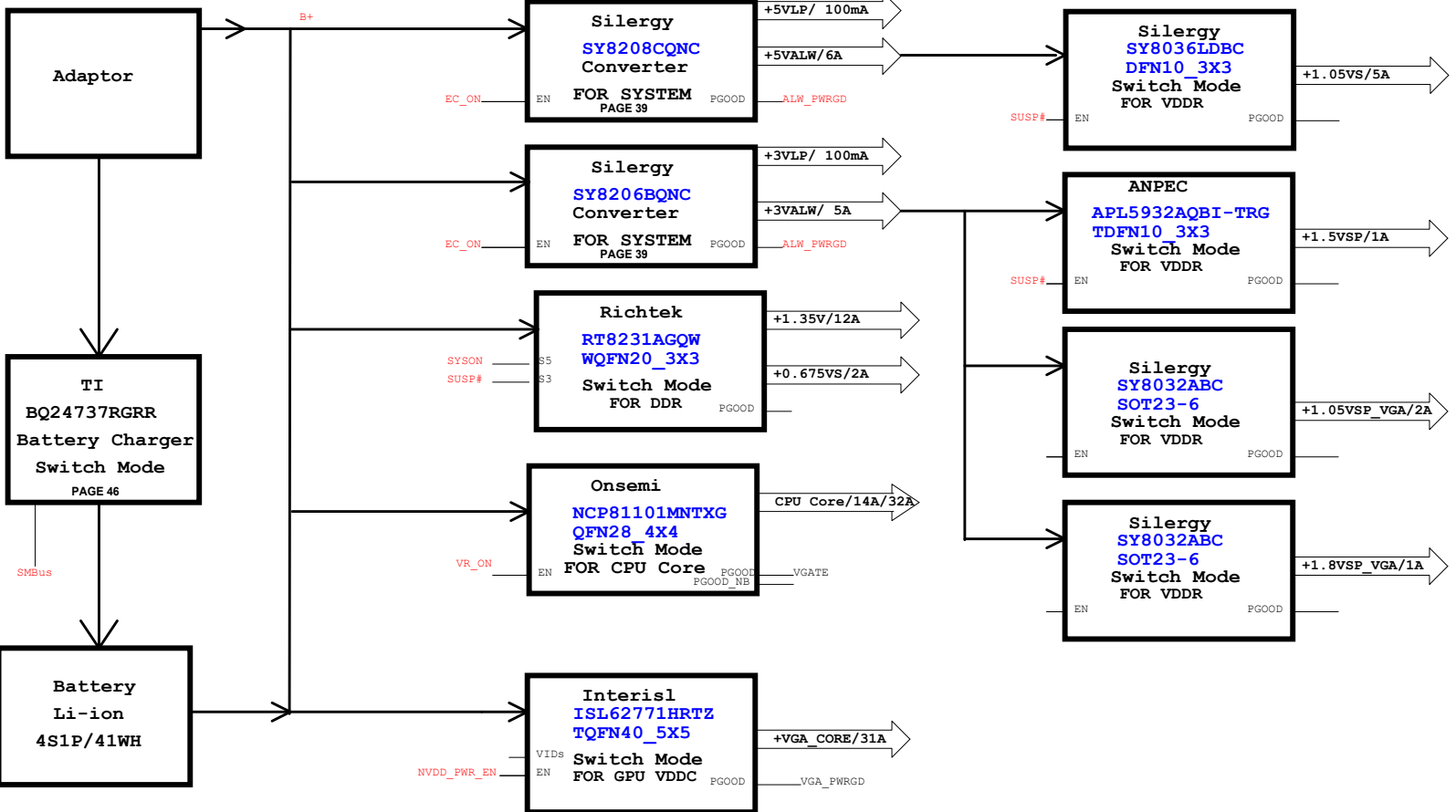
Board ID


BOARD_ID0	BOARD_ID1	BOARD_ID2	BOARD_ID3	Description	Stuff Resistor
0	0	0	0	BDW + Jet-LE sku	RC107,RC108,RC109,RC123
0	0	1	0	BDW + Topaz-XT sku	RC107,RC108,RC102,RC123
0	1	0	0	BDW + N15V-GM sku	RC107,RC101,RC109,RC123
0	1	1	0	BDW + N15S-GT sku	RC107,RC101,RC102,RC123
1	0	0	0	HSW + Jet-LE sku	RC100,RC108,RC109,RC123
1	0	1	0	HSW + Topaz-XT sku	RC100,RC108,RC102,RC123
1	1	0	0	HSW + N15V-GM sku	RC100,RC101,RC109,RC123
1	1	1	0	HSW + N15S-GT sku	RC100,RC101,RC102,RC123
0	0	0	1	BDW + UMA sku	RC107,RC108,RC109,RC123
1	0	0	1	HSW + UMA sku	RC100,RC108,RC109,RC123

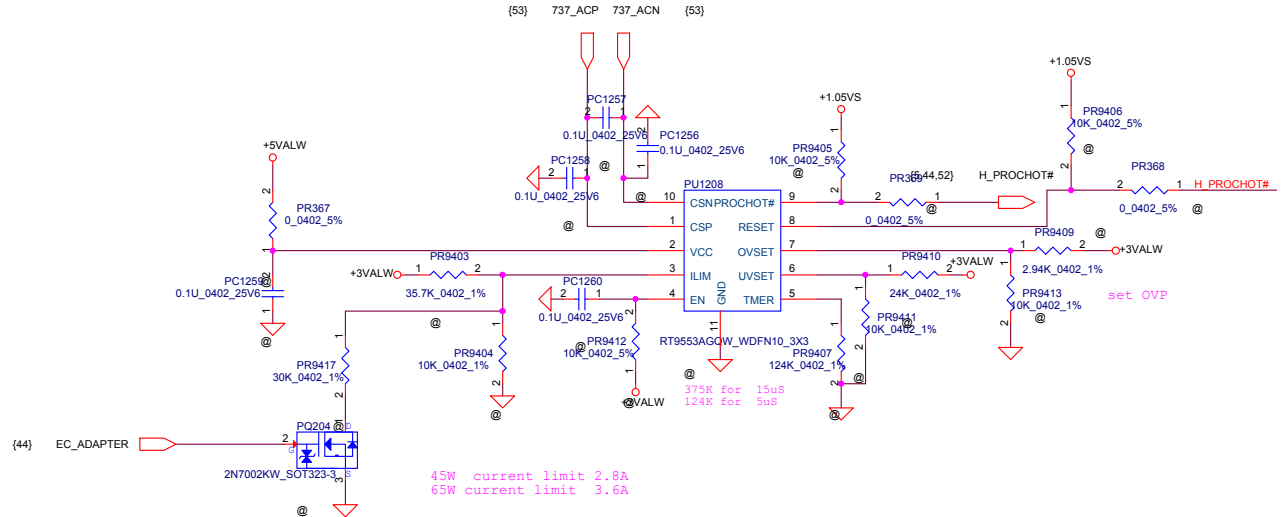
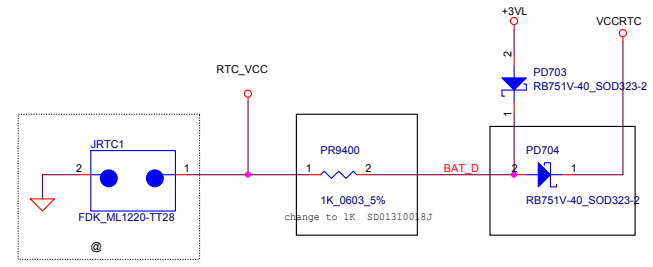
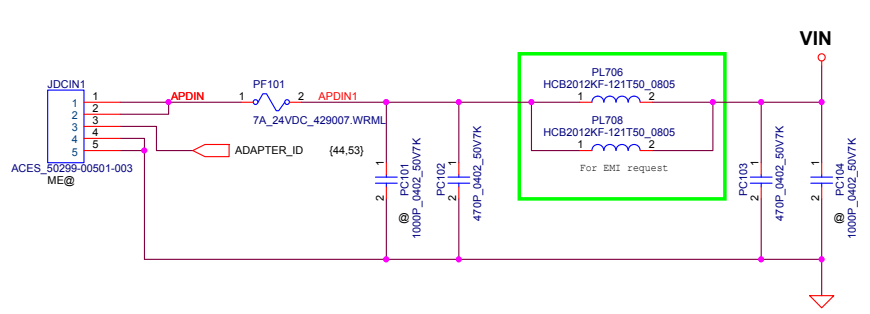
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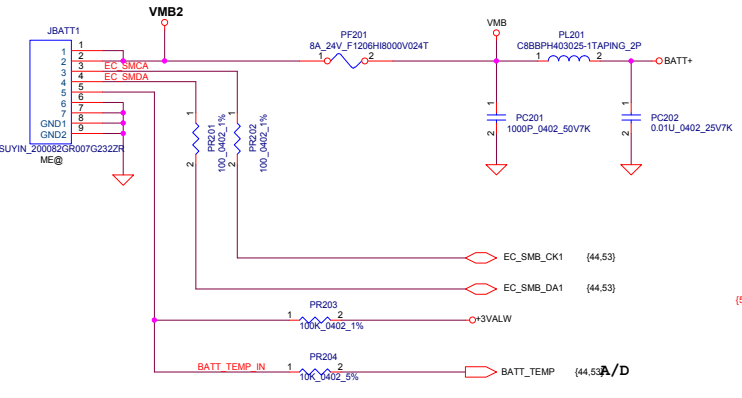
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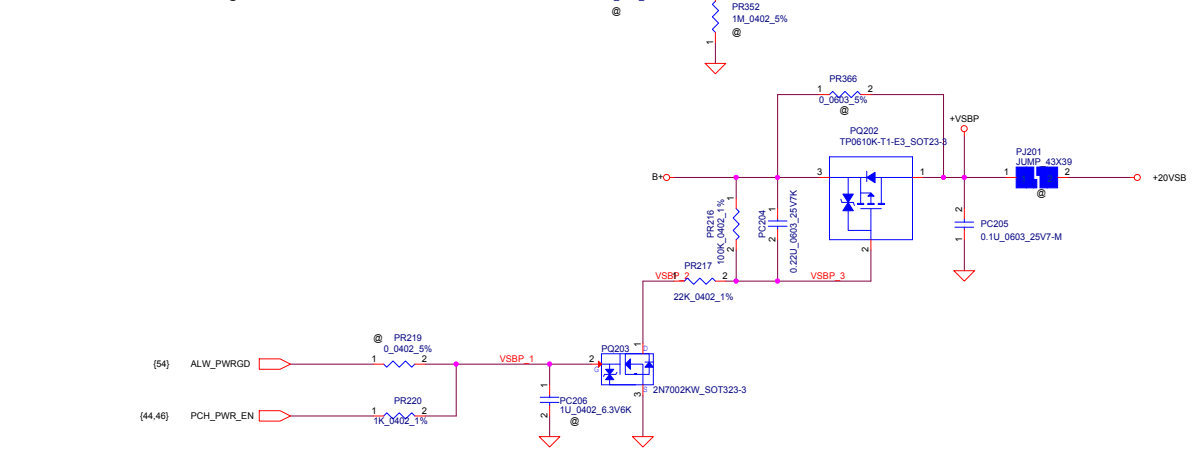
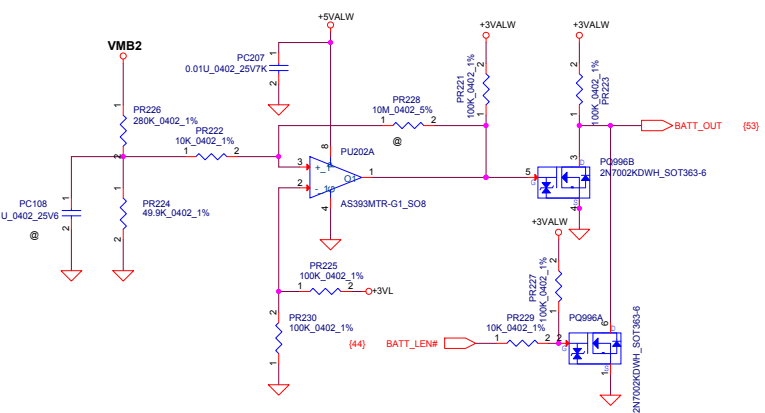
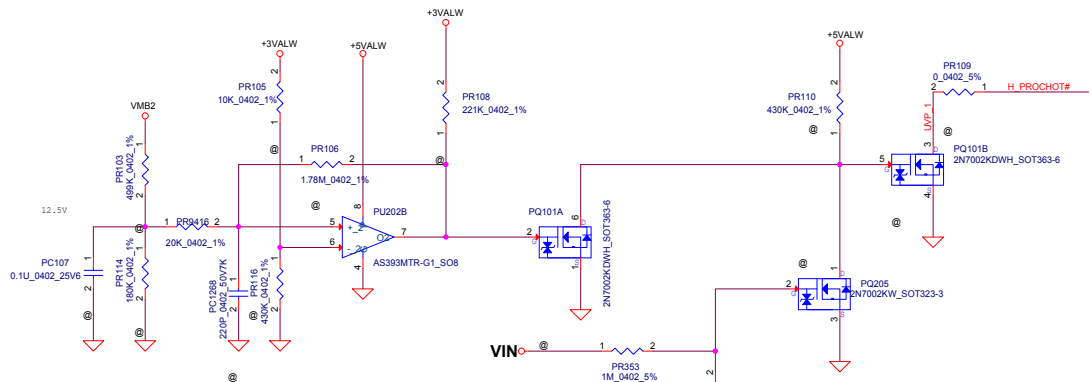
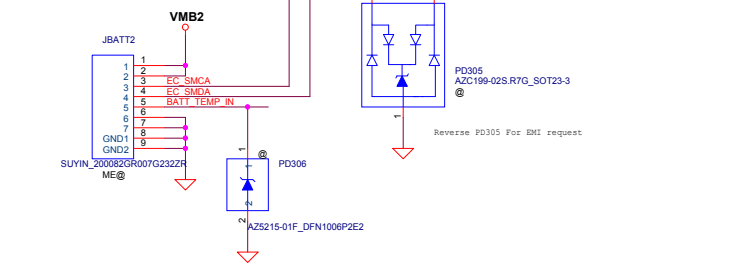
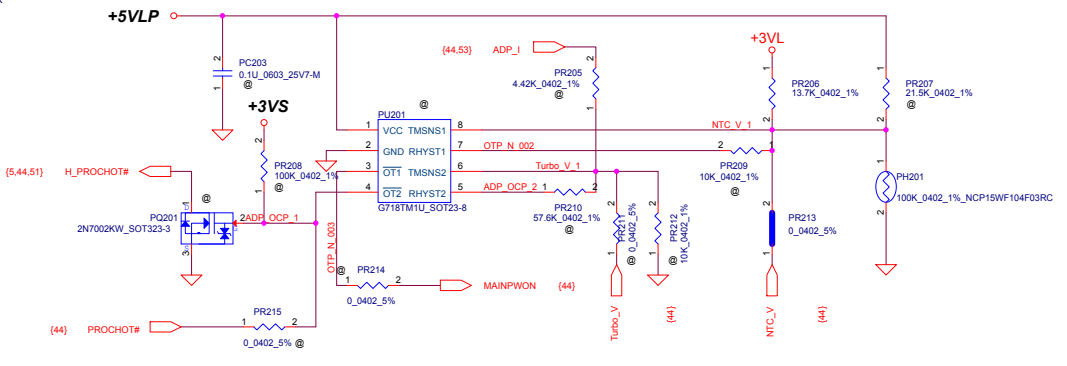
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Size	Document Number	Rev
Custom	UMA	1.0
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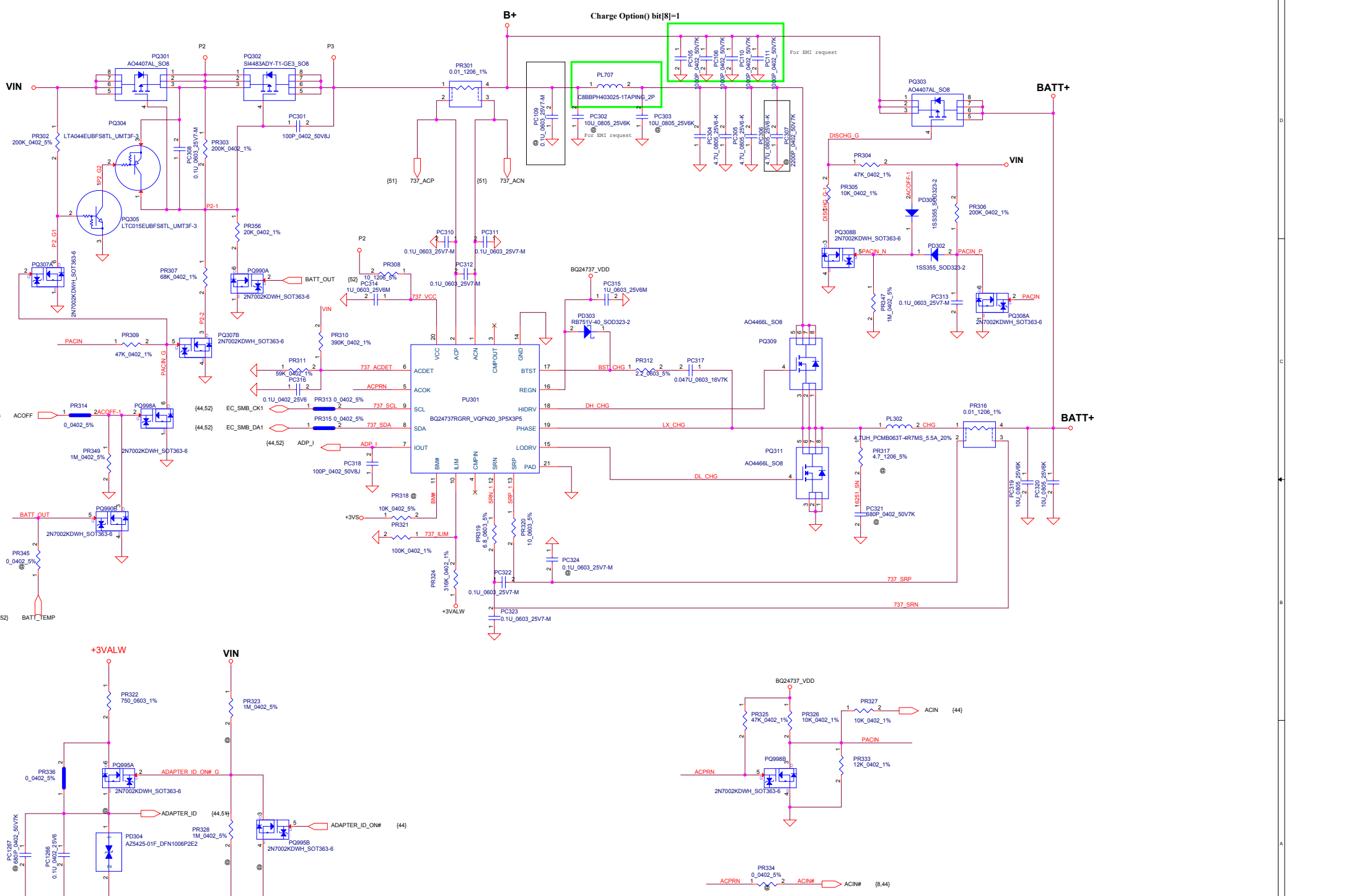




PH201 under CPU botten side :
CPU thermal protection at 92+3 degree C
Recovery at 56 +3 degree C

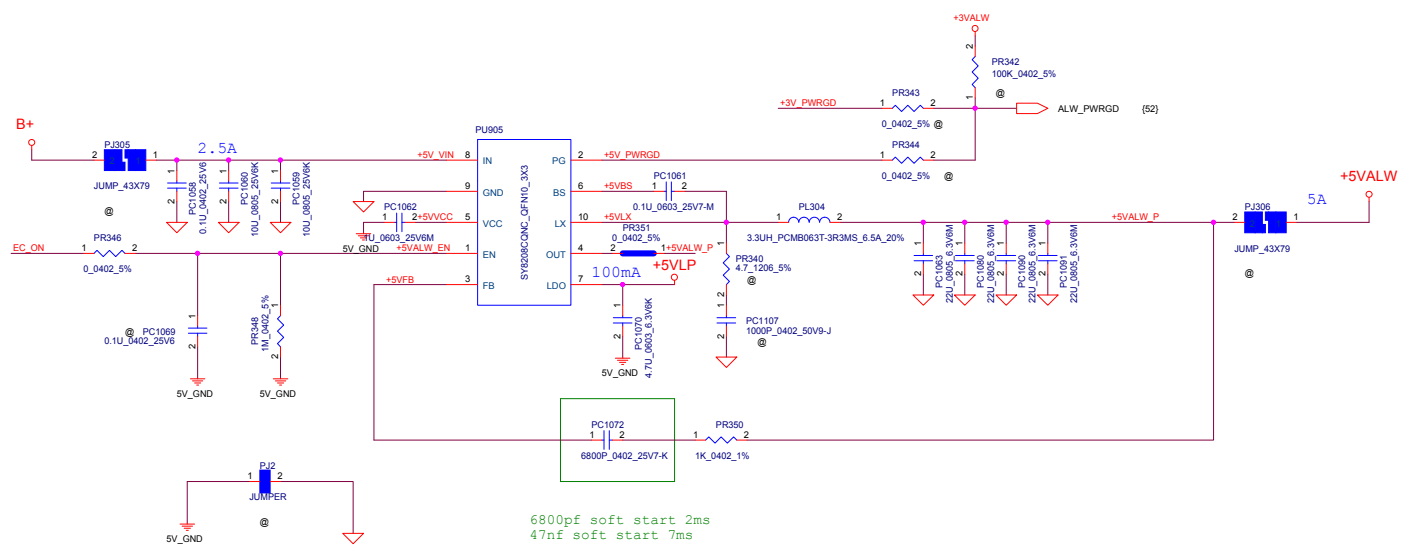
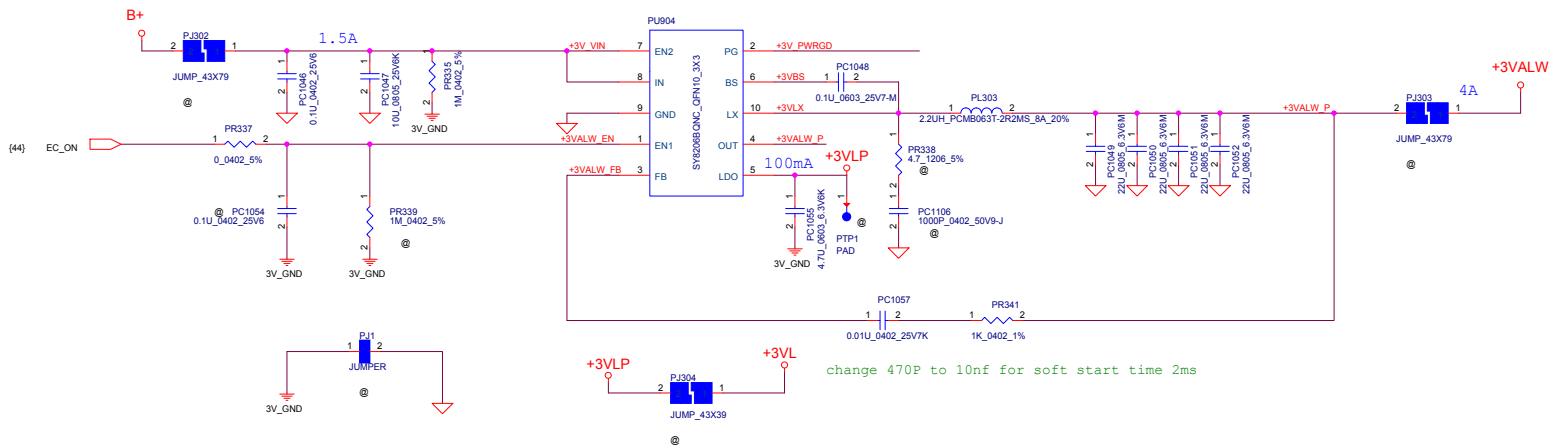
For KB930 --> Keep PU1 circuit
(Vth = 0.825V)
For KB9012 (Red square) --> Remove PU201 circuit, but keep PR206
PH201, PR205, PR211, PQ201, PR208, PR212

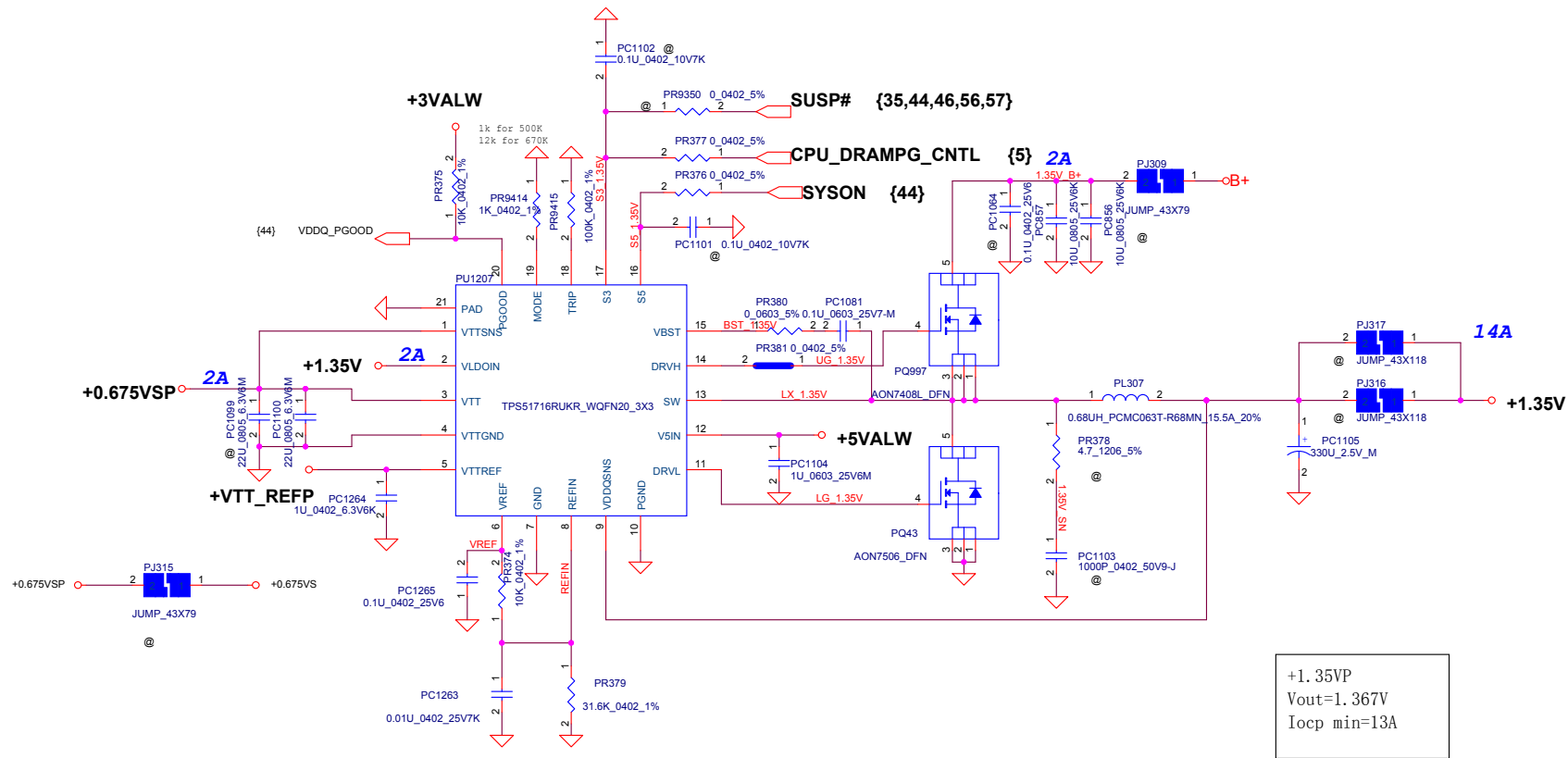


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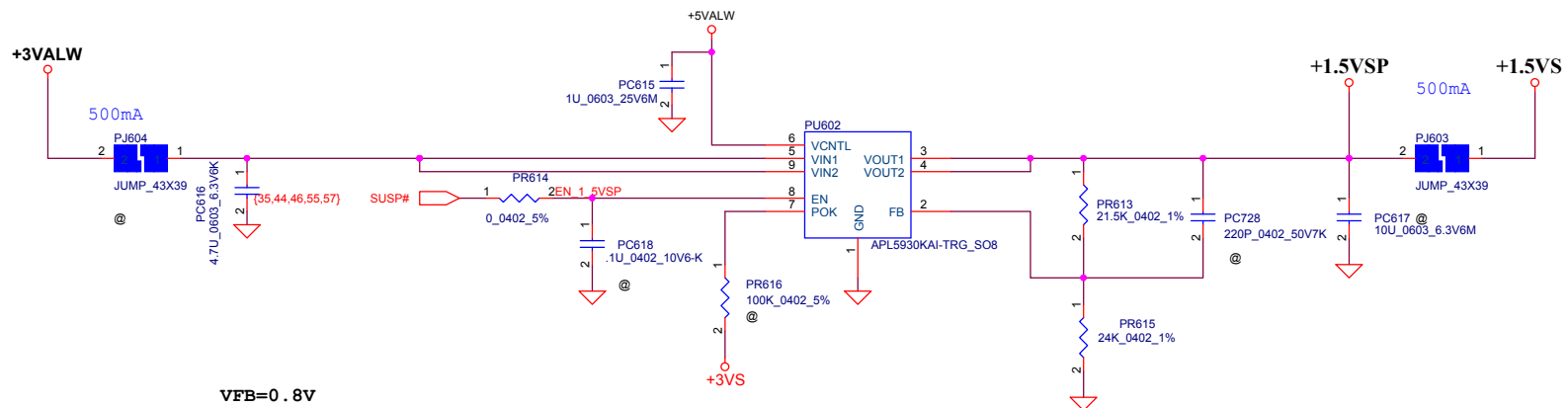
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Size	Document Number	Rev	1.0	
Date:	Monday, December 09, 2013	Sheet	83	of 89






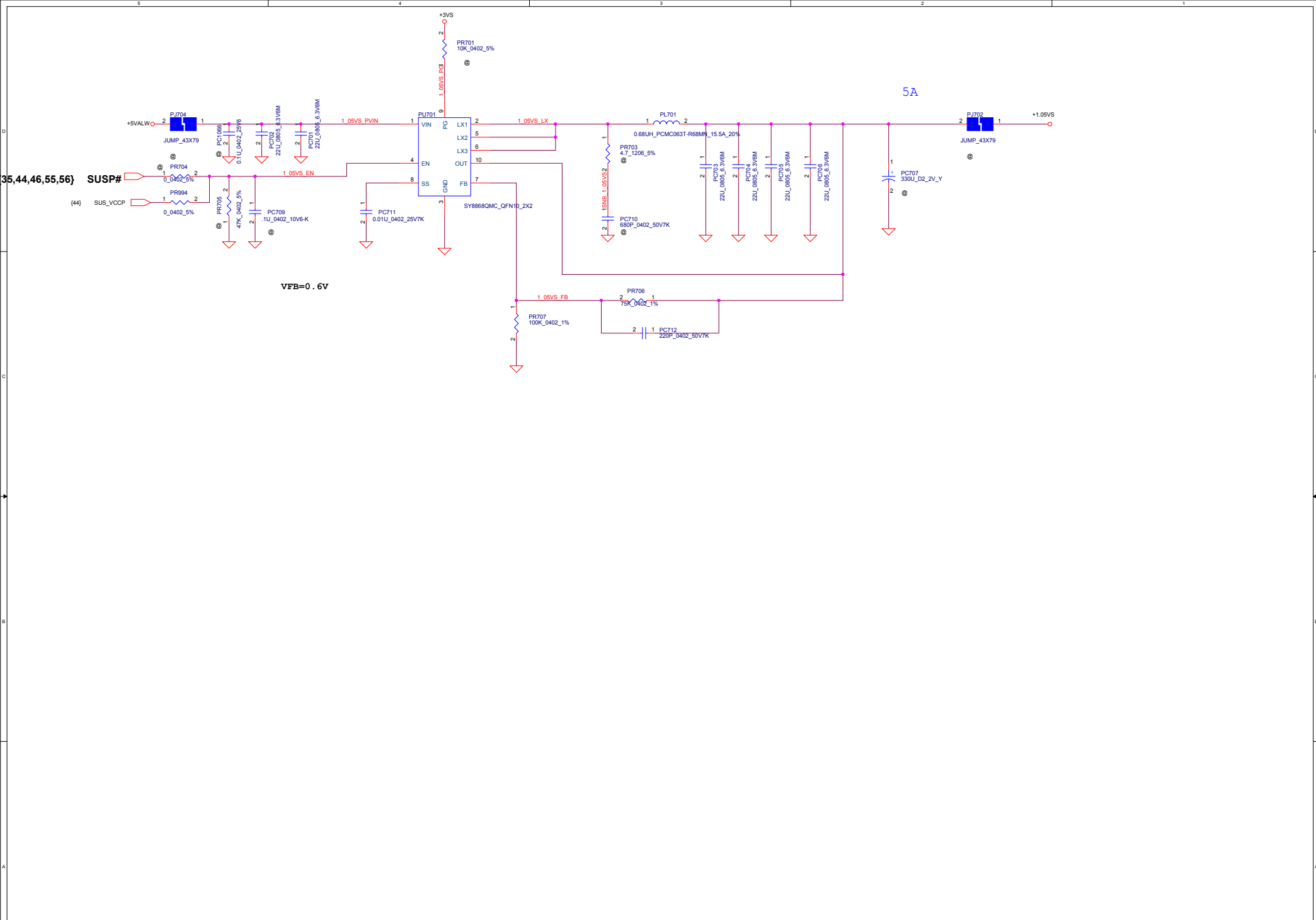
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Title		
1.35VS/+0.675VS		
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					Rev: 1.0 Sheet: 56 of 59




35,44,46,55,56}


SUSP#

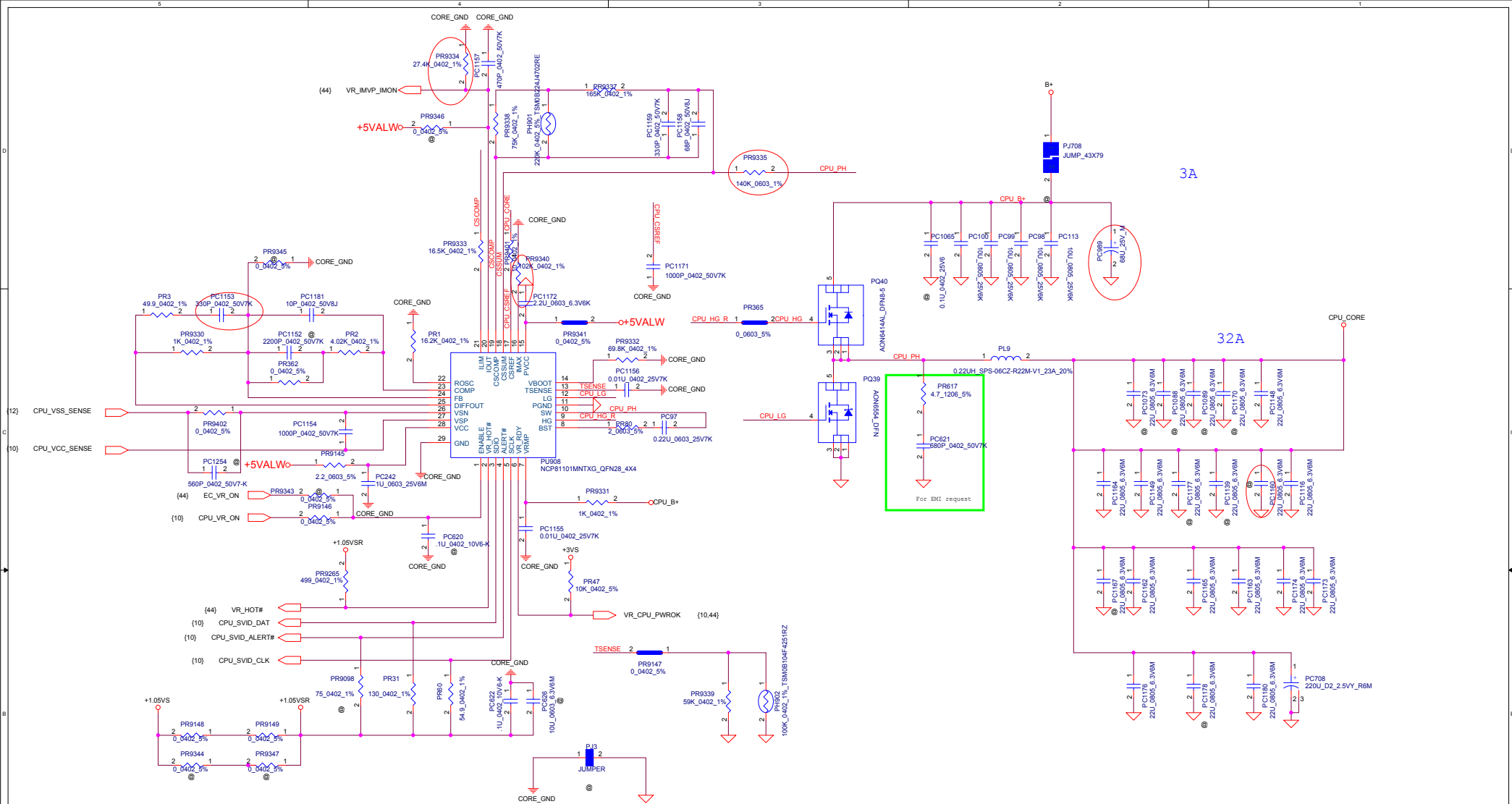
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