

Enrico/Caruso 15" UMA Schematics Document

Sandy Bridge

Intel PCH

2011-06-02

REV : A00

起点主板维修网 www.qdzbwx.com

DY :None Installed
PSL:10mW internal schematic
10mW: 10mW schematic installed
Surge: Surege schematic installed
GIGA: GIGA schematic installed
10/100: 10/100 schematic installed
HDMI: HDMI schematic installed
Debug: Debug schematic installed

DV15 HR Vos GIGA HDMI NoSurge



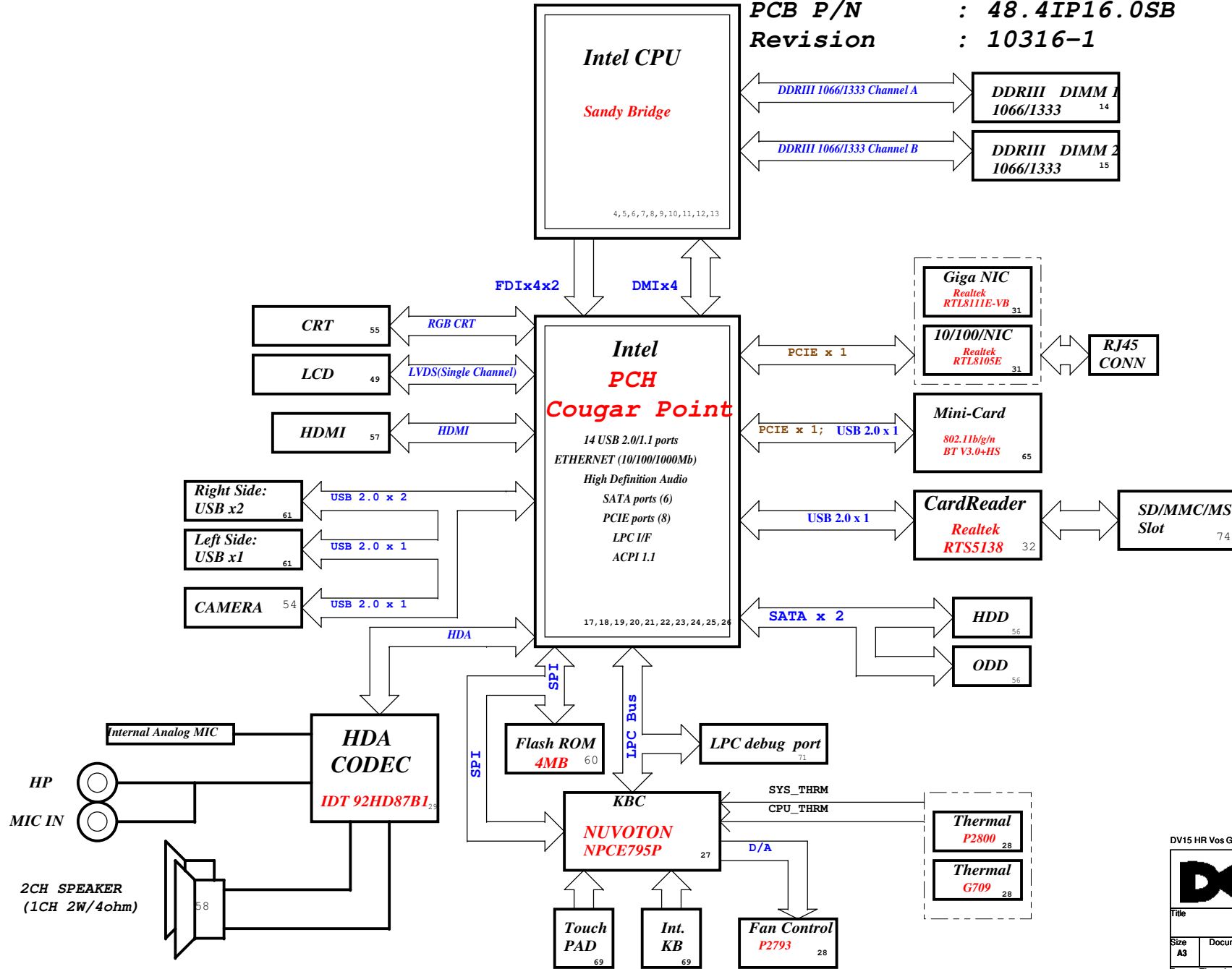
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Cover Page		
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DV15 Huron River UMA Block Diagram

起点主板维修网 www.qdzbwx.com

www.Laptopblue.vn

Project code : 91.4IP01.001
 PCB P/N : 48.4IP16.0SB
 Revision : 10316-1



SYSTEM DC/DC TPS51461 48	
INPUTS	OUTPUTS
DCBATOUT	0D85V_S0
CPU DC/DC ISL95831HRTZ 42~44	
INPUTS	OUTPUTS
DCBATOUT	VCC_CORE
GFX DC/DC ISL95831HRTZ 44	
INPUTS	OUTPUTS
DCBATOUT	VCC_GFXCORE
SYSTEM DC/DC TPS51218 45	
INPUTS	OUTPUTS
DCBATOUT	1D05V_VTT
SYSTEM DC/DC TPS51123RGER 41	
INPUTS	OUTPUTS
DCBATOUT	5V_AUX_S5 3D3V_AUX_S5 5V_S5 3D3V_S5 15V_S5
SYSTEM DC/DC TPS51216RUKR 46	
INPUTS	OUTPUTS
DCBATOUT	1D5V_S3 0D75V_S0 DDR_VREF_S3
MAXIM CHARGER BQ24707 40	
INPUTS	OUTPUTS
+DC_IN_S5 +PBATT	DCBATOUT
SYSTEM DC/DC TPS51311RGTR 47	
INPUTS	OUTPUTS
3D3V_S5	1D8V_S0
Switches	
INPUTS	OUTPUTS
1D5V_S3 5V_S5 3D3V_S5	1D5V_S0 5V_S0 3D3V_S0
PCB LAYER	
L1: Top	L4: Signal
L2: GND	L5: VCC
L3: Signal	L6: Bottom

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Title: **Block Diagram**

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Name	Schematics Notes
SPKR	Reboot option at power-up Default Mode: Internal weak Pull-down. No Reboot Mode with TCO Disabled: Connect to Vcc3_3 with 8.2-kΩ - 10-kΩ weak pull-up resistor.
INIT3_3V#	Weak internal pull-up. Leave as "No Connect".
GNT3#/GPIO55 GNT2#/GPIO53 GNT1#/GPIO51	GNT[3:0]# functionality is not available on Mobile. Mobile: Used as GPIO only Pull-up resistors are not required on these signals. If pull-ups are used, they should be tied to the Vcc3_3power rail.
SPI_MOSI	Enable Danbury: Connect to Vcc3_3 with 8.2-k? weak pull-up resistor. Disable Danbury: left floating, no pull-down required.
NV_ALE	Enable Danbury: Connect to +NVRAM_VCCQ with 8.2-kohm weak pull-up resistor [CRB has it pulled up with 1-kohm no-stuff resistor] Disable Danbury: leave floating (internal pull-down)
NC_CLE	DMI termination voltage. Weak internal pull-up. Do not pull low.
HAD_DOCK_EN# /GPIO[33]	Low (0) - Flash Descriptor Security will be overridden. Also, when this signals is sampled on the rising edge of PWROK then it will also disable Intel ME and its features. High (1) - Security measure defined in the Flash Descriptor will be enabled. Platform design should provide appropriate pull-up or pull-down depending on the desired settings. If a jumper option is used to tie this signal to GND as required by the functional strap, the signal should be pulled low through a weak pull-down in order to avoid asserting HDA_DOCK_EN# inadvertently. Note: CRB recommends 1-kohm pull-down for FD Override. There is an internal pull-up of 20 kohm for DA_DOCK_EN# which is only enabled at boot/reset for strapping functions.
HDA_SDO	Weak internal pull-down. Do not pull high. Sampled at rising edge of RSMRST#.
HDA_SYNC	Weak internal pull-down. Do not pull high. Sampled at rising edge of RSMRST#.
GPIO15	Low (1) - Intel ME Crypto Transport Layer Security (TLS) cipher suite with no confidentiality High (1) - Intel ME Crypto Transport Layer Security (TLS) cipher suite with confidentiality Note : This is an un-muxed signal. This signal has a weak internal pull-down of 20 kohm which is enabled when PWROK is low. Sampled at rising edge of RSMRST#. CRB has a 1-kohm pull-up on this signal to +3.3VA rail.
GPIO8	GPIO8 on PCH is the Integrated Clock Enable strap and is required to be pulled-down using a 1k +/- 5% resistor. When this signal is sampled high at the rising edge of RSMRST#, Integrated Clocking is enabled, When sampled low, Buffer Through Mode is enabled.
GPIO27	Default = Do not connect (floating) High(1) = Enables the internal VccVRM to have a clean supply for analog rails. No need to use on-board filter circuit. Low (0) = Disables the VccVRM. Need to use on-board filter circuits for analog rails.

Pin Name	Strap Description	Configuration (Default value for each bit is 1 unless specified otherwise)	Default Value
CFG[2]	PCI-Express Static Lane Reversal	1: Normal Operation. 0: Lane Numbers Reversed 15 -> 0, 14 -> 1, ...	1
CFG[4]		Disabled - No Physical Display Port attached to Embedded DisplayPort. 1: Embedded DisplayPort. 0: Enabled - An external Display Port device is connect to the EMBEDDED display Port	0
CFG[6:5]	PCI-Express Port Bifurcation Straps	11 : x16 - Device 1 functions 1 and 2 disabled 10 : x8, x8 - Device 1 function 1 enabled ; function 2 disabled 01 : Reserved - (Device 1 function 1 disabled ; function 2 enabled) 00 : x8, x4, x4 - Device 1 functions 1 and 2 enabled	11
CFG[7]	PEG DEFER TRAINING	1: PEG Train immediately following xxRESETB de assertion 0: PEG Wait for BIOS for training	1

POWER PLANE	VOLTAGE	Voltage Rails		DESCRIPTION
		ACTIVE IN		
5V_S0 3D3V_S0 1D8V_S0 1D5V_S0 1D05V_VTT 0D85V_S0 0D75V_S0 VCC_CORE VCC GFXCORE	5V 3.3V 1.8V 1.5V 1.05V 0.95 - 0.85V 0.75V 0.35V to 1.5V 0.4 to 1.25V	S0		CPU Core Rail Graphics Core Rail
5V_USBX_S3 1D5V_S3 DDR_VREF_S3	5V 1.5V 0.75V	S3		
BT+ DCBATOUT 5V_S5 5V_AUX_S5 3D3V_S5 3D3V_AUX_S5	9V-12.6V 9V-19V 5V 5V 3.3V 3.3V	All S states		AC Brick Mode only
3D3V_LAN_S5	3.3V	WOL_EN		Legacy WOL
3D3V_AUX_KBC	3.3V	DSW, Sx		ON for supporting Deep Sleep states
3D3V_AUX_S5	3.3V	G3, Sx		Powered by Li Coin Cell in G3 and +V3ALW in Sx

USB Table

Pair	Device
0	X
1	USB Ext. port 1
2	X
3	X
4	X
5	CARD READER
6	X
7	X
8	USB Ext. port 2
9	USB Ext. port 3
10	X
11	Mini Card1 (WLAN)
12	CAMERA
13	X

PCIE Routing

LANE1	X
LANE2	Onboard LAN
LANE3	x
LANE4	Mini Card1 (WLAN)
LANE5	X
LANE6	X
LANE7	X
LANE8	X

SATA Table

SATA	
Pair	Device
0	HDD1
1	X
2	X
3	X
4	ODD1
5	X

SMBus ADDRESSES

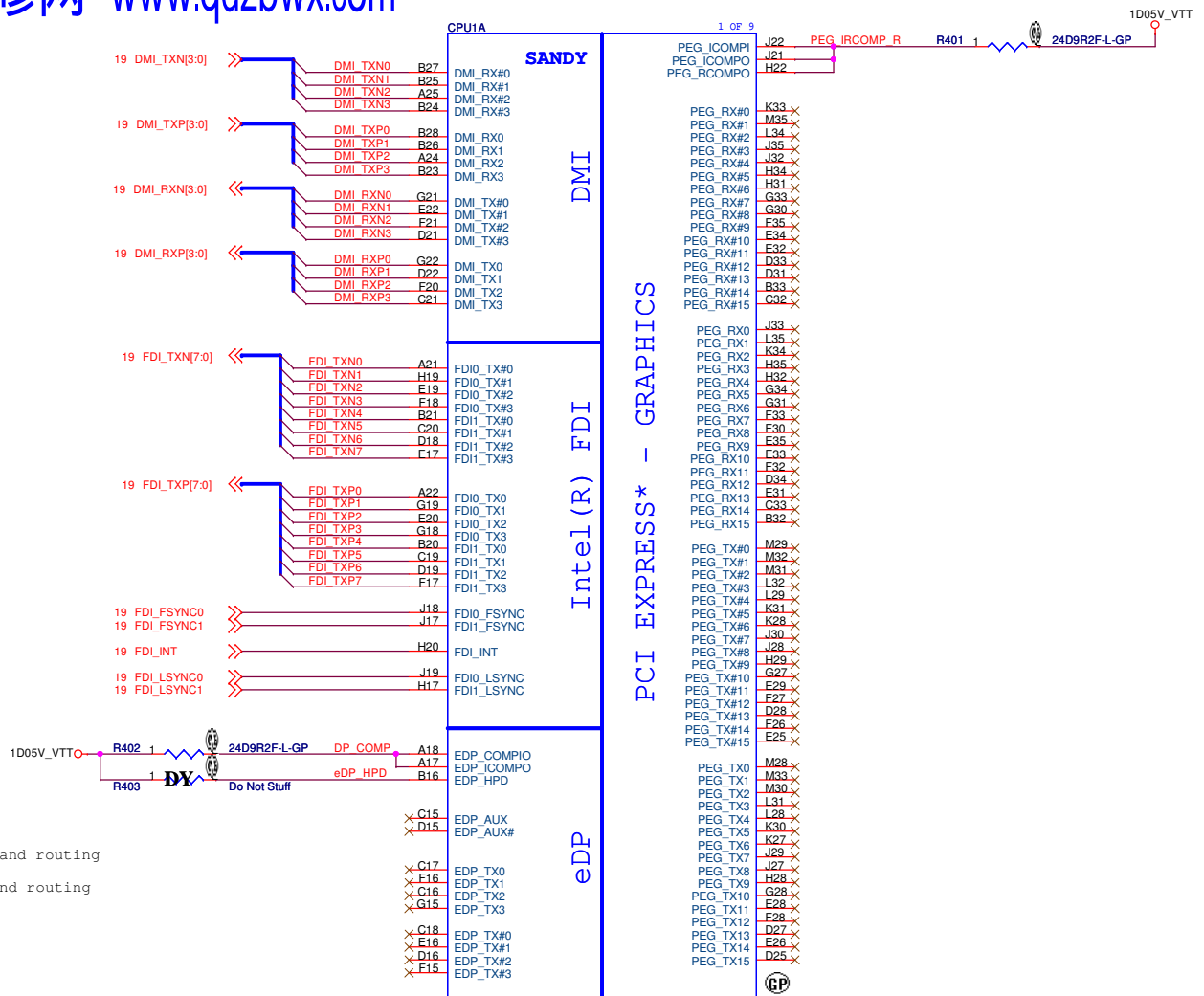
I ² C / SMBus Addresses		Ref Des	HURON RIVER ORB Bus	
Device	Address	Hex	Bus	
EC SMBus 1 Battery CHARGER			BAT_SCL/BAT_SDA BAT_SCL/BAT_SDA BAT_SCL/BAT_SDA	
EC SMBus 2 PCH			SML1_CLK/SML1_DATA SML1_CLK/SML1_DATA	
PCH SMBus SO-DIMMA (SPD) SO-DIMMB (SPD) MINI			PCH_SMBDATA/PCH_SMBCLK PCH_SMBDATA/PCH_SMBCLK PCH_SMBDATA/PCH_SMBCLK PCH_SMBDATA/PCH_SMBCLK	

DV15 HR Vos GIGA HDMI NoSurge



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Signal Routing Guideline:
PEG_ICOMPO keep W/S=12/15 mils and routing length less than 500 mils.
PEG_ICOMPI & PEG_RCOPMO keep W/S=4/15 mils and routing length less than 500 mils.



Signal Routing Guideline:
EDP_ICOMPO keep W/S=12/15 mils and routing length less than 500 mils.
EDP_COMPIO keep W/S=4/15 mils and routing length less than 500 mils.

SKT-BGA989C468393H184-NF
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2nd = 62.10040.771

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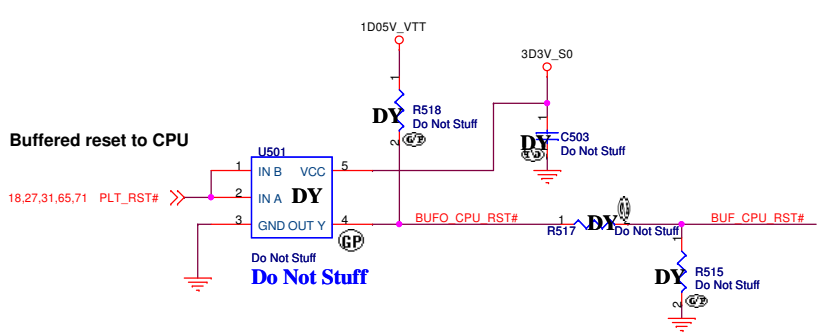
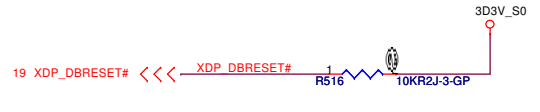
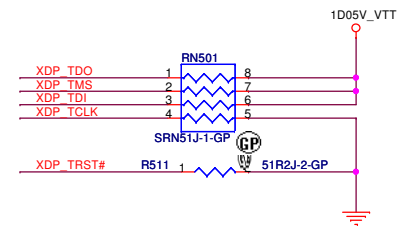
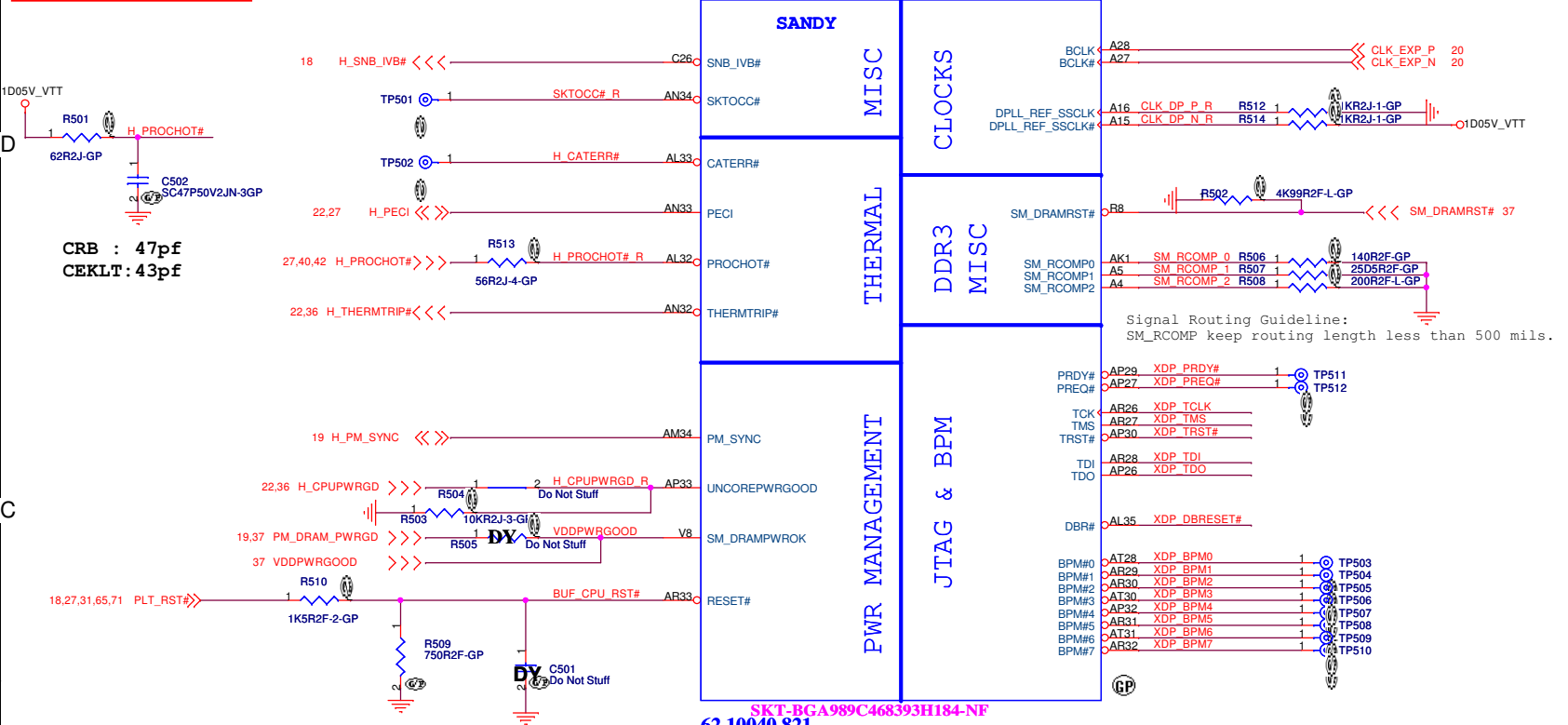
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Title: **CPU (PCIe/DMI/FDI)**

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SSID = CPU

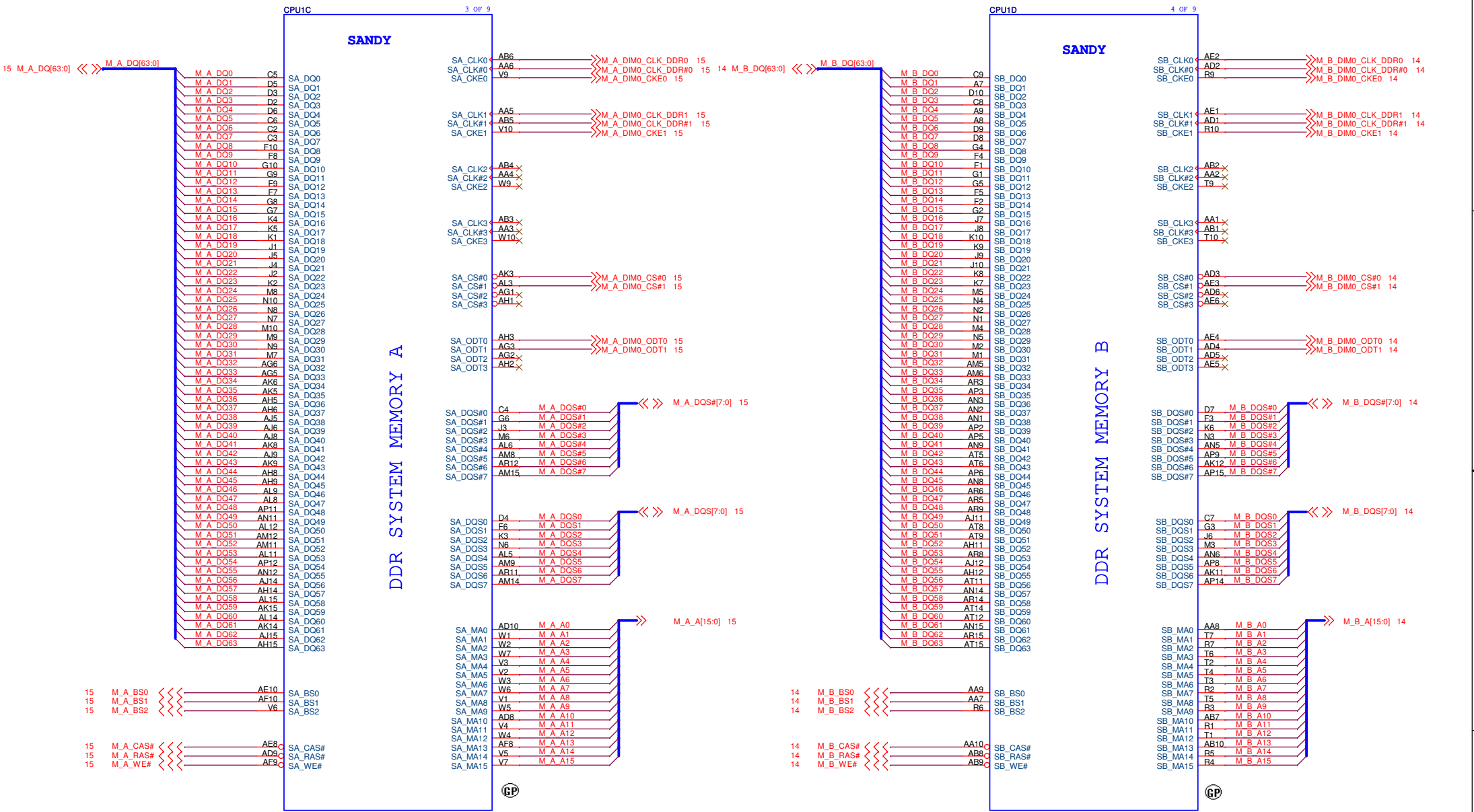


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Title **CPU (THERMAL/CLOCK/PM)**


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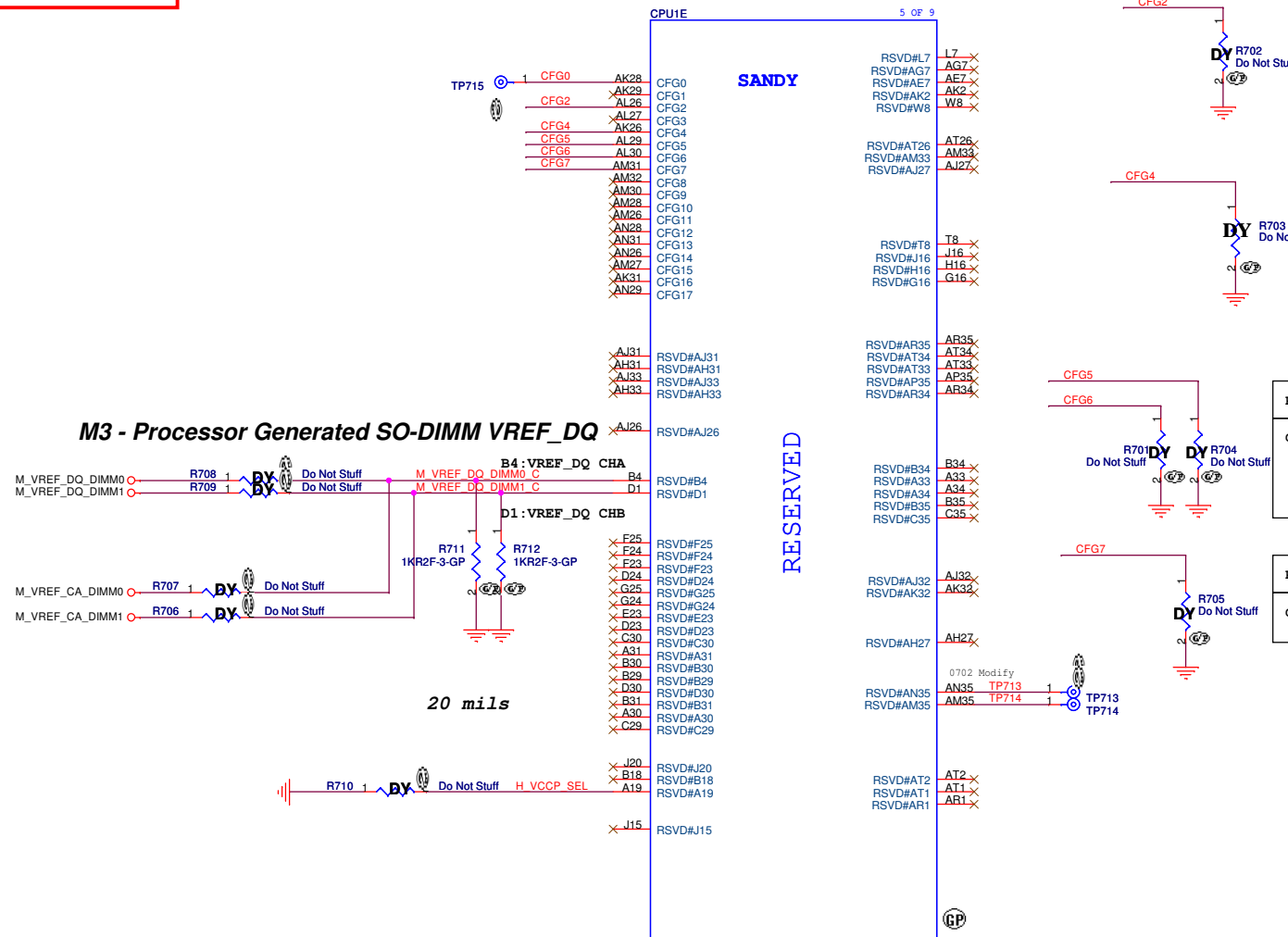


62.10040.821
2nd = 62.10040.771

62.10040.821
2nd = 62.10040.771

DV15 HR Vos GIGA HDMI NoSurge

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Title: **CPU (DDR)**
 Size: A3
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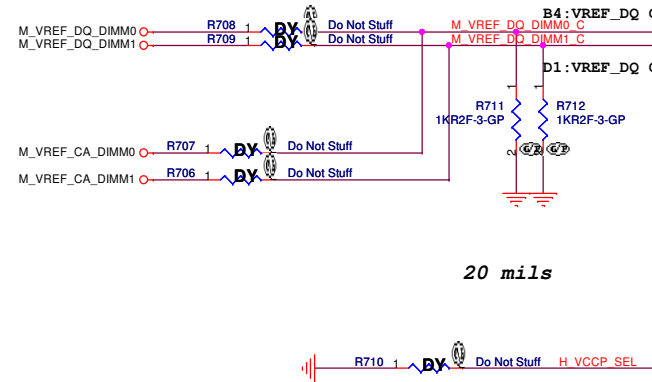
PEG Static Lane Reversal	
CFG2	1: Normal Operation; Lane # definition matches socket pin map definition 0: Lane Reversed

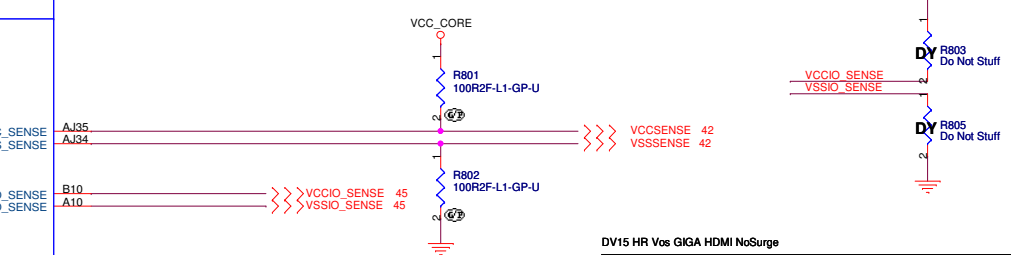
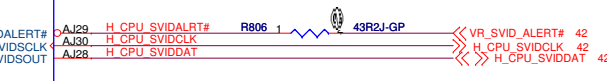
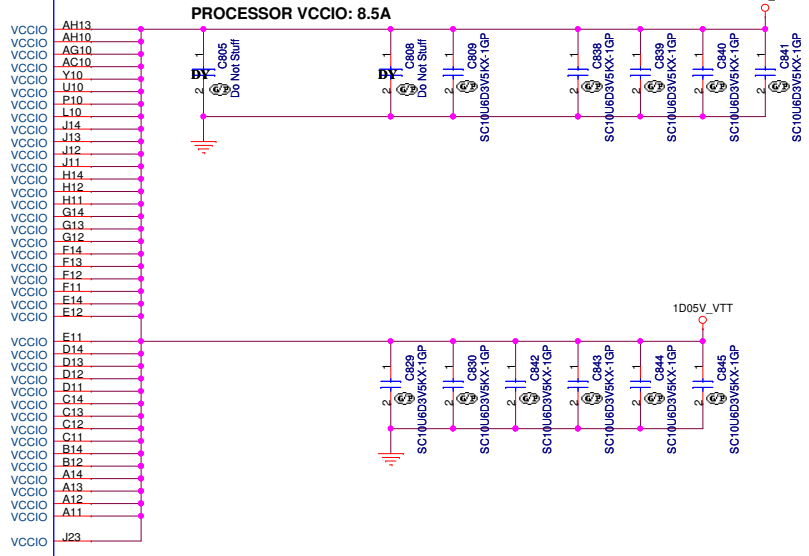
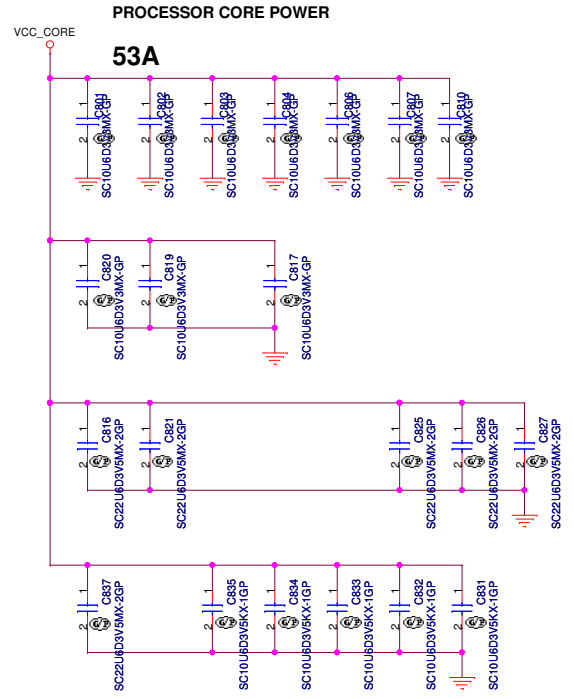
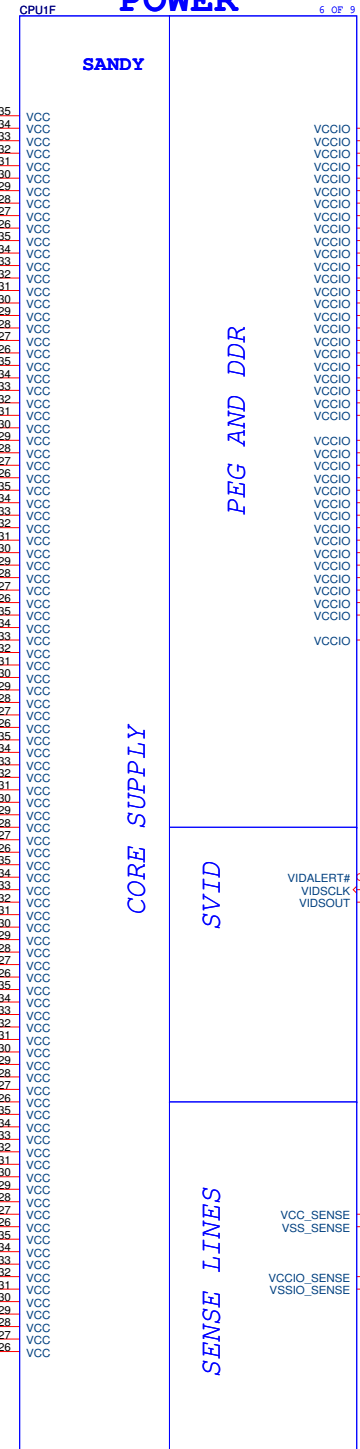
Display Port Presence Strap	
CFG4	1: Disabled; No Physical Display Port attached to Embedded Display Port 0: Enabled; An external Display Port device is connected to the Embedded Display Port

PCIe Port Bifurcation Straps	
CFG[6:5]	11: x16 - Device 1 functions 1 and 2 disabled 10: x8, x8 - Device 1 function 1 enabled; function 2 disabled 01: Reserved - (Device 1 function 1 disabled; function 2 enabled) 00: x8, x4, x4 - Device 1 functions 1 and 2 enabled

PEG DEFER TRAINING	
CFG7	1: PEG Train immediately following xxRESETB de assertion 0: PEG Wait for BIOS for training

M3 - Processor Generated SO-DIMM VREF_DQ





起点主板维修网 www.qdzbwx.com

62.10040.821 2nd = 62.10040.771

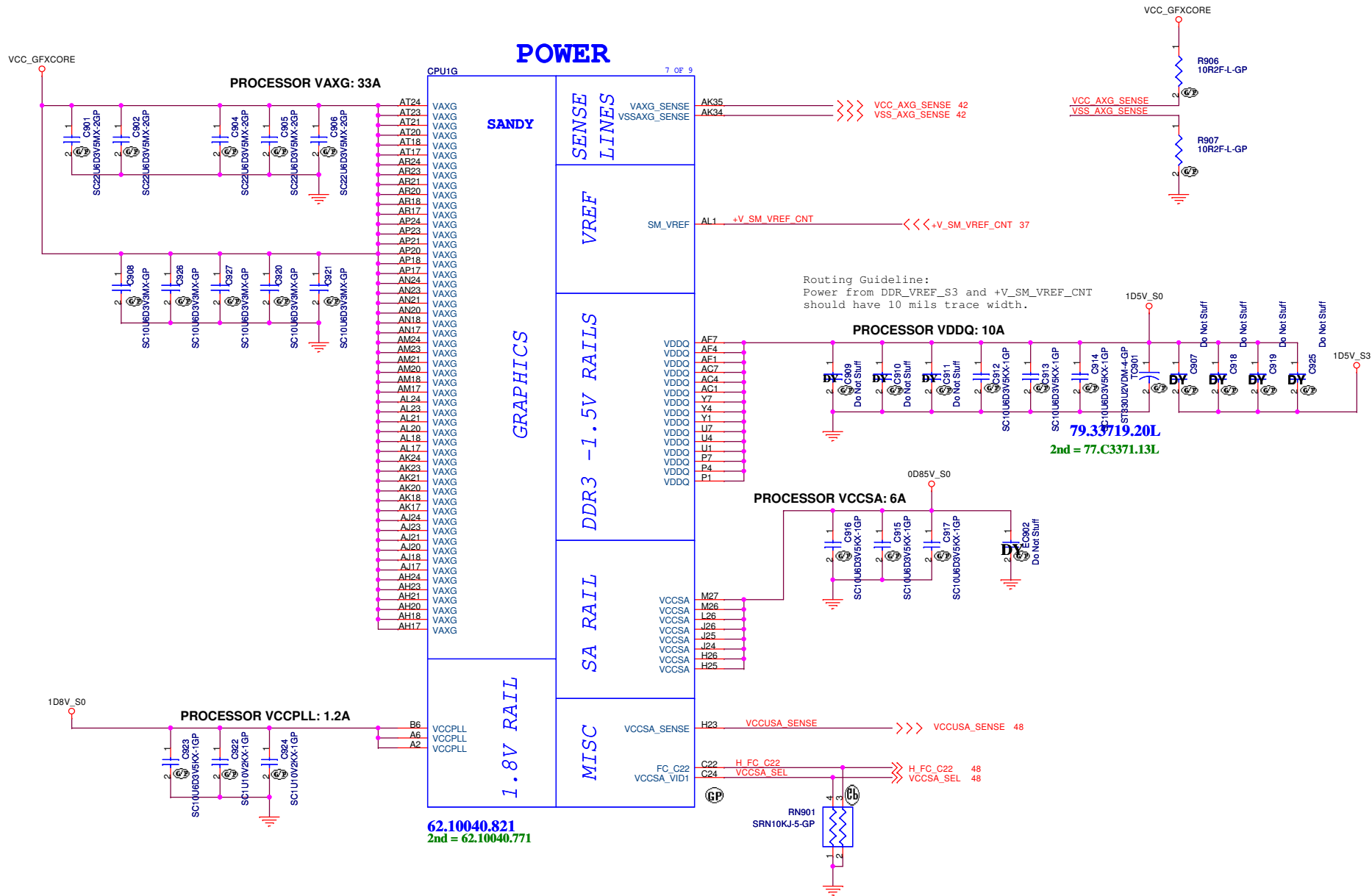
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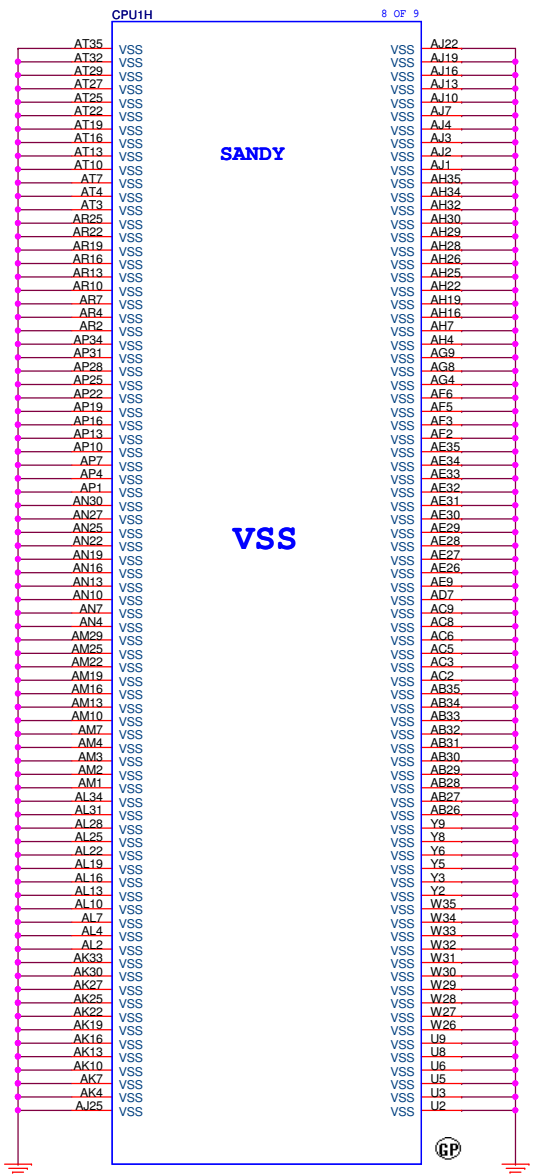
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Title **CPU (VCC CORE)**

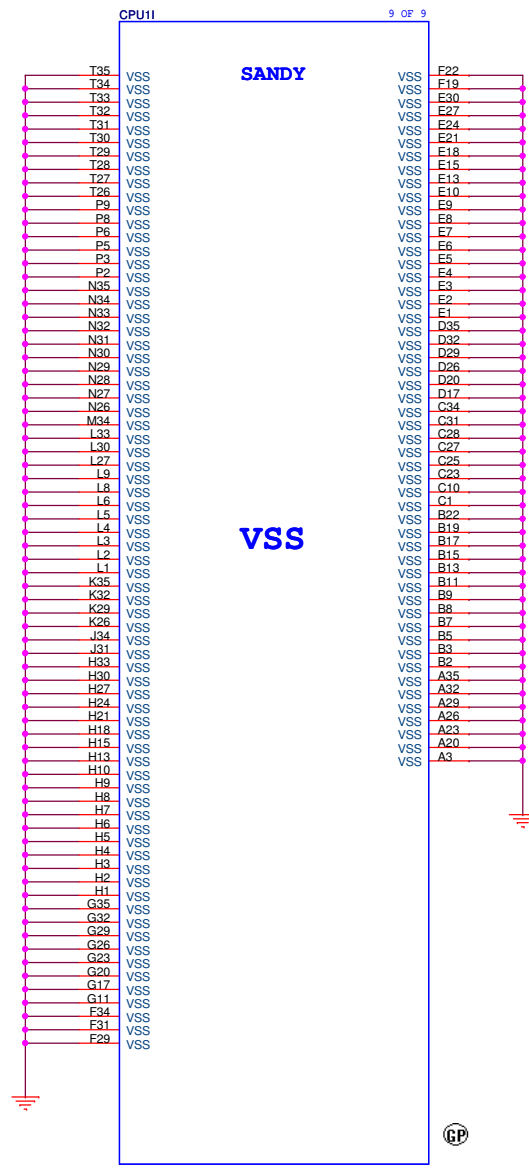
Size Custom Document Number **Enrico/Caruso 15 HR** Rev **X01**

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62.10040.821
2nd = 62.10040.771



62.10040.821
2nd = 62.10040.771

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Title: **CPU (VSS)**

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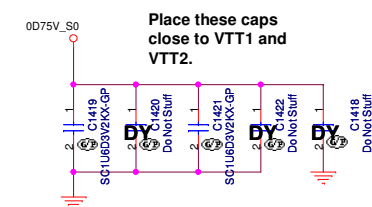
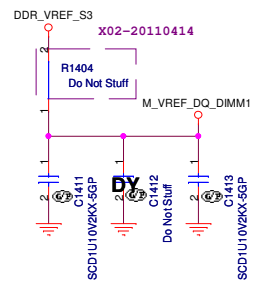
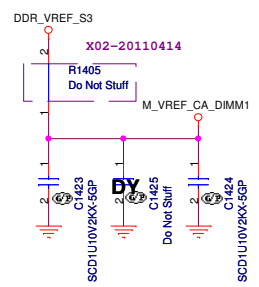
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SSID = MEMORY

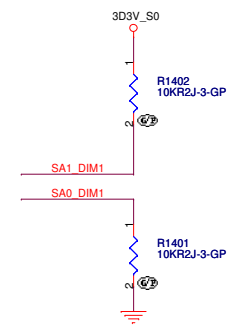


Place these caps close to VTT1 and VTT2.

M_B A0	98	A0	
M_B A1	97	A1	
M_B A2	96	A2	
M_B A3	95	A3	
M_B A4	92	A4	
M_B A5	91	A5	
M_B A6	90	A6	
M_B A7	88	A7	
M_B A8	89	A8	
M_B A9	85	A9	
M_B A10	107	A10/AP	
M_B A11	84	A11	
M_B A12	83	A12	
M_B A13	119	A13	
M_B A14	80	A14	
M_B A15	78	A15	
M_B BS2	>>>	A16/BA2	
M_B BS0	>>>		
M_B_DQ[63:0]	>>>		
M_B DQ0	5	DQ0	
M_B DQ1	7	DQ1	
M_B DQ2	15	DQ2	
M_B DQ3	17	DQ3	
M_B DQ4	4	DQ4	
M_B DQ5	6	DQ5	
M_B DQ6	16	DQ6	
M_B DQ7	18	DQ7	
M_B DQ8	21	DQ8	
M_B DQ9	23	DQ9	
M_B DQ10	38	DQ10	
M_B DQ11	35	DQ11	
M_B DQ12	22	DQ12	
M_B DQ13	24	DQ13	
M_B DQ14	36	DQ14	
M_B DQ15	39	DQ15	
M_B DQ16	41	DQ16	
M_B DQ17	39	DQ17	
M_B DQ18	51	DQ18	
M_B DQ19	53	DQ19	
M_B DQ20	40	DQ20	
M_B DQ21	42	DQ21	
M_B DQ22	50	DQ22	
M_B DQ23	52	DQ23	
M_B DQ24	57	DQ24	
M_B DQ25	59	DQ25	
M_B DQ26	67	DQ26	
M_B DQ27	69	DQ27	
M_B DQ28	56	DQ28	
M_B DQ29	58	DQ29	
M_B DQ30	68	DQ30	
M_B DQ31	70	DQ31	
M_B DQ32	129	DQ32	
M_B DQ33	131	DQ33	
M_B DQ34	141	DQ34	
M_B DQ35	143	DQ35	
M_B DQ36	130	DQ36	
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M_B DQ40	147	DQ40	
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M_B DQ42	157	DQ42	
M_B DQ43	159	DQ43	
M_B DQ44	146	DQ44	
M_B DQ45	148	DQ45	
M_B DQ46	158	DQ46	
M_B DQ47	180	DQ47	
M_B DQ48	163	DQ48	
M_B DQ49	165	DQ49	
M_B DQ50	175	DQ50	
M_B DQ51	177	DQ51	
M_B DQ52	164	DQ52	
M_B DQ53	166	DQ53	
M_B DQ54	174	DQ54	
M_B DQ55	176	DQ55	
M_B DQ56	181	DQ56	
M_B DQ57	183	DQ57	
M_B DQ58	191	DQ58	
M_B DQ59	193	DQ59	
M_B DQ60	180	DQ60	
M_B DQ61	182	DQ61	
M_B DQ62	192	DQ62	
M_B DQ63	194	DQ63	
M_B DQS#0	10	DQS0#	
M_B DQS#1	27	DQS1#	
M_B DQS#2	45	DQS2#	
M_B DQS#3	62	DQS3#	
M_B DQS#4	135	DQS4#	
M_B DQS#5	152	DQS5#	
M_B DQS#6	168	DQS6#	
M_B DQS#7	186	DQS7#	
M_B DQS0	12	DQS0	
M_B DQS1	29	DQS1	
M_B DQS2	47	DQS2	
M_B DQS3	64	DQS3	
M_B DQS4	137	DQS4	
M_B DQS5	154	DQS5	
M_B DQS6	171	DQS6	
M_B DQS7	188	DQS7	
M_B_DIM0_ODT0	>>>	116	ODT0
M_B_DIM0_ODT1	>>>	120	ODT1
M_VREF_CA_DIMM1	>>>	126	VREF_CA
M_VREF_DQ_DIMM1	>>>	1	VREF_DQ
15.37 DDR3_DRAMRST#	>>>	30	RESET#
0D75V_S0	>>>	203	VTT1
	>>>	204	VTT2

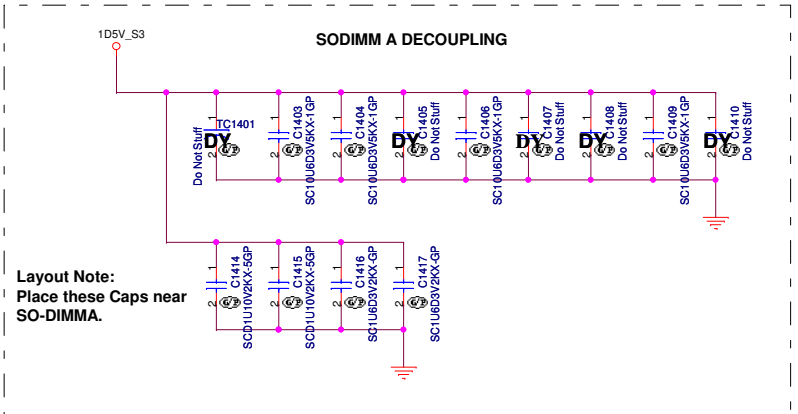
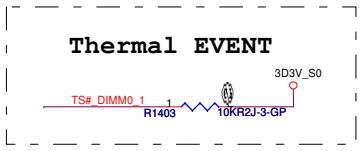
NP1	NP1		
NP2	NP2		
RAS#	>>>	M_B_RAS# 6	
WE#	>>>	M_B_WE# 6	
CAS#	>>>	M_B_CAS# 6	
CS0#	>>>	M_B_DIM0_CS#0 6	
CS1#	>>>	M_B_DIM0_CS#1 6	
CKE0	>>>	M_B_DIM0_CKE0 6	
CKE1	>>>	M_B_DIM0_CKE1 6	
CK0	>>>	M_B_DIM0_CLK_DDR0 6	
CK0#	>>>	M_B_DIM0_CLK_DDR#0 6	
CK1	>>>	M_B_DIM0_CLK_DDR1 6	
CK1#	>>>	M_B_DIM0_CLK_DDR#1 6	
DM0	11		
DM1	28		
DM2	46		
DM3	63		
DM4	136		
DM5	153		
DM6	170		
DM7	187		
SDA	200	>>>	PCH_SMBDATA 15.20.65
SCL	202	>>>	PCH_SMBCLK 15.20.65
EVENT#	198	>>>	TS#_DIMM0_1 15
VDDSPD	199		
SA0	197	SA0 DIM1	
SA1	201	SA1 DIM1	
NC#1	77	X	
NC#2	122	X	
NC#3	125	X	
VDD1	75		
VDD2	76		
VDD3	81		
VDD4	82		
VDD5	87		
VDD6	88		
VDD7	93		
VDD8	94		
VDD9	99		
VDD10	100		
VDD11	105		
VDD12	106		
VDD13	111		
VDD14	112		
VDD15	117		
VDD16	118		
VDD17	123		
VDD18	124		
VSS	2		
VSS	3		
VSS	8		
VSS	9		
VSS	13		
VSS	14		
VSS	19		
VSS	20		
VSS	25		
VSS	26		
VSS	31		
VSS	32		
VSS	37		
VSS	38		
VSS	43		
VSS	44		
VSS	48		
VSS	49		
VSS	54		
VSS	55		
VSS	59		
VSS	60		
VSS	61		
VSS	65		
VSS	66		
VSS	71		
VSS	72		
VSS	127		
VSS	128		
VSS	133		
VSS	134		
VSS	138		
VSS	139		
VSS	144		
VSS	145		
VSS	150		
VSS	151		
VSS	155		
VSS	156		
VSS	161		
VSS	162		
VSS	167		
VSS	168		
VSS	172		
VSS	173		
VSS	178		
VSS	179		
VSS	184		
VSS	185		
VSS	189		
VSS	190		
VSS	195		
VSS	196		
VSS	205		
VSS	206		
VREF_CA	184		
VREF_DQ	185		
RESET#	189		
RESET#	190		
RESET#	195		
RESET#	196		
RESET#	205		
RESET#	206		

DDR3-204P-43-GP
62.10017.N71



Note:
If SA0_DIM0 = 0, SA1_DIM0 = 0
SO-DIMMA SPD Address is 0xA0
SO-DIMMA TS Address is 0x30

If SA0_DIM0 = 0, SA1_DIM0 = 1
SO-DIMMA SPD Address is 0xA2
SO-DIMMA TS Address is 0x32



Layout Note:
Place these Caps near SO-DIMMA.

起点主板维修网 www.qdzbwx.com

DV15 HR Vos GIGA HDMI NoSurge


Wistron Corporation
21F, 88, Sec. 1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

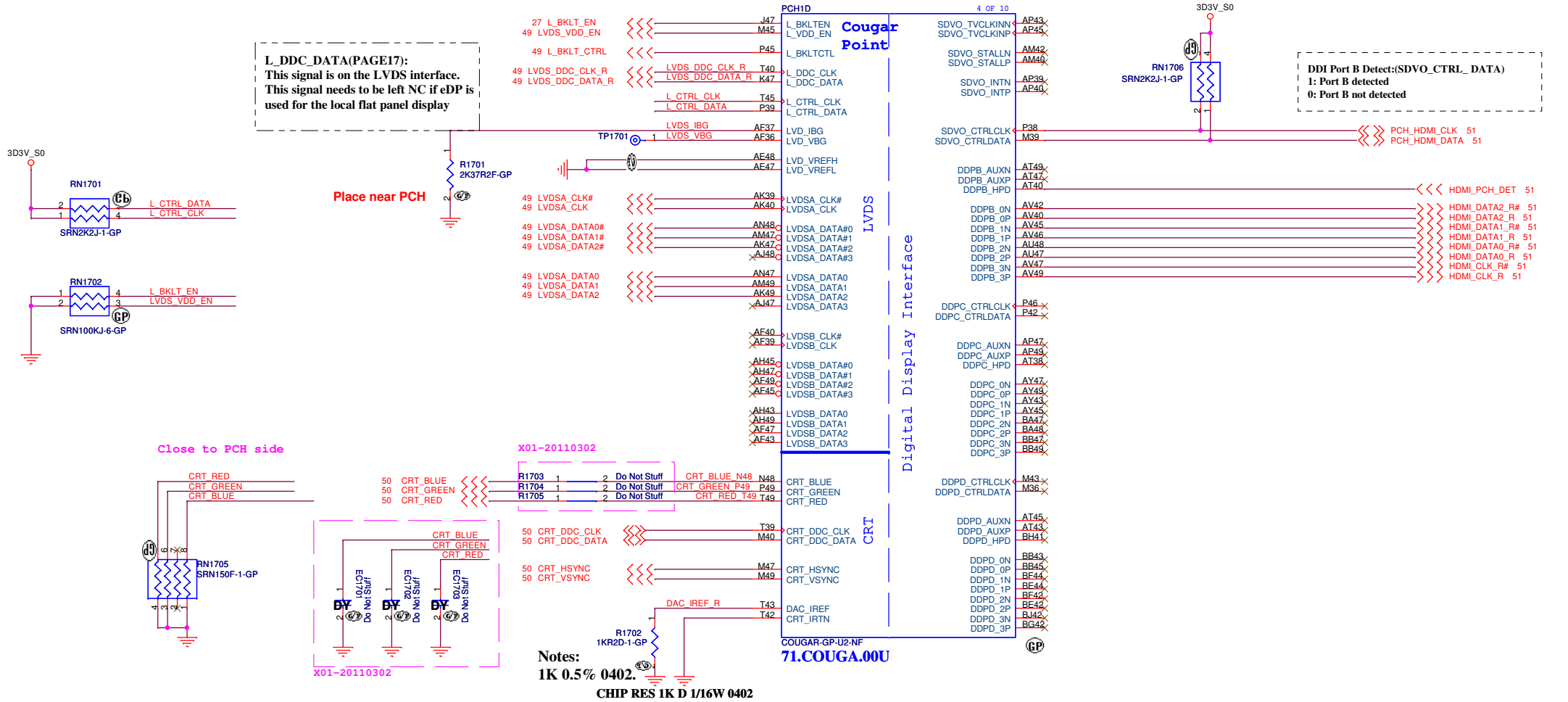
Title: **DDR3-SODIMM2**

Size	Document Number	Rev
Custom	Enrico/Caruso 15 HR	X01
Date:	Thursday, June 02, 2011	Sheet 14 of 104

(Blanking)

DV15 HR Vos GIGA HDMI NoSurge

		Wistron Corporation 21F, 88, Sec. 1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.
Title		
Reserved		
Size	Document Number	Rev
A3	Enrico/Caruso 15 HR	X01
Date: Thursday, June 02, 2011	Sheet 16	of 104



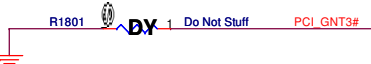
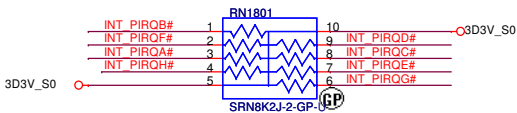
L_DDC_DATA(PAGE17):
This signal is on the LVDS interface.
This signal needs to be left NC if eDP is used for the local flat panel display

DDI Port B Detect:(SDVO_CTRL_DATA)
1: Port B detected
0: Port B not detected

Notes:
1K 0.5% 0402.
CHIP RES 1K D 1/16W 0402

SSID = PCH

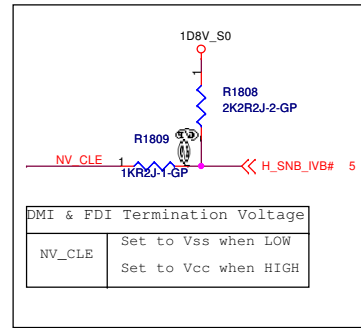
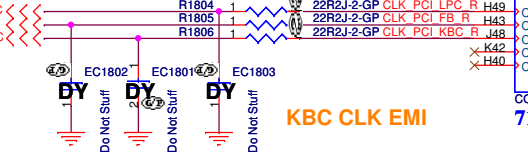
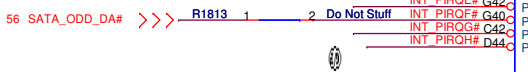
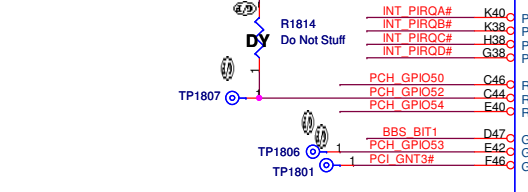
起点主板维修网 www.qdzbwx.com



Al6 swap override Strap/Top-Block Swap Override jumper	
PCI_GNT#3	Low = Al6 swap override/Top-Block Swap Override enabled High = Default



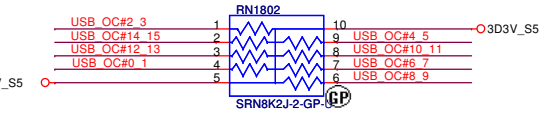
BOOT BIOS Strap		
GNT1#/GPIO51	SATA1GP/GPIO19	BOOT BIOS Location
0	0	LPC
0	1	Reserved
1	0	Reserved
1	1	SPI (Default)



DMI & FDI Termination Voltage	
NV_CLE	Set to Vss when LOW
	Set to Vcc when HIGH

USB Ext. port 1 (HS)
External debug port use on Huron river platform
USB Table

Pair	Device
0	X
1	USB Ext. port 1 (HS)
2	X
3	X
4	X
5	CARD READER
6	X
7	X
8	USB Ext. port 2
9	USB Ext. port 3
10	X
11	Mini Card1 (WLAN)
12	CAMERA
13	X



DV15 HR Vos GIGA HDMI NoSurge

Wistron Corporation
21F, 88, Sec. 1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.

Title: **PCH (PCI/USB/NVRAM)**

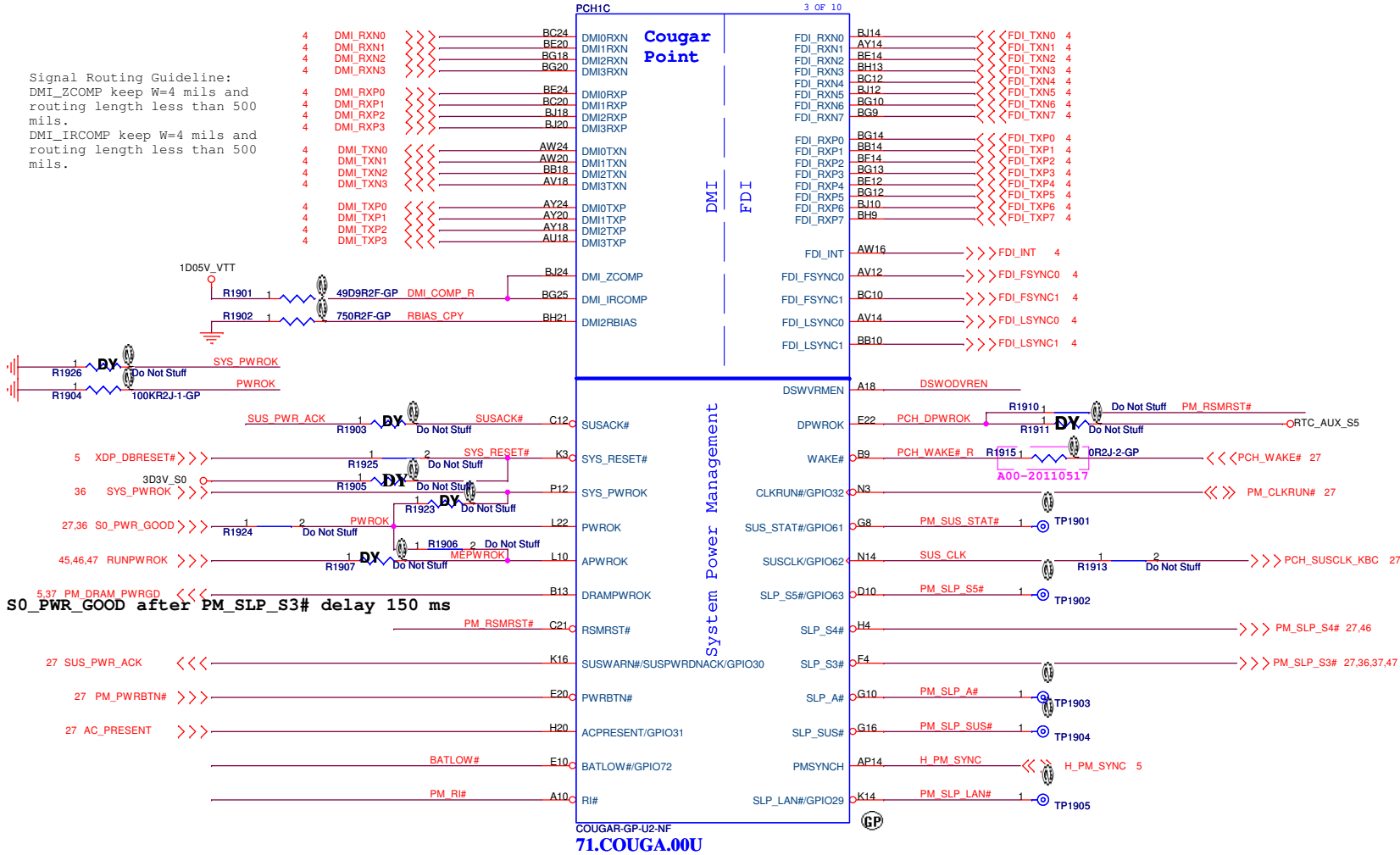
Size A3 Document Number **Enrico/Caruso 15 HR** Rev **X01**

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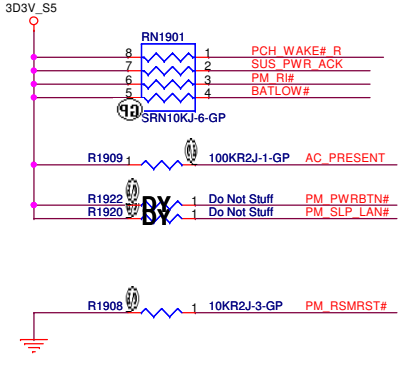
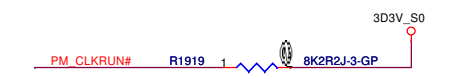
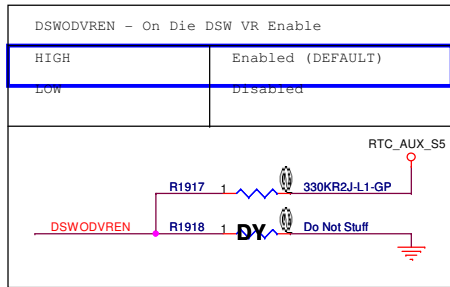
SSID = PCH



Signal Routing Guideline:
 DMI_ZCOMP keep W=4 mils and routing length less than 500 mils.
 DMI_IRCOMP keep W=4 mils and routing length less than 500 mils.



S0_PWR_GOOD after PM_SLP_S3# delay 150 ms

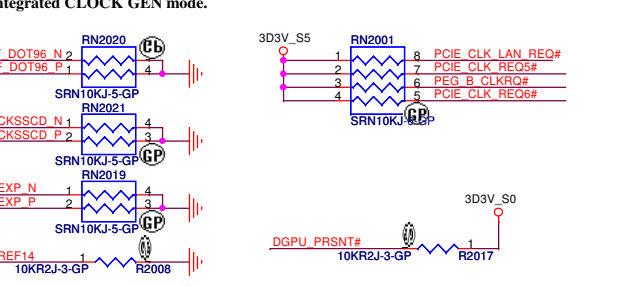
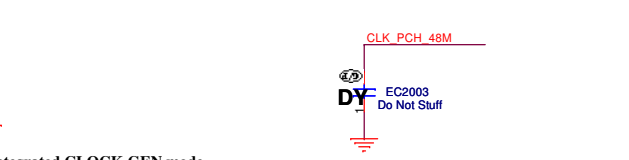
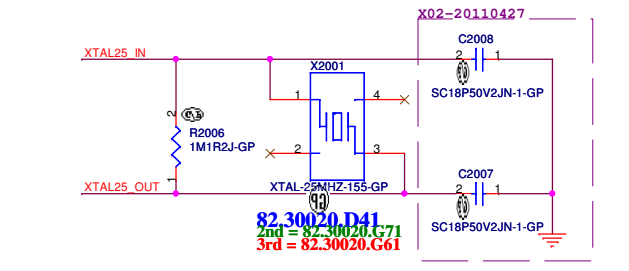
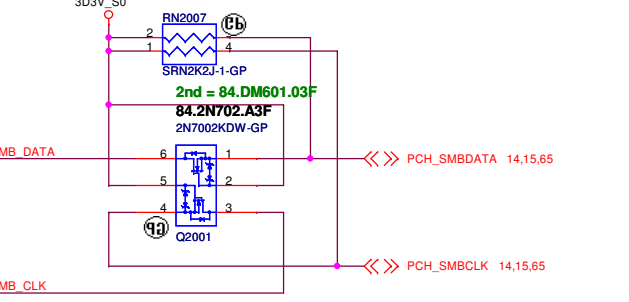
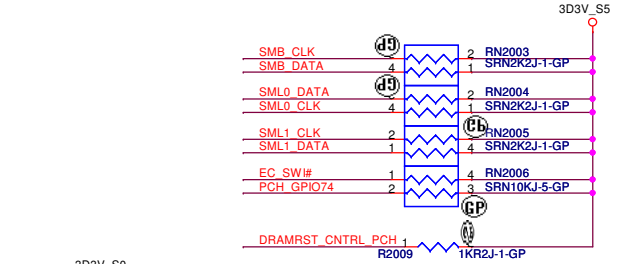
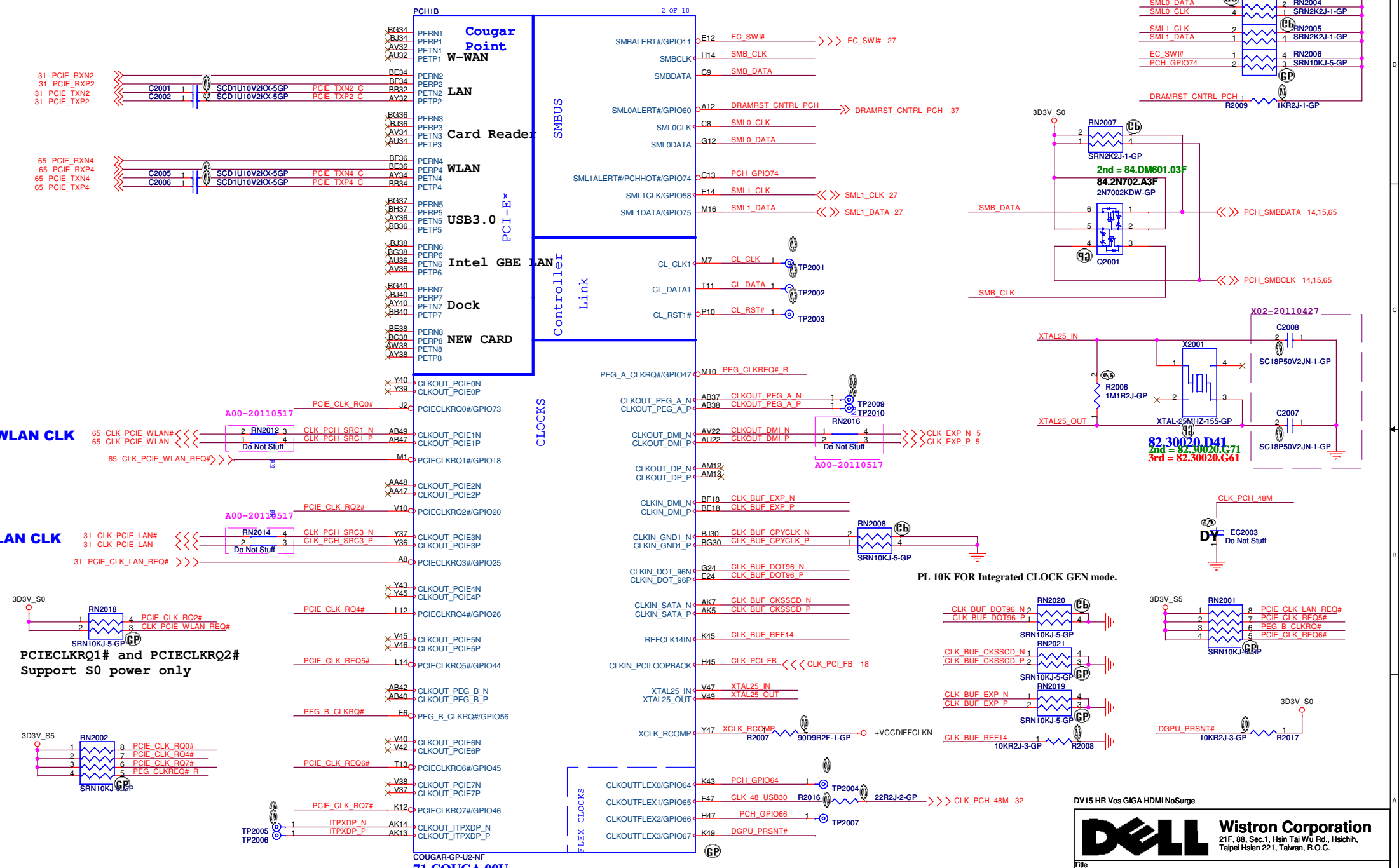


Wistron Corporation
 21F, 88, Sec. 1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.

Title: **PCH (DM I/FDI/PM)**
 Size: A3
 Document Number: **Enrico/Caruso 15 HR**
 Date: Thursday, June 02, 2011
 Sheet: 19 of 104

Rev: **X01**

SSID = PCH



WLAN CLK

LAN CLK

PCIECLKRQ1# and PCIECLKRQ2# Support S0 power only

PL 10K FOR Integrated CLOCK GEN mode.

71.COUGA.00U

- Prioritize 27/14/24/48/25-MHz FLEX on FLEX1 and FLEX3
 - Do not configure 27/14/24/48/25-MHz FLEX clock on FLEX0 and FLEX2
 if more than 2 PCI clocks + PCI loopback are routed.

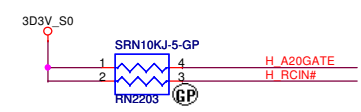
DV15 HR Vos GIGA HDMI NoSurge

DELL Wistron Corporation
 21F, 88, Sec. 1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.

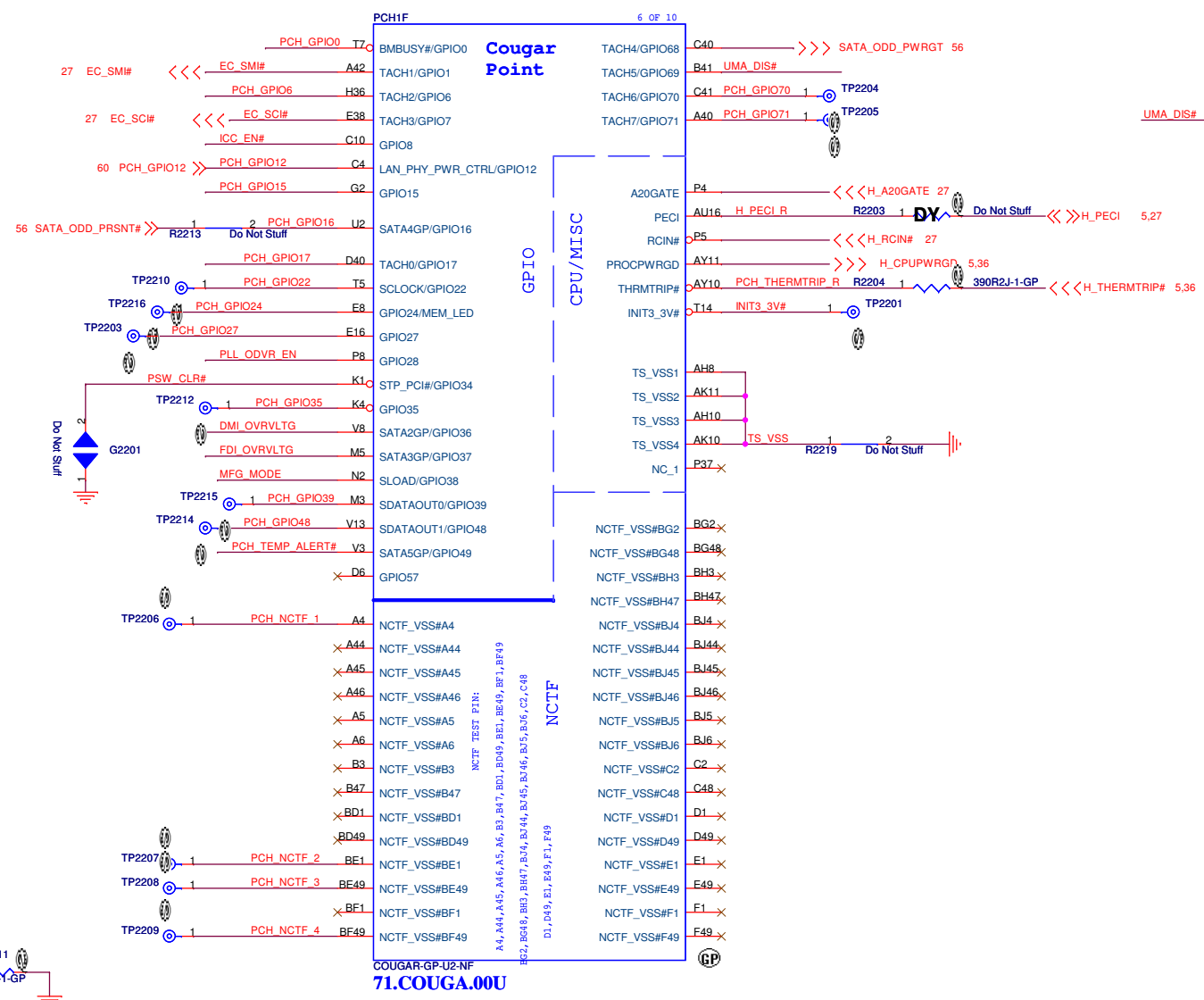
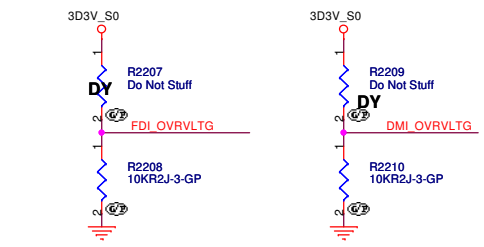
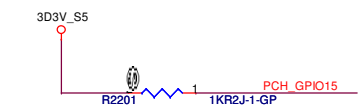
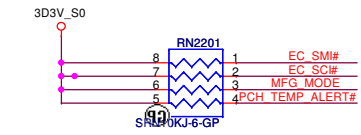
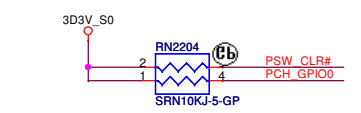
Title: **PCH (PCI-E/SMBUS/CLOCK/CL)**

Size A3 Document Number: **Enrico/Caruso 15 HR** Rev: **X01**

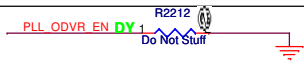
Date: Thursday, June 02, 2011 Sheet 20 of 104



GPIO27 has a weak[20K] internal pull up. To enable on-die PLL Voltage regulator, should not place external pull down.



PLL ON DIE VR ENABLE
 NOTE: This signal has a weak internal pull-up 20k
 ENABLED -- HIGH (R2212 UNSTUFFED) DEFAULT
 DISABLED -- LOW (R2212 STUFFED)



DV15 HR Vos GIGA HDMI NoSurge

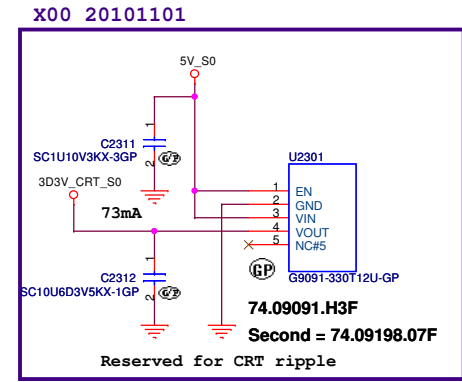
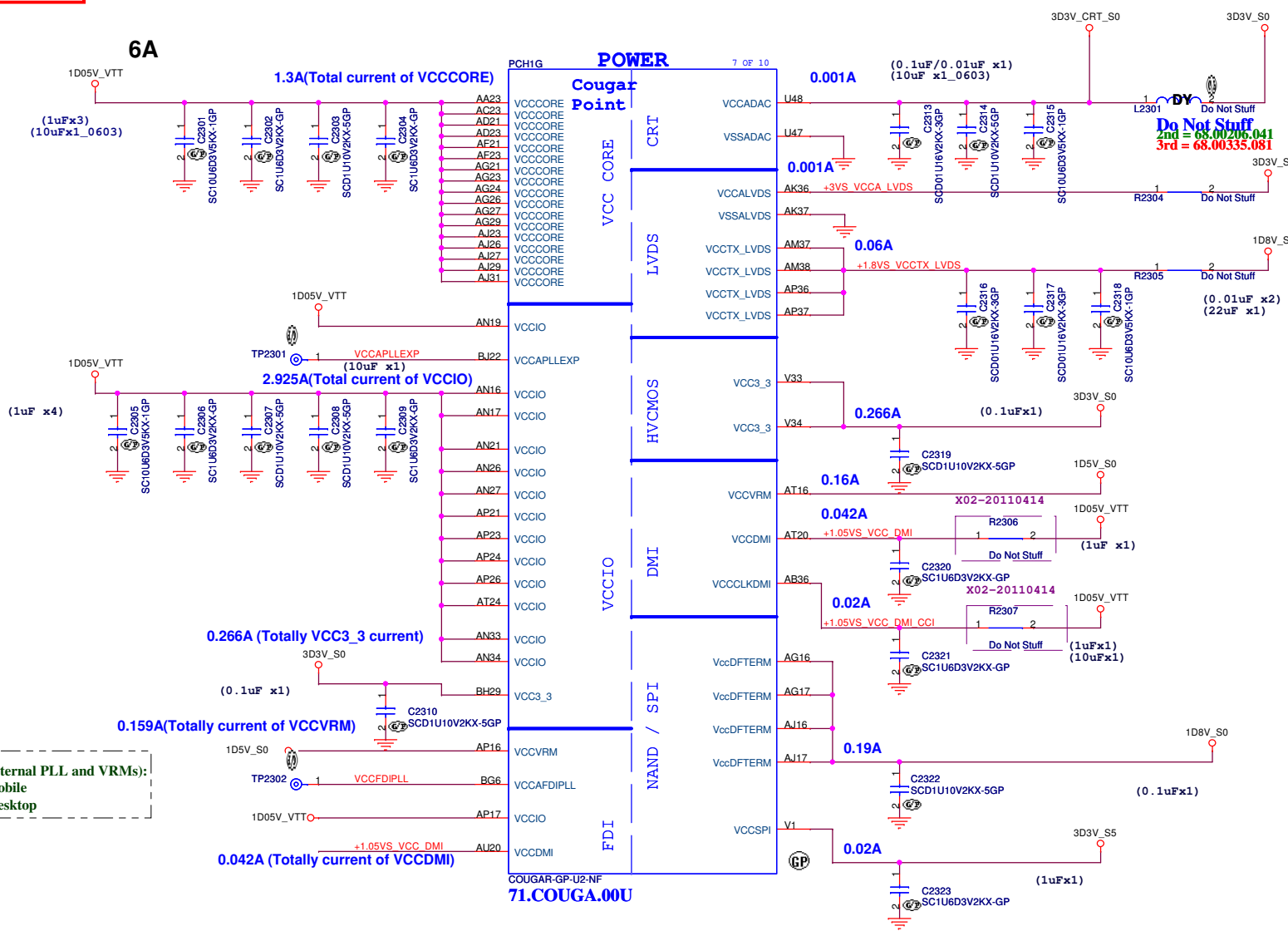
DELL Wistron Corporation
 21F, 88, Sec. 1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.

Title: **PCH (GPIO/CPU)**

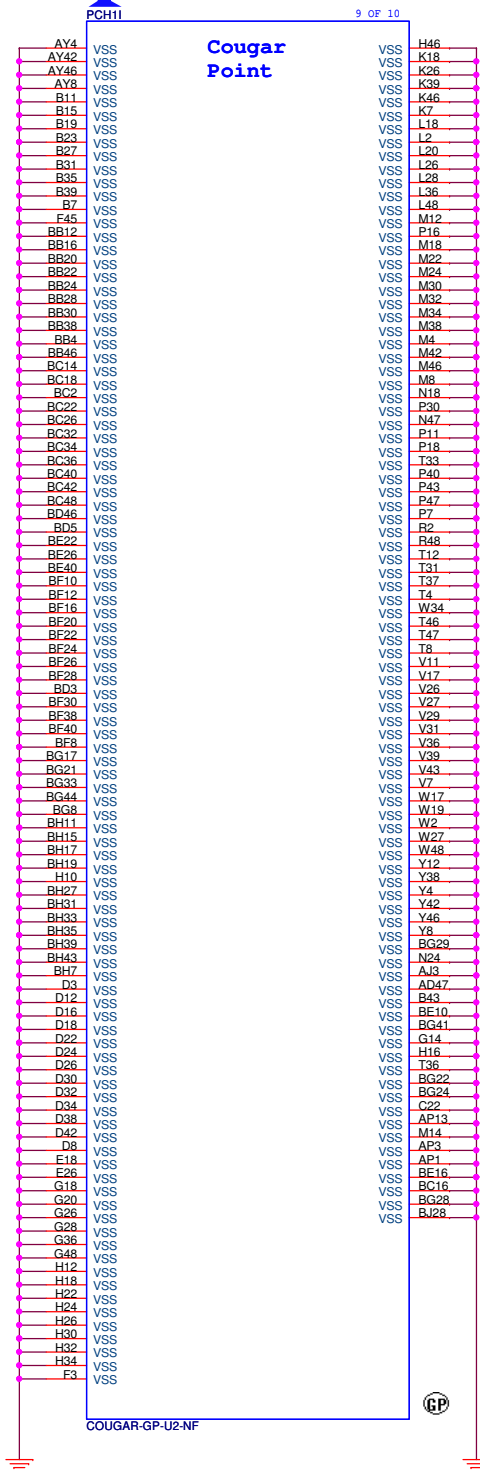
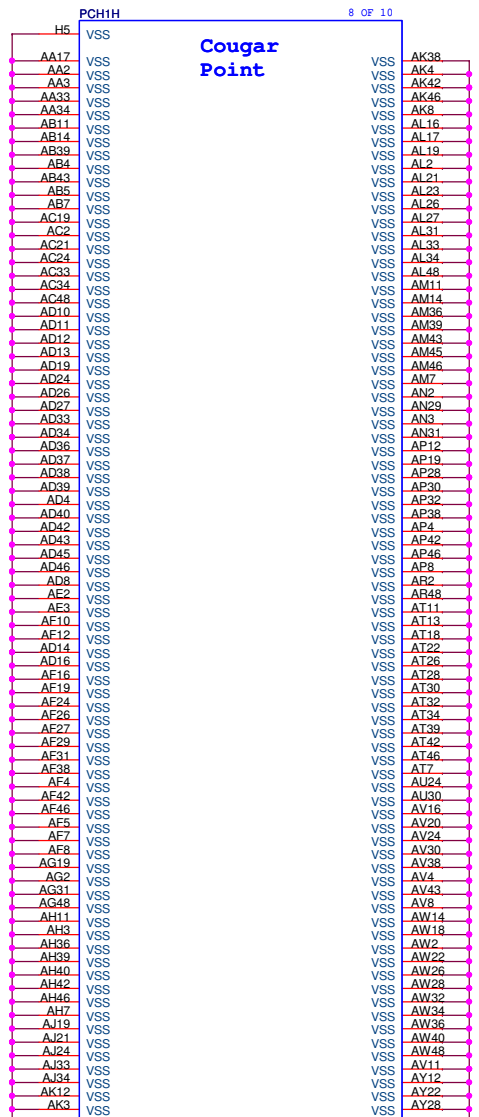
Size A3 Document Number: **Enrico/Caruso 15 HR** Rev: **X01**

Date: Thursday, June 02, 2011 Sheet 22 of 104

SSID = PCH



SSID = PCH



起点主板维修网 www.qdzbwx.com

DV15 HR Vos GIGA HDMI NoSurge

DELL Wistron Corporation
21F, 88, Sec. 1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.

Title: **PCH (VSS)**

Size A3	Document Number	Rev
	Enrico/Caruso 15 HR	X01

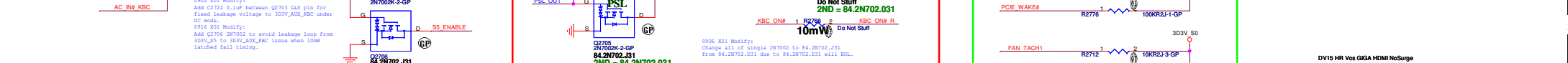
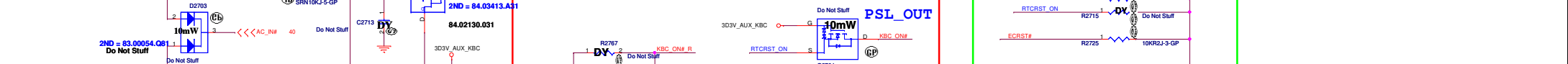
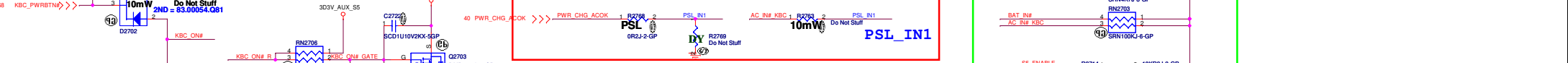
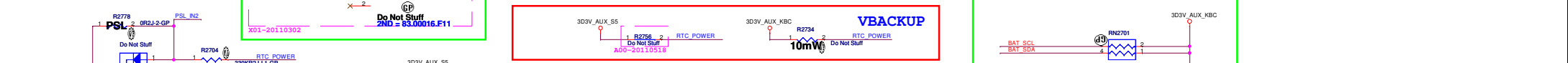
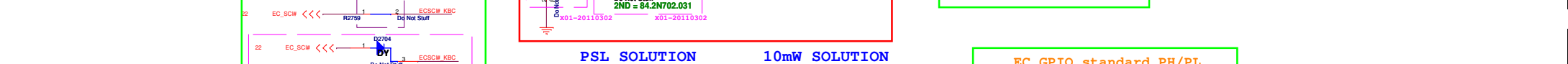
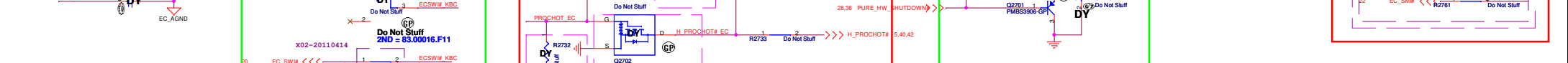
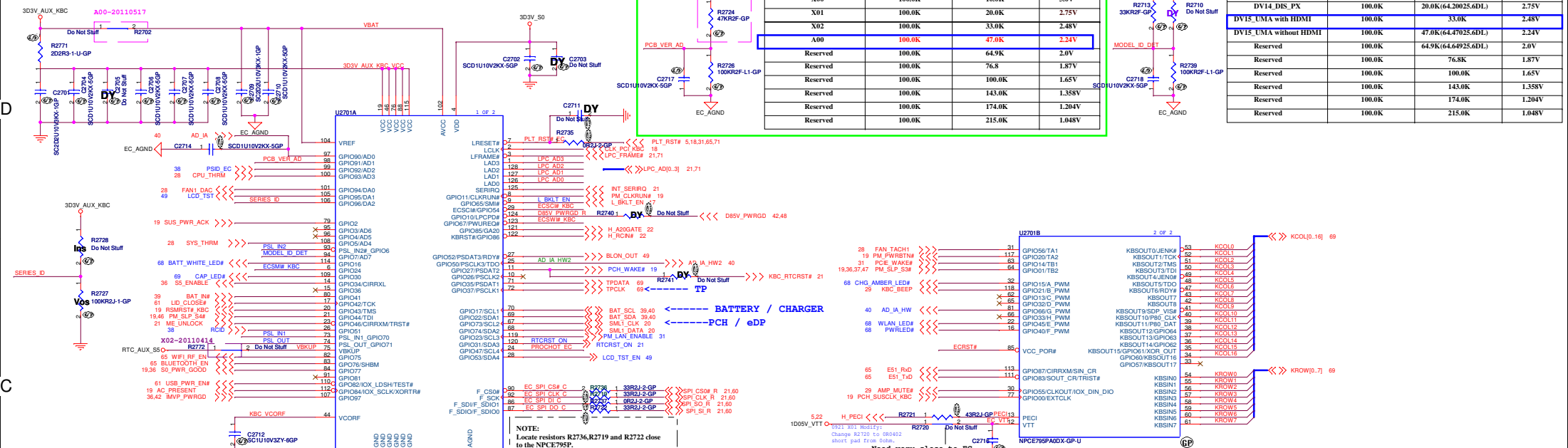
Date: Thursday, June 02, 2011 Sheet 25 of 104

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DV15 HR Vos GIGA HDMI NoSurge



Title		
Reserved		
Size A3	Document Number Enrico/Caruso 15 HR	Rev X01
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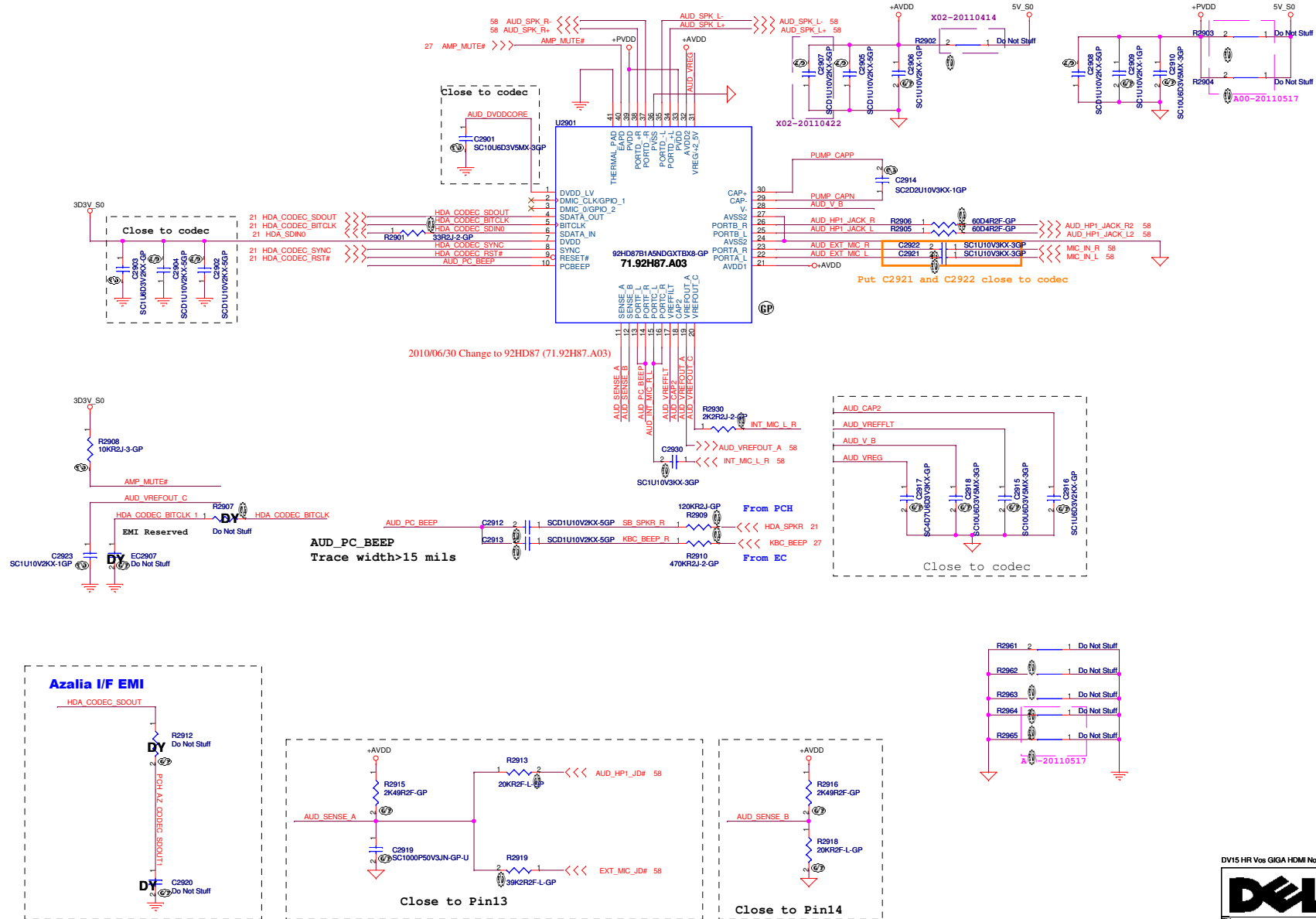
NOTES:
Please make sure there's no pull-down resistor on USB_PWR_EN#,AC_PRESENT,ES1_TXD.

Wistron Corporation
21F, 88, Sec. 1, Hsin Tai Wu Rd., Hsinchu, Taipei Hsein 301, Taiwan, R.O.C.

File: **KBC NuvoTon NPCE795**
Size: Document Number
A2: **Enrico/Caruso 15 HR**
Date: 11/09/2011, June 02, 2011 Sheet 27 of 104 Rev X01

SSID = AUDIO

起点主板维修网 www.qdzbxw.com



DV15 HR Vos GIGA HDMI NoSurge

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsiehshih,
Taippei Hsien 221, Taiwan, R.O.C.

Title			Audio Codec 92HD87B1
Size	Document Number	Rev	
Custom	Enrico/Caruso 15 HR	X01	
Date: Thursday, June 02, 2011	Sheet 29	of	104

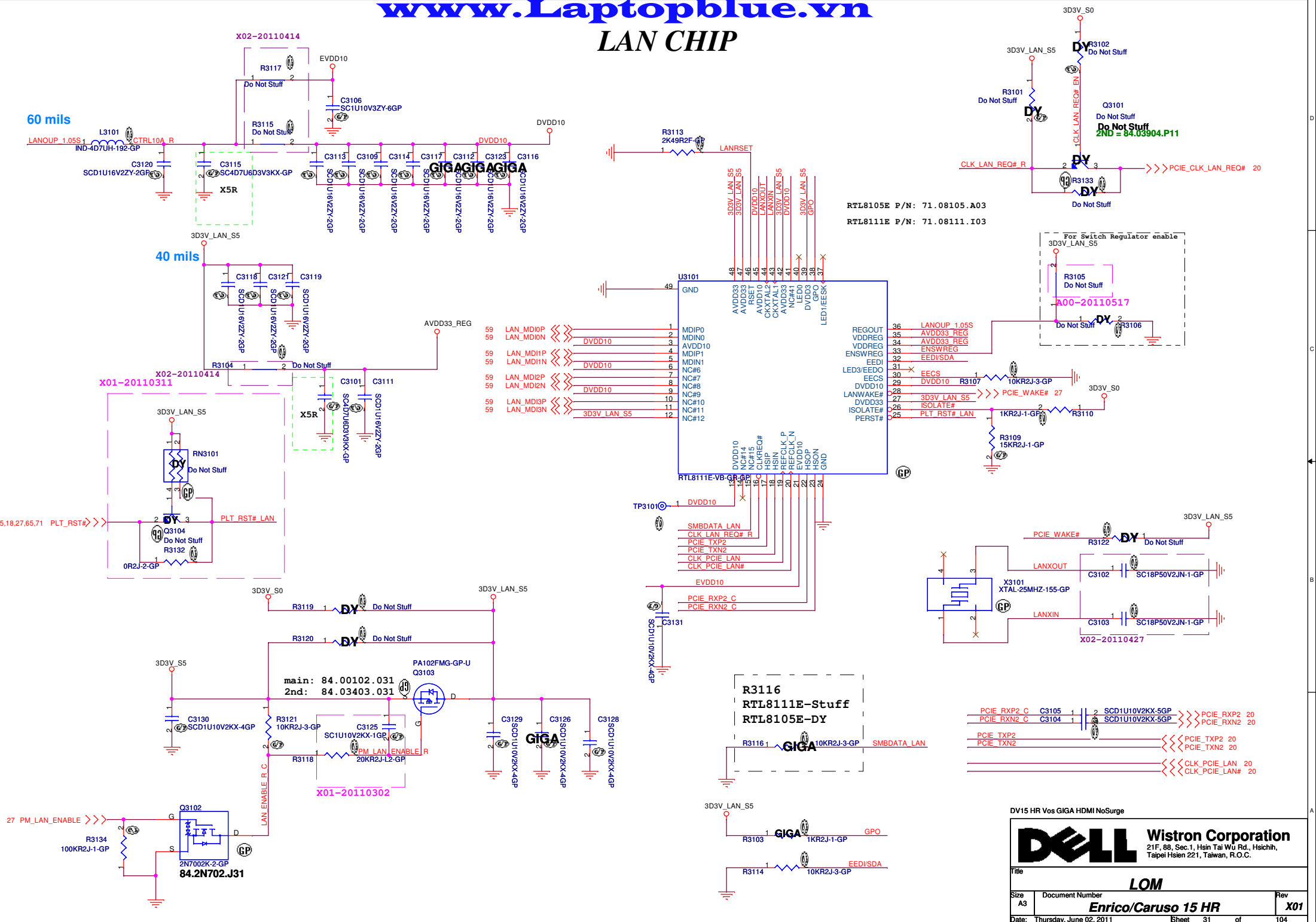
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DV15 HR Vos GIGA HDMI NoSurge

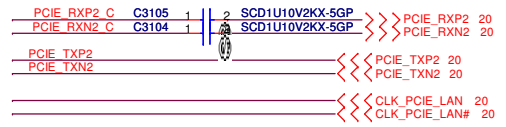
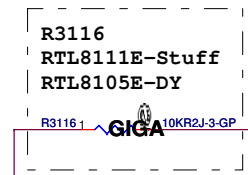
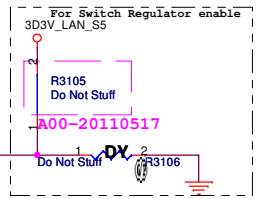


Title		
Reserved		
Size	Document Number	Rev
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LAN CHIP



RTL8105E P/N: 71.08105.A03
 RTL8111E P/N: 71.08111.I03



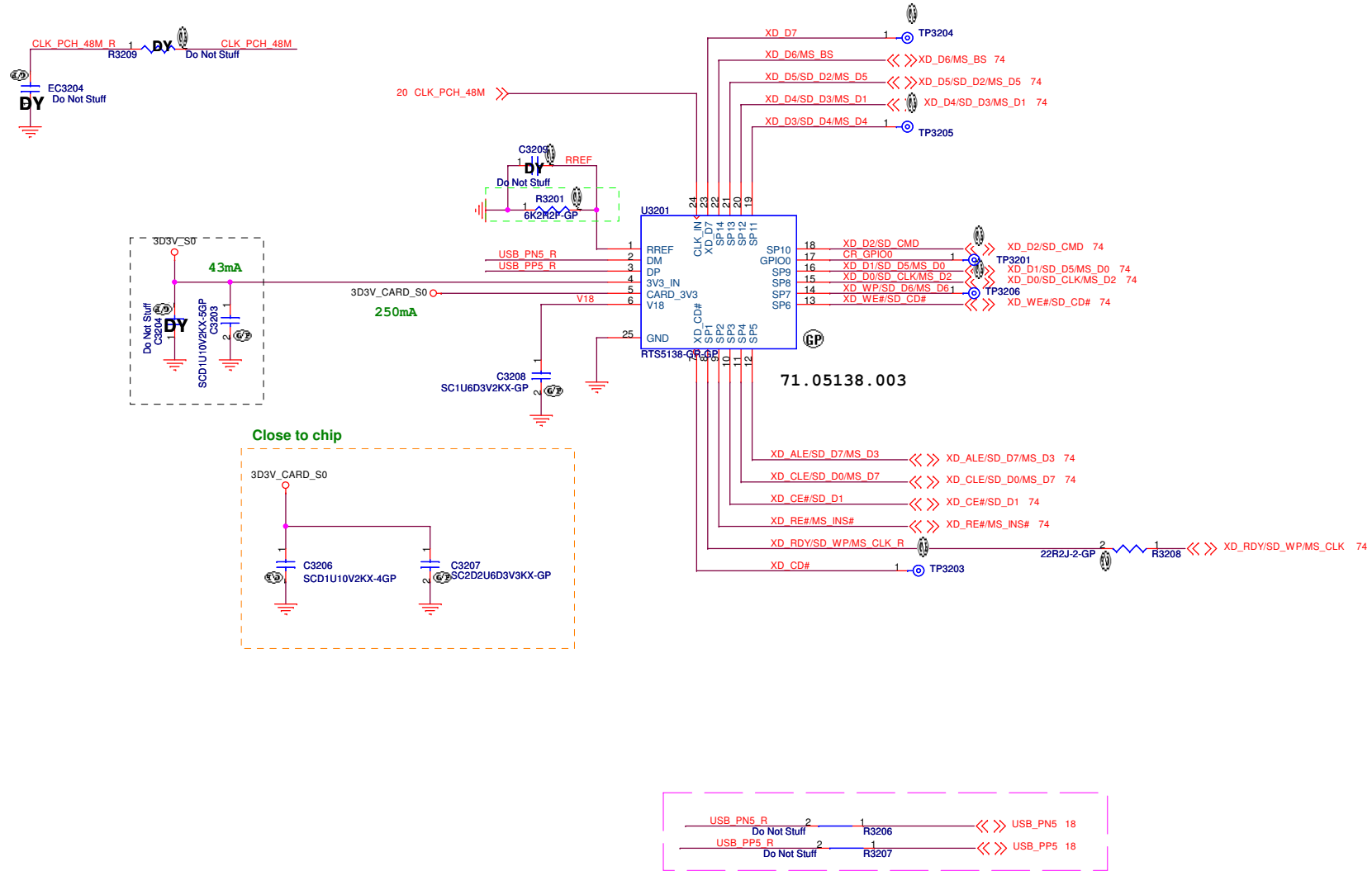
DV15 HR Vos GIGA HDMI NoSurge

Wistron Corporation
 21F, 88, Sec. 1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.

Title: **LOM**

Size: A3	Document Number: Enrico/Caruso 15 HR	Rev: X01
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SSID = SDIO



A00-20110530

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DV15 HR Vos GIGA HDMI NoSurge



Title		
Reserved		
Size A3	Document Number Enrico/Caruso 15 HR	Rev X01
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DV15 HR Vos GIGA HDMI NoSurge

	Wistron Corporation 21F, 88, Sec. 1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.
---------------------------------------------------------------------------------------	--------------------------------------------------------------------------------------------------------------

Title		
Reserved		
Size	Document Number	Rev
A3	Enrico/Caruso 15 HR	X01
Date: Thursday, June 02, 2011	Sheet 34 of	104

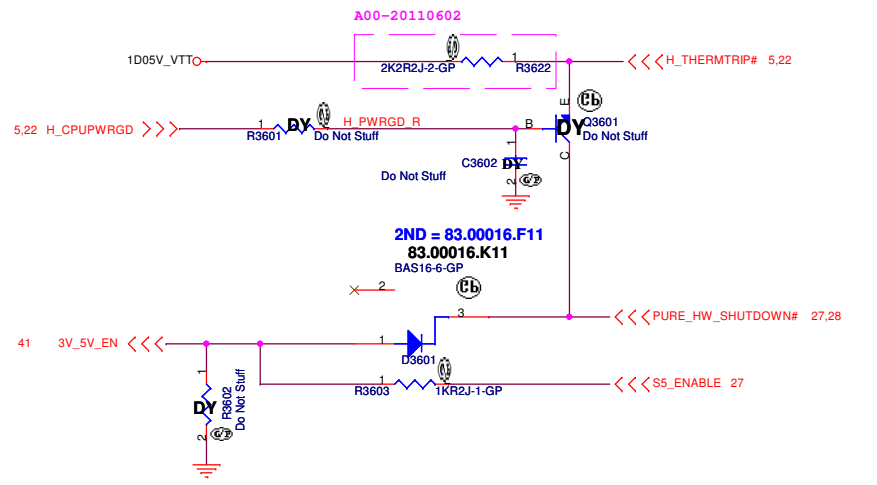
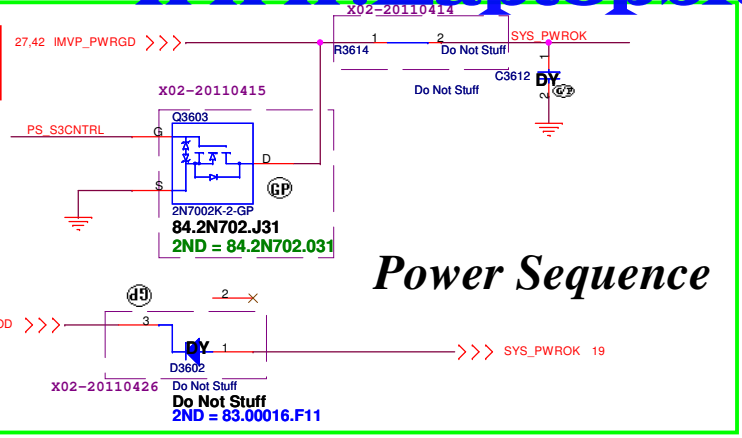
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DV15 HR Vos GIGA HDMI NoSurge

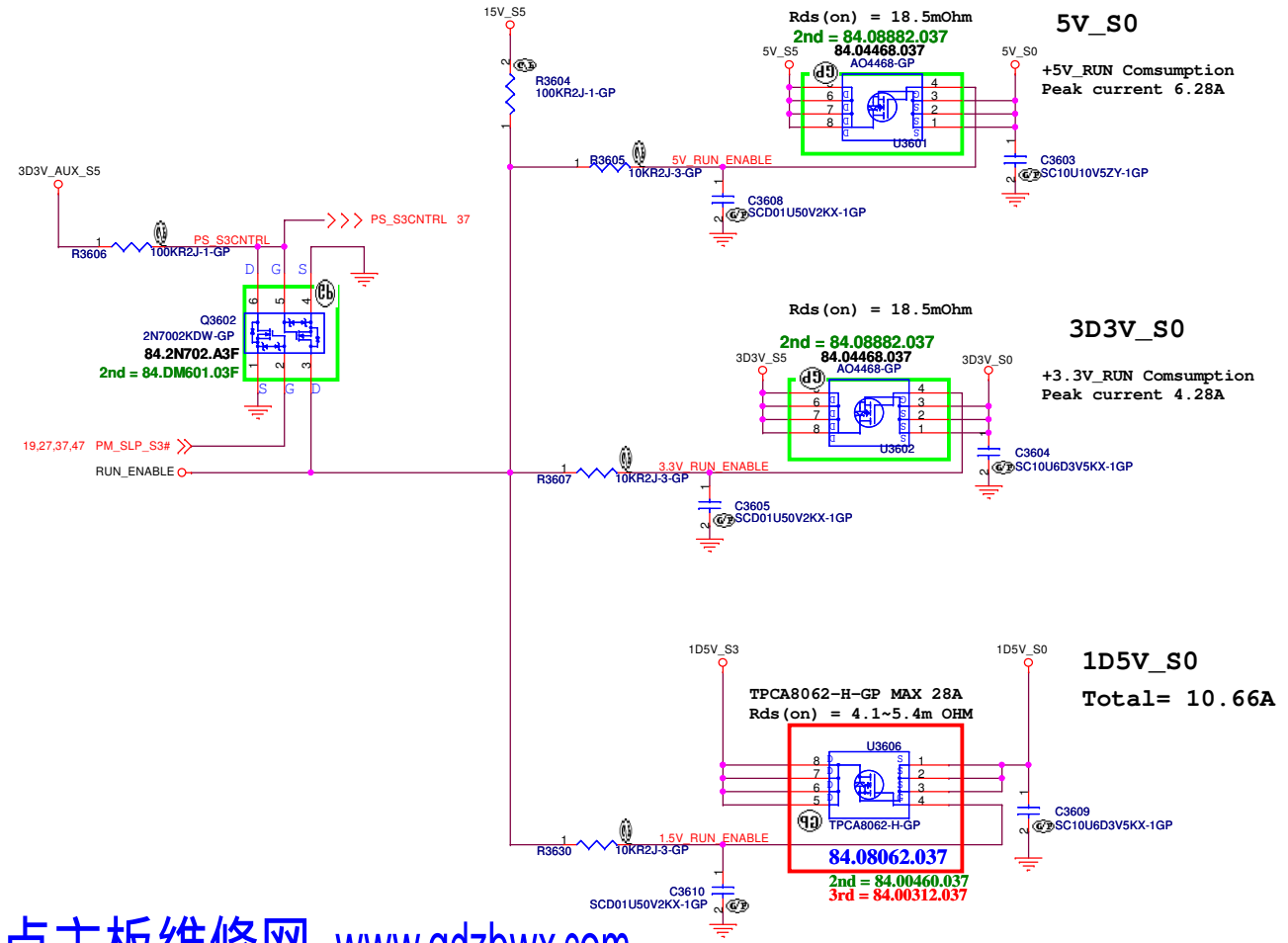


Title		
Reserved		
Size A3	Document Number Enrico/Caruso 15 HR	Rev X01
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SSID = Reset.Suspend



ROSA Run Power



DV15 HR Vos GIGA HDMI NoSurge

DELL Wistron Corporation

21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.

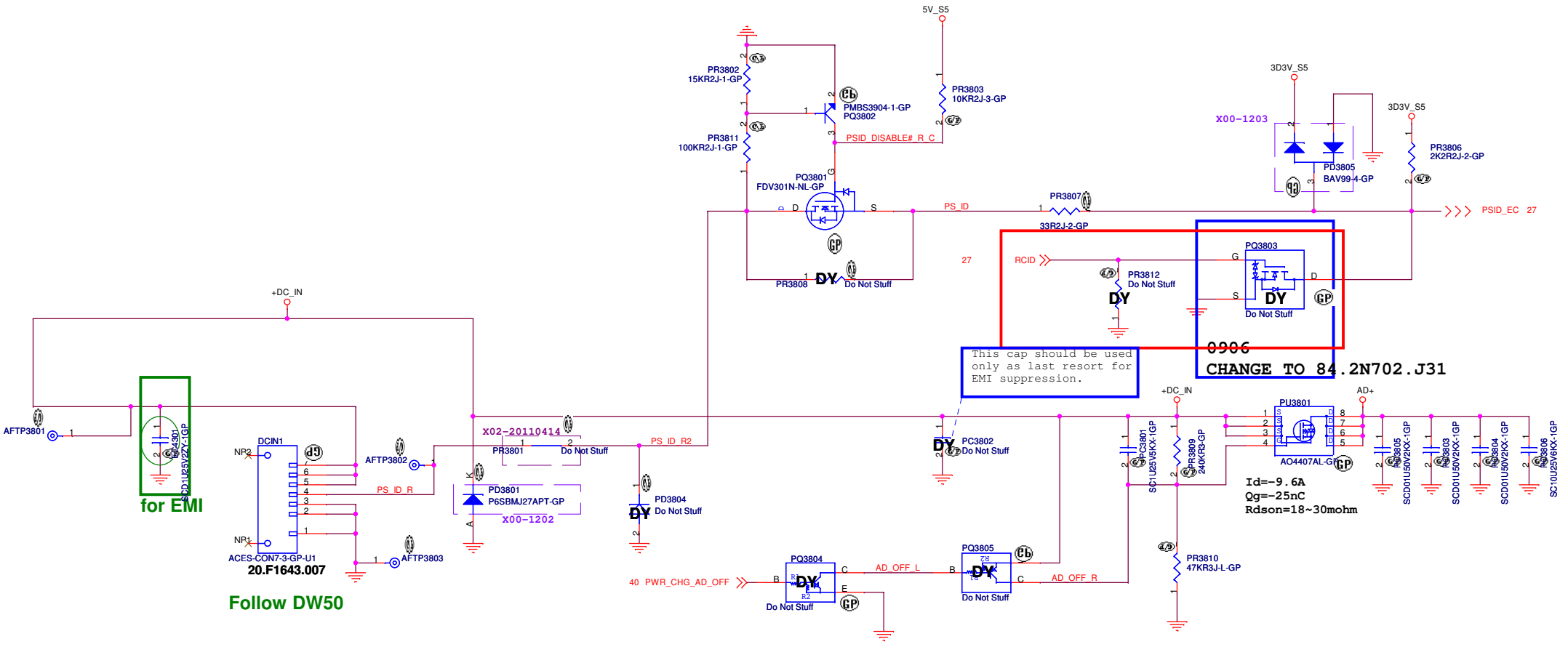
Title: **Power Plane Enable**

Size A3 Document Number: **Enrico/Caruso 15 HR** Rev: **X01**

Date: Thursday, June 02, 2011 Sheet 36 of 104

SSID = PWR.Support

DCin CONN



for EMI

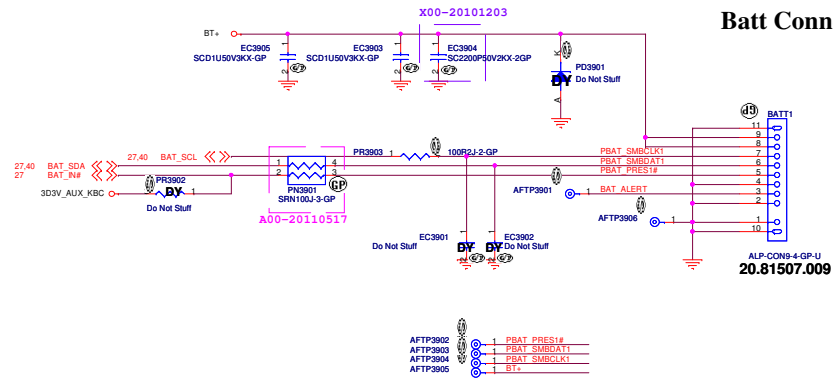
Follow DW50

This cap should be used only as last resort for EMI suppression.

CHANGE TO 84.2N702.J31

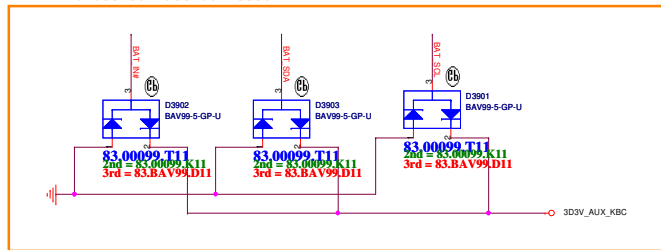
Id = -9.6A
 Qg = 25nC
 Rds(on) = 18~30mohm

Batt Connector



For actual location, need to be swap all pin

Close to Batt Connector



SSID = Charger

起点主板维修网 www.qdzbwx.com

EE need pull high and net pink

0802 Rename H_PROCHOT#

27.42 H_PROCHOT#

PWR_CHG_CMPIN

AD_IA_HW 27

PWR_CHG_CMPIN

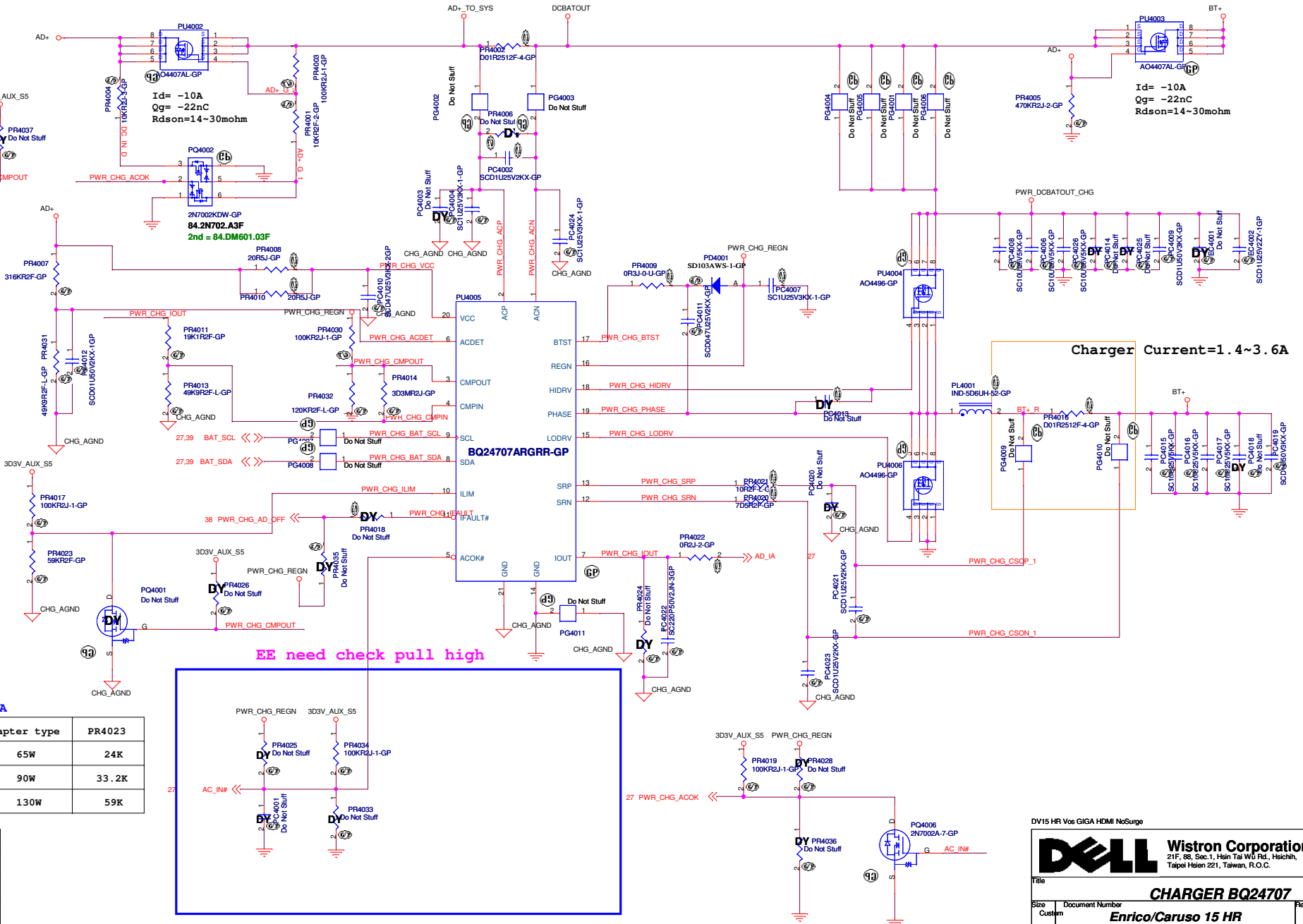
AD_IA_HW2 27


EC code only BQ24707

ROSA

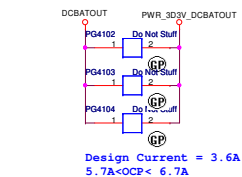
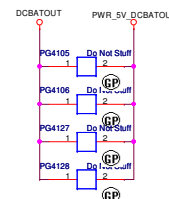
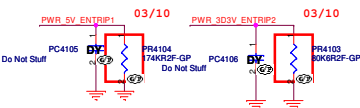
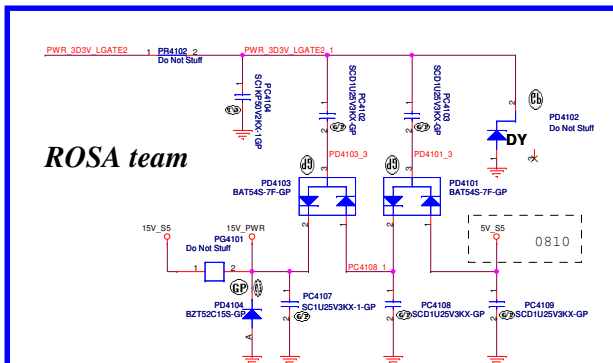
Adapter type	PR4023
65W	24K
90W	33.2K
130W	59K

H_PROCHOT#	AD_IA_HW	AD_IA_HW2
65W	0	0
90W	1	0
130W	0	1



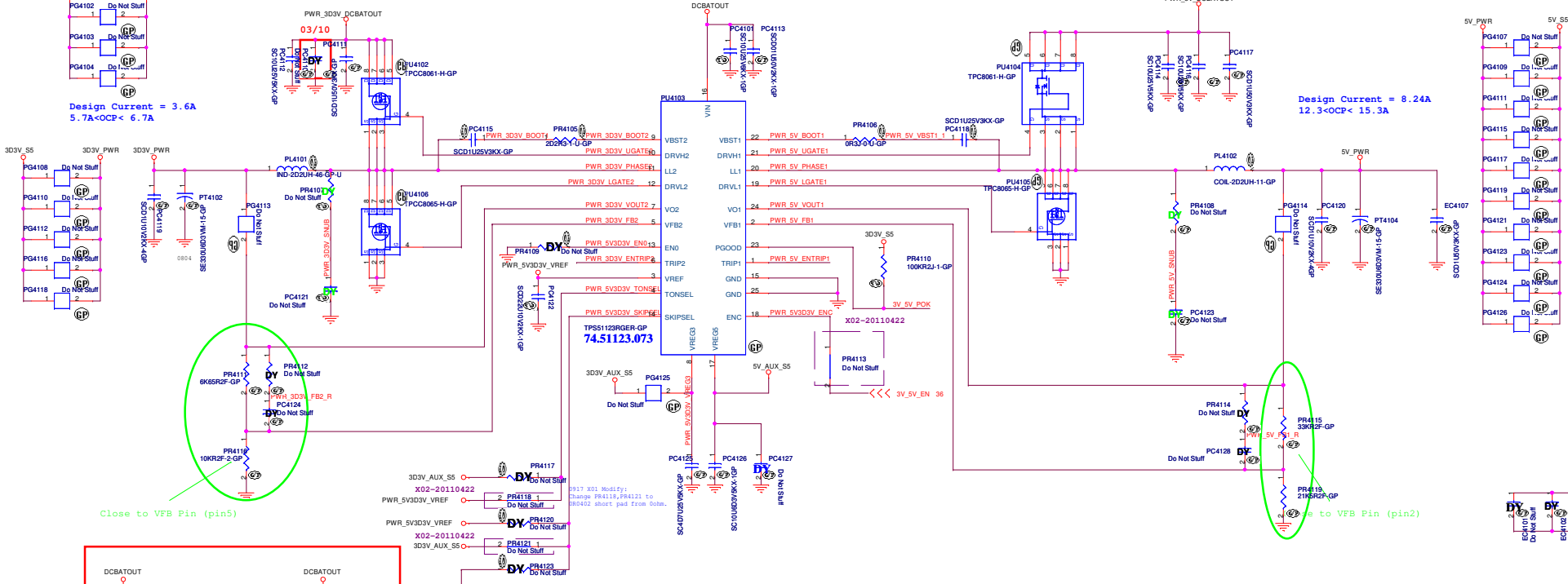

Wistron Corporation
 21F, 88, Sec.1, Hsin Tai Wu Rd., Heichih, Taipei Hsien 221, Taiwan, R.O.C.
 Title: **CHARGER BQ24707**
 Size: Custom Document Number: **Enrico/Caruso 15 HR** Rev: X01
 Date: Thursday, June 02, 2011 Sheet: 40 of 104

SSID = PWR.Plane.Regulator_5v3p3v



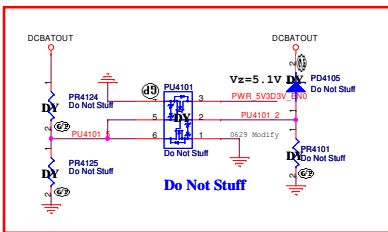
Design Current = 3.6A
5.7A < OCP < 6.7A

Design Current = 8.24A
12.3 < OCP < 15.3A



Close to VFB Pin (pin5)

Close to VFB Pin (pin2)

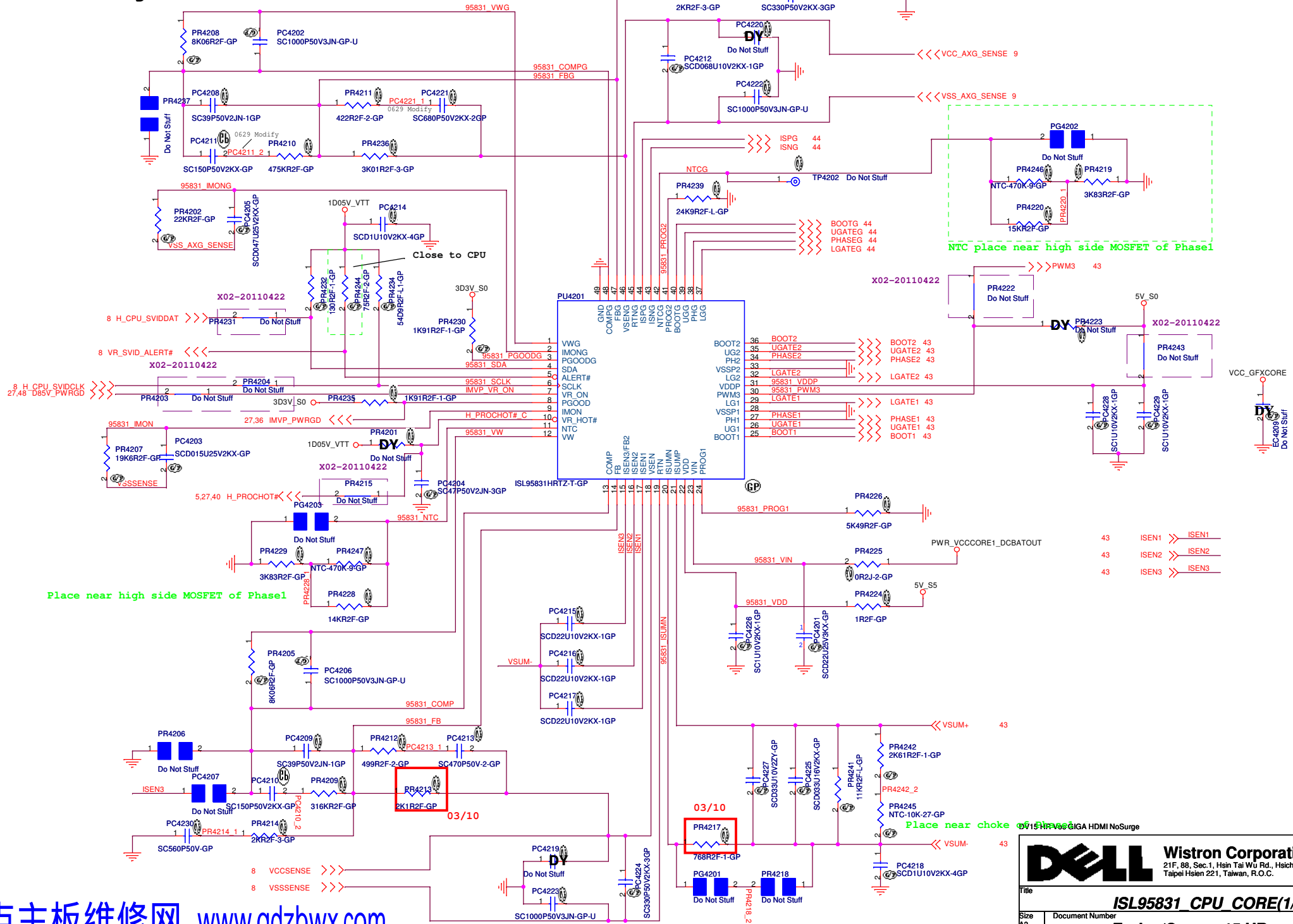


TONSEL	CH1	CH2
GND	200kHz	250kHz
VREF	300kHz	375kHz
VREG3 or VREG5	400kHz	500kHz

SKIPSEL	VREG3 or VREG5	VREF (2V)	GND
Operating Mode	OOA Auto Skip	Auto Skip	PWM only

I/P cap: 10u 25V K0805 X5R/ 78.10622.51L
 Inductor: 2.20UH PCMC104T-2R2 Cynotec 7mohm Isat =27Arms 68.2R210.20C
 O/P cap: 33006.3V M6.345.7 15mOhm 3.16Arms Matsuki/77.53371.04L
 H/S: TPC8061-H / 21mohm/30mohm@4.5Vgs/ 84.08061.037
 L/S: TPC8065-H / 12mohm/15mohm@4.5Vgs/ 84.08065.037

SSID = CPU.Regulator

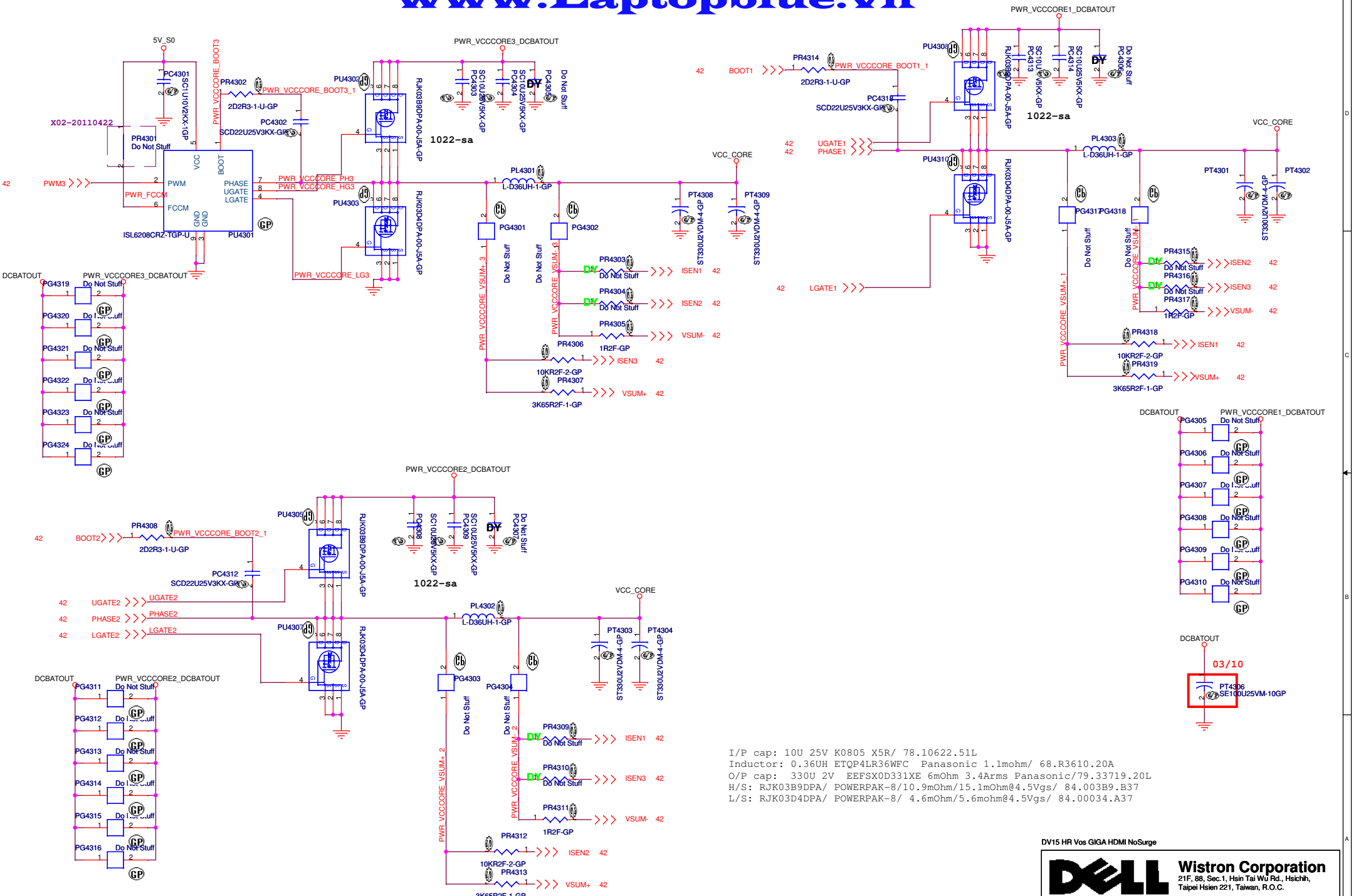


DELL Wistron Corporation
 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
 Taipei Hsien 221, Taiwan, R.O.C.

Title: **ISL95831 CPU CORE(1/3)**

Size A3	Document Number	Rev
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Date: Thursday, June 02, 2011 Sheet 42 of 104



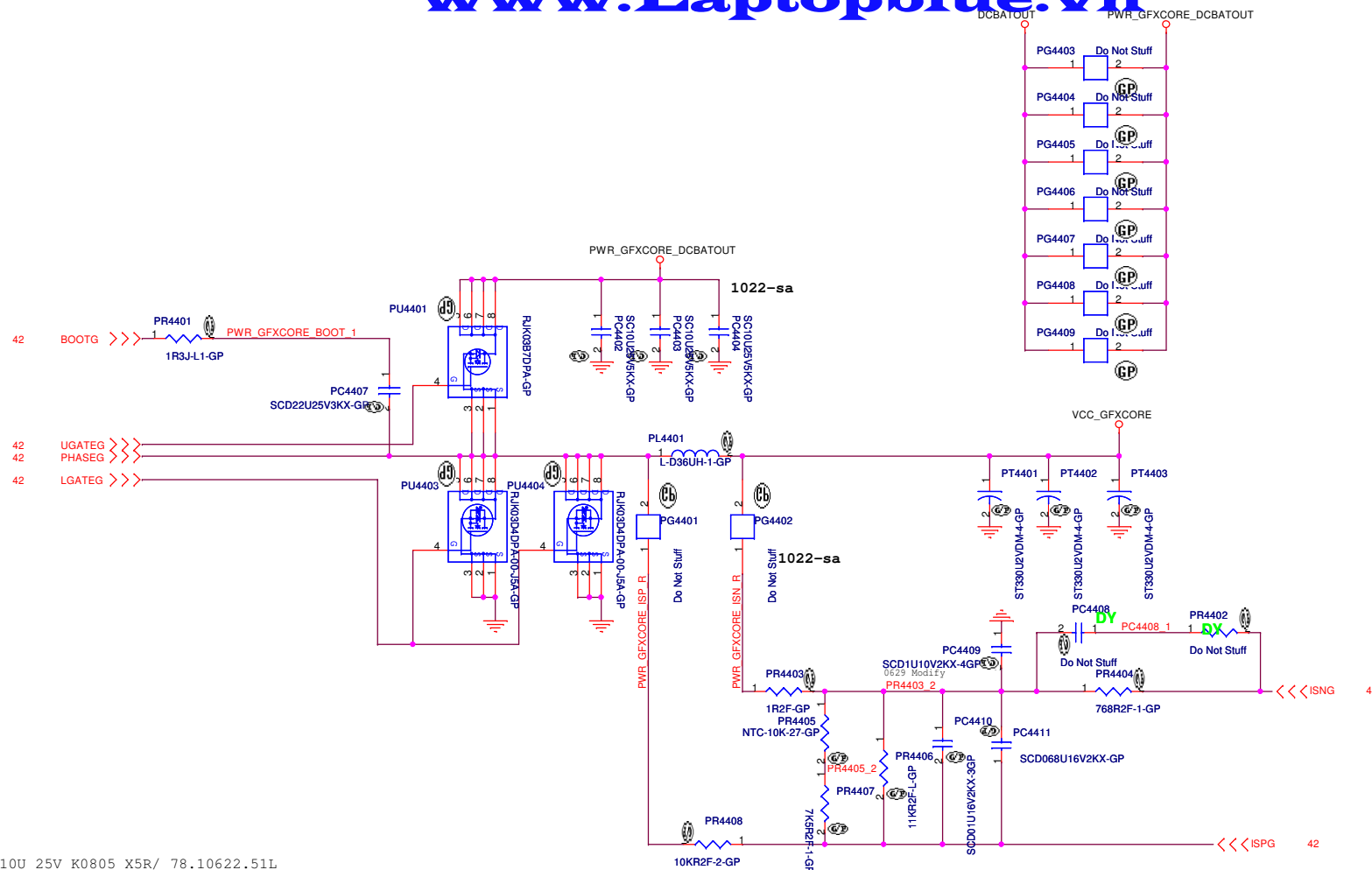
I/P cap: 10U 25V K0805 X5R/ 78.10622.51L
 Inductor: 0.36UH ETQP4LR36WFC Panasonic 1.1mohm/ 68.R3610.20A
 O/P cap: 330U 2V EEP5X0D331XE 6mOhm 3.4Arms Panasonic/79.33719.20L
 H/S: RJK03B9DPA/ POWERPAK-8/10.9mOhm/15.1mOhm@4.5Vgs/ 84.003B9.B37
 L/S: RJK03D4DPA/ POWERPAK-8/ 4.6mOhm/5.6mohm@4.5Vgs/ 84.00034.A37

DV15 HR Vos GIGA HDMI NoSurge

Wistron Corporation
 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
 Taipei Hsien 221, Taiwan, R.O.C.

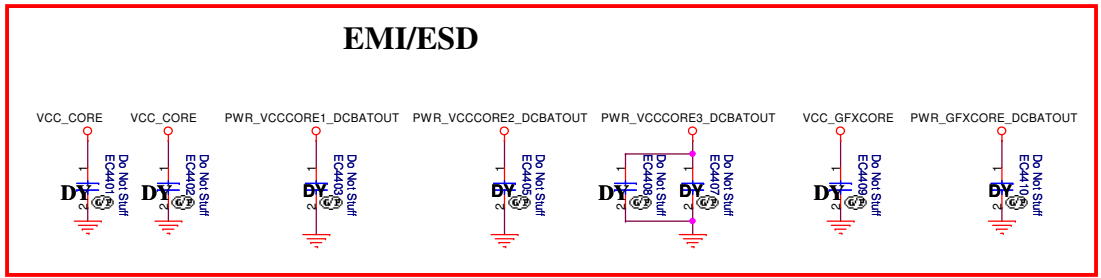
Title: **ISL95831 CPU CORE (2 of 3)**

Size: Custom	Document Number: Enrico/Caruso 15 HR	Rev: X01
Date: Thursday, June 02, 2011	Sheet: 43	of: 104



VCC_GFXCORE
I_{omax}=33A
OCP>50A

I/P cap: 10U 25V K0805 X5R/ 78.10622.51L
 Inductor: 0.36UH ETQP4LR36WFC Panasonic 1.1mohm/ 68.R3610.20A
 O/P cap: 330U 2V EEFSX0D331XE 6mOhm 3.4Arms Panasonic/79.33719.20L
 H/S: RJK03B7DPA NC WPAK 8P/7.7mOhm/10.7mOhm@4.5Vgs/84.003B7.037
 L/S: RJK03D4DPA/ POWERPAK-8/ 4.6mOhm/5.6mohm@4.5Vgs/ 84.00034.A37

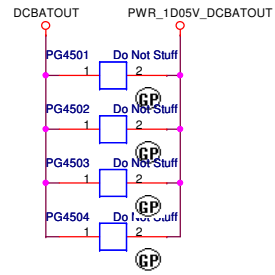


DV15 HR Vos GIGA HDMI NoSurge

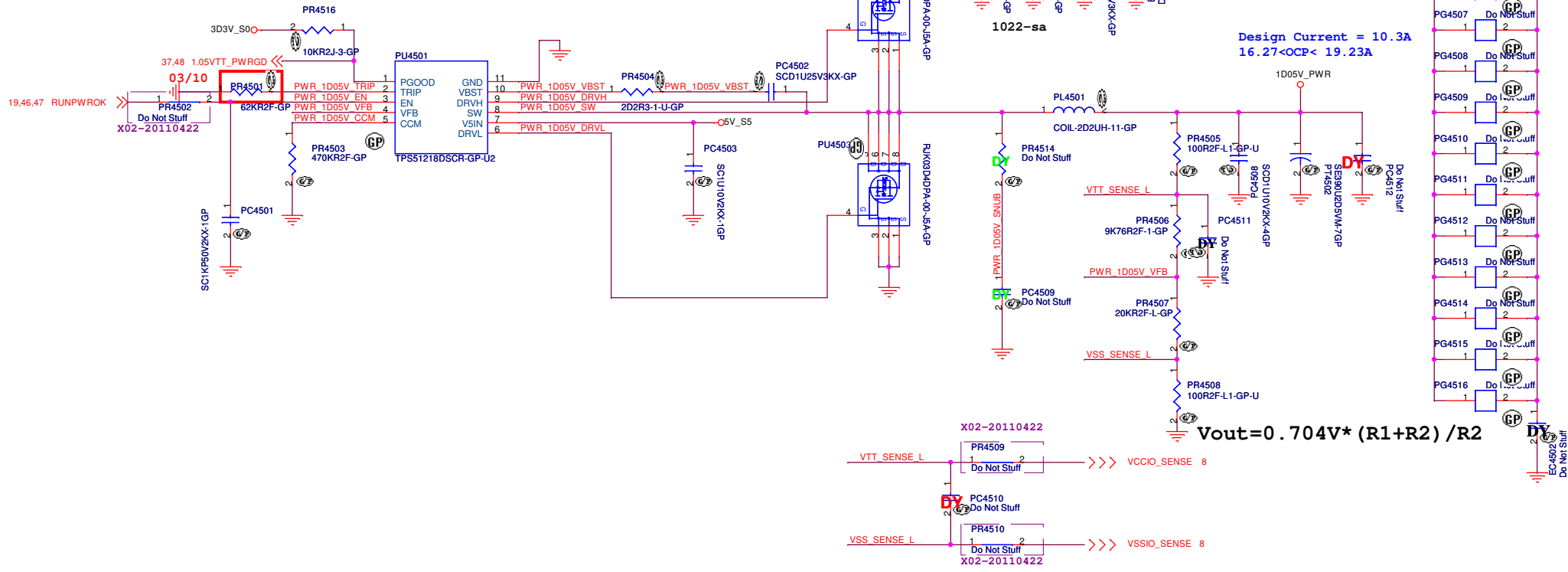
Wistron Corporation
 21F, 88, Sec. 1, Hsin Tai Wu Rd., Hsichih,
 Taipei Hsien 221, Taiwan, R.O.C.

Title: **ISL95831 CPU CORE(3/3)**

Size A3	Document Number	Rev
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TPS51218 for 1D05V



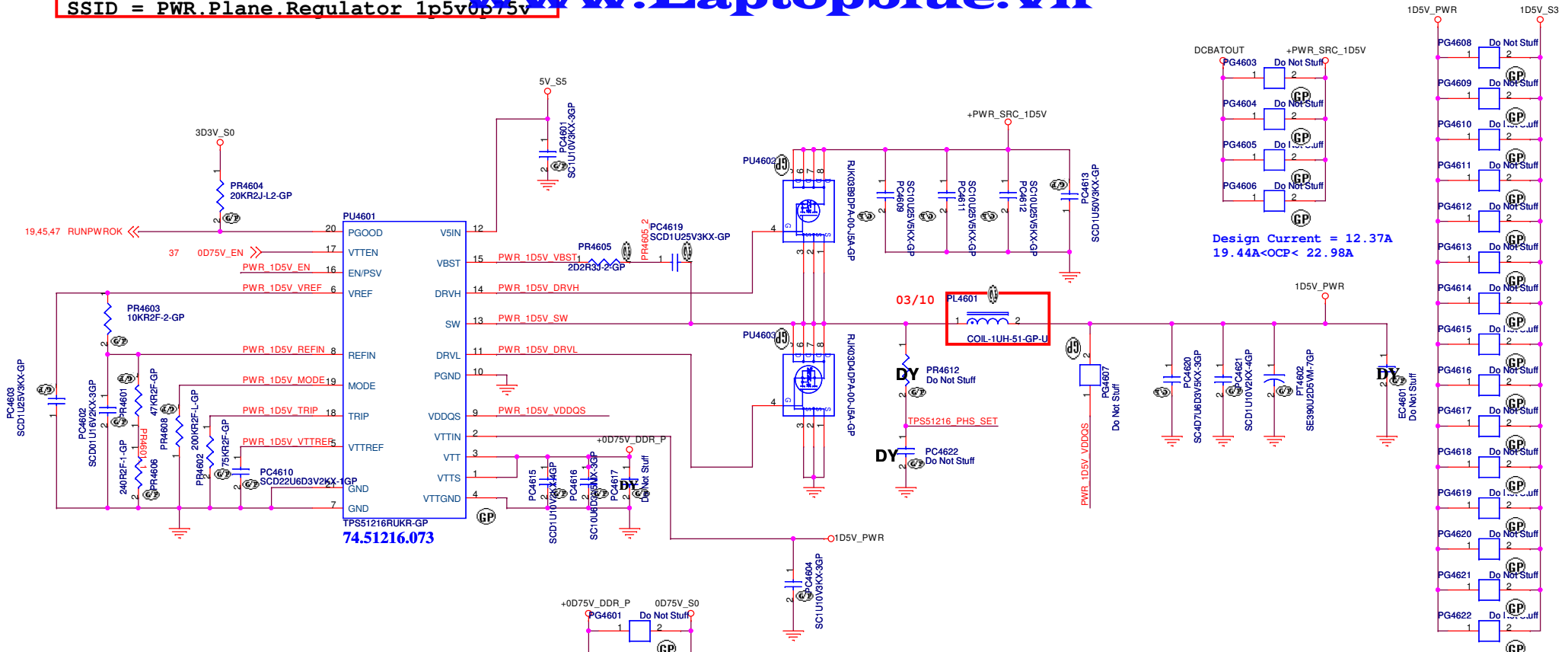
I/P cap: 10U 25V K0805 X5R/ 78.10622.51L
 Inductor: 2.20UH PCMC104T-2R2 Cynotec 7mohm Isat =27Arms 68.2R210.20C
 O/P cap: 390U 2.5V M 6.3*5.7/ 10mOhm 3.87Arms Matsuki/79.3971V.30L
 H/S: RJK03B9DPA/ POWERPAK-8/10.9mOhm/15.1mOhm@4.5Vgs/ 84.003B9.B37
 L/S: RJK03D4DPA/ POWERPAK-8/ 4.6mOhm/5.6mohm@4.5Vgs/ 84.00034.A37

DV15 HR Vos GIGA HDMI NoSurge

Wistron Corporation
 21F, 88, Sec. 1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.

Title: **TPS51218 +1.05V VTT**

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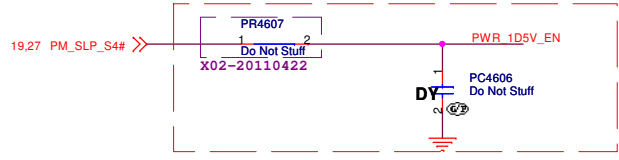
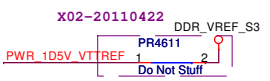


Design Current = 12.37A
19.44A < OCP < 22.98A

74.51216.073

State	S3	S5	VDDR	VTTREF	VTT
S0	Hi	Hi	On	On	On
S3	Lo	Hi	On	On	Off (Hi-Z)
S4/S5	Lo	Lo	Off	Off	Off

MODE	Frequency	Discharge Mode
PR4608	400kHz	Tracking Discharge
200k ohm	300kHz	
100k ohm	300kHz	Non-tracking Discharge
68k ohm	400kHz	



I/P cap: 10U 25V K0805 X5R/ 78.10622.51L
 Inductor: 1.0UH PCB104T-1R0M Cyntec 3mohm Isat =28Arms 68.1R01C.10Q
 O/P cap: 390U 2.5V M 6.3*5.7/ 10mOhm 3.87Arms Matsuki/79.3971V.30L
 H/S: RJK03B9DPA/ POWERPAK-8/10.9mOhm/15.1mOhm@4.5Vgs/ 84.003B9.B37
 L/S: RJK03D4DPA/ POWERPAK-8/ 4.6mOhm/5.6mohm@4.5Vgs/ 84.00034.A37

DV15 HR Vos GIGA HDMI NoSurge

Wistron Corporation
 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
 Taipei Hsien 221, Taiwan, R.O.C.

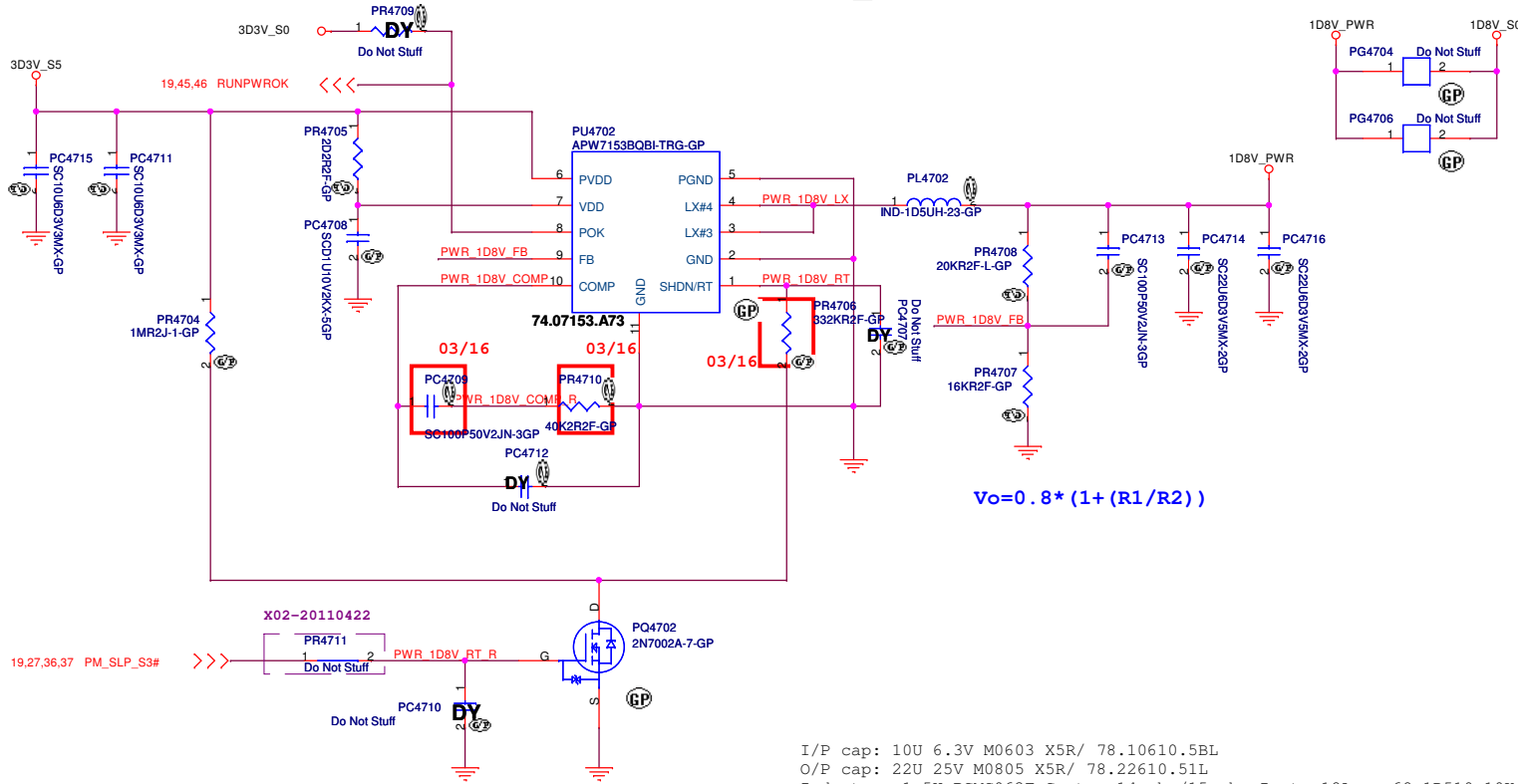
Title: **TPS51116 +1.5V SUS**

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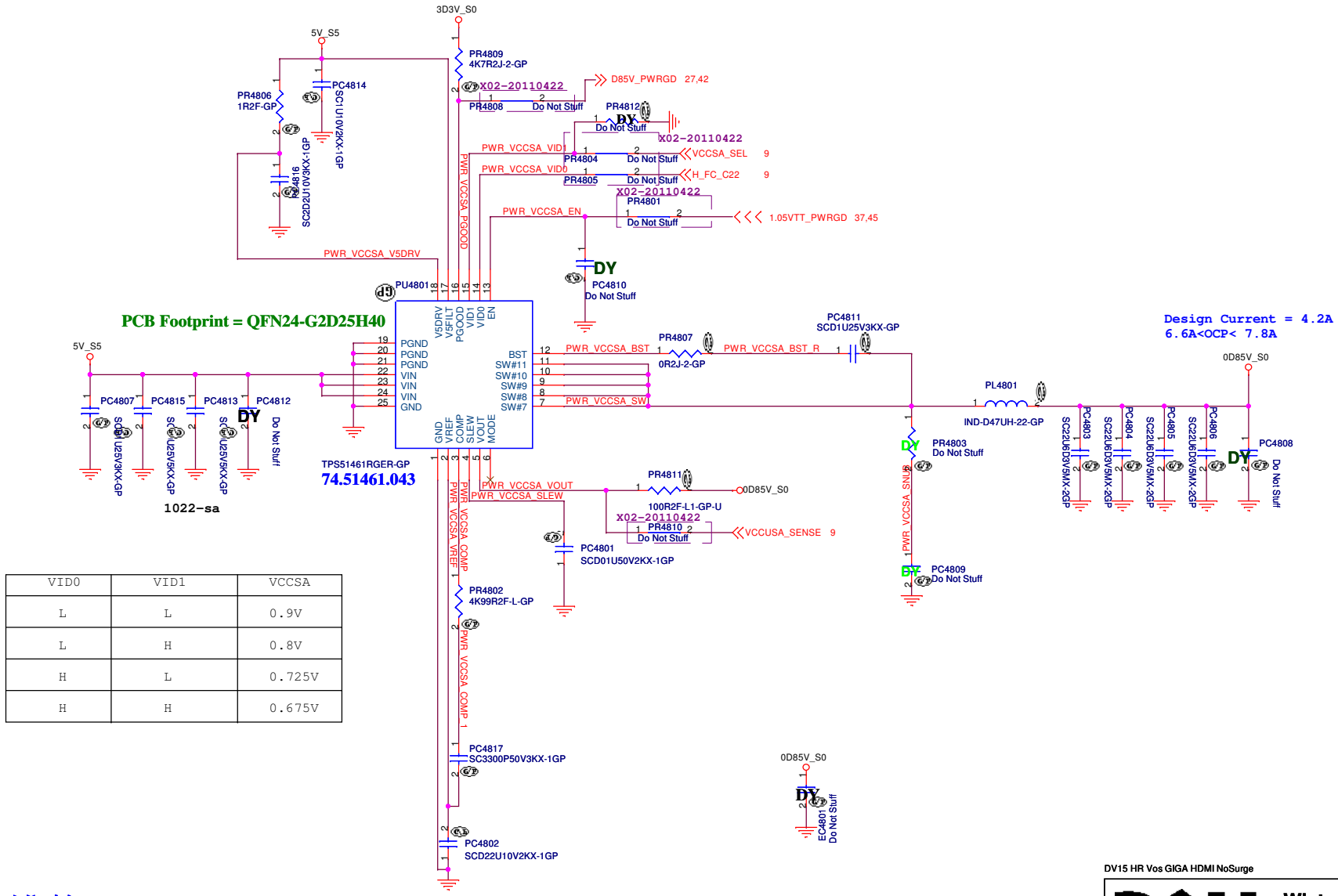
SSID = PWR.Plane.Regulator_1D8V_S0

+1.8V_RUN
Design current = 0.87A

APW7153B for 1D8V_S0



TPS51461 for VCCSA



起点主板维修网 www.qdzbwx.com

DV15 HR Vos GIGA HDMI NoSurge

Wistron Corporation
21F, 88, Sec. 1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.

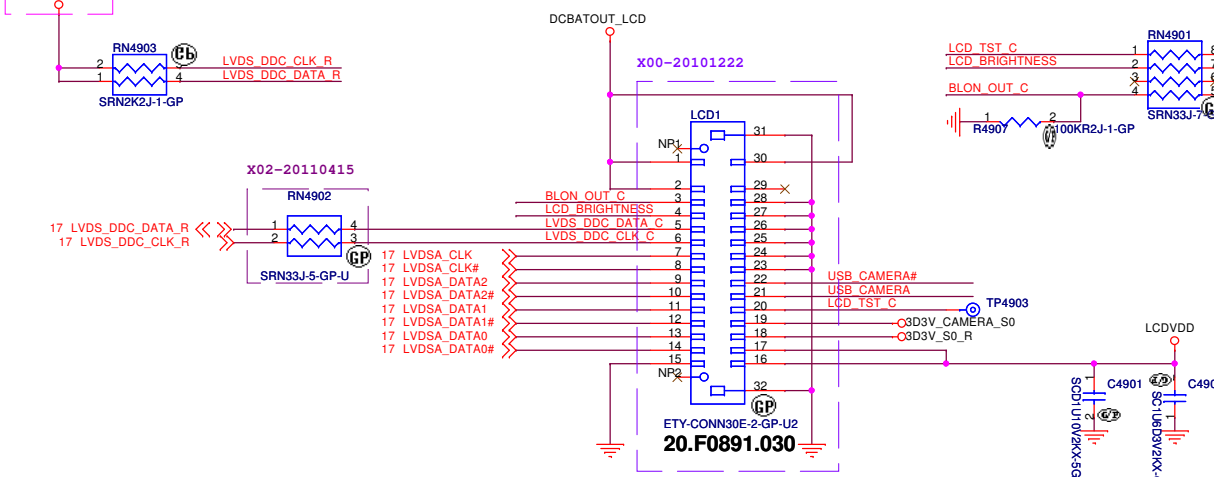
Title: **TPS51461 VCCSA**

Size A3	Document Number	Rev
	Enrico/Caruso 15 HR	X01

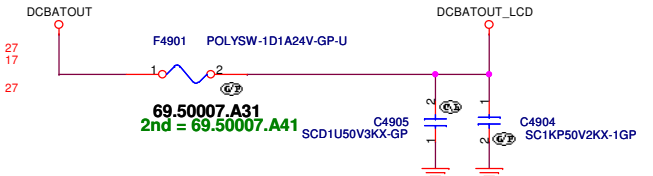
Date: Thursday, June 02, 2011 Sheet 48 of 104

X01-20110307

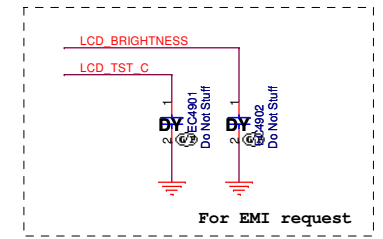
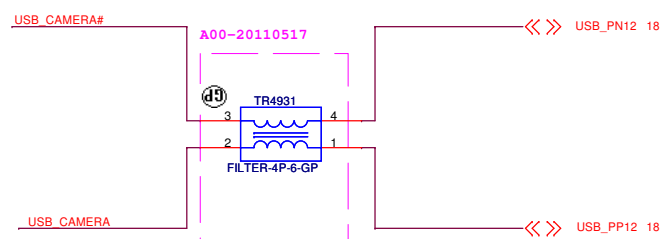
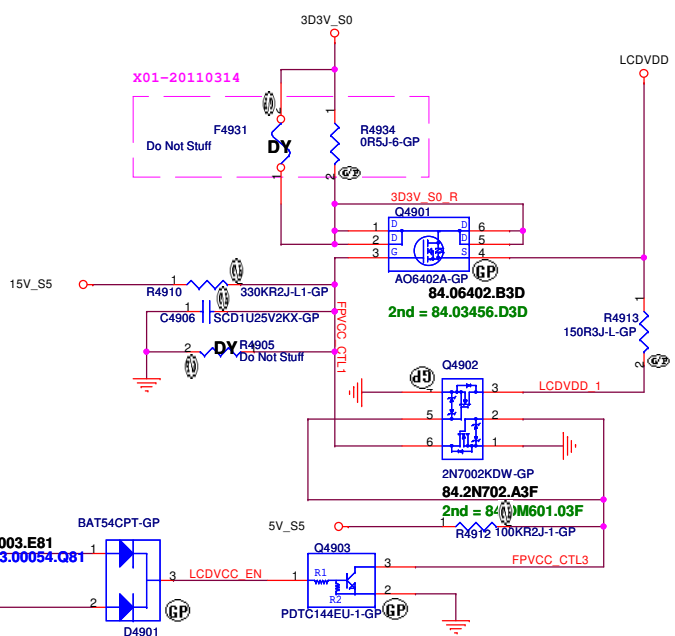
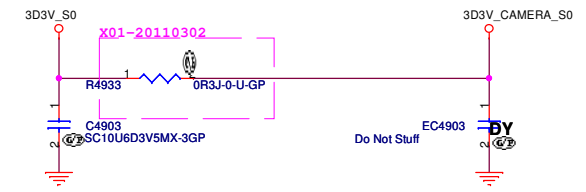
LVDS CONNECTOR



INVERTER POWER



Camera Power



DV15 HR Vos GIGA HDMI NoSurge

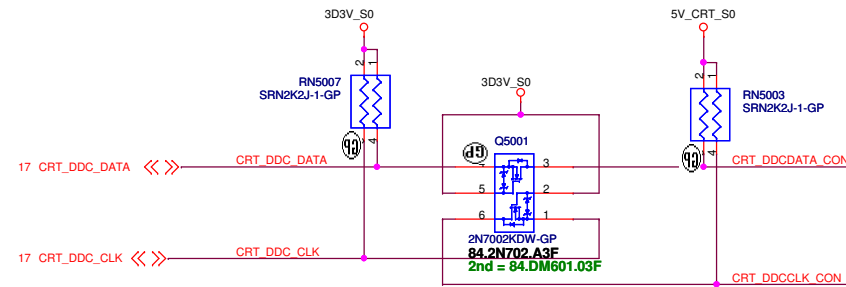
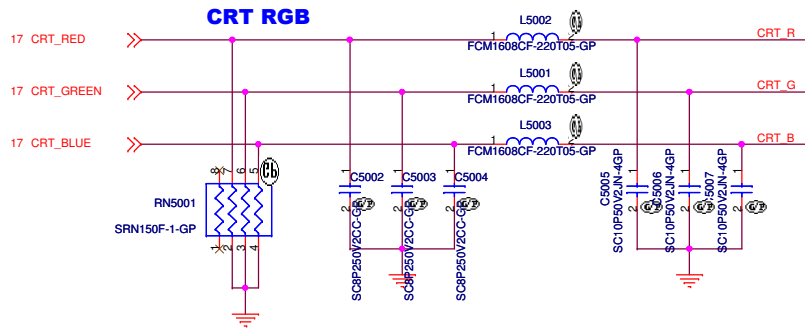
 Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.		
LCD Connector		
File	Document Number	Rev
Size A3	Enrico/Caruso 15 HR	X01
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SSID = VIDEO

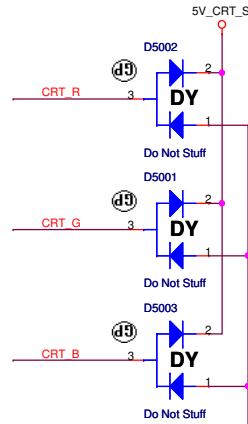
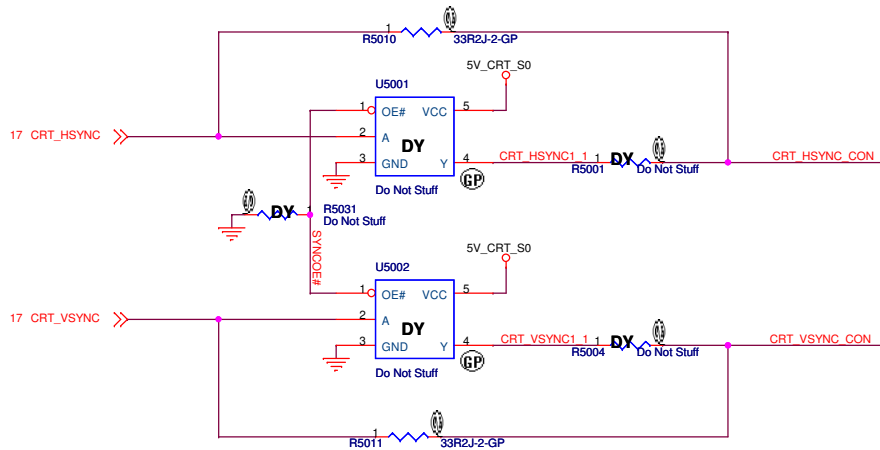
Layout Note:

*Pi-filter & 150 Ohm pull-down resistors should be as close as to CRT CONN.

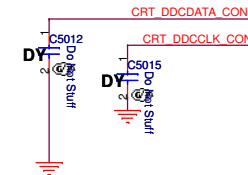
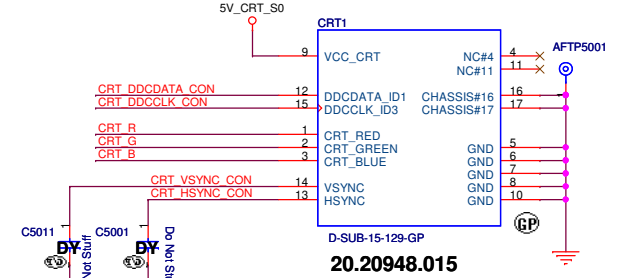
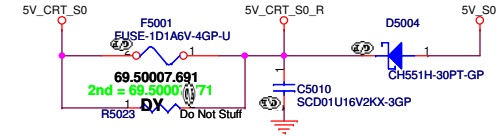
* RGB signal will hit 75 Ohm first, then pi-filter, finally CRT CONN.



Hsync & Vsync



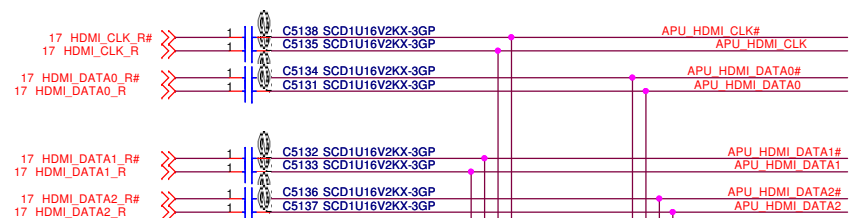
- AFTP5002 1 5V_CRT_S0
- AFTP5003 1 CRT_DDCDATA_CON
- AFTP5004 1 CRT_DDCCLK_CON
- AFTP5005 1 CRT_R
- AFTP5006 1 CRT_G
- AFTP5007 1 CRT_B
- AFTP5008 1 CRT_HSYNC_CON
- AFTP5009 1 CRT_VSYNC_CON



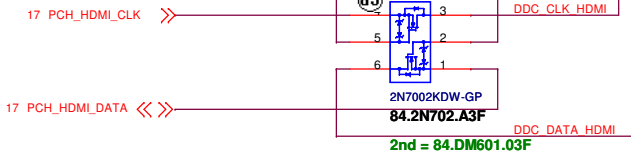
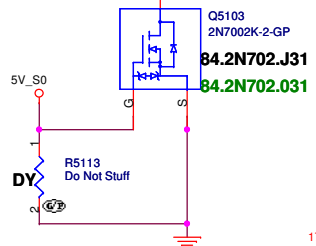
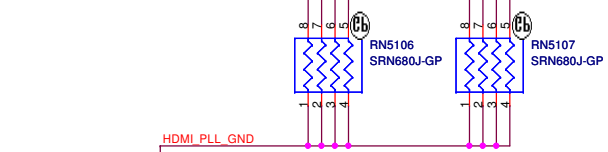
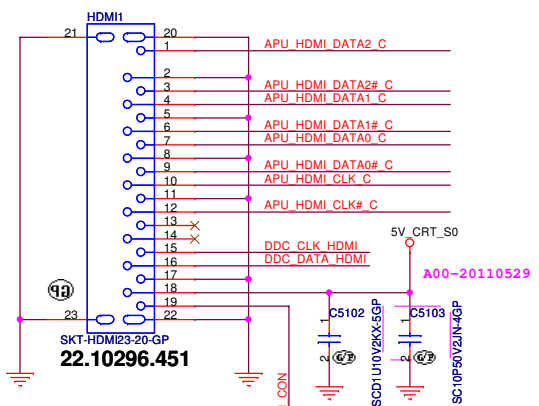
DV15 HR Vos GIGA HDMI NoSurge

DELL		Wistron Corporation	
		21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
CRT Connector			
Size	Document Number	Rev	
Custom	Enrico/Caruso 15 HR	X01	
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SSID = VIDEO



HDMI CONN



APU HDMI_DATA1	1	2	APU HDMI_DATA1_C	1	2	APU HDMI_CLK	1	2	APU HDMI_CLK_C
Do Not Stuff			R5146			Do Not Stuff			R5144
APU HDMI_DATA1#	1	2	APU HDMI_DATA1#_C	1	2	APU HDMI_CLK#	1	2	APU HDMI_CLK#_C
Do Not Stuff			R5147			Do Not Stuff			R5145
APU HDMI_DATA2	1	2	APU HDMI_DATA2_C	1	2	APU HDMI_DATA0	1	2	APU HDMI_DATA0_C
Do Not Stuff			R5148			Do Not Stuff			R5143
APU HDMI_DATA2#	1	2	APU HDMI_DATA2#_C	1	2	APU HDMI_DATA0#	1	2	APU HDMI_DATA0#_C
Do Not Stuff			R5142			Do Not Stuff			R5141

A00-20110530

84.03904.L06
2nd = 84.03904.P11
3rd = 84.03904.T11

DV15 HR Vos GIGA HDMI NoSurge

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21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.

Title: **HDMI Level Shifter/Connector**

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	Wistron Corporation 21F, 88, Sec. 1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.
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Title		
Reserved		
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(Blanking)

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		Wistron Corporation 21F, 88, Sec. 1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.
Title		
LVDS Switch		
Size	Document Number	Rev
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(Blanking)

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Title		
Reserved		
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SSID = User.Interface

(Blanking)

DV15 HR Vos GIGA HDMI NoSurge

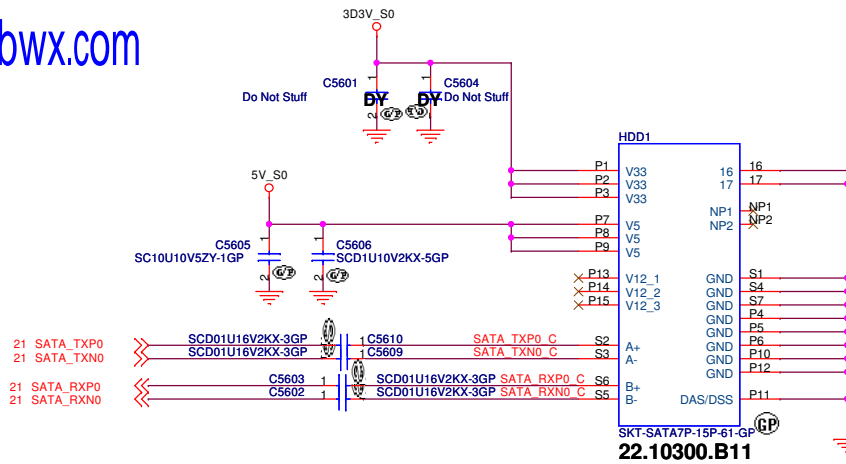


Title		
ITP/Fan Connector		
Size	Document Number	Rev
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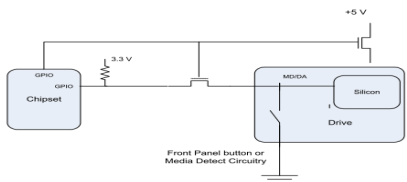
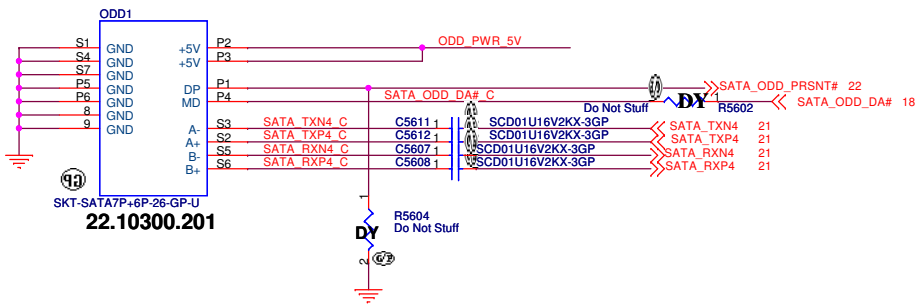
SSID = SATA

SATA HDD Connector

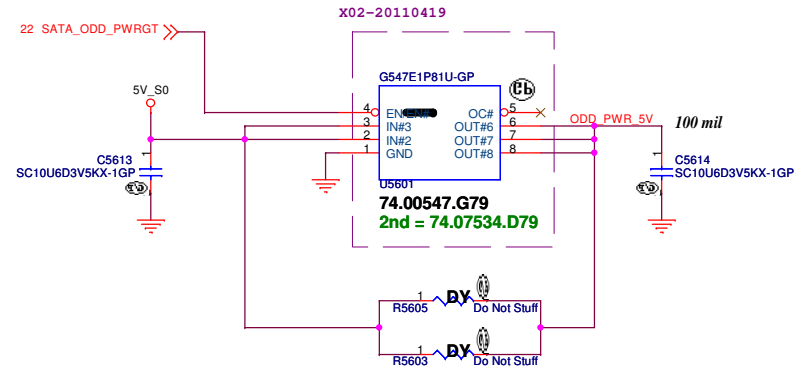
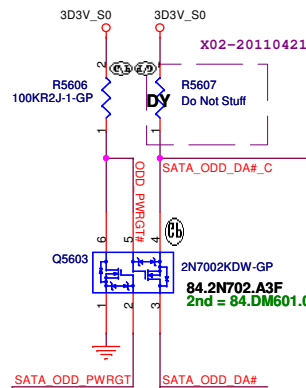
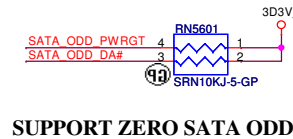
起点主板维修网 www.qdzbwx.com



ODD Connector



When the drive is powered on, the FET to the MD/DA pin drive is OFF.
When the drive is powered off, the FET to the MD/DA pin is ON



DV15 HR Vos GIGA HDMI NoSurge



File HDD/ODD			
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SSID = ESATA

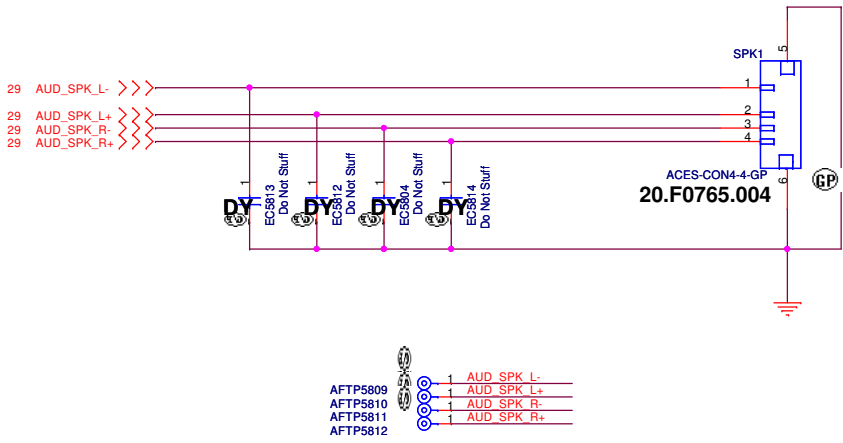
DV15 HR Vos GIGA HDMI NoSurge



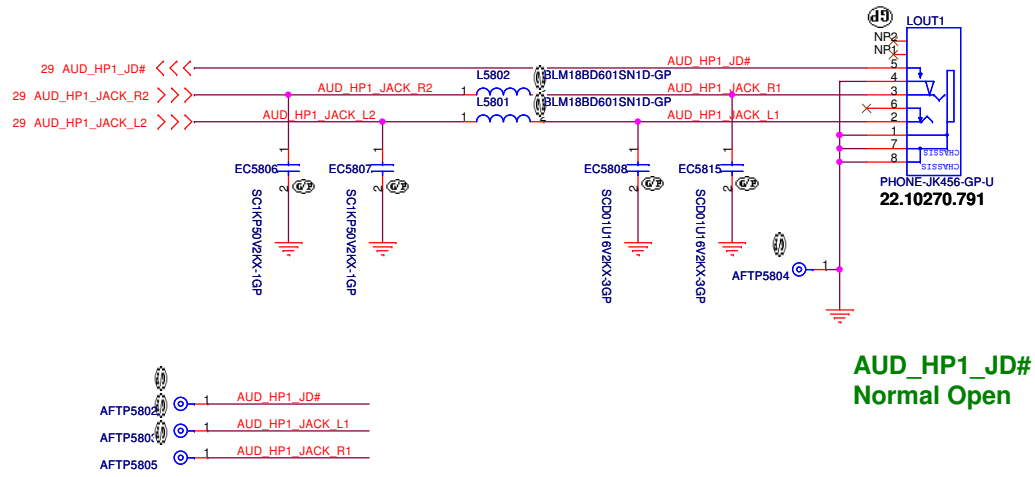
Title			ESATA		
Size	Document Number	Rev			
A3	Enrico/Caruso 15 HR	X01			
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SSID = AUDIO

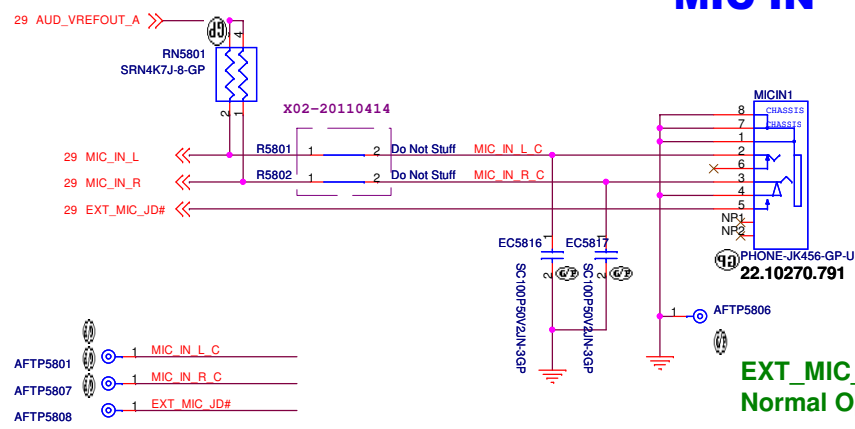
Speaker Connector



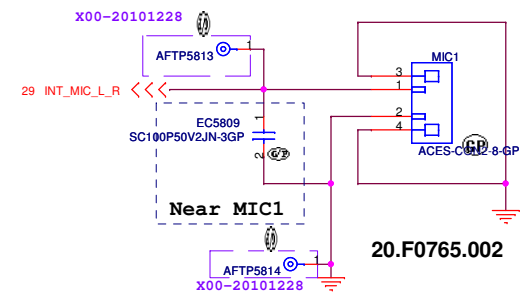
LINE1 OUT



MIC IN



Internal Microphone



DV15 HR Vos GIGA HDMI NoSurge

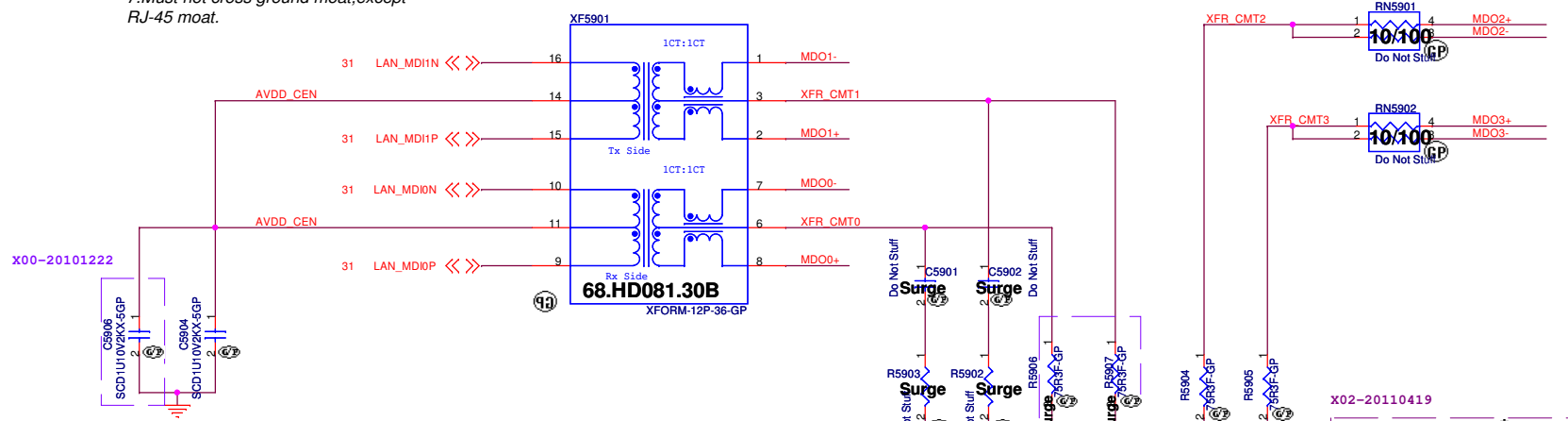
DELL Wistron Corporation
 21F, 88, Sec. 1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.

Title: **SPEAKER CONN**

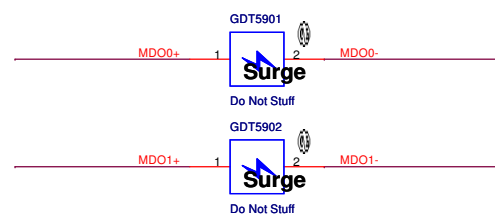
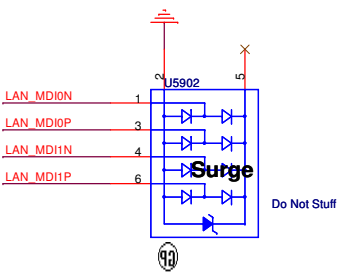
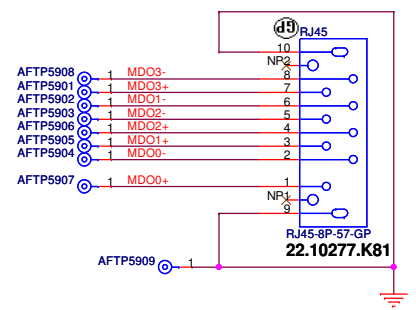
Size: A3	Document Number: Enrico/Caruso 15 HR	Rev: X01
Date: Thursday, June 02, 2011	Sheet: 58 of 104	

- 1.route on bottom as differential pairs.
- 2.Tx+/Tx- are pairs. Rx+/Rx- are pairs.
- 3.No vias, No 90 degree bends.
- 4.pairs must be equal lengths.
- 5.6mil trace width, 12mil separation.
- 6.36mil between pairs and any other trace.
- 7.Must not cross ground moat,except RJ-45 moat.

10/100M Lan Transformer

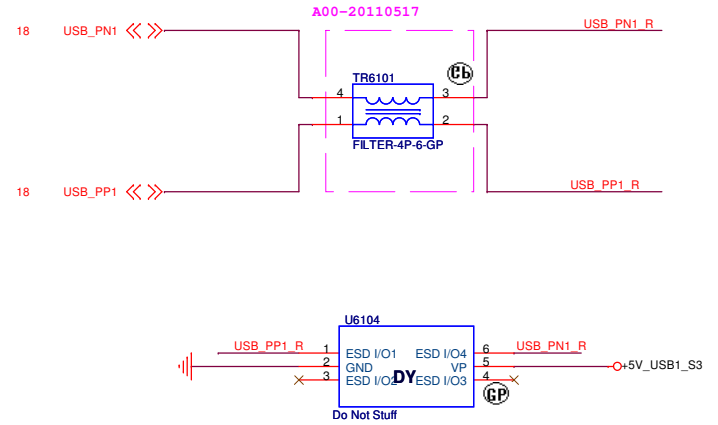
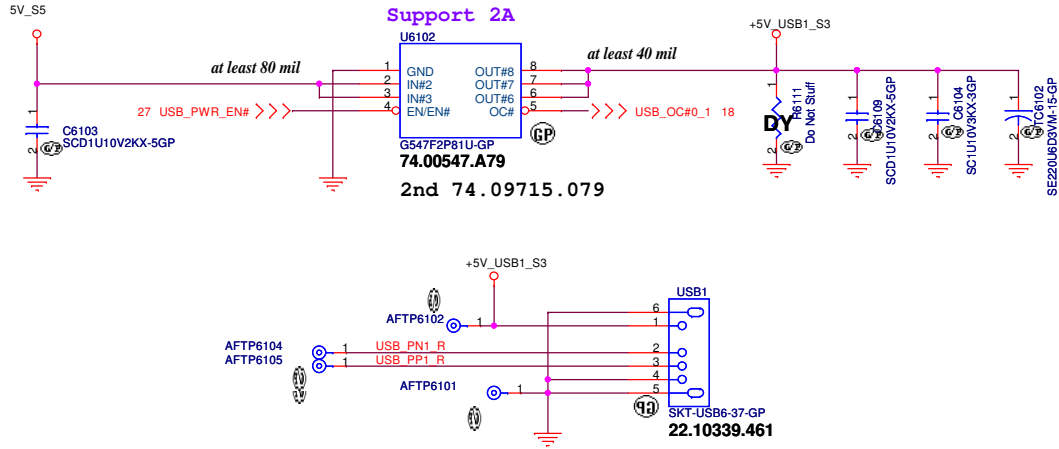


RJ45 Connector

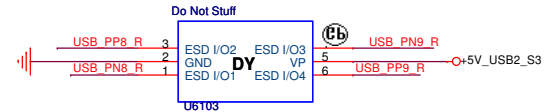
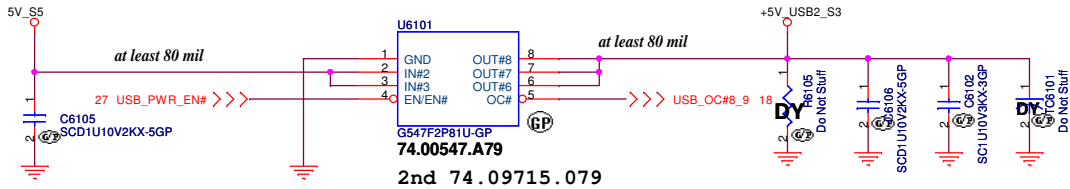


SSID = USB

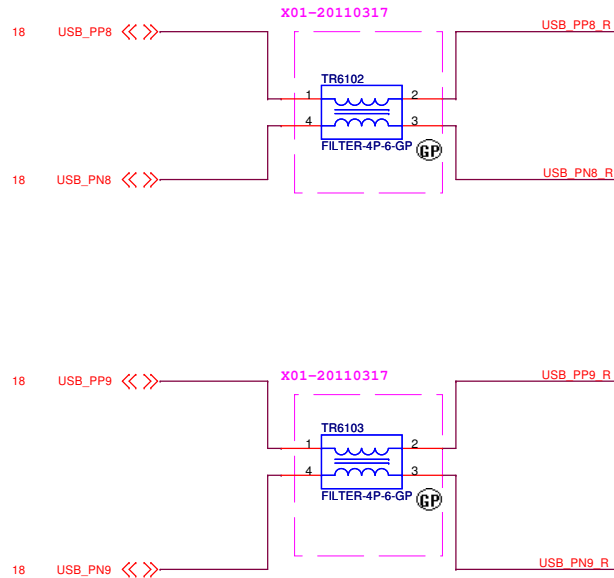
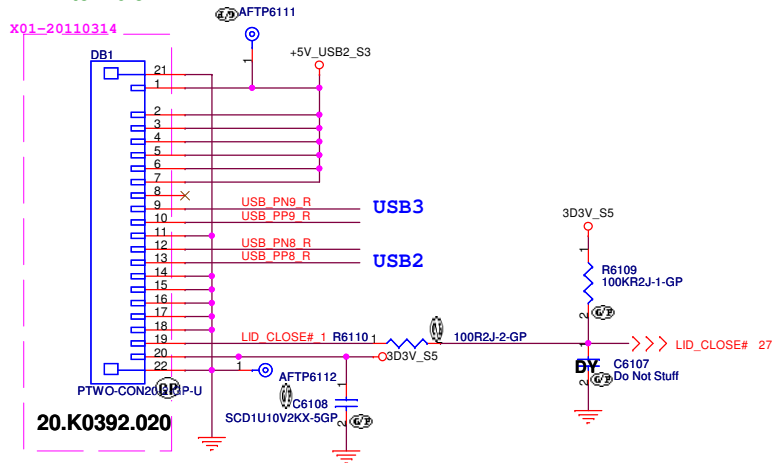
Left USB Power x1



Right USB Power x2



Pitch=0.5mm



- AFTP6107 1 USB_PN8_R
- AFTP6108 1 USB_PP8_R
- AFTP6109 1 USB_PN9_R
- AFTP6110 1 USB_PP9_R
- AFTP6106 1 3D3V_S5
- AFTP6103 1 LID_CLOSE# 1

DV15 HR Vos GIGA HDMI NoSurge



Title			USB Power SW		
Size	Document Number		Rev		
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Title		
Reserved		
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SSID = User.Interface

DV15 HR Vos GIGA HDMI NoSurge



Title		
Bluetooth		
Size	Document Number	Rev
A3	Enrico/Caruso 15 HR	X01
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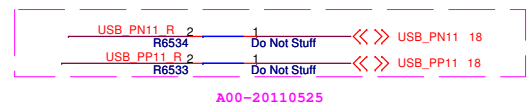
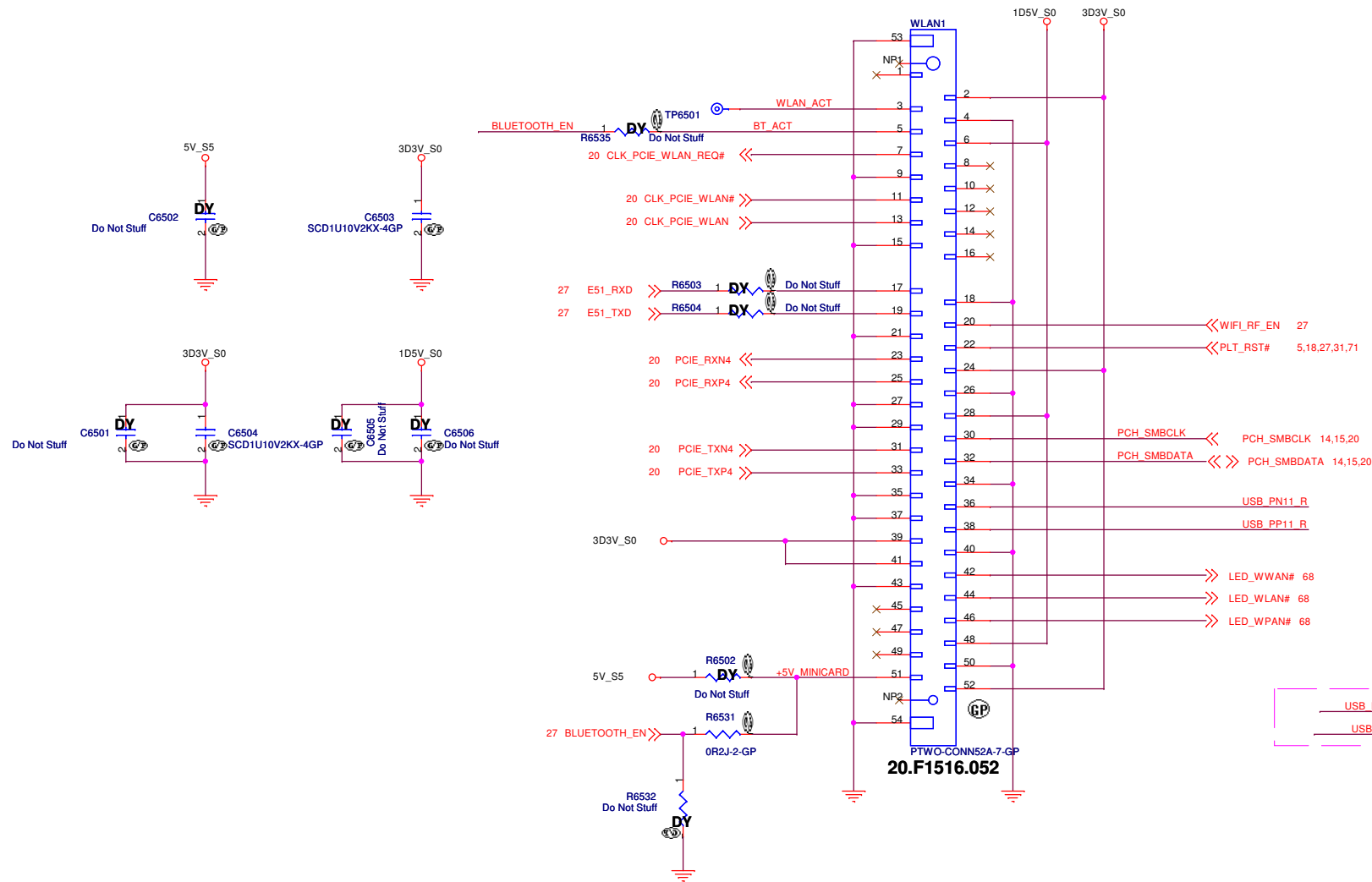
DV15 HR Vos GIGA HDMI NoSurge



Title		
RESERVED		
Size	Document Number	Rev
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SSID = Wireless


Mini Card Connector(802.11b/g/n)



A00-20110525

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DV15 HR Vos GIGA HDMI NoSurge

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Title		
Reserved		
Size A3	Document Number Enrico/Caruso 15 HR	Rev X01
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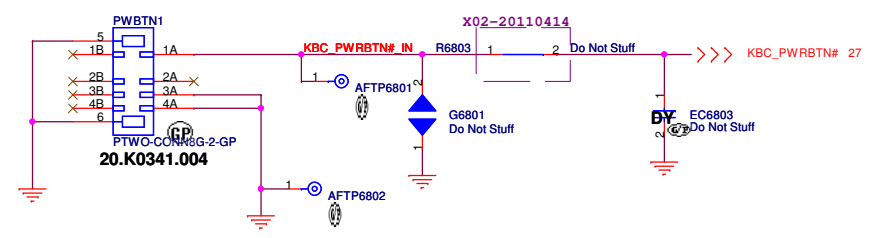
DV15 HR Vos GIGA HDMI NoSurge



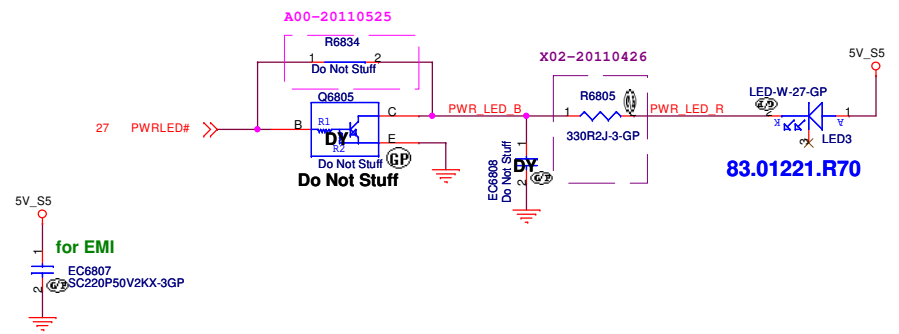
Title		
Reserved		
Size A3	Document Number Enrico/Caruso 15 HR	Rev X01
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SSID = User.Interface

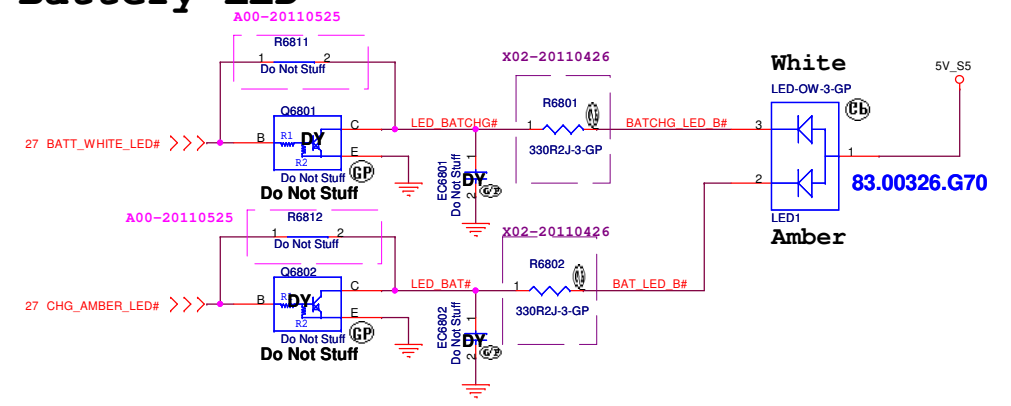
Power BTN Connector



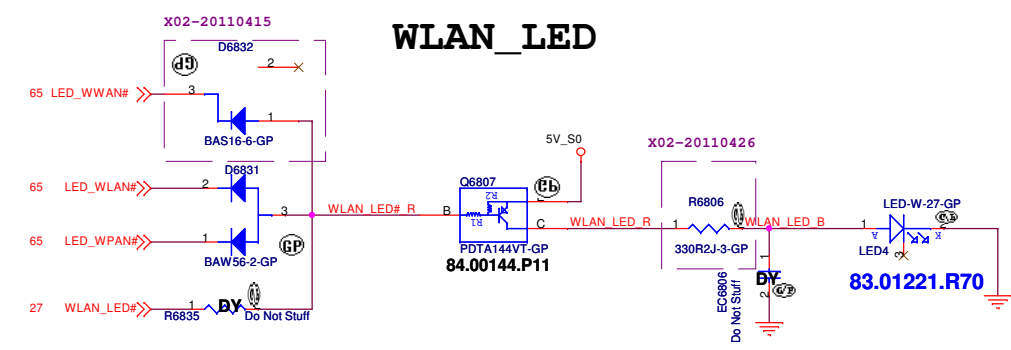
Power LED



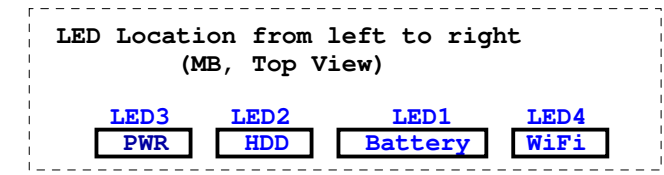
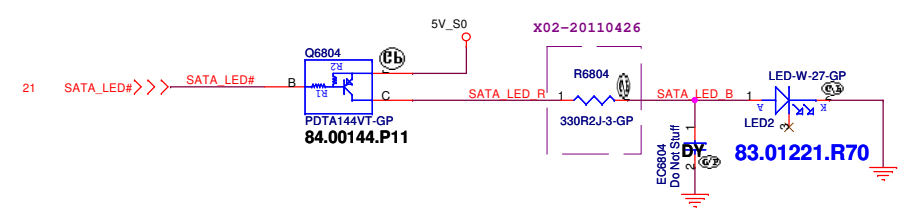
Battery LED



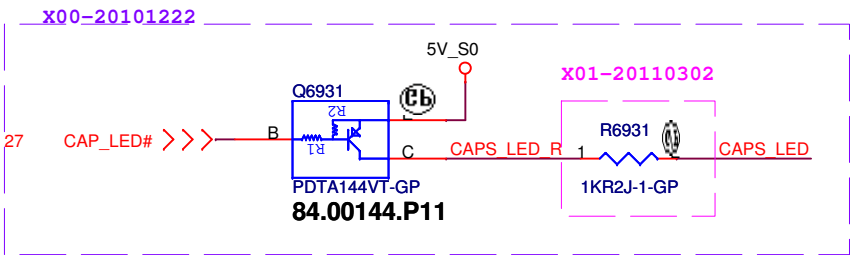
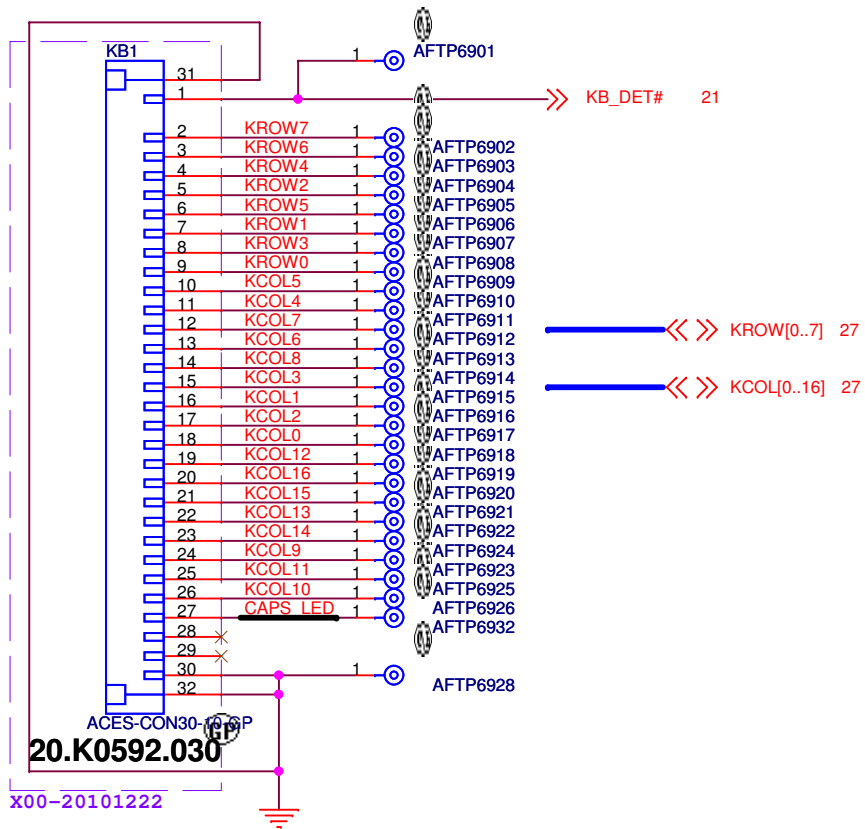
WLAN_LED



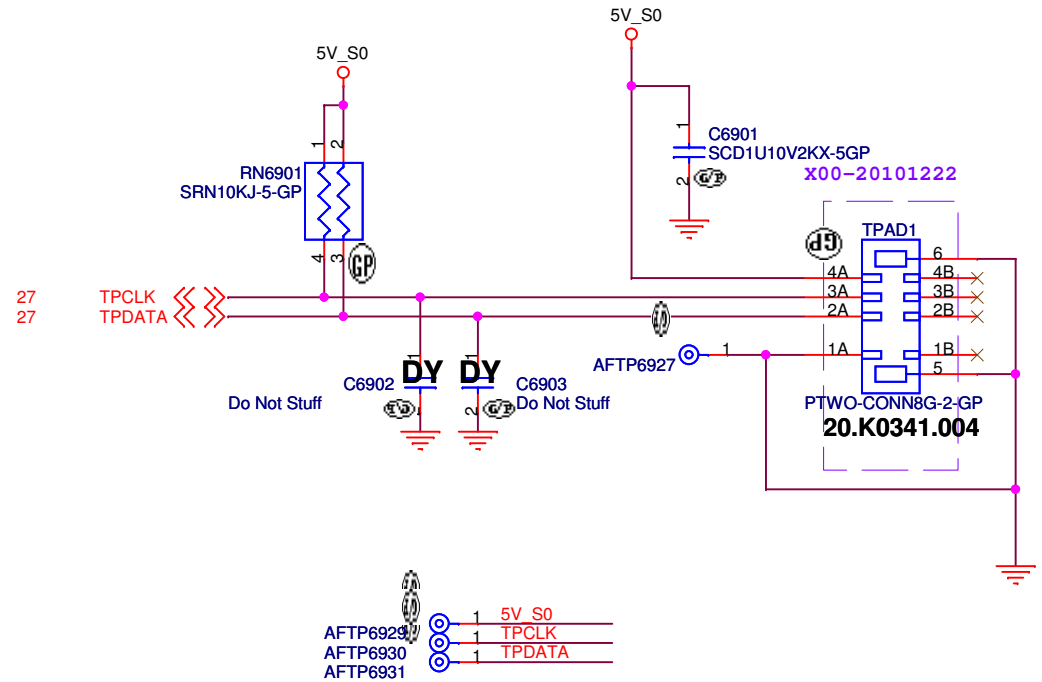
HDD LED



Internal KeyBoard Connector



TouchPad Connector



DV15 HR Vos GIGA HDMI NoSurge

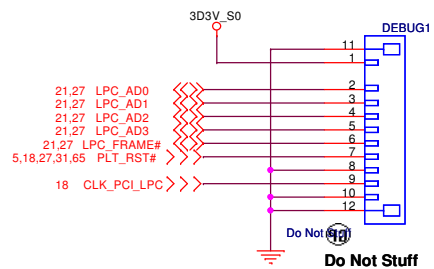


Title		
Key Board/Touch Pad		
Size	Document Number	Rev
A4		X01
Enrico/Caruso 15 HR		
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起点主板维修网 www.qdzbwx.com

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		Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.
Title		
Hall Sensor		
Size A3	Document Number Enrico/Caruso 15 HR	Rev X01
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		Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.
Title: Dubug connector		
Size: A3	Document Number: Enrico/Caruso 15 HR	Rev: X01
Date: Thursday, June 02, 2011	Sheet 71 of	104


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		Wistron Corporation 21F, 88, Sec. 1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.
Title		
Reserved		
Size	Document Number	Rev
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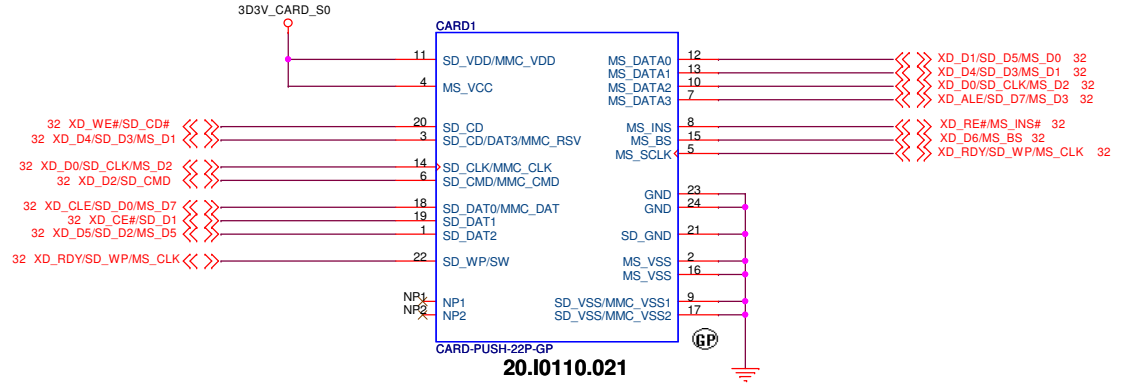
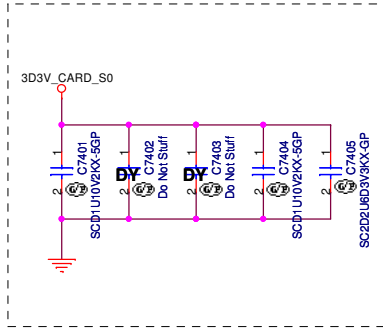
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DV15 HR Vos GIGA HDMI NoSurge

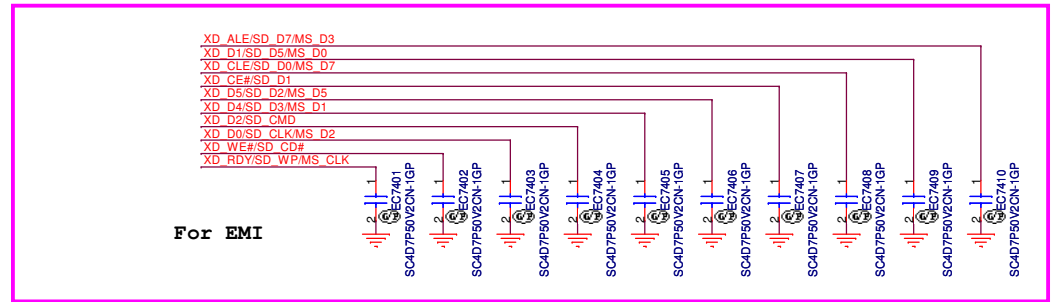
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Title		
Reserved		
Size	Document Number	Rev
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SSID = SDIO

SD/MMC/MS Card Reader



X01-20110315



SSID = ExpressCard


起点主板维修网 www.qdzbwx.com

DV15 HR Vos GIGA HDMI NoSurge

		Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title			
Express Card			
Size	Document Number	Rev	
A3	Enrico/Caruso 15 HR	X01	
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DV15 HR Vos GIGA HDMI NoSurge

		Wistron Corporation 21F, 88, Sec. 1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.
Title		
Reserved		
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DV15 HR Vos GIGA HDMI NoSurge

		Wistron Corporation 21F, 88, Sec. 1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.
Title		
Reserved		
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DV15 HR Vos GIGA HDMI NoSurge



Title		
Reserved		
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SSID = User.Interface

DV15 HR Vos GIGA HDMI NoSurge

			Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.		
Title					
Free Fall Sensor					
Size	Document Number				Rev
A3	Enrico/Caruso 15 HR				X01
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DV15 HR Vos GIGA HDMI NoSurge

		Wistron Corporation 21F, 88, Sec. 1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.
Title		
Reserved		
Size	Document Number	Rev
A3	Enrico/Caruso 15 HR	X01
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DV15 HR Vos GIGA HDMI NoSurge

			Wistron Corporation 21F, 88, Sec. 1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.
Title			Reserved
Size A3	Document Number Enrico/Caruso 15 HR	Rev X01	
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DV15 HR Vos GIGA HDMI NoSurge



Title		
IO Board Connector		
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DV15 HR Vos GIGA HDMI NoSurge

		Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title			
GPU PCIE/STRAPPING(1/5)			
Size	Document Number	Rev	
A3	Enrico/Caruso 15 HR	X01	
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DV15 HR Vos GIGA HDMI NoSurge

			Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsiehshih, Taipei Hsien 221, Taiwan, R.O.C.
Title			
GPU Memory(2/5)			
Size	Document Number	Rev	
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DV15 HR Vos GIGA HDMI NoSurge

			Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.		
Title					
GPU-VRAM1,2 (1/4)					
Size	Document Number				Rev
Custom	Enrico/Caruso 15 HR				X01
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DV15 HR Vos GIGA HDMI NoSurge

			Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.		
Title					
GPU-VRAM3,4 (2/4)					
Size	Document Number				Rev
Custom	Enrico/Caruso 15 HR				X01
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DV15 HR Vos GIGA HDMI NoSurge

		Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title			
GPU-VRAM5,6 (3/4)			
Size	Document Number	Rev	
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DV15 HR Vos GIGA HDMI NoSurge

		Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title			
GPU-VRAM7,8 (4/4)			
Size	Document Number	Rev	
A3	Enrico/Caruso 15 HR	X01	
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DV15 HR Vos GIGA HDMI NoSurge

			Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.		
Title					
RT8208B +VGA CORE					
Size	Document Number				Rev
A3	Enrico/Caruso 15 HR				X01
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DV15 HR Vos GIGA HDMI NoSurge

		Wistron Corporation 21F, 88, Sec. 1, Hsin Tsu Wu Rd., Hsinchu, Taippei Hsien 221, Taiwan, R.O.C.
Title DISCRETE VGA POWER		
Size A2	Document Number Enrico/Caruso 15 HR	Rev X01
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		Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.
Title		
LVDS Switch		
Size	Document Number	Rev
A3	Enrico/Caruso 15 HR	X01
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DV15 HR Vos GIGA HDMI NoSurge

		Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title			
CRT Switch			
Size	Document Number		Rev
A3	Enrico/Caruso 15 HR		X01
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SSID = SDIO

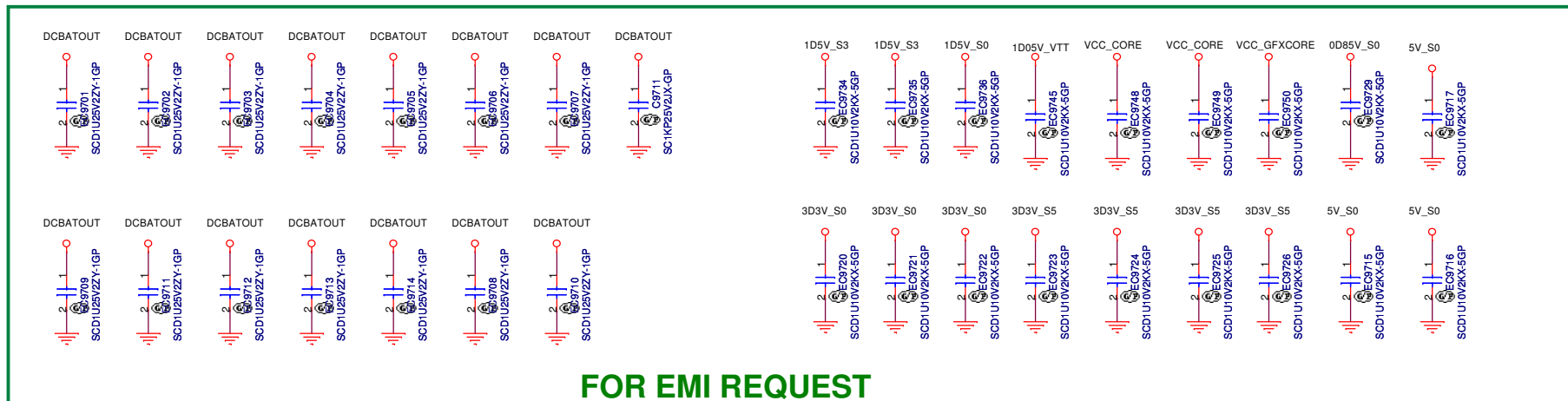
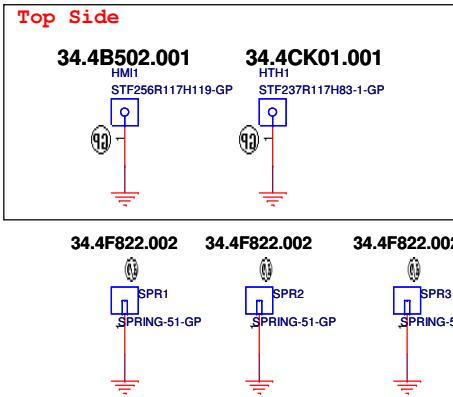
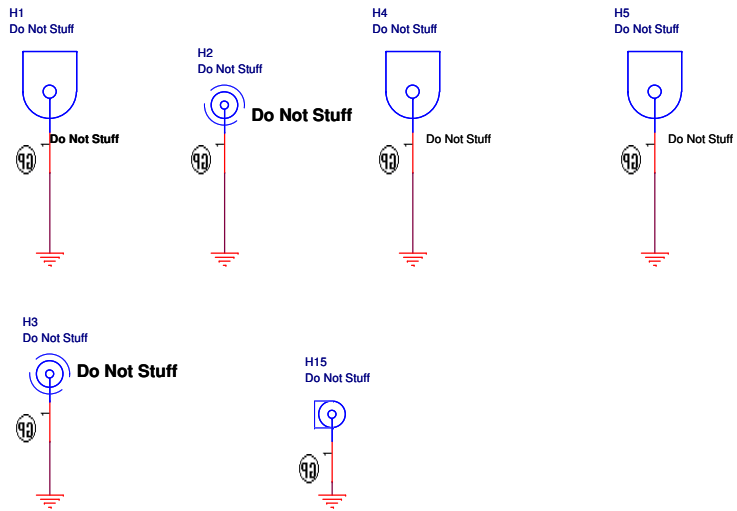
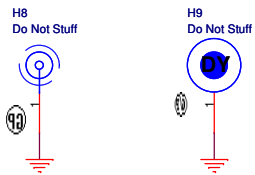
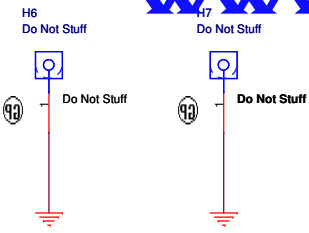
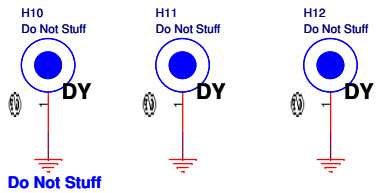
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DV15 HR Vos GIGA HDMI NoSurge



Title		
TOUCH PANEL		
Size A3	Document Number Enrico/Caruso 15 HR	Rev X01
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SSID = Mechanical



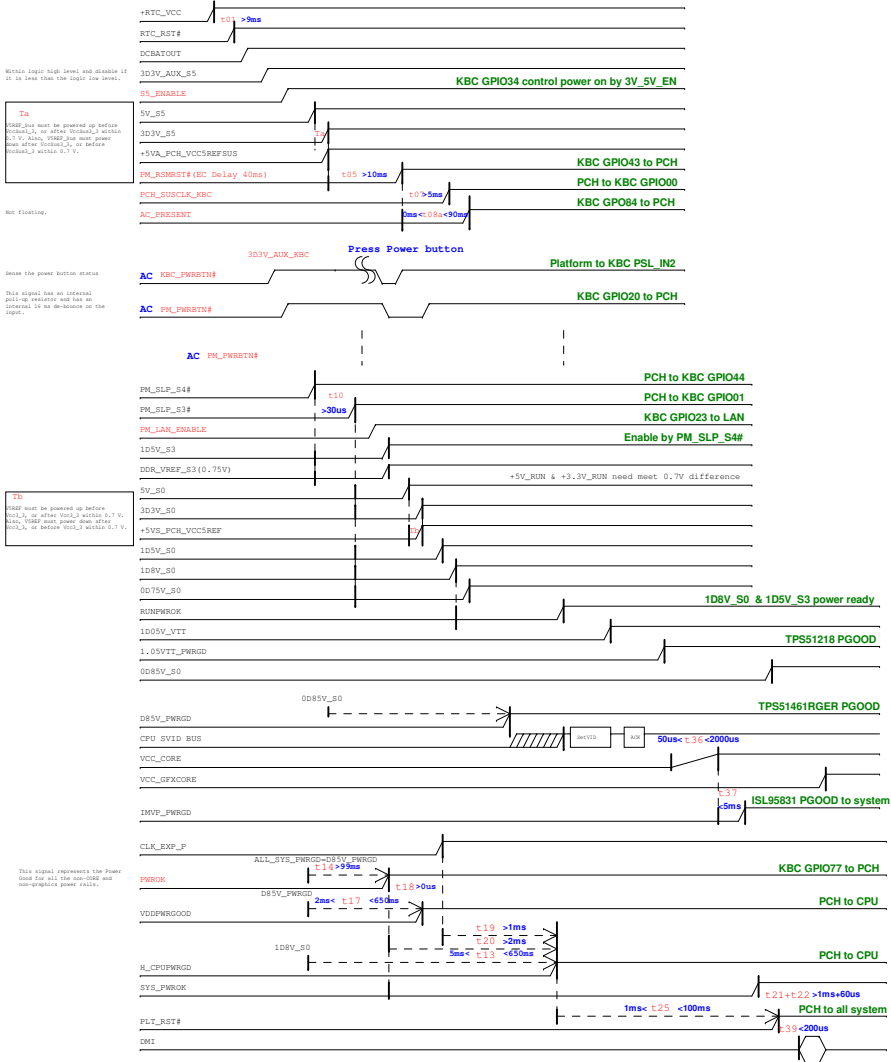
FOR EMI REQUEST

DV15 HR Vos GIGA HDMI NoSurge



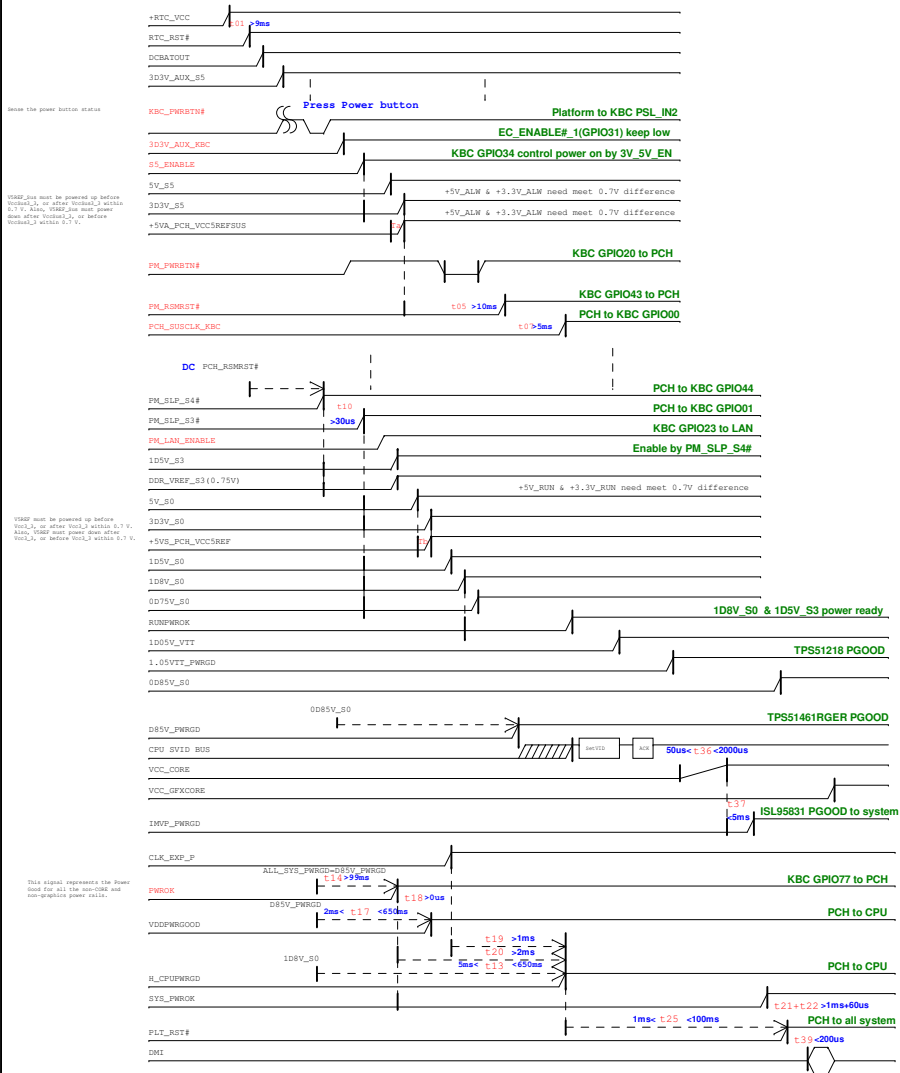
(AC mode)

red word: KBC GPIO

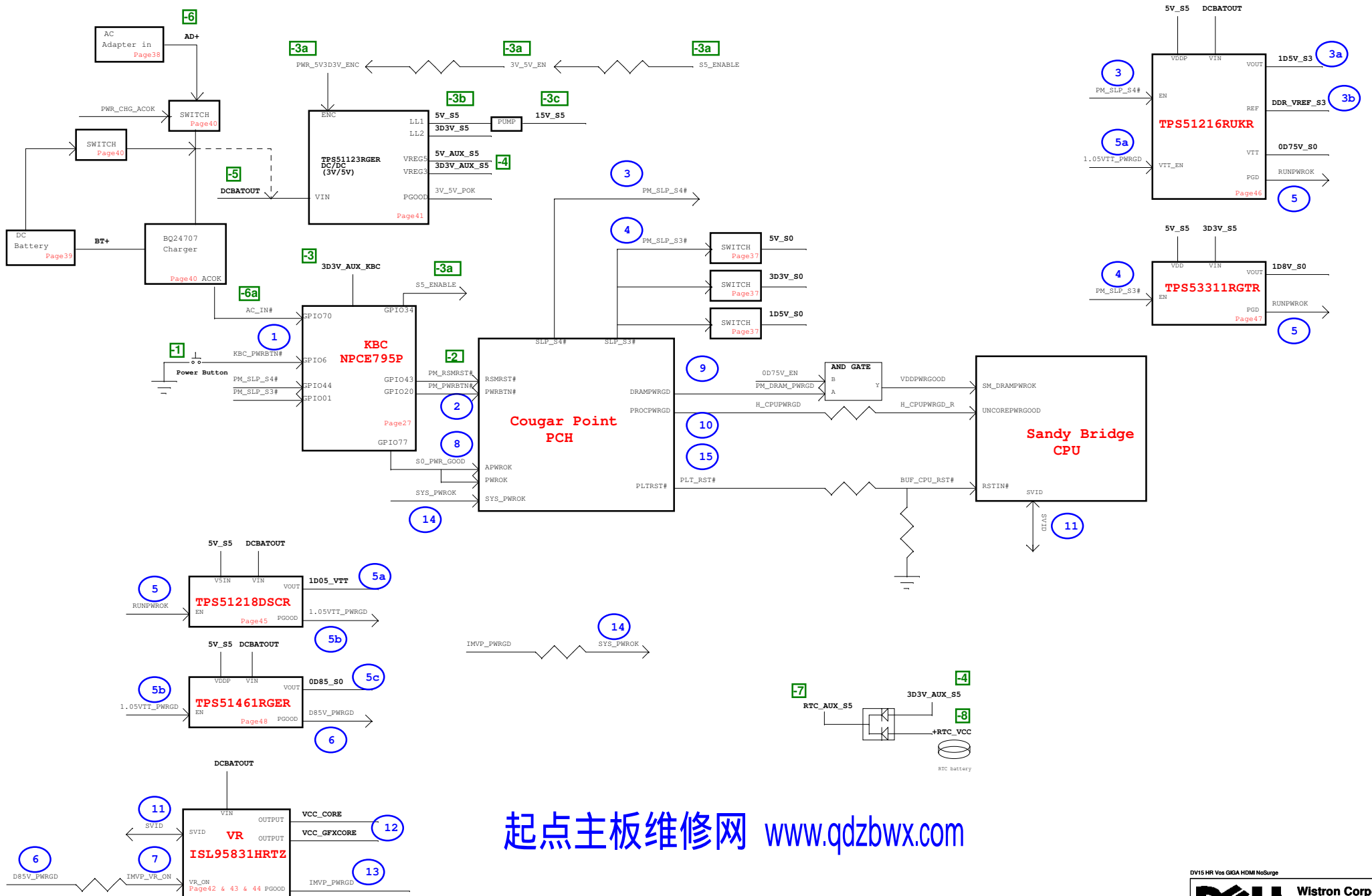


(DC mode)

red word: KBC GPIO

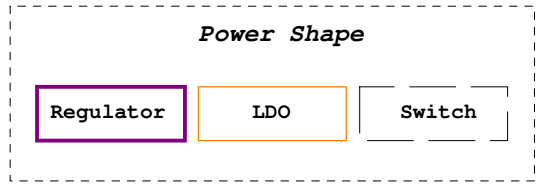
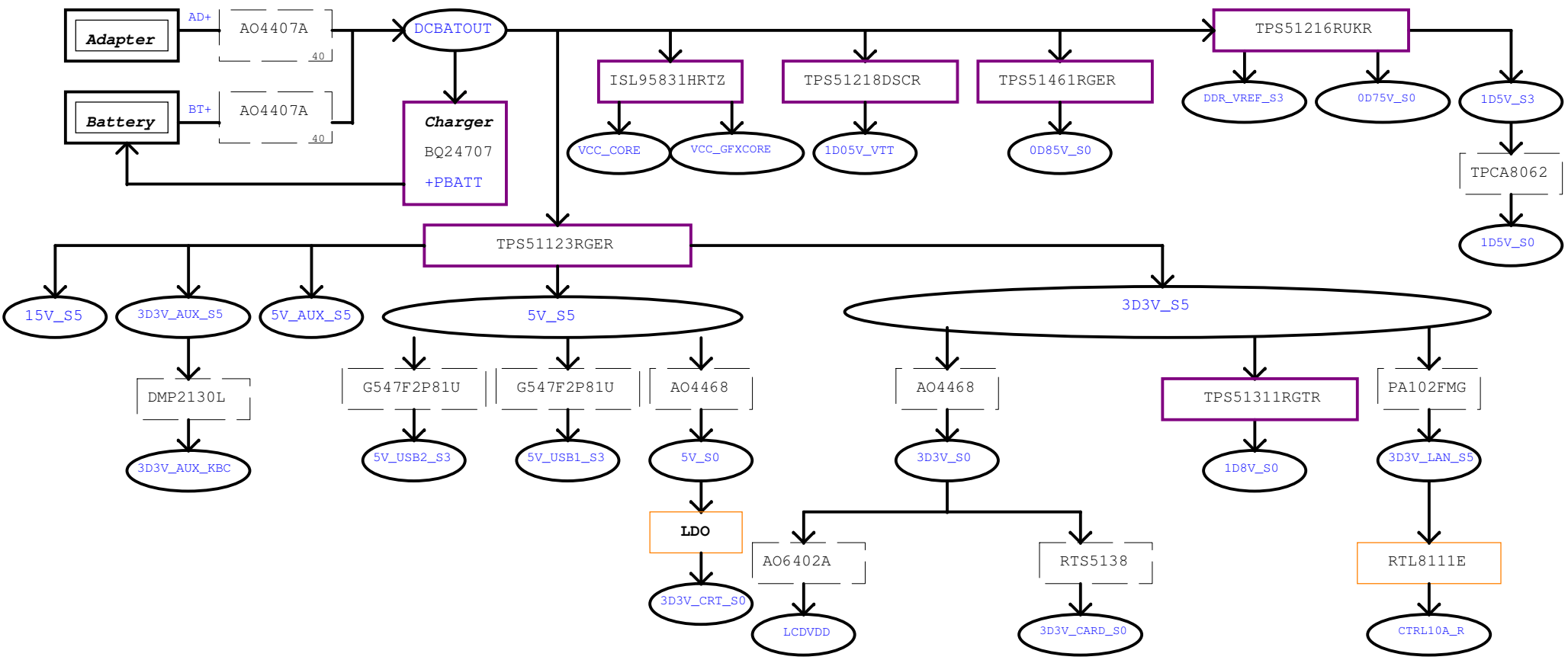


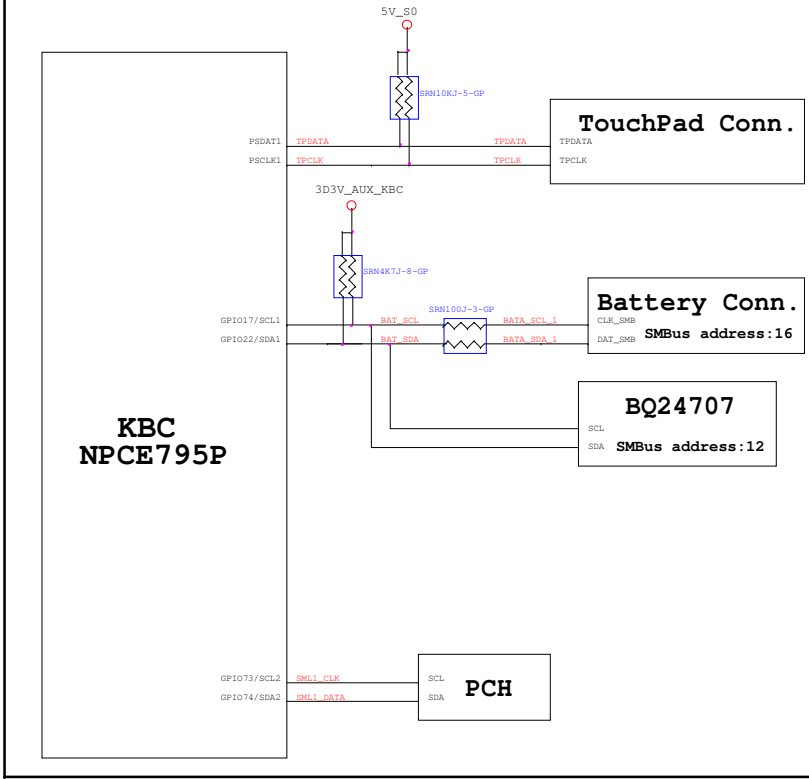
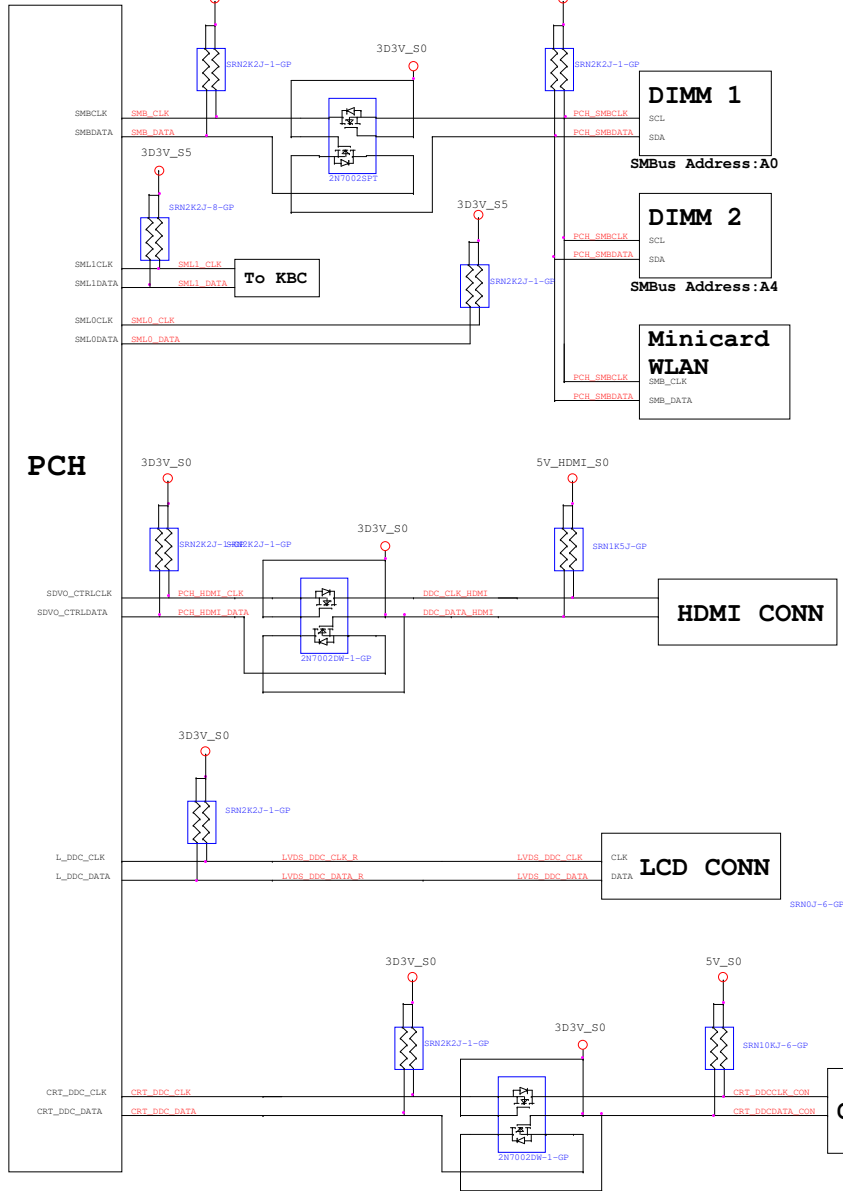
Wistron HURON RIVER POWER UP SEQUENCE DIAGRAM



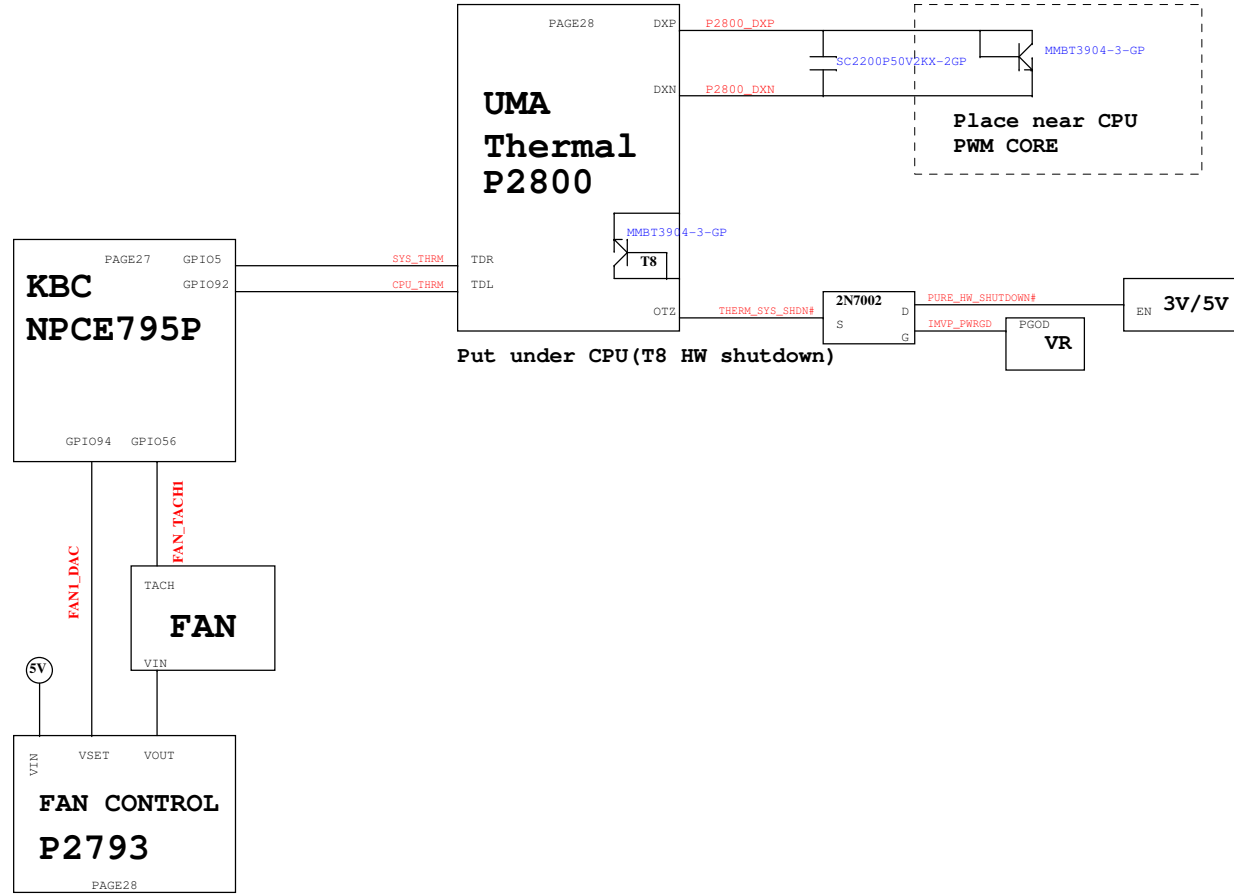
起点主板维修网 www.qdzbwx.com

Power Up Sequence: [-8] ~ [15]





Thermal Block Diagram



Audio Block Diagram

