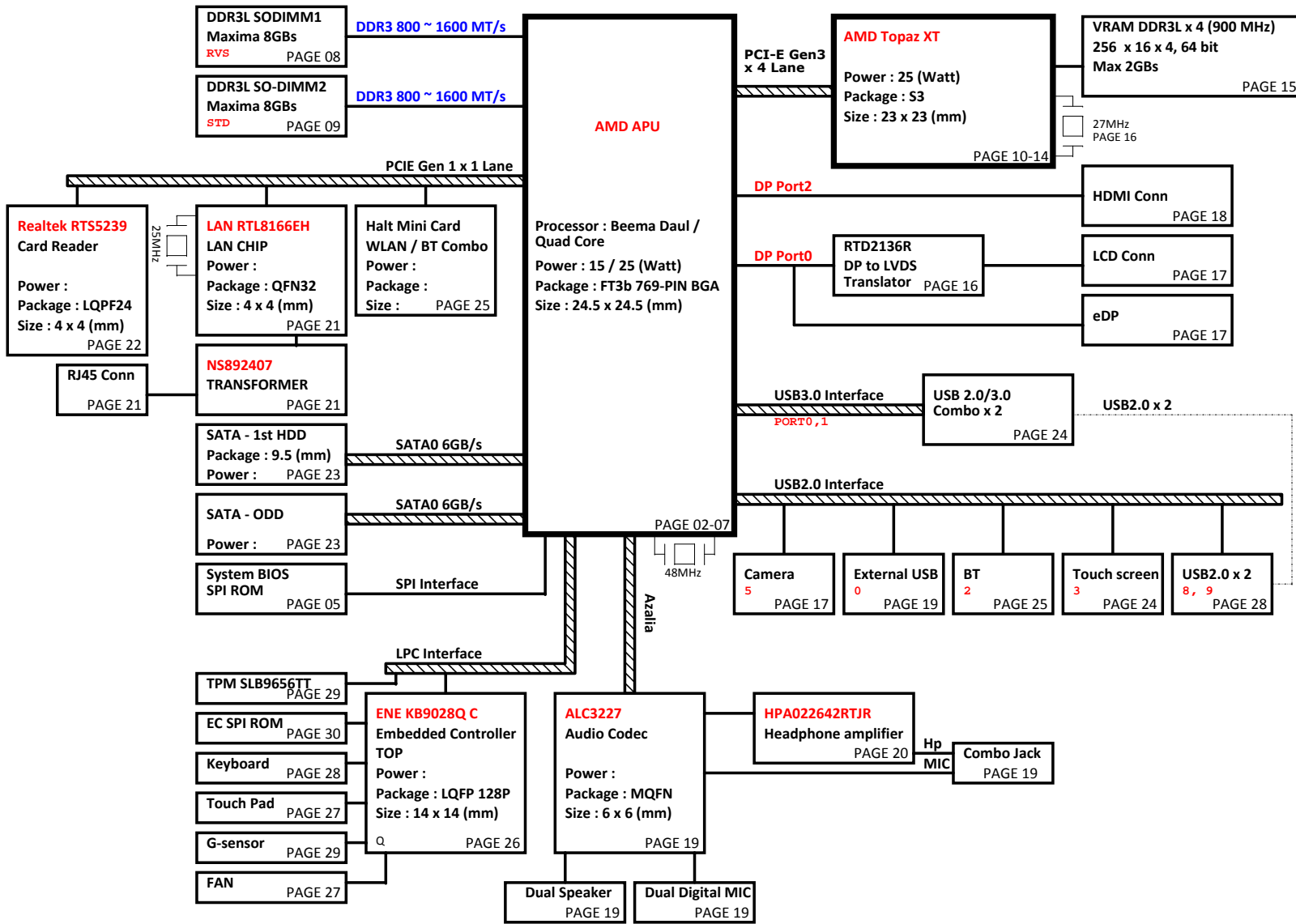


VINE_AMD Beema DIS/UMA (14.0"/15.6"/17.3")



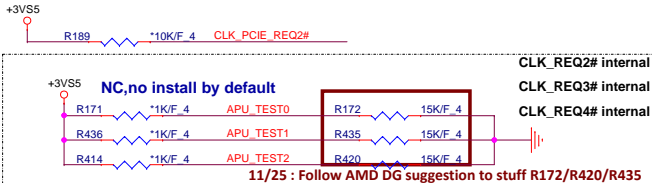
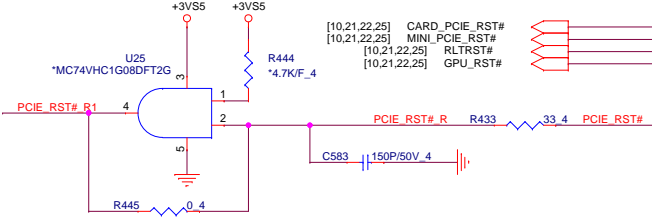
PCB 6L STACK UP

- LAYER 1 : TOP
- LAYER 2 : SGND
- LAYER 3 : IN1(High)
- LAYER 4 : IN2(Low)
- LAYER 5 : SVCC
- LAYER 6 : BOT

Power Source

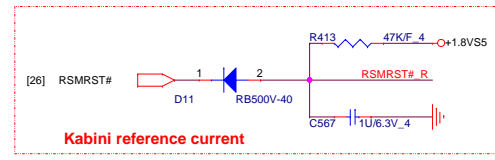
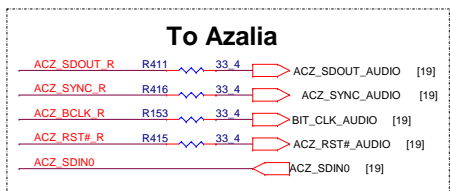
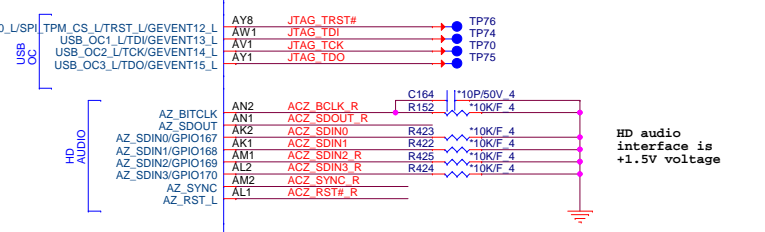
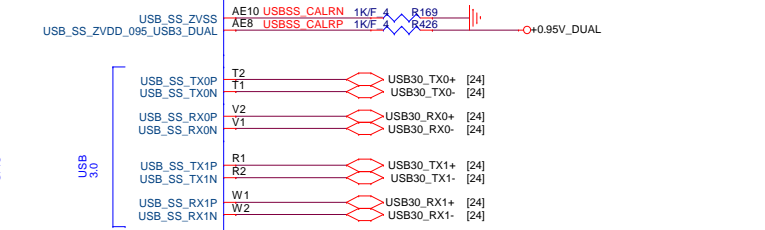
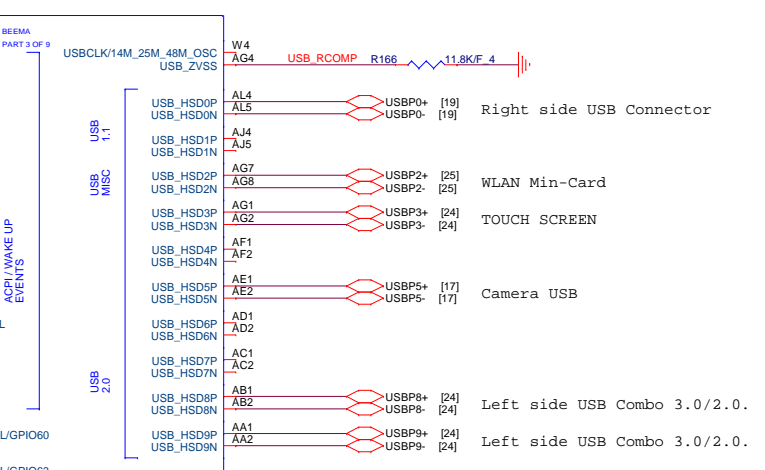
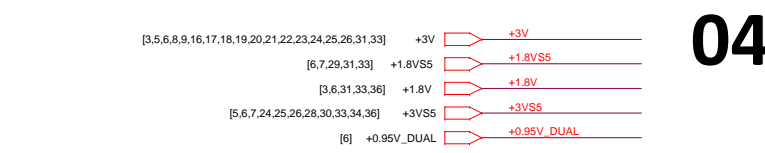
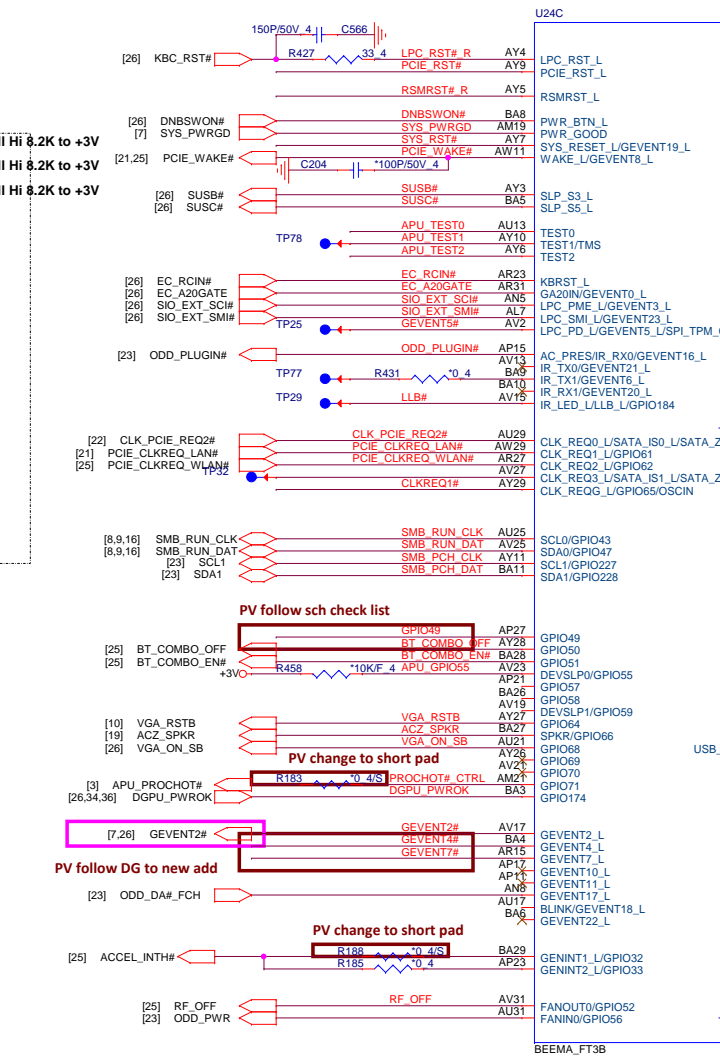
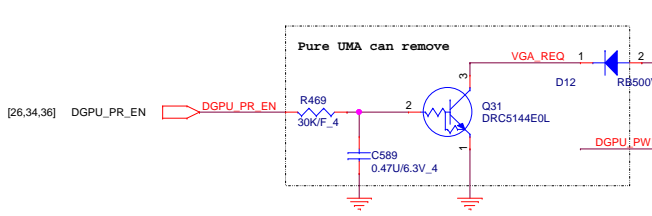
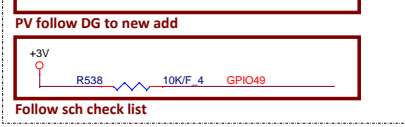
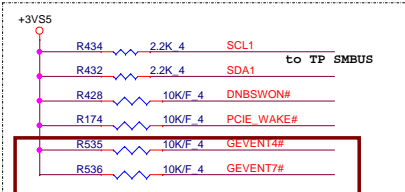
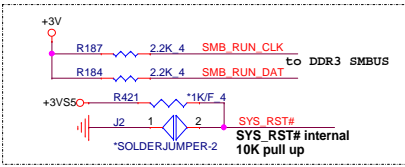
- BQ24728H**
System Charge Power (+BATCHG)
- SY8208B / SY8208C**
System Power (+3VPCU/+5VPCU/+3V55/+5V55)
- RT8231BGQW**
System Memory Power (+1.35VSUS/+0.65V_DDR_VTT)
- ISL6277A / ISL6208BCRZ**
Processor Power (+VCC_CORE/+VDDNB_CORE)
- AOZ1267QI-02 / APW8824**
Processor Power (+0.95V/+0.95V55/+1.5V55)
- RT8899AGQW**
DGPU Power (+VGA_CORE/+1.35V_VGA)
- APW8804 / APL3523A**
DGPU Power (+0.95V_VGA/+3V_VGA/+1.8V_VGA)

	PROJECT : Y22A		Rev 1A
	Quanta Computer Inc.		
	Size	Document Number	
Block Diagram		Date: Thursday, March 27, 2014	Sheet 1 of 36



11/25 : Follow AMD DG suggestion to stuff R172/R420/R435

TEST2	TEST1	TEST0	Description
0	0	0	FCH TAP accessible from APU when TAPEN is asserted FCH JTAG pins are overloaded for multiple functions, in this configuration the FCH JTAG are used as non-JTAG pins
0	0	1	Reserved
0	1	X	Reserved
1	TMS	0	FCH JTAG multi-function pins are configured as JTAG pins, in this configuration the FCH TAP can be accessed from FCH JTAG pins
1	TMS	1	Use on ATE only Yuba JTAG enabled



PROJECT : Y22A
Quanta Computer Inc.

NB5

Size: Document Number: **GPIO/USB/AZ (3/6)** Rev: 1A

Date: Wednesday, March 19, 2014 Sheet 4 of 36

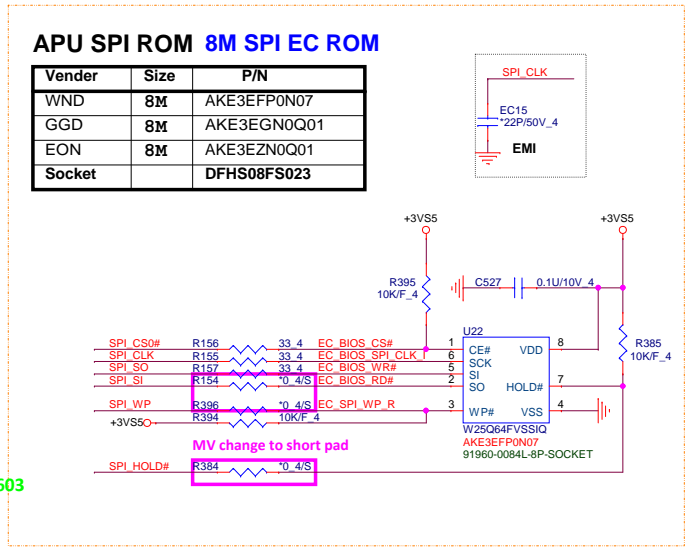
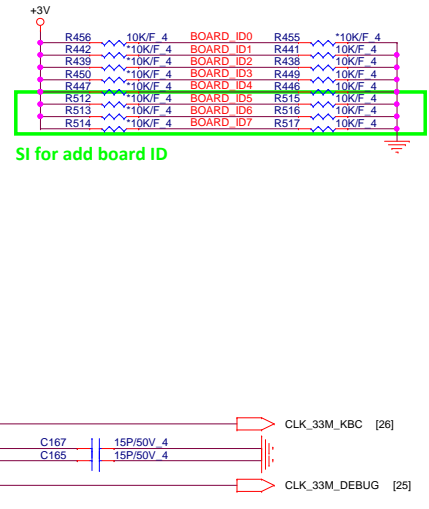
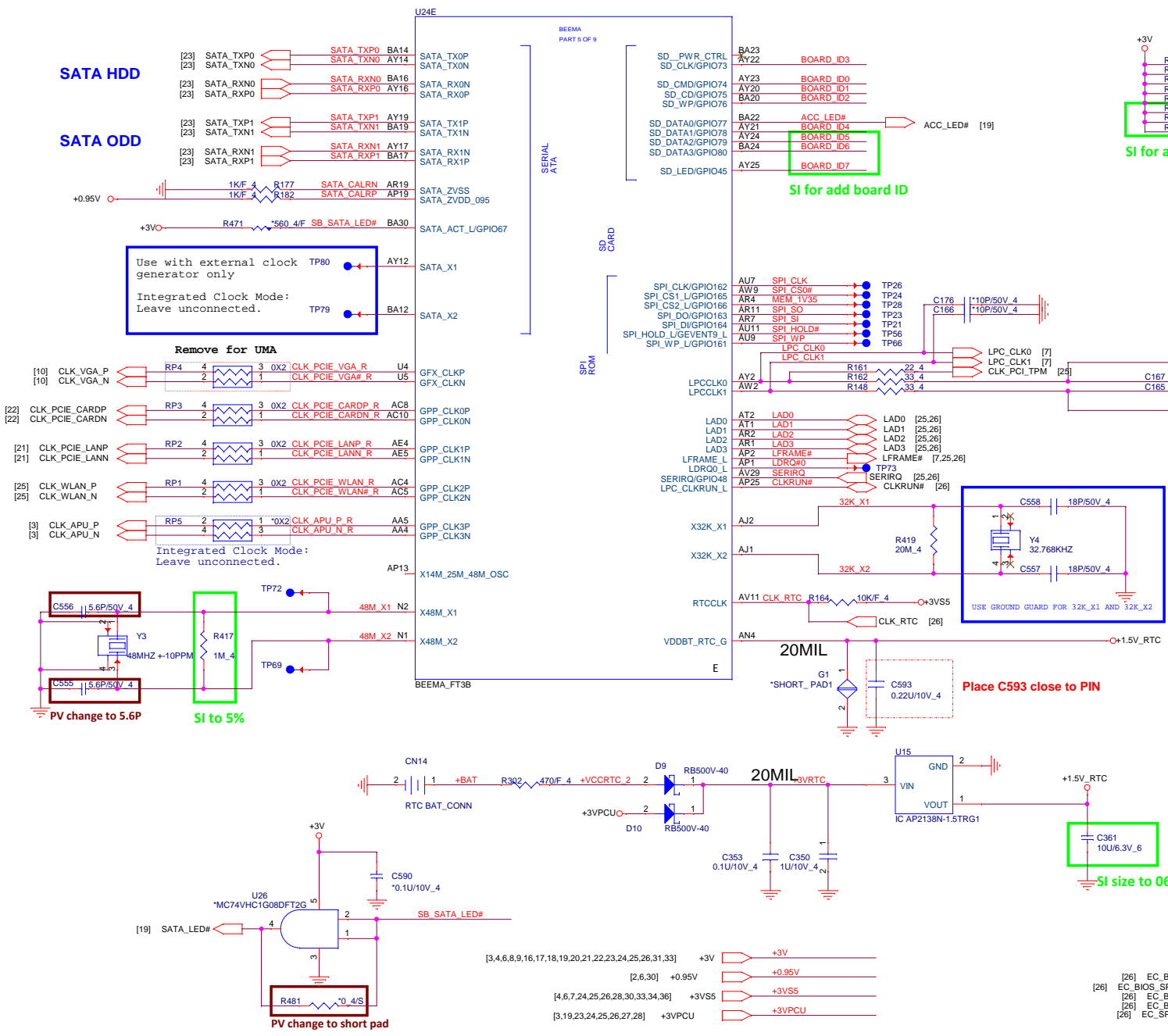
BOARD ID SETTING

Board ID 0	Definition
0	UMA
1	SG

Board ID [2:1]	Definition
00	14"
01	15"
10	17"

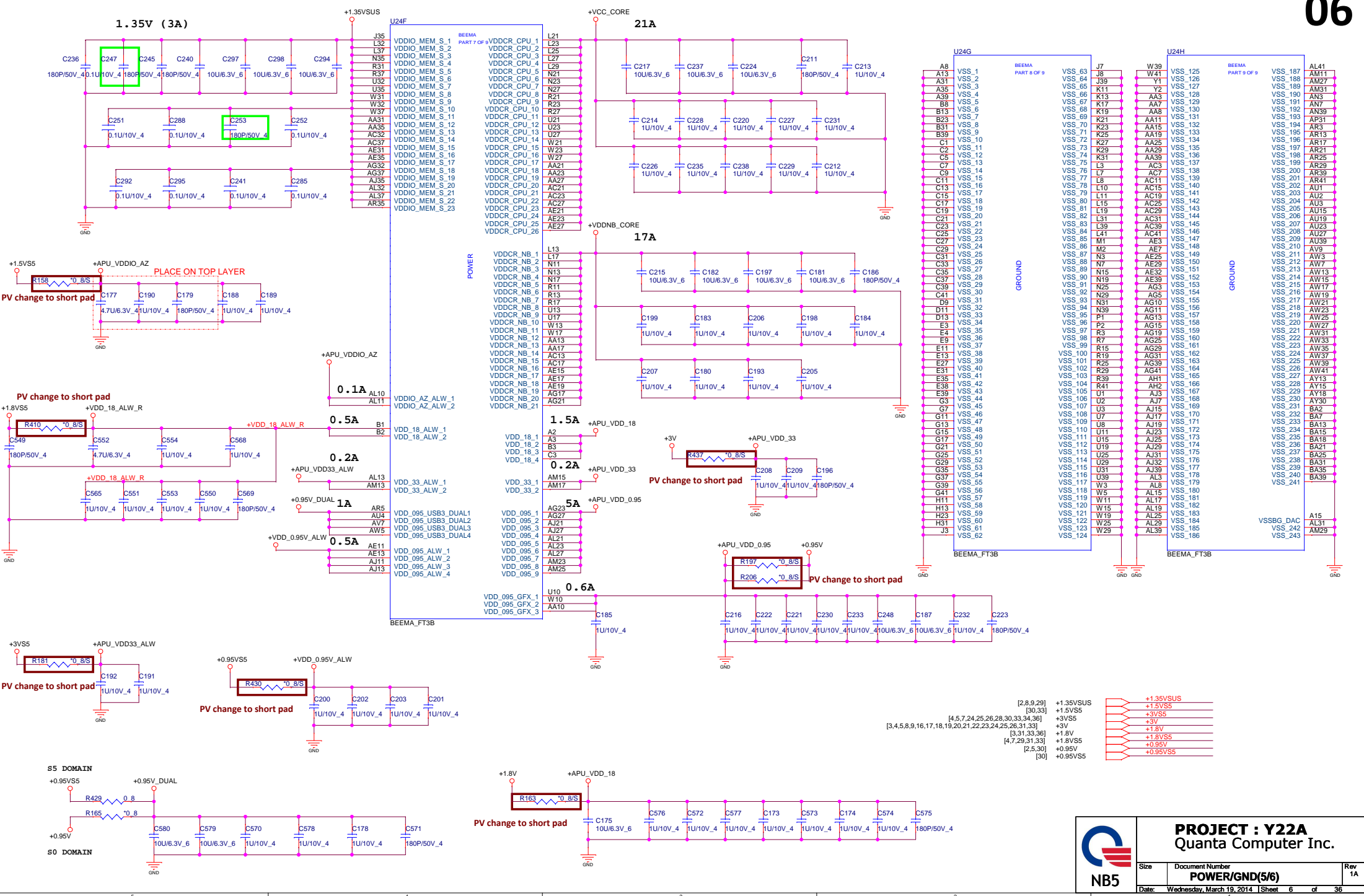
Board ID [4:3]	Definition
00	Pavilion
01	Envy
10	Pavilion Special Edition

Board ID [7:5]	Definition
000	Reserve



PROJECT : Y22A
Quanta Computer Inc.

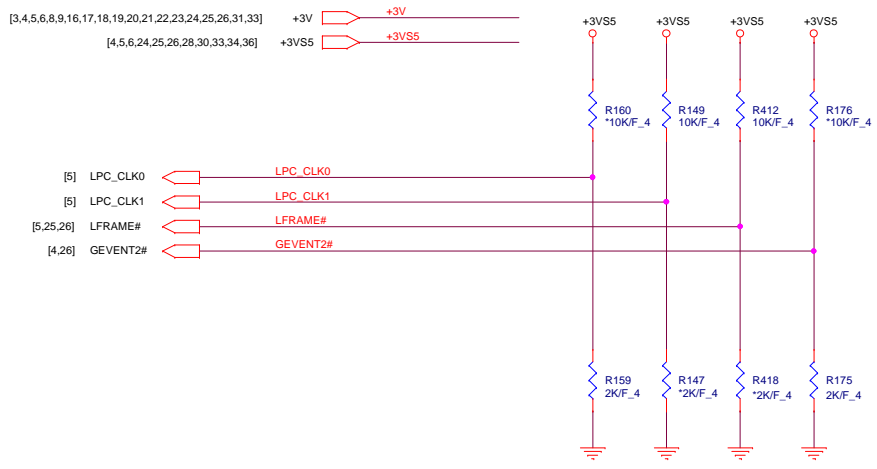
Size	Document Number SATA/CLK (4/6)	Rev 1A
Date: Thursday, March 27, 2014 Sheet 5 of 36		



	PROJECT : Y22A Quanta Computer Inc.		Rev 1A
	Size	Document Number POWER/GND(5/6)	

STRAPS PINS

OVERLAP COMMON PADS WHERE POSSIBLE FOR DUAL-OP RESISTORS.

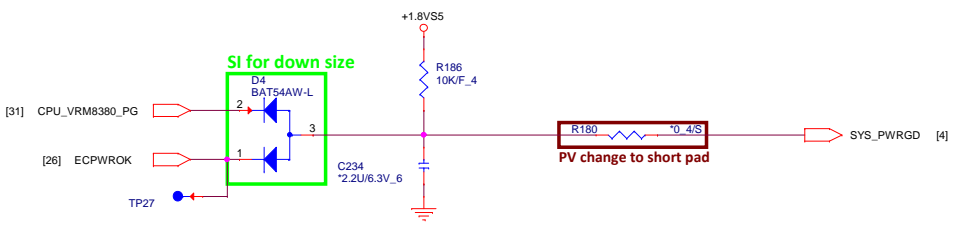


REQUIRED STRAPS

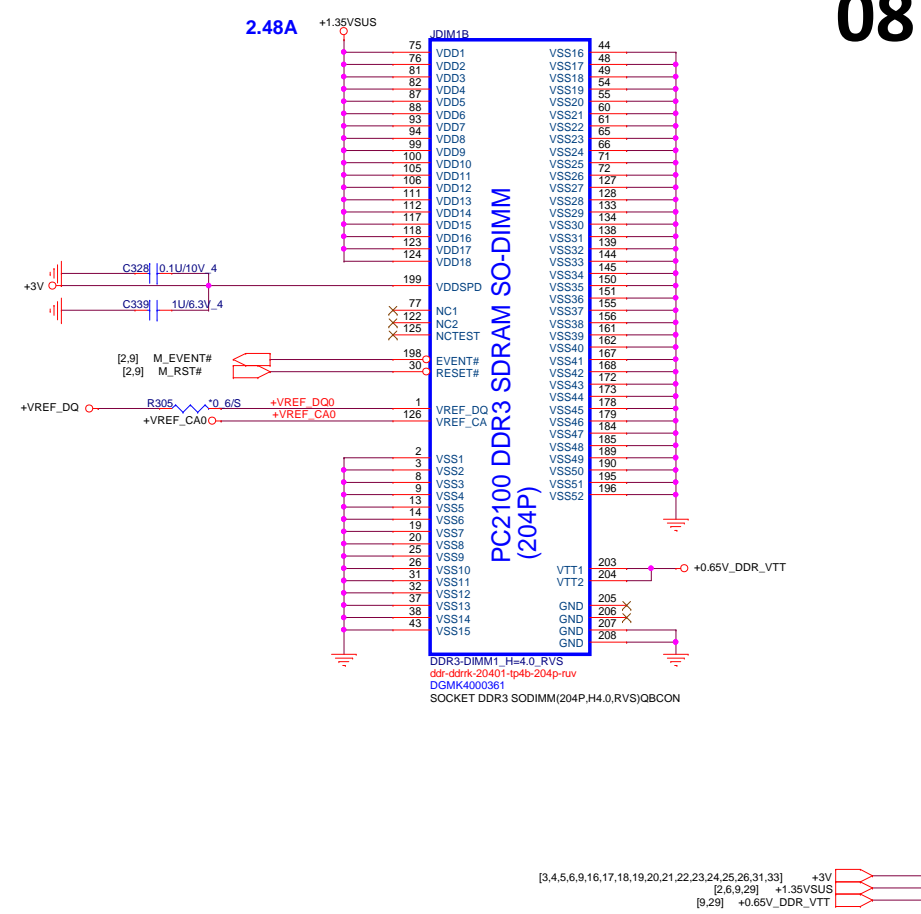
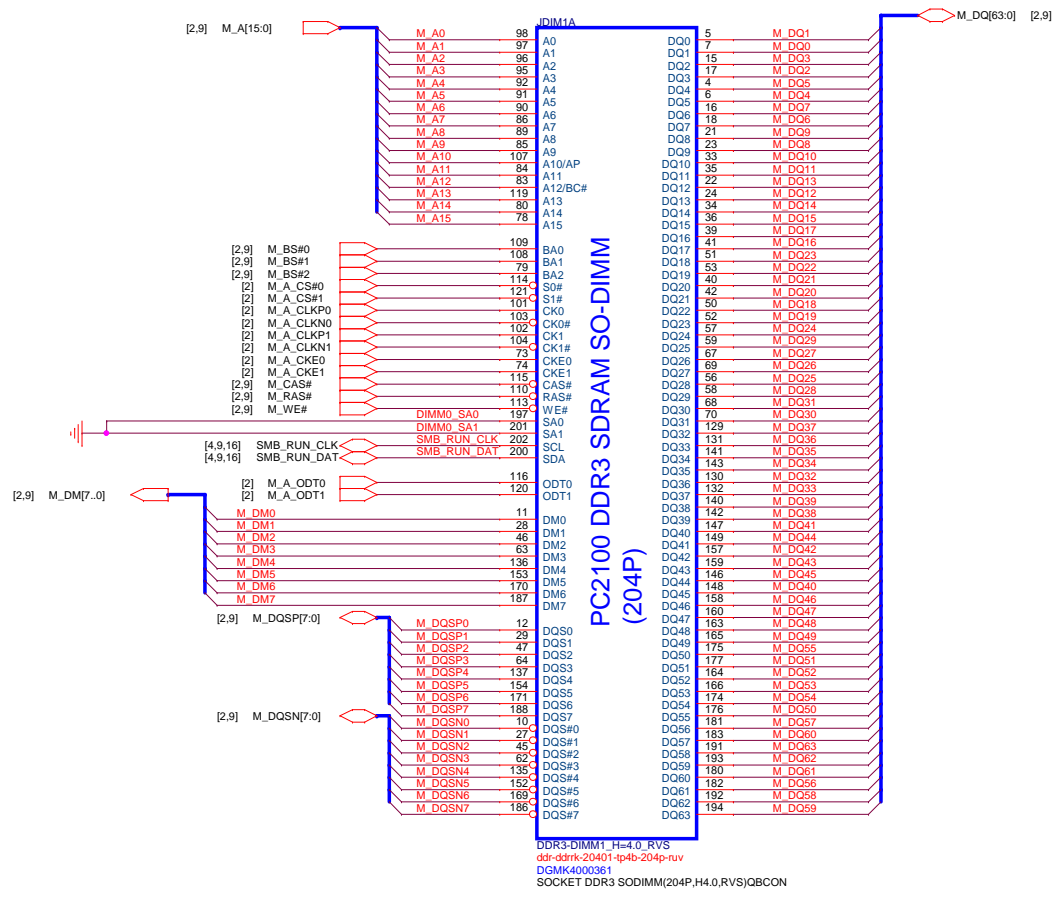
				LPC_CLK0	LPC_CLK1	LFRAME#	GEVENT2#
PULL HIGH				BOOT FAIL TIMER ENABLED	CLKGEN ENABLED DEFAULT	SPI ROM DEFAULT	1.8V SPI ROM
PULL LOW				BOOT FAIL TIMER DISABLED DEFAULT	CLKGEN DISABLED	LPC ROM	3.3V SPI ROM DEFAULT

DEBUG STRAPS

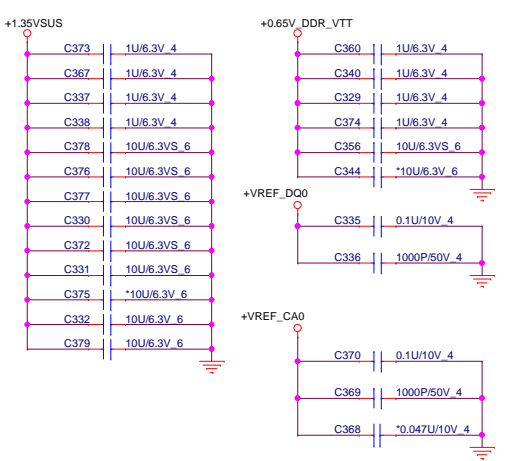
SYS_PWRGD



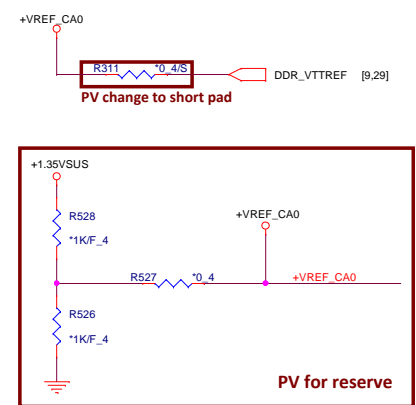
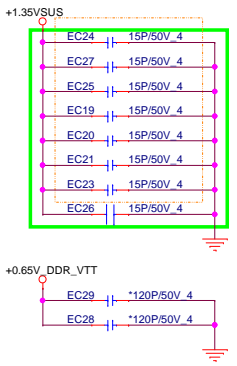
	PROJECT : Y22A		Rev 1A
	Quanta Computer Inc.		
	Size	Document Number	
	STRAP (6/6)		
	Date: Wednesday, March 19, 2014		Sheet 7 of 36



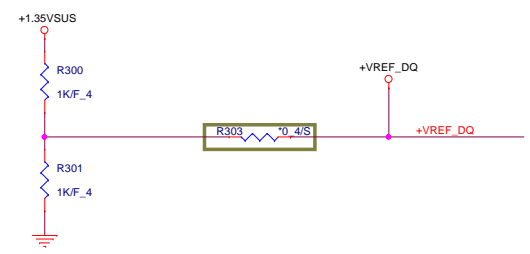
Place these Caps near So-Dimm0.



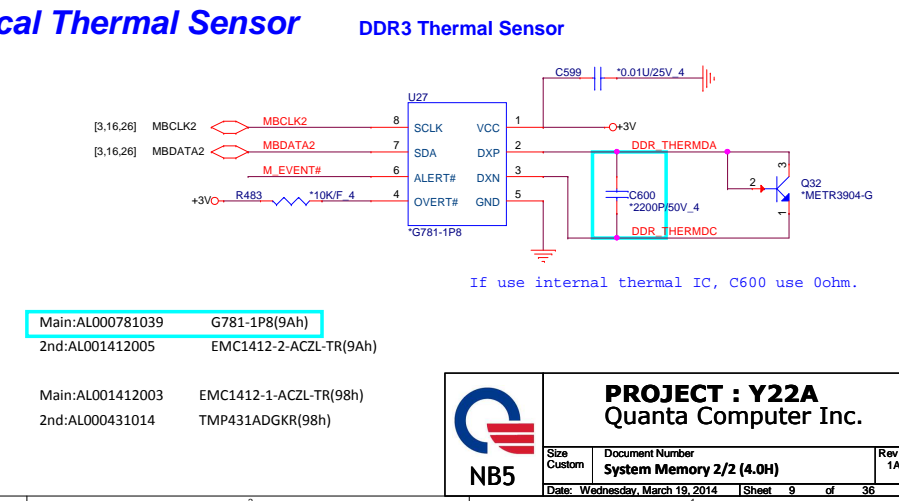
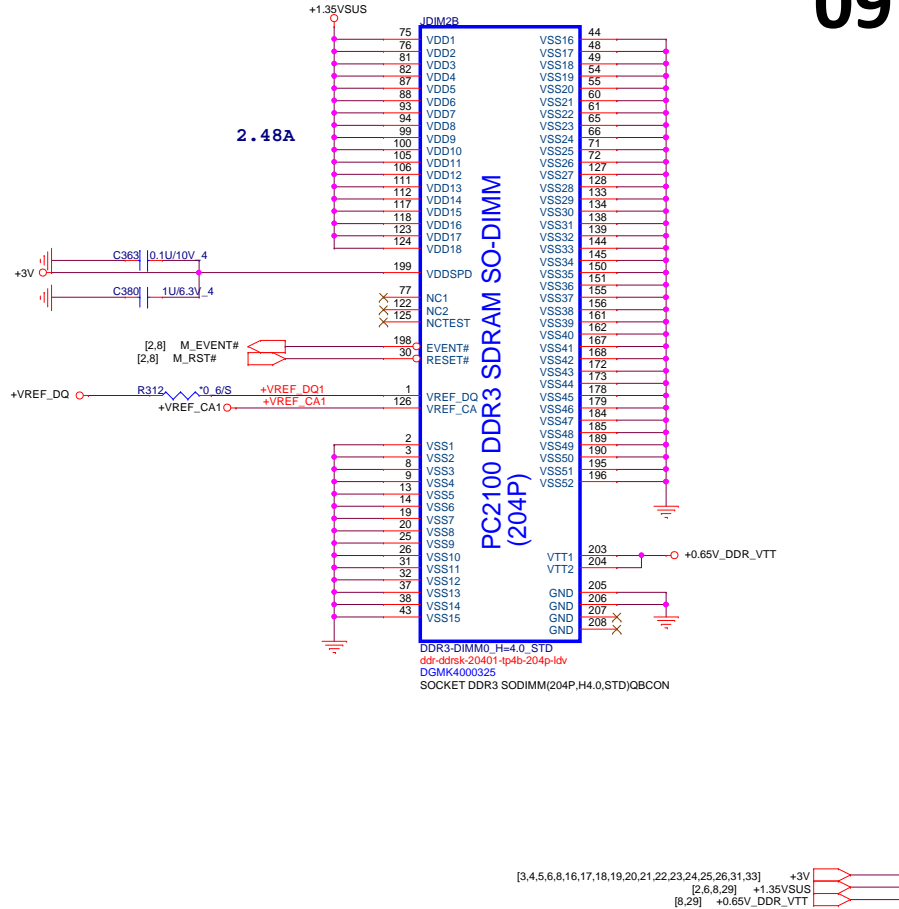
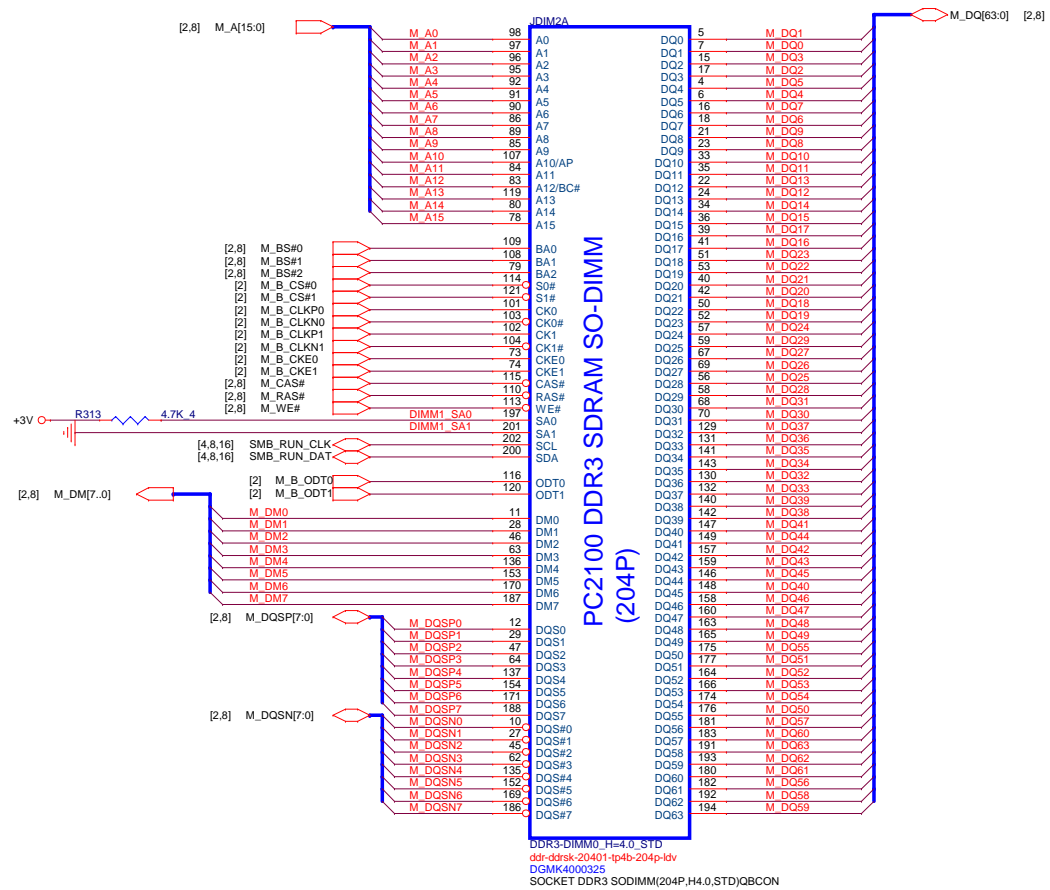
For EMI RESERVE



Reserved for AMD suggest



	PROJECT : Y22A		Rev 1A
	Quanta Computer Inc.		
	Size Custom	Document Number System Memory 1/2 (4.0H)	
Date: Wednesday, March 19, 2014	Sheet 8	of 36	

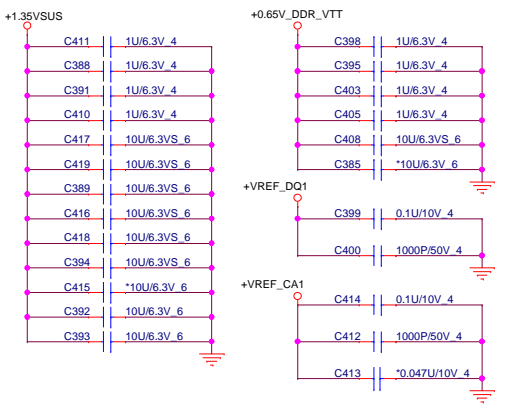


Main:AL000781039	G781-1P8(9Ah)
2nd:AL001412005	EMC1412-2-ACZL-TR(9Ah)
Main:AL001412003	EMC1412-1-ACZL-TR(98h)
2nd:AL000431014	TMP431ADGKR(98h)

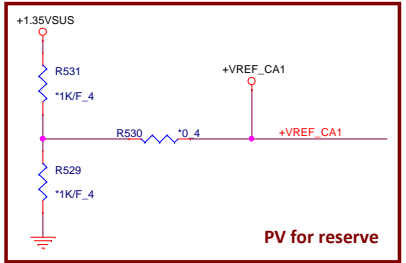
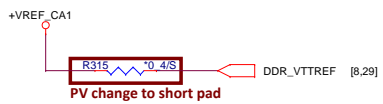
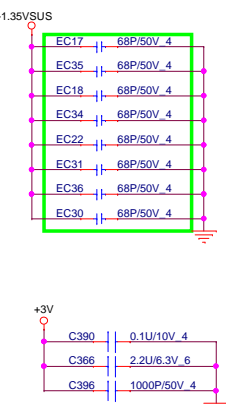
PROJECT : Y22A
Quanta Computer Inc.

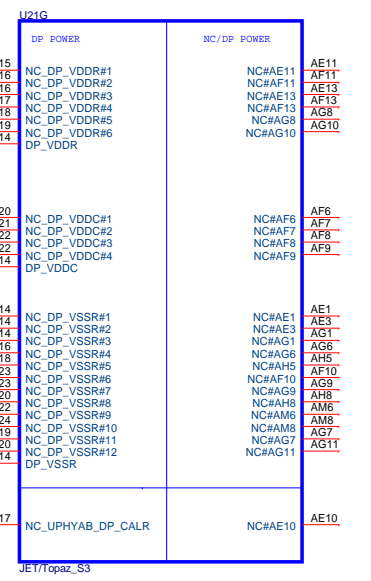
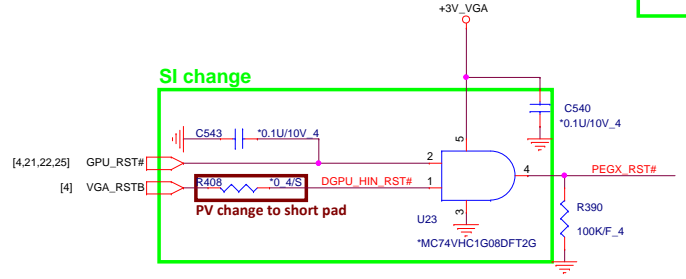
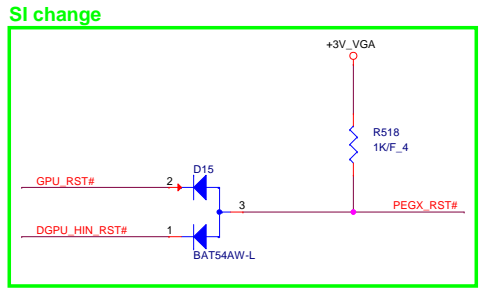
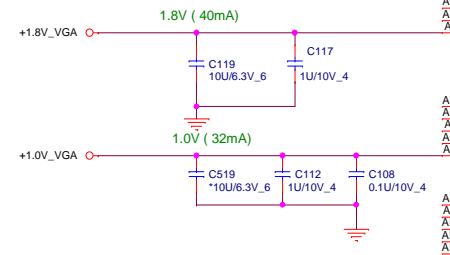
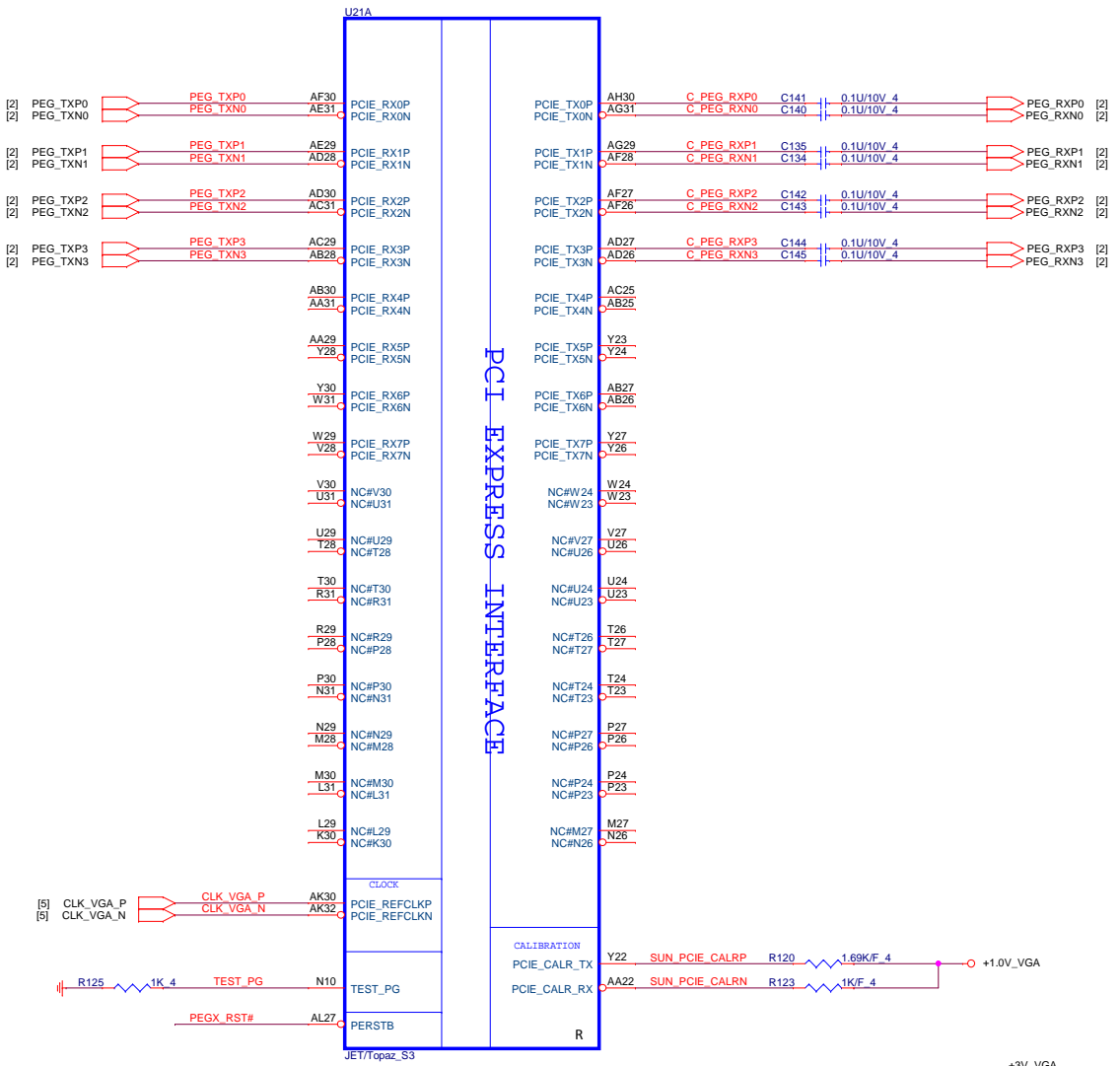
Size	Document Number	Rev
Custom	System Memory 2/2 (4.0H)	1A
Date: Wednesday, March 19, 2014	Sheet 9 of 36	

Place these Caps near So-Dimm1.

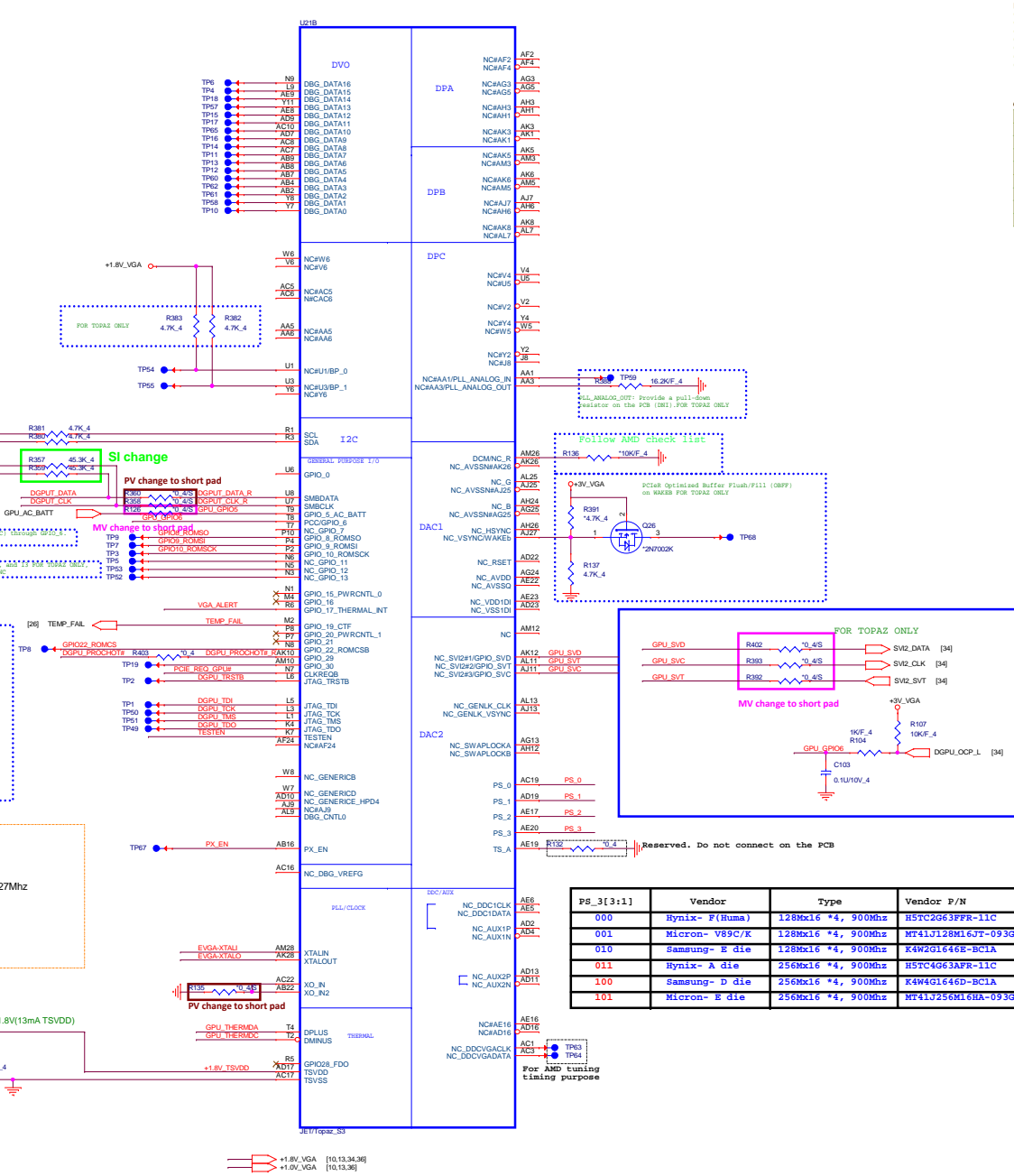
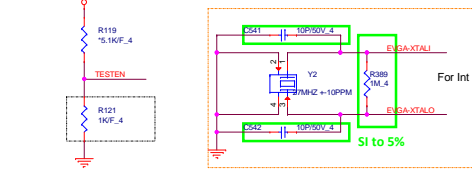
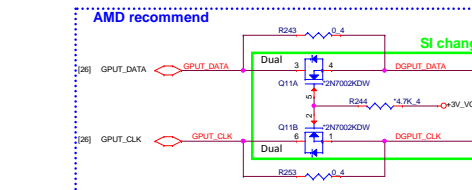
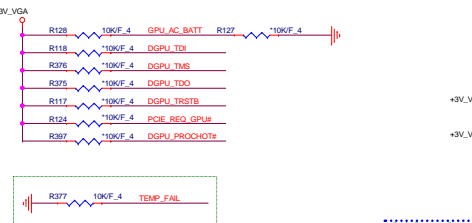
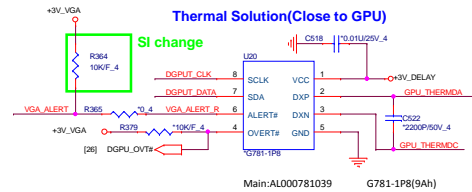


For EMI RESERVE





	PROJECT : Y22A Quanta Computer Inc.		Rev 1A
	Size NB5	Document Number TOPAZ S3 PCIE/DP power	



MPS Implementation

- Connect GPIO_28 to 10K pull-down to enable MPS
- If any of PS_0/1/2/3 is not used, leave "no connect"
- R_pu, R_pd and C must be properly populated per tables below
- Place MPS circuit components as close to the ASIC as possible
- Total DC resistance of trace between PS pin and C should be less than 2 ohms
- Total DC resistance of trace between C and ground should be less than 2 ohms
- Trace capacitance should be of +/-1% tolerance

C (pF)	0805(3,4)
680	00
82	01
10	10
NC	11

R_pu (Ohm)	R_pd (Ohm)	Bits(2,1)
NC	NC	4750 000
82	01	8450 2000 001
10	10	4530 2000 010
NC	11	6980 4990 011
		4530 4990 100
		3240 5620 101
		3400 10000 110
		4750 NC 111

MPS Bit	Strap Name	Description	Recommended Settings
PS_011	ROM_CONFIG0	If STRAP_BIOS_ROM_EN = 1, ROM_CONFIG[0] defines the ROM type.	Design dependent, see the description.
PS_012	ROM_CONFIG1	If STRAP_BIOS_ROM_EN = 0, ROM_CONFIG[0] defines the primary memory aperture size. See Primary Memory Aperture Size (p. 29)	Design dependent, see the description.
PS_013	ROM_CONFIG2		
PS_041	N/A	Reserved for internal use only. Must be 1 at reset.	1
PS_015	N/A	Reserved.	1
PS_111	STRAP_BIF_GEN3_EN_A	PCIe GEN3 capability. 0 = PCIe GEN3 is not supported. 1 = PCIe GEN3 is supported.	Design dependent, see the description.
PS_112	STRAP_BIF_CLK_PM_EN	Determines whether or not the PCIe reference clock power management capability is reported in the PCI configuration space (otherwise known as CLKREQ#). 0 = The CLKREQ# power management capability is disabled. 1 = The CLKREQ# power management capability is enabled.	0
PS_113	N/A	Reserved for internal use only. Must be 0 at reset.	0
PS_114	STRAP_TX_CFG_DRV_FULL_SWING	Control the transmitter full-half-swing mode. 0 = The transmitter half-swing is enabled. 1 = The transmitter full-swing is enabled.	1
PS_211	STRAP_TX_DEEMPH_EN	PCI EXPRESS transmitter, deemphasis enable. 0 = Tx deemphasis disabled. 1 = Tx deemphasis enabled.	Design dependent, see the description.
PS_212	N/A	Reserved.	0
PS_213	STRAP_BIOS_ROM_EN	To enable the external BIOS ROM device. 0 = Disable the external BIOS ROM device. 1 = Enable the external BIOS ROM device.	Design dependent, see the description.
PS_214	N/A	Reserved.	1
PS_215	N/A	Reserved.	1
PS_311	BOARD_CONFIG0	Board configuration related strapping, such as for memory ID	Design dependent, see the description.
PS_312	BOARD_CONFIG1		
PS_313	BOARD_CONFIG2		
PS_314	N/A	Reserved.	1
PS_315	N/A	Reserved.	1

PS_3[3:1]	Vendor	Type	Vendor P/N	PU	PD
000	Hynix- F(huma)	128Mx16 *4, 900Mhz	H5TC2G61FR-11C	NC	4.75K
001	Micron- V89C/K	128Mx16 *4, 900Mhz	MT41J128H16J7-093G:K	8.45K	2K
010	Samsung- E die	128Mx16 *4, 900Mhz	K4WZG1646E-BCL1A	4.53K	2K
011	Hynix- A die	256Mx16 *4, 900Mhz	H5TC4G63AFR-11C	6.98K	4.99K
100	Samsung- D die	256Mx16 *4, 900Mhz	K4W4G1646D-BCL1A	4.53K	4.99K
101	Micron- E die	256Mx16 *4, 900Mhz	MT41J256M16HA-093G:E	3.24K	5.62K

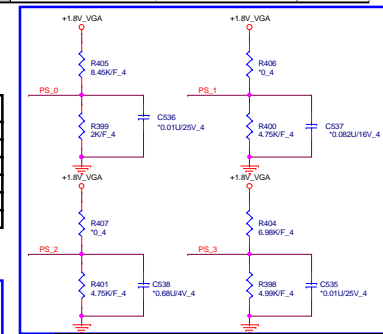
BITS => BIT0

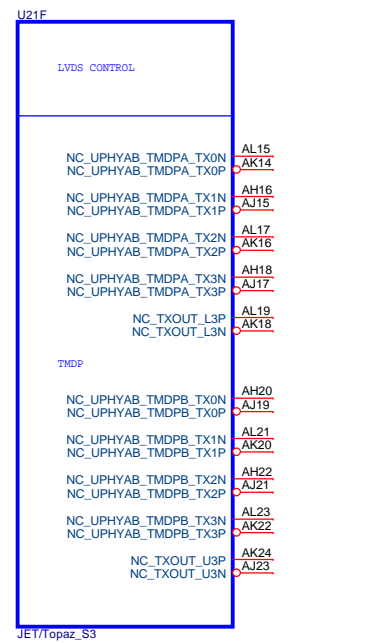
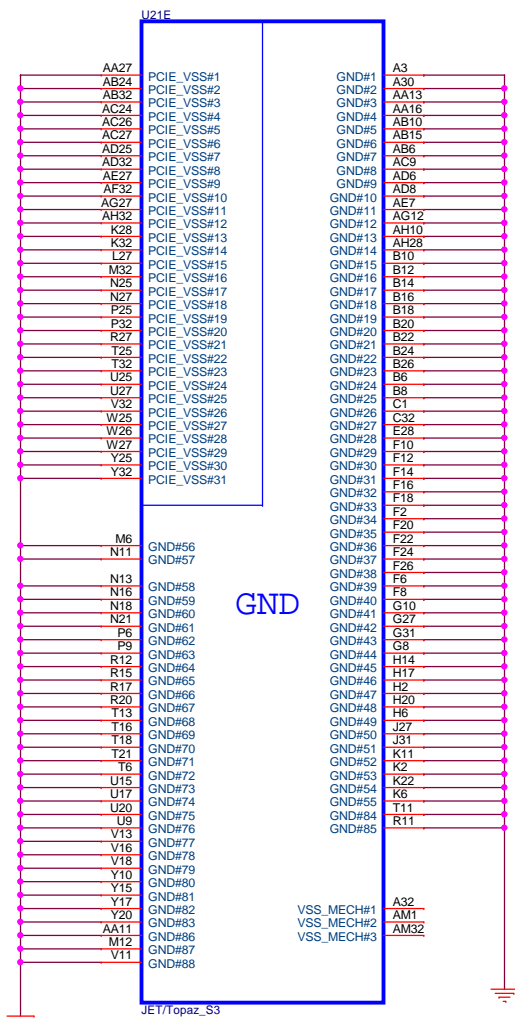
PS0 => 11001

PS1 => 11000

PS2 => 11000

PS3 => 11011





CONFIGURATION STRAPS-- SEE EACH DATABOOK FOR STRAP DETAILS

ALLOW FOR PULLUP PADS FOR THESE STRAPS AND IF THESE GPIOs ARE USED, THEY MUST NOT CONFLICT DURING RESET

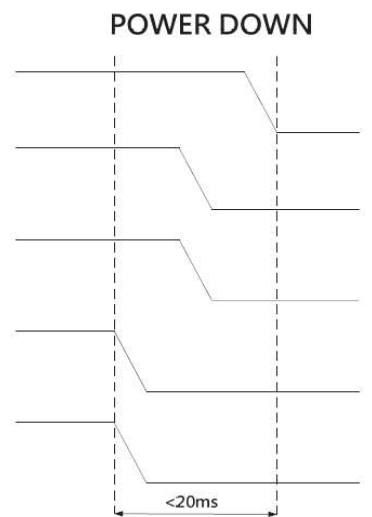
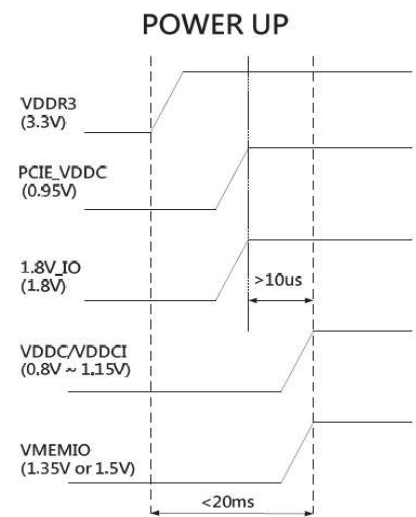
RECOMMENDED SETTINGS
 0= DO NOT INSTALL RESISTOR
 1= INSTALL 3K RESISTOR
 X = DESIGN DEPENDANT
 NA = NOT APPLICABLE

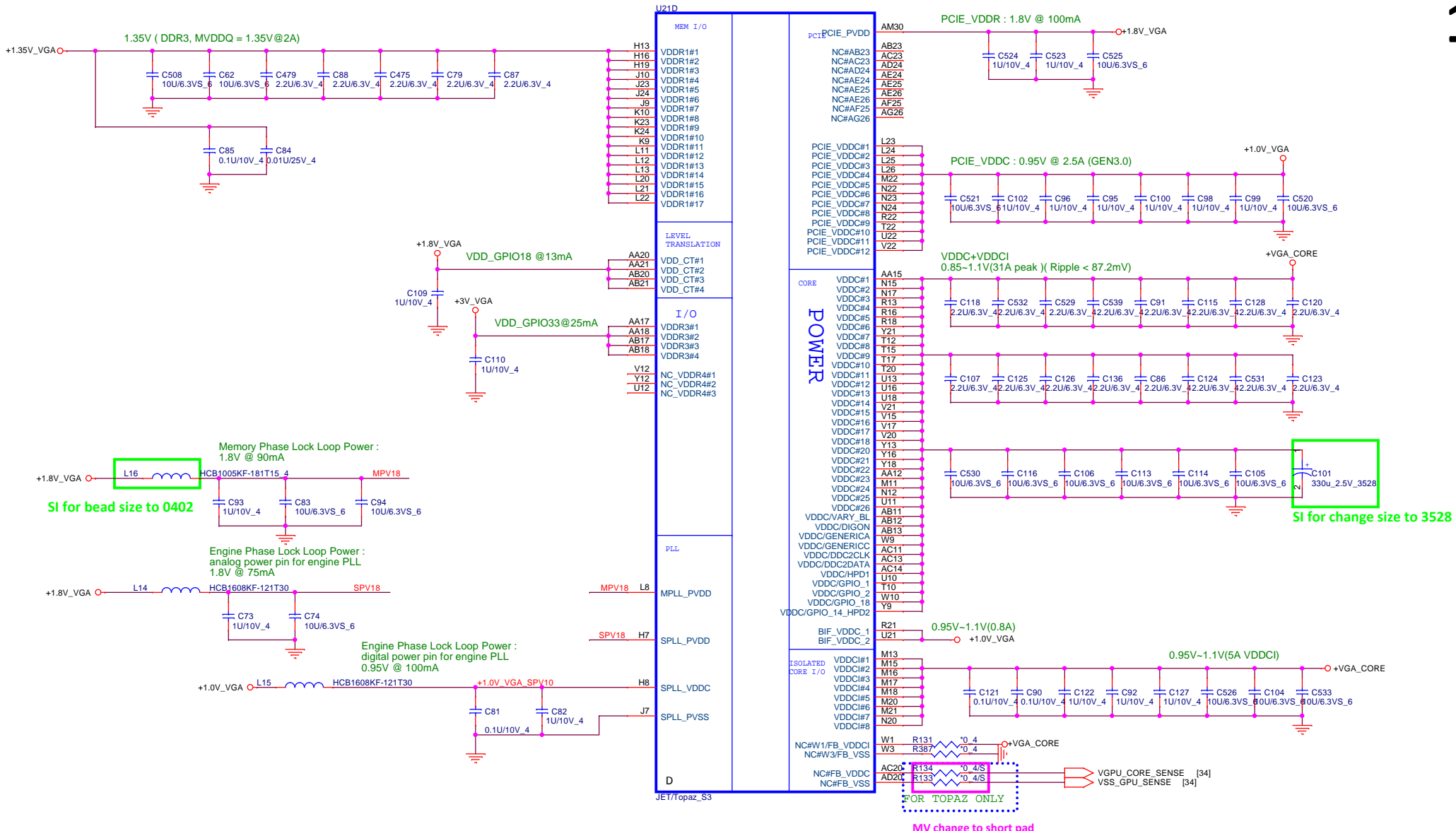
STRAPS	PIN	DESCRIPTION OF DEFAULT SETTINGS	
TX_PWRS_ENB	GPIO0	PCIE FULL TX OUTPUT SWING	0
TX_DEEMPH_EN	GPIO1	PCIE TRANSMITTER DE-EMPHASIS ENABLED	X
RSVD	GPIO2	RESERVED	0
RSVD	GPIO8	RESERVED	0
BIF_VGA_DIS	GPIO9	VGA ENABLED	0
RSVD	GPIO21	RESERVED	0
BIOS_ROM_EN	GPIO_22_ROMCSB	ENABLE EXTERNAL BIOS ROM	0
ROMIDCFG(2:0)	GPIO[13:11]	SERIAL ROM TYPE OR MEMORY APERTURE SIZE SELECT	0 0 1
VIP_DEVICE_STRAP_ENA	V2SYNC	IGNORE VIP DEVICE STRAPS (Removed on Seymour/W/histler)	0
RSVD	H2SYNC	RESERVED	0
AUD[1]	HSYNC	SEE DATABOOK FOR DETAIL	0
AUD[0]	VSYN	SEE DATABOOK FOR DETAIL	0
RSVD	GENERICC	RESERVED	0

NOTE1: AMD RESERVED CONFIGURATION STRAPS
 ALLOW FOR PULLUP PADS FOR THESE STRAPS BUT DO NOT INSTALL RESISTOR. IF THESE GPIOs ARE USED, THEY MUST KEEP "LOW" AND NOT CONFLICT DURING RESET.

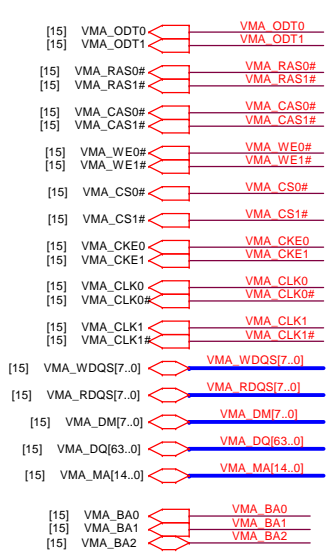
GPIO21 H2SYNC GENERICC GPIO8 GPIO2

POWER UP / POWER DOWN SEQUENCE

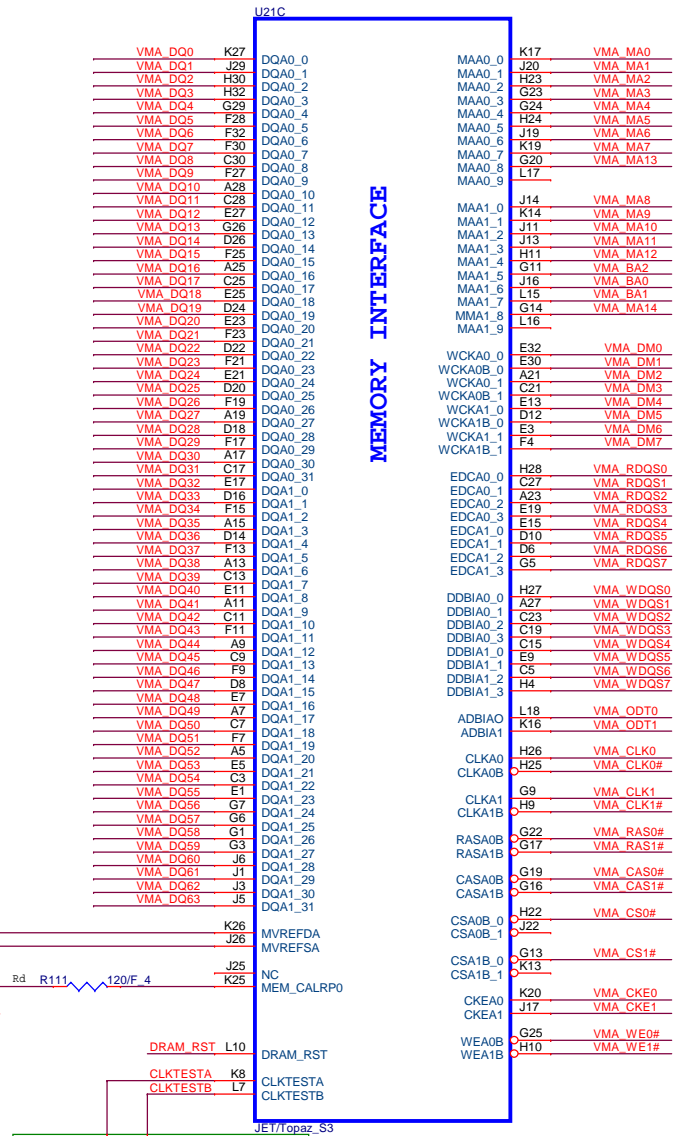
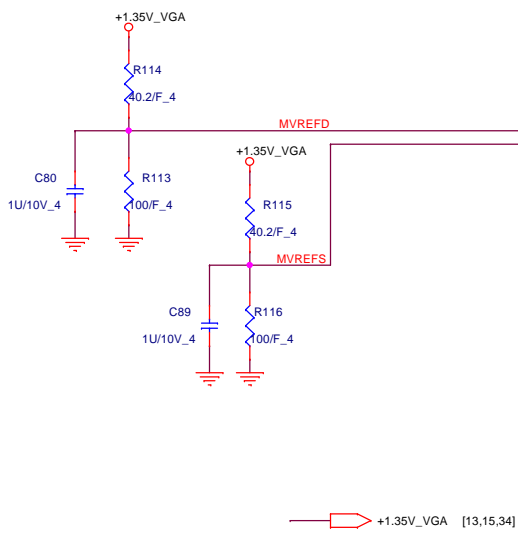




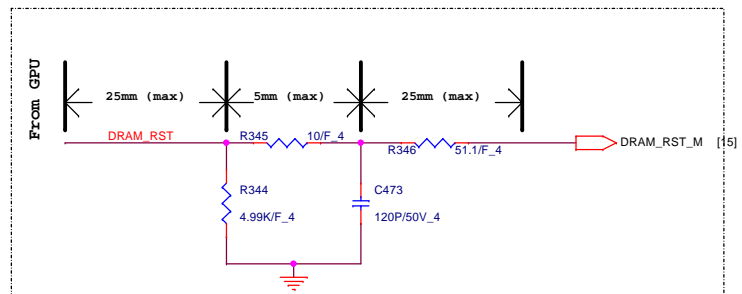
	PROJECT : Y22A		Rev 1A
	Quanta Computer Inc.		
	Size	Document Number	
	TOPAZ S3 Power		
Date: Thursday, March 27, 2014	Sheet 13	of 36	



support 1Gbit
VRAM (64M X 16)



MEMORY INTERFACE



Place all these components very close to GPU (Within 25mm) and keep all component close to each Other (within 5mm) except Rser2

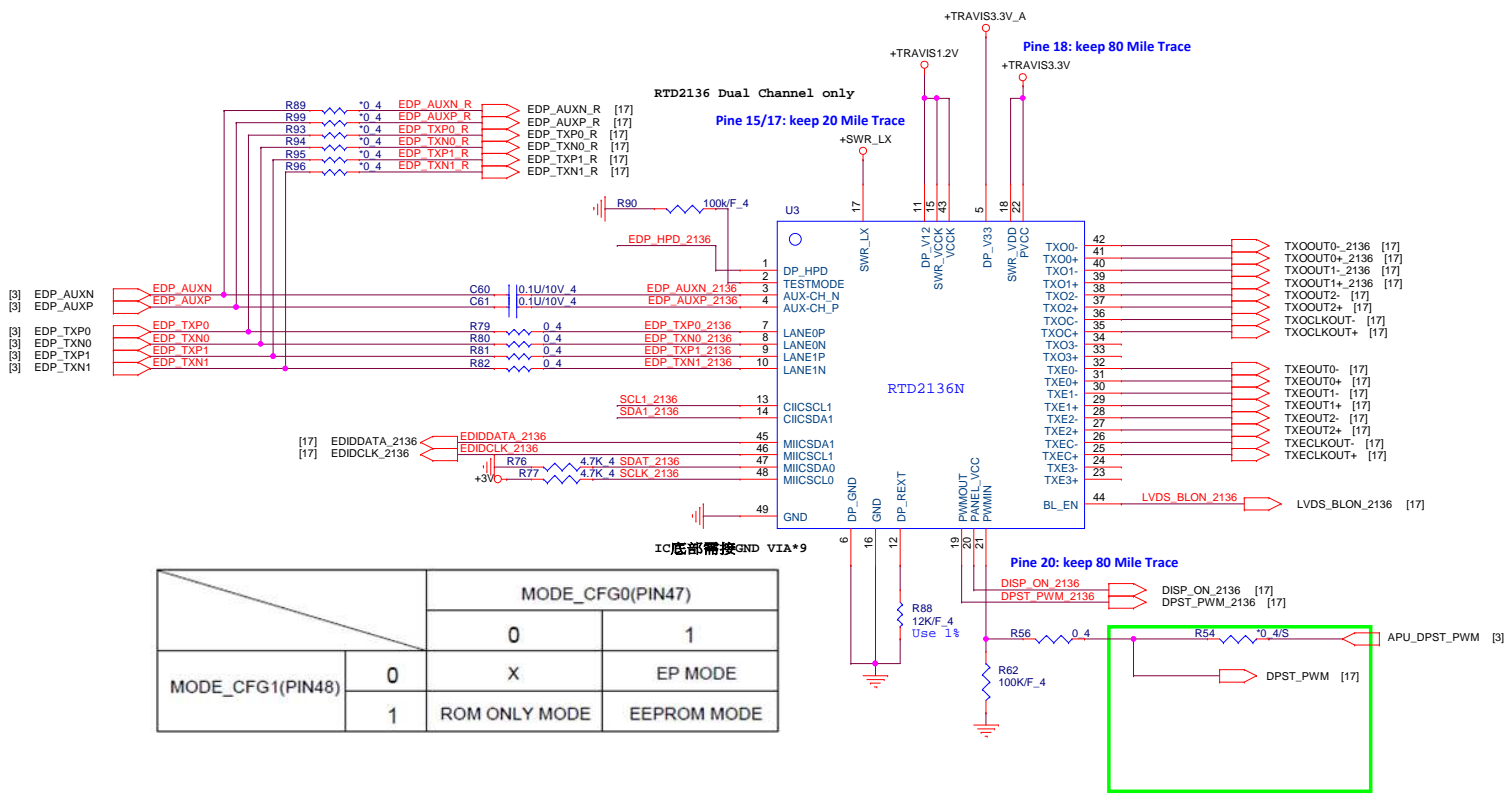
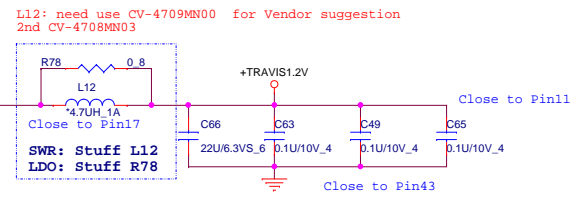
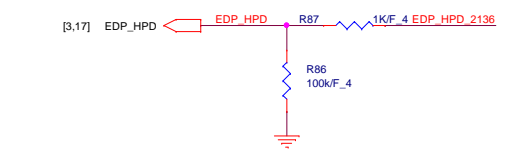
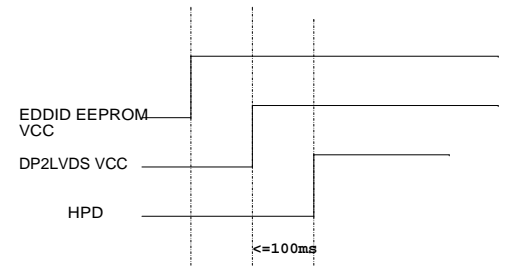
This basic topology should be used for DRAM_RST for DDR3/GDDR5. These Capacitors and Resistor values are an example only. The Series R and || Cap values will depend on the DRAM load and will have to be calculated for different Memory ,DRAM Load and board to pass Reset Signal Spec.



PROJECT : Y22A
Quanta Computer Inc.

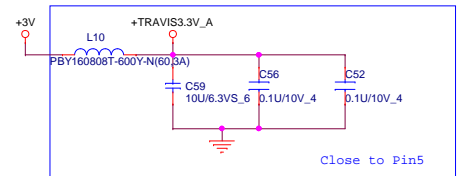
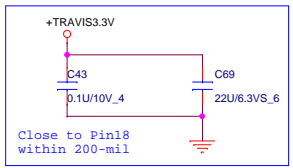
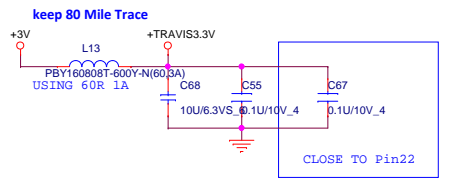
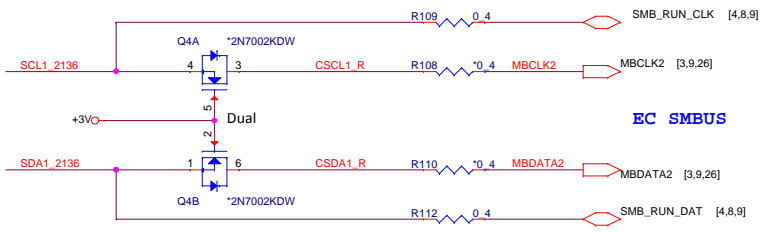
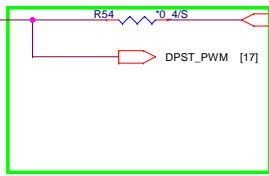
Size	Document Number	Rev
	TPOAZ_S3_MEM_Interface	1A
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RTD2136S Power Up Sequence



IC底部需接GND VIA*9

		MODE_CFG0(PIN47)	
		0	1
MODE_CFG1(PIN48)	0	X	EP MODE
	1	ROM ONLY MODE	EEPROM MODE

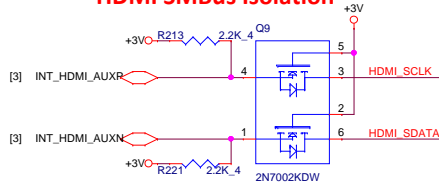


[3,4,5,6,8,9,17,18,19,20,21,22,23,24,25,26,31,33] +3V
[19,25,33] +1.5V

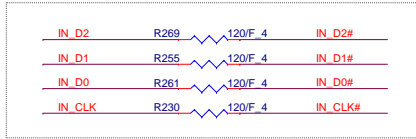
PROJECT : Y22A
Quanta Computer Inc.

Size Custom	Document Number LVDS converter RTD2136	Rev 1A
Date: Wednesday, March 19, 2014 Sheet 16 of 36		

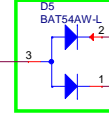
HDMI SMBus Isolation



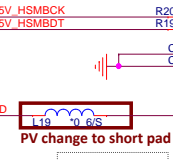
Close to HDMI connector



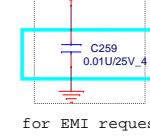
SI for down size



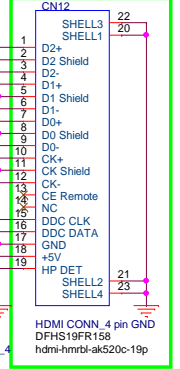
PV change to short pad



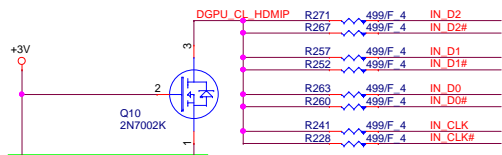
for EMI request



SI for change footprint & P/N

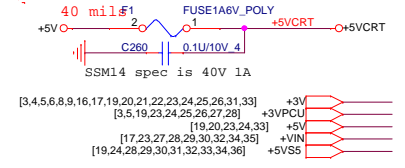
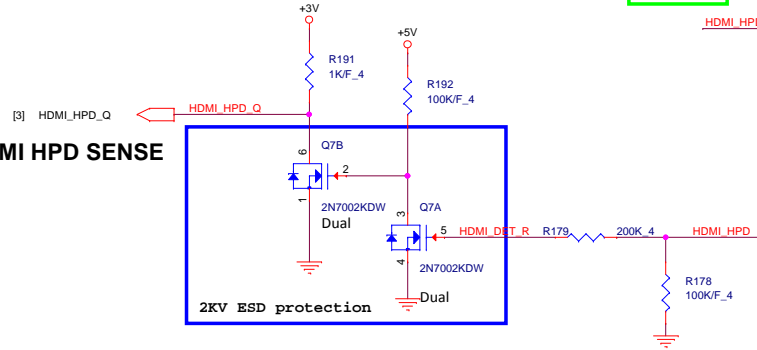


Check list recommend 604 ohm



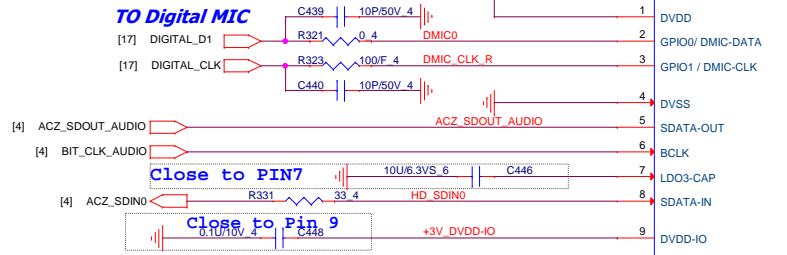
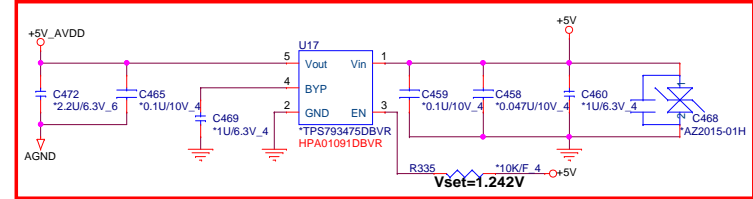
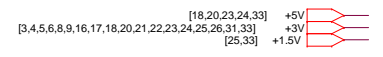
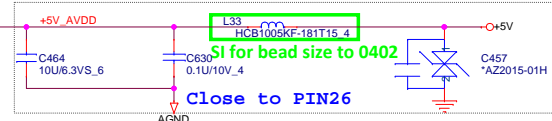
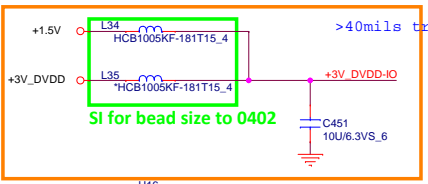
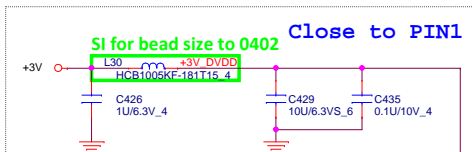
SI change to DNI

HDMI HPD SENSE



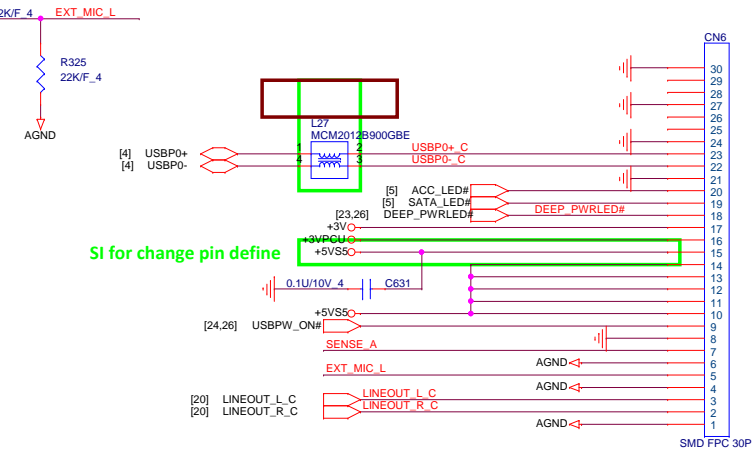
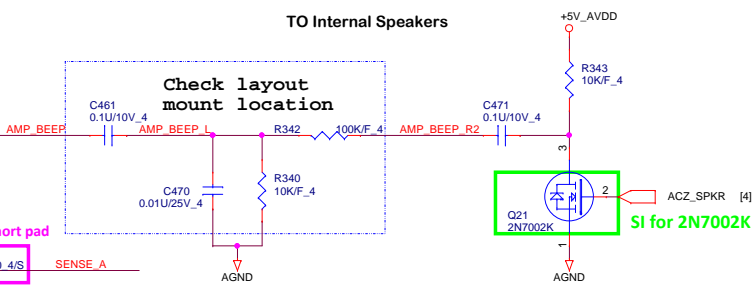
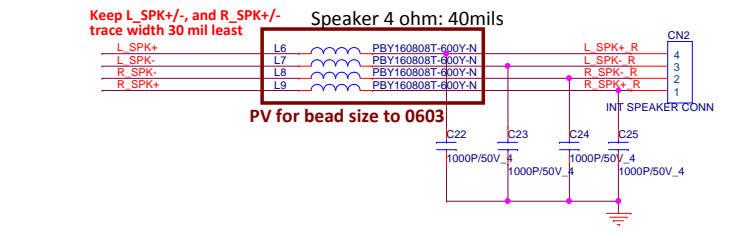
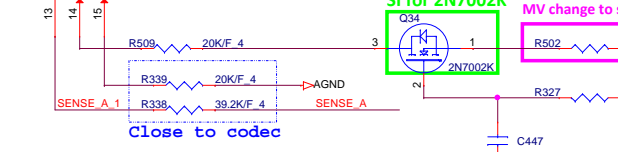
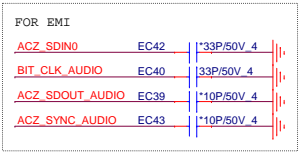
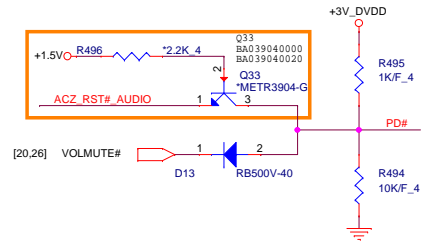
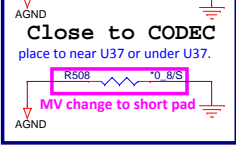
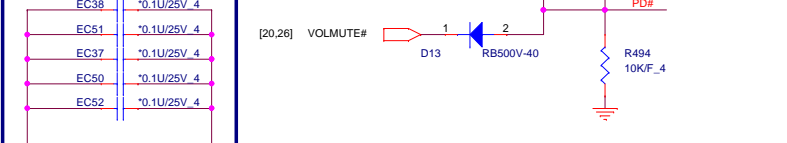
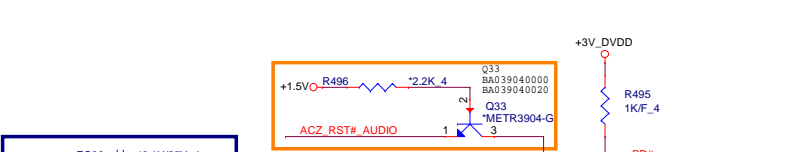
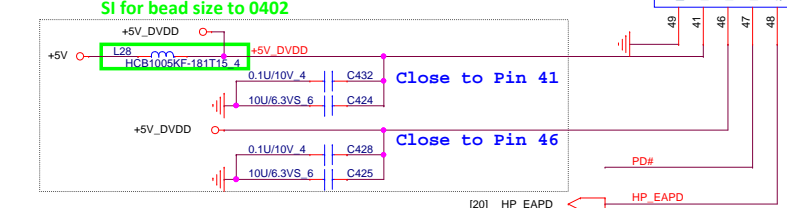
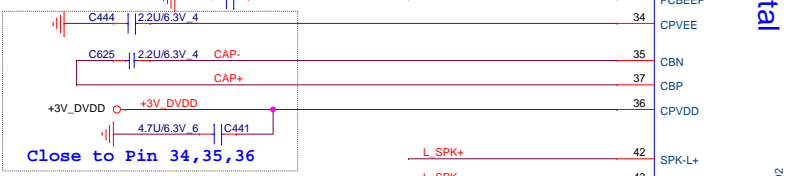
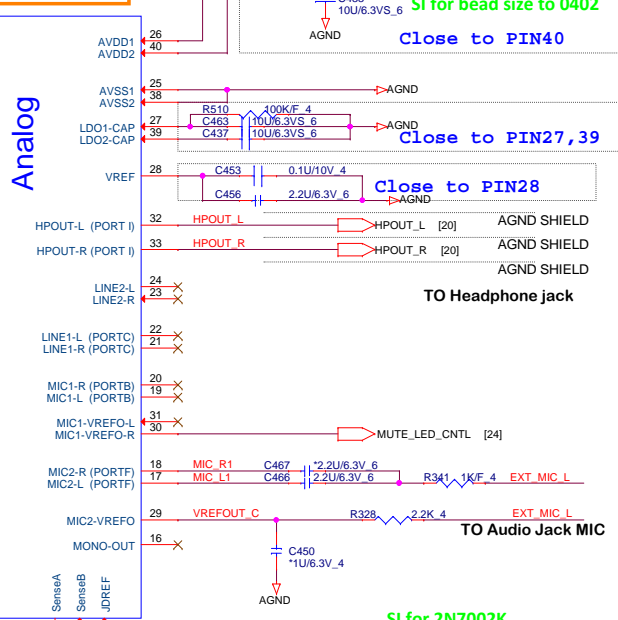
[3,4,5,6,8,9,16,17,19,20,21,22,23,24,25,26,31,33] +3V
 [3,5,19,23,24,25,26,27,28] +3VPCU
 [18,20,23,24,33] +5V
 [17,23,27,28,29,30,32,34,35] +VIN
 [19,24,28,29,30,31,32,33,34,36] +5VS5

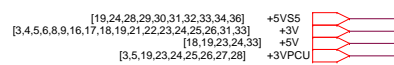
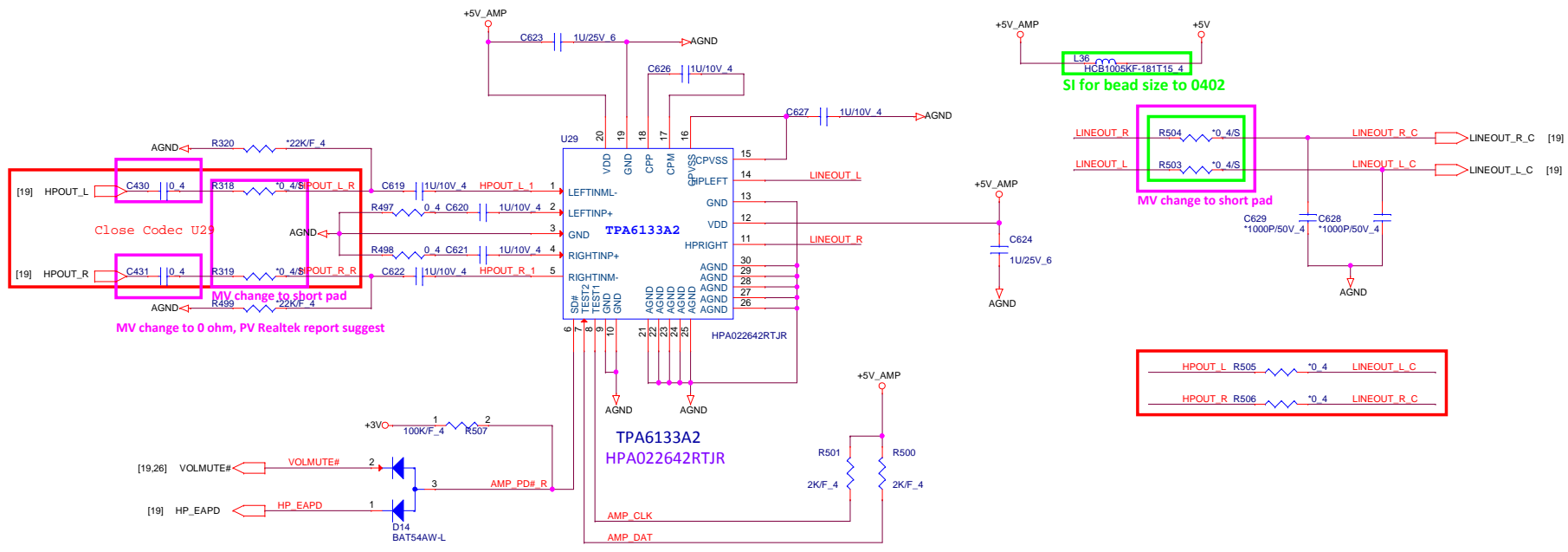
	PROJECT : Y22A		Rev 1A
	Quanta Computer Inc.		
	Size Custom	Document Number LCD Connector (LVDS)	
Date: Wednesday, March 19, 2014		Sheet 18 of 36	



Analog

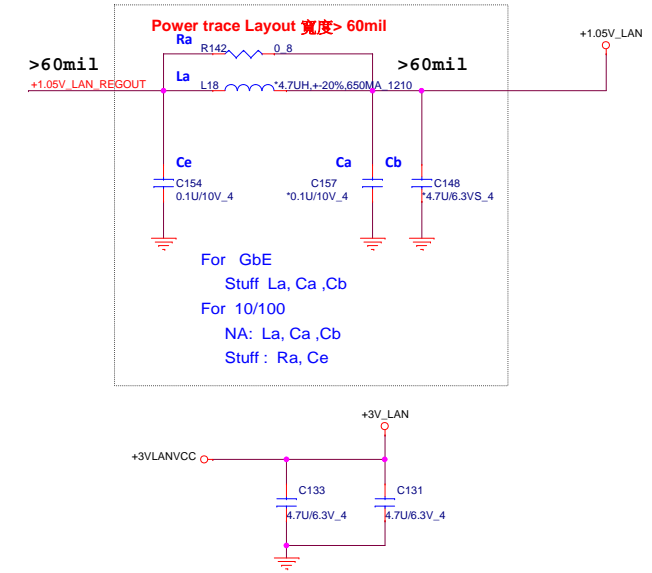
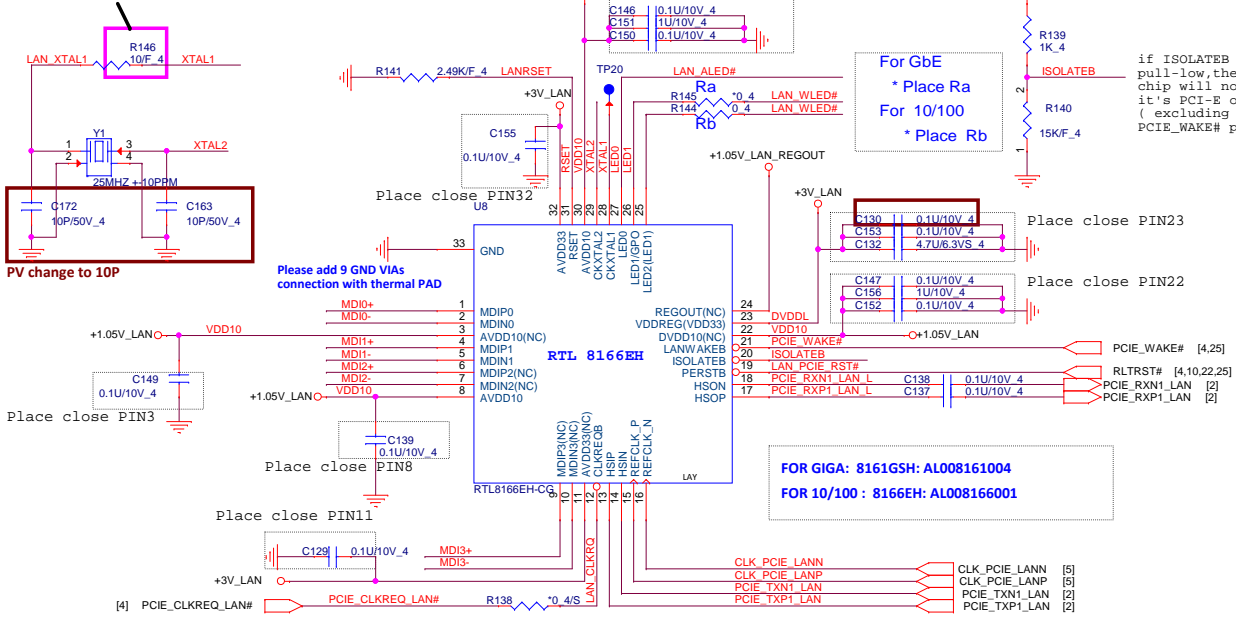
Digital



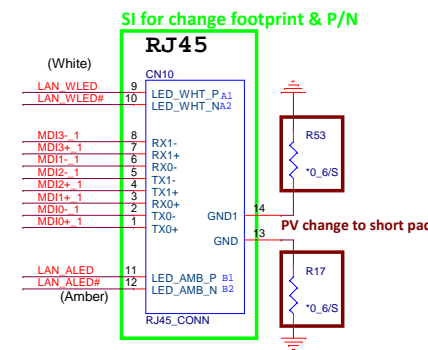
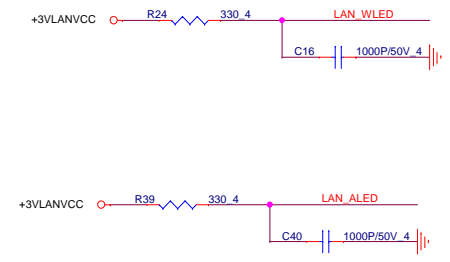
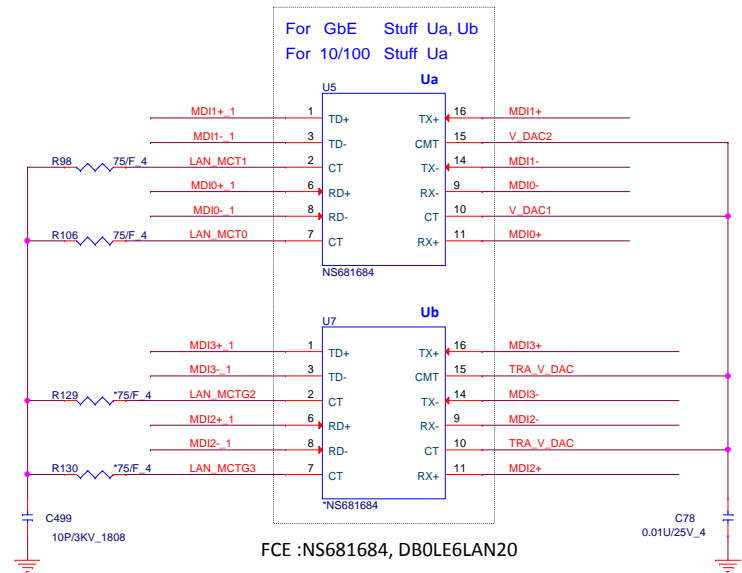


	PROJECT : Y22A Quanta Computer Inc.		
	Size Custom	Document Number AMP TPA6130A2	Rev 1A
	Date: Monday, March 24, 2014		Sheet 20 of 36

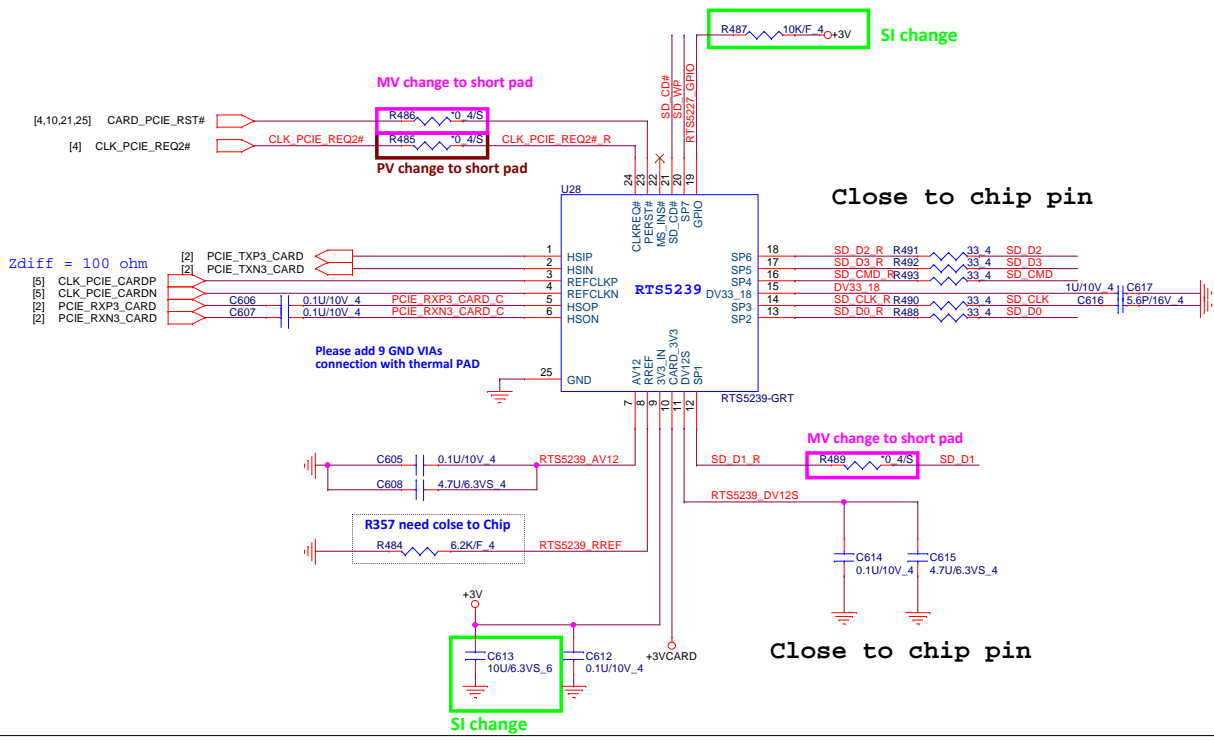
For EMI 0 ~ 22 ohm



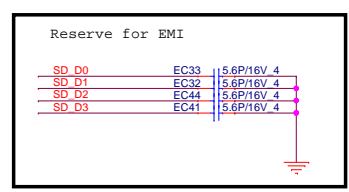
LAN conn



	PROJECT : Y22A	
	Quanta Computer Inc.	
	Size Custom	Document Number RTL 8166EH/8161EHRJ45
Date: Monday, March 24, 2014	Sheet 21	of 36

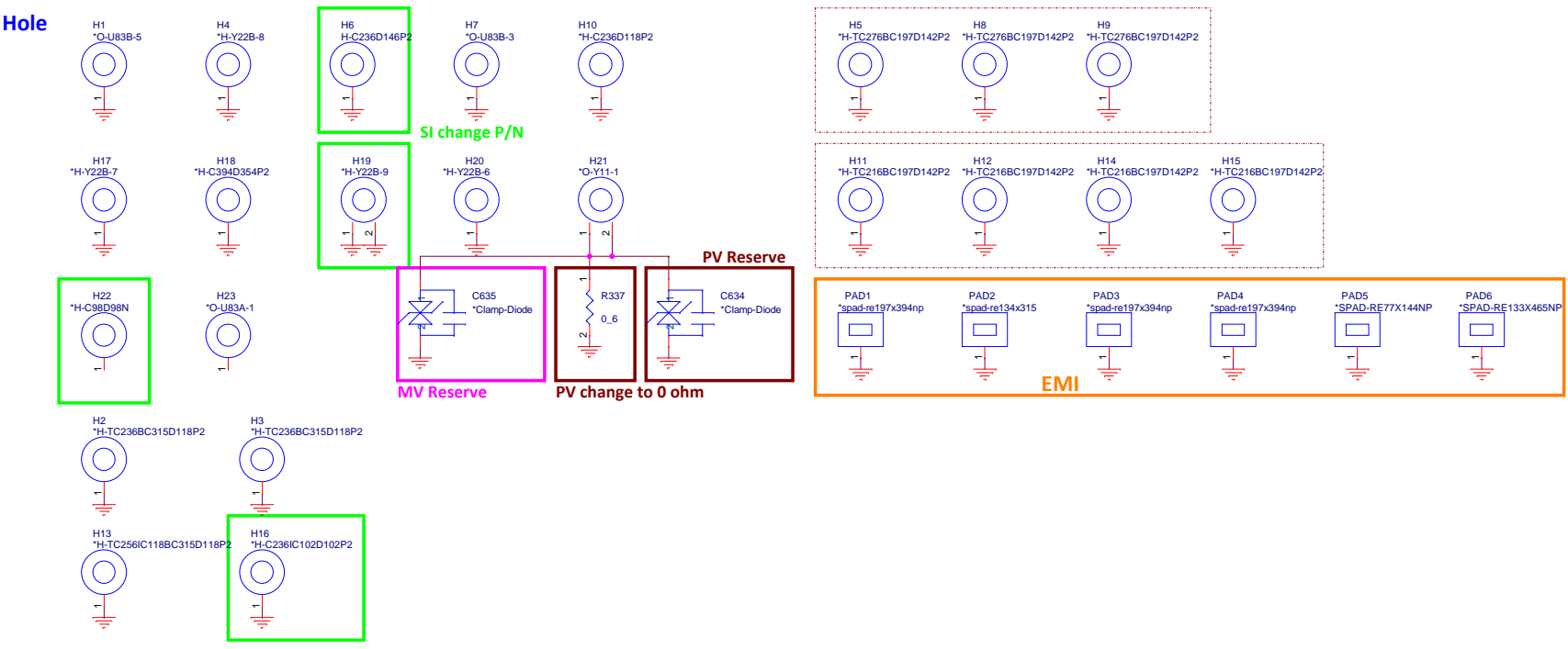
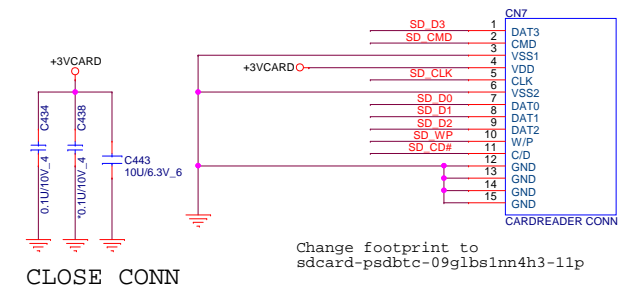


SP1	SD_D1	MS_D1
SP2	SD_D0	MS_D1
SP3	SD_CLK	MS_D0
SP4	SD_CMD	MS_D2
SP5	SD_D3	MS_D3
SP6	SD_D2	MS_CLK
SP7	SD_WP	MS_BS



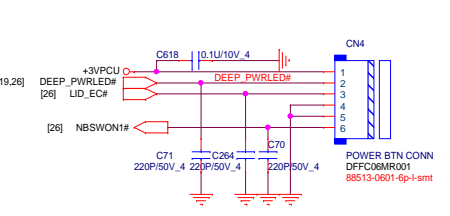
Share Pin

CARD READER

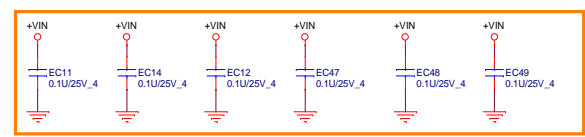
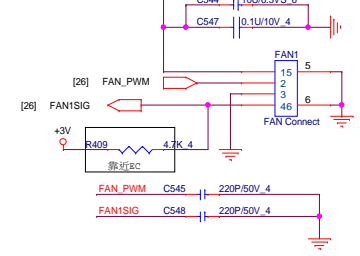


	PROJECT : Y22A		Rev 1A
	Quanta Computer Inc.		
	Size Custom	Document Number	
Date: Monday, March 24, 2014		Sheet 22 of 36	

Power Button Connector



CPU FAN

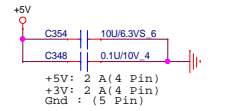
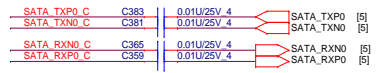
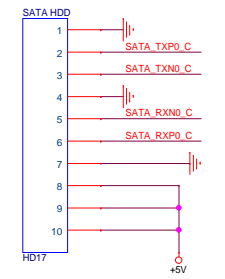


FOR EMI

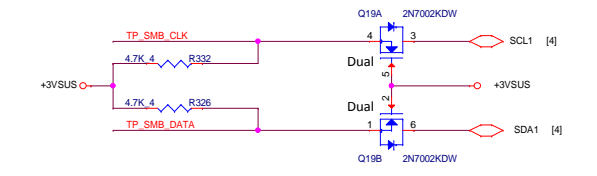
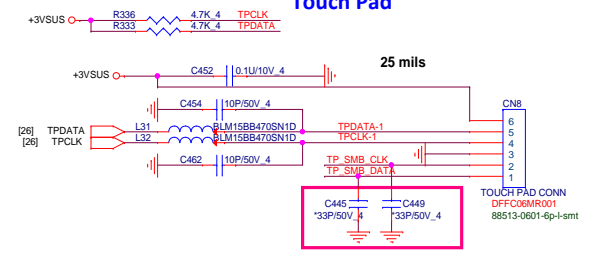
[17,27,28,29,30,32,34,35]



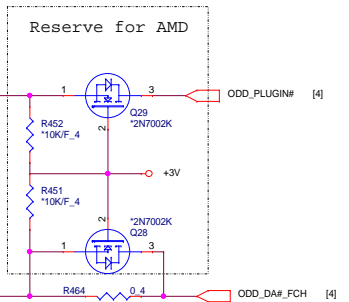
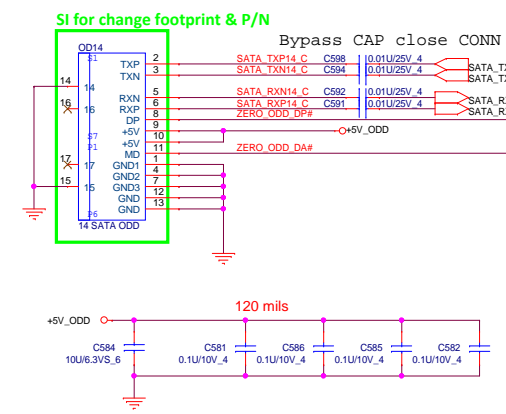
SATA HDD Connector(Cable type)



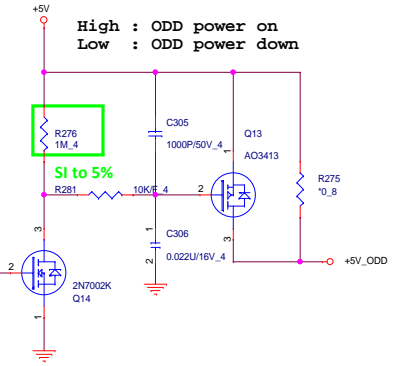
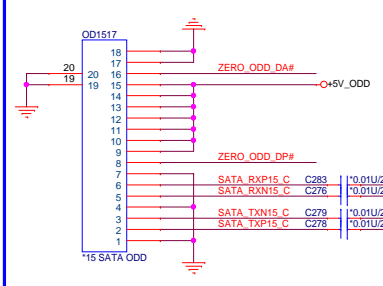
Touch Pad



SATA ODD CONNECTOR



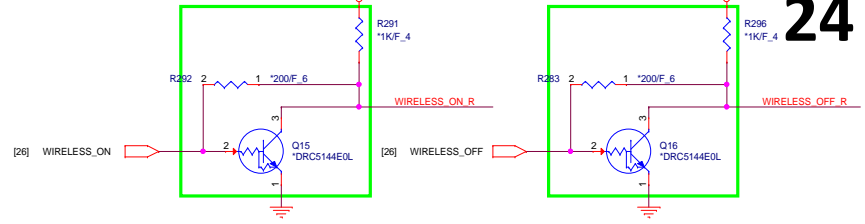
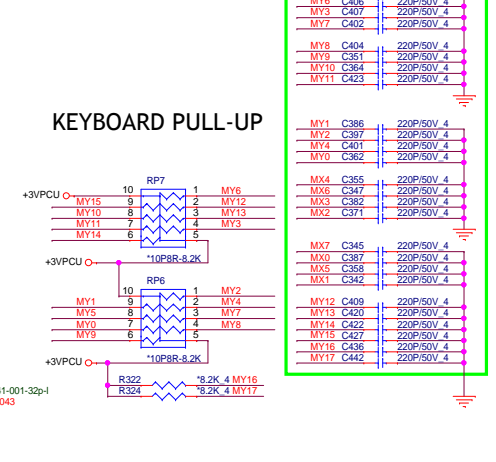
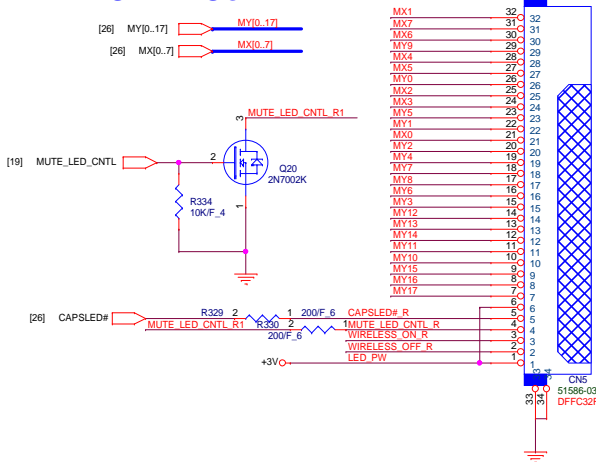
15" & 17" SATA ODD



PROJECT : Y22A
Quanta Computer Inc.

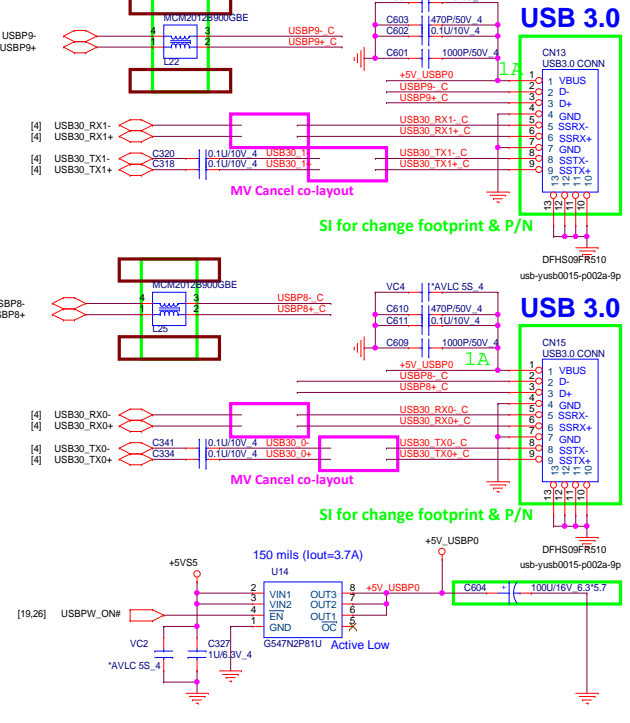
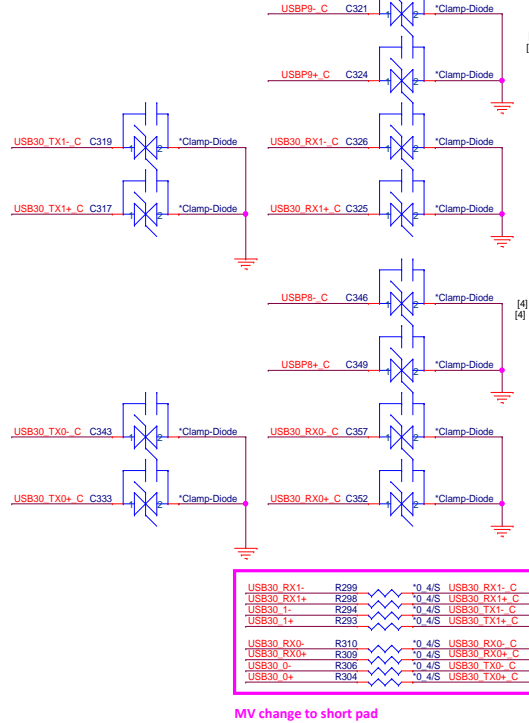
NB5	Size Custom	Document Number	Rev 1A
	HDD/ODD/TP/FAN/HOLE/LID		
Date: Monday, March 24, 2014		Sheet 23 of 36	

KEYBOARD

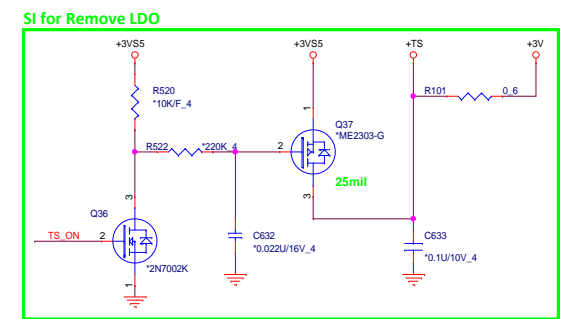
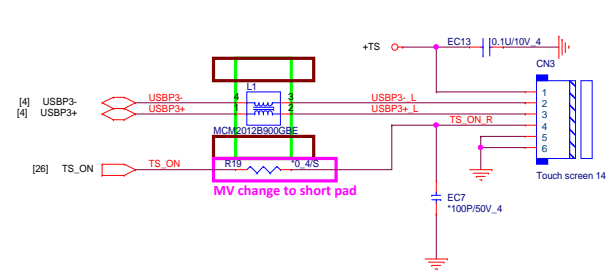


24

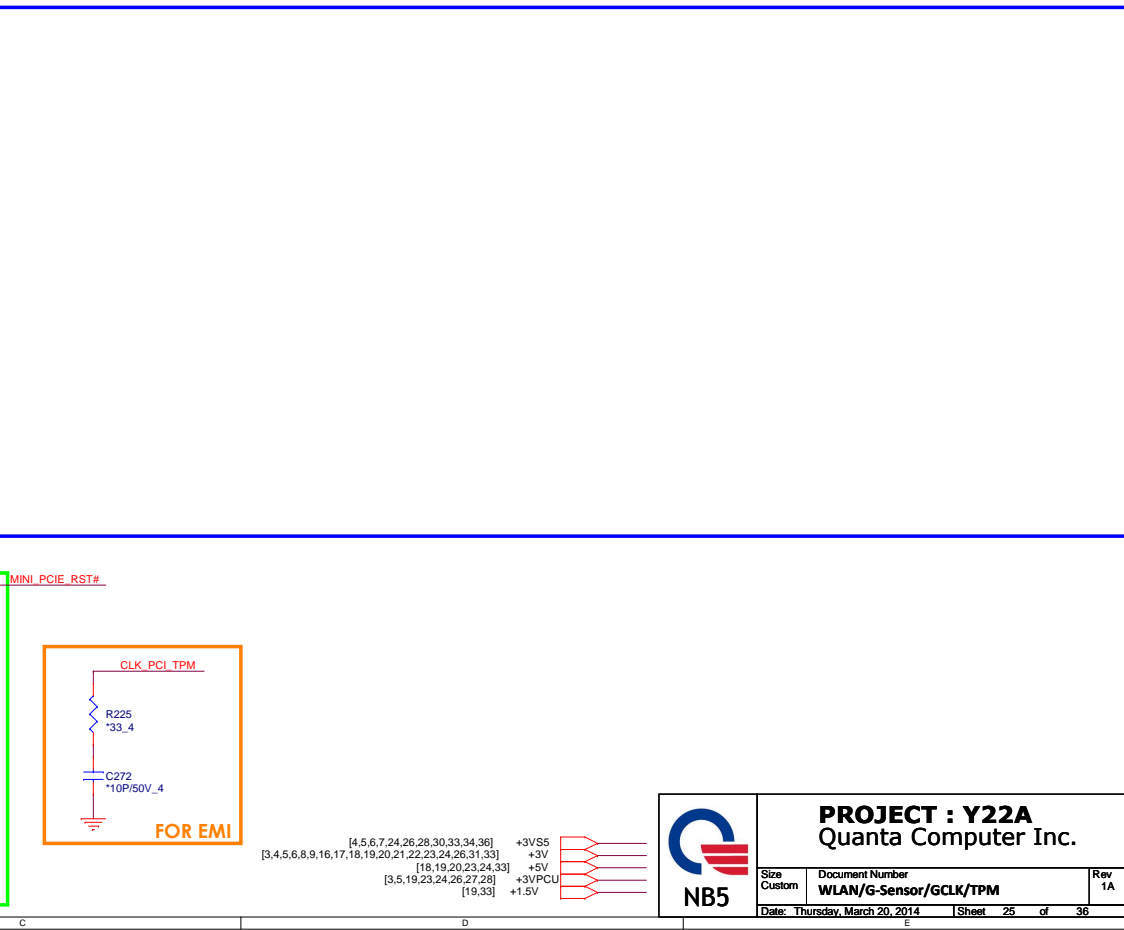
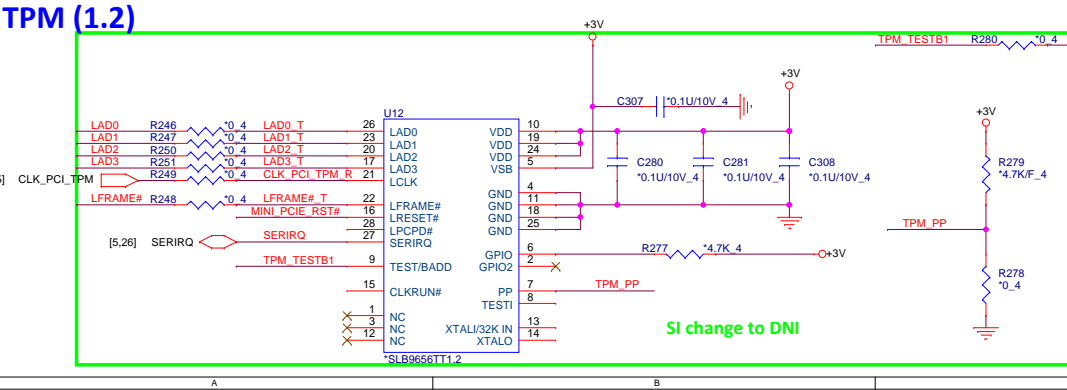
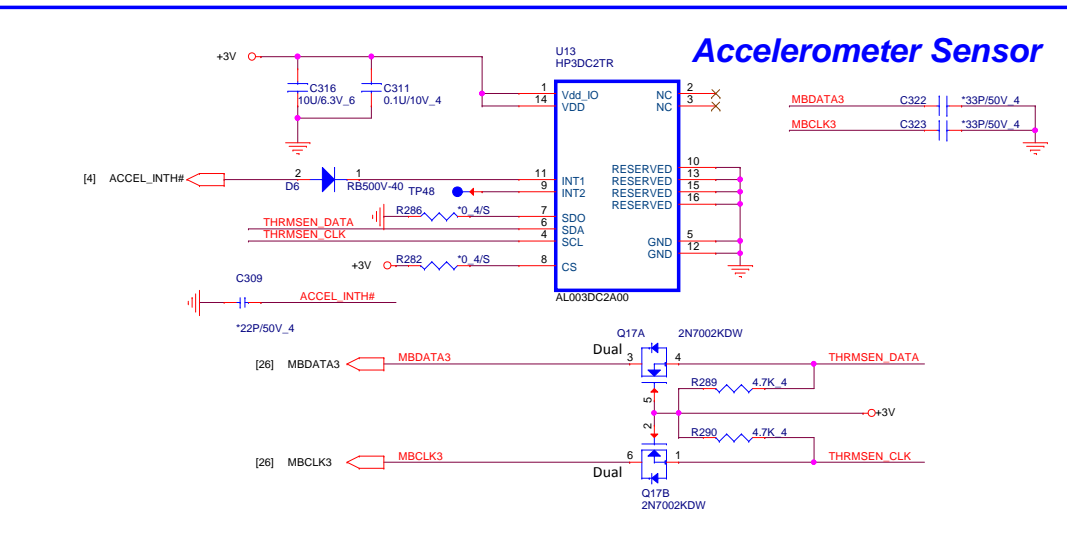
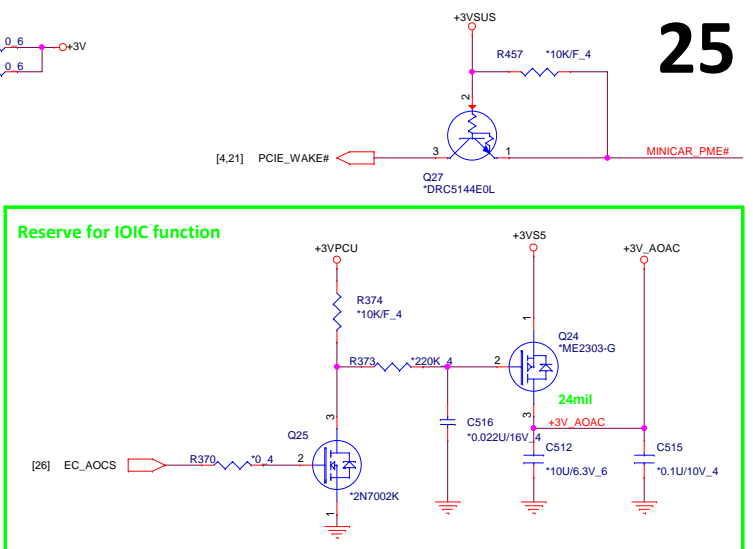
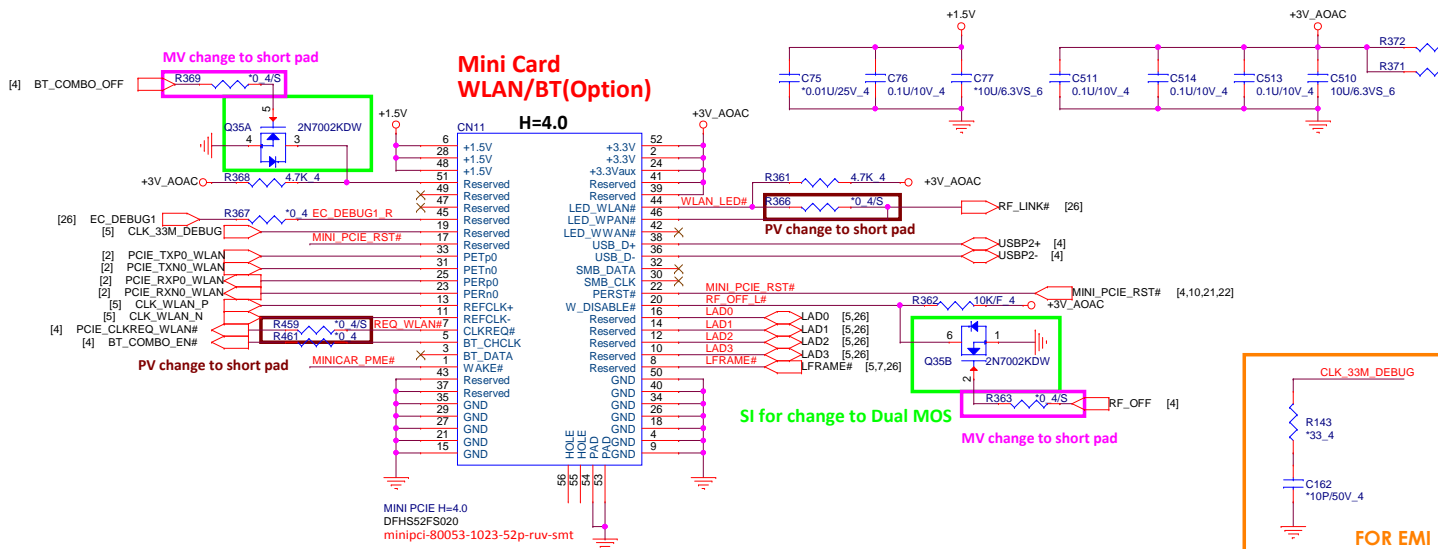
USB 2.0/3.0 Combo



Touch screen



[19,28,29,30,31,32,33,34,36] +5VSS
[3,5,19,23,25,26,27,28] +3VPCU

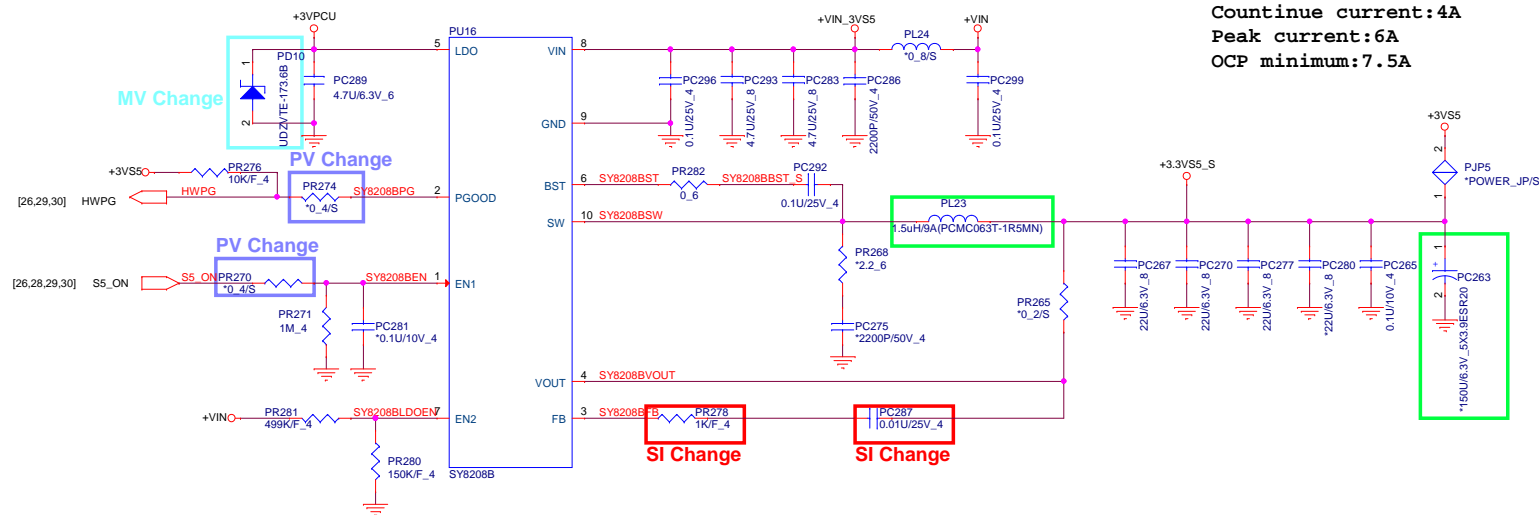


PROJECT : Y22A
Quanta Computer Inc.

Size Custom Document Number [4,5,6,7,24,26,28,30,33,34,36] +3VS5
[3,4,5,6,8,9,16,17,18,19,20,21,22,23,24,26,31,33] +3V
[18,19,20,23,24,33] +5V
[3,5,19,23,24,26,27,28] +3VPCU
[19,33] +1.5V

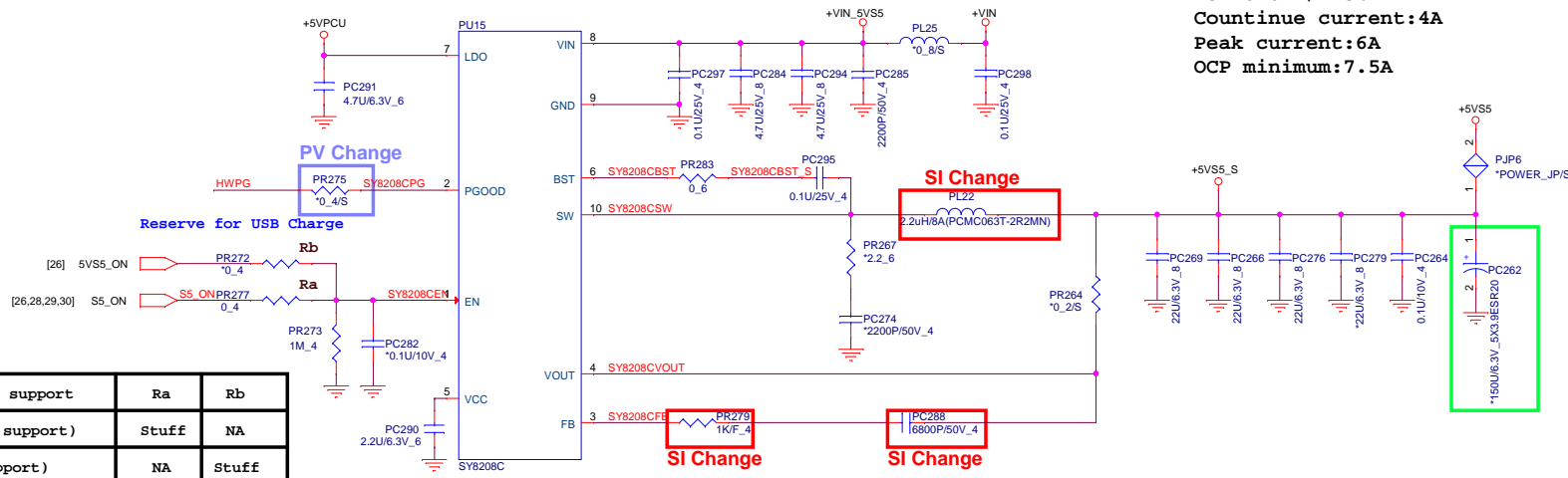
NBS

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+3.3 Volt +/- 5%
 Countinue current:4A
 Peak current:6A
 OCP minimum:7.5A

+3VSS [4,5,6,7,24,25,26,30,33,34,36]
 +5VSS [19,24,29,30,31,32,33,34,36]

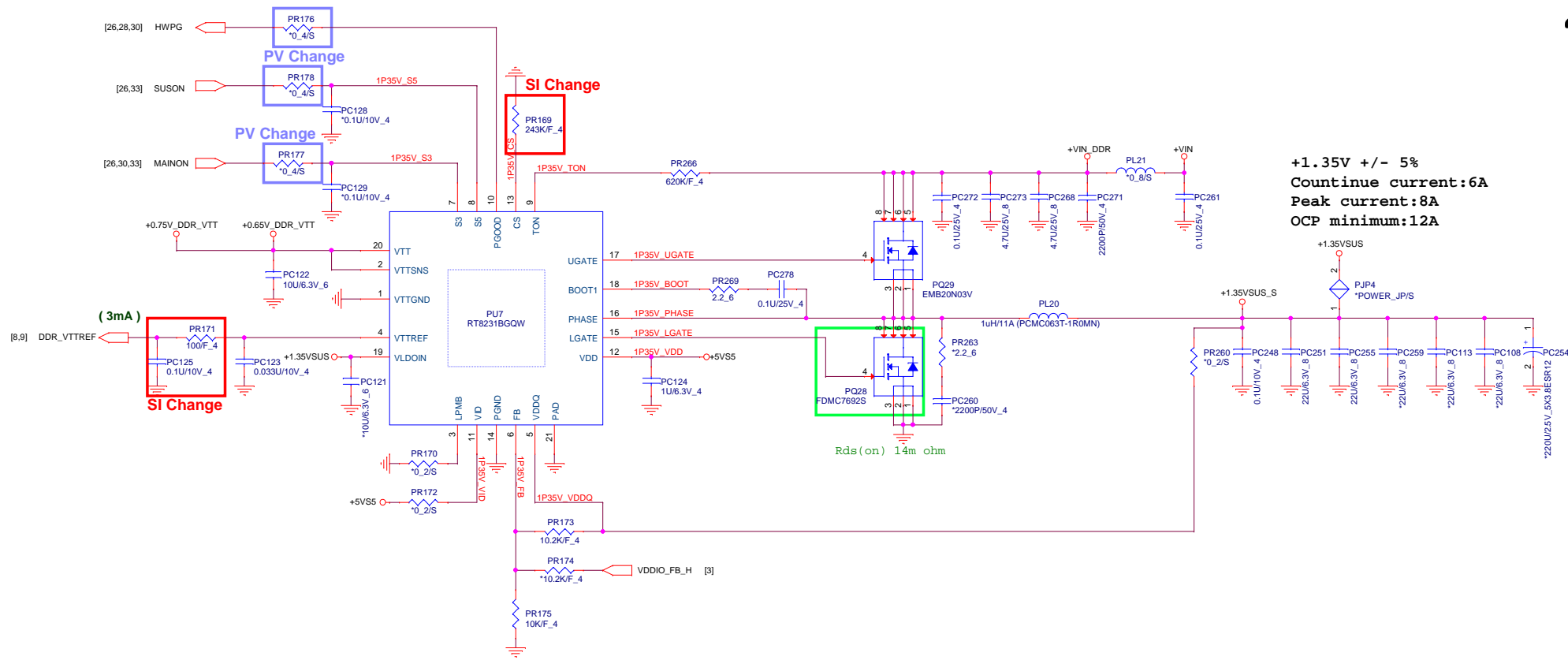


+5 Volt +/- 5%
 Countinue current:4A
 Peak current:6A
 OCP minimum:7.5A

USB Charge support	Ra	Rb
Vine (No support)	Stuff	NA
Envy (Support)	NA	Stuff

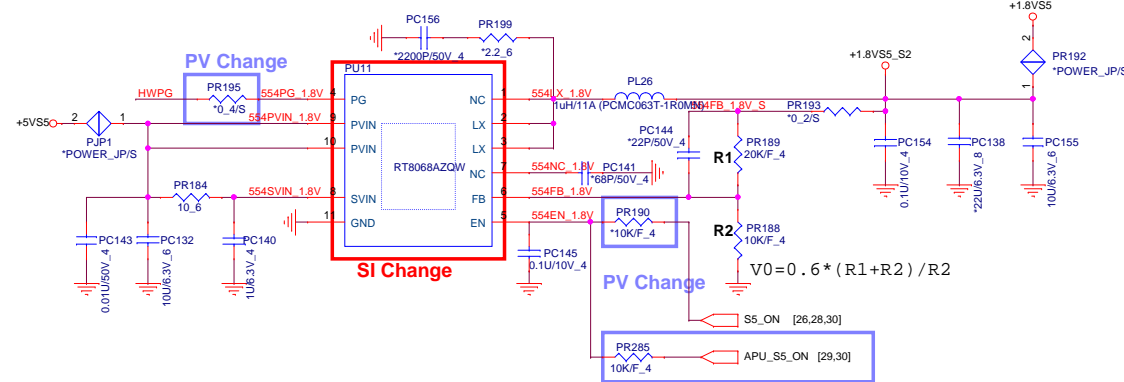
PROJECT : KAVERI
 Quanta Computer Inc.

Size Custom	Document Number 3/5VPCU(SY8208B/SY8208C)	Rev 1A
Date: Wednesday, March 19, 2014 Sheet 28 of 36		



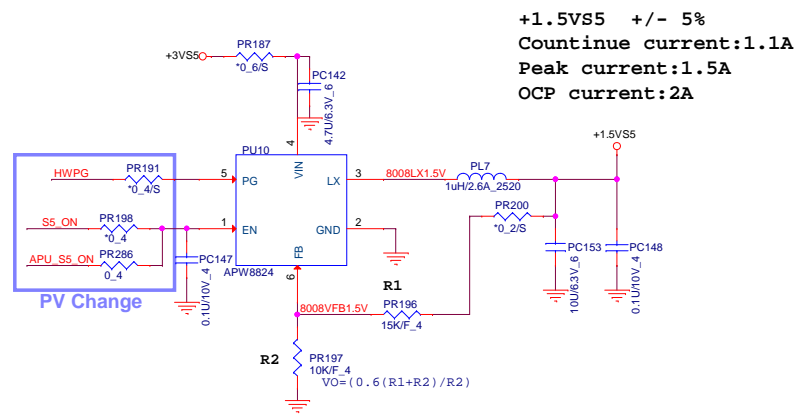
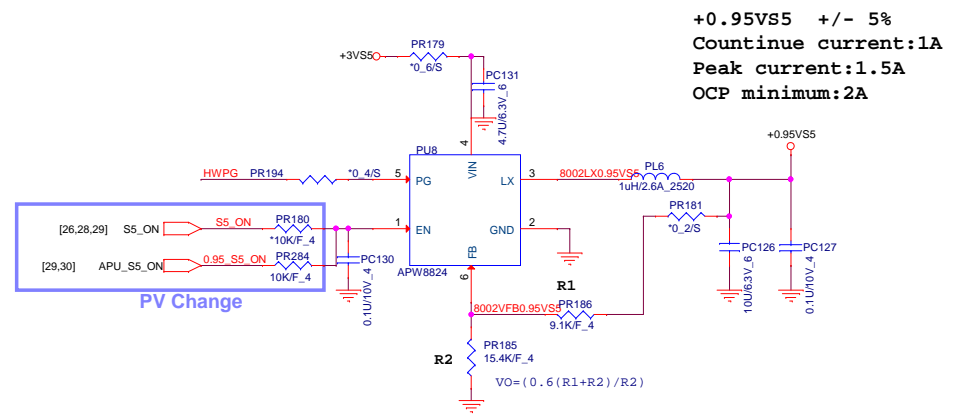
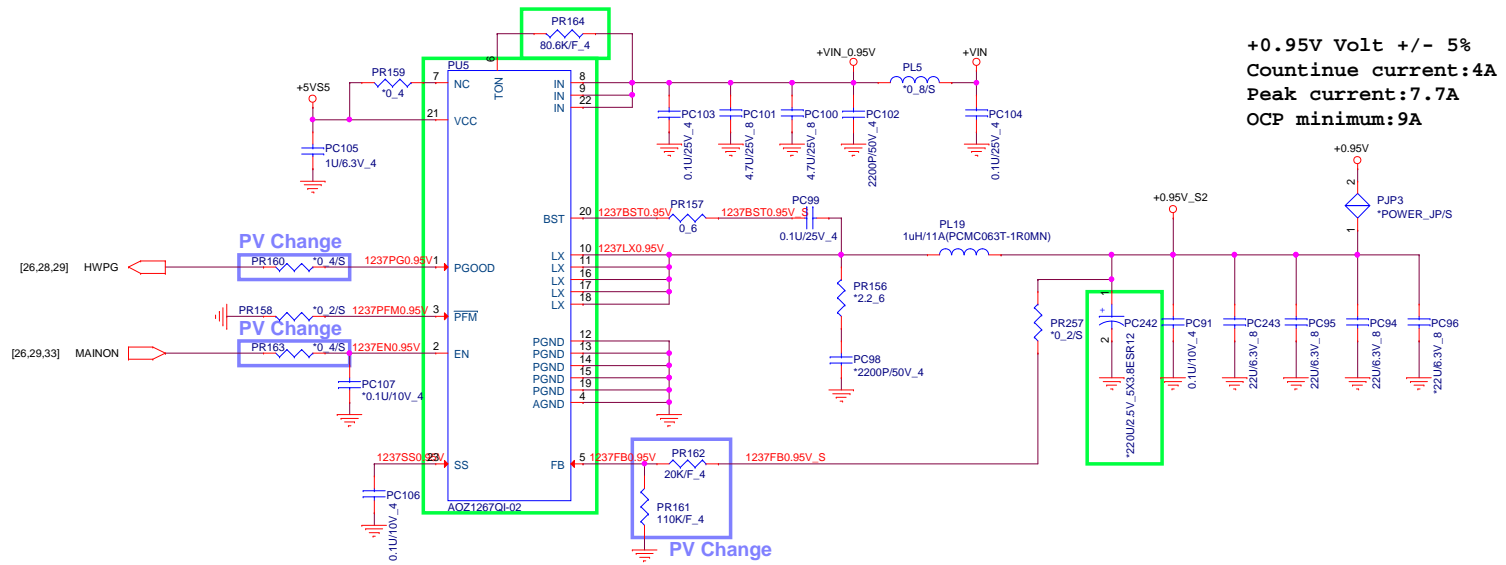
+1.35V +/- 5%
Countinue current:6A
Peak current:8A
OCP minimum:12A

1.8VS5 +/- 3%
Countinue current:2A
Peak current:3A
OCP minimum:4A

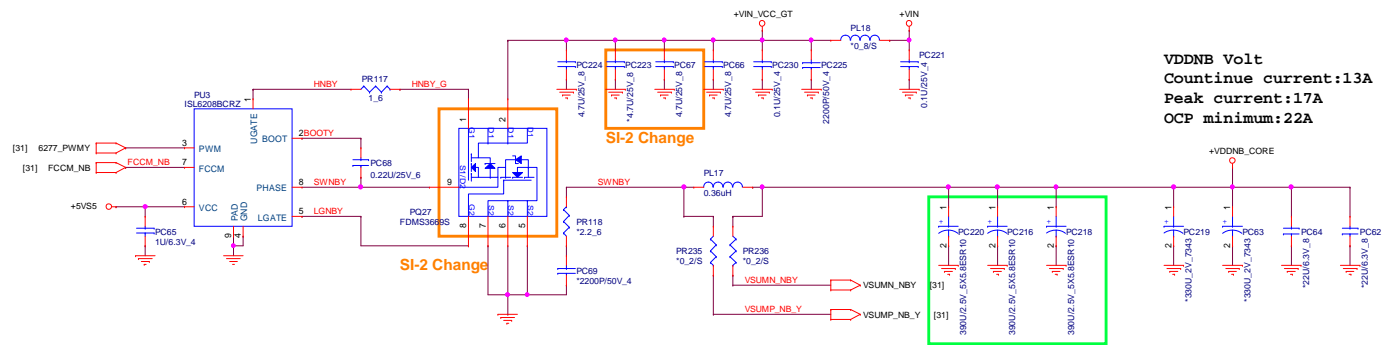
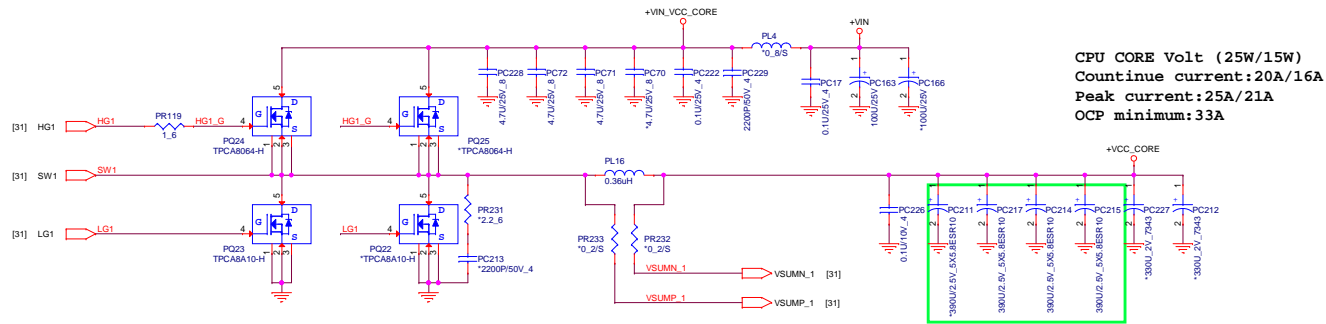


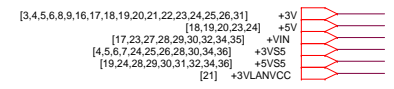
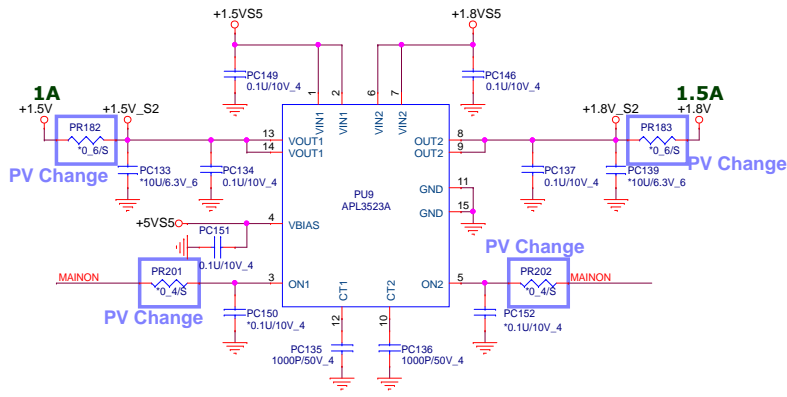
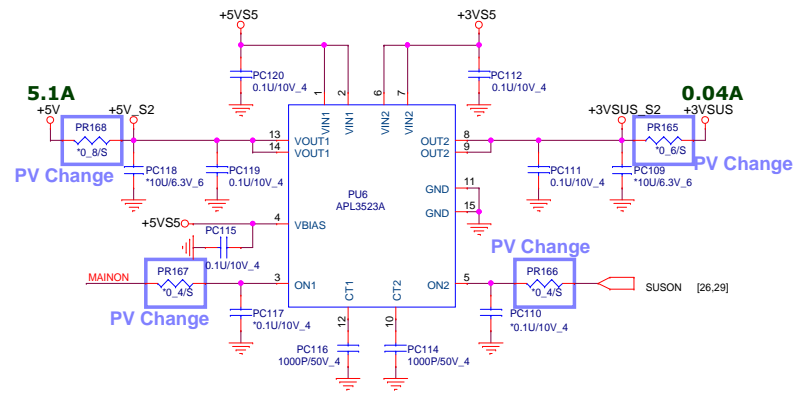
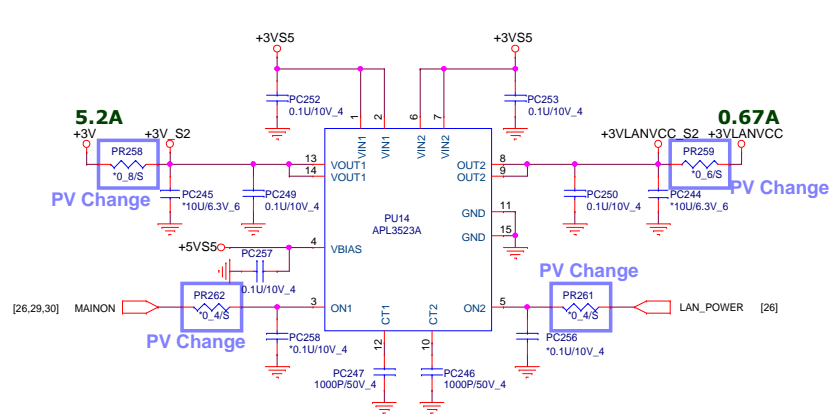
+1.35VSUS [2.6,8,9]

	PROJECT : Y22A	
	Quanta Computer Inc.	
	Size Custom Document Number DDR3 (RT8231A)/1.8VS5 Date: Wednesday, March 19, 2014	Rev 1A Sheet 29 of 36



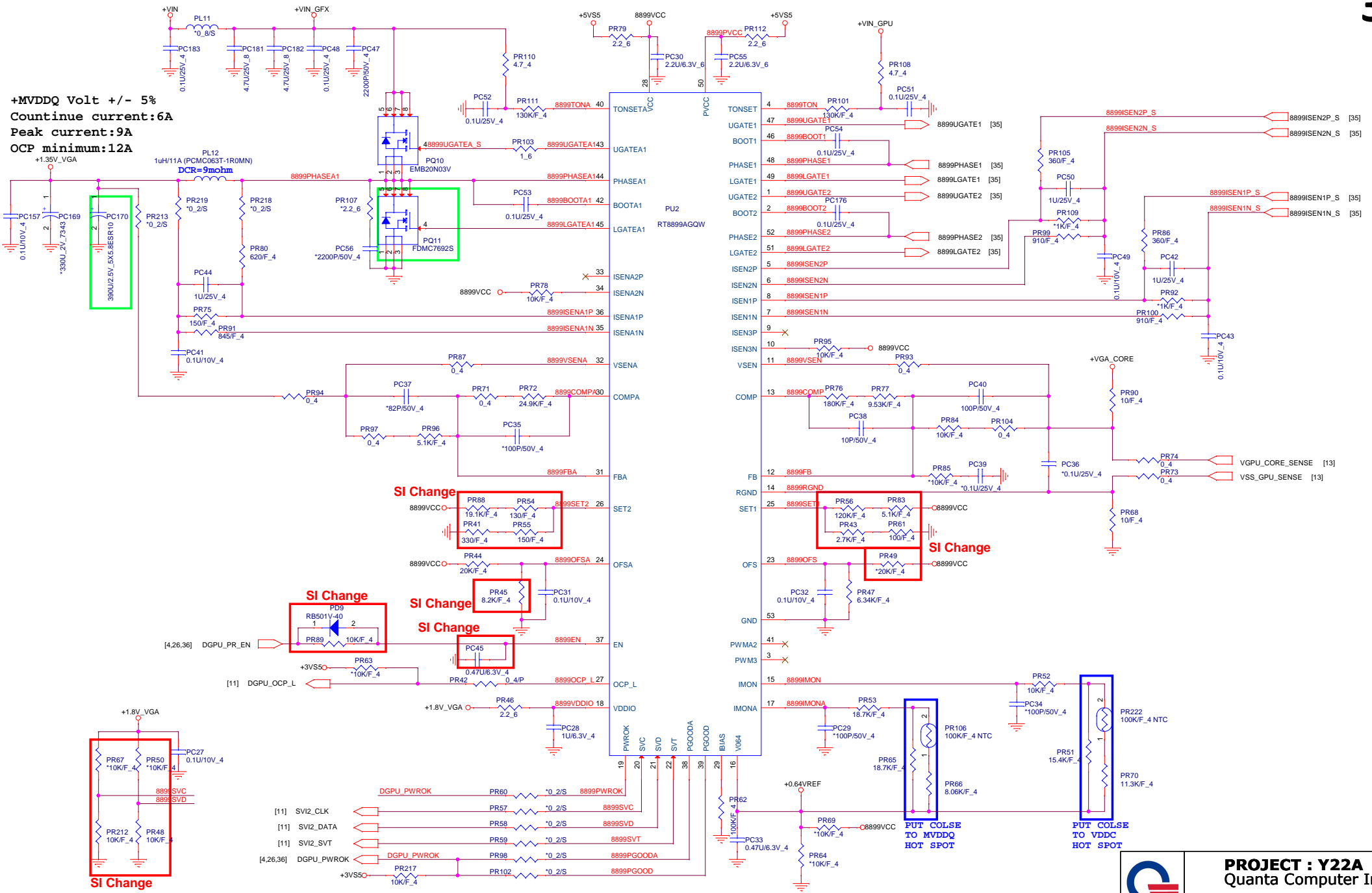
	PROJECT : Y22A	
	Quanta Computer Inc.	
	Size Custom Document Number +1.2V (RT8228)	Rev 1A
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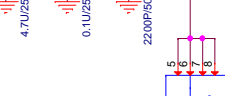
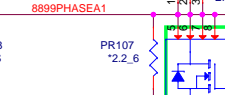
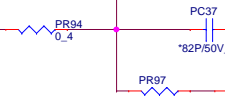
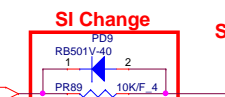
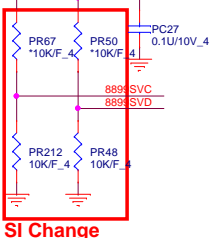


	PROJECT : Y22A Quanta Computer Inc.	
	Size Custom Document Number Dis-charge IC (SLG55448)	Rev 1A
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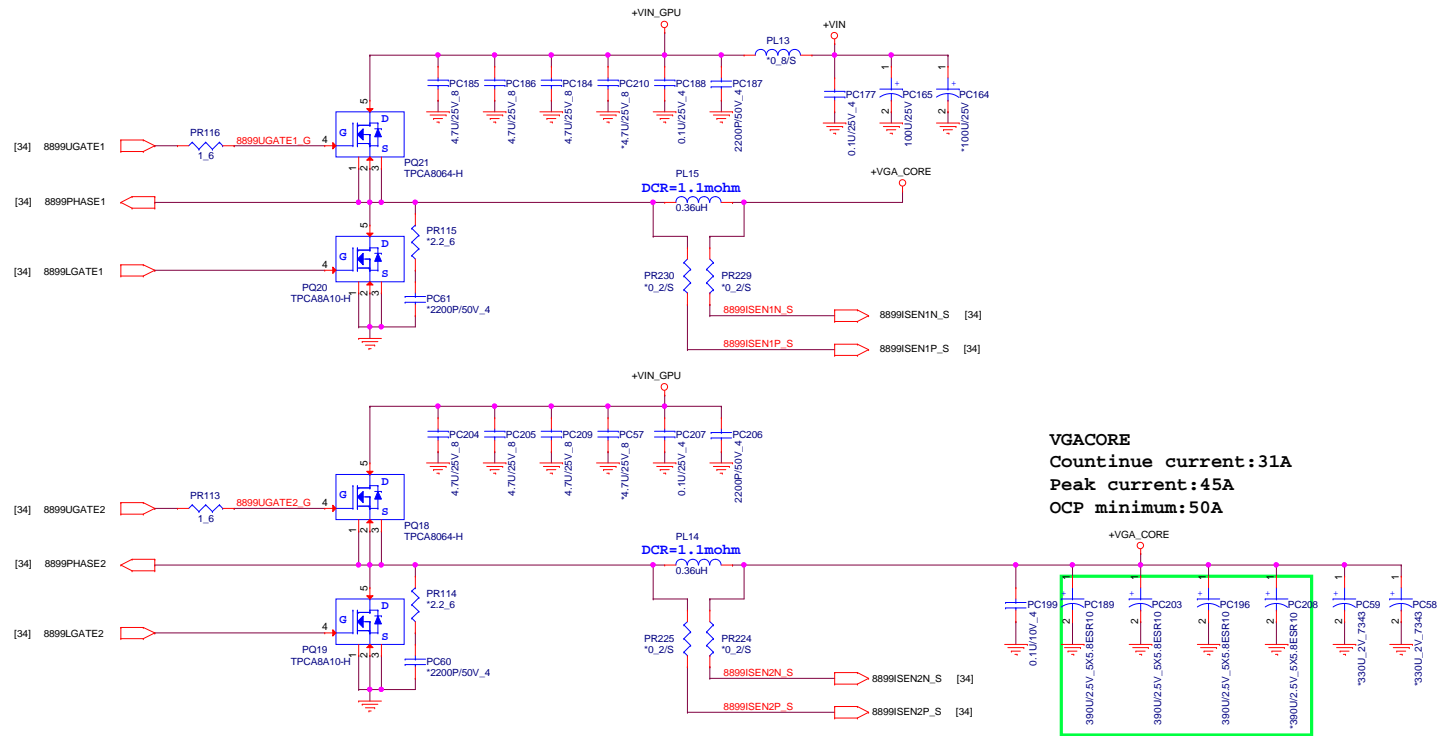
+MVDDQ Volt +/- 5%
Countinue current:6A
Peak current:9A
OCp minimum:12A



- [11] SVI2_CLK
- [11] SVI2_DATA
- [11] SVI2_SVT
- [4,26,36] DGPU_PWROK
- +3VS5



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