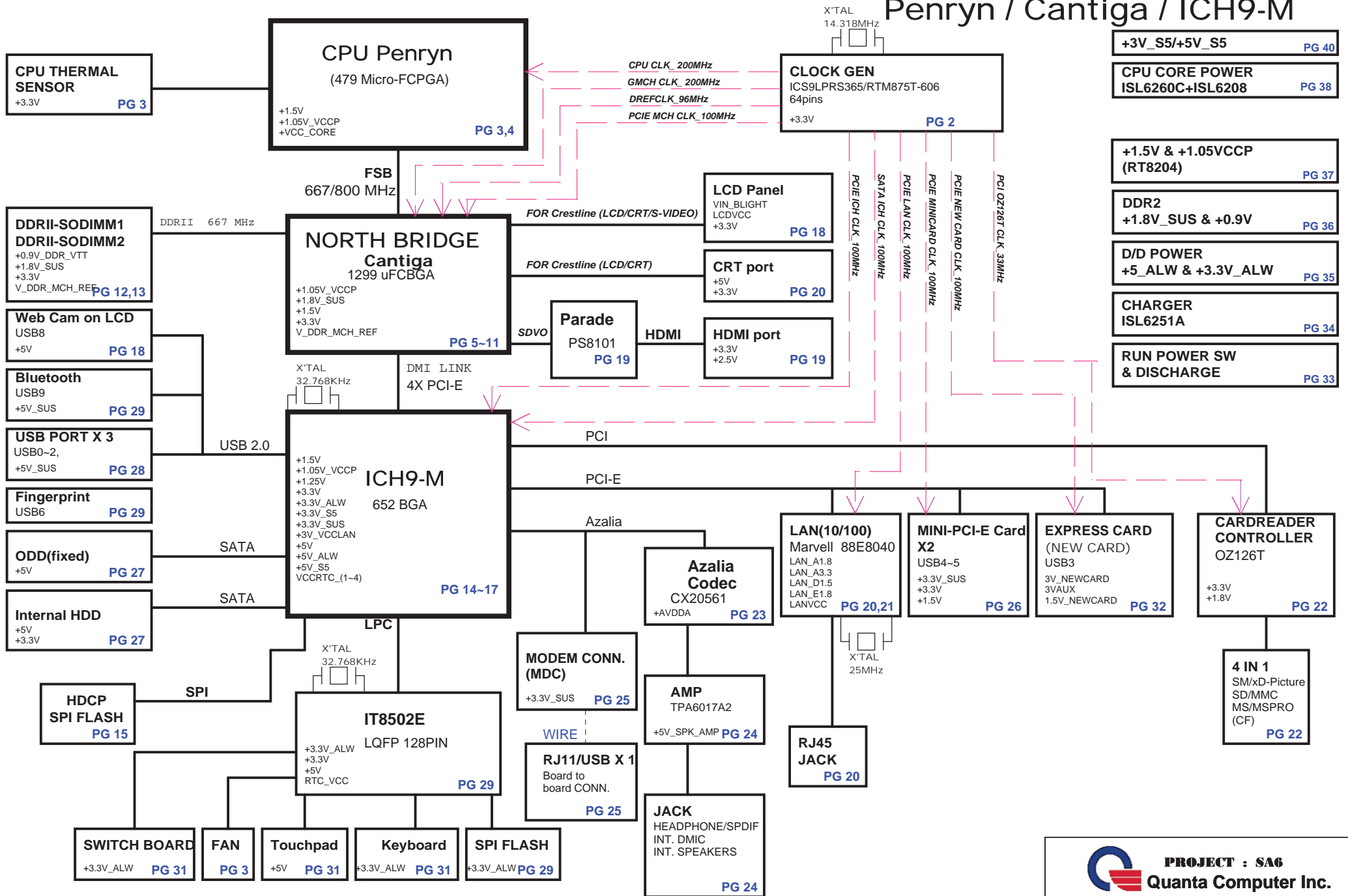
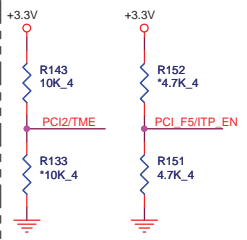
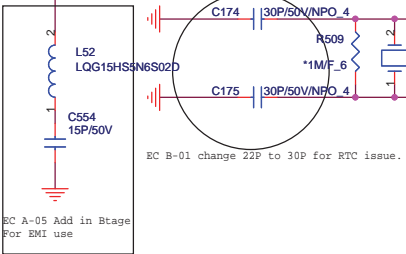
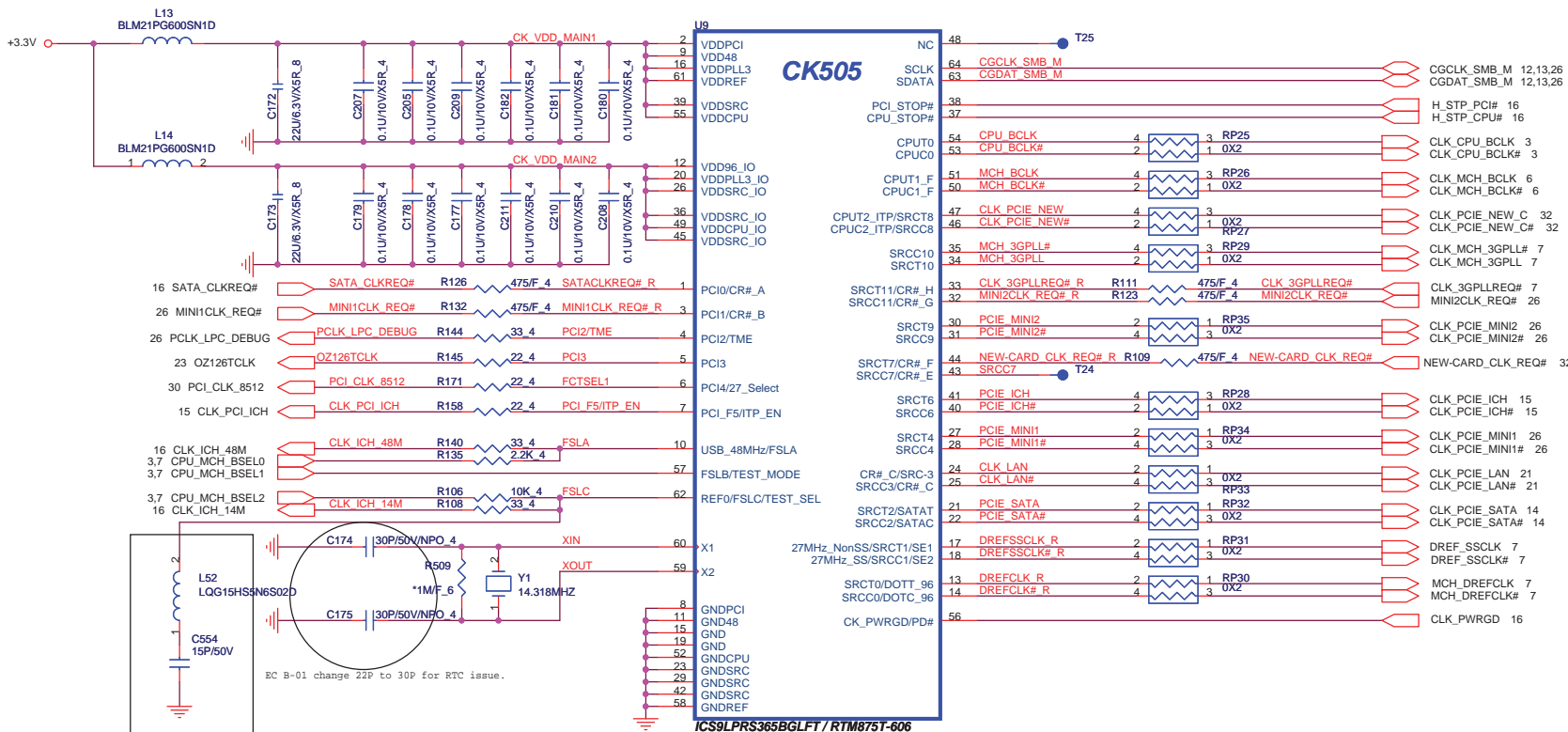


SA6 BLOCK DIAGRAM

Penryn / Cantiga / ICH9-M

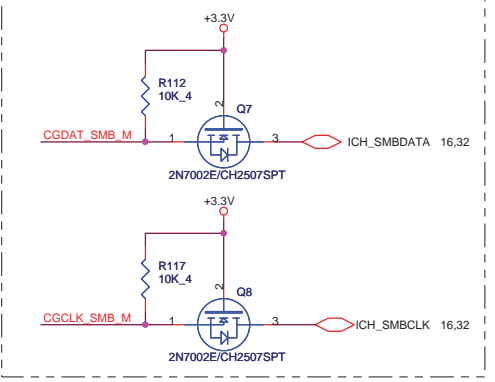
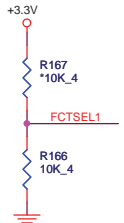




| | PULL HIGH | PULL LOW |
|---------------|---|-------------------------------------|
| PCI F5/ITP_EN | ITP/ITP# | SRC8/SRC8# |
| PCI2/TME | Overclocking of CPU and SRC not allowed | Overclocking of CPU and SRC allowed |

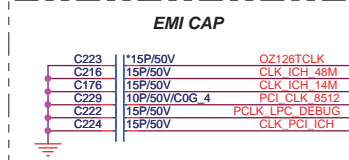
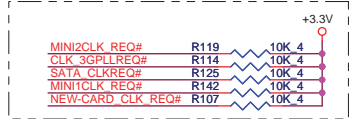
GCLK_SEL = FCTSEL1

| FCTSEL1 (PIN6) | PIN13 | PIN14 | PIN17 | PIN18 |
|------------------|-------|--------|----------------|-----------------|
| 0=UMA | DOT96 | DOT96# | SRC-1/LCDT_100 | SRC-1#/LCDT_100 |
| 1 = External VGA | SRC-0 | SRC-0# | 27Mout-NSS | 27Mout-SS |

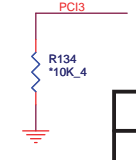


CPU Clock select

| FSC | FSB | FSA | CPU | SRC | PCI |
|-----|-----|-----|--------|-----|-----|
| 1 | 0 | 1 | 100.00 | 100 | 33 |
| 0 | 0 | 1 | 133.33 | 100 | 33 |
| 0 | 1 | 1 | 166.66 | 100 | 33 |
| 0 | 1 | 0 | 200.00 | 100 | 33 |
| 0 | 0 | 0 | 266.66 | 100 | 33 |
| 1 | 0 | 0 | 333.33 | 100 | 33 |
| 1 | 1 | 0 | 400.00 | 100 | 33 |
| 1 | 1 | 1 | 200.00 | 100 | 33 |



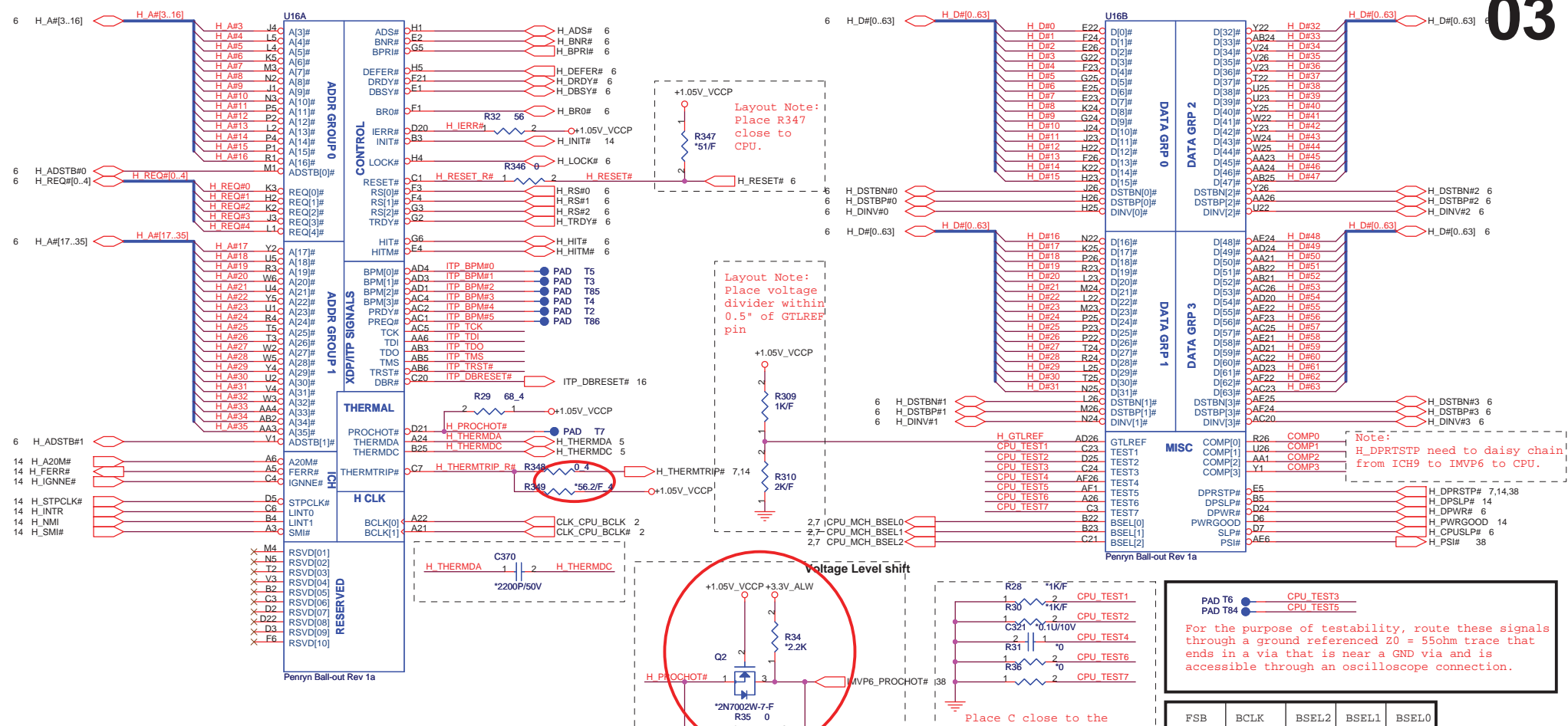
EC C-10/03 Change C229 to 10P and R171 to 22 ohm for meet Clock test.



| | PULL HIGH | PULL LOW |
|------|--|-------------------------------------|
| PCI3 | PIN37/38 is CPU_STOP/PCI_STOP PIN37/38 IS SRC5. | **SRC5_EN/PCI-3 (Internal Pull Low) |

PROJECT : SA6
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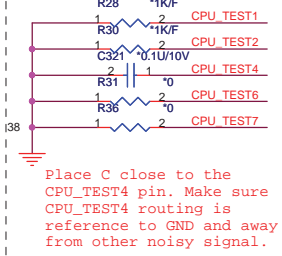
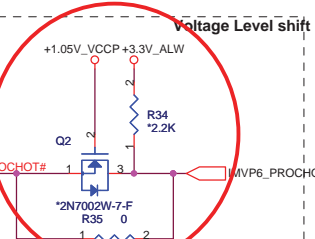
| | | |
|------------------------------|----------------------------------|---------------|
| Size: Custom | Document Number: CLOCK GENERATOR | Rev: 5B |
| Date: Friday, April 25, 2008 | | Sheet 2 of 41 |



Layout Note:
Place R347
close to
CPU.

Layout Note:
Place voltage
divider within
0.5" of GTLREF
pin

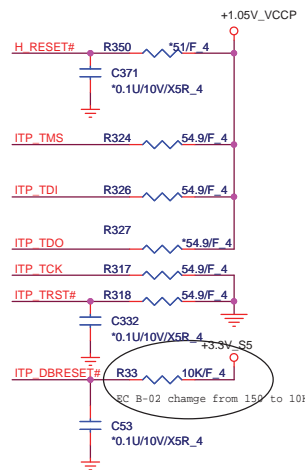
Note:
H_DPRTSTP need to daisy chain
from ICH9 to IMPV6 to CPU.



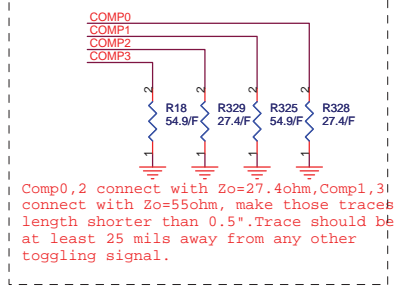
For the purpose of testability, route these signals through a ground referenced Z0 = 55ohm trace that ends in a via that is near a GND via and is accessible through an oscilloscope connection.

| FSB | BCLK | BSEL2 | BSEL1 | BSEL0 |
|-----|------|-------|-------|-------|
| 533 | 133 | 0 | 0 | 1 |
| 667 | 166 | 0 | 1 | 1 |
| 800 | 200 | 0 | 1 | 0 |

Populate ITP700Flex for bringup



| ITP700 layout guidelines | | | | |
|--------------------------|---|------------|--|--|
| Signal | Resistor Value | Connect To | Resistor Placement | |
| TDI | 54.9 ohm ± 5% | VCCP | Place the pull-up near CPU | |
| TMS | 54.9 ohm ± 1% | VCCP | Within 200ps of ITP connector | |
| TRST# | 54.9 ohm ± 5% | GND | Place the pull-down near CPU | |
| TCK | 54.9 ohm ± 1% | GND | Connect to TCK pin of CPU and then connect it to FBO pin of ITP connector in daisy chain. Place the pull-down near TCK0 pin of ITP connector | |
| TDO | 54.9 ohm ± 5% | VCCP | Place the pull-up near ITP | |
| RESET# | 54.9 ohm ± 1% series resistor and pullup 51 ohm ± 1%. | VCCP | Connect to CPURST# pin of GMCH through the series resistor placed within 200ps of ITP connector. Place the pull-up after the series resistor from ITP connector. | |

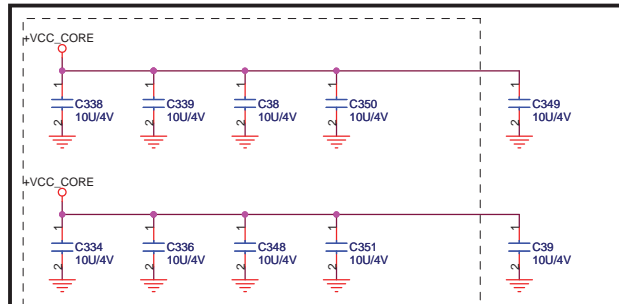


Comp0,2 connect with Zo=27.4ohm, Comp1,3 connect with Zo=55ohm, make those traces length shorter than 0.5". Trace should be at least 25 mils away from any other toggling signal.

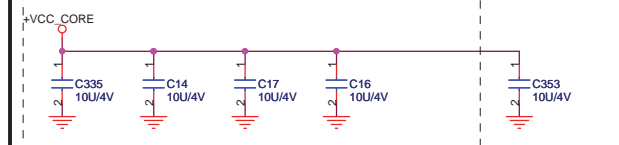
PROJECT : SA6
Quanta Computer Inc.

| | | |
|------------------------------|-----------------------------|---------------|
| Size | Document Number | Rev |
| Custor | Penryn Processor (HOST BUS) | B8 |
| Date: Friday, April 25, 2008 | | Sheet 3 of 41 |

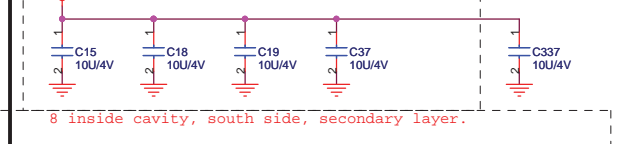
All use 22U 10V(+20%,X5R,1210)Pb-Free.



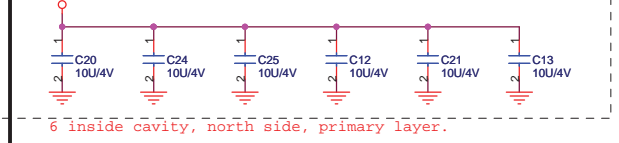
8 inside cavity, north side, secondary layer.



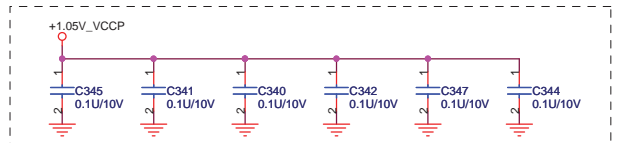
6 inside cavity, south side, secondary layer.



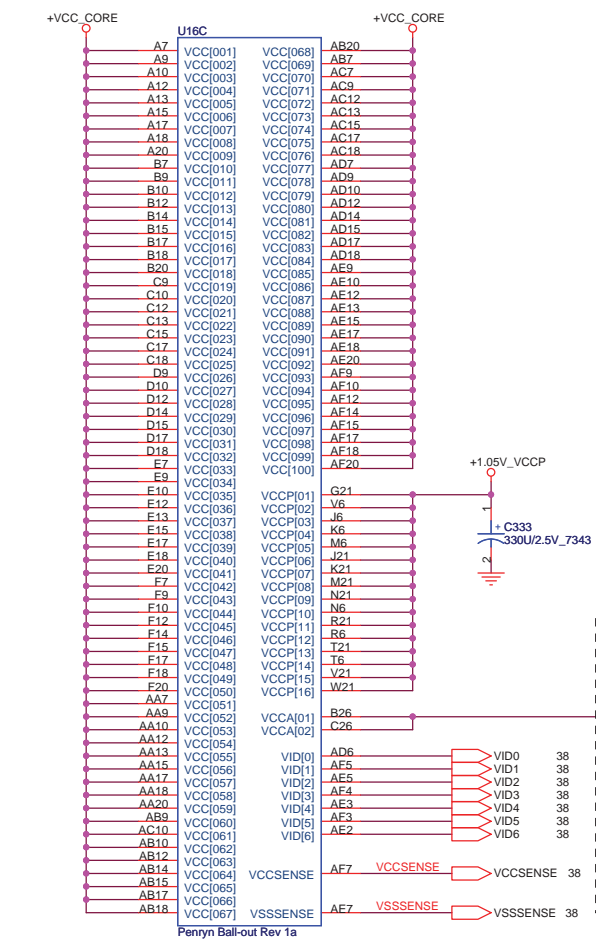
6 inside cavity, north side, primary layer.



6 inside cavity, south side, primary layer.



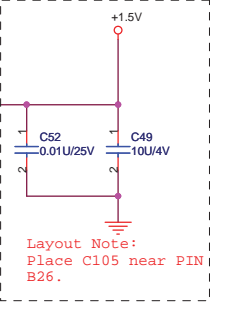
Layout out:
Place these inside socket cavity on North side secondary.



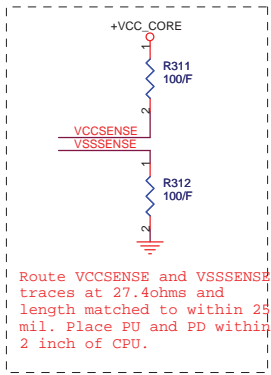
Penryn Ball-out Rev 1a

C331 and C317 remove in B stage
C317 PAD remove in FAI stage

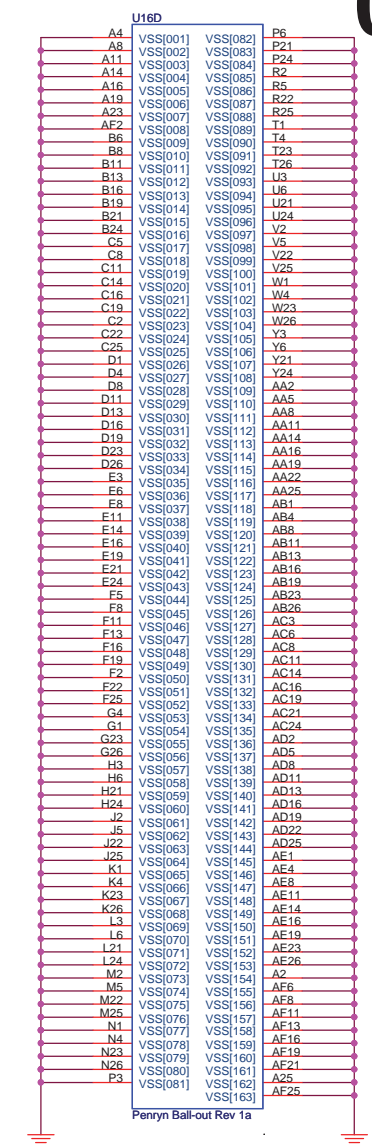
Layout Note:
Need to add 100uF cap on PWR_SRC for cap singing.
Place on PWR_SRC near +VCC_CORE.




Layout Note:
Place C105 near PIN B26.



Route VCCSENSE and VSSSENSE traces at 27.4ohms and length matched to within 25 mil. Place PU and PD within 2 inch of CPU.



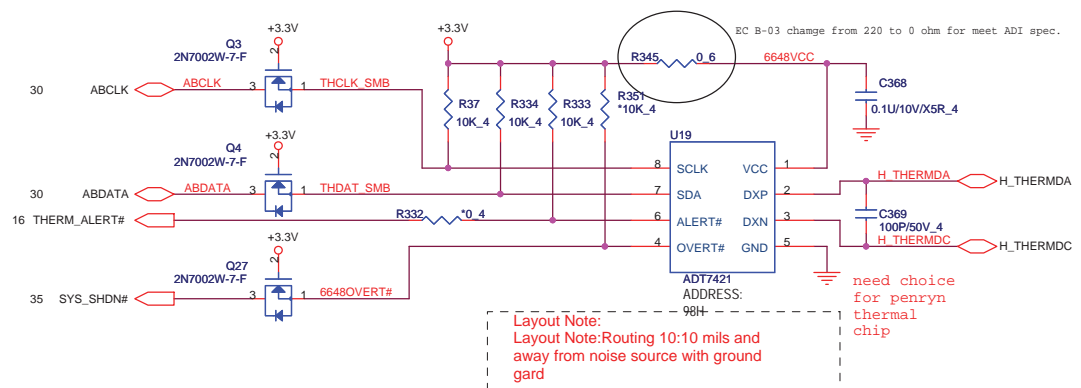
Penryn Ball-out Rev 1a



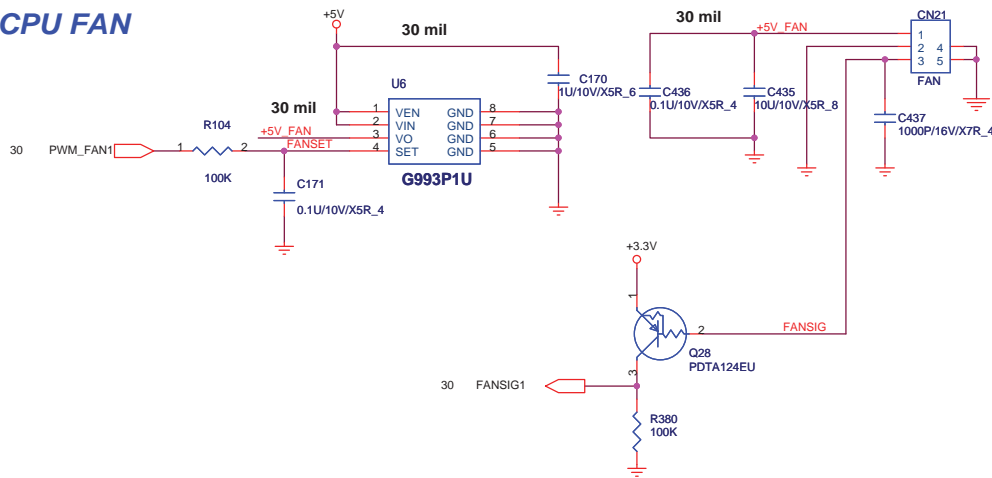
PROJECT : SA6
Quanta Computer Inc.

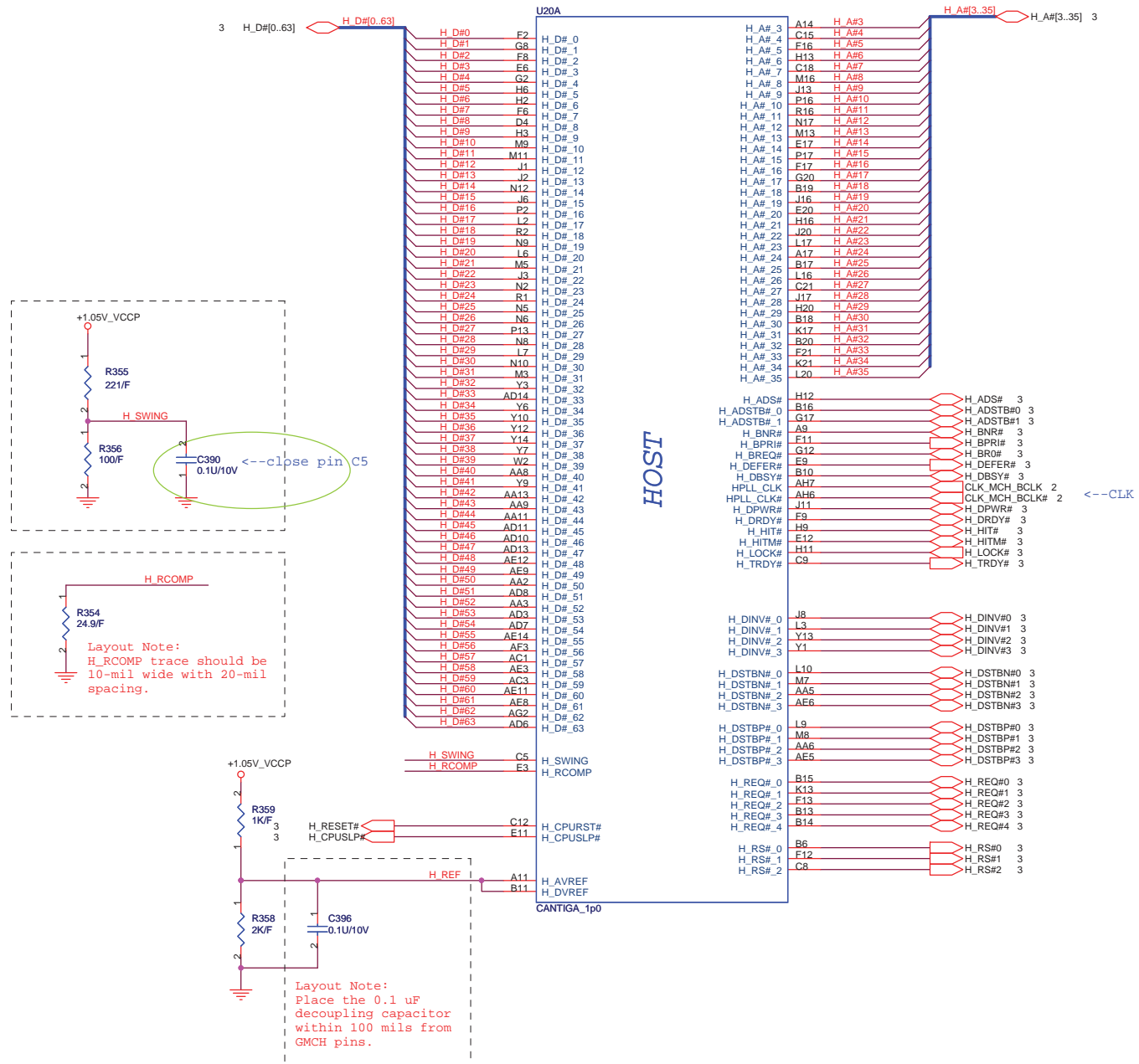
| | | |
|------------------------------|---|---------------|
| Size Custom | Document Number Penryn Processor (POWER) | Rev 5B |
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CPU Thermal monitor



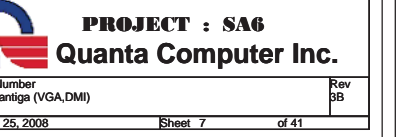
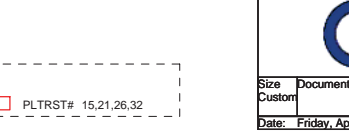
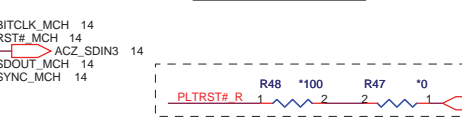
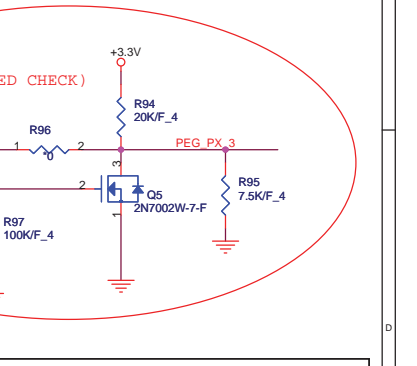
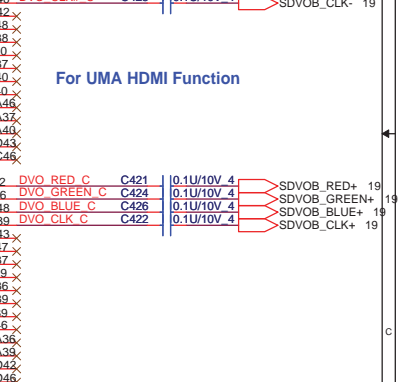
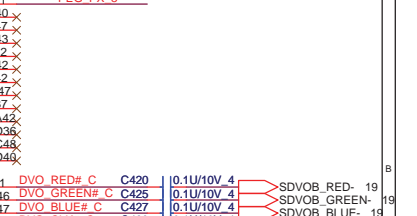
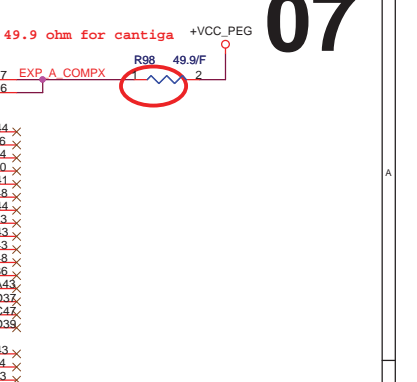
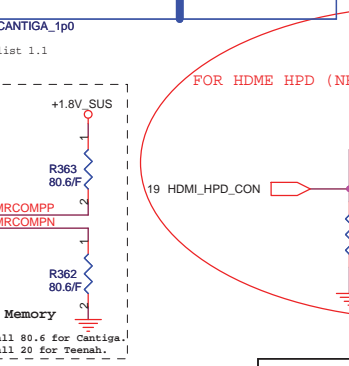
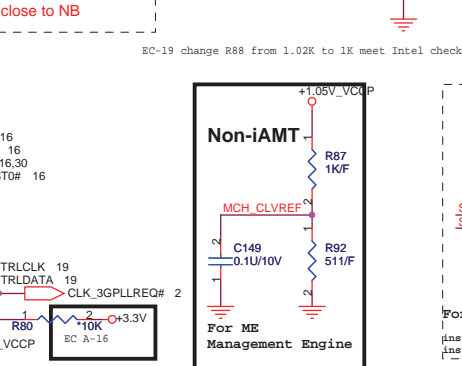
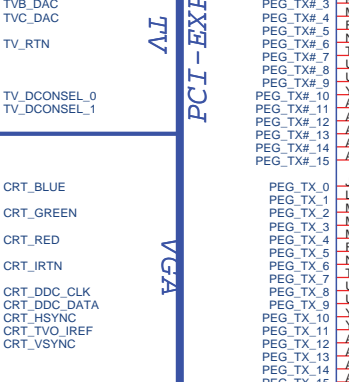
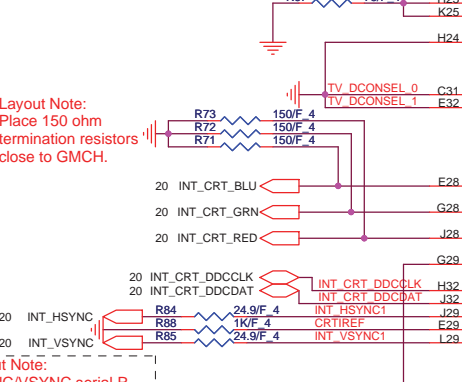
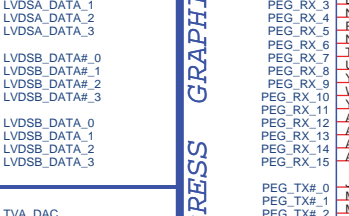
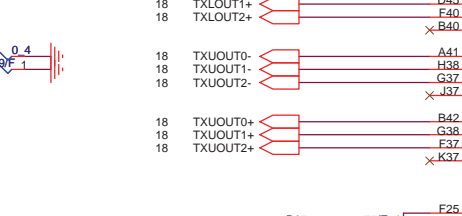
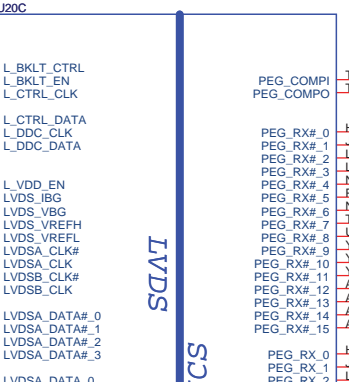
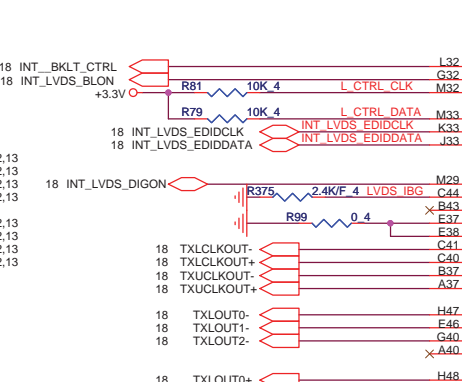
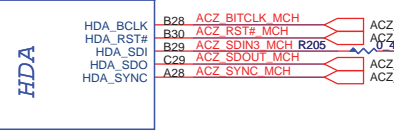
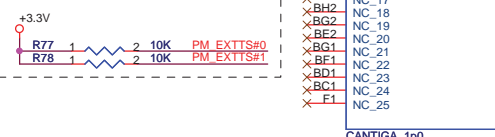
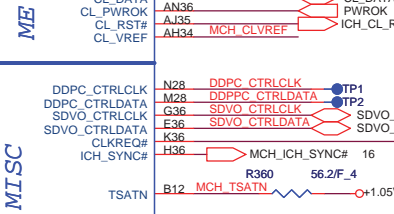
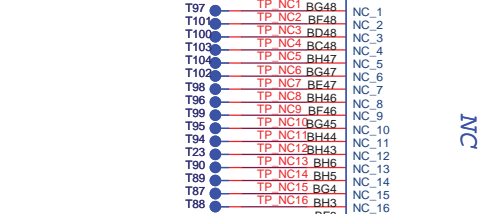
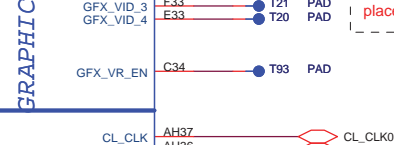
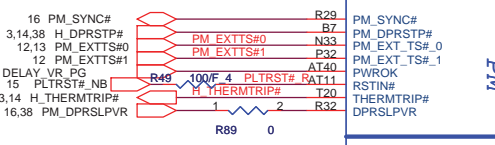
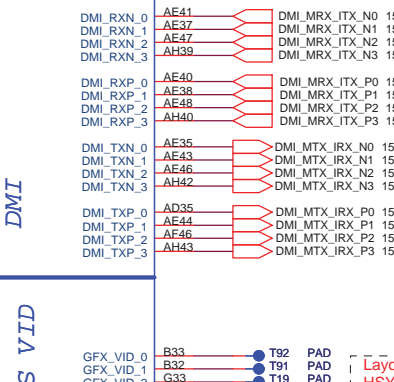
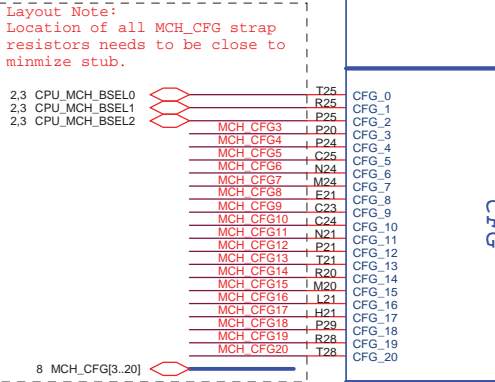
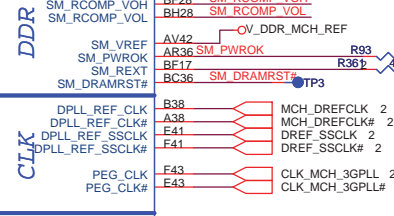
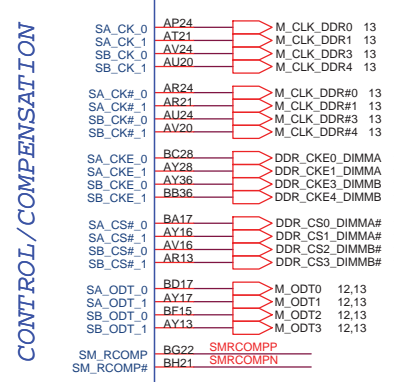
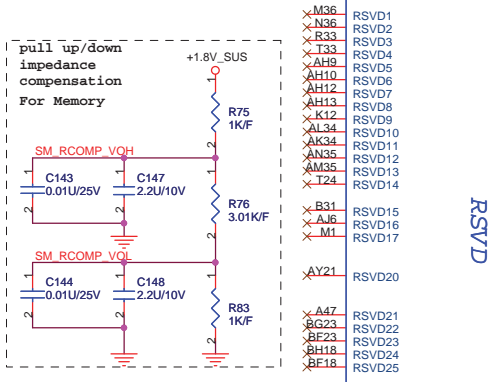
CPU FAN





PROJECT : SA6
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| | | |
|------------------------------|-----------------|---------------|
| Size | Document Number | Rev |
| Custom | Cantiga (HOST) | B8 |
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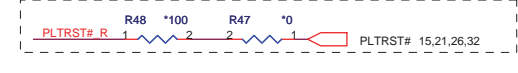
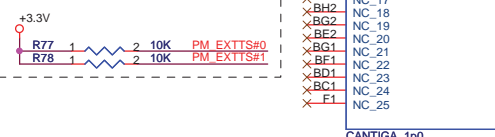
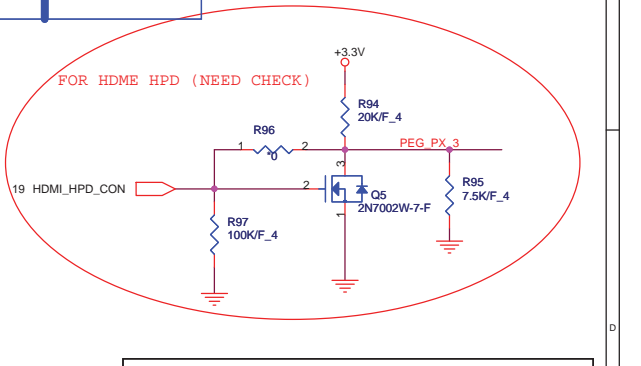
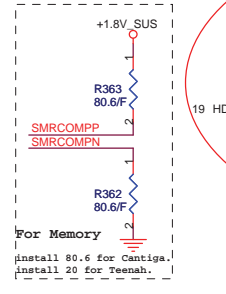
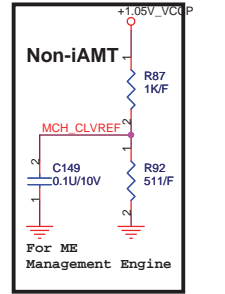


Layout Note: Location of all MCH_CFG strap resistors needs to be close to minimize stub.

Layout Note: Place 150 ohm termination resistors close to GMCH.

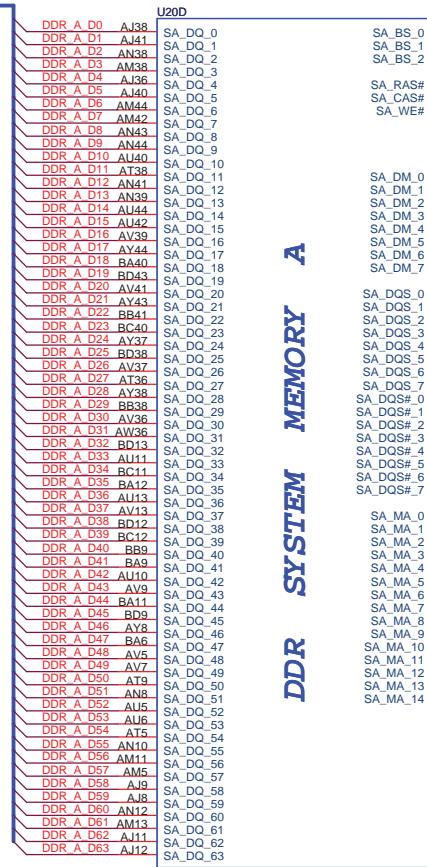
Layout Note: HSYNC/VSYNC serial R place close to NB

EC-19 change R88 from 1.02K to 1K meet Intel check list 1.1



PROJECT : SA6
Quanta Computer Inc.
Size: Custom, Document Number: Cantiga (VGA,DMI), Rev: B6
Date: Friday, April 25, 2008, Sheet 7 of 41

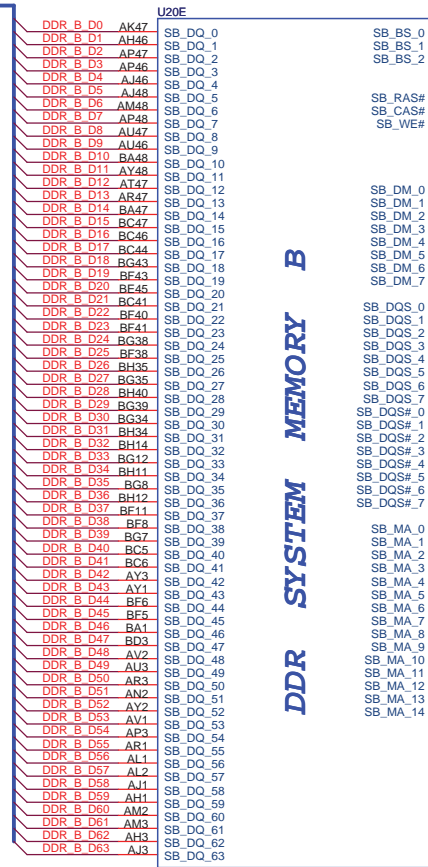
13 DDR_A_D[0..63]



DDR SYSTEM MEMORY A

CANTIGA_1p0

13 DDR_B_D[0..63]

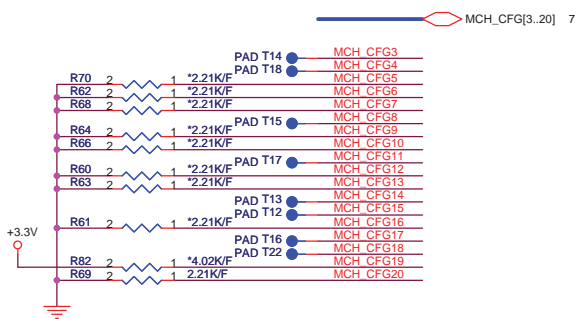


DDR SYSTEM MEMORY B

CANTIGA_1p0

STRAPPING

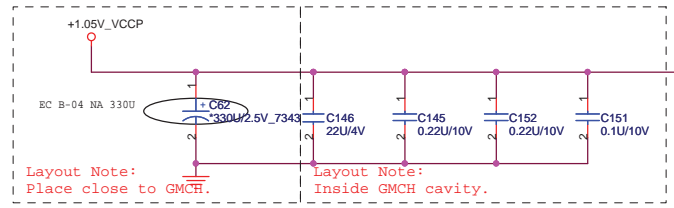
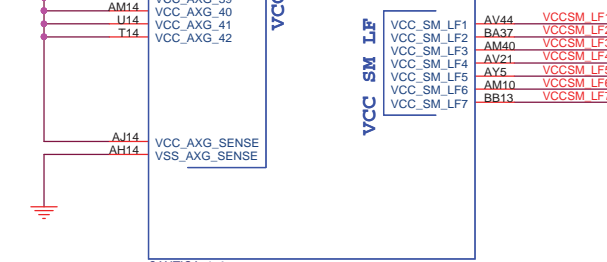
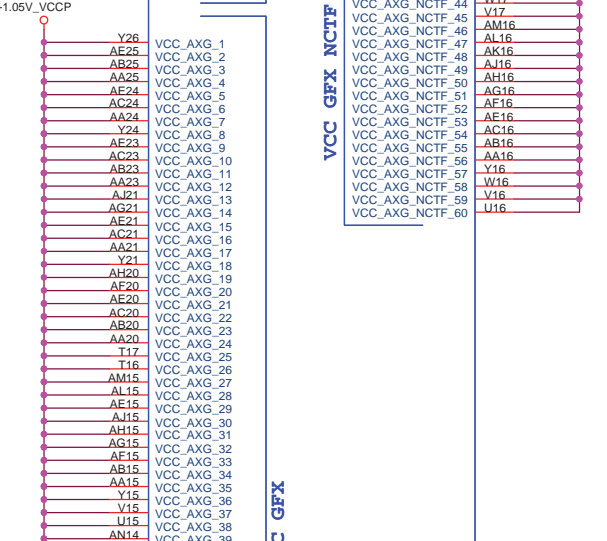
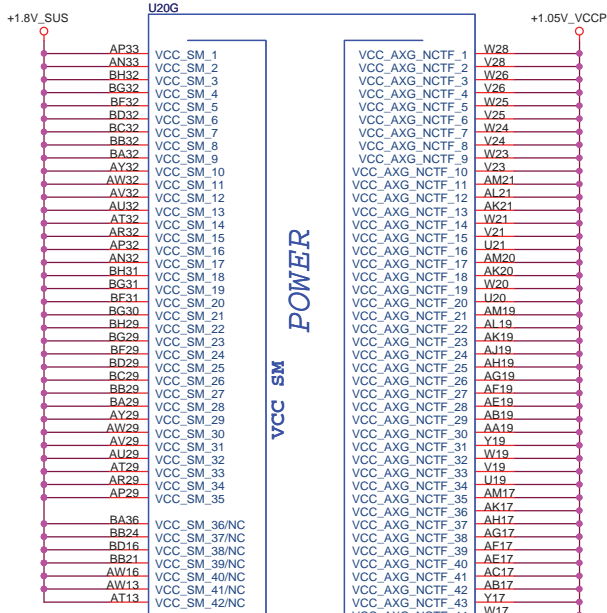
| | | |
|-------|--|--|
| CFG5 | DMI X2 Select | Low=DMIx2 High=DMIx4(Default) |
| CFG6 | iTPM Host Interface | Low= Enable High=Disable(Default) |
| CFG7 | Intel Management Engine Crypto Strap | Low= Intel Management Engine Crypto TLS cipher suite with no Confidentiality High=Intel Management Engine Crypto TLS cipher suite with Confidentiality(Default) |
| CFG9 | PCI Express Graphic Lane | Low= Reverse Lane High=Normal operation |
| CFG10 | PCIe Loopback Enable | Low= Enable High=Disable(Default) |
| CFG16 | FSB Dynamic ODT | Low=Dynamic ODT Disable High=Dynamic ODT Enable(default). |
| CFG19 | DMI Lane Reversal | Low=Normal(default). High=Lane Reversed |
| CFG20 | Digital Display Port(SDVO/DP/iHDMI) and PCIe Concurrent Operation. | Low=Only DP or inly PCIe is operational (defaults) High=DP and PCIe xl are operating simultaneously. |
| CFG13 | CFG12 | XOR / ALLZ / Clock Un-gating 00=Reserved. 10=XOR Mode Enabled. 01=All-Z Mode Enabled. 11=Normal Operation (Default). |



PROJECT : SA6
Quanta Computer Inc.

Size: Custom Document Number: Cantiga (DDR2,STRAPPING) Rev: SB

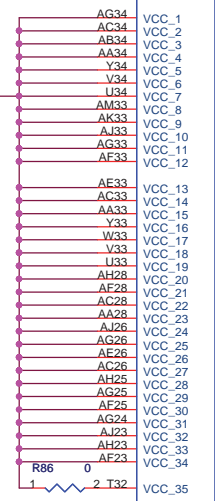
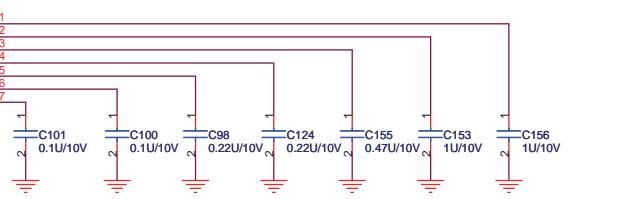
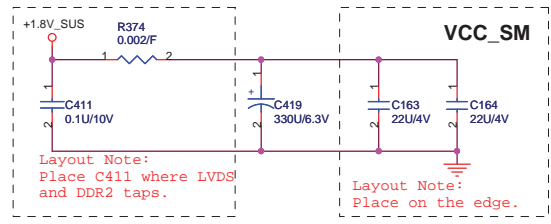
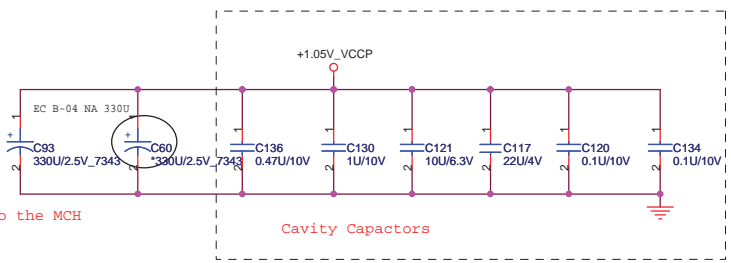
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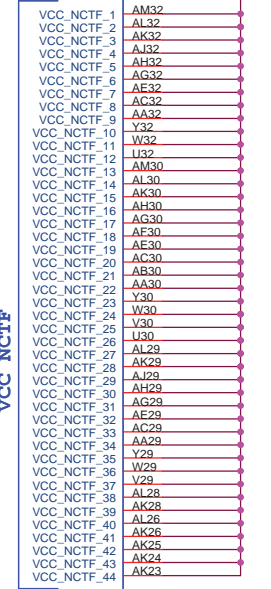
NB Power Status and max current table(1/3)

| POWER PLANE | S0 | S3 | S4/S5 | Voltage | I(max) | Note |
|-----------------|----|----|-------|----------|--------|------------------------|
| VCC(EXT_VGA) | O | X | X | +1.05V | 2178mA | |
| VCC(INT_VGA) | O | X | X | +1.05V | 2899mA | |
| VCC_AXG | O | X | X | +1.05V | 8700mA | Graphics Core |
| VCC_SM(800) | O | O | X | +1.8VSUS | 3A | (DDR11-667) 2.6A |
| VCC_SM(Standby) | O | O | X | +1.8VSUS | 1mA | Self Refresh during S3 |

(See NB EDS Rev:1.0 Section 10.1 for max current)
 (See NB EDS Rev:1.0 Section 12.2 for DC voltage)




VCC CORE
POWER



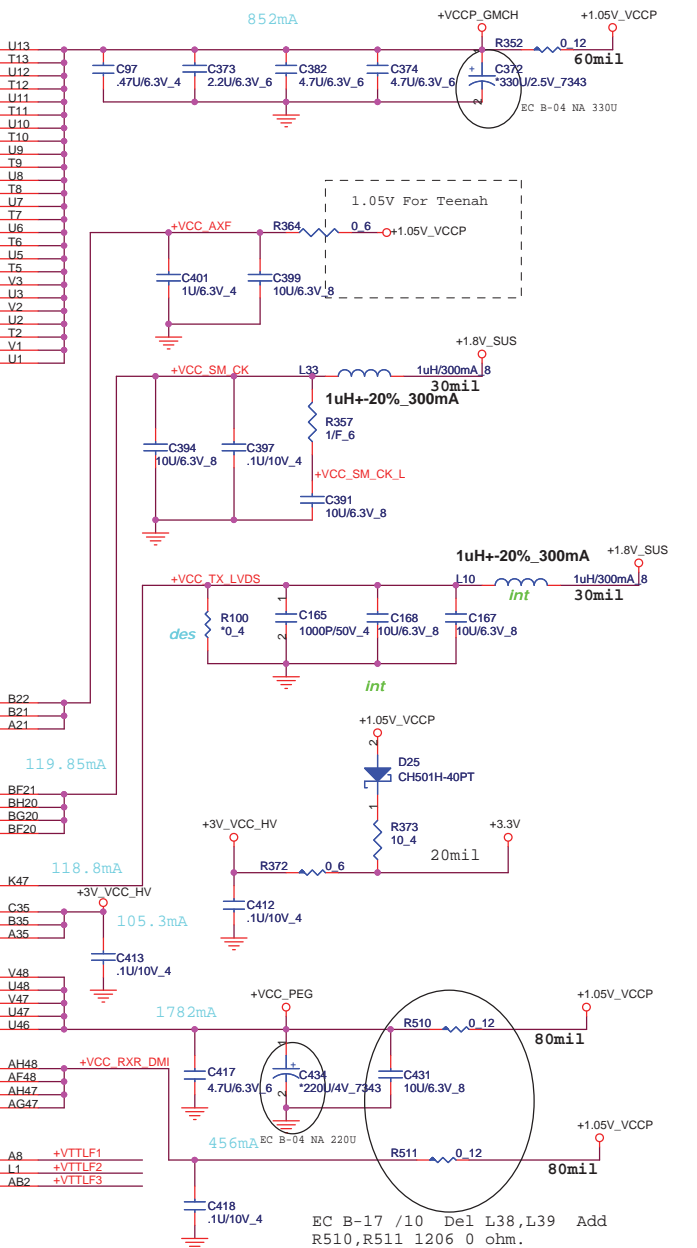
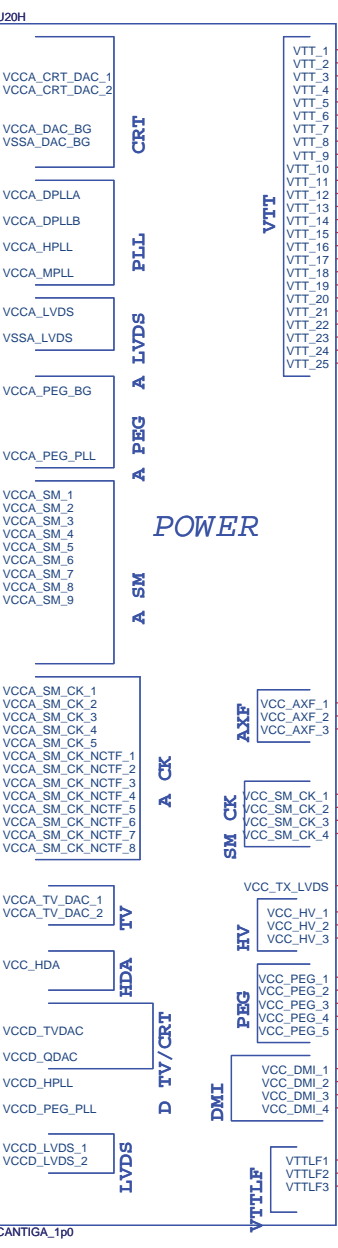
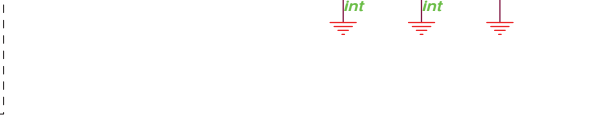
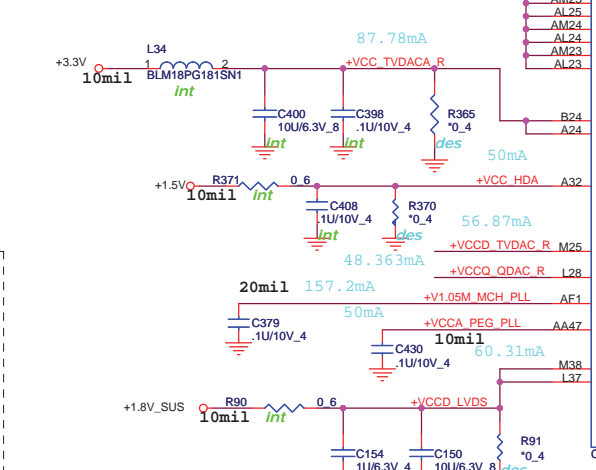
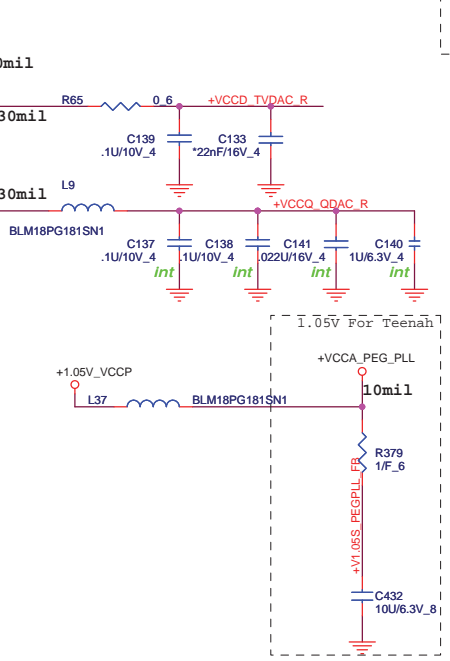
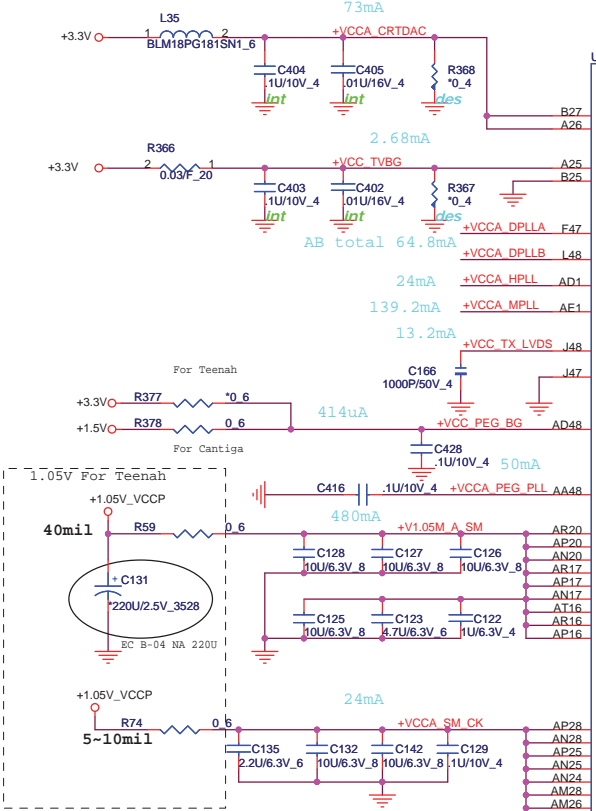
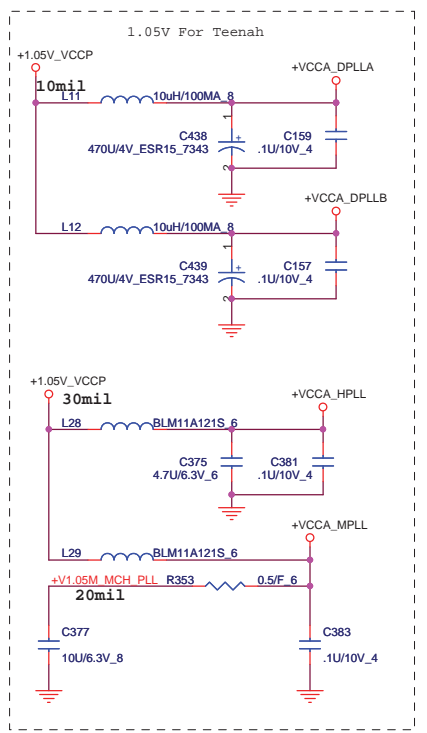
VCC NCTF

CANTIGA_1p0



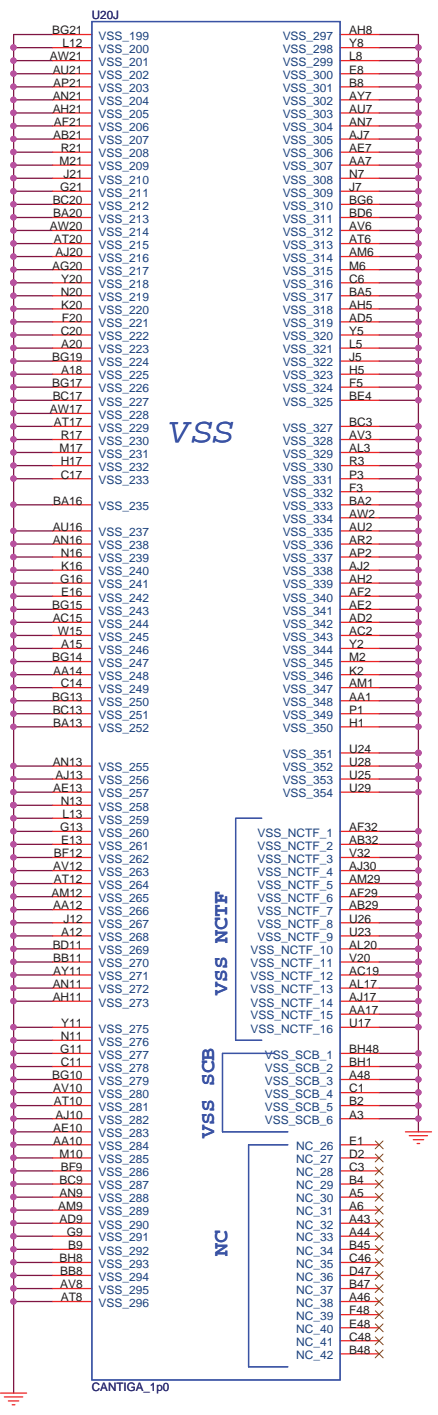
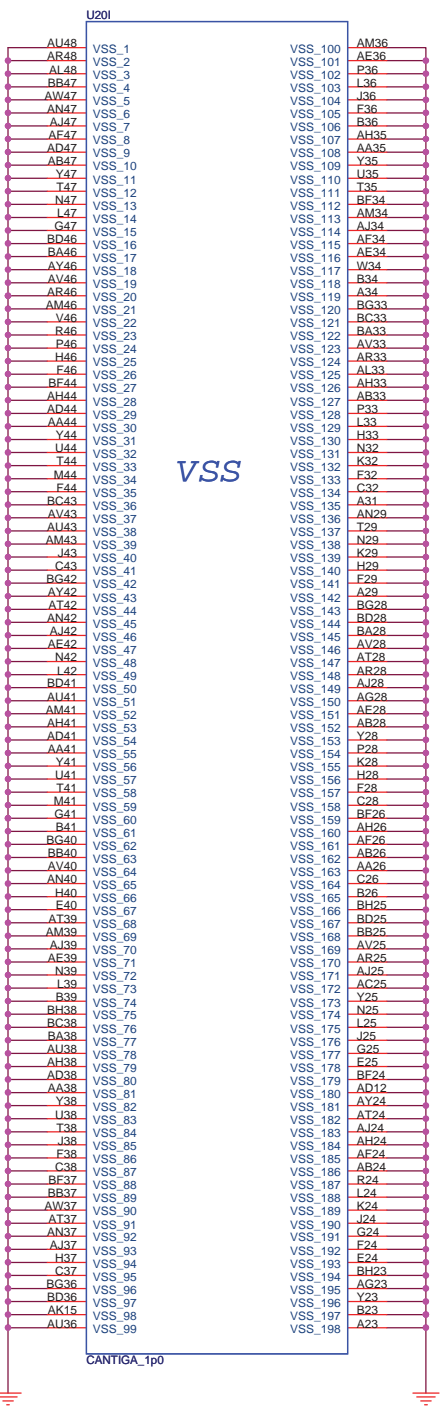
PROJECT : SA6
Quanta Computer Inc.

| | | |
|------------------------------|--------------------|---------------|
| Size | Document Number | Rev |
| Custom | Cantiga (VCC,NCTF) | B8 |
| Date: Friday, April 25, 2008 | | Sheet 9 of 41 |



PROJECT : SA6
Quanta Computer Inc.

| | | | |
|------------------------------|-----------------|----------------|--|
| Size | Document Number | Rev | |
| Custom | Cantiga (POWER) | B6 | |
| Date: Friday, April 25, 2008 | | Sheet 10 of 41 | |



PROJECT : SA6
Quanta Computer Inc.

Size: Document Number
 Custom: Cantiga (VSS)

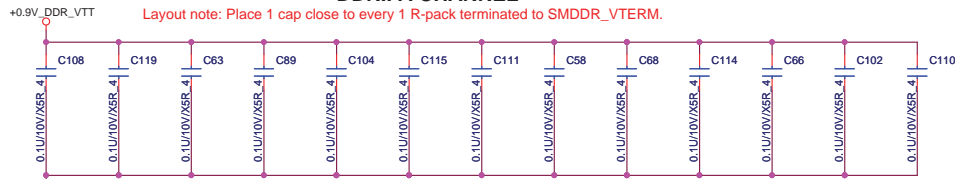
Date: Friday, April 25, 2008

Rev: 88

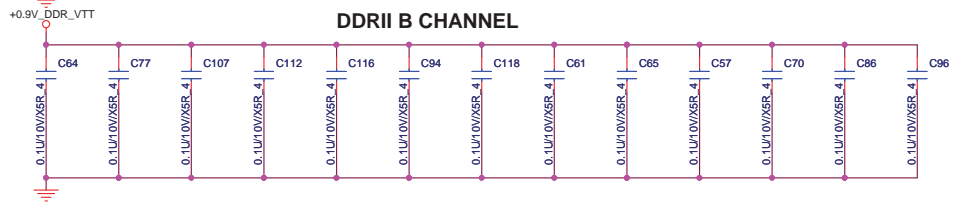
Sheet 11 of 41

DDRII A CHANNEL

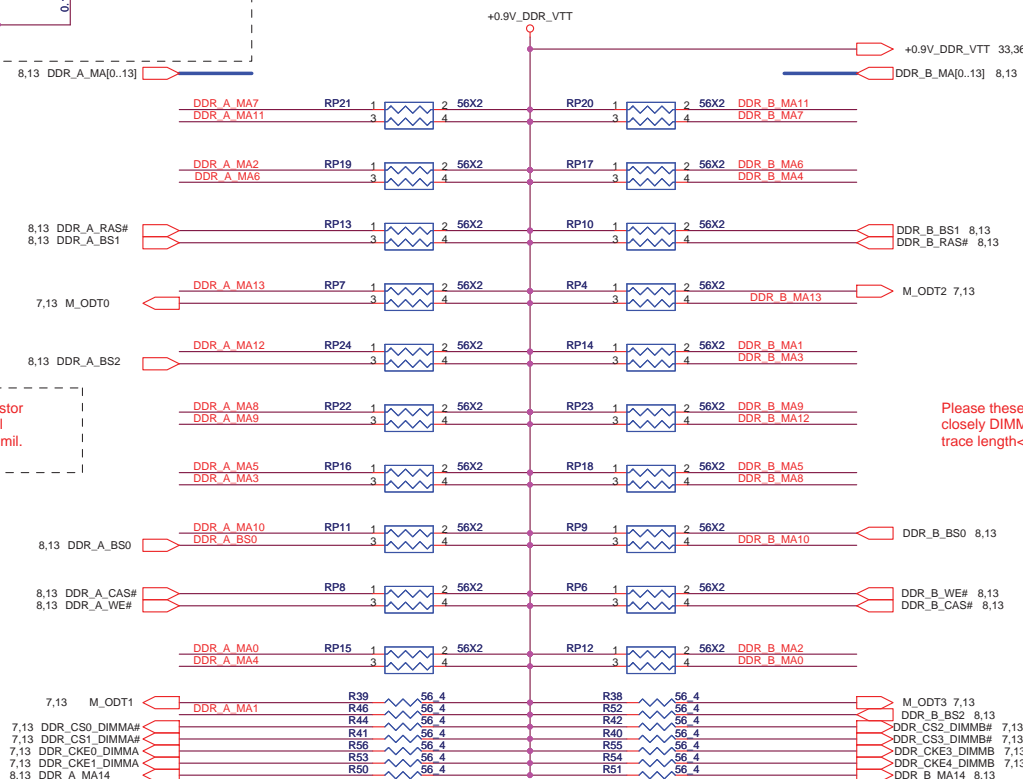
Layout note: Place 1 cap close to every 1 R-pack terminated to SMDDR_VTERM.



DDRII B CHANNEL



8,13 DDR_A_MA[0..13]

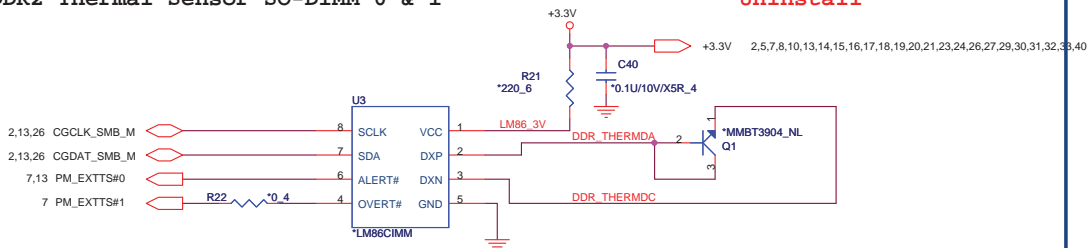


Please these resistor closely DIMMA, all trace length < 750 mil.

Please these resistor closely DIMMB, all trace length < 750 mil.

DDR2 Thermal Sensor SO-DIMM 0 & 1

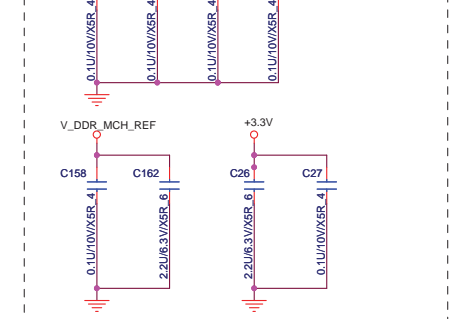
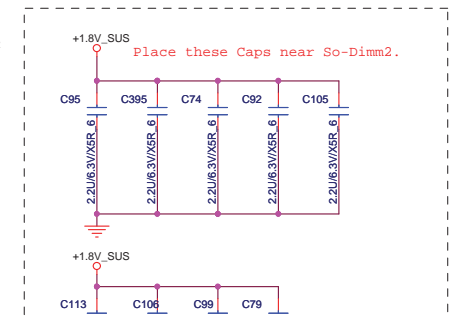
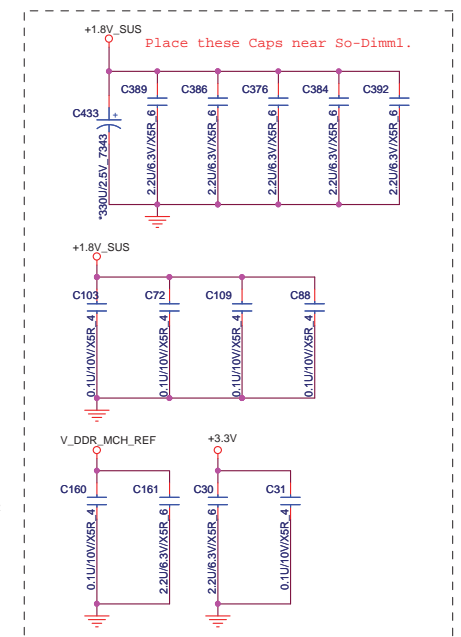
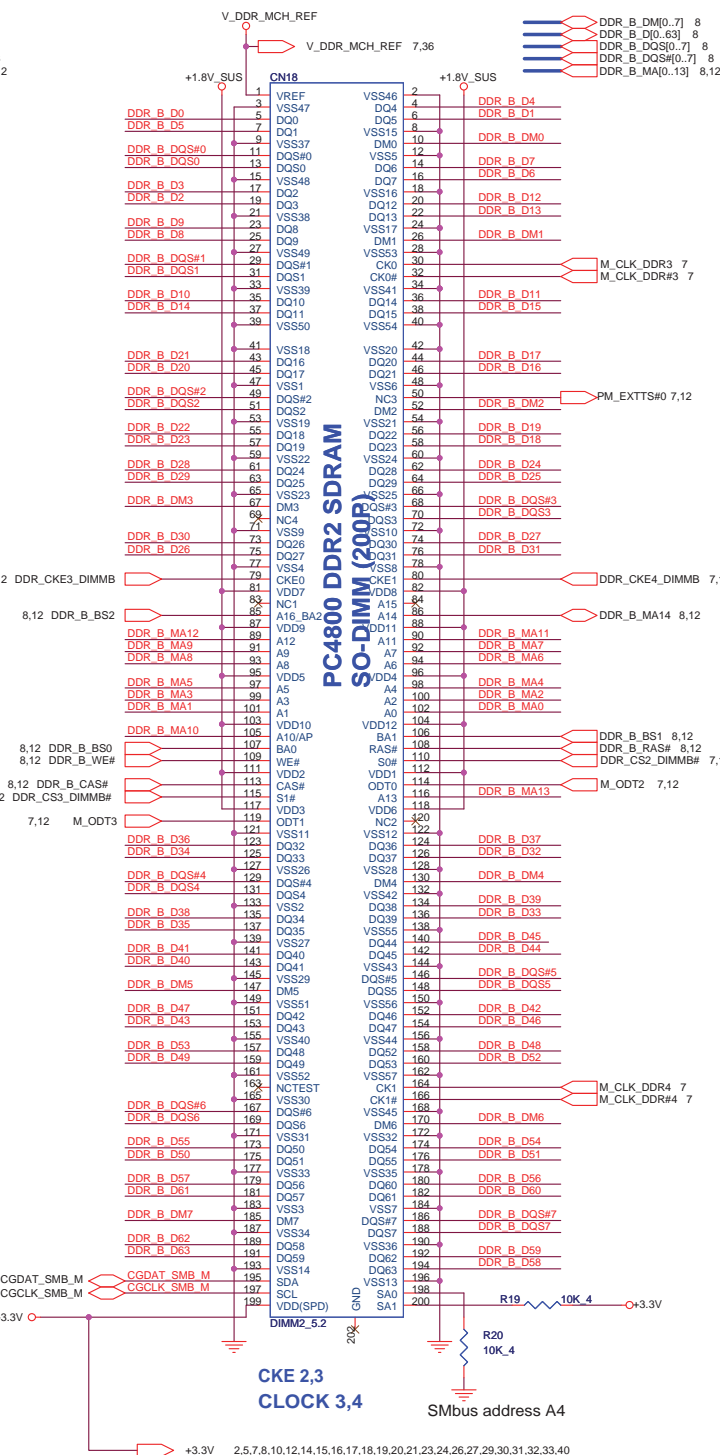
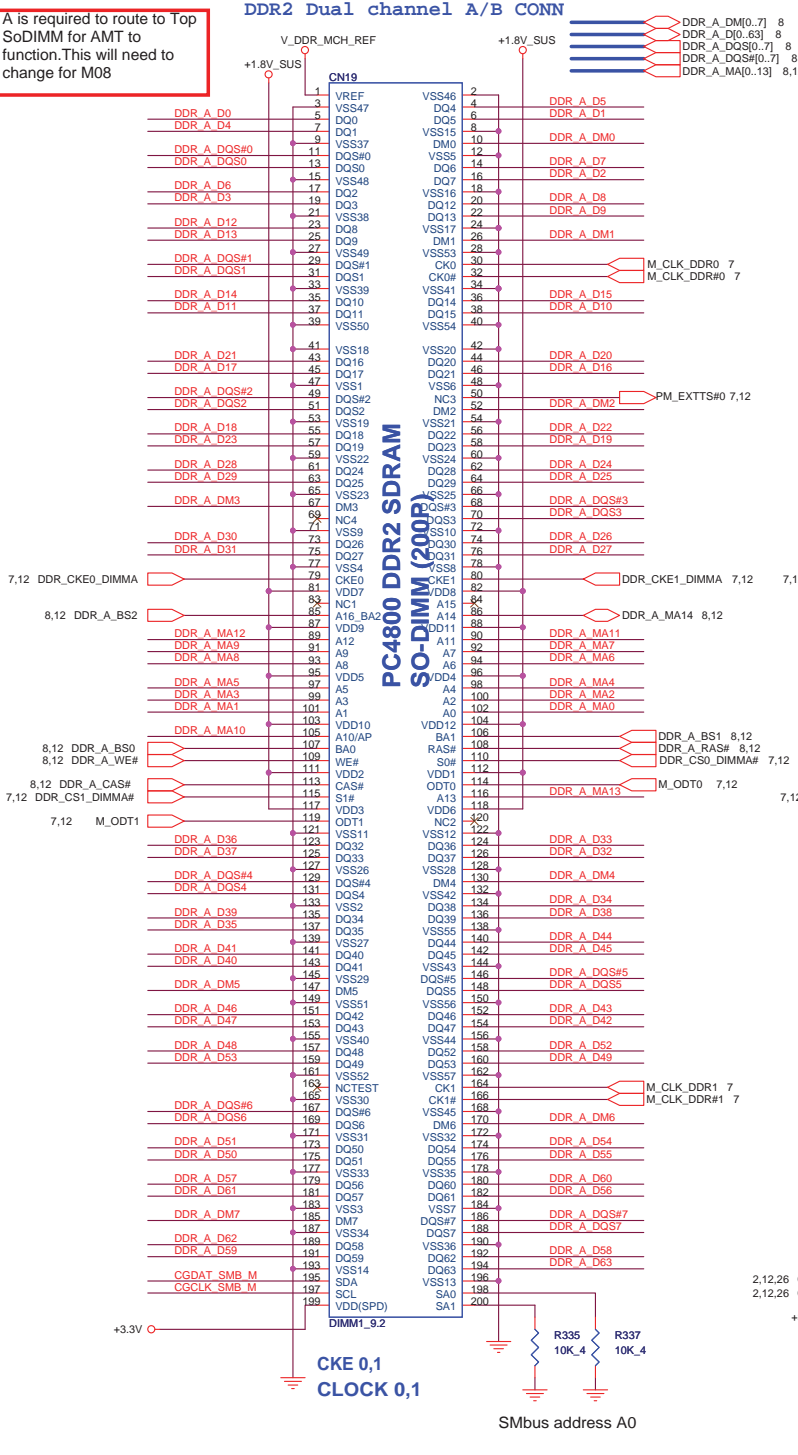
Uninstall



PROJECT : SAG
Quanta Computer Inc.

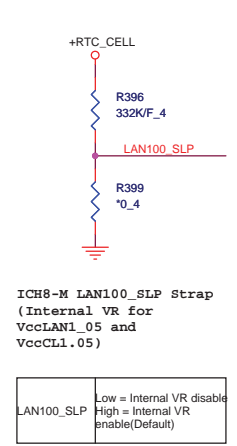
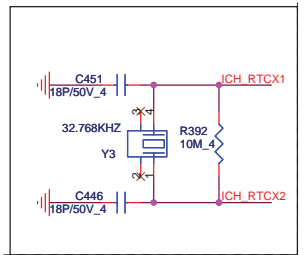
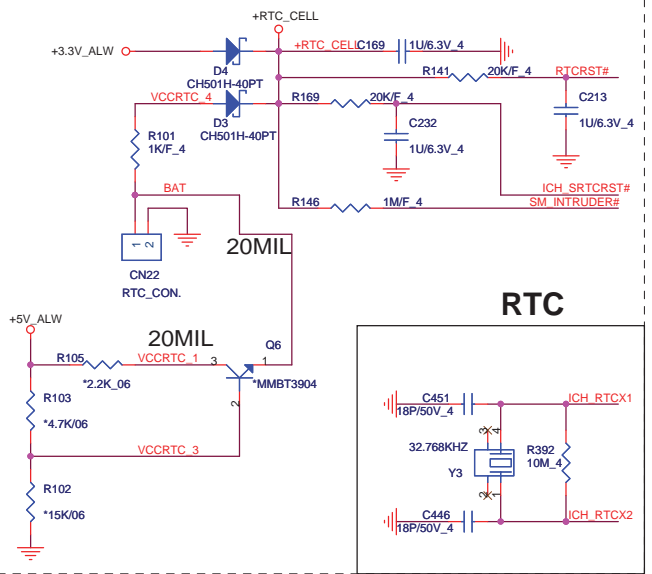
| | | |
|------------------------------|-----------------|-------|
| Size | Document Number | Rev |
| Custom | DDR.RES.ARRAY | 8B |
| Date: Friday, April 25, 2008 | Sheet 12 | of 41 |

A is required to route to Top SoDIMM for AMT to function. This will need to change for M08



PROJECT : SA6
Quanta Computer Inc.

Size: Custom
Document Number: DDR SO-DIMM(200P)
Date: Friday, April 25, 2008
Rev: 8B
Sheet 13 of 41



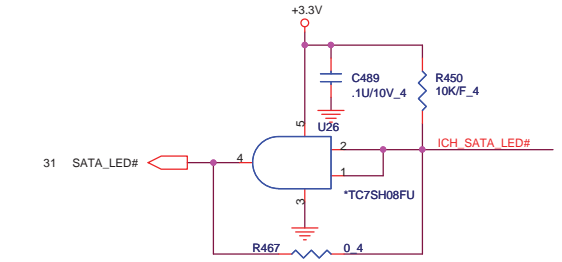
ICH8M Internal VR Enable Strap
(Internal VR for VccSus1.05, VccSus1.5, VccCL1.5)

| | |
|--------------|---|
| ICH_INTVRMEN | Low = Internal VR Disabled High = Internal VR Enabled(Default) |
|--------------|---|

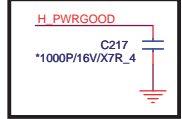
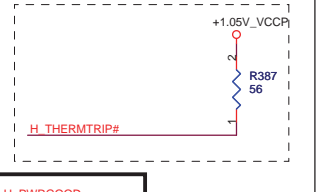
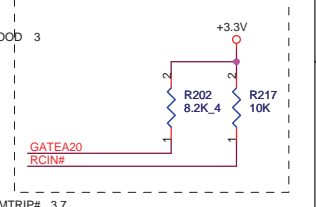
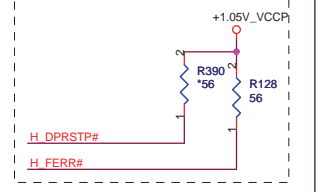
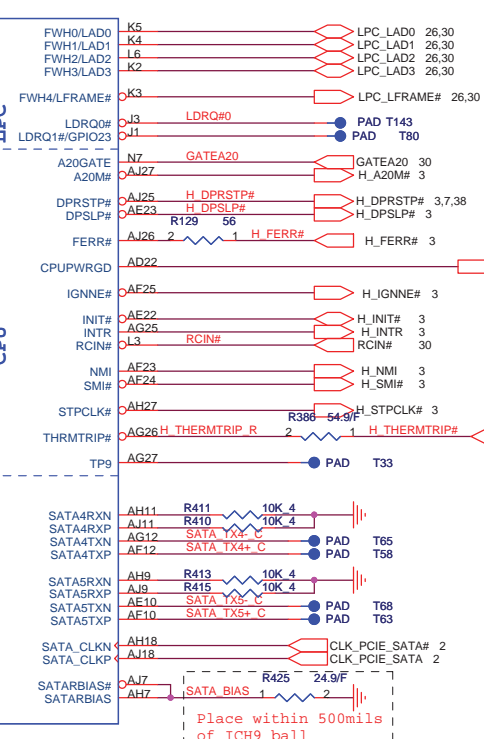
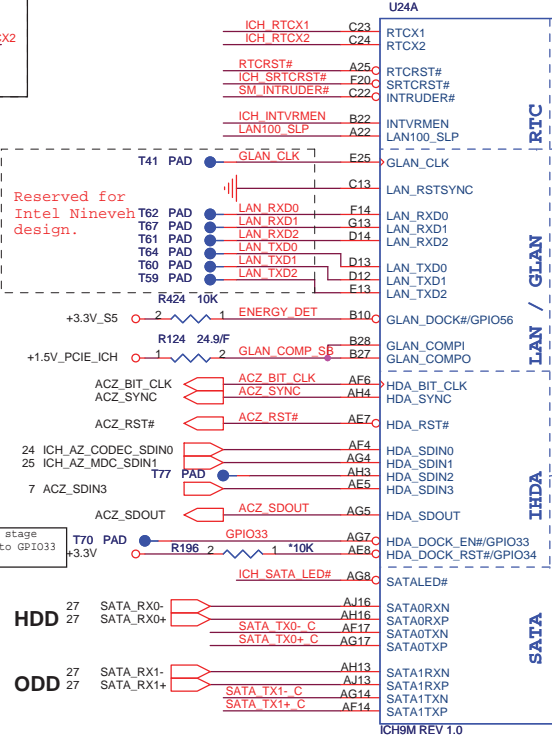
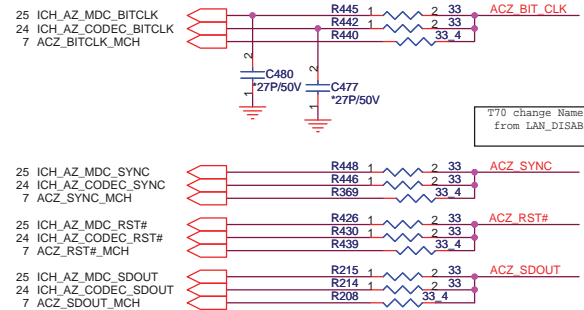
XOR Chain Entrance Strap

| ICH TP3 | HDA SDOUT | Description |
|---------|-----------|----------------------------|
| 0 | 0 | RSVD |
| 0 | 1 | Enter XOR Chain |
| 1 | 0 | Normal Operation (Default) |
| 1 | 1 | Set PCIE port config bit 1 |

SB Strap

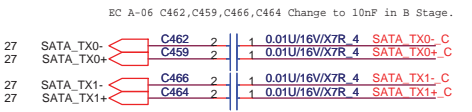


AZ Interface (MDC, CODEC, HDMI)



Place all series terms close to ICH9 except for SDIN input lines, which should be close to source. Placement of R603, R600, R607 & R612 should equal distance to the T split trace point as R604, R599, R606 & R608 respective. Basically, keep the same distance from T for all series termination resistors.

AC-TX for SATA

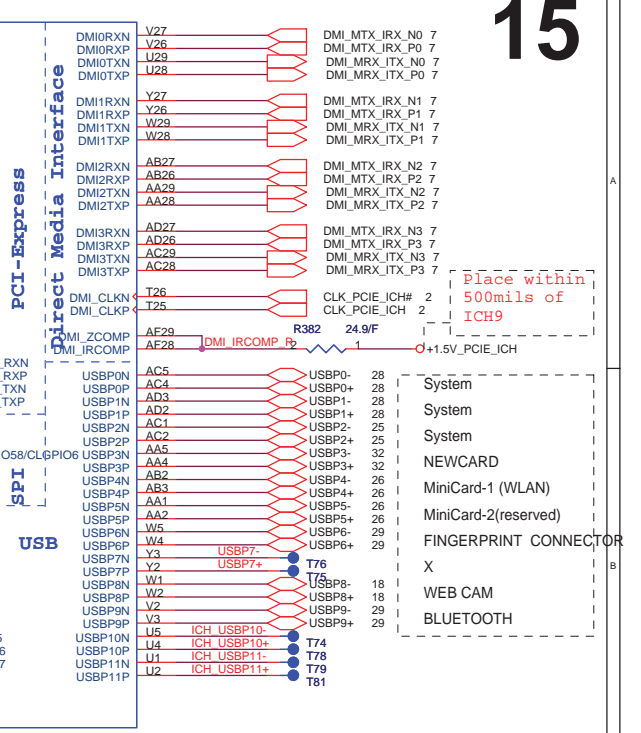
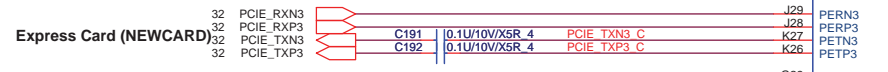
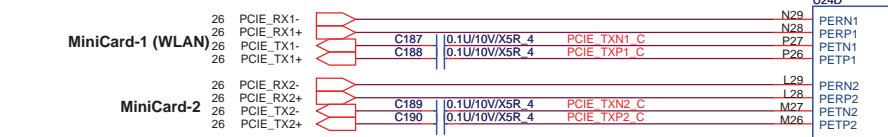
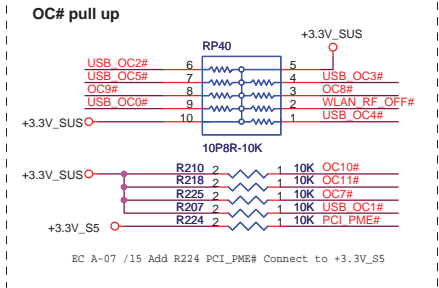


Distance between the ICH-9 M and cap on the "P" signal should be identical distance between the ICH-9 M and cap on the "N" signal for same pair.

PROJECT : SA6
Quanta Computer Inc.

| | | |
|--------|------------------------------------|----------------|
| Size | Document Number | Rev |
| Custom | ICH9-M (CPU,IDE,SATA,LPC,AC97,LAN) | B5 |
| Date: | Friday, April 25, 2008 | Sheet 14 of 41 |

Place TX DC blocking caps close ICH8.



Place within 500mils of ICH9.

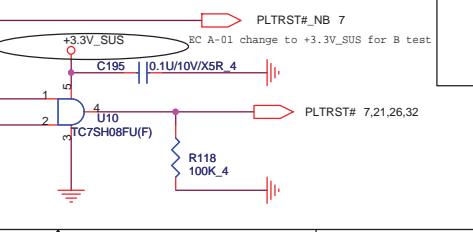
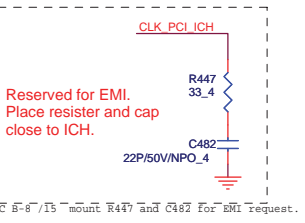
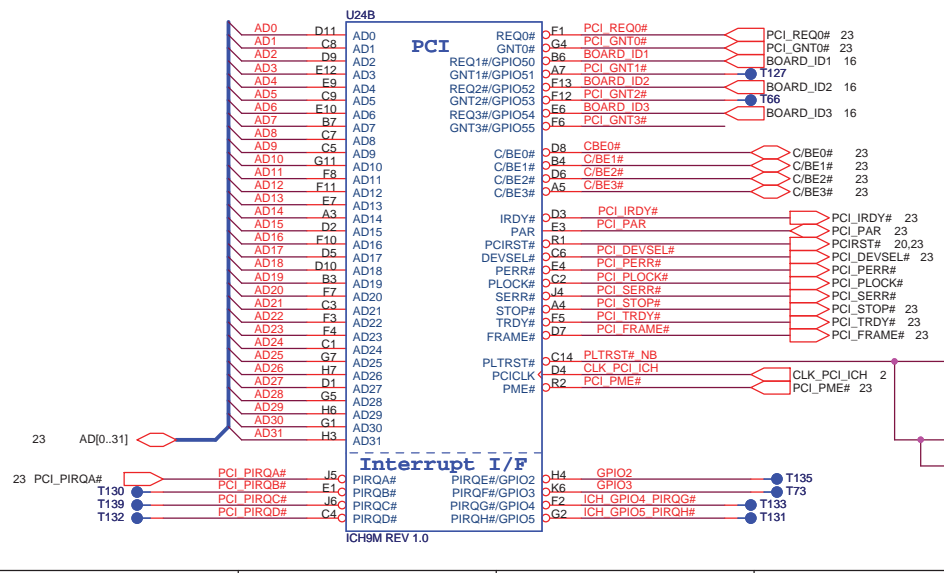
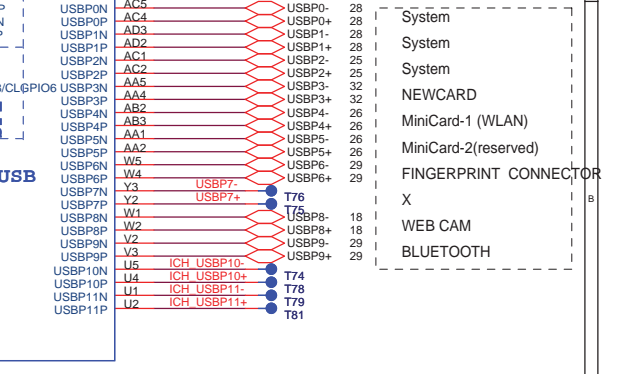
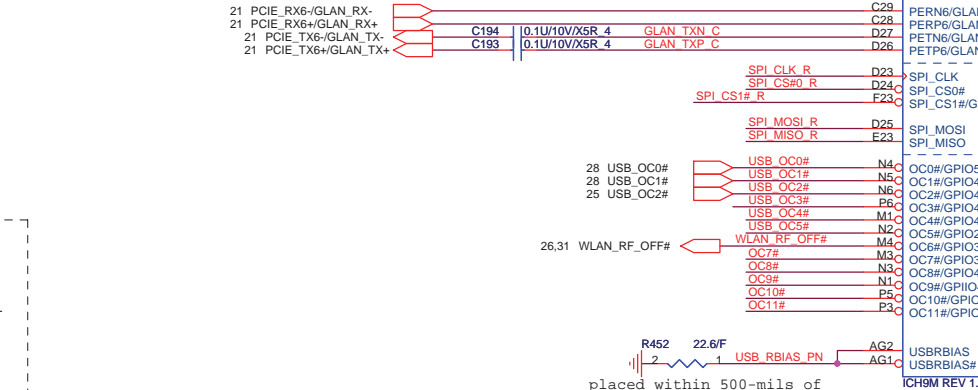
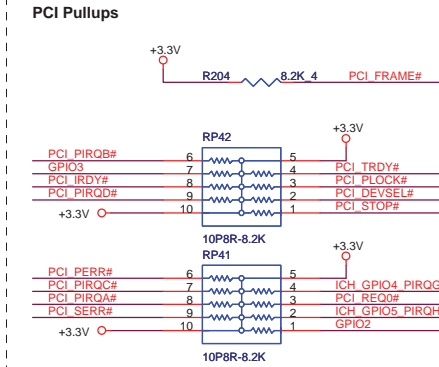
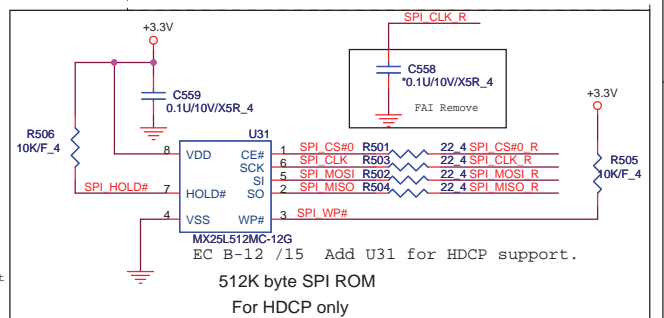


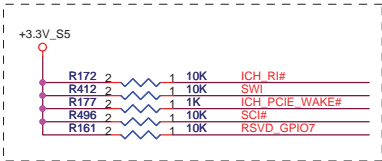
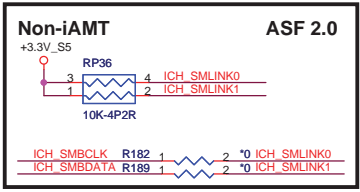
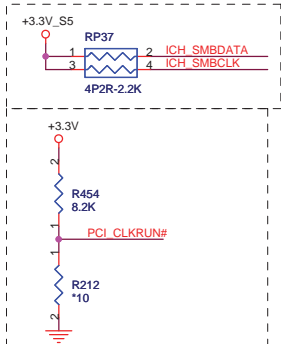
Table titled 'Boot BIOS Strap' with columns for GNT0#, SPI_CS1#, and components LPC, PCI, SPI. LPC has 11 GNT0#, No stuff SPI_CS1#. PCI has 10 GNT0#, No stuff SPI_CS1#. SPI has 01 GNT0#, Stuff SPI_CS1#.

A16 away override strap. Low = A16 swap override enabled. High = Default. Includes resistor R203 (1K).

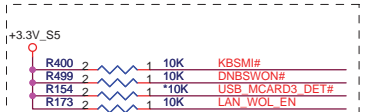
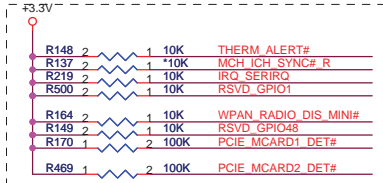
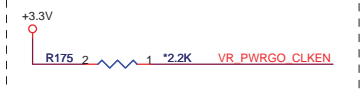
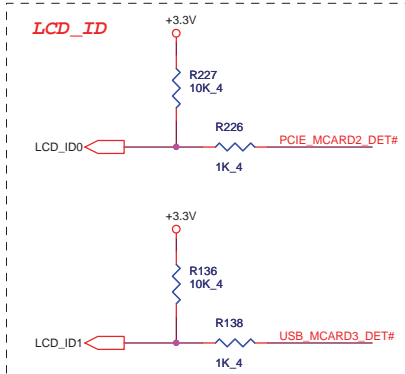


PROJECT : SA6 Quanta Computer Inc. Includes document number ICH9-M (USB,DMI,PCI,PCI) and revision 9B. Date: Friday, April 25, 2008. Sheet 15 of 41.

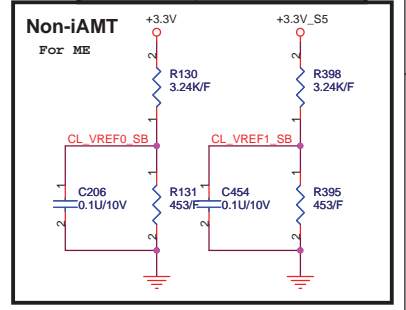
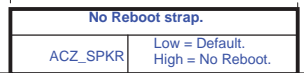
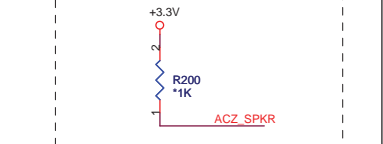
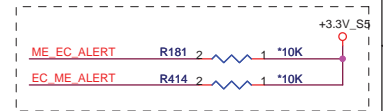
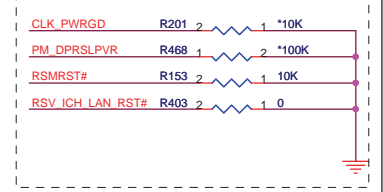
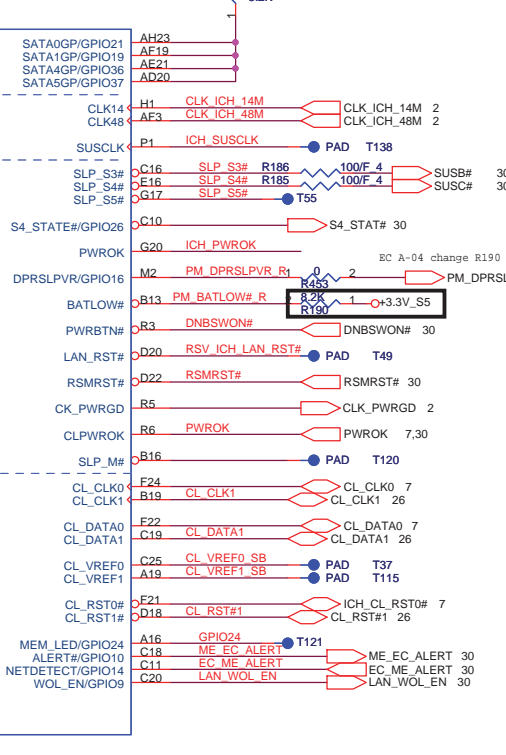
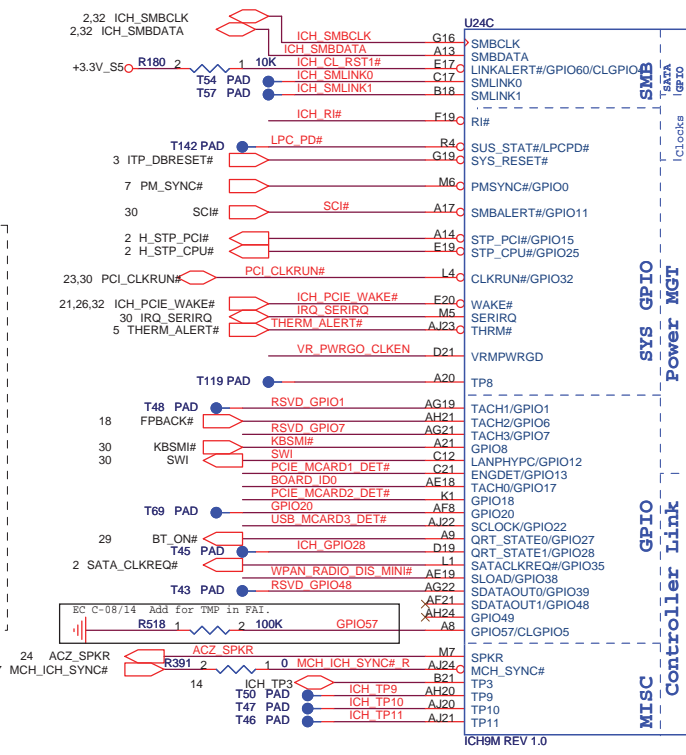
Place these close to ICH8.



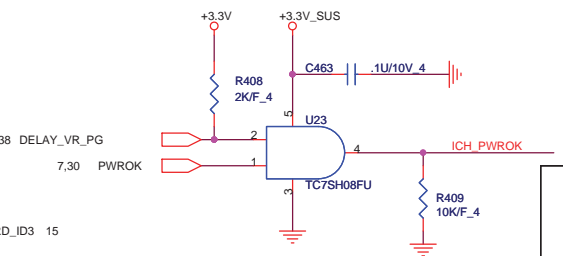
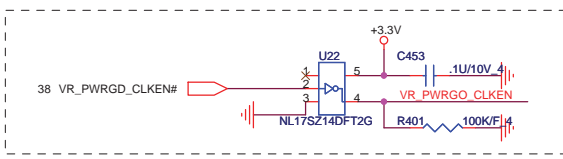
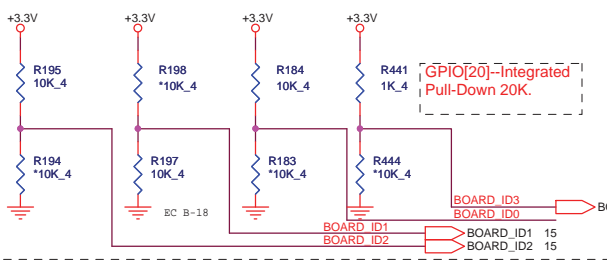
Option to "Disable" clkrun. Pulling it down will keep the clks running.

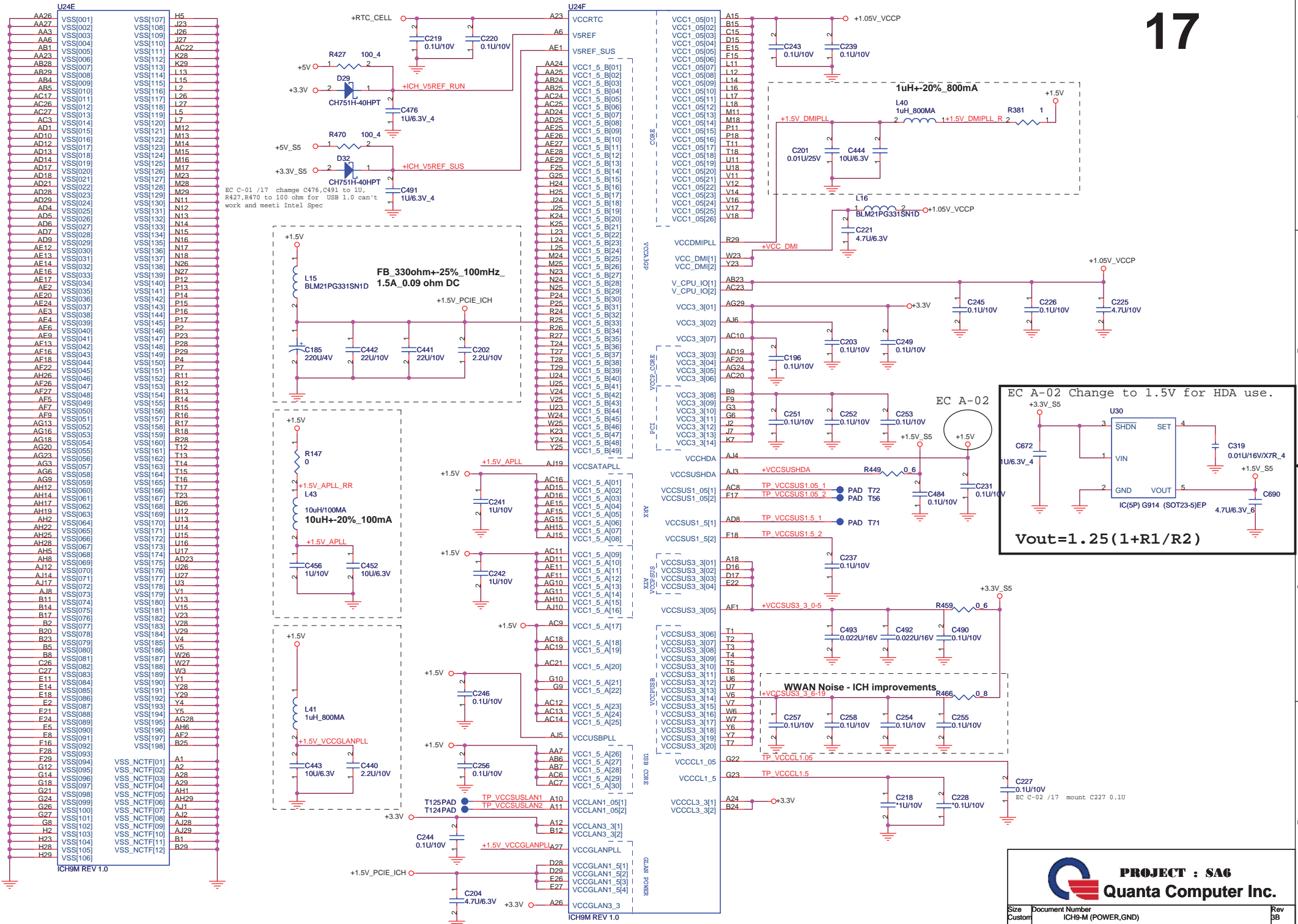


EC A-03 Add R499 Pull high to +3.3V_S5

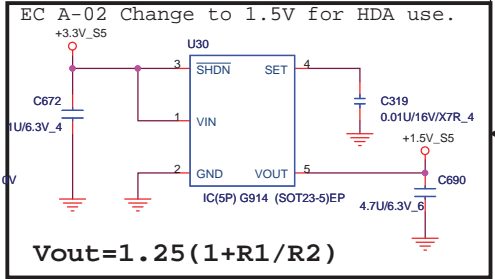


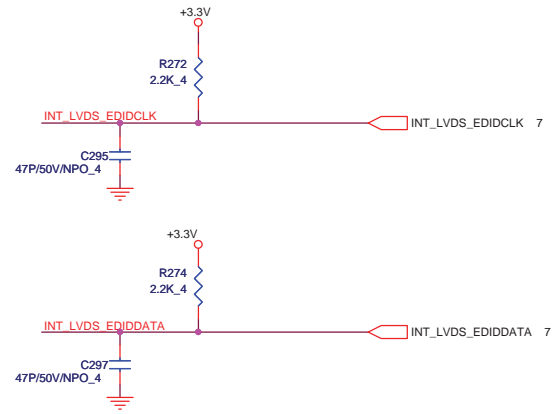
| Board ID | ID3 | ID2 | ID1 | ID0 |
|-----------------|-----|-----|-----|-----|
| INTEL SENTAROSA | 1 | 1 | 1 | 1 |
| INTEL MENTAVIRA | 1 | 1 | 0 | 1 |
| AMD | 1 | 0 | 1 | 1 |
| NVIDIA | 1 | 0 | 0 | 1 |



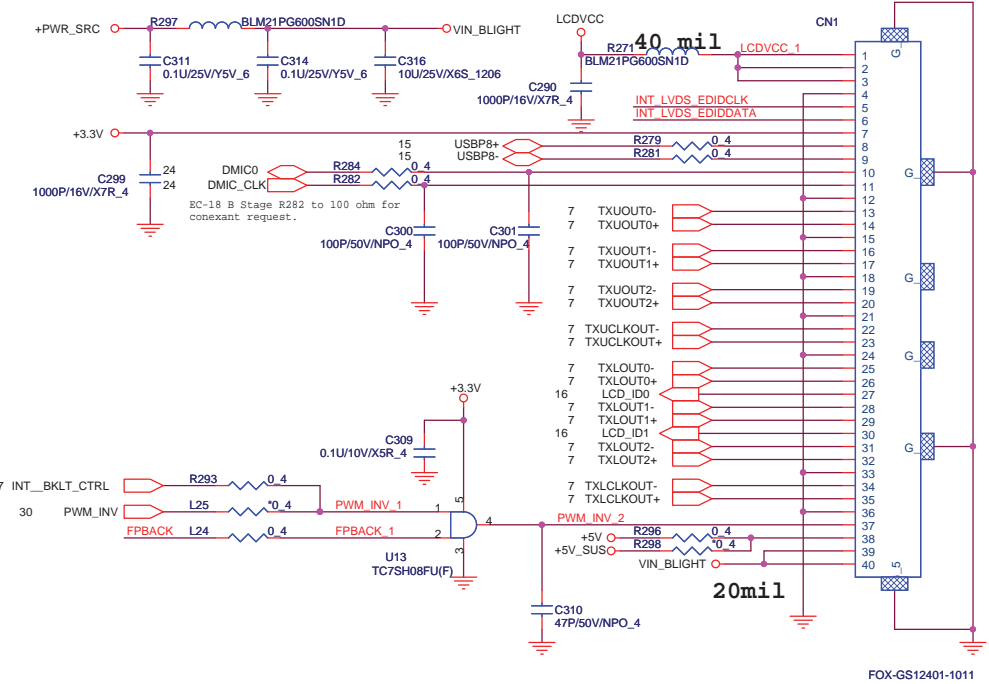


EC C-01 /17 change C476,C491 to 1uH, R427,R470 to 100 ohm for USB 1.0 can't work and meet Intel Spec

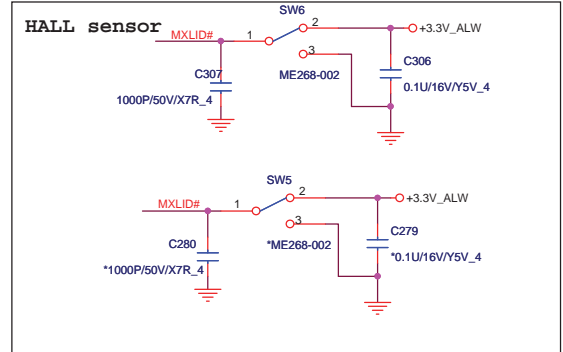
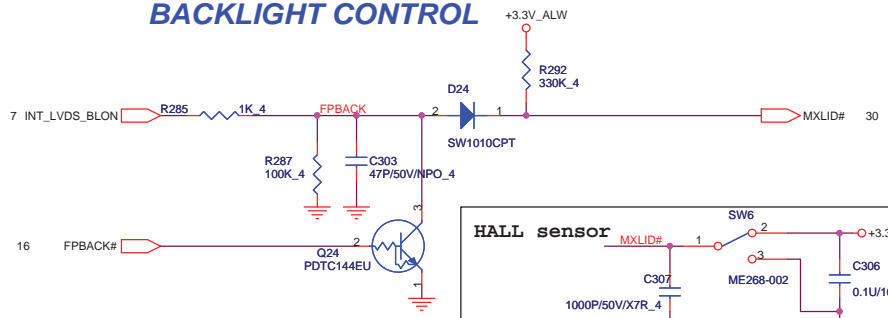




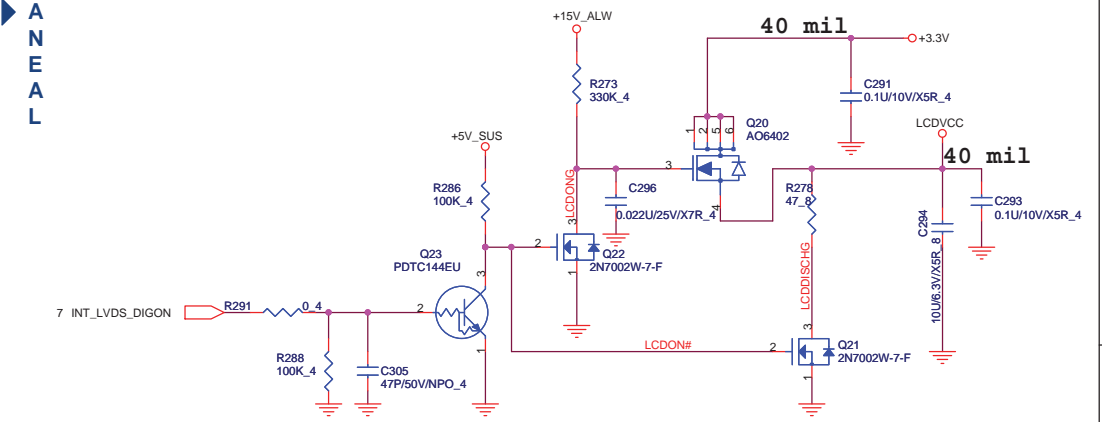
LCD CONNECTOR(Include WEB CAM function)



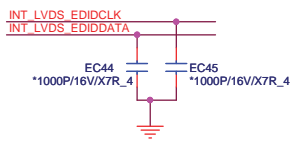
BACKLIGHT CONTROL




PANEL VCC CONTROL



TOP PANEL

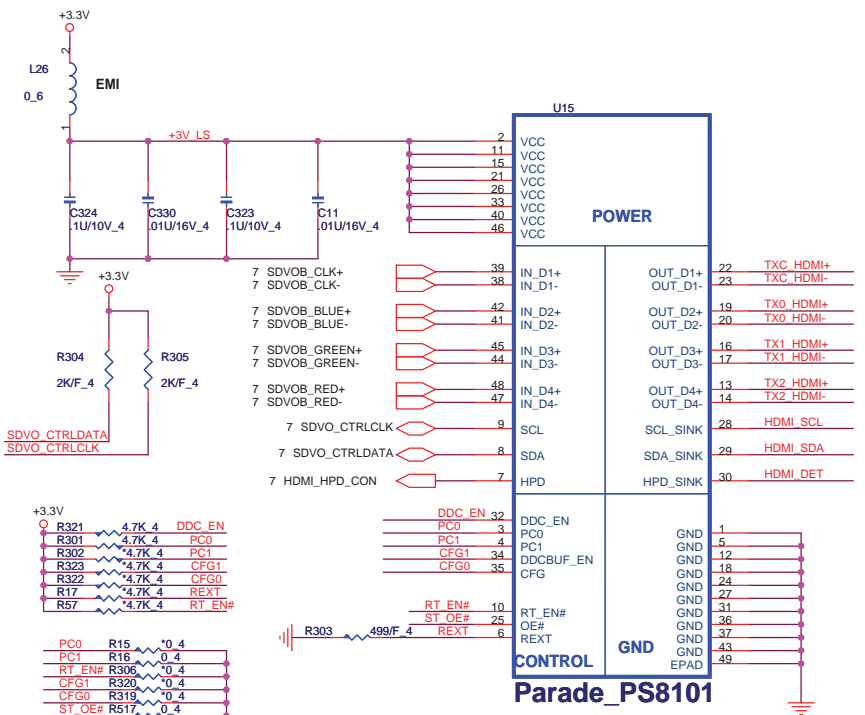




PROJECT : SAG
Quanta Computer Inc.

| | | |
|------------------------------|--|-----------|
| Size Custom | Document Number LVDS/LCD CONN/LID/WEB CAM | Rev 3B |
| Date: Friday, April 25, 2008 | Sheet 18 | of 41 |

For UMA HDMI function

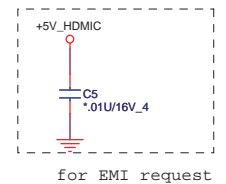
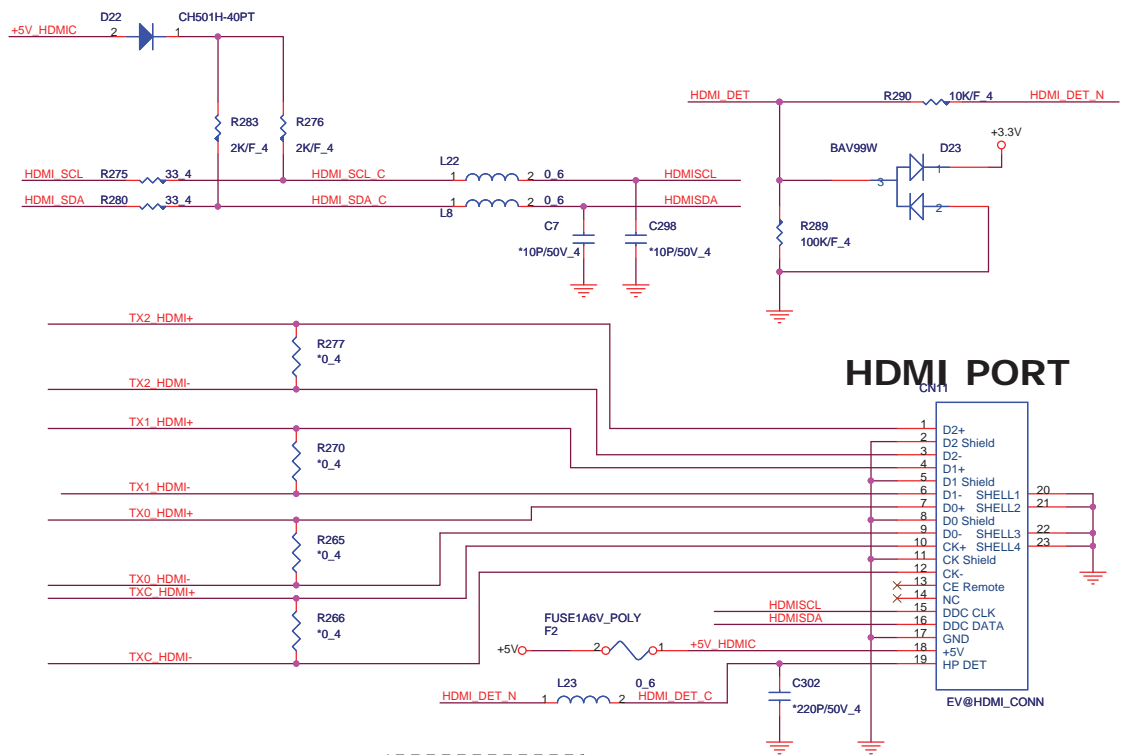


EC C-05 /19 change Pin 25 connect to GND.

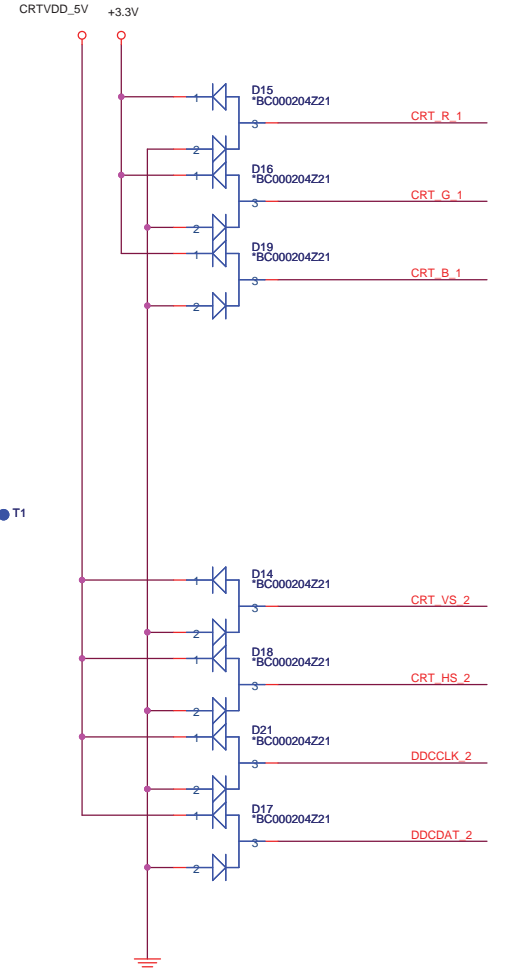
EQUALIZATION SETTING
 PC1:PC0=0:0 8dB
 PC1:PC0=0:1 4dB Recommended
 PC1:PC0=1:0 12dB
 PC1:PC0=1:1 0dB

SCLZ/SDAZ Low-level input/output Voltage
 CFG1:CFG0=0:0 VIL:<0.4V VOL:0.6V (Default)
 CGF1:CGF0=0:1 VIL:<0.36V VOL:0.55V
 CGF1:CGF0=1:0 VIL:<0.44V VOL:0.65V
 CGF1:CGF0=1:1 VIL:<0.36V VOL:0.6V

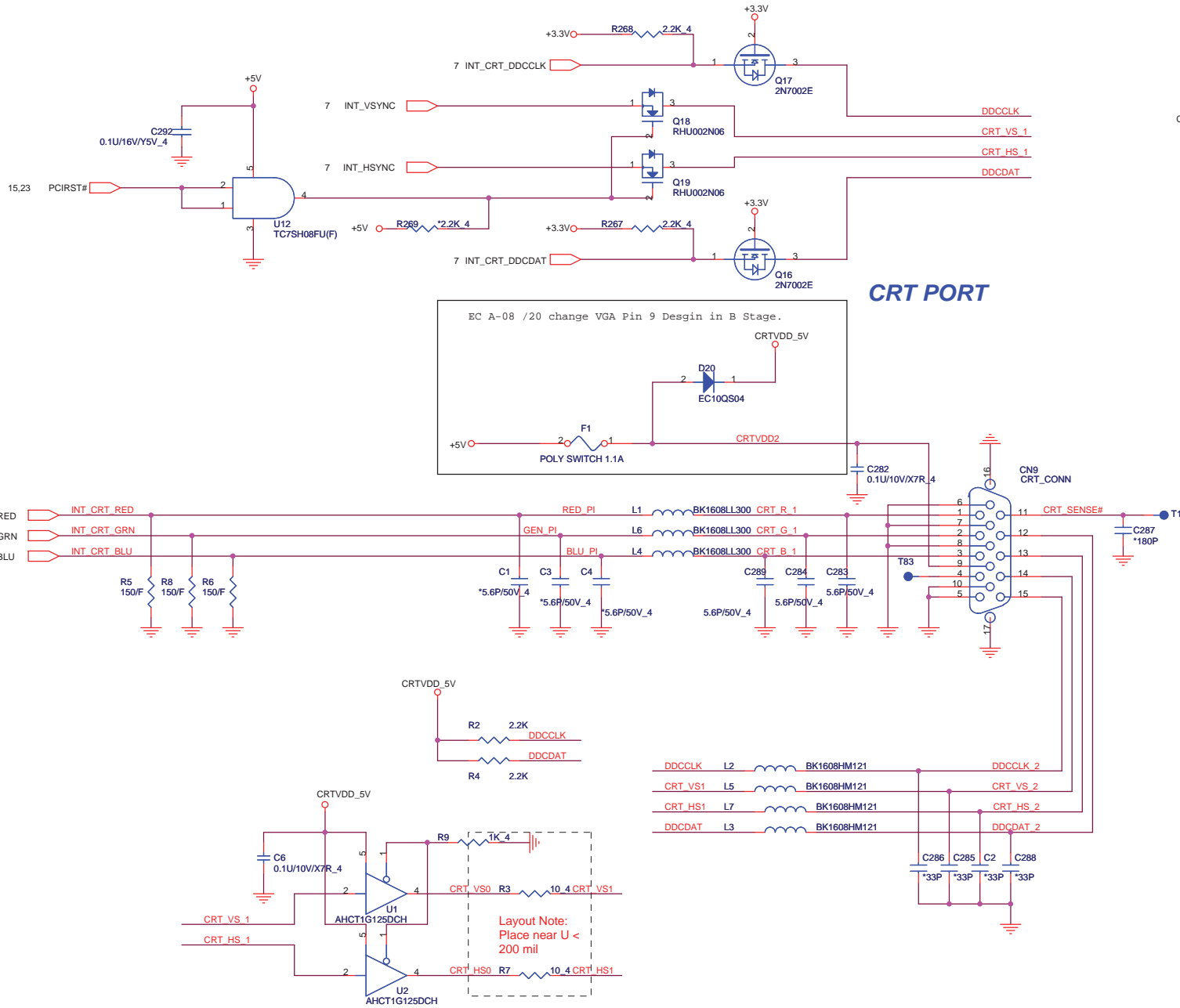
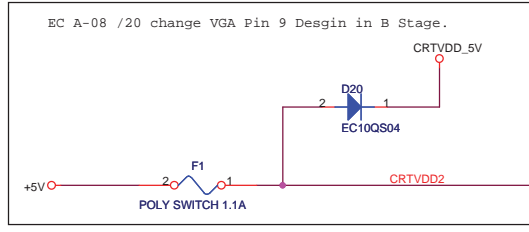
Use Pericom ST
 Add R15,R16,R306,R319,R320 0 ohm. R303 4.7K
 R277,R270,R265,R266 mount 0.2P.



ESD PORTECTION

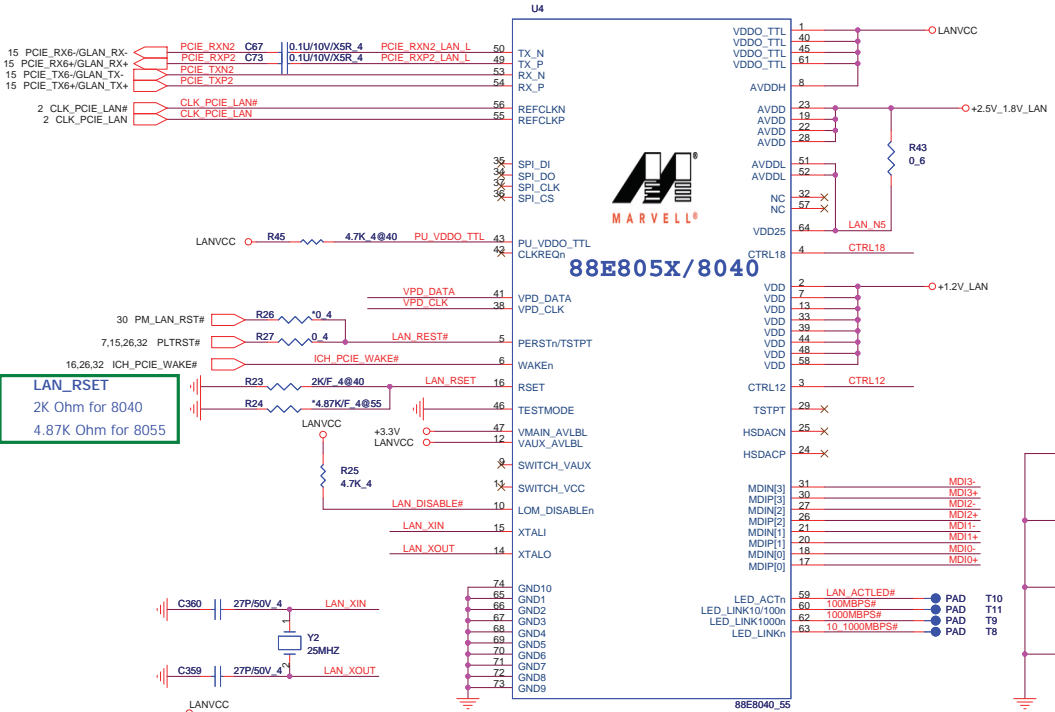


CRT PORT



PROJECT : SA6
Quanta Computer Inc.

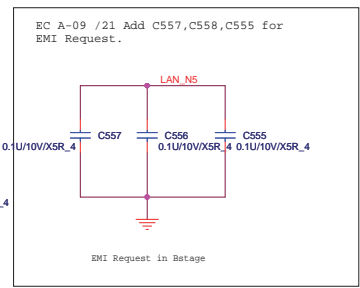
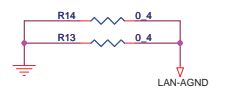
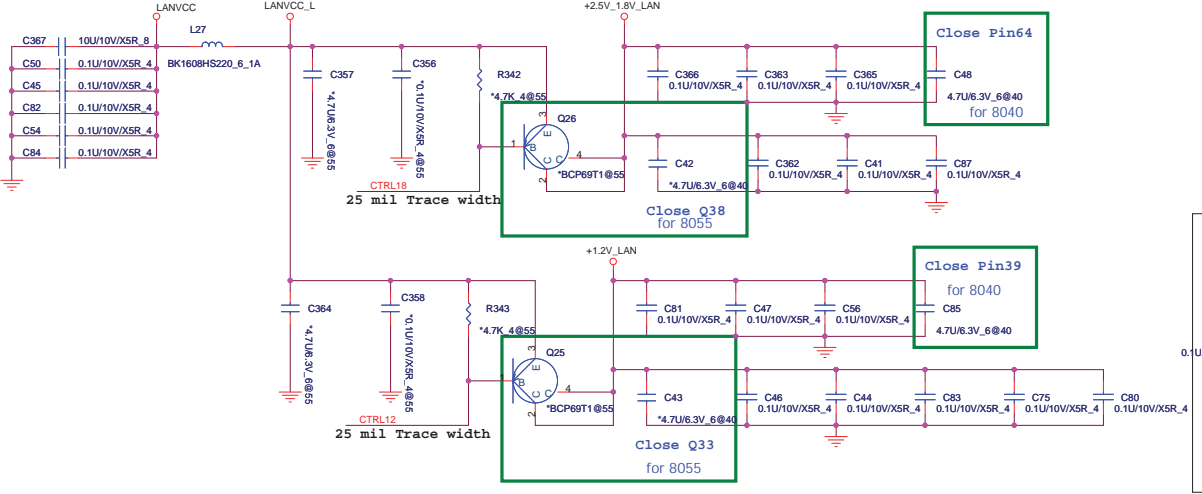
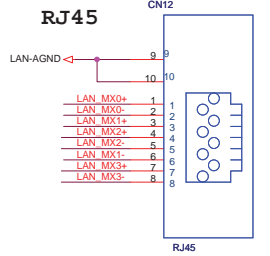
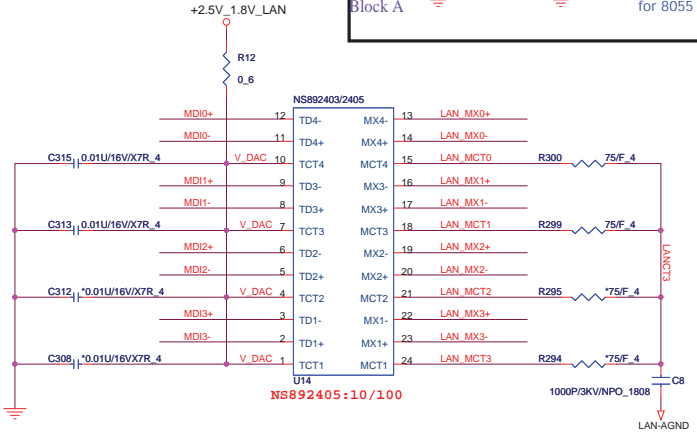
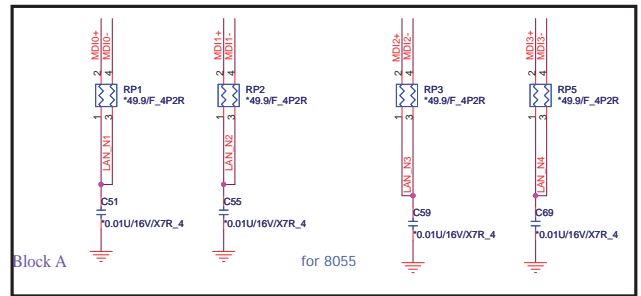
| | | |
|--------|------------------------|----------------|
| Size | Document Number | Rev |
| Custom | CRT PORT | 3B |
| Date: | Friday, April 25, 2008 | Sheet 20 of 41 |




LAN_RSET
2K Ohm for 8040
4.87K Ohm for 8055

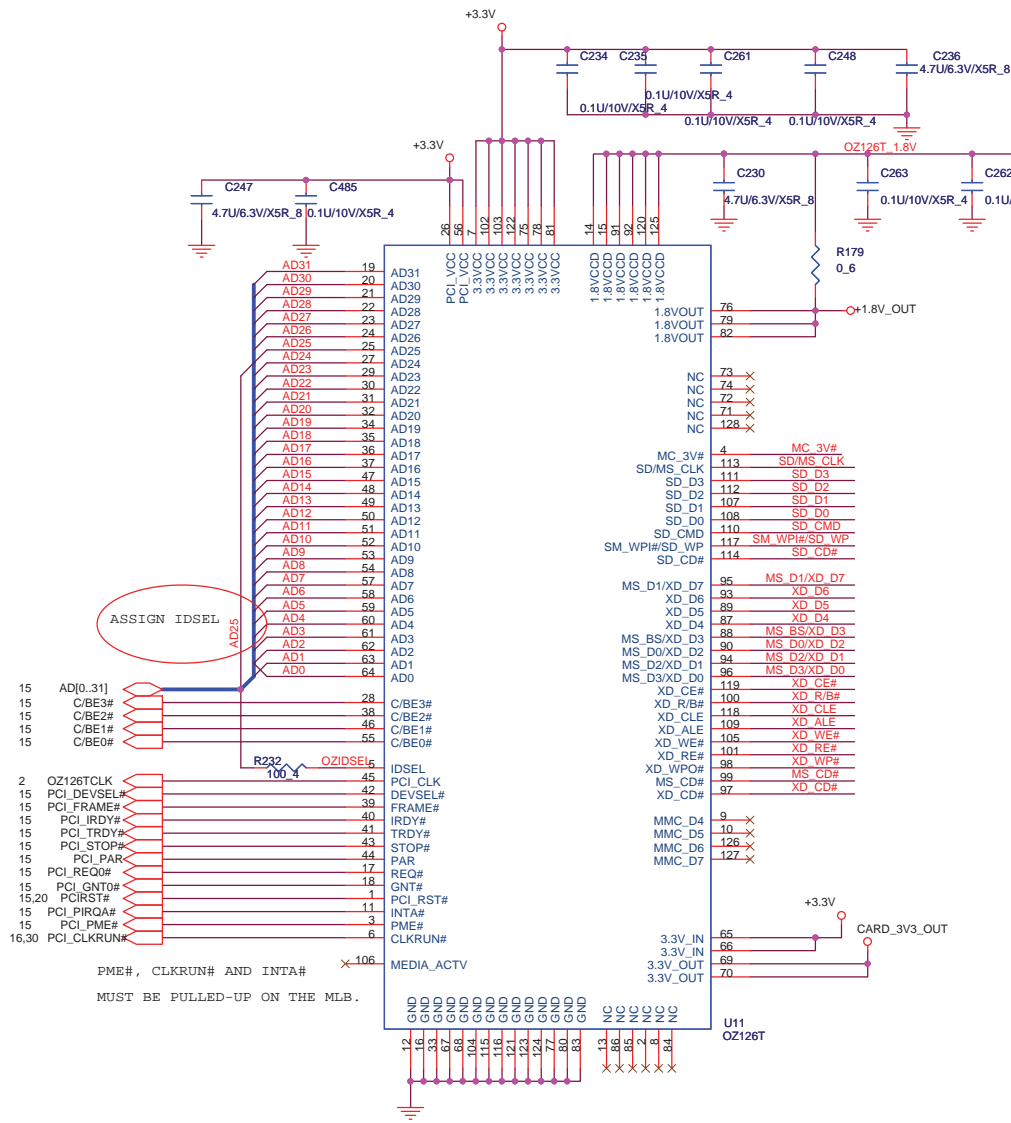
EEPROM No Use
VPD_DATA Pull Down
Rev:B use BIOS

| | ASM | No ASM |
|----------|-------------------|-------------------|
| Use BIOS | R338 | R340, R339,U17 |
| EEPROM | R340, R339,U17 | R338 |

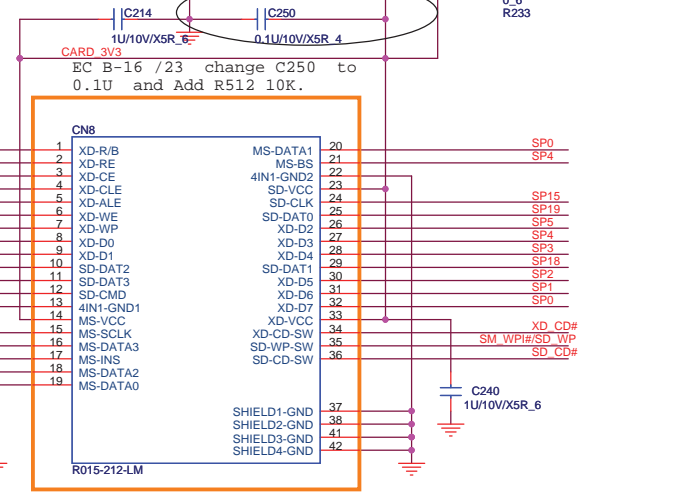
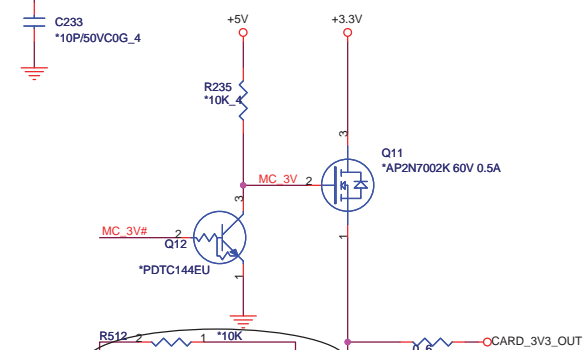
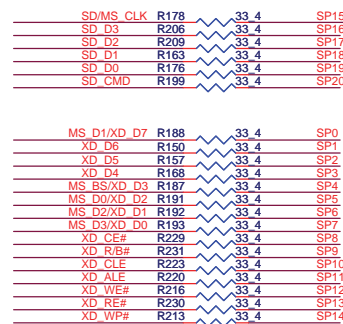


| | ASM | No ASM |
|---------|---------------|--|
| 88E8040 | C48, C85, R23 | RP1,RP2,RP3,RP5 C51,C55,C59,C69 C312,C308 Q25,Q26,C42,C43 R524,R294,R295 U4(8040),U14 10/100 C356,C357,C358,C364,R342,R343 |
| 88E8055 | | C48, C85, R23 |

| | | |
|---|------------------------|----------------|
|  | | |
| PROJECT : SAG | | |
| Quanta Computer Inc. | | |
| Size | Document Number | Rev |
| C | LAN Power | BB |
| Date: | Friday, April 25, 2008 | Sheet 22 of 41 |



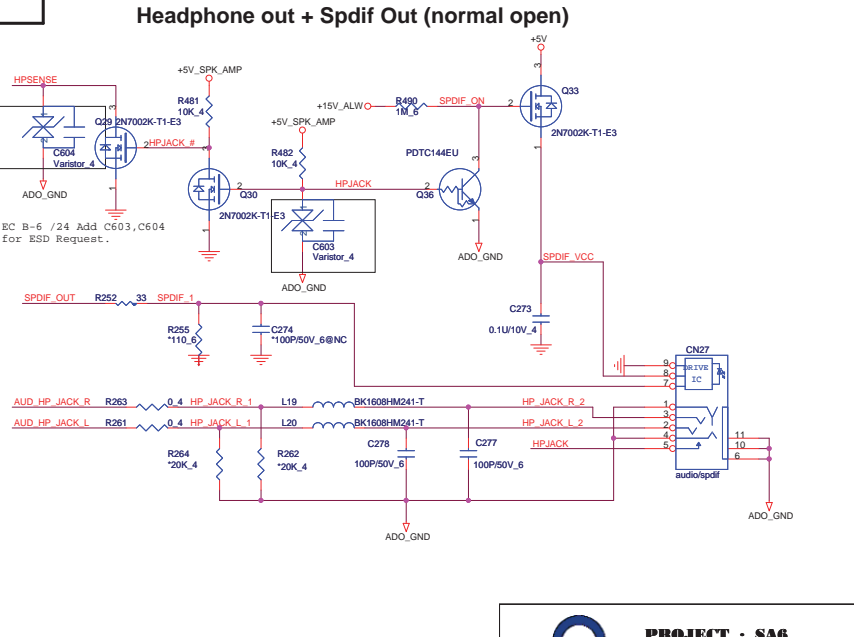
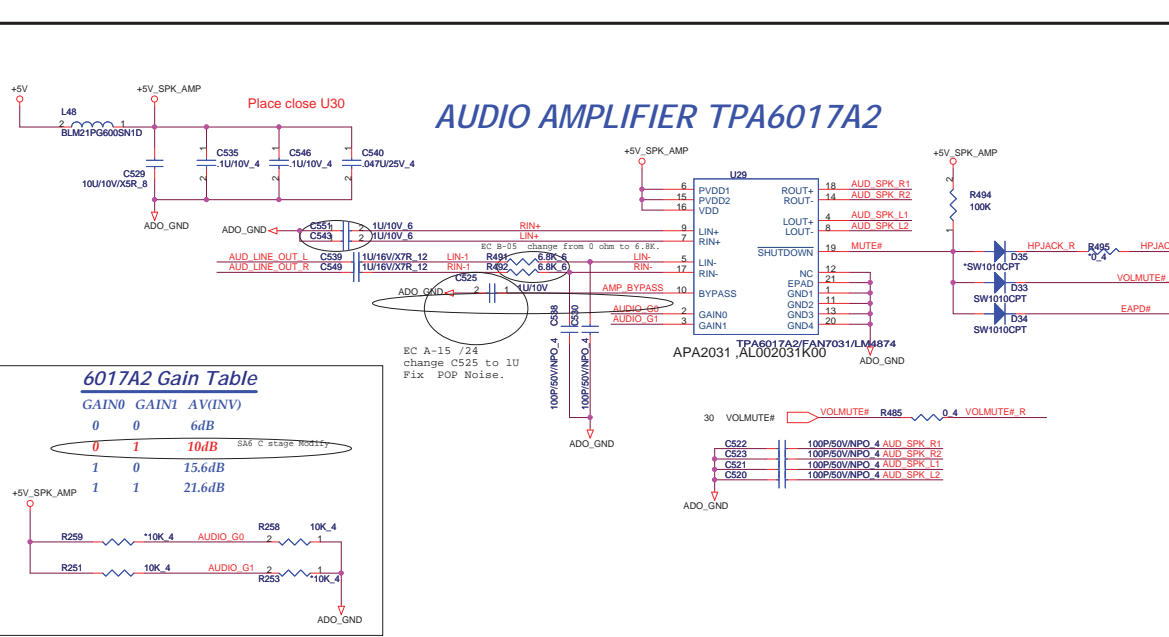
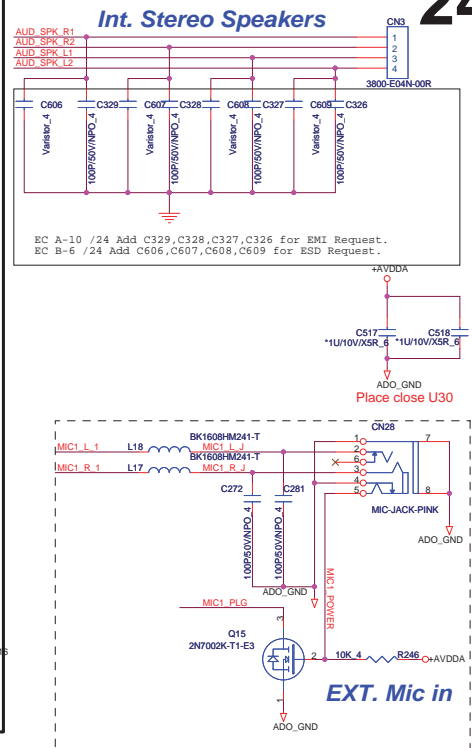
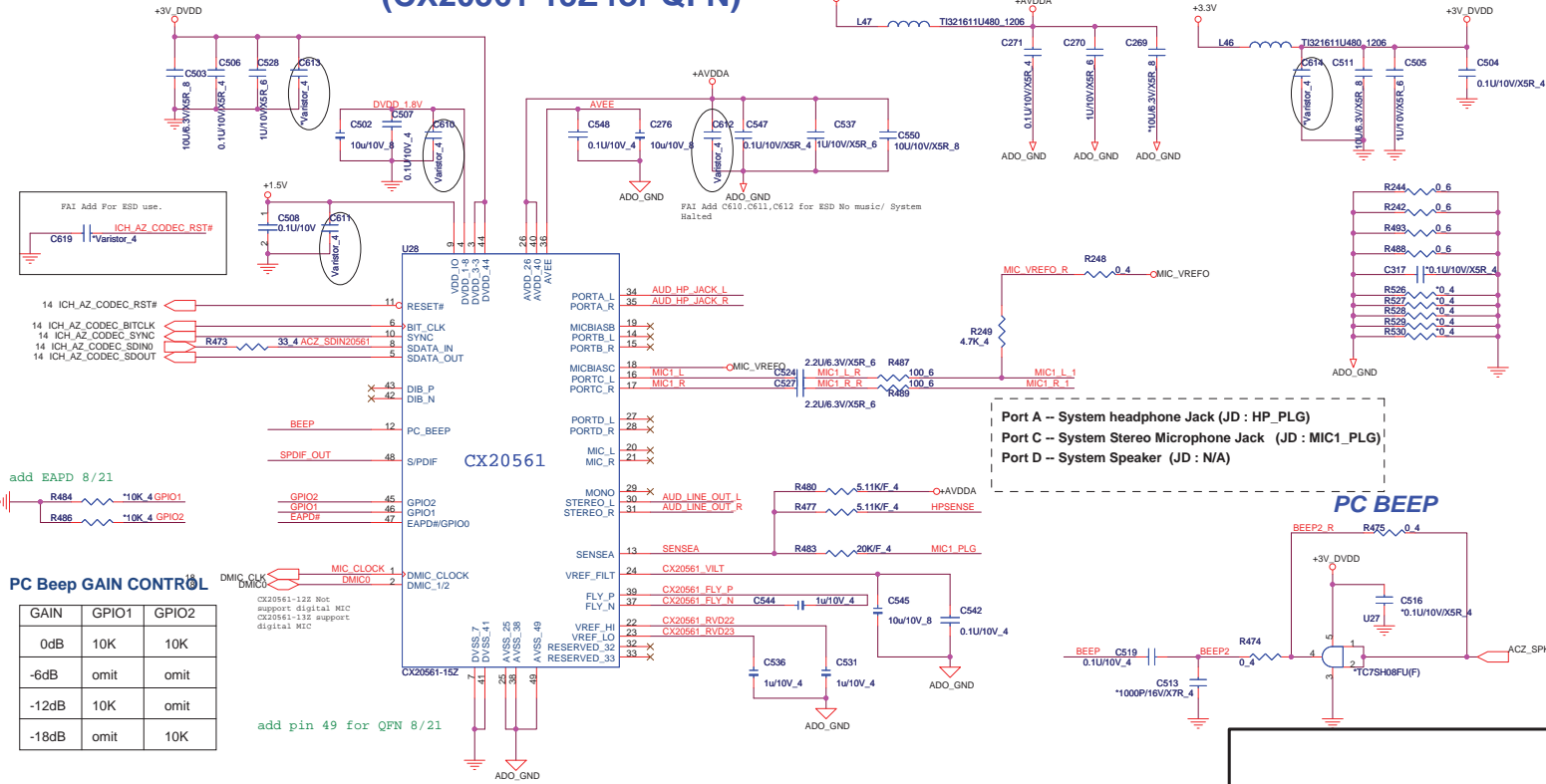
NOTE: PLACE R9 - R29 NEAR CONNECTORS



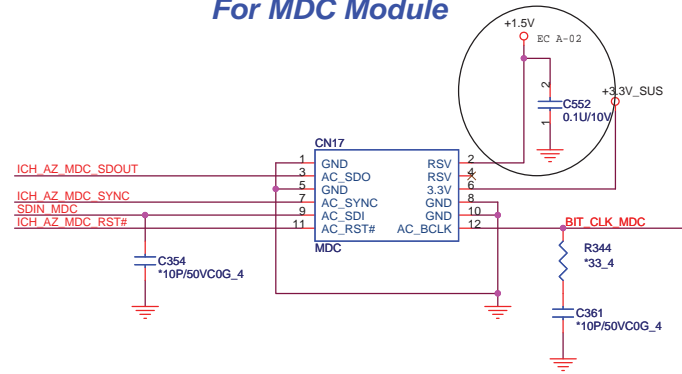
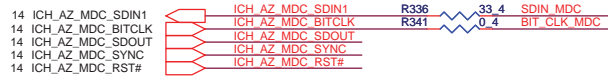
PROJECT : SA6
Quanta Computer Inc.

Size: Custom Document Number: OZ126T Rev: B8
 Date: Friday, April 25, 2008 Sheet 23 of 41

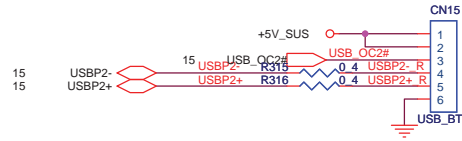
(CX20561-15Z for QFN)



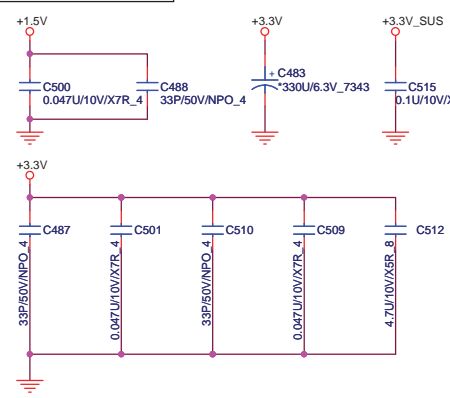
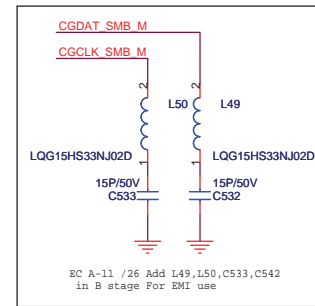
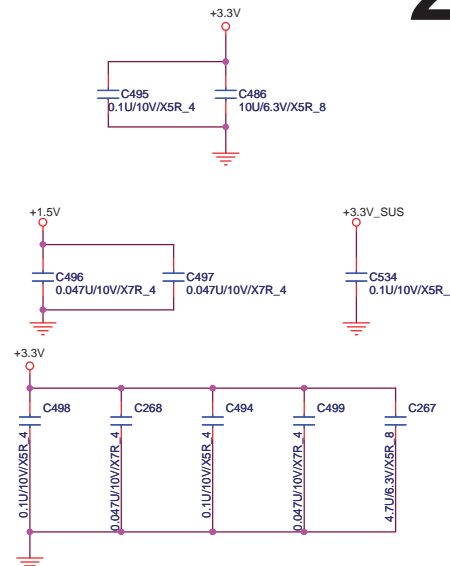
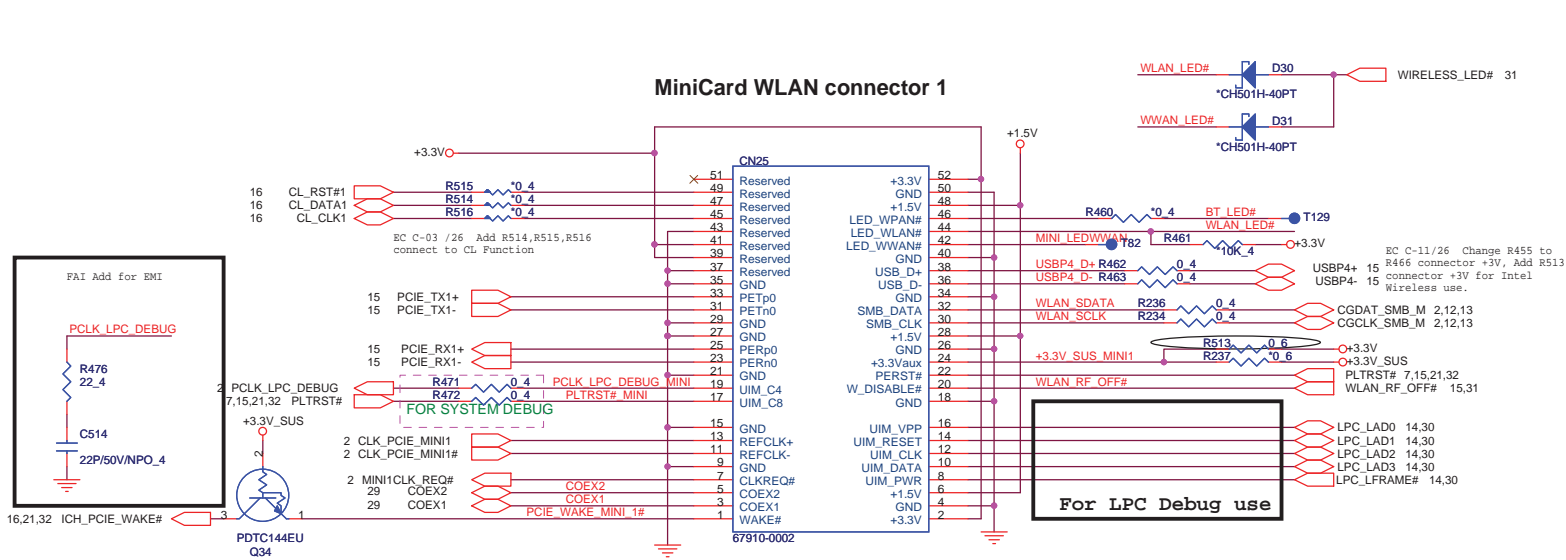
For MDC Module



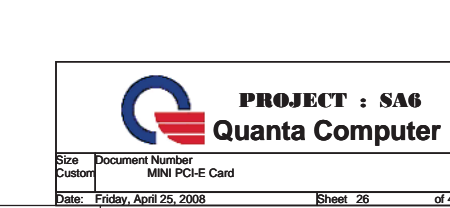
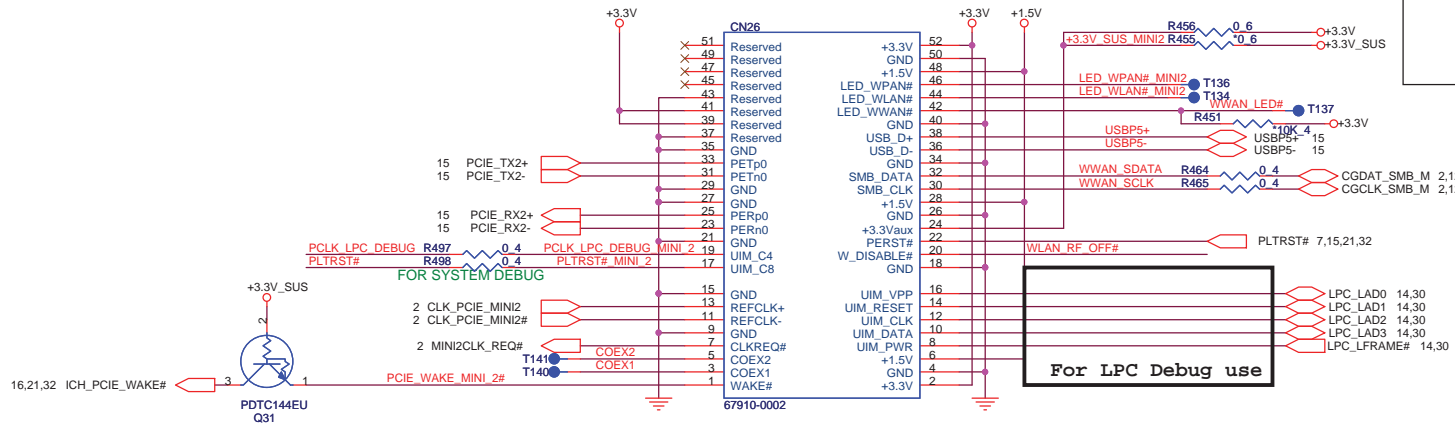
TO RJ11/USB PORT



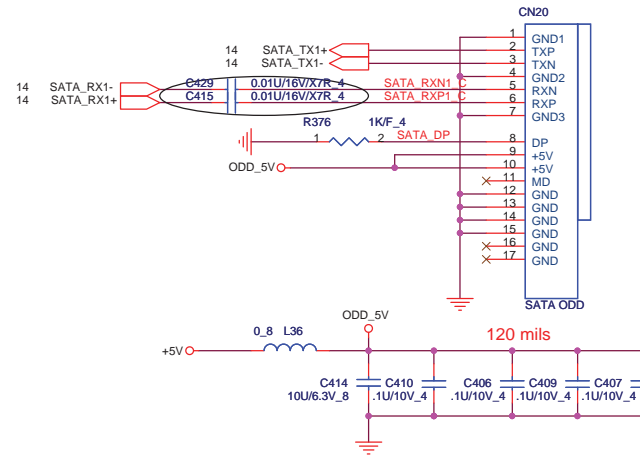
MiniCard WLAN connector 1



MiniCard connector 2

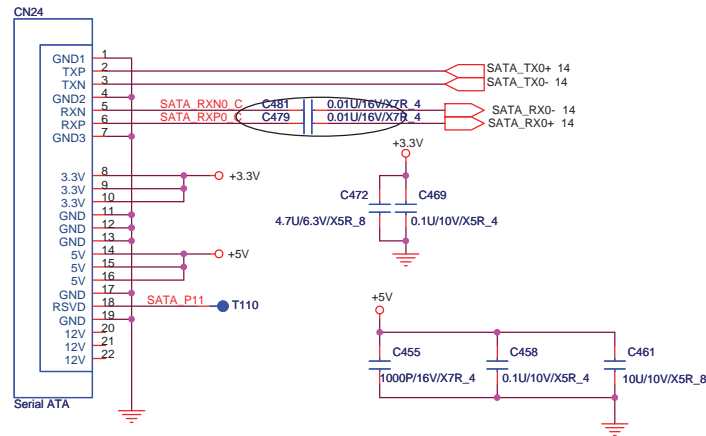


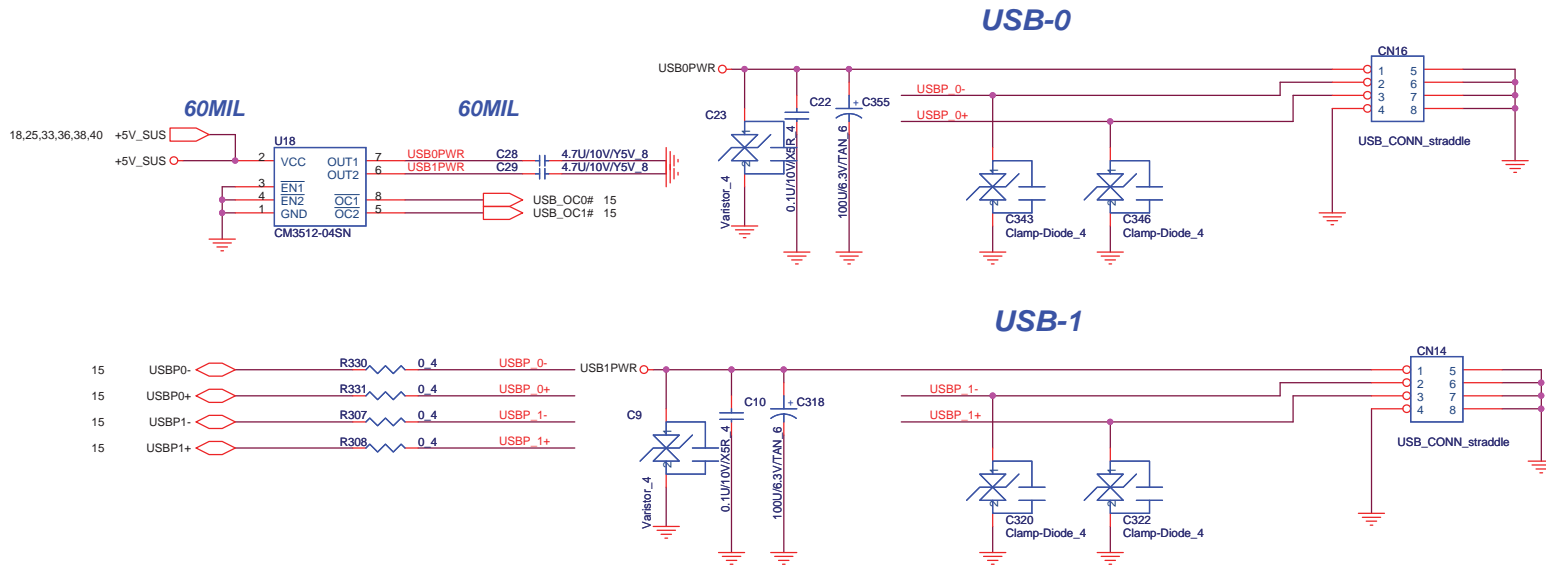
SATA CD-ROM




EC C-06 /27 change C479,C481,C415,C429 to 0.01U for meet Intel Spc.

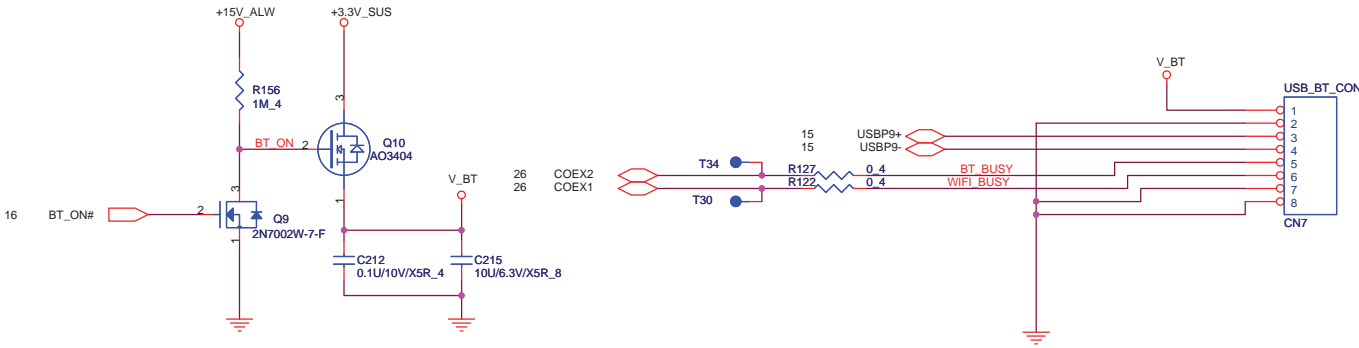
SATA CONNECTOR



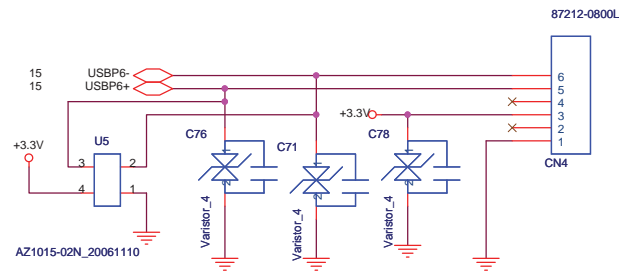


| | | | | |
|---|--|----------|-----------------|-------|
|  PROJECT : SA6 Quanta Computer Inc. | | Size | Document Number | Rev |
| | | Custom | USB CONN | 5B |
| Date: Friday, April 25, 2008 | | Sheet 28 | | of 41 |

BLUETOOTH CONNECTOR

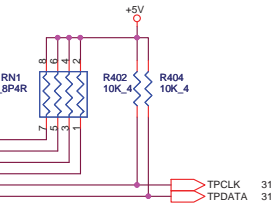
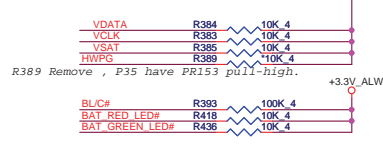
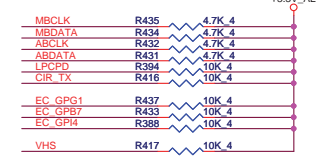
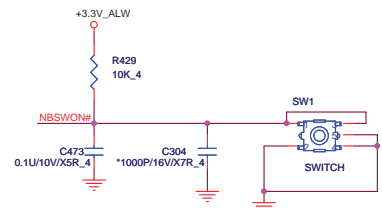


FINGERPRINT CONNECTOR

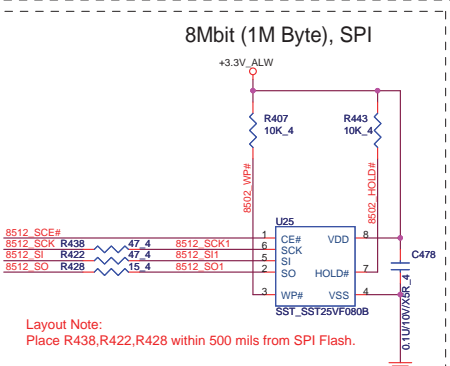
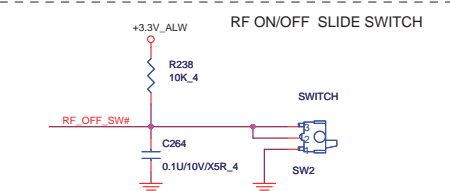
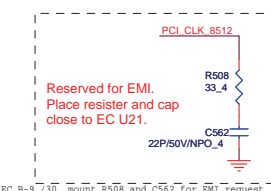
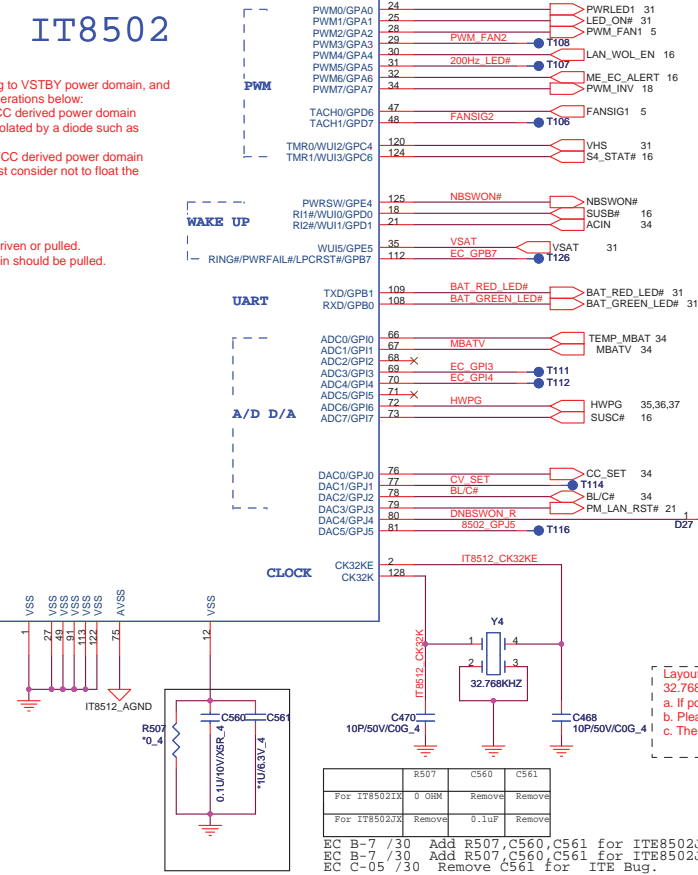
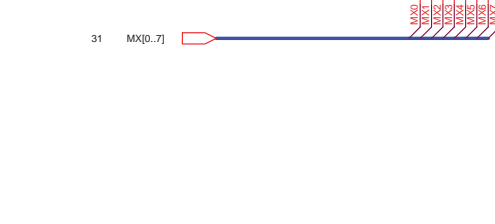
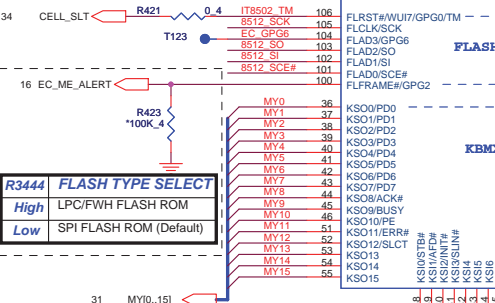
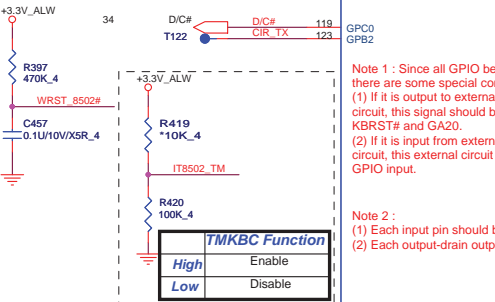
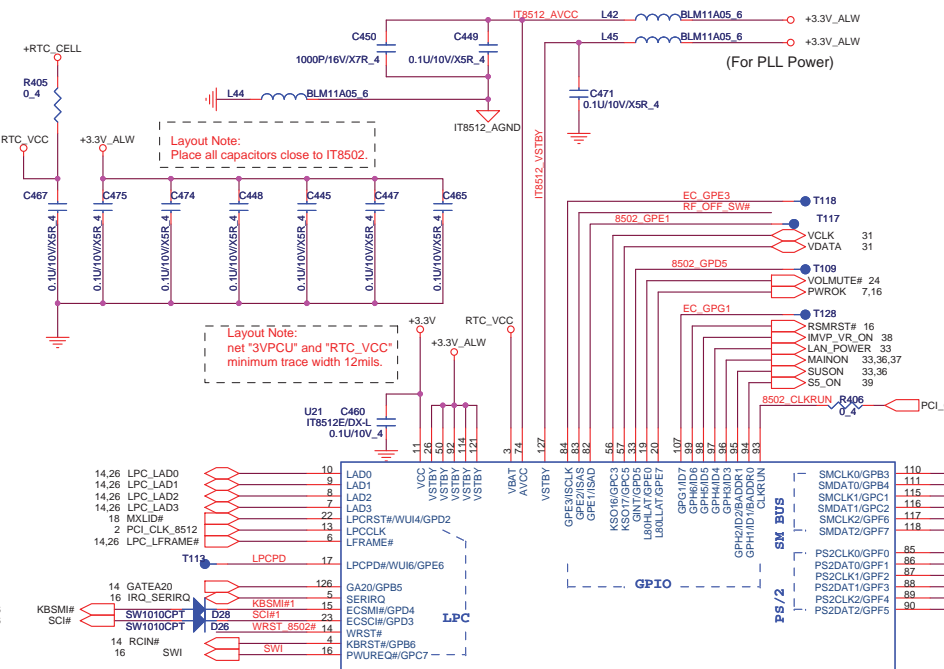


EC B-18 /29 Mount C71,C76 for ESD.

POWER SWITCH



IT8502



Layout Note:
32.768KHz clock lines:
a. If possible, please avoid using any through-hole.
b. Please make the trace length short, and the trace width wide enough.
c. The spacing to the closest neighbor should be wide enough.

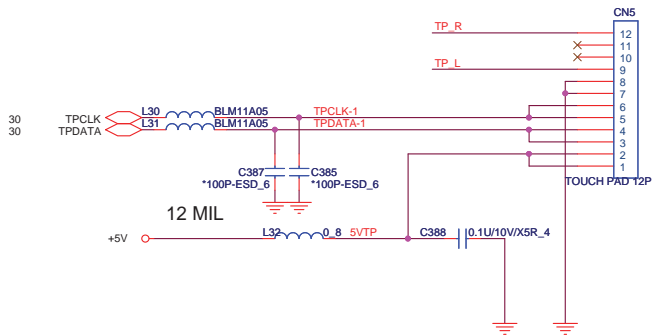
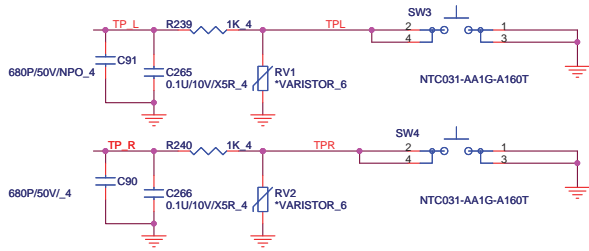
| Part | Value | Comment |
|------|--------|---------|
| R507 | 0 OHM | Remove |
| C560 | 0.1uF | Remove |
| C561 | Remove | Remove |

EC B-7 /30 Add R507,C560,C561 for ITE8502JX use.
EC B-7 /30 Add R507,C560,C561 for ITE8502JX use.
EC C-05 /30 Remove C561 for ITE Bug.

PROJECT : SAG
Quanta Computer Inc.

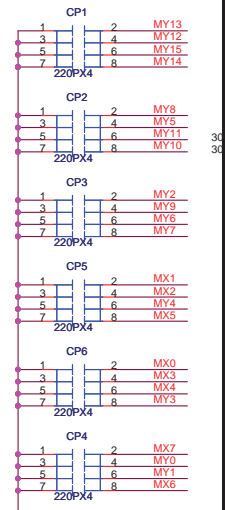
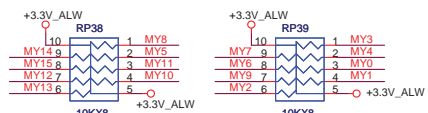
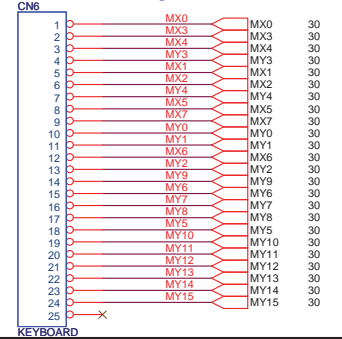
| | | |
|------------------------------|------------------|-------|
| Size | Document Number | Rev |
| Custion | Doc = KBC-IT8502 | BB |
| Date: Friday, April 25, 2008 | Sheet 30 | of 41 |

TOUCHPAD SWITCH CONN

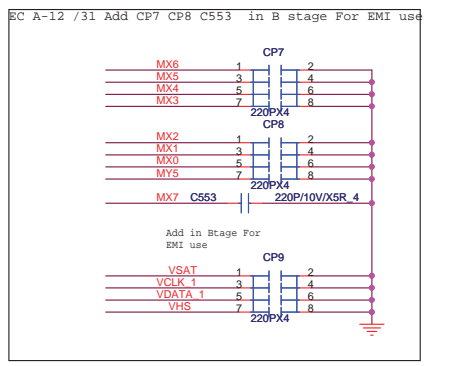
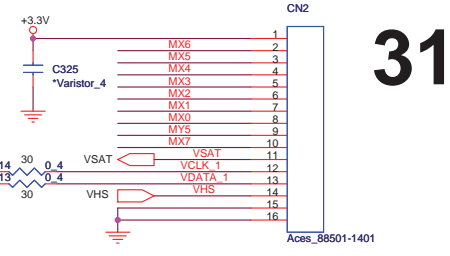
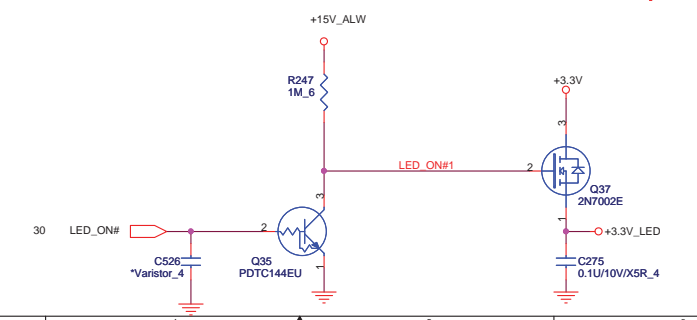
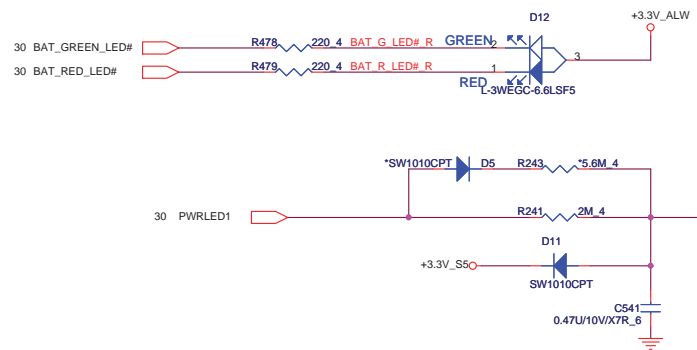
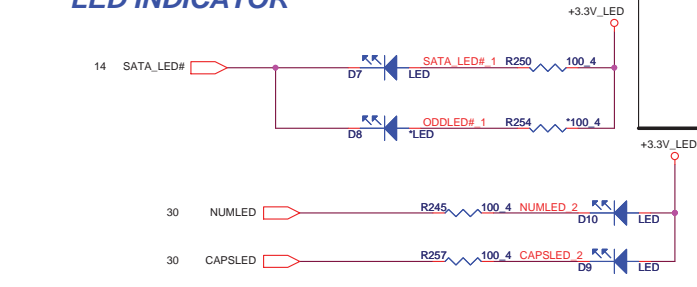


KEYBOARD

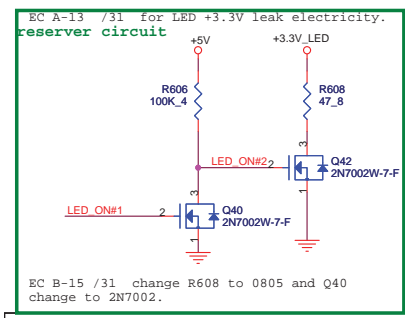
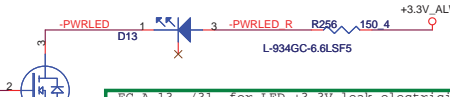
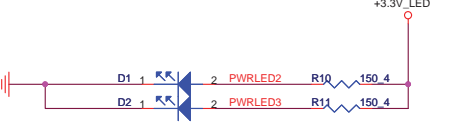
For New Keyboard use.



LED INDICATOR



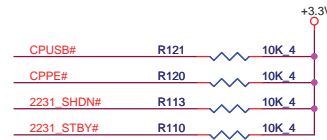
SWITCH/Volume cintral BOARD



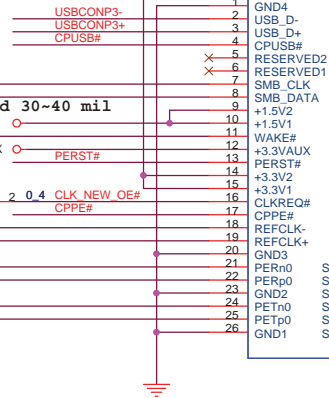
PROJECT : SA6
Quanta Computer Inc.

| | | |
|------------------------------|-------------------------------|--------|
| Size Custom | Document Number TP/KB/LED/MBB | Rev 8B |
| Date: Friday, April 25, 2008 | Sheet 31 | of 41 |

NEWCARD



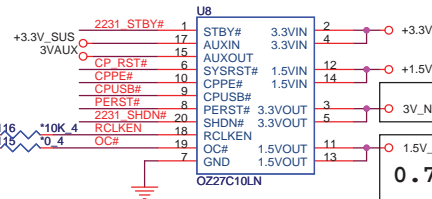
1.35A need 60 mil 3V_NEWCARD



2,16 ICH_SMBCLK
2,16 ICH_SMBDATA
16,21,26 ICH_PCIE_WAKE#

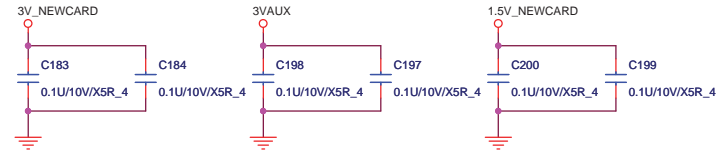
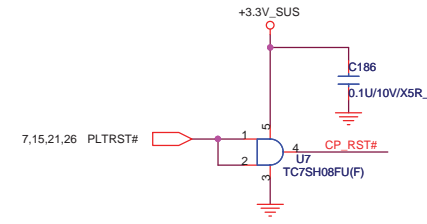
2 NEW-CARD_CLK_REQ#
2 CLK_PCIE_NEW_C#
2 CLK_PCIE_NEW_C
15 PCIE_RXN3
15 PCIE_RXP3
15 PCIE_TXN3
15 PCIE_TXP3

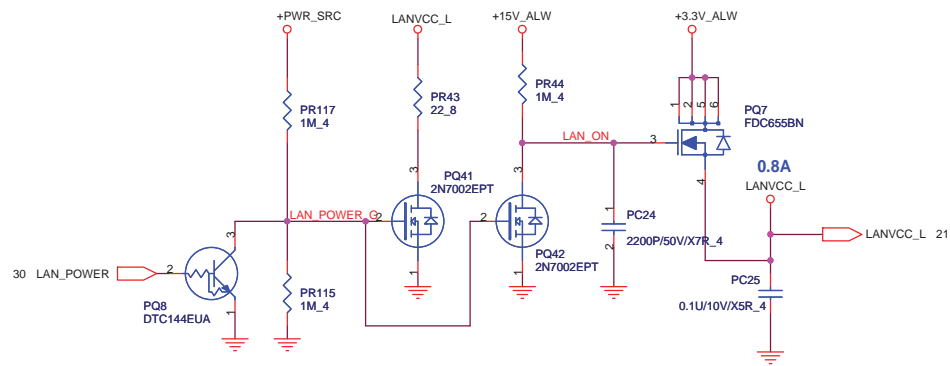
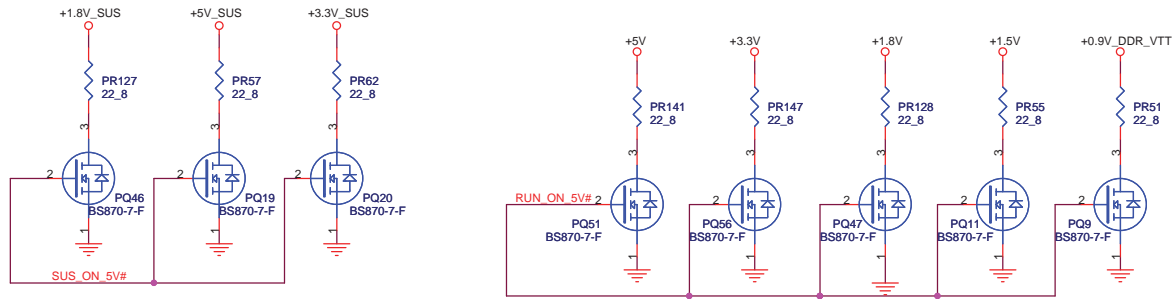
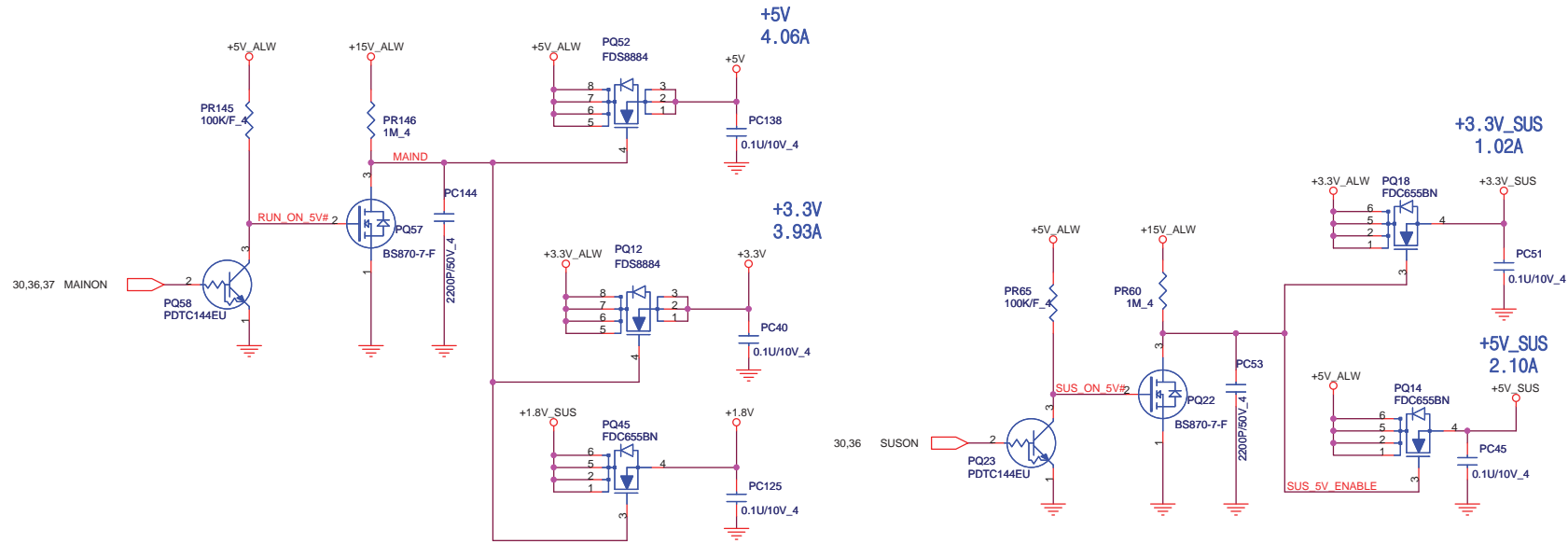
0.75A need 30~40 mil
3VAUX
1.5V_NEWCARD




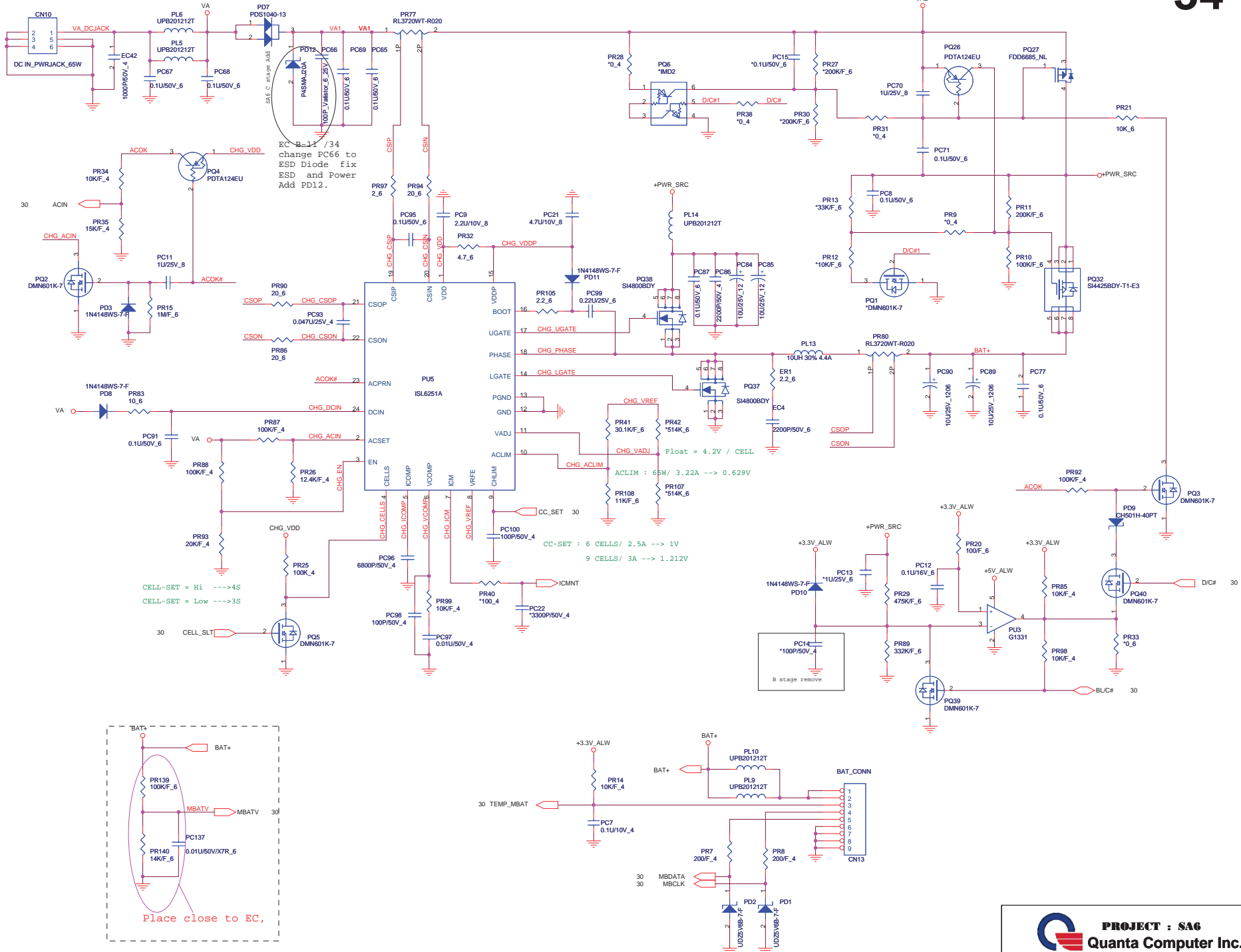
1.35A need 60 mil

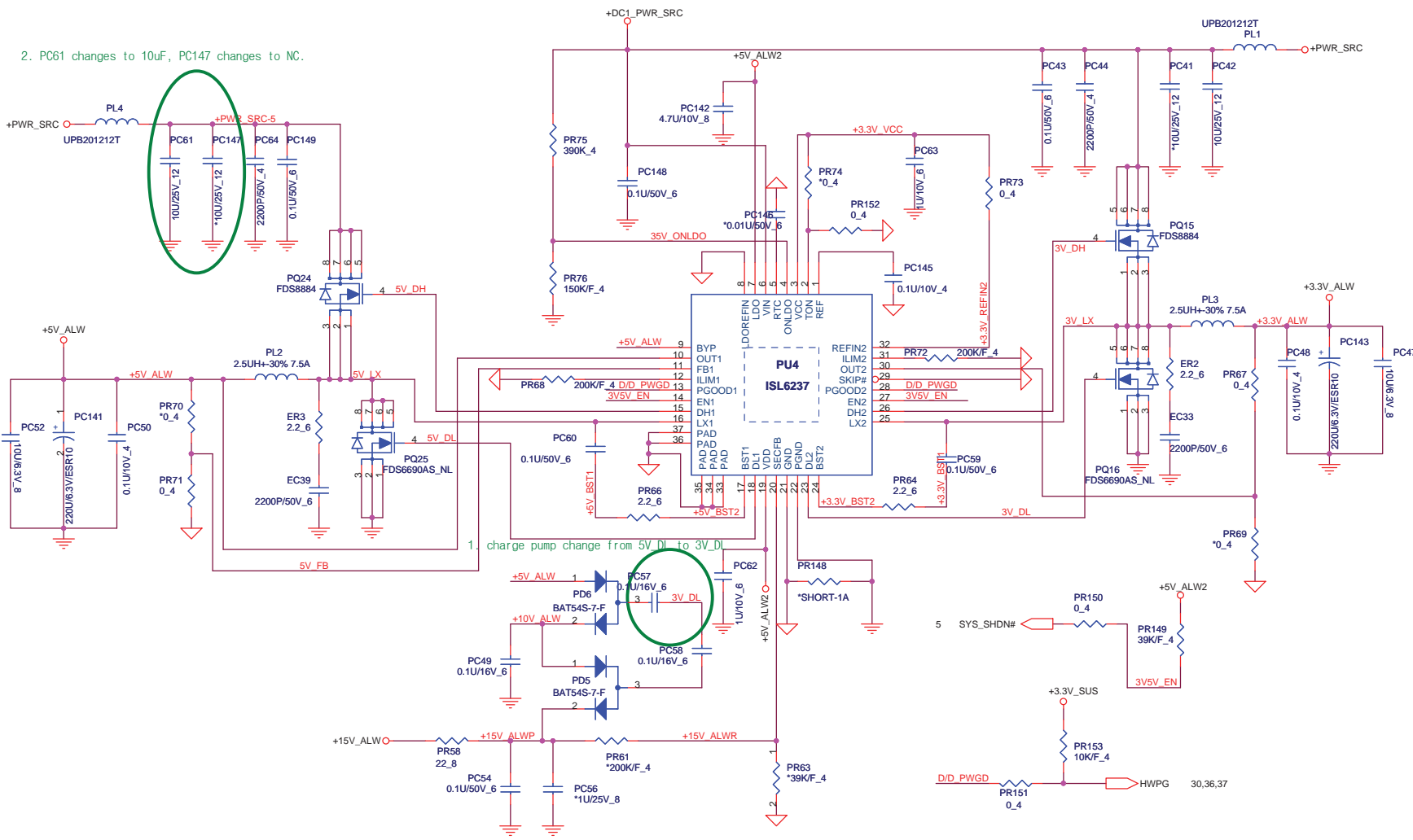
0.75A need 30~40 mil





| | | |
|---|---------------------------|----------------|
|  PROJECT : SA6 Quanta Computer Inc. | | |
| Size | Document Number | Rev |
| Custom | RUN POWER SW & DISCHARGER | 3B |
| Date: | Friday, April 25, 2008 | Sheet 33 of 41 |



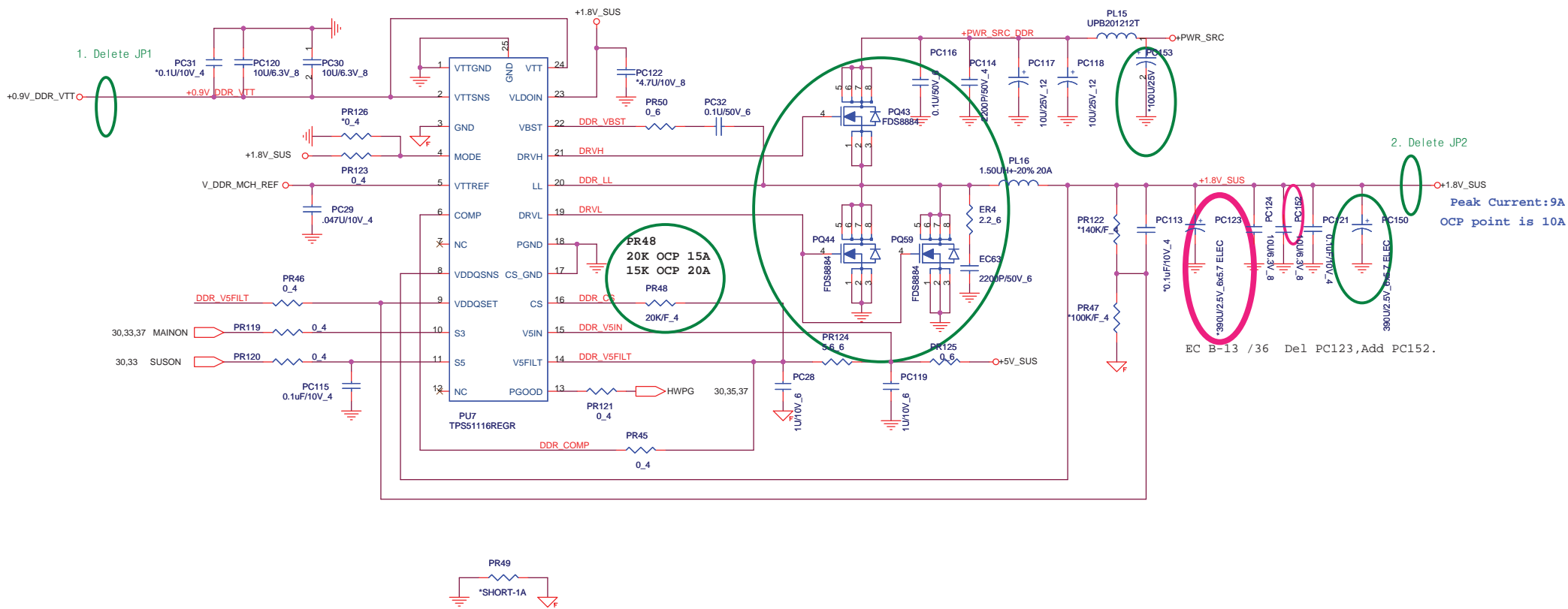


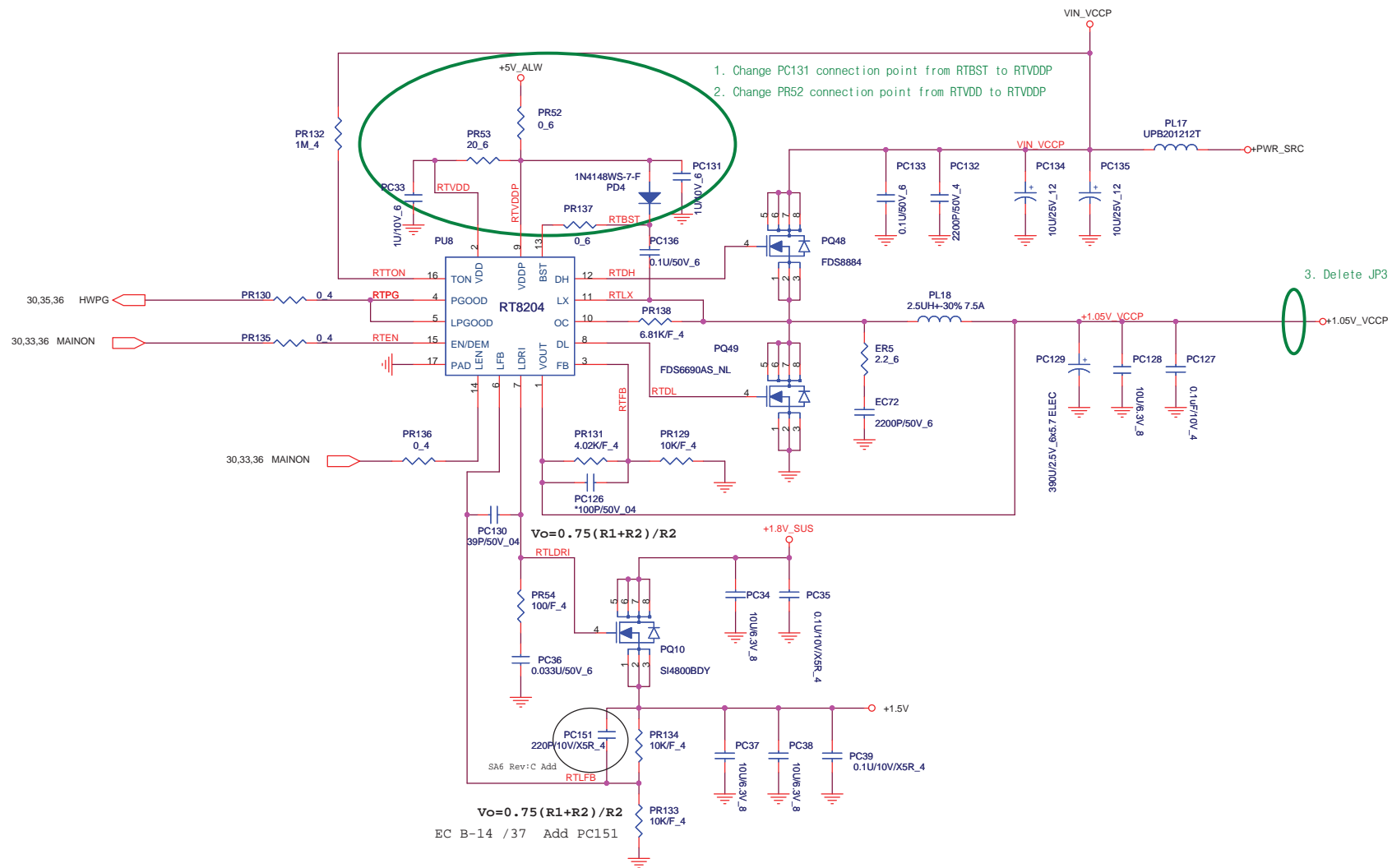
2. PC61 changes to 10uF, PC147 changes to NC.

1. charge pump change from 5V DL to 3V DL

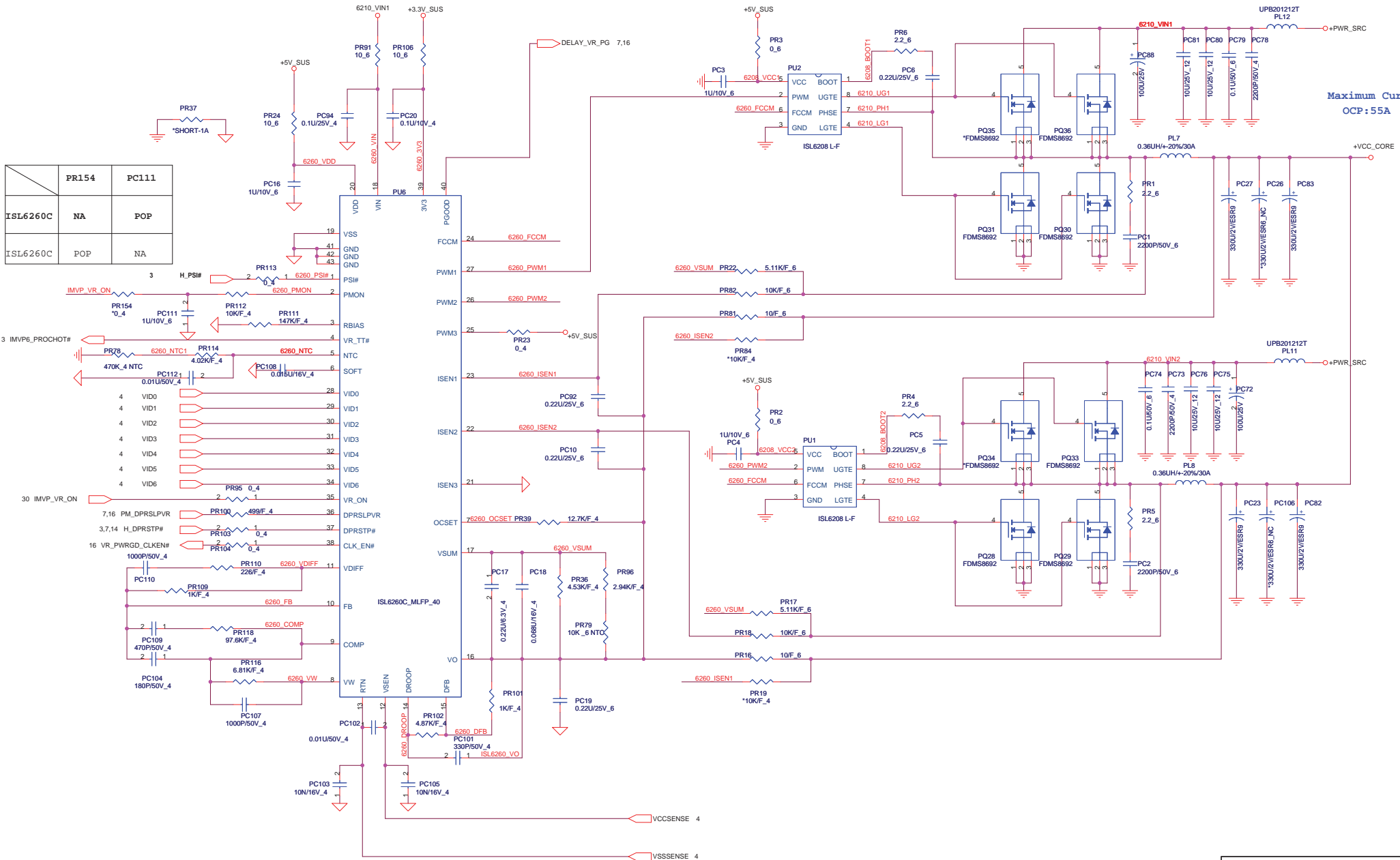
PROJECT : SA6
Quanta Computer Inc.

| | | |
|------------------------------|-----------------|-------|
| Size | Document Number | Rev |
| Custom | D/D POWER | 3B |
| Date: Friday, April 25, 2008 | Sheet 35 | of 41 |





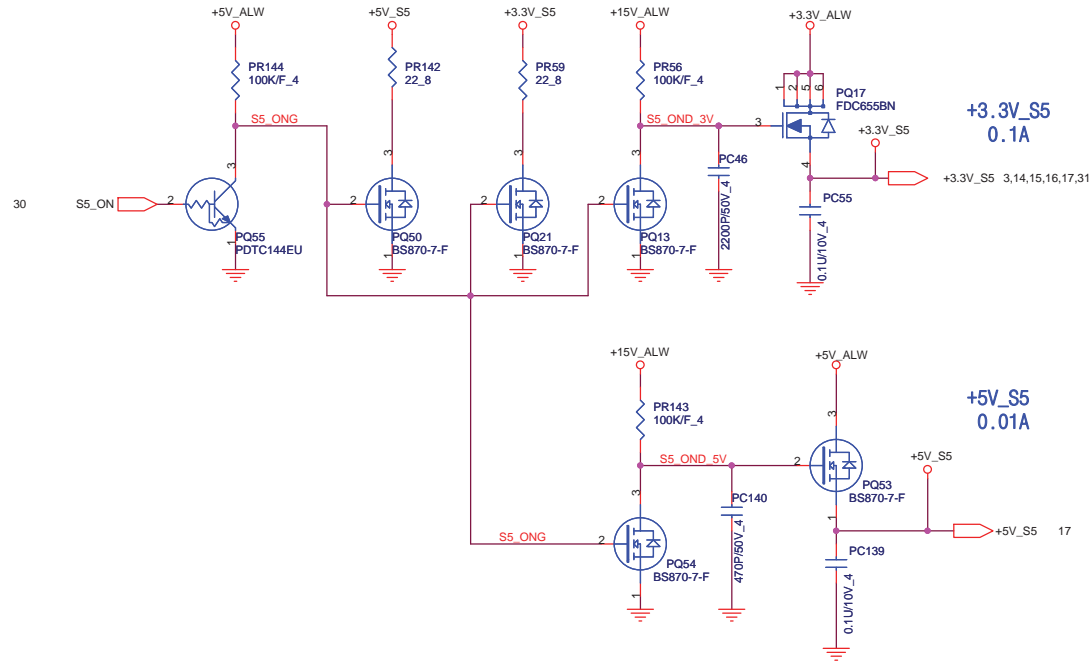
| | | |
|----------|-------|-------|
| | PR154 | PC111 |
| ISL6260C | NA | POP |
| ISL6260C | POP | NA |

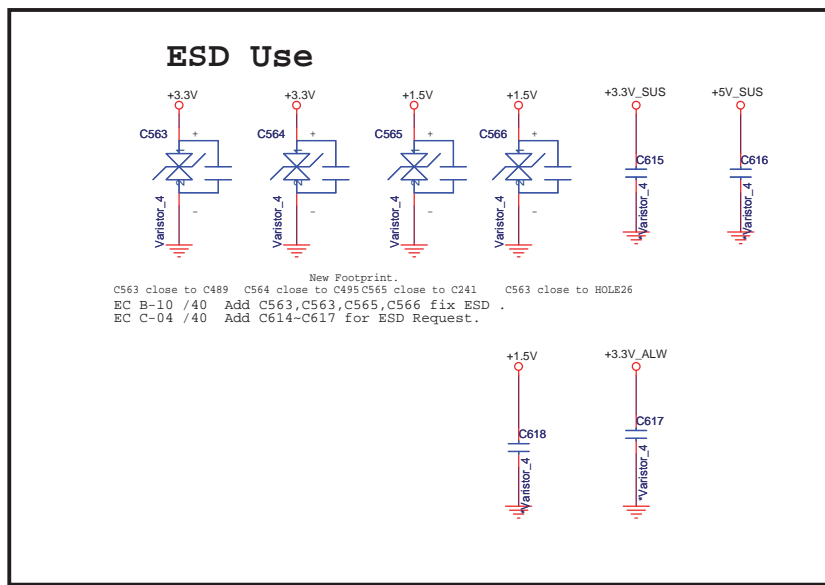
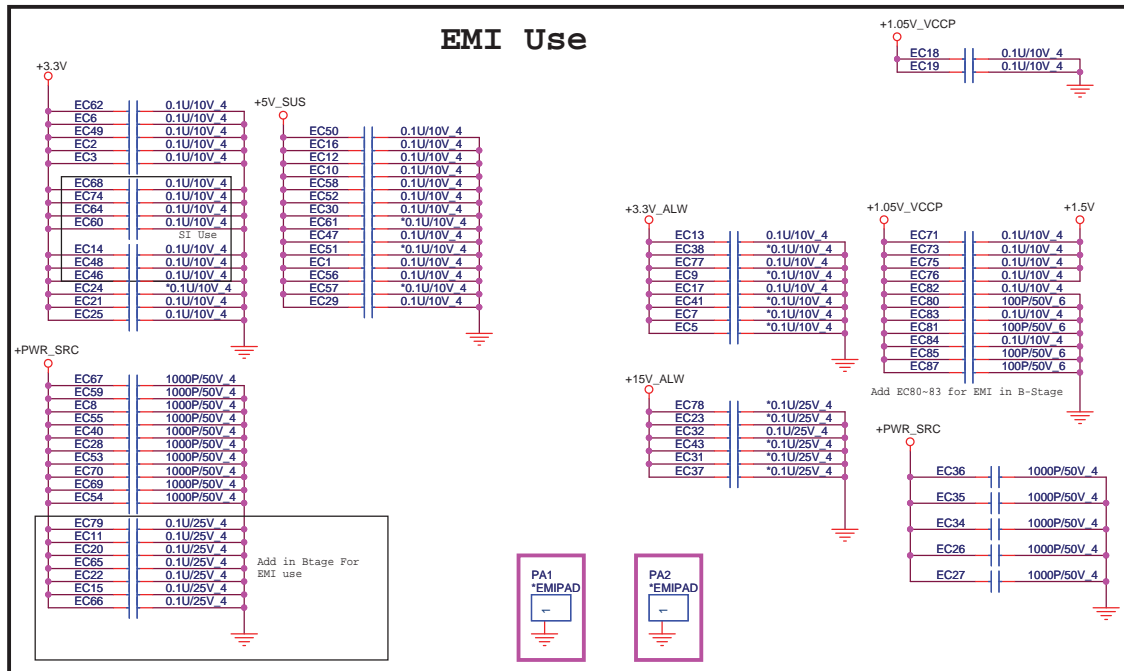
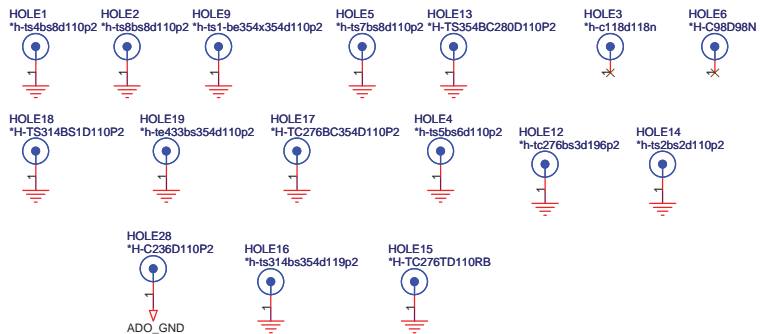
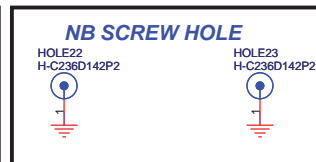
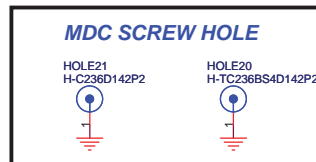
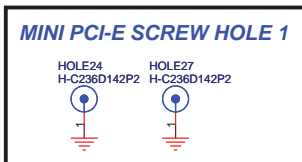
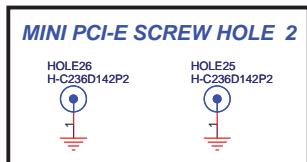
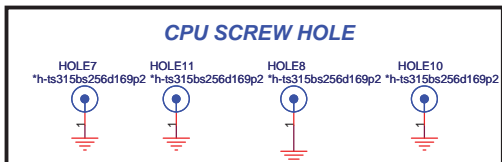


Maximum Current: 44A
OCP:55A

PROJECT : SA6
Quanta Computer Inc.

| | | |
|------------------------------|--------------------------------|----------------|
| Size Custom | Document Number CPU_CORE POWER | Rev 88 |
| Date: Friday, April 25, 2008 | | Sheet 38 of 41 |





A-test to B-test EC list

EC A-01 /15 change to +3.3V_SUS for B test
EC A-02 /24 and 15 Change to 1.5V for HDA use.
EC A-03 /16 Add R499 Pull high to +3.3V_S5
EC A-04 /16 change R190 pull-high to +3.3V_S5
EC A-05 /02 Add EMI Request L52 C554.
EC A-06 /14 C462,C459,C466,C464 Change to 10nF in B Stage.
EC A-07 /15 Add R224 PCI_PME# Connect to +3.3V_S5
EC A-08 /20 change VGA Pin 9 Desgin in B Stage.
EC A-09 /21 Add C557,C558,C555 for EMI Request.
EC A-10 /24 Add C329,C328,C327,C326 for EMI Request.
EC A-11 /26 Add L49,L50,C533,C542 in B stage For EMI use
EC A-12 /31 Add CP7 CP8 C553 in B stage For EMI use
EC A-14 /31 for LED +3.3V leak electricity.
EC A-15 /24 change C525 to 1U Fix POP Noise.
EC A-16 /7 CLK_3GPLLREQ# pull-high Page2 have, So remove R80 CLK_3GPLLREQ# Pull High.
EC A-17 / 21 Use BIOS MAC address , remove R340,R339,U17 , Mount R338.
EC A-18 / 18 B Stage R282 to 100 ohm for conexant request.

B-test to C-test EC list

EC B-01 /02 change 22P to 30P for RTC issue.
EC B-02 /03 change to 10K for meet Intel spec.
EC B-03 /05 change to 0 ohm for meet ADI spec.
EC B-04 /09/10 NA 220U and 330U.
EC B-05 /24 change R491,R492 from 0 ohm to 6.8K C551,C543 to 1U and change AMP Gain to 10 db for meet SPK Spec 1.5W.

EC B-6 /24 Add C603,C604,C606,C607,C608,C609 for ESD Request.
EC B-7 /30 Add R507,C560,C561 for ITE8502JX use.
EC B-8 /15 mount R447 and C482 for EMI request.
EC B-9 /30 Add R508 and C562 for EMI request.
EC B-10 /40 Add C563,C564,C565,C566 fix ESD .
EC B-11 /34 change PC66 to ESD Diode fix ESD .
EC B-12 /15 Add U31 for HDCP support.
EC B-13 /36 Del PC123,Add PC152.
EC B-14 /37 Add PC151
EC B-15 /31 change R608 to 0805 and Q40 change to 2N7002.
EC B-16 /23 Remove Q11,Q12,R235,R159 change C250 to 0.1U for OZ126 Rev:B use.
EC B-17 /10 Del L38,L39 Add R510,R511 1206 0 ohm.
EC B-18 /29 Mount C71,C76 for ESD.
EC B-19 /07 change R88 from 1.02K to 1K meet Intel check list 1.1

C-test to FAI-test EC list

EC C-01 /17 change C476,C491 to 1U, R427,R470 to 100 ohm for USB 1.0 can't work and meeti Intel Spec.
EC C-02 /17 mount C227 0.1U
EC C-03 /26 Add R514,R515,R516 connect to CL Function
EC C-04 /40 Add C614~C617 for ESD Request.
EC C-05 /30 Remove C561 for ITE Bug.
EC C-06 /27 change C479,C481,C415,C429 to 0.01U for meet Intel Spc.
EC C-07 /19 Add R517 Pin 25 connect to GND, ST Add R320,R319.
EC C-08/14 Add for TMP in FAI
EC C-09/14 Add R424 10K to meet Intel Demo Board.
EC C-10/03 Change C229 to 10P and R171 to 22 ohm for meet Clock test.
EC C-11/26 Change R455 to R466 connector +3V, Add R513 connector +3V for Intel Wireless use.