

# Roberts Discrete VGA ATI M92LP-S2 Schematics Document


## uFCPGA Mobile Penryn

### Intel PM45 + ICH9M

2009-05-19

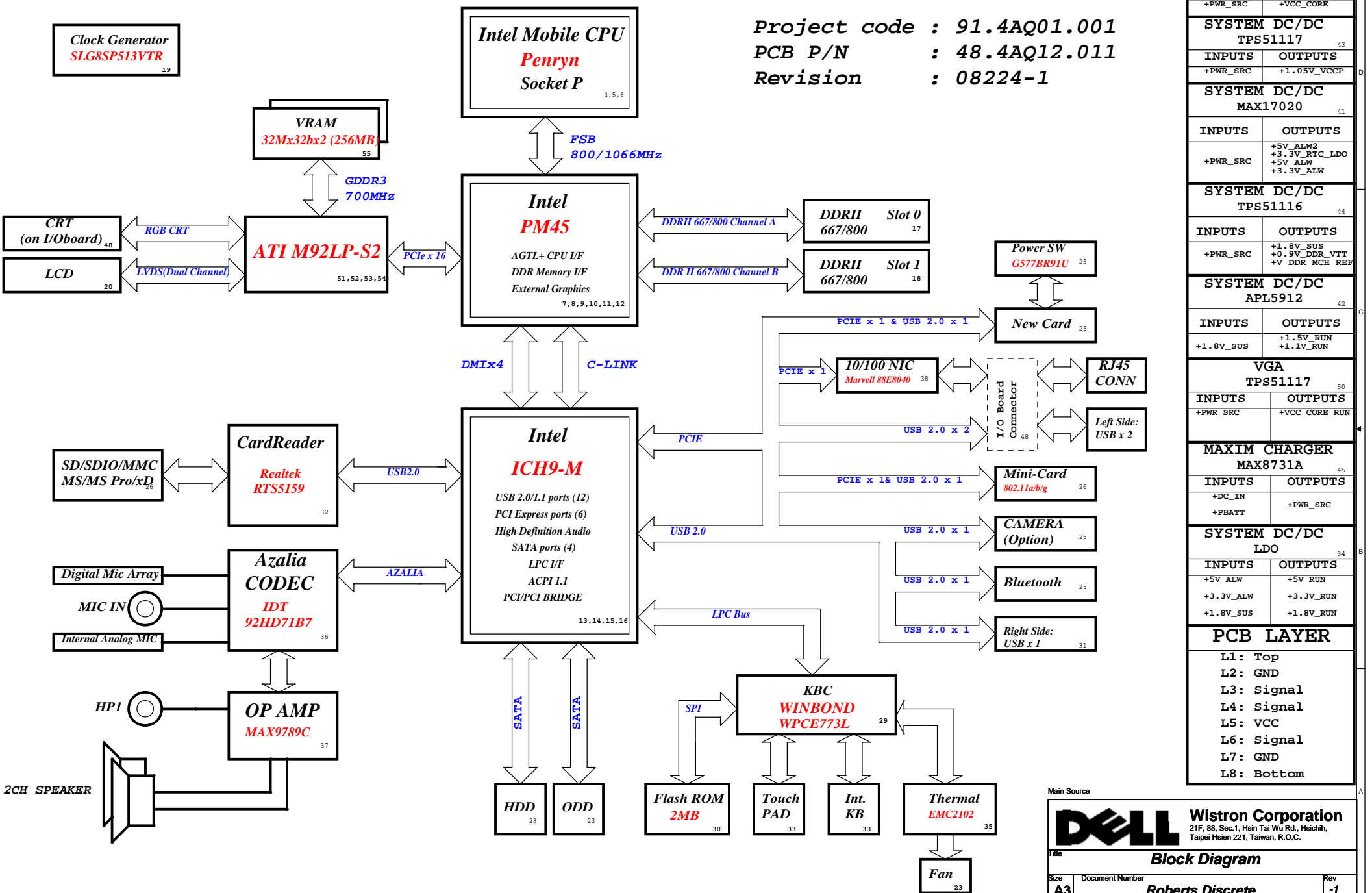
REV :-1

*DY : Nopop Component*

Main Source			
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Title			
<b>Cover Page</b>			
Size Custom	Document Number <b>Roberts Discrete</b>	Rev -1	
Date: Tuesday, May 19, 2009	Sheet 1	of	60

# Roberts Discrete Block Diagram

Project code : 91.4AQ01.001  
 PCB P/N : 48.4AQ12.011  
 Revision : 08224-1



CPU DC/DC	
ISL6266A <sup>39,40</sup>	
INPUTS	OUTPUTS
+PWR_SRC	+VCC_CORE
SYSTEM DC/DC	
TPS51117 <sup>43</sup>	
INPUTS	OUTPUTS
+PWR_SRC	+1.05V_VCCP
SYSTEM DC/DC	
MAX17020 <sup>41</sup>	
INPUTS	OUTPUTS
+PWR_SRC	+5V_ALW2 +3.3V_RTC_LDO +5V_ALW +3.3V_ALW
SYSTEM DC/DC	
TPS51116 <sup>44</sup>	
INPUTS	OUTPUTS
+PWR_SRC	+1.8V_SUS +0.9V_DDR_VTT +V_DDR_MCH_REF
SYSTEM DC/DC	
APL5912 <sup>42</sup>	
INPUTS	OUTPUTS
+1.8V_SUS	+1.5V_RUN +1.1V_RUN
VGA	
TPS51117 <sup>50</sup>	
INPUTS	OUTPUTS
+PWR_SRC	+VCC_CORE_RUN
MAXIM CHARGER	
MAX8731A <sup>45</sup>	
INPUTS	OUTPUTS
+DC_IN	+PWR_SRC
+PBATT	
SYSTEM DC/DC	
LDO <sup>34</sup>	
INPUTS	OUTPUTS
+5V_ALW	+5V_RUN
+3.3V_ALW	+3.3V_RUN
+1.8V_SUS	+1.8V_RUN
PCB LAYER	
L1: Top	
L2: GND	
L3: Signal	
L4: Signal	
L5: VCC	
L6: Signal	
L7: GND	
L8: Bottom	

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Title: **Block Diagram**

Size: **A3** Document Number: **Roberts Discrete** Rev: **-1**

Date: **Tuesday, May 19, 2009** Sheet: **2** of **60**

# ICH9M Functional Strap Definitions

ICH9 EDS 642879 Rev.1.5

# ICH9 Integrated pull-up and pull-down Resistors

ICH9 EDS 642879 Rev.1.5

# Cantiga chipset and ICH9M I/O controller Hub strapping configuration

Montevina Platform Design guide 22339 Rev.0.5

Signal	Usage/When Sampled	Comment
HDA_SDOUT	XOR Chain Entrance/ PCIe Port Config1 bit1 Rising Edge of PWROK.	Allows entrance to XOR Chain testing when TP3 pulled low. When TP3 not pulled low at rising edge of PWROK, sets bit1 of RPC.PC (Config Registers: offset 224h). This signal has weak internal pull-down.
HDA_SYNC	PCIe config1 bit0, Rising Edge of PWROK.	This signal has a weak internal pull-down. Sets bit0 of PRC.PC (Config Registers: Offset 224h).
GNT2#/ GPIO53	PCIe config2 bit2, Rising Edge of PWROK.	This signal has a weak internal pull-up. Sets bit2 of PRC.PC2 (Config Registers: Offset 224h).
GPIO20	Reserved.	This signal should not be pulled high.
GNT1#/ GPIO51	ESI Strap (Server Only) Rising Edge of PWROK.	ESI compatible mode is for server platforms only. This signal should not be pulled low for desktop and mobile.
GNT3#/ GPIO55	Top-Block Swap override. Rising Edge of PWROK.	Sampled low: Top-Block Swap mode (inverts A16 for all cycles targeting FWH BIOS space) Note: Software will not be able to clear the Top-Swap bit until the system is rebooted without GNT3# being pulled down.
GNT0#/ SPI_CS1#/ GPIO58	Boot BIOS Destination Selection 0:1. Rising Edge of PWROK.	Controllable via Boot BIOS Destination bit (Config Registers: Offset 3410h:bit 11:10). GNT0# is MSB, 01-SPI, 10-PCI, 11-LPC
SPI_MOSI	Integrated TPM Enable, Rising Edge of CLPWROK	Sample low: the integrated TPM will be disable. Sample high: the MCH TPM enable strap is sampled low and the TPM Disable bit is clear, the Integrated TPM will be enable.
GPIO49	DMI Termination Voltage. Rising Edge of CLPWROK.	The signal is required to be low for desktop applications and required to be high for mobile applications.
SATALED#	PCI Express Lane Reversal. Rising Edge of PWROK.	Signal has weak internal pull-up. Sets bit 27 of MPC.LR (Device 28: Function 0:Offset D8).
SPKR	No Reboot. Rising Edge of PWROK.	If sampled high, the system is strapped to the "No Reboot" mode (ICH9 will disable the TCO Timer system reboot feature). The status is readable via the NO REBOOT bit.
TP3	XOR Chain Entrance. Rising Edge of PWROK.	This signal should not be pull low unless using XOR Chain testing.
GPIO33/ HDA_DOCK _EN#	Flash Descriptor Security Override Strap. Rising Edge of PWROK.	Sampled low: the Flash Descriptor Security will be overridden. If high, the security measures will be in effect. This should only be enabled in manufacturing environments using an external pull-up resistor.

SIGNAL	Resistor Type/Value
CL_CLK[1:0]	PULL-UP 20K
CL_DATA[1:0]	PULL-UP 20K
CL_RST0#	PULL-UP 20K
DPRSLPVR/GPIO16	PULL-DOWN 20K
ENERGY_DETECT	PULL-UP 20K
HDA_BIT_CLK	PULL-DOWN 20K
HDA_DOCK_EN#/GPIO33	PULL-UP 20K
HDA_RST#	PULL-DOWN 20K
HDA_SDIN[3:0]	PULL-DOWN 20K
HDA_SDOUT	PULL-DOWN 20K
HDA_SYNC	PULL-DOWN 20K
GLAN_DOCK#	The pull-up or pull-down active when configured for native GLAN_DOCK# functionality and determined by LAN controller.
GNT[3:0]#/GPIO[55,53,51]	PULL-UP 20K
GPIO20	PULL-DOWN 20K
GPIO49	PULL-UP 20K
LDA[3:0]#/FWH[3:0]#	PULL-UP 20K
LAN_RXD[2:0]	PULL-UP 20K
LDRQ[0]	PULL-UP 20K
LDRQ[1]/GPIO23	PULL-UP 20K
PME#	PULL-UP 20K
PWRBTN#	PULL-UP 20K
SATALED#	PULL-UP 15K
SPI_CS1#/GPIO58/CLGPIO6	PULL-UP 20K
SPI_MOSI	PULL-DOWN 20K
SPI_MISO	PULL-UP 20K
SPKR	PULL-DOWN 20K
TACH[3:0]	PULL-UP 20K
TP[3]	PULL-UP 20K
USB[11:0][P,N]	PULL-DOWN 15K

Pin Name	Strap Description	Configuration
CFG[2:0]	FSB Frequency Select	000 = FSB1067 011 = FSB667 010 = FSB800 others = Reserved
CFG[4:3] CFG8 CFG[15:14] CFG[18:17]	Reserved	
CFG5	DMI x2 Select	0 = DMI x2 1 = DMI x4 (Default)
CFG6	iTPM Host Interface	0 = The iTPM Host Interface is enabled (Note 2) 1 = The iTPM Host Interface is disabled (default)
CFG7	Intel Management engine crypto strap	0 = Transport Layer Security (TLS) cipher suite with no confidentiality 1 = TLS cipher suite with confidentiality(Default)
CFG9	PCIe Graphics Lane	0 = Reserved Lanes, 15->0, 14->1 ect.. 1 = Normal operation (Default): Lane Numbered in Order
CFG10	PCIe Loopback enable	0 = Enable (Note 3) 1 = Disable (Default)
CFG[13:12]	XOR/ALL	00 = Reserve 10 = XOR mode Enabled 01 = ALLZ mode Enable (Note 3) 11 = Disabled (Default)
CFG16	FSB Dynamic ODT	0 = Dynamic ODT Disabled 1 = Dynamic ODT Enabled (Default)
CFG19	DMI Lane Reversal	0 = Normal operation (Default): Lane Numbered in Order 1 = Reverse Lanes DMI x4 mode [MCH->ICH]: (3->0, 2->1, 1->2 and 0->3) DMI x2 mode [MCH->ICH]: (3->0, 2->1)
CFG20	Digital Display Port (SDVO/DP/iHDMI) Concurrent with PCIe	0 = Only Digital Display Port or PCIe is operational (Default) 1 = Digital display Port and PCIe are operating simultaneously via the PEG port
SDVO _CTRLDATA	SDVO Present	0 = No SDVO Card Present (Default) 1 = SDVO Card Present
L_DDC_DATA	Local Flat Panel (LFP) Present	0 = LFP Disabled (Default) 1 = LFP Card Present; PCIe disabled

**NOTE:**

- All strap signals are sampled with respect to the leading edge of the (G)MCH Power OK (PWROK) signal.
- iTPM can be disabled by a 'Soft-Strap' option in the Flash-decriptor section of the Firmware. This 'Soft-Strap' is activated only after enabling iTPM via CFG6. Only one of the CFG10/CFG12/CFG13 straps can be enabled at any time.


## PCIe Routing

LANE2	MiniCard WLAN
LANE3	LAN
LANE5	New Card

## USB Table

USB	
Pair	Device
0	USB1
1	USB2
2	USB3
3	RESERVED
4	MINI CARD
5	RESERVED
6	BLUETOOTH
7	NEW CARD
8	RESERVED
9	RESERVED
10	Card Reader
11	CAMERA

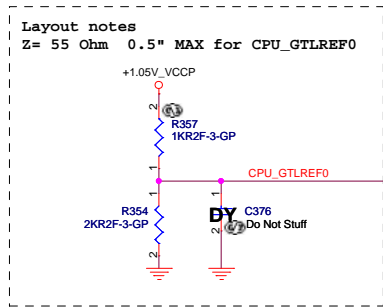
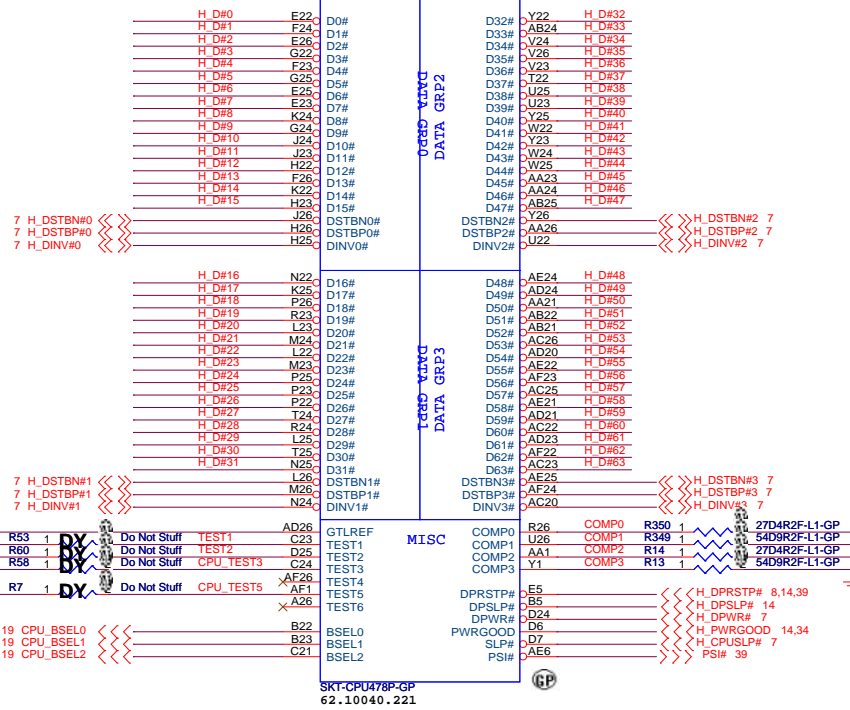
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		Title <b>Table of Content</b>	
Size	Document Number	Rev	
Custom			-1
Date:	Tuesday, May 19, 2009	Sheet	3 of 60



H\_DINV#[3..0] <<<>> H\_DINV#[3..0] 7  
 H\_DSTBN#(3..0) <<<>> H\_DSTBN#(3..0) 7  
 H\_DSTBP#(3..0) <<<>> H\_DSTBP#(3..0) 7  
 H\_D#(63..0) <<<>> H\_D#(63..0) 7

U41B 2 OF 4



**Layout Note:**  
 Comp0, 2 connect with Zo=27.4 ohm, make trace length shorter than 0.5".  
 Comp1, 3 connect with Zo=55 ohm, make trace length shorter than 0.5".

Route the CPU\_TEST3 and CPU\_TEST5 signals through a ground referenced Zo = 55-ohm trace that ends in a via that is near a GND via and is accessible through an oscilloscope connection.

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Title: **CPU-FSB(2/3)**

Size: Document Number  
 Custom: **Roberts Discrete**

Date: Tuesday, May 19, 2009 Sheet 5 of 60

Rev: **-1**

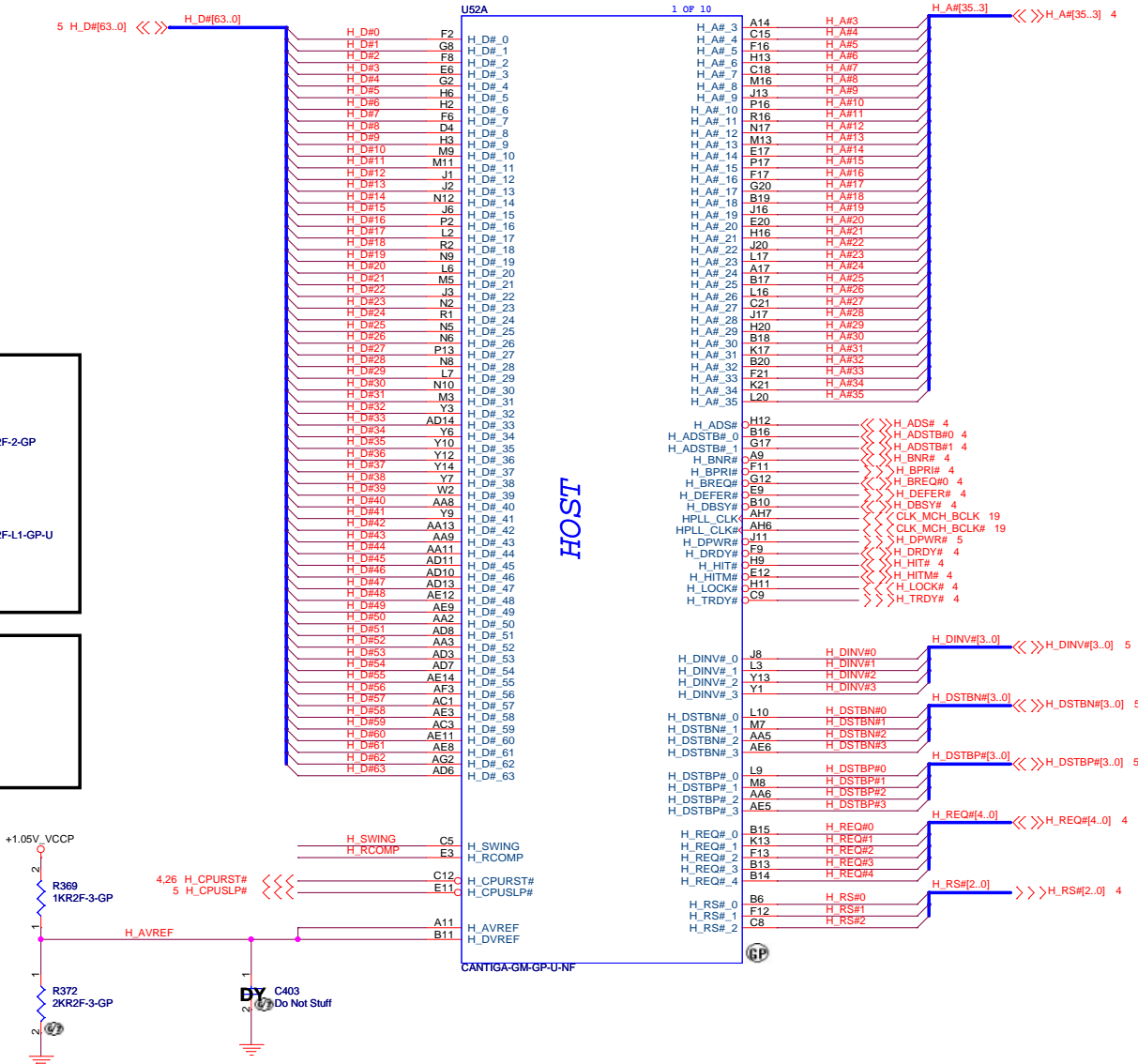
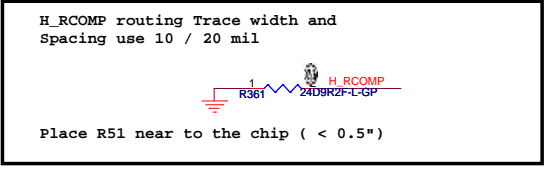
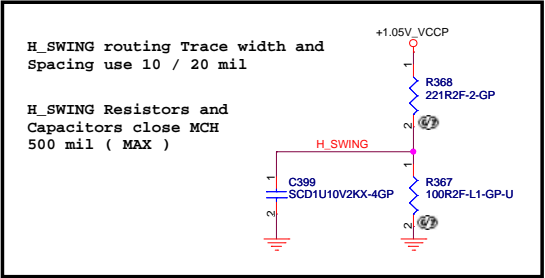
# SSID = CPU



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File			CPU-Power(3/3)		
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Date:	Tuesday, May 19, 2009		Sheet	6	of 60



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Title: **Cantiga-HOST(1/6)**

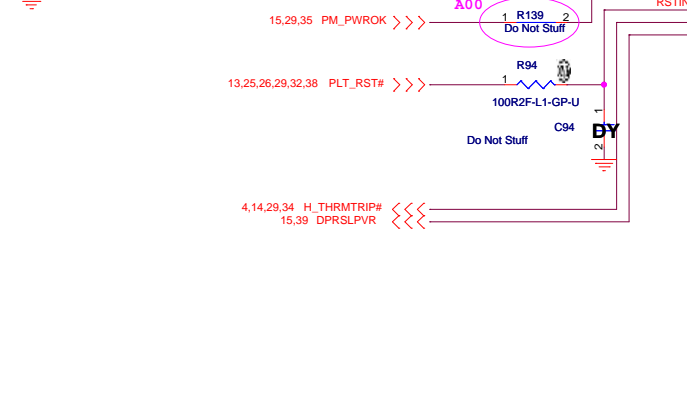
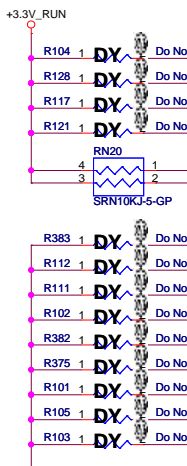
Size	Document Number	Rev
Custom	<b>Roberts Discrete</b>	-1

Date: Tuesday, May 19, 2009 Sheet 7 of 60

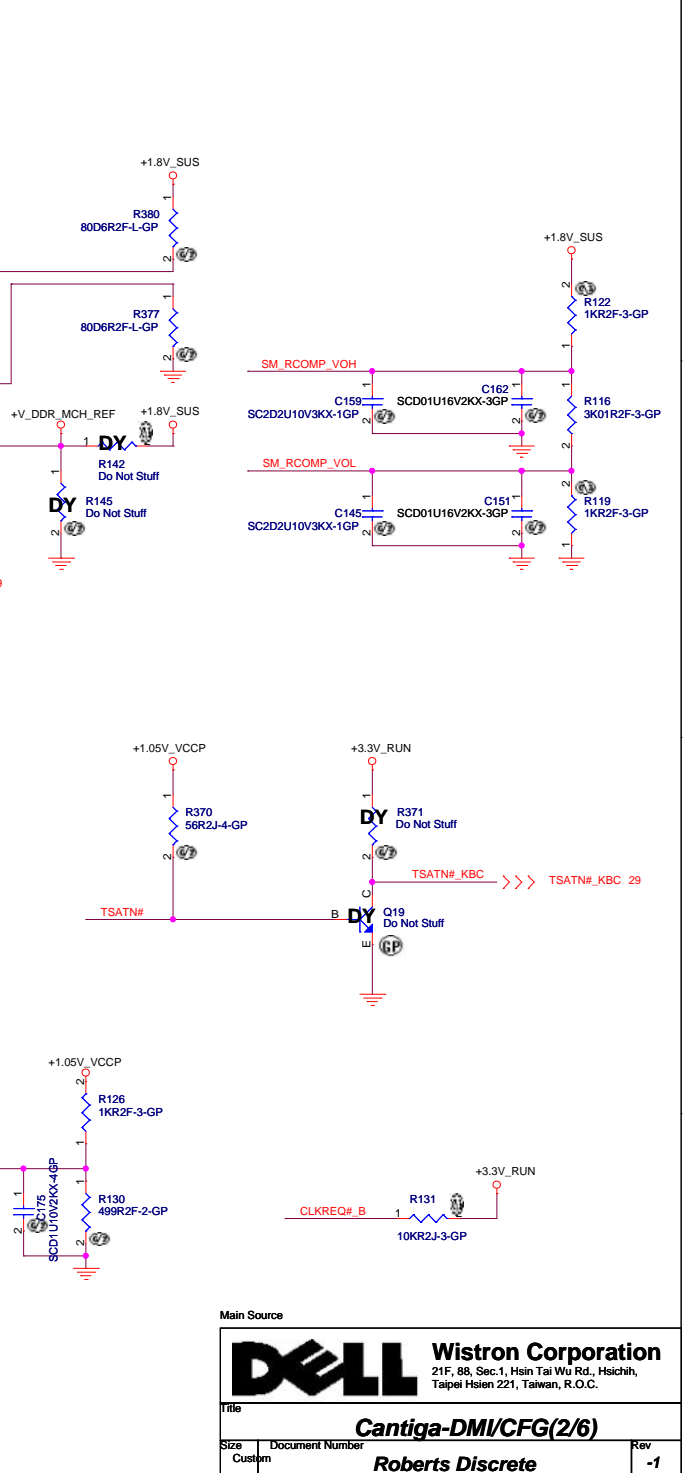
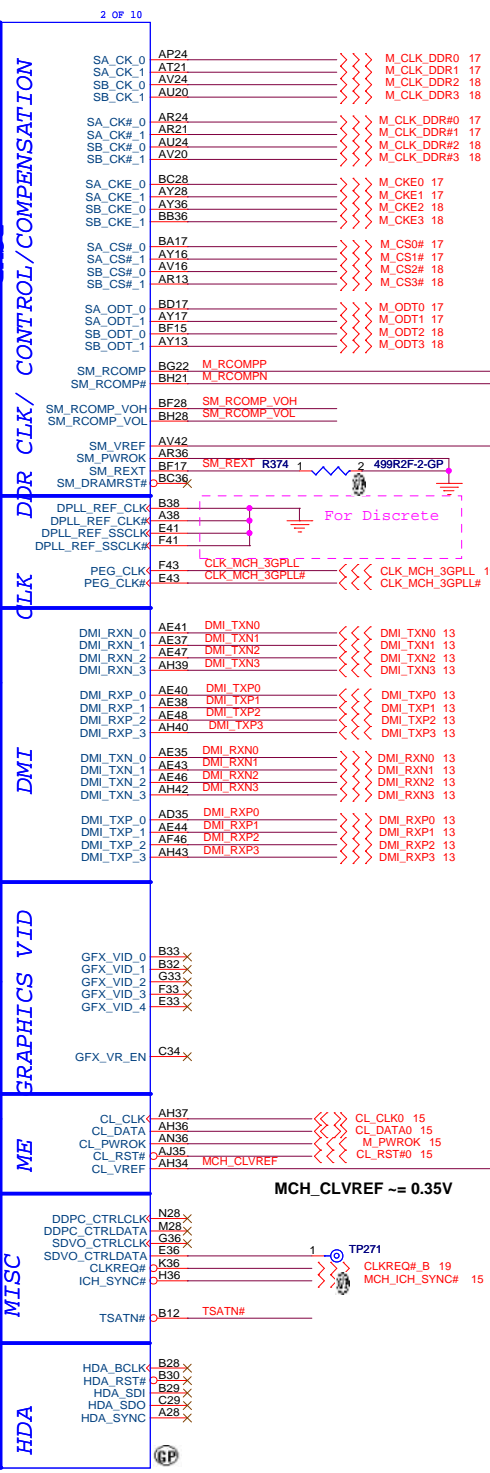
# SSID = MCH

\* is current setting

CFG Strap	Low	High
CFG 5	DMI X 2	DMI X 4 *
CFG 6	ITPM enable	ITPM disable *
CFG 7	TLS cipher suite with no confidentiality	TLS cipher suite with confidentiality *
CFG 9	PCIe GFX lane reversed	PCIe GFX lane numbered in order *
CFG 10	PCIe loopback enable	PCIe loopback disable *
CFG 12	ALLZ mode enable	ALLZ mode disable *
CFG 13	XOR mode enable	XOR mode disable *
CFG 16	FSB dynamic ODT disable	FSB Dynamic ODT enable *
CFG 19	DMI Lane Reserved	Reverse DMI lanes *
CFG 20	SDVO concurrent with PCIe	PCIe and SDVO are operating simultaneously via the PEG port *
SDVO_CTRLDATA	SDVO interface disable *	SDVO interface enable
L_DDC_DATA	LFP disable *	LFP card present
DDPC_CTRLDATA	SDVO/iHDMI/DP interface disabled *	SDVO/iHDMI/DP interface enabled



- M36 RESERVED#M36
- N36 RESERVED#N36
- R33 RESERVED#R33
- T33 RESERVED#T33
- AH9 RESERVED#AH9
- AH10 RESERVED#AH10
- AH12 RESERVED#AH12
- AH13 RESERVED#AH13
- K12 RESERVED#K12
- AL34 RESERVED#AL34
- AK34 RESERVED#AK34
- AM35 RESERVED#AM35
- T24 RESERVED#T24
- B31 RESERVED#B31
- B2 RESERVED#B2
- M1 RESERVED#M1
- AY21 RESERVED#AY21
- BG23 RESERVED#BG23
- BF23 RESERVED#BF23
- BH18 RESERVED#BH18
- BF18 RESERVED#BF18
- BG23 RESERVED#BG23
- BF23 RESERVED#BF23
- BH18 RESERVED#BH18
- BF18 RESERVED#BF18
- AV42 RESERVED#AV42
- AR36 RESERVED#AR36
- BF17 RESERVED#BF17
- BC36 RESERVED#BC36
- B38 RESERVED#B38
- A38 RESERVED#A38
- E41 RESERVED#E41
- F41 RESERVED#F41
- F43 RESERVED#F43
- E43 RESERVED#E43
- T25 CFG\_0
- R29 CFG\_1
- P25 CFG\_2
- P20 CFG\_3
- P24 CFG\_4
- C25 CFG\_5
- M24 CFG\_6
- M24 CFG\_7
- E21 CFG\_8
- C23 CFG\_9
- C24 CFG\_10
- N21 CFG\_11
- T21 CFG\_12
- C23 CFG\_13
- M20 CFG\_14
- L21 CFG\_15
- H21 CFG\_16
- H21 CFG\_17
- R28 CFG\_18
- R28 CFG\_19
- T28 CFG\_20
- R29 PM\_SYNC#
- B7C PM\_DPRSTP#
- N33 PM\_EXT\_TS#\_0
- P32 PM\_EXT\_TS#\_1
- AT40 PWROK
- AT11C RSTIN#
- T20 THERMTRIP#
- R32 DPRSLPVR
- NC#BG48
- NC#BF48
- NC#BD48
- NC#BC48
- NC#BH47
- NC#BG47
- NC#BE47
- NC#BH46
- NC#BF46
- NC#BG45
- NC#BH44
- NC#BH43
- NC#BH6
- NC#BH5
- NC#BH4
- NC#BH3
- NC#BF3
- NC#BH2
- NC#BG2
- NC#BE2
- NC#BG1
- NC#BF1
- NC#BD1
- NC#BC1
- F1 NC#F1
- NC#A47
- BG48 NC#BG48
- BF48 NC#BF48
- BD48 NC#BD48
- BC48 NC#BC48
- BH47 NC#BH47
- BG47 NC#BG47
- BE47 NC#BE47
- BH46 NC#BH46
- BF46 NC#BF46
- BG45 NC#BG45
- BH44 NC#BH44
- BH43 NC#BH43
- BH6 NC#BH6
- BH5 NC#BH5
- BH4 NC#BH4
- BH3 NC#BH3
- BF3 NC#BF3
- BH2 NC#BH2
- BG2 NC#BG2
- BE2 NC#BE2
- BG1 NC#BG1
- BF1 NC#BF1
- BD1 NC#BD1
- BC1 NC#BC1
- F1 NC#F1
- A47 NC#A47



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File: **Cantiga-DMI/CFG(2/6)**

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Date: Tuesday, May 19, 2009 Sheet 8 of 60



17 M\_A\_DQ[63.0] <<< M\_A\_DQ[63.0]

M A D00	AJ38	SA_DQ_0
M A D01	AJ41	SA_DQ_1
M A D02	AN38	SA_DQ_2
M A D03	AM38	SA_DQ_3
M A D04	AJ36	SA_DQ_4
M A D05	AJ40	SA_DQ_5
M A D06	AM44	SA_DQ_6
M A D07	AM42	SA_DQ_7
M A D08	AN43	SA_DQ_8
M A D09	AN44	SA_DQ_9
M A D10	AU40	SA_DQ_10
M A D11	AT38	SA_DQ_11
M A D12	AN41	SA_DQ_12
M A D13	AN39	SA_DQ_13
M A D14	AU44	SA_DQ_14
M A D15	AU42	SA_DQ_15
M A D16	AV39	SA_DQ_16
M A D17	A144	SA_DQ_17
M A D18	BA40	SA_DQ_18
M A D19	BD43	SA_DQ_19
M A D20	AV41	SA_DQ_20
M A D21	A143	SA_DQ_21
M A D22	BB41	SA_DQ_22
M A D23	BC40	SA_DQ_23
M A D24	AY37	SA_DQ_24
M A D25	BD38	SA_DQ_25
M A D26	AV37	SA_DQ_26
M A D27	AT36	SA_DQ_27
M A D28	AV38	SA_DQ_28
M A D29	BB38	SA_DQ_29
M A D30	AV36	SA_DQ_30
M A D31	AW36	SA_DQ_31
M A D32	BD13	SA_DQ_32
M A D33	AU11	SA_DQ_33
M A D34	BC11	SA_DQ_34
M A D35	BA12	SA_DQ_35
M A D36	AU13	SA_DQ_36
M A D37	AV13	SA_DQ_37
M A D38	BD12	SA_DQ_38
M A D39	BC12	SA_DQ_39
M A D40	BB9	SA_DQ_40
M A D41	BA9	SA_DQ_41
M A D42	AU10	SA_DQ_42
M A D43	AV9	SA_DQ_43
M A D44	BA11	SA_DQ_44
M A D45	BD9	SA_DQ_45
M A D46	AY8	SA_DQ_46
M A D47	BA6	SA_DQ_47
M A D48	AV5	SA_DQ_48
M A D49	AV7	SA_DQ_49
M A D50	AT9	SA_DQ_50
M A D51	AN8	SA_DQ_51
M A D52	AU5	SA_DQ_52
M A D53	AU6	SA_DQ_53
M A D54	AT5	SA_DQ_54
M A D55	AN10	SA_DQ_55
M A D56	AM11	SA_DQ_56
M A D57	AM5	SA_DQ_57
M A D58	AJ9	SA_DQ_58
M A D59	AJ8	SA_DQ_59
M A D60	AN12	SA_DQ_60
M A D61	AM13	SA_DQ_61
M A D62	AJ11	SA_DQ_62
M A D63	AJ12	SA_DQ_63

**DDR SYSTEM MEMORY A**

4 OF 10

SA_BS_0	BD21	M A_BS#0	17
SA_BS_1	BG18	M A_BS#1	17
SA_BS_2	AT25	M A_BS#2	17
SA_RAS#	BB20	M A_RAS#	17
SA_CAS#	BD20	M A_CAS#	17
SA_WE#	AY20	M A_WE#	17
SA_DM_0	AM37	M A_DM[7.0]	17
SA_DM_1	AT41	M A_DM1	17
SA_DM_2	AY41	M A_DM2	17
SA_DM_3	AU39	M A_DM3	17
SA_DM_4	BB12	M A_DM4	17
SA_DM_5	AY6	M A_DM5	17
SA_DM_6	AT7	M A_DM6	17
SA_DM_7	AJ5	M A_DM7	17
SA_DQS_0	AJ44	M A_DQS0	17
SA_DQS_1	AT44	M A_DQS1	17
SA_DQS_2	BA43	M A_DQS2	17
SA_DQS_3	BC37	M A_DQS3	17
SA_DQS_4	AW12	M A_DQS4	17
SA_DQS_5	BC8	M A_DQS5	17
SA_DQS_6	AU8	M A_DQS6	17
SA_DQS_7	AM7	M A_DQS7	17
SA_DQS#_0	AJ43	M A_DQS#0	17
SA_DQS#_1	AT43	M A_DQS#1	17
SA_DQS#_2	BA44	M A_DQS#2	17
SA_DQS#_3	BD37	M A_DQS#3	17
SA_DQS#_4	AY12	M A_DQS#4	17
SA_DQS#_5	BD8	M A_DQS#5	17
SA_DQS#_6	AU8	M A_DQS#6	17
SA_DQS#_7	AM6	M A_DQS#7	17
SA_MA_0	BA21	M A_A0	17
SA_MA_1	BC24	M A_A1	17
SA_MA_2	BG24	M A_A2	17
SA_MA_3	BH24	M A_A3	17
SA_MA_4	BG25	M A_A4	17
SA_MA_5	BA24	M A_A5	17
SA_MA_6	BD24	M A_A6	17
SA_MA_7	BG27	M A_A7	17
SA_MA_8	BF25	M A_A8	17
SA_MA_9	BC21	M A_A9	17
SA_MA_10	BG56	M A_A10	17
SA_MA_11	BH26	M A_A11	17
SA_MA_12	BH17	M A_A12	17
SA_MA_13	AY25	M A_A13	17
SA_MA_14	AY25	M A_A14	17

18 M\_B\_DQ[63.0] <<< M\_B\_DQ[63.0]

M B D00	AK47	SB_DO_0
M B D01	AH46	SB_DO_1
M B D02	AP47	SB_DO_2
M B D03	AP46	SB_DO_3
M B D04	AJ46	SB_DO_4
M B D05	AJ48	SB_DO_5
M B D06	AM48	SB_DO_6
M B D07	AP48	SB_DO_7
M B D08	AU47	SB_DO_8
M B D09	AU46	SB_DO_9
M B D10	BA48	SB_DO_10
M B D11	AY48	SB_DO_11
M B D12	AT47	SB_DO_12
M B D13	AR47	SB_DO_13
M B D14	BA47	SB_DO_14
M B D15	BC47	SB_DO_15
M B D16	BC46	SB_DO_16
M B D17	BC44	SB_DO_17
M B D18	BG43	SB_DO_18
M B D19	BF43	SB_DO_19
M B D20	BE45	SB_DO_20
M B D21	BC41	SB_DO_21
M B D22	BF40	SB_DO_22
M B D23	BF41	SB_DO_23
M B D24	BG38	SB_DO_24
M B D25	BF39	SB_DO_25
M B D26	BH35	SB_DO_26
M B D27	BG35	SB_DO_27
M B D28	BH40	SB_DO_28
M B D29	BG39	SB_DO_29
M B D30	BG34	SB_DO_30
M B D31	BH34	SB_DO_31
M B D32	BH14	SB_DO_32
M B D33	BG12	SB_DO_33
M B D34	BH11	SB_DO_34
M B D35	BG8	SB_DO_35
M B D36	BH12	SB_DO_36
M B D37	BF11	SB_DO_37
M B D38	BF8	SB_DO_38
M B D39	BG7	SB_DO_39
M B D40	BC5	SB_DO_40
M B D41	BC6	SB_DO_41
M B D42	AY3	SB_DO_42
M B D43	AY11	SB_DO_43
M B D44	BF6	SB_DO_44
M B D45	BF5	SB_DO_45
M B D46	BA1	SB_DO_46
M B D47	BD3	SB_DO_47
M B D48	AV2	SB_DO_48
M B D49	AU3	SB_DO_49
M B D50	AR3	SB_DO_50
M B D51	AN2	SB_DO_51
M B D52	AY2	SB_DO_52
M B D53	AV1	SB_DO_53
M B D54	AP3	SB_DO_54
M B D55	AR1	SB_DO_55
M B D56	AL1	SB_DO_56
M B D57	AL2	SB_DO_57
M B D58	AJ1	SB_DO_58
M B D59	AH1	SB_DO_59
M B D60	AM2	SB_DO_60
M B D61	AM3	SB_DO_61
M B D62	AH3	SB_DO_62
M B D63	AJ3	SB_DO_63

**DDR SYSTEM MEMORY B**

5 OF 10

SB_BS_0	BB17	M B_BS#0	18
SB_BS_1	BB33	M B_BS#1	18
SB_BS_2	BB33	M B_BS#2	18
SB_RAS#	AU17	M B_RAS#	18
SB_CAS#	BG16	M B_CAS#	18
SB_WE#	BF14	M B_WE#	18
SB_DM_0	AM47	M B_DM0	18
SB_DM_1	AY47	M B_DM1	18
SB_DM_2	BD40	M B_DM2	18
SB_DM_3	BF35	M B_DM3	18
SB_DM_4	BG11	M B_DM4	18
SB_DM_5	BA3	M B_DM5	18
SB_DM_6	AP1	M B_DM6	18
SB_DM_7	AK2	M B_DM7	18
SB_DQS_0	AL47	M B_DQS0	18
SB_DQS_1	AV48	M B_DQS1	18
SB_DQS_2	BG41	M B_DQS2	18
SB_DQS_3	BG37	M B_DQS3	18
SB_DQS_4	BH9	M B_DQS4	18
SB_DQS_5	BB2	M B_DQS5	18
SB_DQS_6	AU1	M B_DQS6	18
SB_DQS_7	AN6	M B_DQS7	18
SB_DQS#_0	AL46	M B_DQS#0	18
SB_DQS#_1	AV47	M B_DQS#1	18
SB_DQS#_2	BH41	M B_DQS#2	18
SB_DQS#_3	BH37	M B_DQS#3	18
SB_DQS#_4	BG9	M B_DQS#4	18
SB_DQS#_5	BC2	M B_DQS#5	18
SB_DQS#_6	AT2	M B_DQS#6	18
SB_DQS#_7	AN5	M B_DQS#7	18
SB_MA_0	AV17	M B_A0	18
SB_MA_1	BA25	M B_A1	18
SB_MA_2	BC25	M B_A2	18
SB_MA_3	AU25	M B_A3	18
SB_MA_4	AW25	M B_A4	18
SB_MA_5	BB28	M B_A5	18
SB_MA_6	AU28	M B_A6	18
SB_MA_7	AW28	M B_A7	18
SB_MA_8	AT33	M B_A8	18
SB_MA_9	BD33	M B_A9	18
SB_MA_10	BB16	M B_A10	18
SB_MA_11	AW33	M B_A11	18
SB_MA_12	AY33	M B_A12	18
SB_MA_13	BH15	M B_A13	18
SB_MA_14	AU33	M B_A14	18

CANTIGA-GM-GP-U-NF

CANTIGA-GM-GP-U-NF

Main Source

**DELL** Wistron Corporation  
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.

Title: **Cantiga-DDR(3/6)**

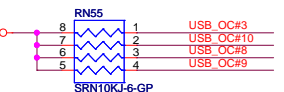
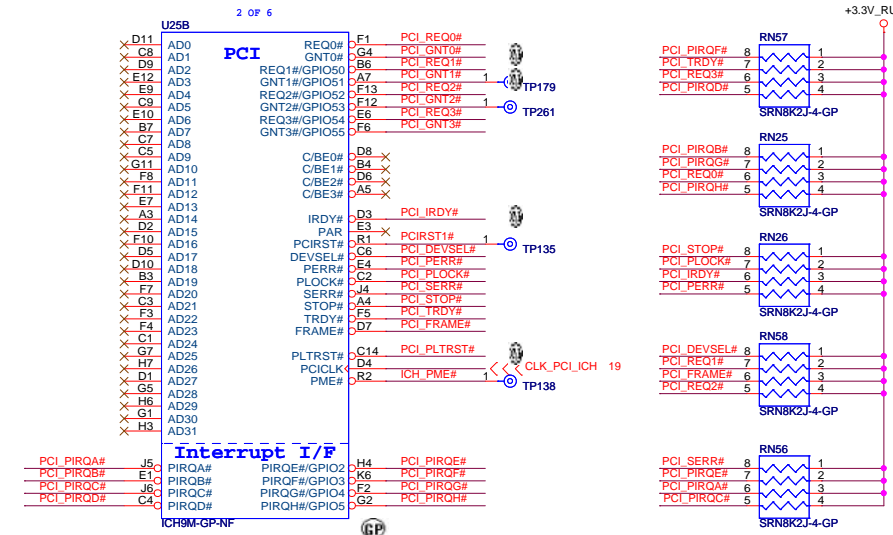
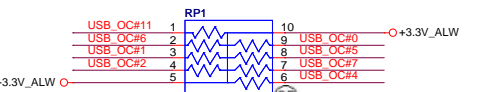
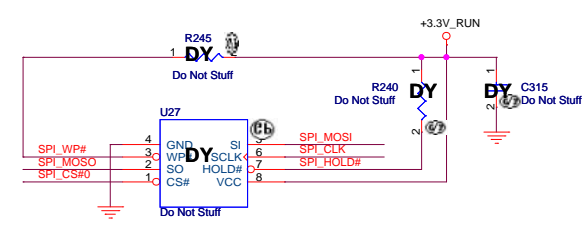
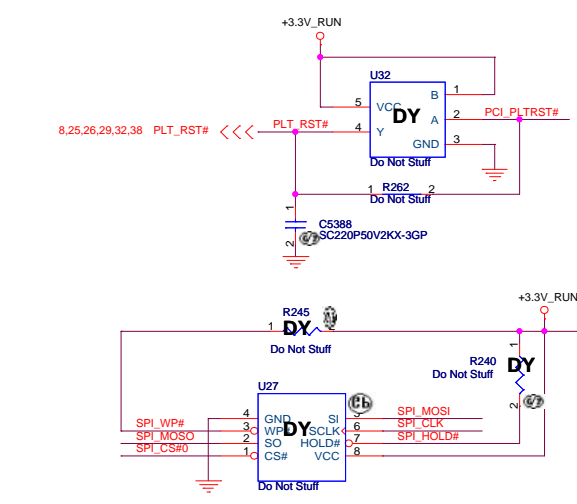
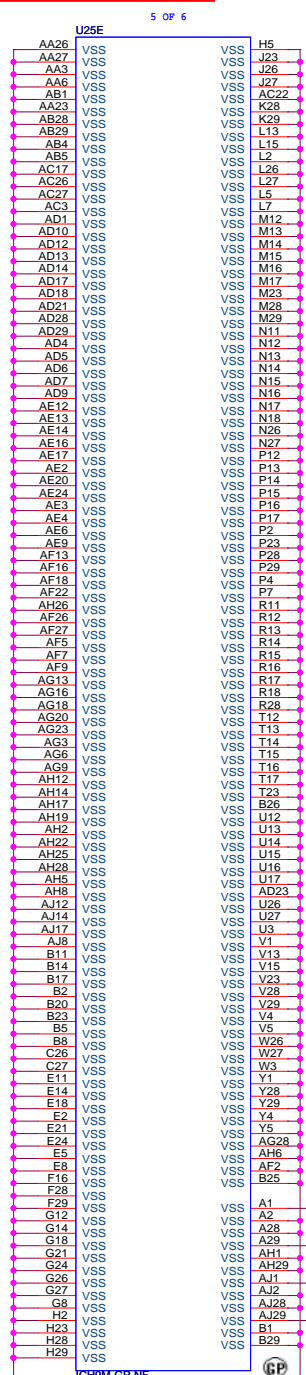
Size	Document Number	Rev
Custom	<b>Roberts Discrete</b>	-1
Date:	Tuesday, May 19, 2009	Sheet 9 of 60







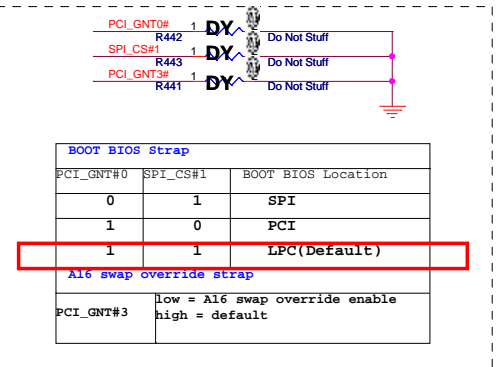
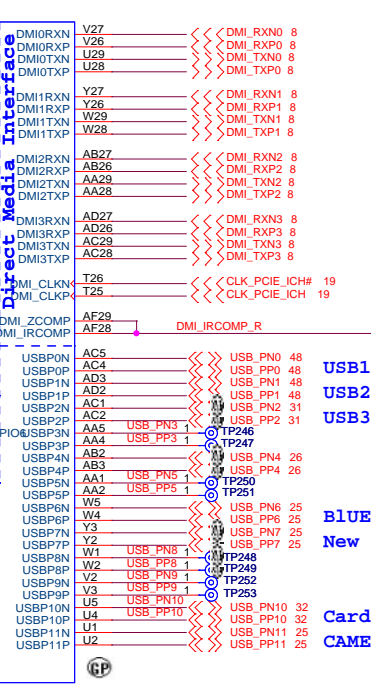
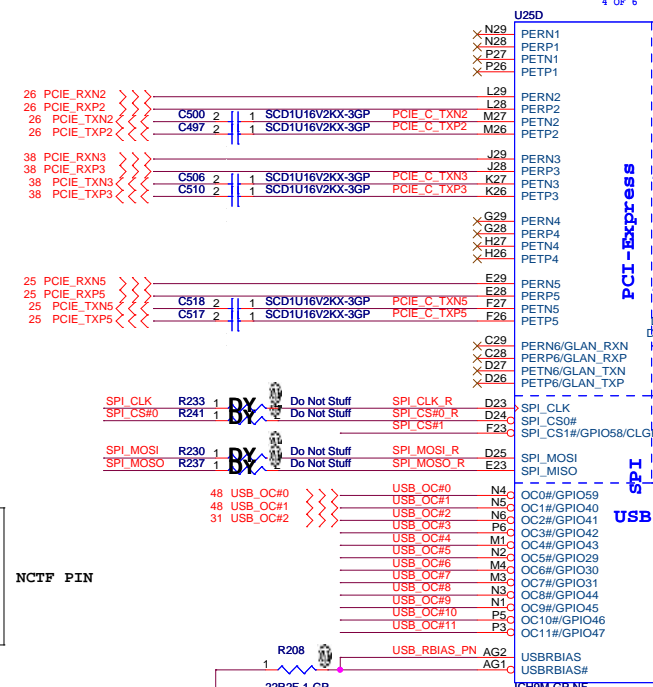
**SSID = ICH**



Mini Card

LAN

New Card



BOOT BIOS Strap		
PCI_GNT#0	SPI_CS#1	BOOT BIOS Location
0	1	SPI
1	0	PCI
1	1	LPC(Default)

Al6 swap override strap  
low = Al6 swap override enable  
high = default

USB Pair	Device
0	USB1
1	USB2
2	USB3
3	RESERVED
4	MINI CARD
5	RESERVED
6	BLUETOOTH
7	NEW CARD
8	RESERVED
9	RESERVED
10	Card Reader
11	CAMERA

Main Source

**Wistron Corporation**  
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File: **ICH9-PCI/PCIE/DMI/USB/GND(1/4)**

Size: Custom Document Number  
Date: Tuesday, May 19, 2009 Sheet 13 of 60

Rev: -1  
Roberts Discrete



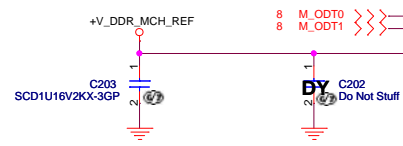
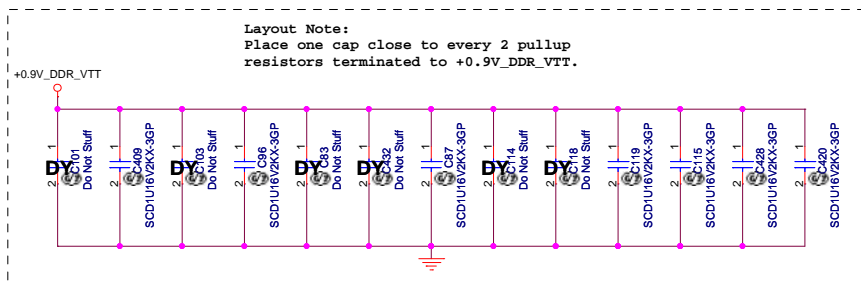
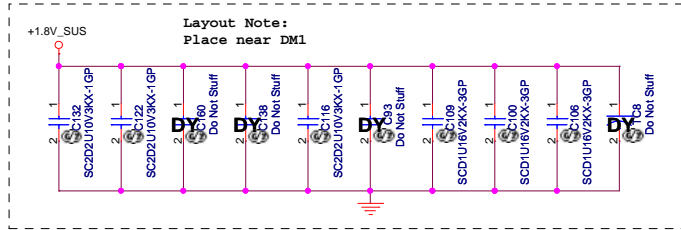






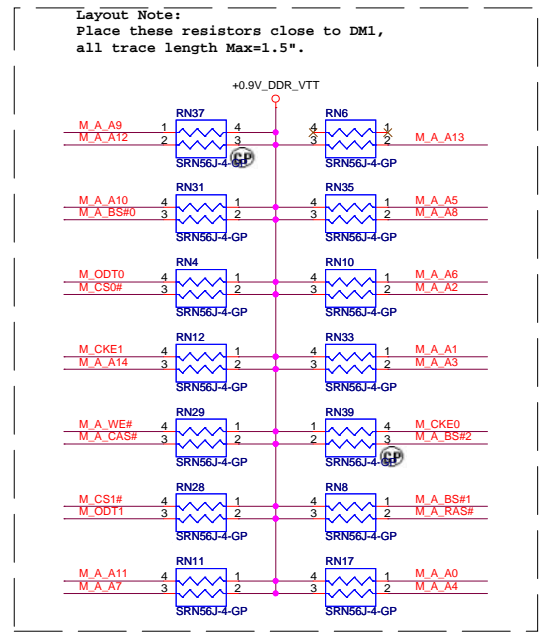
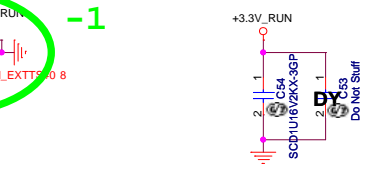
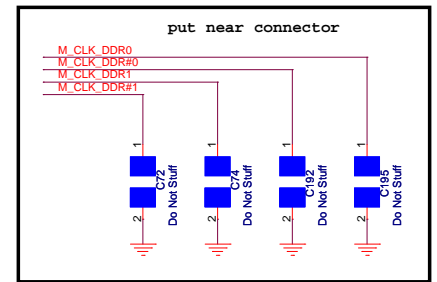
# SSID = MEMORY

9 M\_A\_DQS#{7..0} <<< <<<  
 9 M\_A\_DQ{63..0} <<< <<<  
 9 M\_A\_DM{7..0} <<< <<<  
 9 M\_A\_DQS{7..0} <<< <<<  
 9 M\_A\_A[14..0] <<< <<<



M_A A0	102	A0
M_A A1	101	A1
M_A A2	100	A2
M_A A3	99	A3
M_A A4	98	A4
M_A A5	97	A5
M_A A6	94	A6
M_A A7	92	A7
M_A A8	91	A8
M_A A9	89	A9
M_A A10	105	A10/AP
M_A A11	90	A11
M_A A12	89	A12
M_A A13	116	A13
M_A A14	86	A14
M_A BS#2	84	A15
M_A BS#0	85	A16/BA2
M_A BS#1	107	BA0
M_A BS#1	106	BA1
M_A DQ0	5	DQ0
M_A DQ1	7	DQ1
M_A DQ2	17	DQ2
M_A DQ3	19	DQ3
M_A DQ4	4	DQ4
M_A DQ5	6	DQ5
M_A DQ6	14	DQ6
M_A DQ7	16	DQ7
M_A DQ8	23	DQ8
M_A DQ9	25	DQ9
M_A DQ10	35	DQ10
M_A DQ11	37	DQ11
M_A DQ12	20	DQ12
M_A DQ13	22	DQ13
M_A DQ14	36	DQ14
M_A DQ15	38	DQ15
M_A DQ16	43	DQ16
M_A DQ17	45	DQ17
M_A DQ18	55	DQ18
M_A DQ19	57	DQ19
M_A DQ20	44	DQ20
M_A DQ21	46	DQ21
M_A DQ22	56	DQ22
M_A DQ23	58	DQ23
M_A DQ24	61	DQ24
M_A DQ25	63	DQ25
M_A DQ26	73	DQ26
M_A DQ27	75	DQ27
M_A DQ28	62	DQ28
M_A DQ29	64	DQ29
M_A DQ30	74	DQ30
M_A DQ31	76	DQ31
M_A DQ32	123	DQ32
M_A DQ33	125	DQ33
M_A DQ34	135	DQ34
M_A DQ35	137	DQ35
M_A DQ36	124	DQ36
M_A DQ37	126	DQ37
M_A DQ38	134	DQ38
M_A DQ39	136	DQ39
M_A DQ40	141	DQ40
M_A DQ41	151	DQ41
M_A DQ42	153	DQ42
M_A DQ43	140	DQ43
M_A DQ44	142	DQ44
M_A DQ45	152	DQ45
M_A DQ46	154	DQ46
M_A DQ47	157	DQ47
M_A DQ48	159	DQ48
M_A DQ49	173	DQ49
M_A DQ50	175	DQ50
M_A DQ51	158	DQ51
M_A DQ52	160	DQ52
M_A DQ53	174	DQ53
M_A DQ54	176	DQ54
M_A DQ55	179	DQ55
M_A DQ56	181	DQ56
M_A DQ57	189	DQ57
M_A DQ58	191	DQ58
M_A DQ59	180	DQ59
M_A DQ60	182	DQ60
M_A DQ61	192	DQ61
M_A DQ62	194	DQ62
M_A DQ63		DQ63
M_A DQS#0	11	DQS0#
M_A DQS#1	29	DQS1#
M_A DQS#2	49	DQS2#
M_A DQS#3	68	DQS3#
M_A DQS#4	129	DQS4#
M_A DQS#5	146	DQS5#
M_A DQS#6	167	DQS6#
M_A DQS#7	186	DQS7#
M_A DQSO	13	DQSO#
M_A DQS1	31	DQS1#
M_A DQS2	51	DQS2#
M_A DQS3	70	DQS3#
M_A DQS4	131	DQS4#
M_A DQS5	148	DQS5#
M_A DQS6	169	DQS6#
M_A DQS7	188	DQS7#
M_A DQSO	114	DQSO#
M_A DQS1	119	DQS1#
OTD0		OTD0
OTD1		OTD1
VREF	1	VREF
VSS	2	VSS
GND	202	GND
MH1		MH1
MH2		MH2

RAS#	108	M_A_RAS# 9
WE#	109	M_A_WE# 9
CAS#	113	M_A_CAS# 9
CS0#	110	M_CS0# 8
CS1#	115	M_CS1# 8
CKE0	79	M_CKE0 8
CKE1	80	M_CKE1 8
CK0	30	M_CLK_DDR0
CK0#	32	M_CLK_DDR#0
CK1	164	M_CLK_DDR1
CK1#	166	M_CLK_DDR#1
DM0	10	M_A_DM0
DM1	26	M_A_DM1
DM2	52	M_A_DM2
DM3	67	M_A_DM3
DM4	130	M_A_DM4
DM5	147	M_A_DM5
DM6	170	M_A_DM6
DM7	185	M_A_DM7
SDA	195	ICH_SMBDATA ICH_SMBDATA 15,18,19
SCL	197	ICH_SMBCLK ICH_SMBCLK 15,18,19
VDDSPD	199	+3.3V_RUN
SA0	198	R55 Do Not Stuff
SA1	200	R56 Do Not Stuff
NC#50	50	PM_EXTT#0 8
NC#69	69	
NC#83	83	
NC#120	120	
NC#163/TEST	163	
VDD	81	
VDD	82	
VDD	87	
VDD	88	
VDD	96	
VDD	96	
VDD	103	
VDD	104	
VDD	111	
VDD	112	
VDD	117	
VDD	118	
VSS	3	
VSS	8	
VSS	9	
VSS	12	
VSS	15	
VSS	15	
VSS	24	
VSS	24	
VSS	27	
VSS	28	
VSS	33	
VSS	34	
VSS	39	
VSS	40	
VSS	41	
VSS	42	
VSS	47	
VSS	47	
VSS	48	
VSS	53	
VSS	54	
VSS	59	
VSS	60	
VSS	65	
VSS	66	
VSS	71	
VSS	72	
VSS	72	
VSS	78	
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VSS	127	
VSS	128	
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VSS	133	
VSS	138	
VSS	139	
VSS	144	
VSS	145	
VSS	149	
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VSS	155	
VSS	156	
VSS	161	
VSS	162	
VSS	165	
VSS	168	
VSS	171	
VSS	172	
VSS	177	
VSS	178	
VSS	183	
VSS	184	
VSS	187	
VSS	190	
VSS	193	
VSS	196	
GND	201	
GND	201	
MH1		MH1
MH2		MH2



Main Source

**DELL** Wistron Corporation  
 21F, 88, Sec. 1, Hsin Tai Wu Rd., Hsichih,  
 Taipei Hsien 221, Taiwan, R.O.C.

File: **DDR11-SODIMM SLOT1**

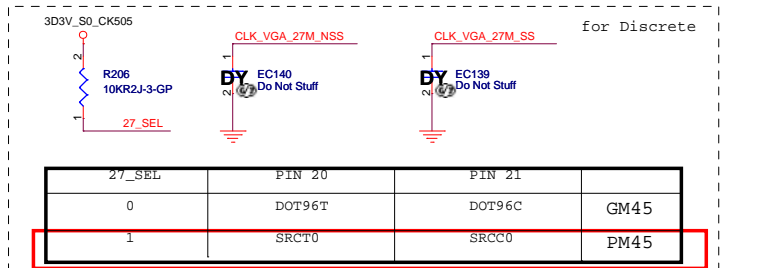
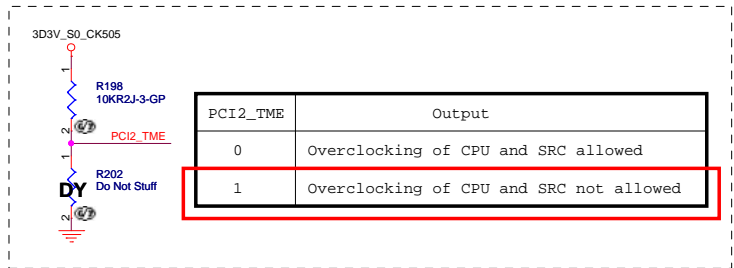
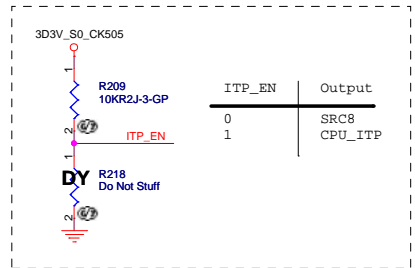
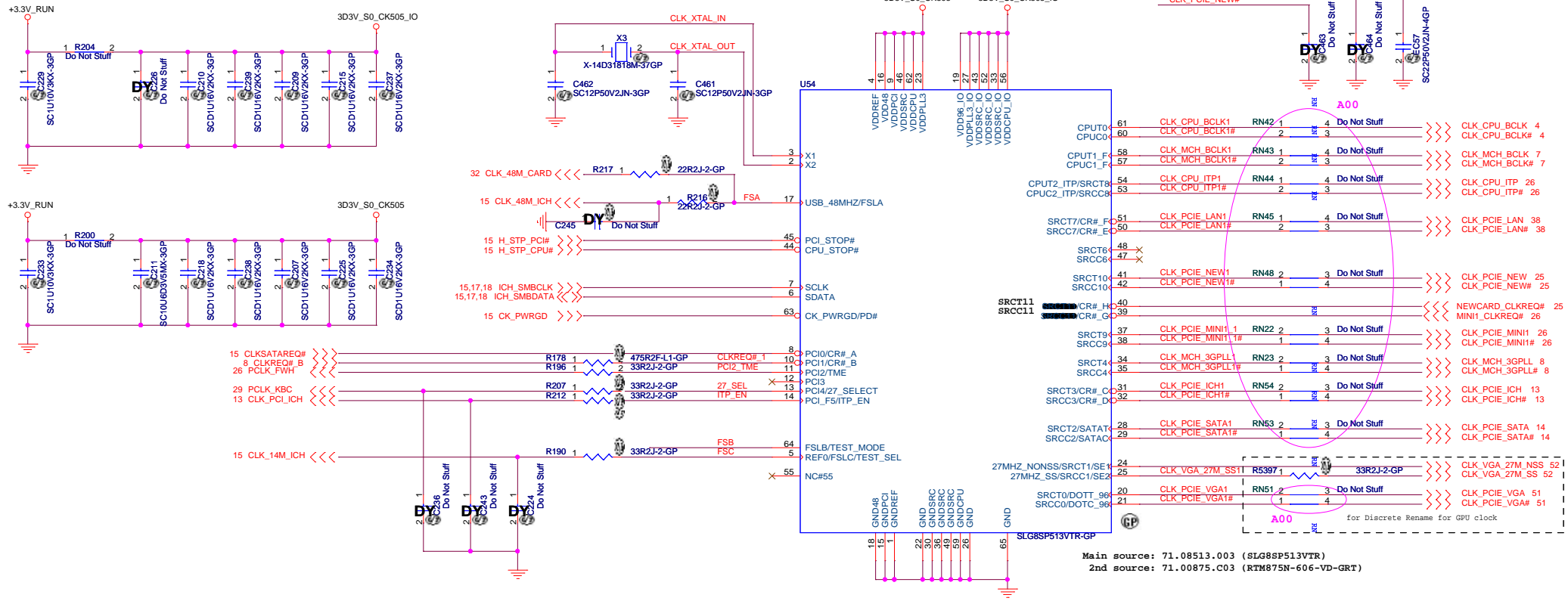
Size: Custom Document Number  
 Date: Tuesday, May 19, 2009  
 Sheet 17 of 60

Rev: -1

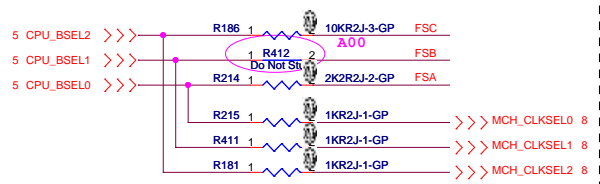
Roberts Discrete



# SSID = CLOCK



SEL2	SEL1	SEL0	CPU	FSB
FSC	FSB	FSA		
1	0	1	100M	X
0	0	1	133M	533M
0	1	1	166M	667M
0	1	0	200M	800M
0	0	0	266M	1067M



Main Source

**DELL** Wistron Corporation  
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File: **Clock Generator SLG8SP513VTR**

Size: Custom Document Number  
Date: Tuesday, May 19, 2009 Sheet 19 of 60


Rev: -1

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		<b>Wistron Corporation</b>	
		21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title		<b>CRT</b>	
Size	Document Number	Rev	
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Date:	Tuesday, May 19, 2009	Sheet	21 of 60

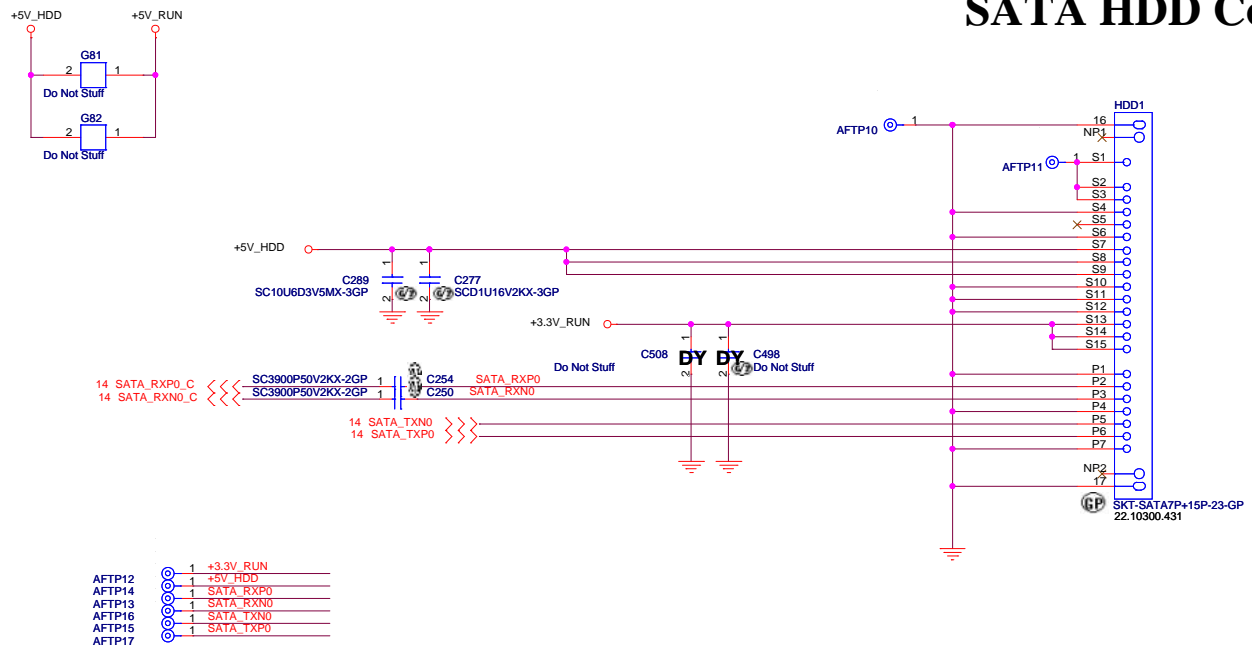
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		<b>Wistron Corporation</b>	
		21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title		<b>HDMI</b>	
Size	Document Number	Rev	
Custom	<b>Roberts Discrete</b>	<b>-1</b>	
Date:	Tuesday, May 19, 2009	Sheet	22 of 60

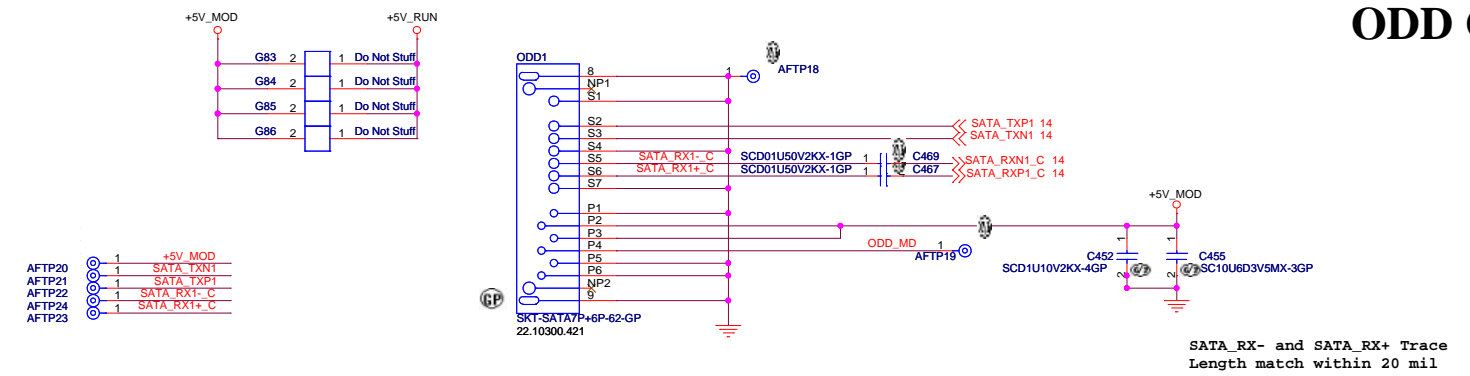
SSID = SATA

# SATA HDD Connector



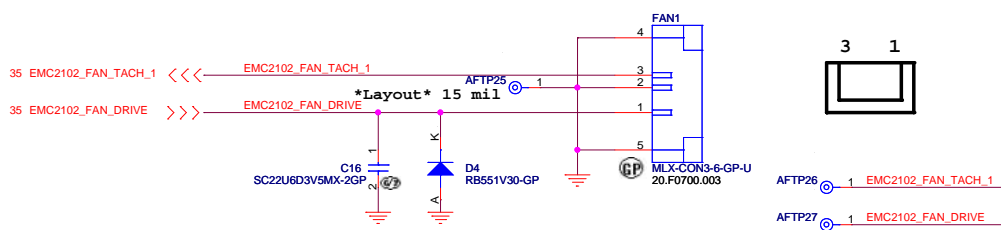
SSID = SATA

# ODD Connector



SSID = Thermal

# Fan Connector



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Title: **HDD/ODD/FAN**

Size	Document Number	Rev
Custom	<b>Roberts Discrete</b>	-1
Date:	Tuesday, May 19, 2009	Sheet 23 of 60

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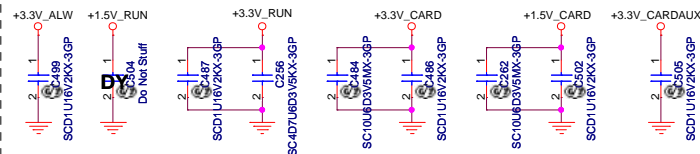
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		<b>Wistron Corporation</b>	
		21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title		<b>PCI</b>	
Size	Document Number	Rev	
Custom	<b>Roberts Discrete</b>	<b>-1</b>	
Date:	Tuesday, May 19, 2009	Sheet	24 of 60

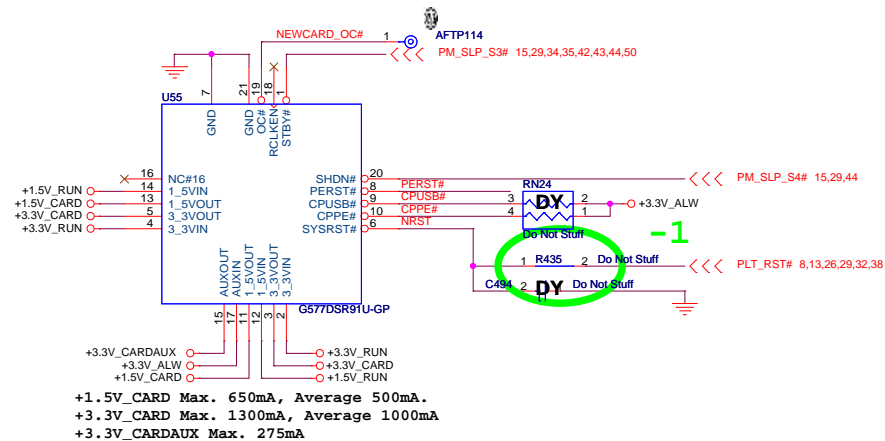


# SSID = ExpressCard

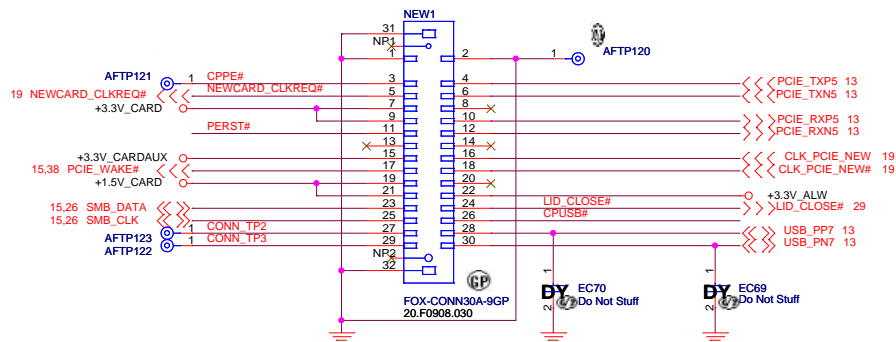
Place them Near to Chip



- AFTP92 PCIE\_TXP5
- AFTP96 PCIE\_TXN5
- AFTP95 PCIE\_RXP5
- AFTP98 PCIE\_RXN5
- AFTP97 CLK\_PCIE\_NEW
- AFTP100 CLK\_PCIE\_NEW#
- AFTP99 +3.3V\_ALW
- AFTP101 LID\_CLOSE#
- AFTP102 CPUSS#
- AFTP103 USB\_PP7
- AFTP104 USB\_PN7
- AFTP105 NEWCARD\_CLKREQ#
- AFTP106 +3.3V\_CARD
- AFTP108 PERST#
- AFTP110 +3.3V\_CARDAUX
- AFTP110 PCIE\_WAKE#
- AFTP109 +1.5V\_CARD
- AFTP112 SMB\_DATA
- AFTP111 SMB\_CLK
- AFTP113

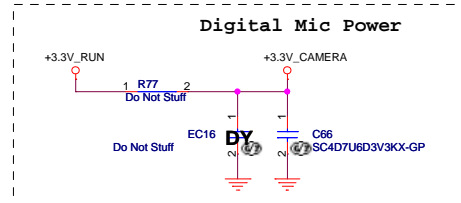
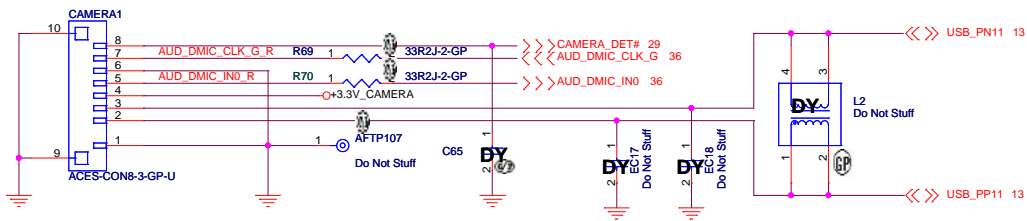


# New Card Connector



# Camera Connector

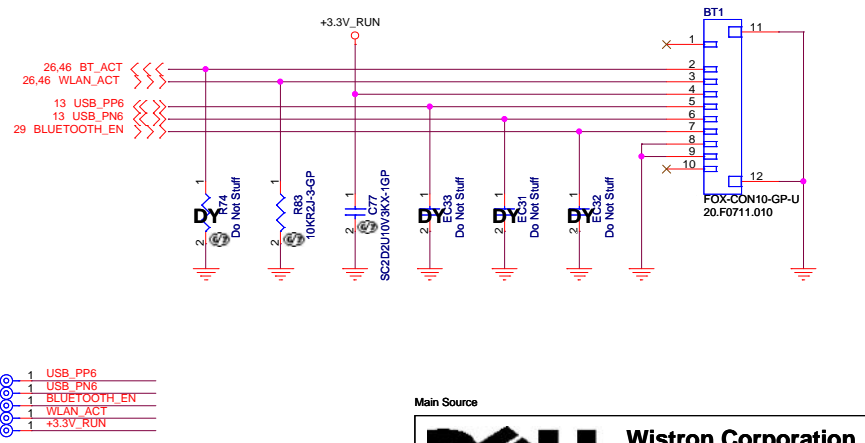
# SSID = User.Interface



- AFTP88 CAMERA\_DET#
- AFTP89 AUD\_MIC\_CLK\_G
- AFTP90 AUD\_MIC\_IN0\_R
- AFTP91 +3.3V\_CAMERA
- AFTP91 USB\_PN11
- AFTP93 USB\_PP11
- AFTP94

# SSID = User.Interface

# Bluetooth Module conn.



- AFTP116 USB\_PP6
- AFTP116 USB\_PN6
- AFTP117 BLUETOOTH\_EN
- AFTP117 WLAN\_ACT
- AFTP118 USB\_PP7
- AFTP119 USB\_PN7

Main Source

**Wistron Corporation**  
 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,  
 Taipei Hsien 221, Taiwan, R.O.C.


File: **Bluetooth/CAM/New Card**

Size	Document Number	Rev
Custom	<b>Roberts Discrete</b>	-1
Date:	Tuesday, May 19, 2009	Sheet 25 of 60




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		<b>Wistron Corporation</b>	
		21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title		<b>WWAN</b>	
Size	Document Number	Rev	
Custom	<b>Roberts Discrete</b>	<b>-1</b>	
Date:	Tuesday, May 19, 2009	Sheet	27 of 60

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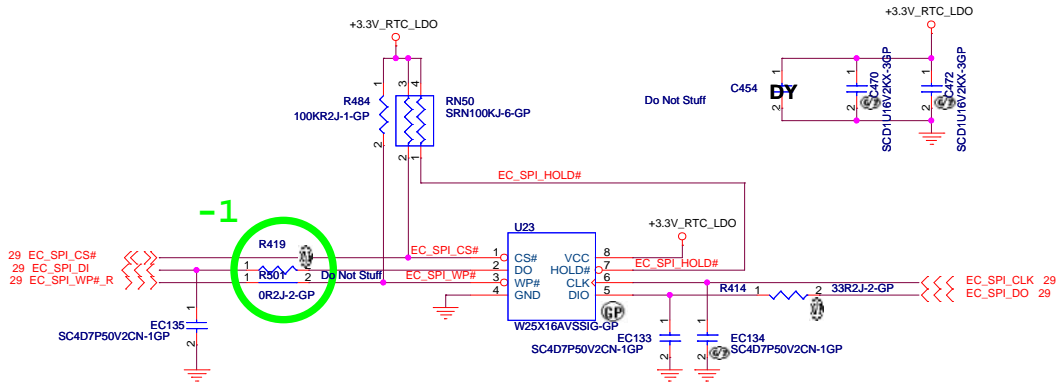
Main Source

		<b>Wistron Corporation</b>	
		21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title		<b>WPAN</b>	
Size	Document Number	Rev	
Custom	<b>Roberts Discrete</b>	<b>-1</b>	
Date:	Tuesday, May 19, 2009	Sheet	28 of 60



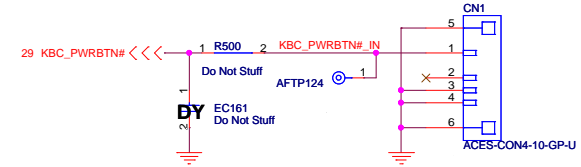
# SPI FLASH ROM (16M bits)

SSID = Flash.ROM



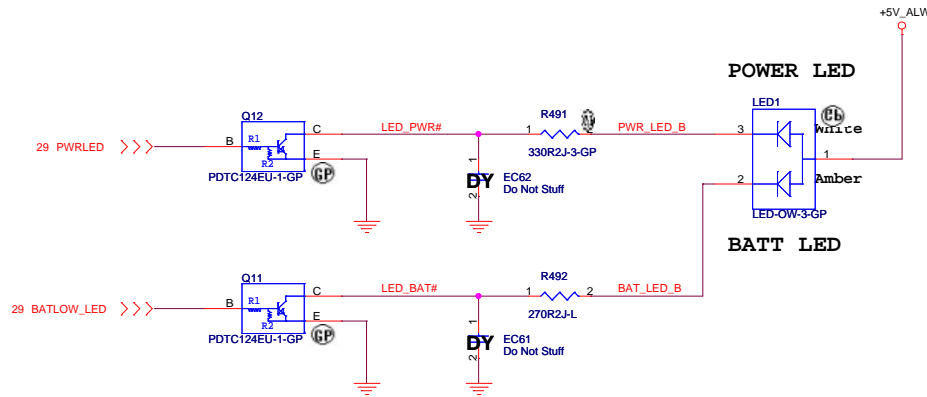
SSID = User.Interface

# Power Board to Board CONN



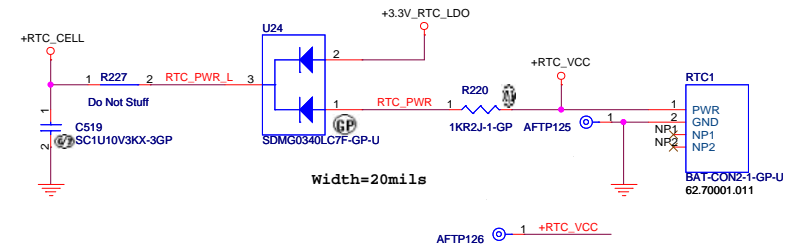
SSID = User.Interface

# Power/Battery LED



SSID = RBATT

# RTC Connector



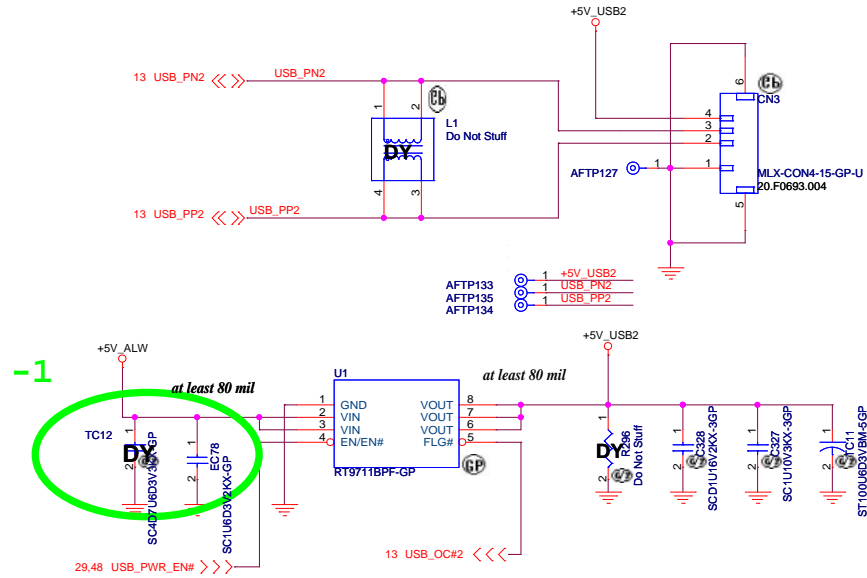
Main Source



Title			FWH/LED/Power Dash/RTC		
Size	Document Number		Rev		
Custom	Roberts Discrete				-1
Date:	Tuesday, May 19, 2009	Sheet	30	of	60

**SSID = USB**

### Right USB Port CONN

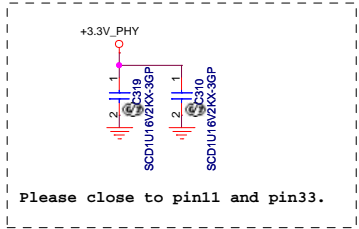


Main Source

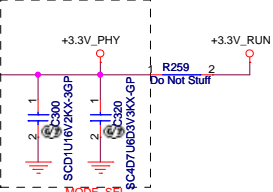


File		<b>USB</b>	
Size	Document Number	Rev	
Custom	<b>Roberts Discrete</b>	<b>-1</b>	
Date	Tuesday, May 19, 2009	Sheet	31 of 60

**SSID = SDIO**



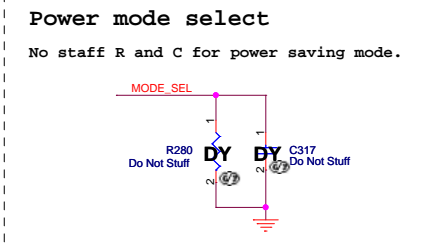
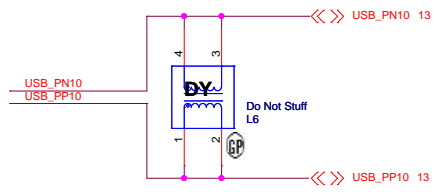
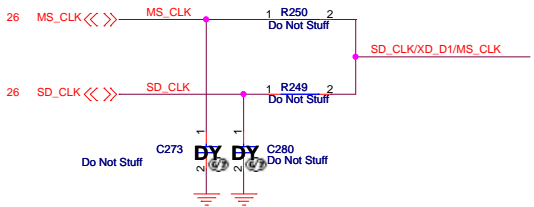
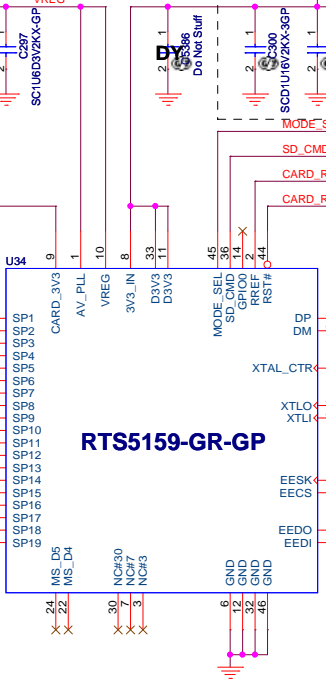
Please close to pin8.



- 26 XD\_CD#
- 26 SD\_WP
- 26 SD\_CD#
- 26 XD\_D4/SD\_DAT1
- 26 XD\_D5/MS\_BS
- 26 XD\_D3/MS\_D1
- 26 SD\_DAT0/XD\_D6/MS\_D0
- 26 XD\_D2/MS\_D2
- 26 MS\_INS#
- 26 XD\_D7/MS\_D3
- 26 SD\_CLK/XD\_D1/MS\_CLK
- 26 XD\_D0
- 26 XD\_WP#
- 26 XD\_RDY
- 26 SD\_DAT3/XD\_WE#
- 26 SD\_DAT2/XD\_RE#
- 26 XD\_ALE
- 26 XD\_CEP
- 26 XD\_CLE

- XD\_CD#
- SD\_WP
- SD\_CD#
- XD\_D4/SD\_DAT1
- XD\_D5/MS\_BS
- XD\_D3/MS\_D1
- SD\_DAT0/XD\_D6/MS\_D0
- XD\_D2/MS\_D2
- MS\_INS#
- XD\_D7/MS\_D3
- SD\_CLK/XD\_D1/MS\_CLK
- XD\_D0
- XD\_WP#
- XD\_RDY
- SD\_DAT3/XD\_WE#
- SD\_DAT2/XD\_RE#
- XD\_ALE
- XD\_CEP
- XD\_CLE

**RTS5159-GR-GP**



Main Source

**DELL** Wistron Corporation  
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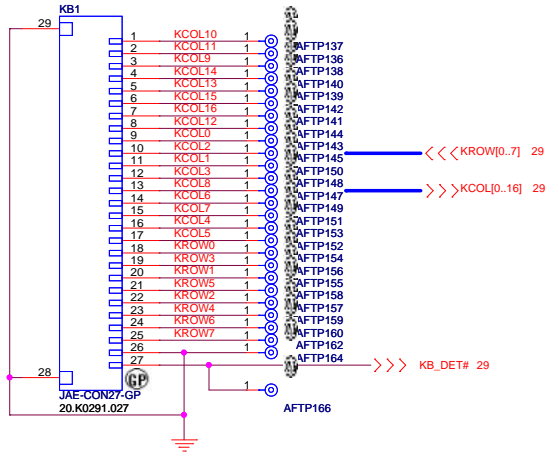
File: **RTS5158E**

Size	Document Number	Rev
Custom	<b>Roberts Discrete</b>	<b>-1</b>
Date:	Tuesday, May 19, 2009	Sheet 32 of 60



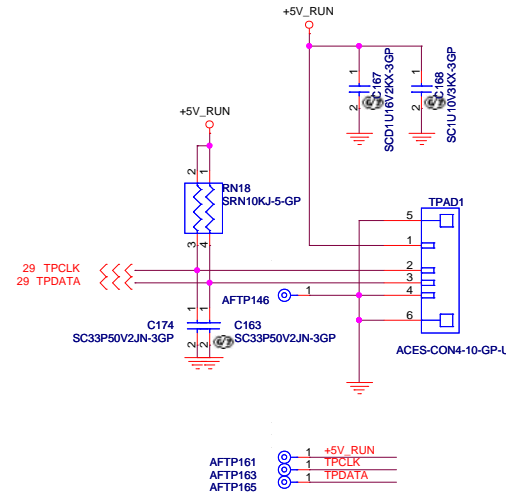
SSID = KBC

### Internal KeyBoard Connector

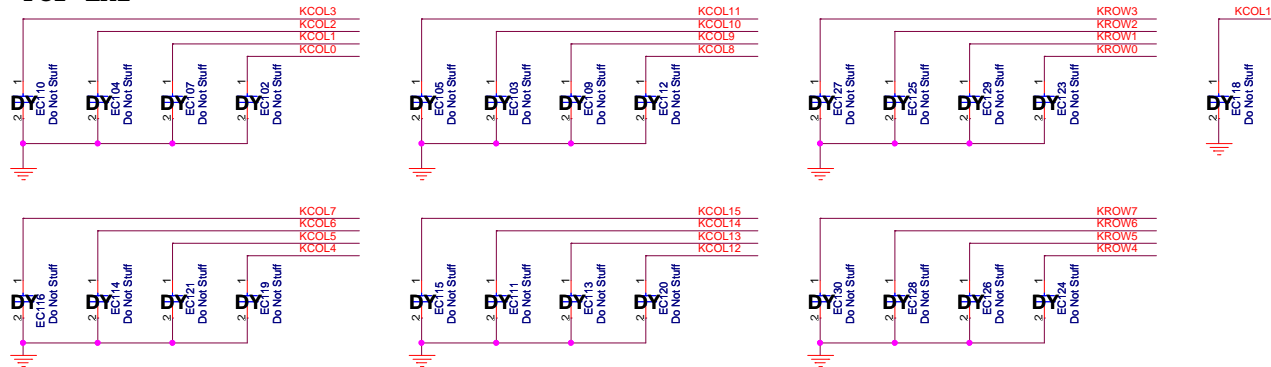


SSID = Touch.Pad

### TouchPad Connector



### For EMI



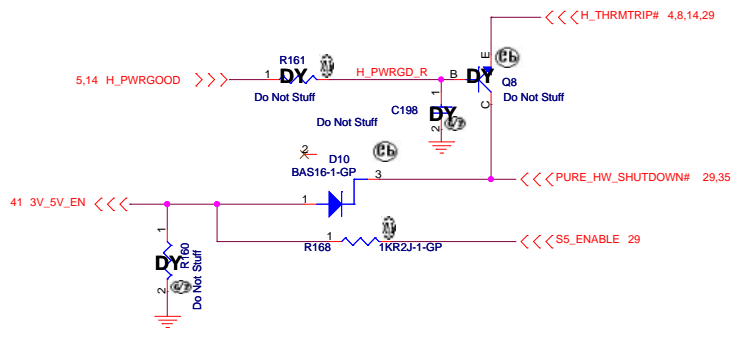
Main Source

**DELL** Wistron Corporation  
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,  
Taipei Hsien 221, Taiwan, R.O.C.

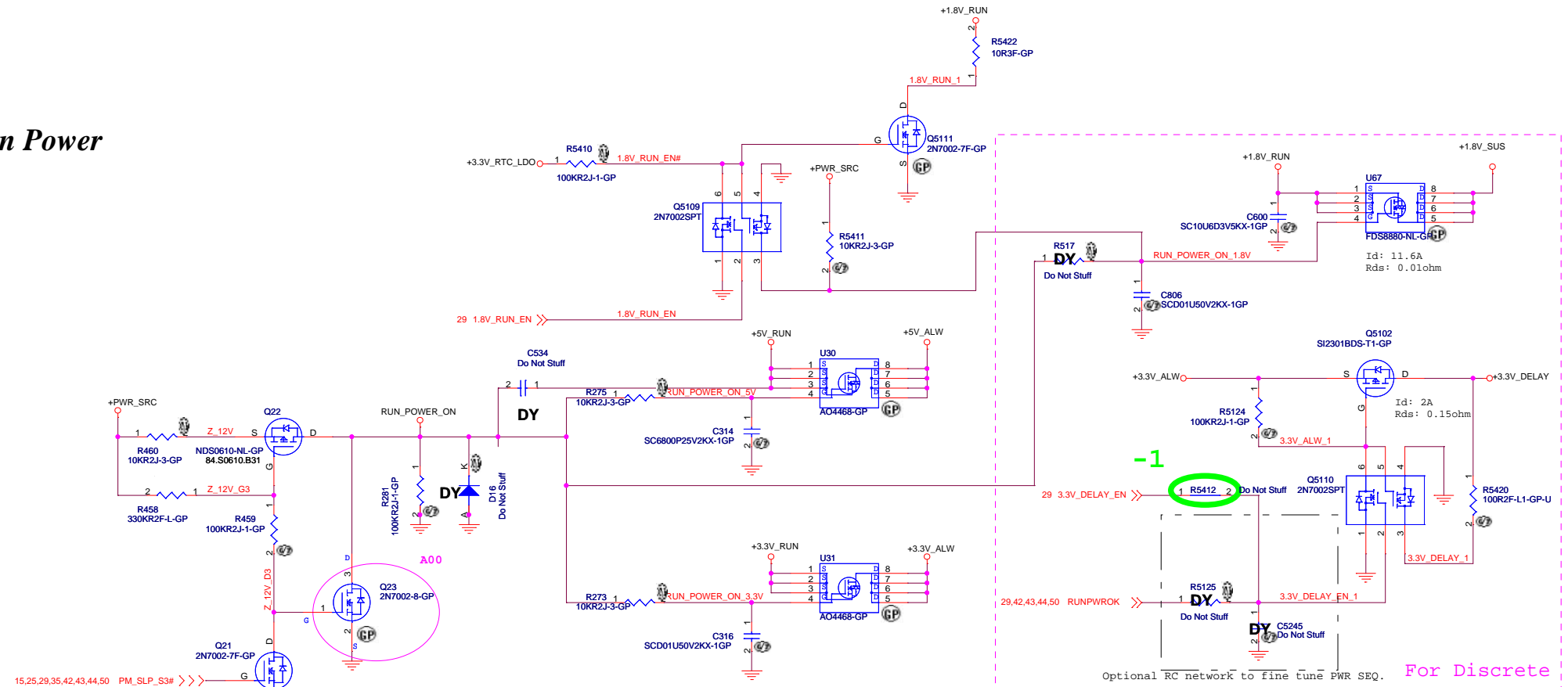
File: **KeyBoard/Touch Pad**

Size	Document Number	Rev
Custom	<b>Roberts Discrete</b>	-1
Date:	Tuesday, May 19, 2009	Sheet 33 of 60

**SSID = Reset.Suspend**



**Run Power**



Main Source

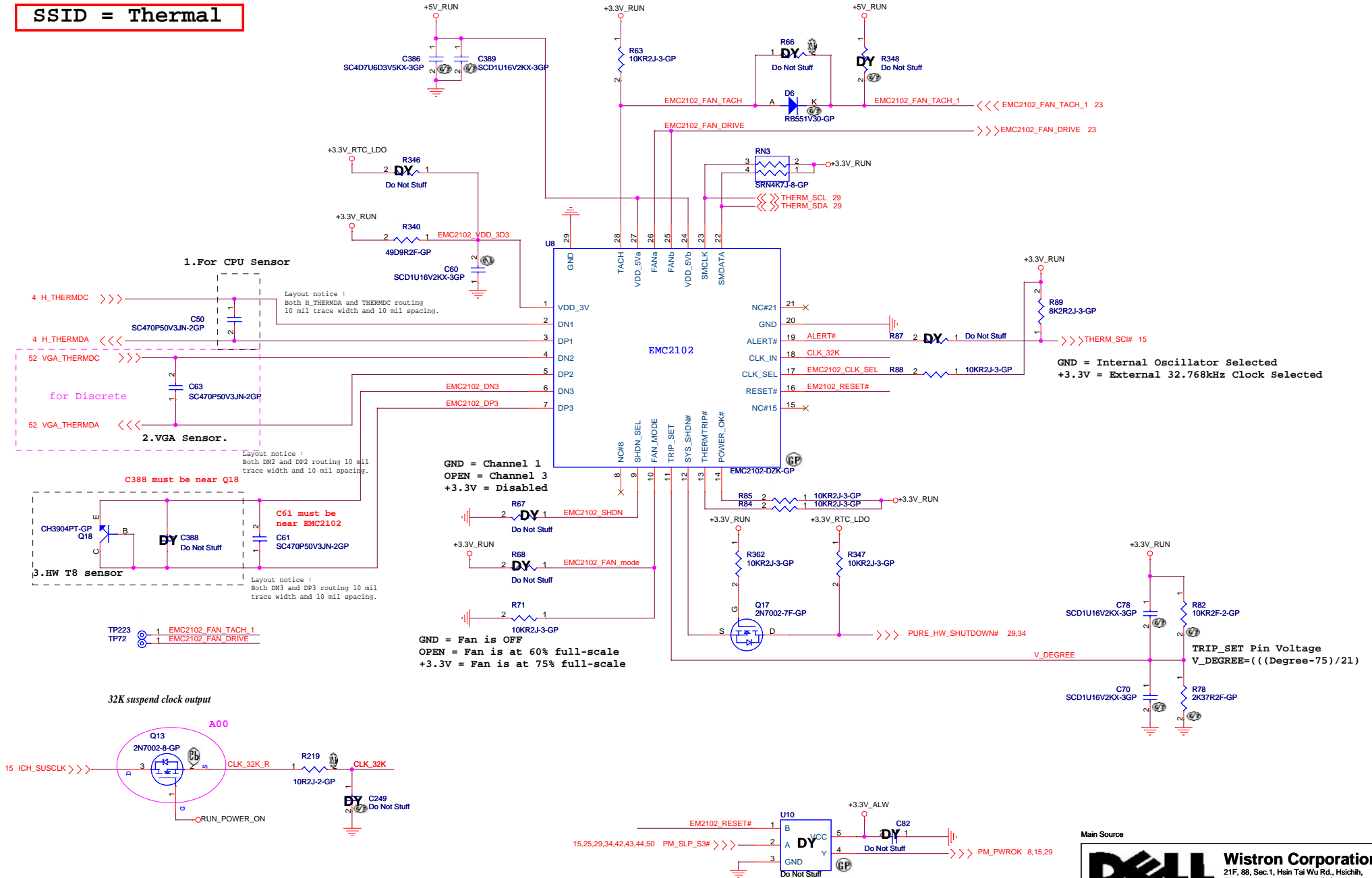
**DELL** Wistron Corporation  
 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,  
 Taipei Hsien 221, Taiwan, R.O.C.

Title: **Power Plane Enable**

Size	Document Number	Rev
Custom	<b>Roberts Discrete</b>	-1

Date: Tuesday, May 19, 2009 Sheet 34 of 60

SSID = Thermal



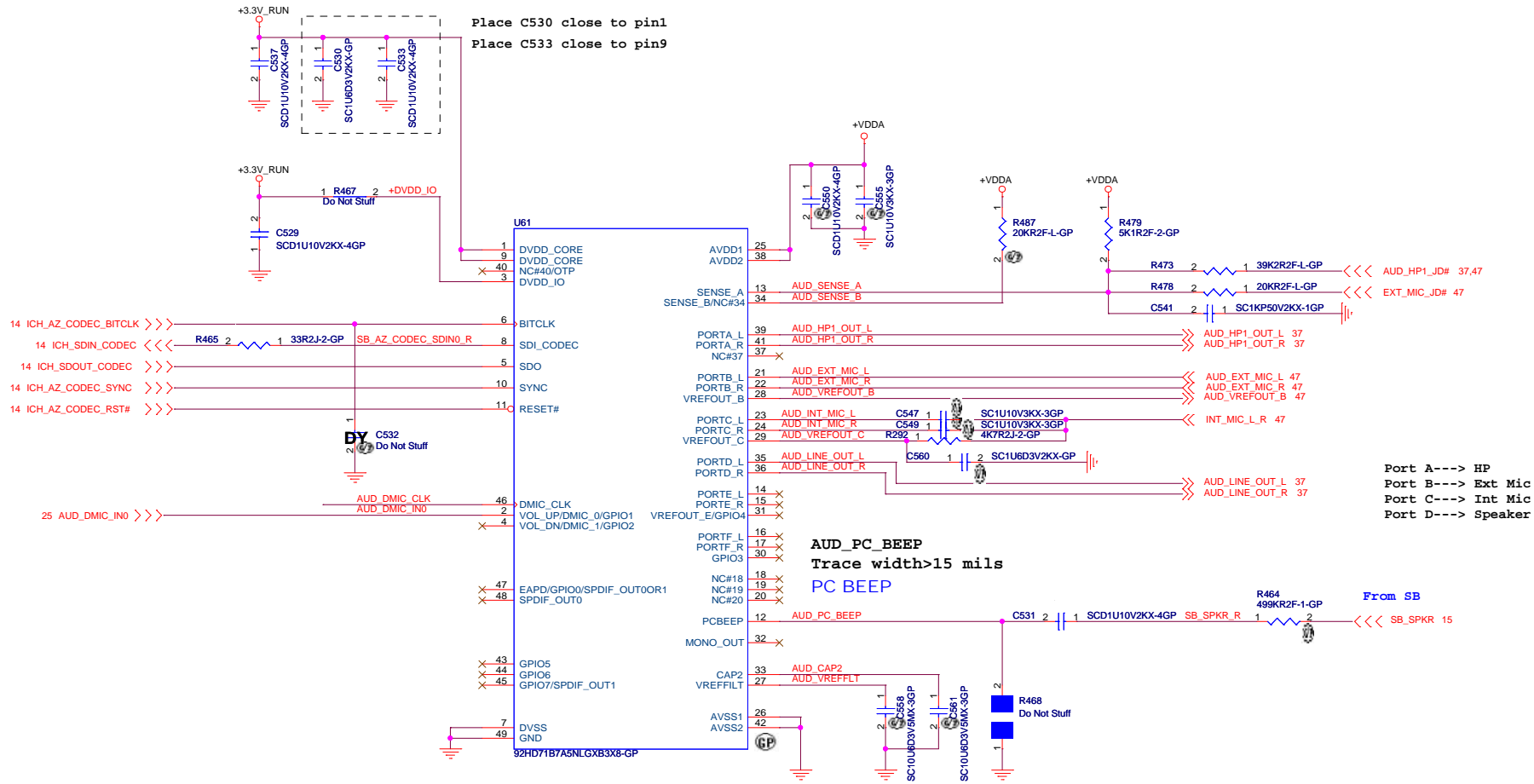
Main Source

**DELL** Wistron Corporation  
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 Taipei Hsien 221, Taiwan, R.O.C.

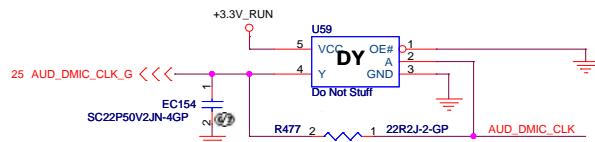
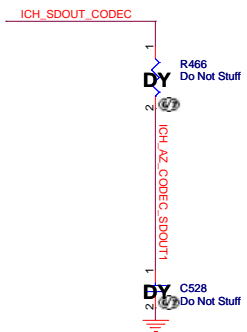
File: **Thermal EMC2102**

Size	Document Number	Rev
Custom	<b>Roberts Discrete</b>	-1
Date:	Tuesday, May 19, 2009	Sheet 35 of 60

**SSID = AUDIO**



**Azalia I/F EMI**



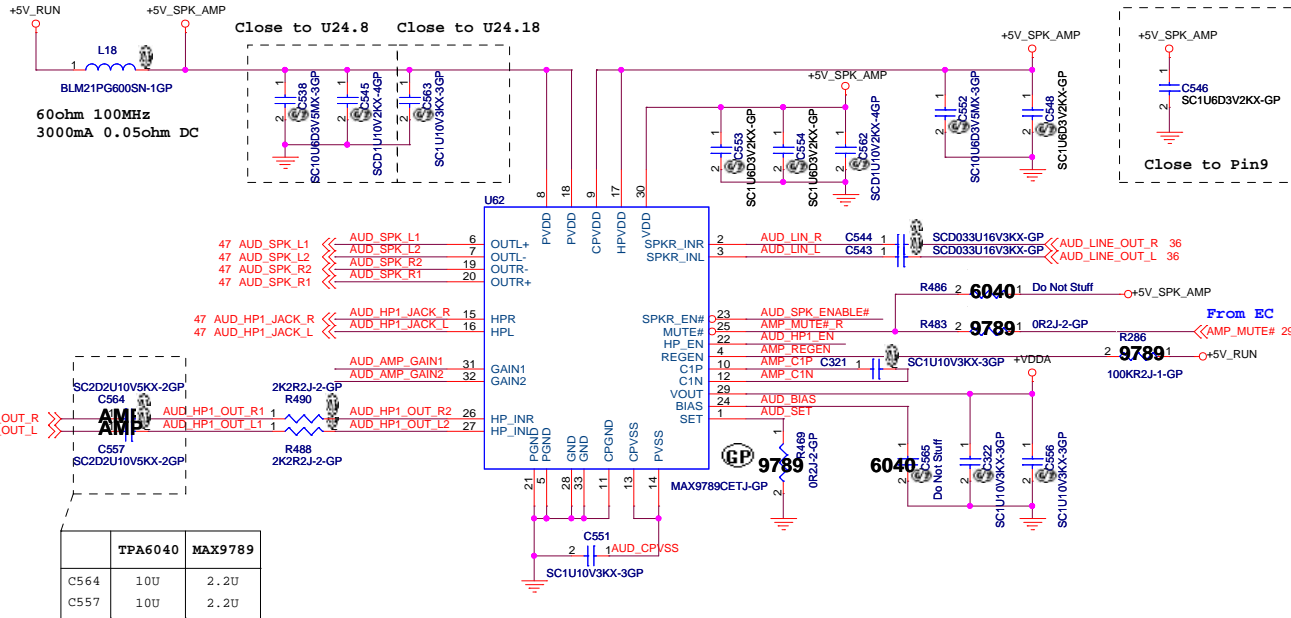
Main Source

**DELL** Wistron Corporation  
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Taipei Hsien 221, Taiwan, R.O.C.

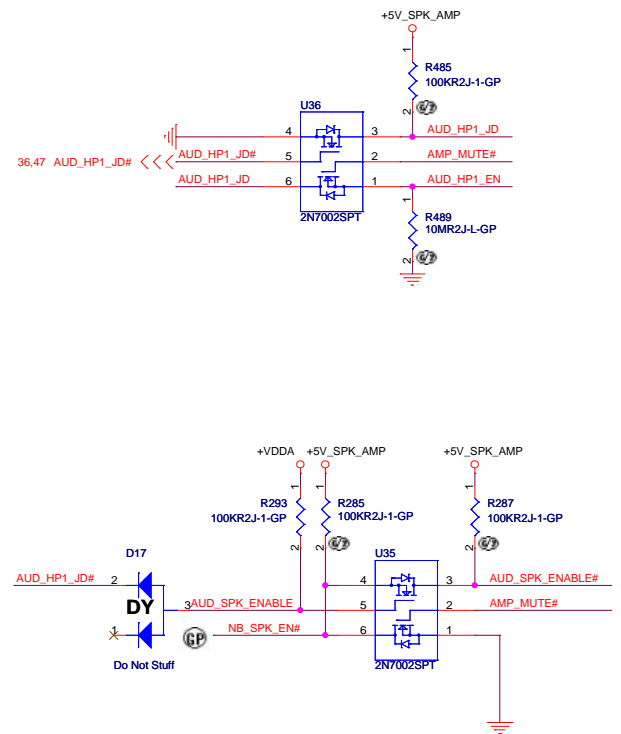
Title: **AUDIO CODEC 92HD71B7**

Size	Document Number	Rev
Custom	<b>Roberts Discrete</b>	-1
Date:	Tuesday, May 19, 2009	Sheet 36 of 60

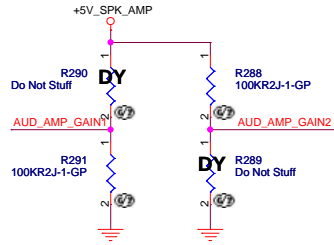
# SSID = AUDIO



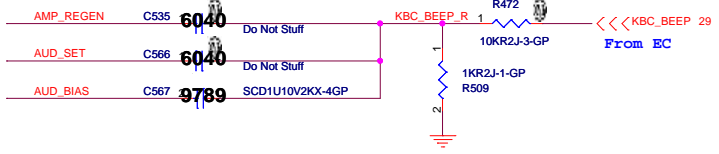
## Signal inverter for speaker shutdown



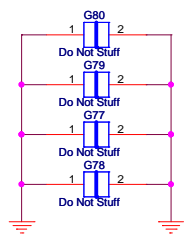
## GAIN SETTING



GAIN1	GAIN2	GAIN
0	0	6dB
0	1	10dB
1	0	15.6dB
1	1	21.6dB



	Main source	Second source
	TPA6040A (74.06040.013)	MAX9789A (74.09789.013)
R486	100K	No ASM
R483	No ASM	0 Ohm
R469	No ASM	0 Ohm
R286	No ASM	100K
C535	0.033uF	No ASM
C566	0.033uF	No ASM
C565	1uF	No ASM
C567	No ASM	0.1uF
C564	10uF	2.2uF
C557	10uF	2.2uF



Main Source

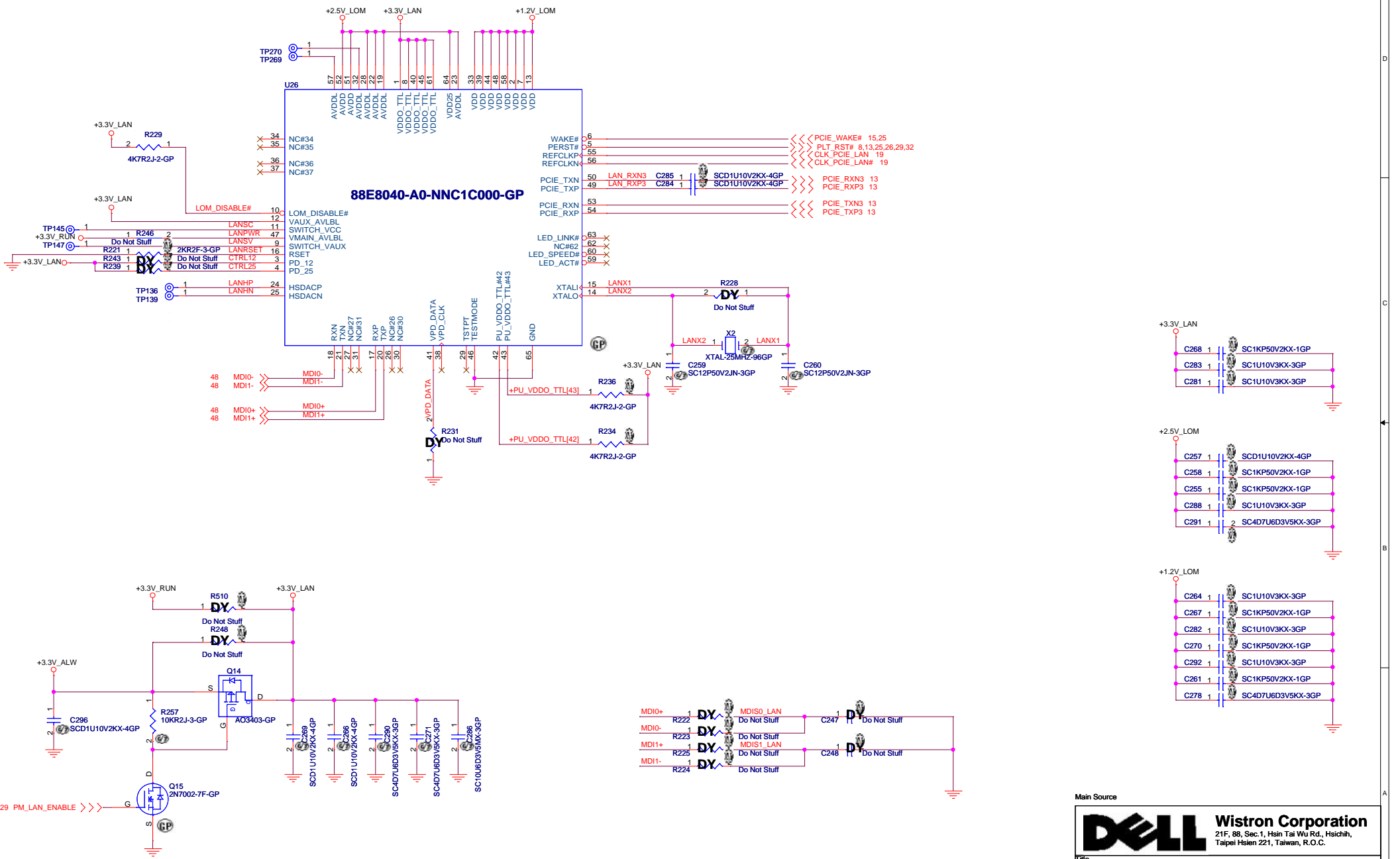
**DELL** Wistron Corporation  
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.

File: **AUDIO AMP/SPEAKER**

Size: Custom      Document Number: **Roberts Discrete**      Rev: -1

Date: Tuesday, May 19, 2009      Sheet: 37 of 60

**SSID = LOM**



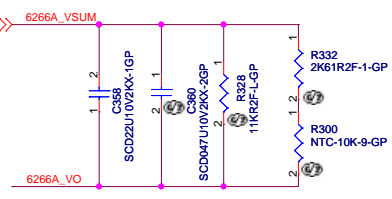
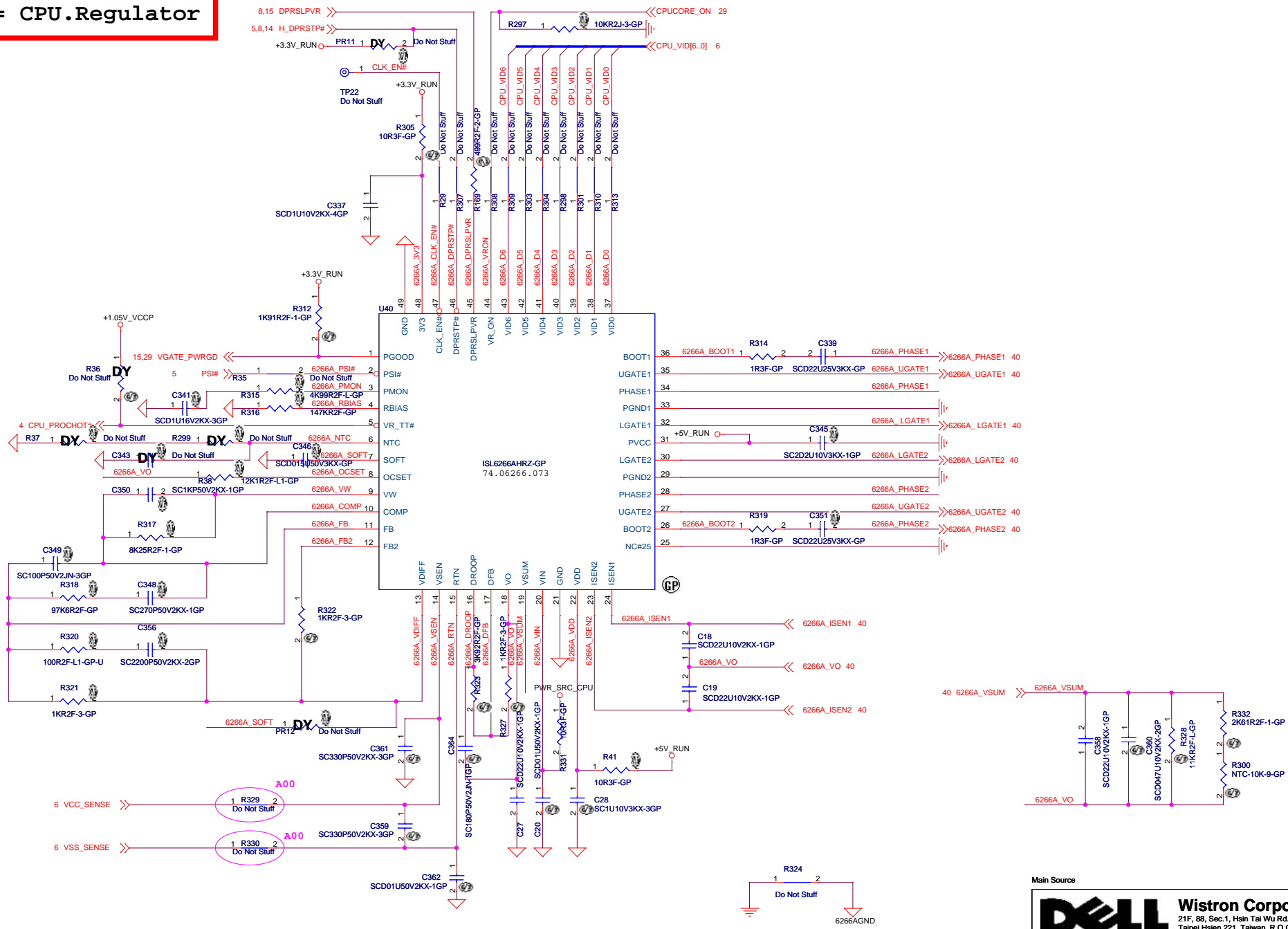
Main Source

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 Taipei Hsien 221, Taiwan, R.O.C.

File: **LAN Marvell-88E8040**

Size	Document Number	Rev
Custom	<b>Roberts Discrete</b>	-1
Date:	Tuesday, May 19, 2009	Sheet 38 of 60

**SSID = CPU.Regulator**



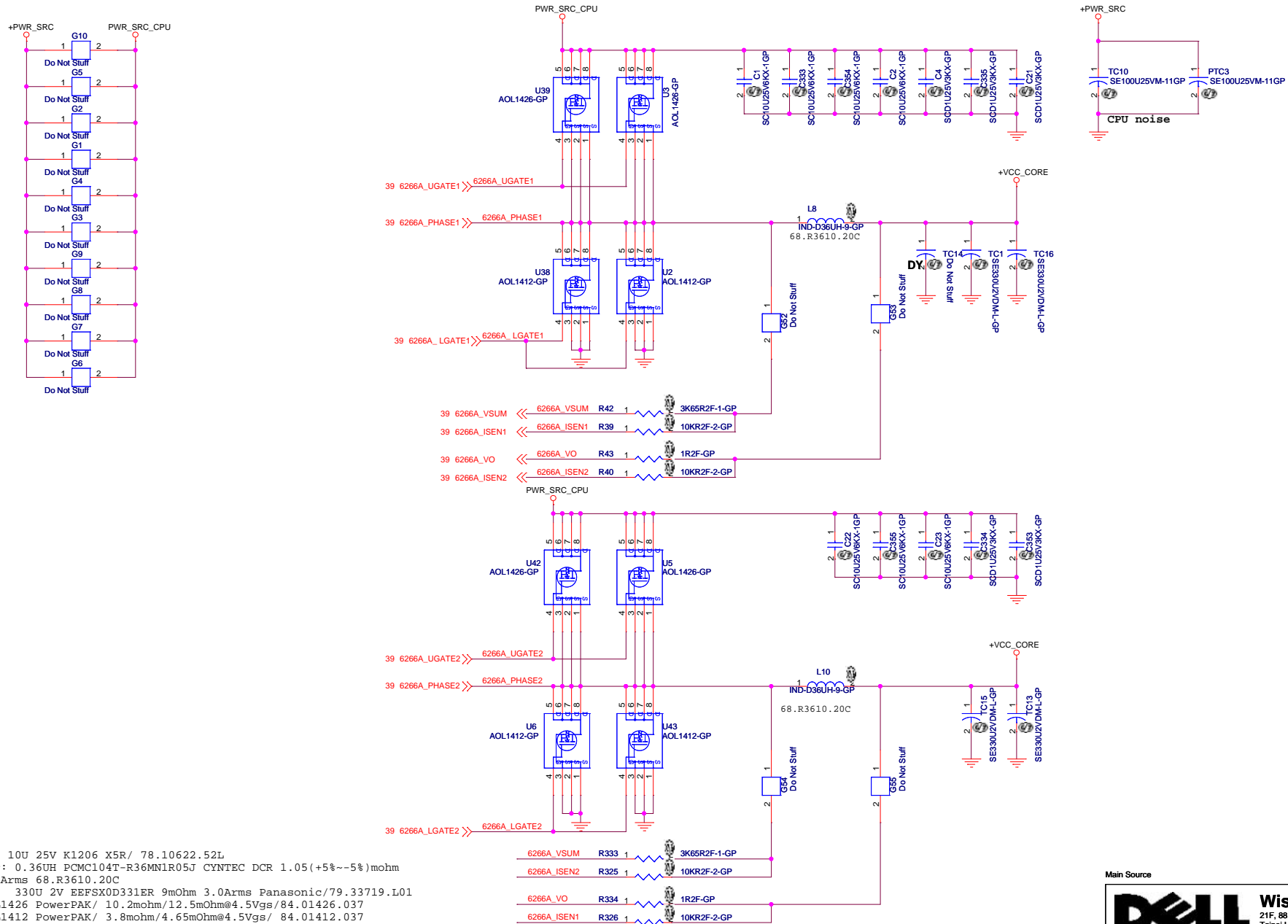
Main Source

**DELL** Wistron Corporation  
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 Taipei Hsien 221, Taiwan, R.O.C.

File: **CPU VCORE POWER(1/2)**

Size	Document Number	Rev
Custom		-1
Date:	Tuesday, May 19, 2009	Sheet 39 of 60

# SSID = CPU.Regulator



I/P cap: 10U 25V K1206 X5R/ 78.10622.52L  
 Inductor: 0.36UH PCMC104T-R36MN1R05J CYNTEC DCR 1.05(+5%~-5%)mohm  
 Isat =60Arms 68.R3610.20C  
 O/P cap: 330U 2V EEFSX0D331ER 9mOhm 3.0Arms Panasonic/79.33719.L01  
 H/S: AOL1426 PowerPAK/ 10.2mohm/12.5mOhm@4.5Vgs/84.01426.037  
 L/S: AOL1412 PowerPAK/ 3.8mohm/4.65mOhm@4.5Vgs/ 84.01412.037

Main Source

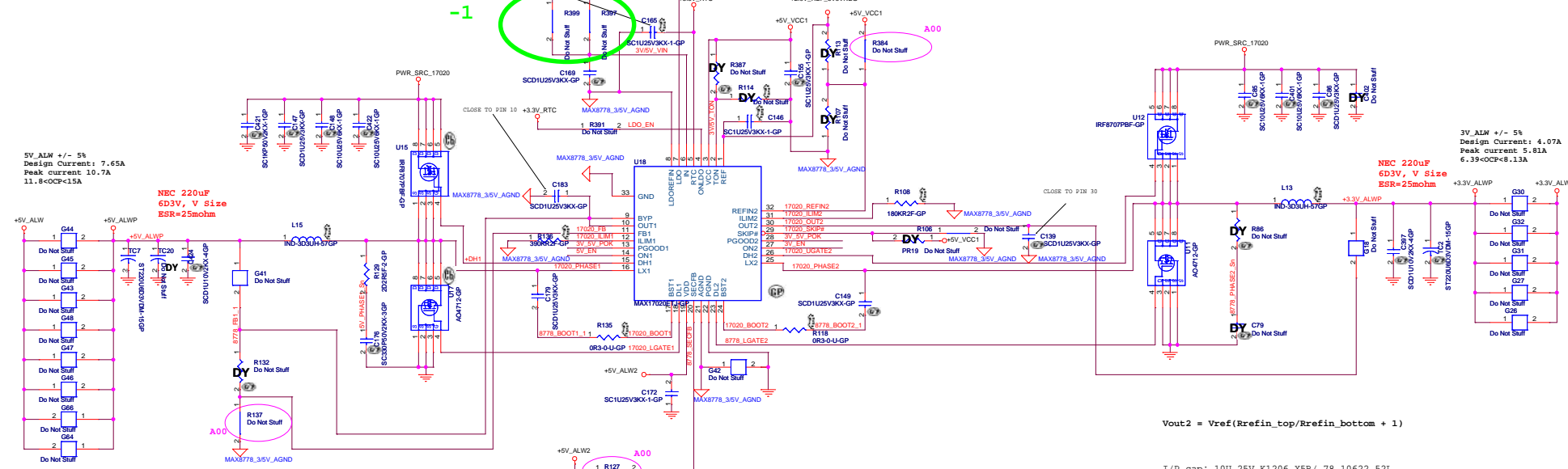
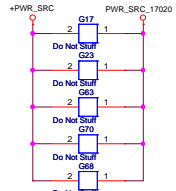
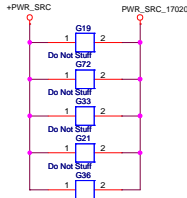
**DELL** Wistron Corporation  
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 Taipei Hsien 221, Taiwan, R.O.C.

File: **CPU Vcore POWER(2/2)**

Size	Document Number	Rev
Custom	<b>Roberts Discrete</b>	-1
Date:	Tuesday, May 19, 2009	Sheet 40 of 60



# SSID = PWR.Plane.Regulator\_3p3v5v

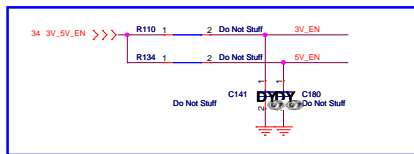


SV\_ALW +/- 5%  
Design Current: 7.65A  
Peak current 10.7A  
11.8<math>\mu\text{COP}</math>15A

NEC 220uF  
6D3V, V size  
ESR=25mohm

3V\_ALW +/- 5%  
Design Current: 4.07A  
Peak current 5.81A  
6.39<math>\mu\text{COP}</math>8.13A

$V_{out1} = 0.7(R_{top}/R_{bottom} + 1)$



$V_{out2} = V_{ref}(R_{refin\_top}/R_{refin\_bottom} + 1)$

I/P cap: 10u 25V K1206 X5R/ 78.10622.52L  
Inductor: 3.3uH PCMC063T3R3MN CYNTEC DCR 28-30mohm Isat =13.5Arms 68.3R310.20A  
O/P cap: 220U 6.3V PSLVQJ227M(25) 25mohm 2.236Arms NEC\_TOKIN/77.C2271.00L  
O/P cap: 150U 6.3V PSLB20J157M(45) 45mohm 1.374Arms NEC\_TOKIN/77.C1571.09L  
H/S: IRF8707 SO-8/ 14.2mohm/17.5mohm@4.5Vgs/ 84.08707.037  
L/S: AOS4712 SO-8/ 15mohm/18mohm@4.5Vgs/ 84.04712.037

I/P cap: 10U 25V K1206 X5R/ 78.10622.52L  
Inductor: 3.3UH PCMC063T3R3MN CYNTEC DCR 28-30mohm Isat =13.5Arms 68.3R310.20A  
O/P cap: 220U 6.3V PSLVQJ227M(25) 25mohm 2.236Arms NEC\_TOKIN/77.C2271.00L  
O/P cap: 150U 6.3V PSLB20J157M(45) 45mohm 1.374Arms NEC\_TOKIN/77.C1571.09L  
H/S: IRF8707 SO-8/ 14.2mohm/17.5mohm@4.5Vgs/ 84.08707.037  
L/S: AOS4712 SO-8/ 15mohm/18mohm@4.5Vgs/ 84.04712.037

SKIPSEL	GND	Open/REF (2V)	High (VCC or 3.3V)
Operating Mode	pulse-skipping mode	ultrasonic mode	forced-PWM operation
TONSEL	GND	Open (REF)	High (VCC)
CH1 Freq	400kHz	400kHz	200kHz
CH2 Freq	500kHz	300kHz	300kHz

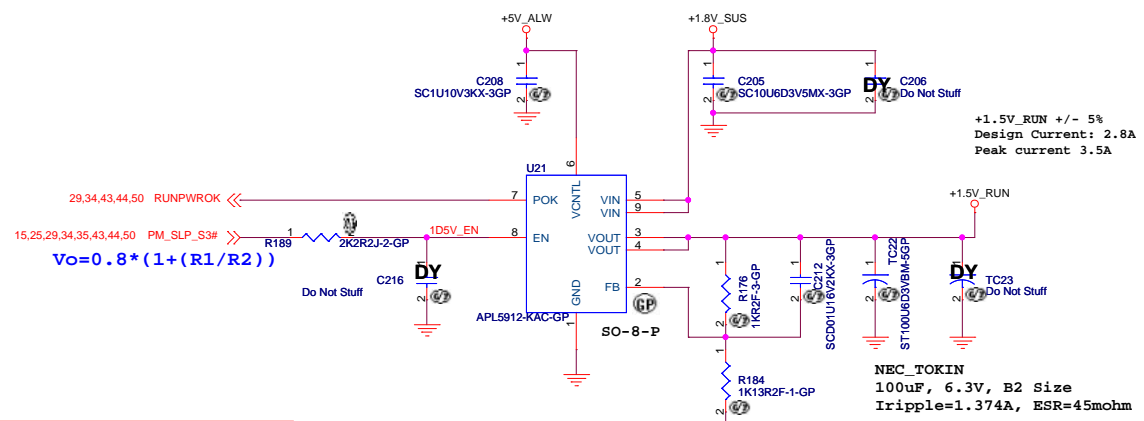
LDOREFIN	GND	VCC	VLDOREFIN = 0.5V
Operating Mode	4.90/5.0/5.10	3.23/3.3/3.37	0.96/1.0/1.04
FB1	GND	VCC	
Operating Mode	4.925/5.00/5.075	1.482/1.50/1.518	

REFIN2	5V	RTC (3.3V)	
Operating Mode	3.255/3.30/3.345	1.038/1.050 /1.062	

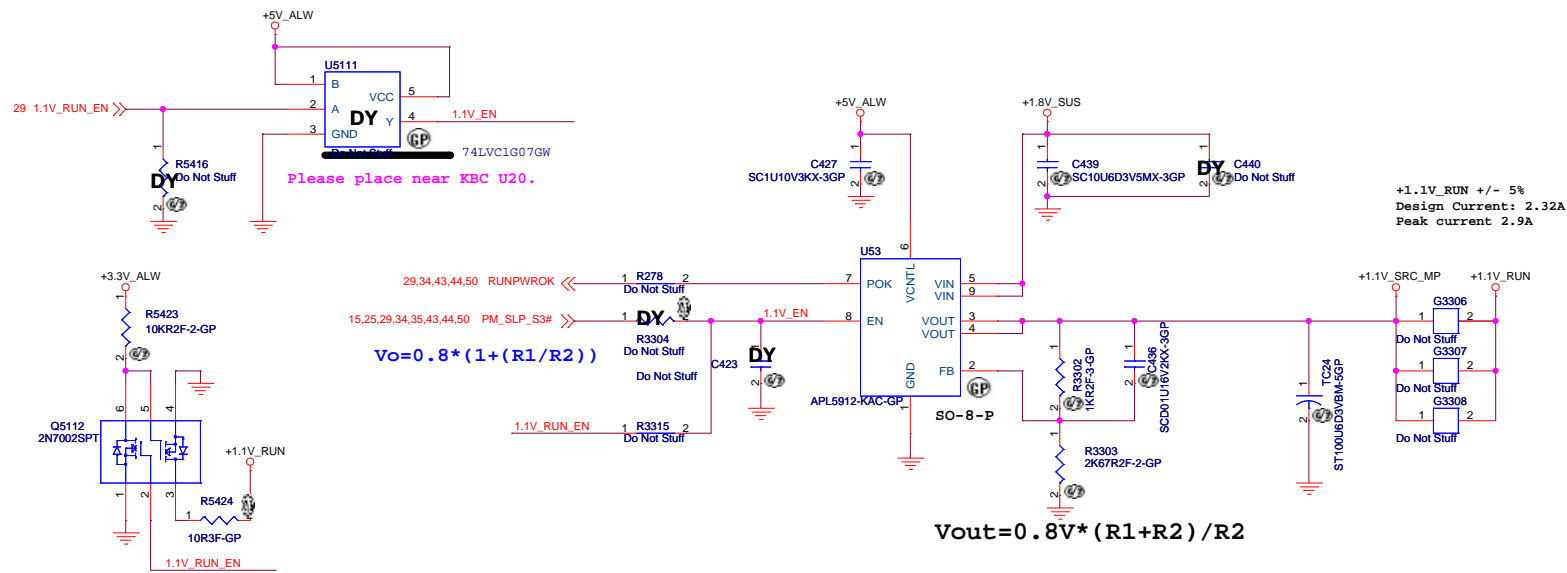
Main Source

**DC to DC 3.3V/5V**  
Roberts Discrete

**SSID = PWR.Plane.Regulator\_1p5v**



**SSID = PWR.Plane.Regulator\_1p1v**



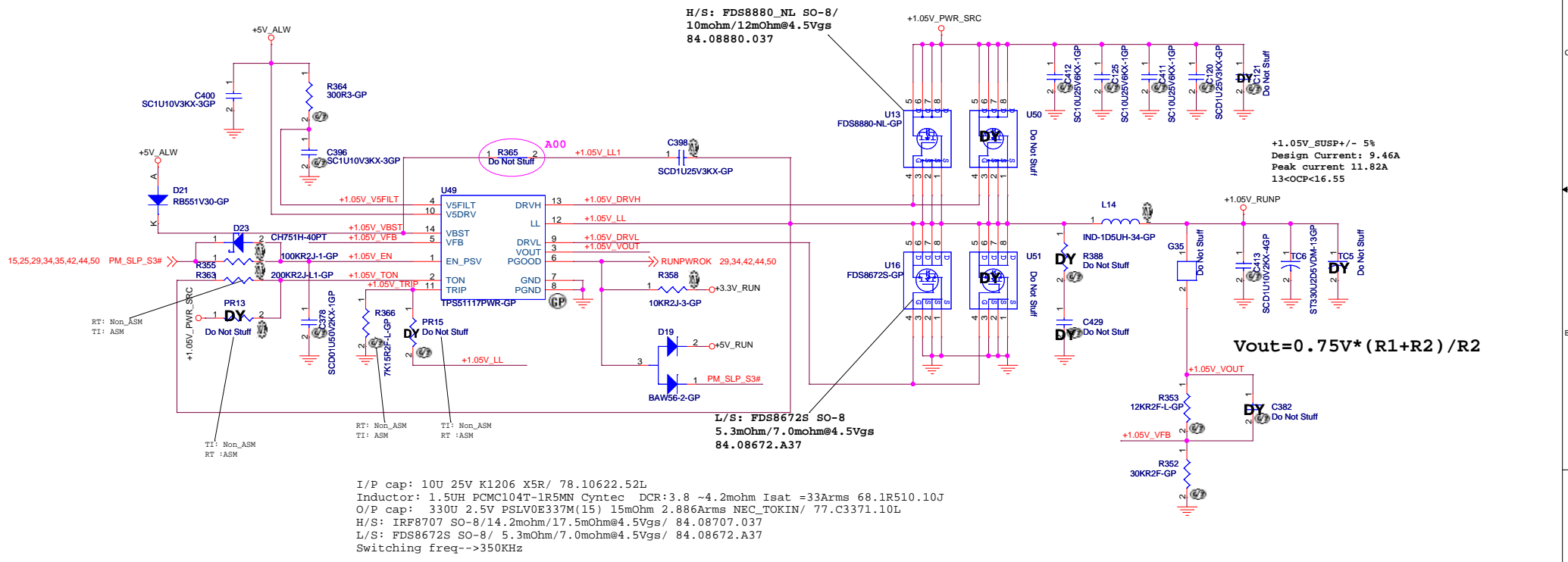
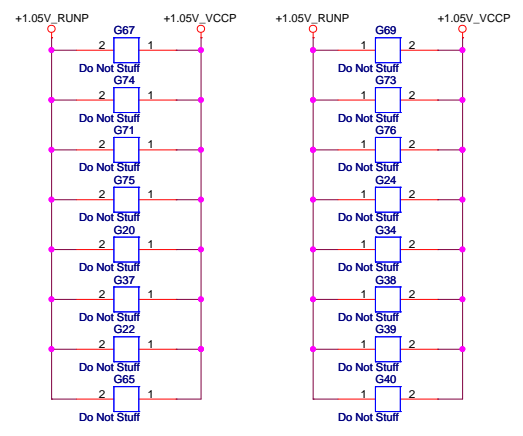
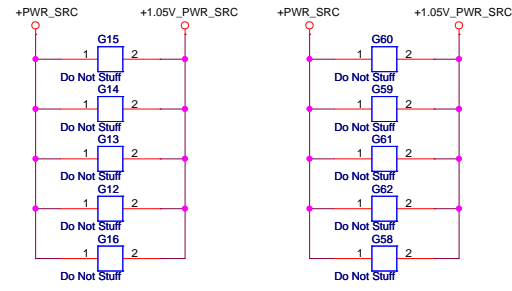
Main Source

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File: **DC to DC 1.5V/1.1V**

Size	Document Number	Rev
Custom	<b>Roberts Discrete</b>	-1
Date:	Tuesday, May 19, 2009	Sheet 42 of 60

# SSID = PWR.Plane.Regulator\_1p05v



Main Source

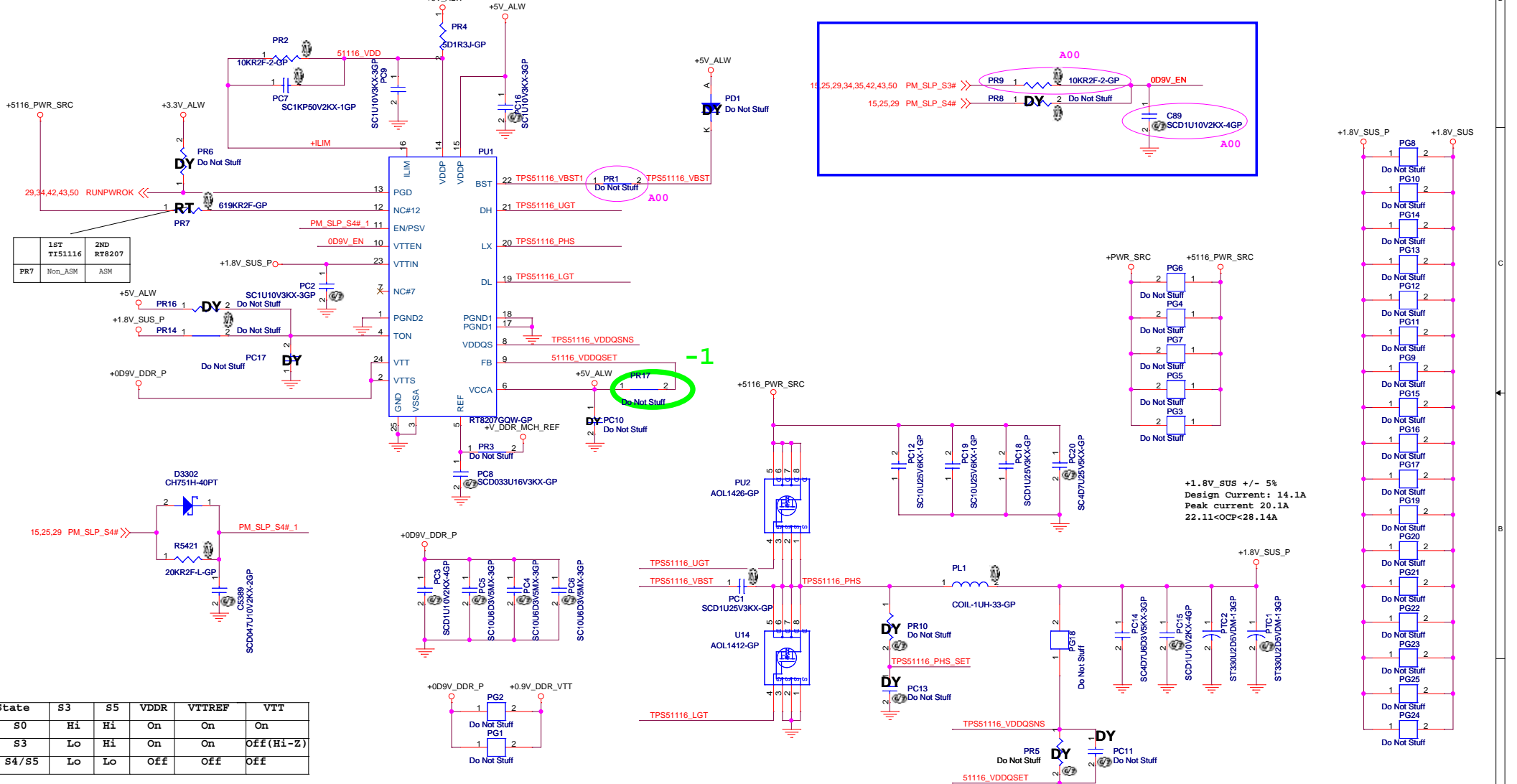
**Wistron Corporation**  
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Taipei Hsien 221, Taiwan, R.O.C.

File: **DC to DC 1.05V**

Size	Document Number	Rev
Custom	<b>Roberts Discrete</b>	-1
Date:	Tuesday, May 19, 2009	Sheet 43 of 60

**SSID = PWR.Plane.Regulator\_1p8v0p9v**

**TI TPS51116 for 1.8V and 0.9V**



1ST	2ND
TI51116	RT8207
PR7	Mon_ASM
	ASM

State	S3	S5	VDDR	VTTREF	VTT
S0	Hi	Hi	On	On	On
S3	Lo	Hi	On	On	Off(Hi-Z)
S4/S5	Lo	Lo	Off	Off	Off

VDDQSET	VDDQ (V)	VTTREF and VTT	NOTE
GND	2.5	VVDDQSNS/2	DDR
V5IN	1.8	VVDDQSNS/2	DDR2
FB Resistors	Adjustable	VVDDQSNS/2	1.5 V < VVDDQ < 3 V

I/P cap: 10U 25V K1206 X5R/ 78.10622.52L  
 Inductor: 0.82UH PCMC063T-R82MN Cynotec DCR:14~15mohm Isat =18Arms 68.R8210.10V  
 O/P cap: 330U 2.5V PSLV0E337M(15) 15mOhm 2.886Arms NEC\_TOKIN/ 77.C3371.10L  
 H/S: AOL1426 PowerPAK/ 10.2mohm/12.5mOhm@4.5Vgs/84.01426.037  
 L/S: AOL1412 PowerPAK/ 3.8mohm/4.65mOhm@4.5Vgs/ 84.01412.037  
 Switching freq-->400KHz

+1.8V\_SUS +/- 5%  
 Design Current: 14.1A  
 Peak current: 20.1A  
 22.11<OCP<28.14A

Main Source

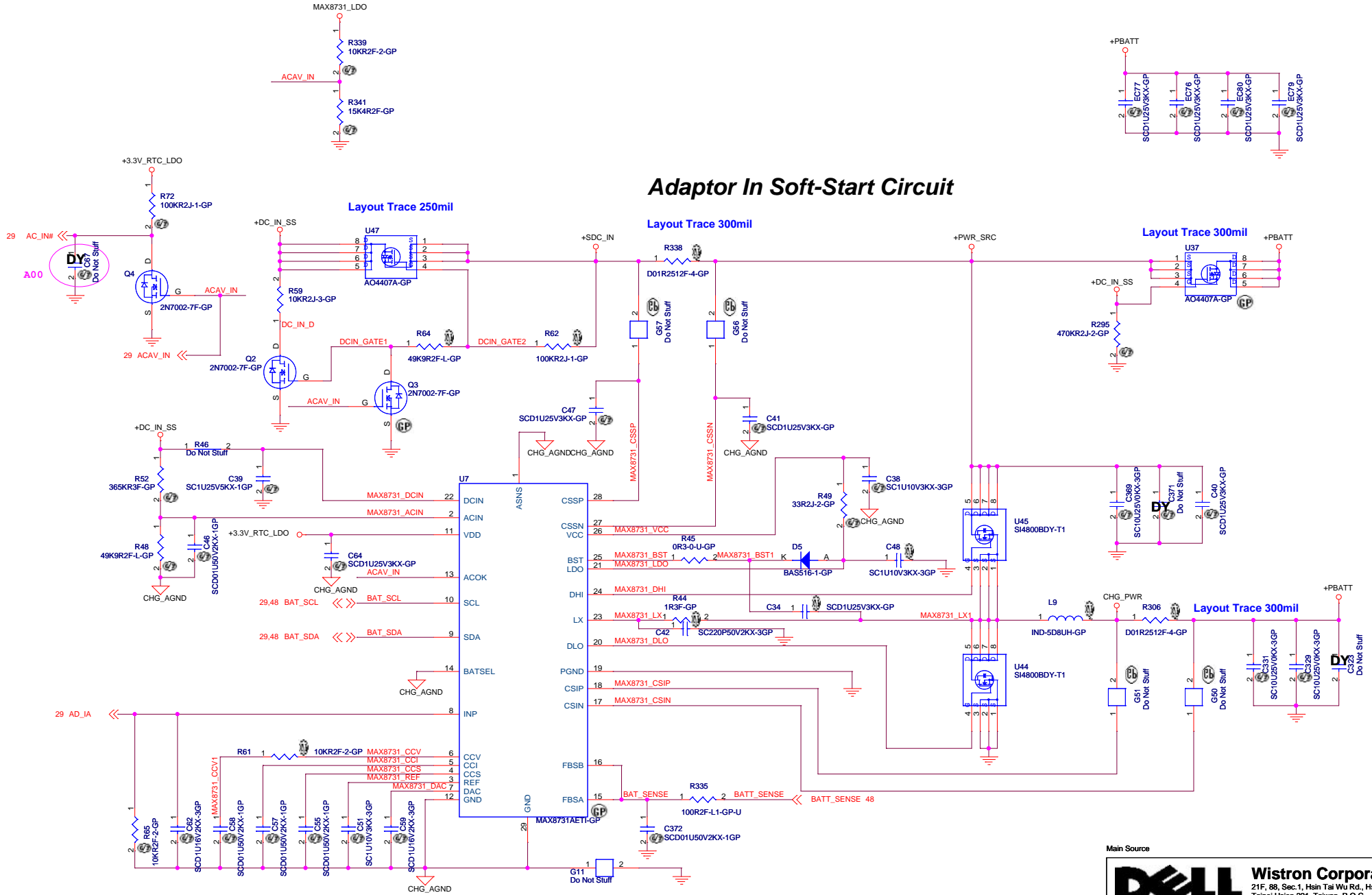
**Wistron Corporation**  
 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,  
 Taipei Hsien 221, Taiwan, R.O.C.

File: **DC to DC 1.8V/0.9V**

Size	Document Number	Rev
Custom		-1

Date: Tuesday, May 19, 2009 Sheet 44 of 60

**SSID = Charger**



**Adaptor In Soft-Start Circuit**

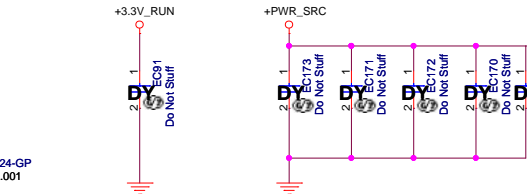
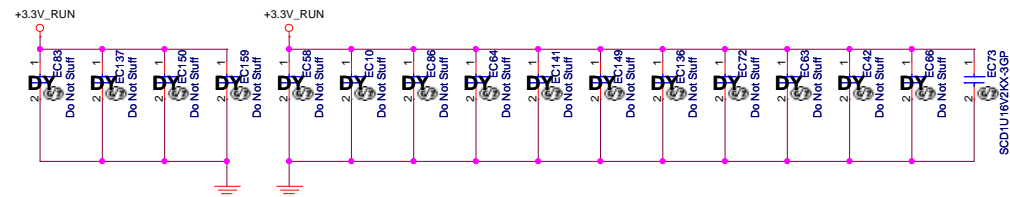
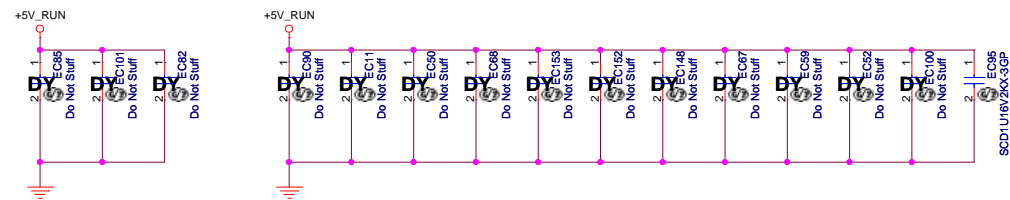
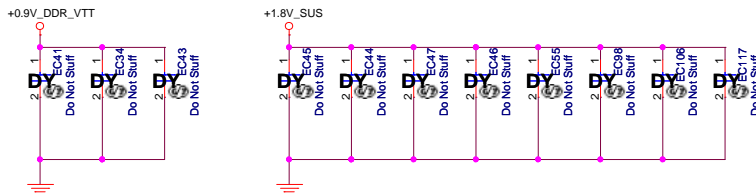
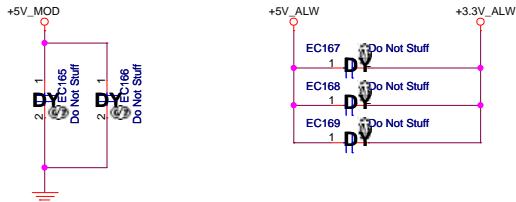
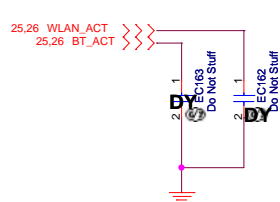
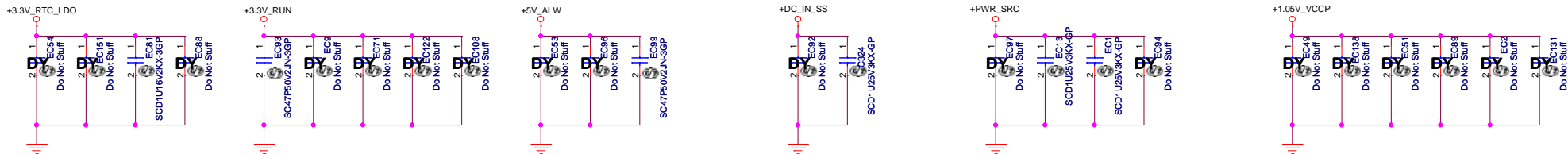
Main Source

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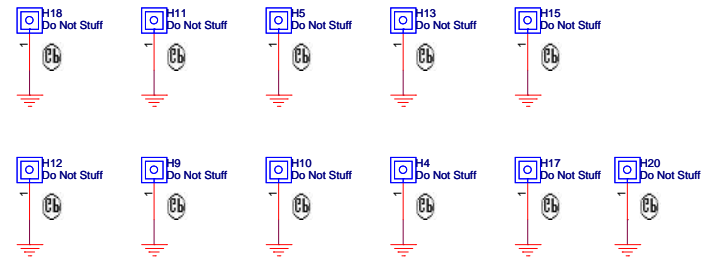
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Size	Document Number	Rev
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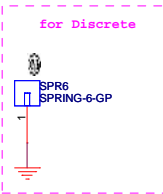
Date: Tuesday, May 19, 2009 Sheet 45 of 60



For EMI



34.4W005.301 Mini Card BOSS  
 34.4W004.501 New Card BOSS  
 34.4W001.201 NB Thermal BOSS



SW1 SPRING-24-GP 34.45T31.001

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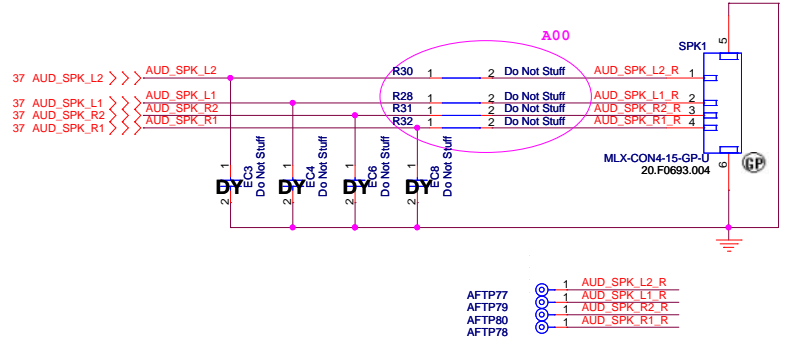
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Size	Document Number	Rev
Custom	<b>Roberts Discrete</b>	-1

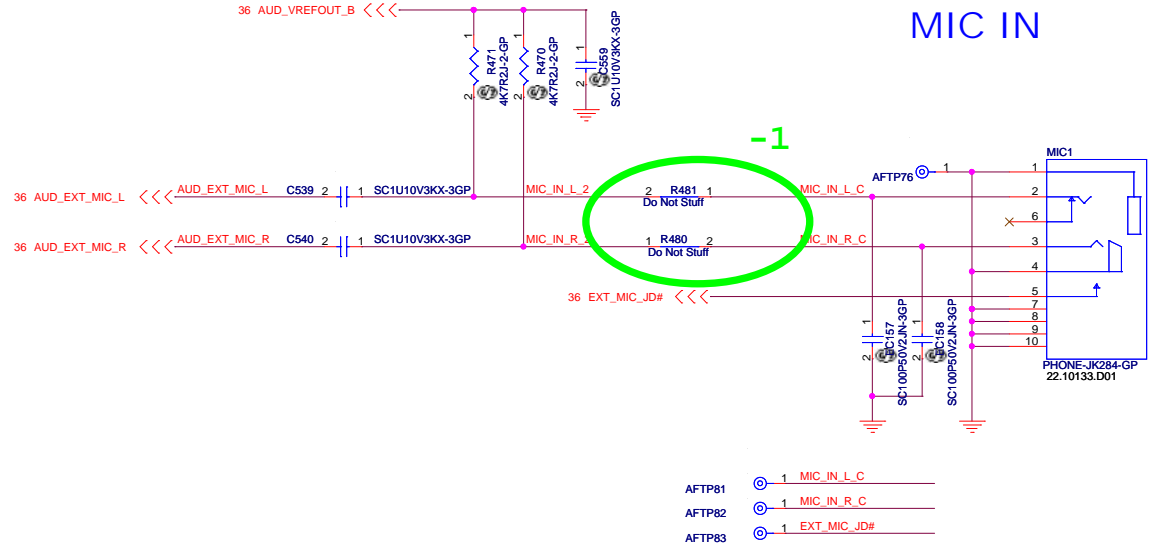
Date: Tuesday, May 19, 2009 Sheet 46 of 60

**SSID = AUDIO**

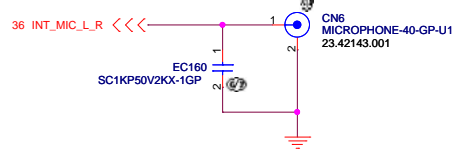
### Speaker Connector



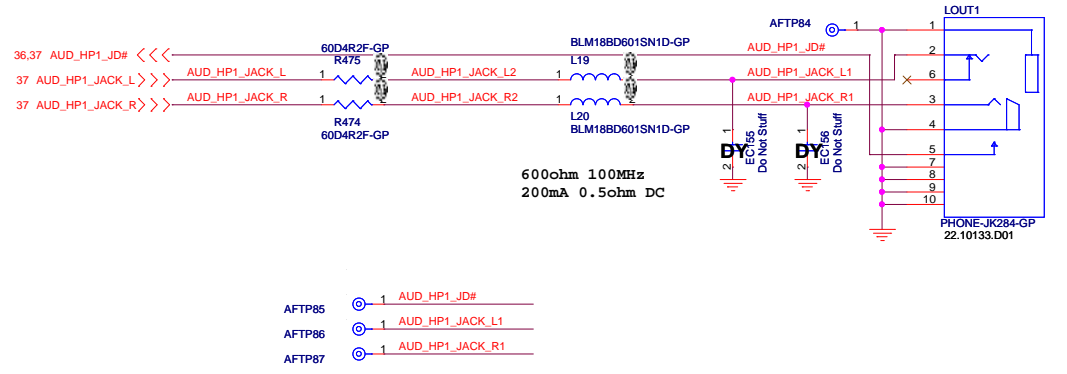
### MIC IN



### Internal Microphone



### LINE1 OUT



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File

**Audio Jack**

Size Document Number  
 Custom

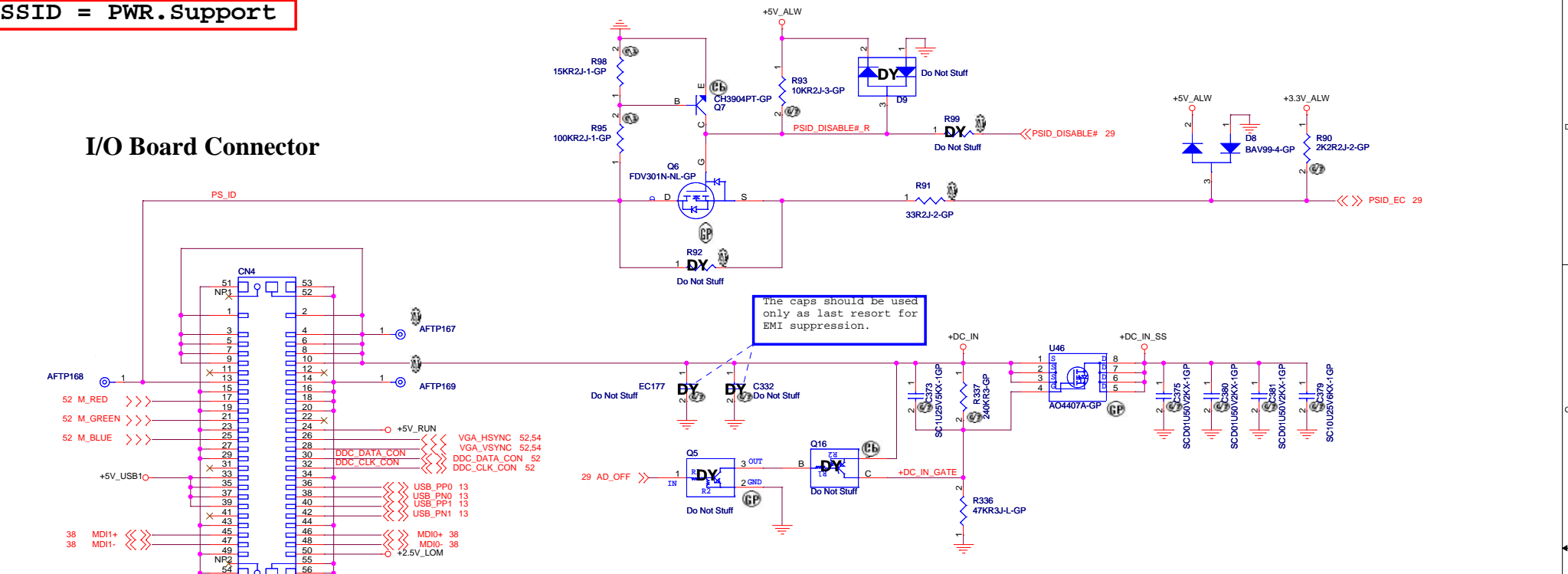
Date: Tuesday, May 19, 2009 Sheet 47 of 60

Rev  
 -1

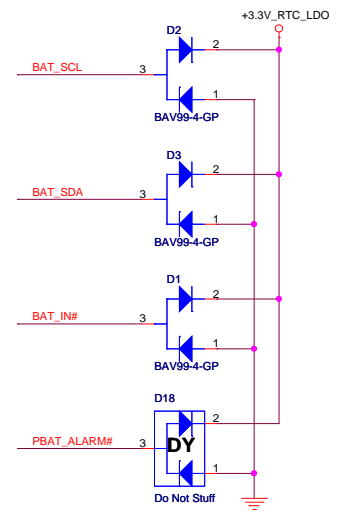
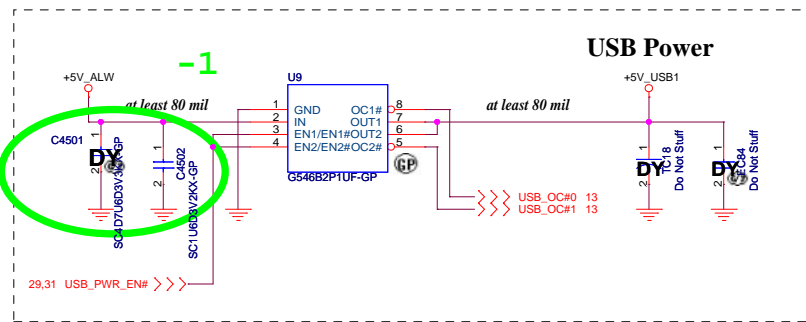
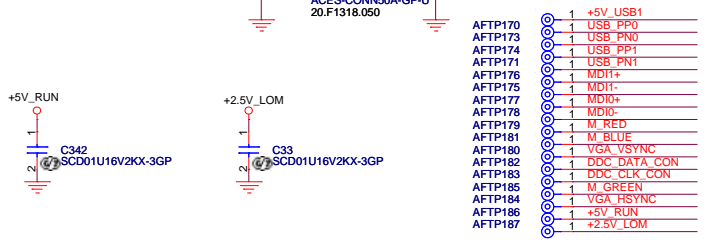
Roberts Discrete

**SSID = PWR.Support**

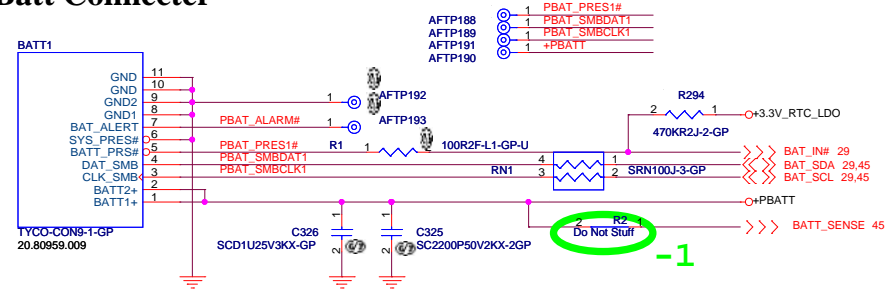
### I/O Board Connector



The caps should be used only as last resort for EMI suppression.



### Batt Connector



**Reserved for EMI**  
Place near DCIN1  
+DC\_IN

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File: **LEFT IO/BATT CONN**

Size: Custom Document Number

Date: Tuesday, May 19, 2009 Sheet 48 of 60

Rev: **-1**

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Title

**USB Port**

Size

Custom

Date:

Tuesday, May 19, 2009

Sheet

49

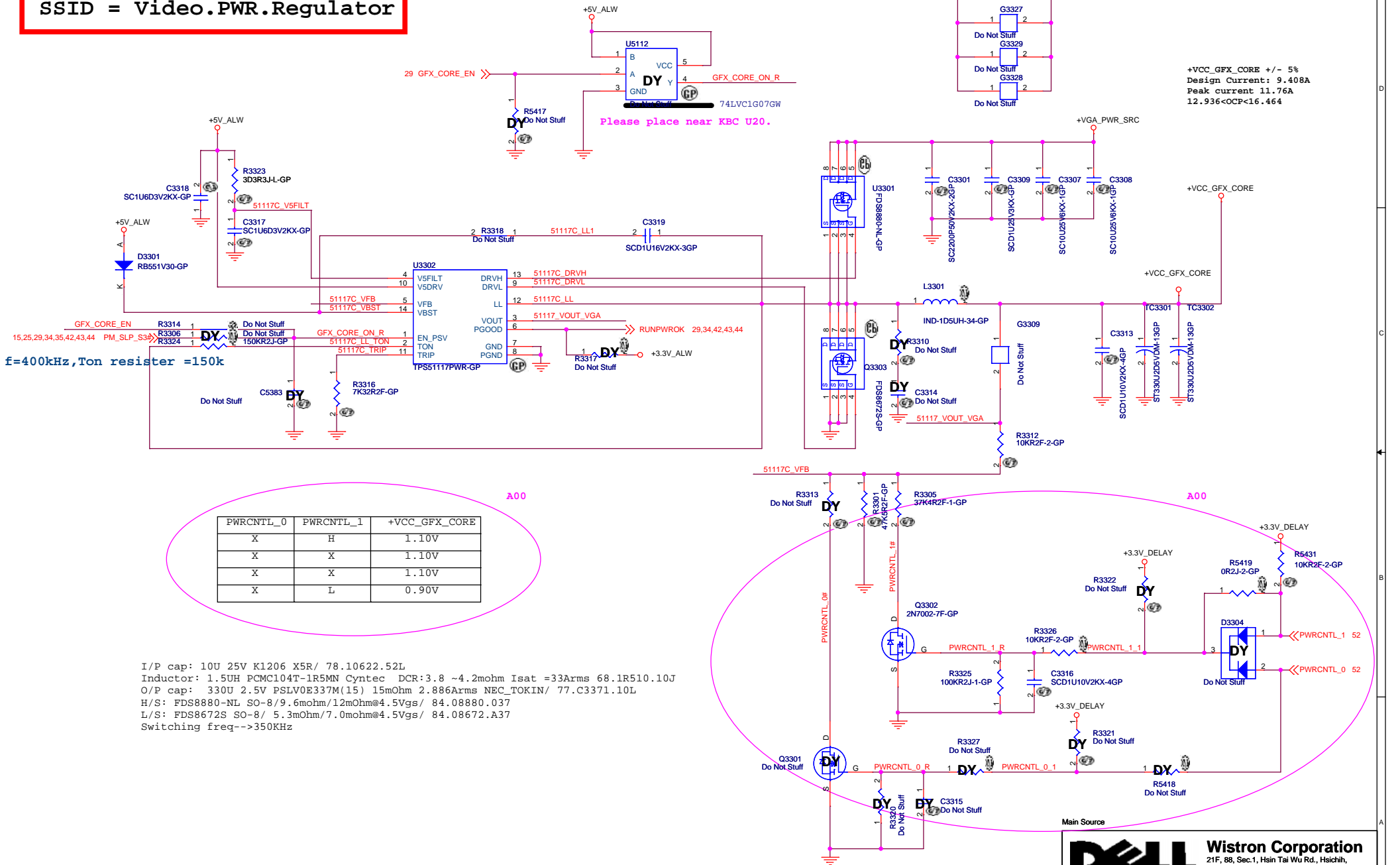
of

60

Rev

-1

# SSID = Video.PWR.Regulator



+VCC\_GFX\_CORE +/- 5%  
 Design Current: 9.408A  
 Peak current 11.76A  
 12.936<OCP<16.464

f=400kHz, Ton resistor =150k

A00

PWRCNTL_0	PWRCNTL_1	+VCC_GFX_CORE
X	H	1.10V
X	X	1.10V
X	X	1.10V
X	L	0.90V

I/P cap: 10U 25V K1206 X5R/ 78.10622.52L  
 Inductor: 1.5UH PCMC104T-1R5MN Cyntec DCR:3.8 ~4.2mohm Isat =33Arms 68.1R510.10J  
 O/P cap: 330U 2.5V PSLV0E337M(15) 15mOhm 2.886Arms NEC\_TOKIN/ 77.C3371.10L  
 H/S: FDS8880-NL SO-8/9.6mohm/12mOhm@4.5Vgs/ 84.08880.037  
 L/S: FDS8672S SO-8/ 5.3mOhm/7.0mohm@4.5Vgs/ 84.08672.A37  
 Switching freq-->350KHz

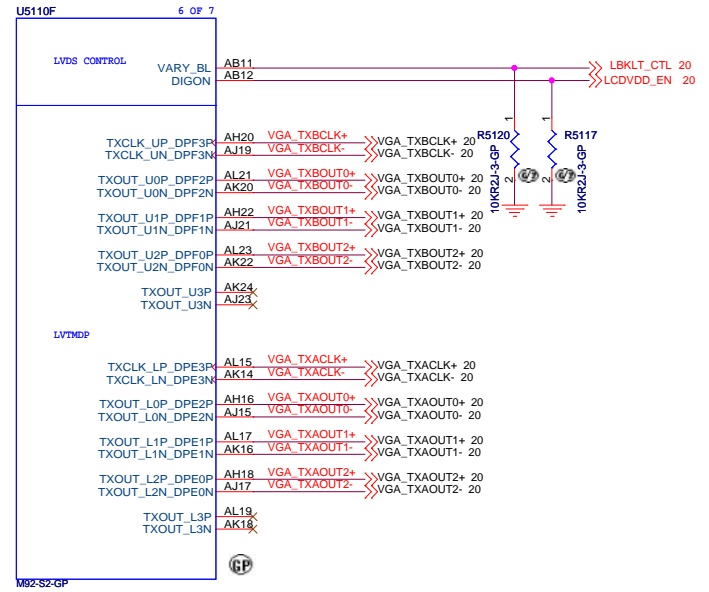
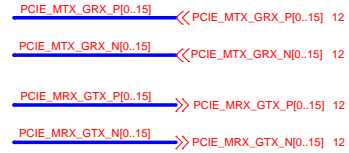
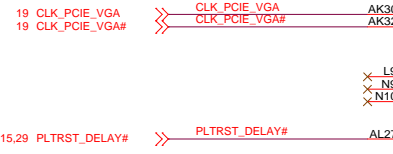
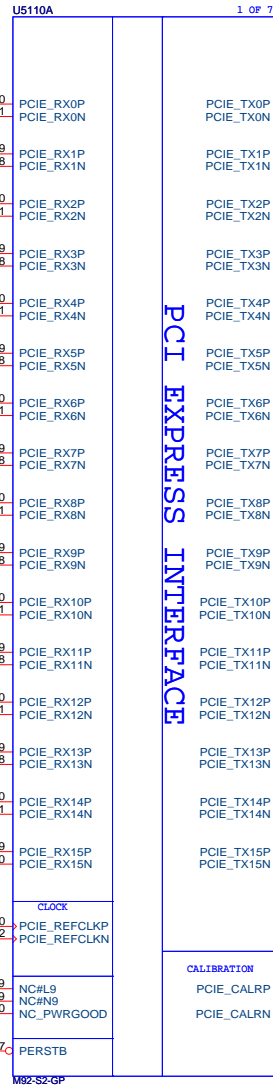
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**VGA\_CORE**

Title	<b>VGA_CORE</b>	
Size	Document Number	Rev
A3	<b>Roberts Discrete</b>	-1
Date:	Tuesday, May 19, 2009	Sheet 50 of 60

**SSID = VIDEO**

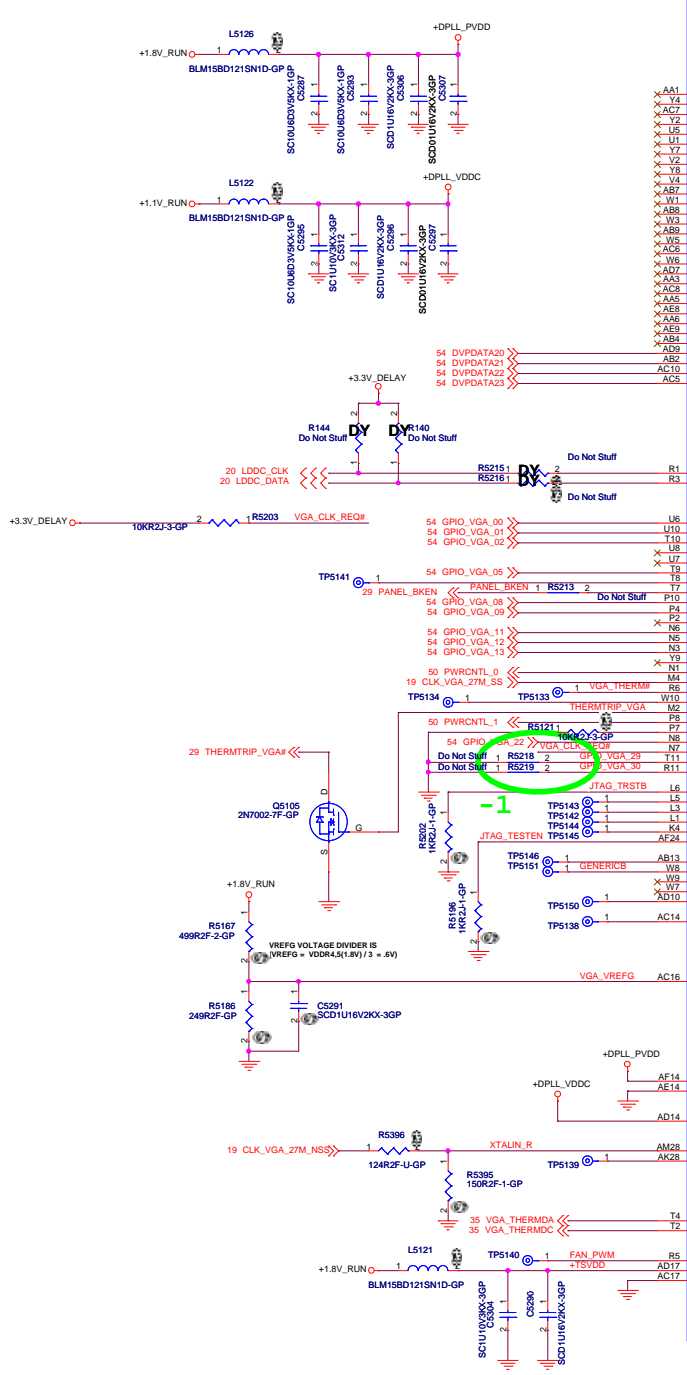


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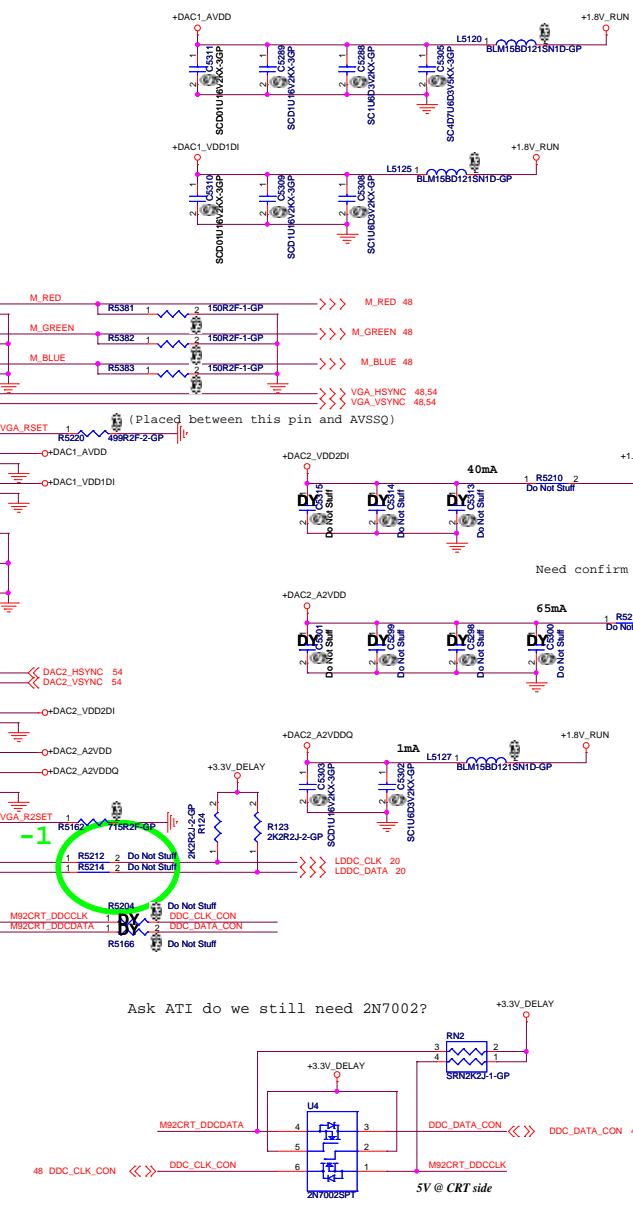
File: **VGA-PCIE/LVDS(1/4)**

Size	Document Number	Rev
Custom	<b>Roberts Discrete</b>	-1
Date:	Tuesday, May 19, 2009	Sheet 51 of 60



U5110B 2 OF 7

Block	Pin	Signal Name	Notes	
DPA	AF2	TXCAP_DPA3P		
	AF4	TXCAM_DPA3N		
	AG3	TXOP_DPA2P		
	AG5	TXOM_DPA2N		
	AH3	TX1P_DPA1P		
	AH1	TX1M_DPA1N		
	AK3	TX2P_DPA0P		
	AK1	TX2M_DPA0N		
	AM3	TXCBP_DPB3P		
	AM5	TXCBM_DPB3N		
	AK6	TX3P_DPB0P		
	AM5	TX3M_DPB2N		
	AJ7	TX4P_DPB1P		
	AH6	TX4M_DPB1N		
	AK8	TX5P_DPB0P		
AL7	TX5M_DPB0N			
DPB	AA1	DVPCNTL_MVP_0		
	AA2	DVPCNTL_MVP_1		
	AA7	DVPCNTL_0		
	AA8	DVPCNTL_1		
	AA9	DVPCNTL_2		
	AA1	DVPCLK		
	AA7	DVPDATA_0		
	AA8	DVPDATA_1		
	AA9	DVPDATA_2		
	AA1	DVPDATA_3		
	AA2	DVPDATA_4		
	AA3	DVPDATA_5		
	AA4	DVPDATA_6		
	AA5	DVPDATA_7		
	AA6	DVPDATA_8		
	AA7	DVPDATA_9		
	AA8	DVPDATA_10		
	AA9	DVPDATA_11		
	AA1	DVPDATA_12		
	AA2	DVPDATA_13		
	AA3	DVPDATA_14		
	AA4	DVPDATA_15		
	AA5	DVPDATA_16		
	AA6	DVPDATA_17		
	AA7	DVPDATA_18		
AA8	DVPDATA_19			
AA9	DVPDATA_20			
AA1	DVPDATA_21			
AA2	DVPDATA_22			
AA3	DVPDATA_23			
IDC	R3	SCL		
	R3	SDA		
	R3	SDA		
DPC1	U6	GPIO_0		
	U10	GPIO_1		
	U10	GPIO_2		
	UB	GPIO_3_SMBDATA		
	UB	GPIO_4_SMBCLK		
	UB	GPIO_5_AC_BATT		
	UB	GPIO_6		
	P10	GPIO_7_BLON		
	P10	GPIO_8_ROMSO		
	P10	GPIO_9_ROMSI		
	P10	GPIO_10_ROMSCK		
	N6	GPIO_11		
	N3	GPIO_12		
	N3	GPIO_13		
	N1	GPIO_14_HPD2		
	N1	GPIO_15_PWRCNTL_0		
	M4	GPIO_16_S5IN		
	M4	GPIO_17_THERMAL_INT		
	M2	GPIO_18_HPD3		
	M2	GPIO_19_CTF		
	P7	GPIO_20_PWRCNTL_1		
	N6	GPIO_21_BB_EN		
	N7	GPIO_22_ROMCSB		
	N7	GPIO_23_CLKREQB		
	N1	GPIO_29_DRM_0		
	N1	GPIO_30_DRM_1		
	DPC2	AB13	GENERICA	
		VB	GENERICB	
		VB	GENERICC	
		W7	GENERICD	
AD10		GENERIC_EHPD4		
AC14		HPD1		
AD19		VDD2DI		
AC19		VSS2DI		
AE20		AZVDD		
AE17		A2VDD		
AE19		AZVSS		
AG13		R2SET		
AE6		DDC1CLK		
AE5		DDC1DATA		
AD4		AUX1P		
AD4	AUX1N			
AC11	DDC2CLK			
AG13	DDC2DATA			
AD19	AUX2P			
AD19	AUX2N			
AE16	DDCAUX5P			
AD16	DDCAUX5N			
AC1	DDC6CLK			
AC3	DDC6DATA			
AD20	DDCAUX7P			
AC2	DDCAUX7N			
THERMAL	T4	DPLUS		
	T2	DMINUS		
	RS	TS_FDO		
	AC17	TSVSS		
DDC/AUX	AE6	DDC1CLK		
	AE5	DDC1DATA		
	AD4	AUX1P		
AD4	AUX1N			
AC11	DDC2CLK			
AG13	DDC2DATA			
AD19	AUX2P			
AD19	AUX2N			
AE16	DDCAUX5P			
AD16	DDCAUX5N			
AC1	DDC6CLK			
AC3	DDC6DATA			
AD20	DDCAUX7P			
AC2	DDCAUX7N			



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File: **VGA-TV/CRT/DP PORT**

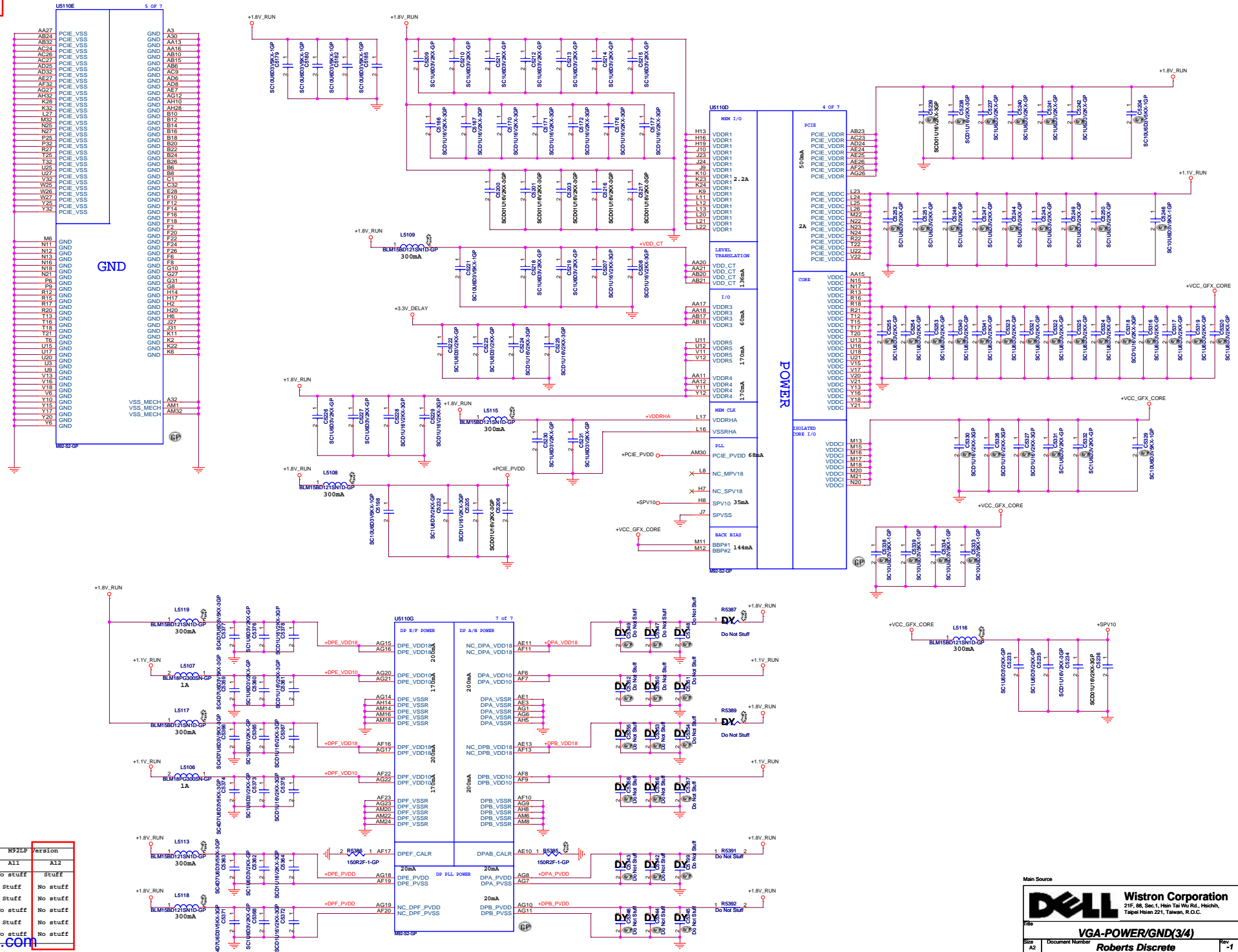
Sheet: **Roberts Discrete**

Page: **-1**

Date: Tuesday, May 18, 2009

Sheet 52 of 60

SSID = VIDEO



hexainf@hotmail.com  
GRATIS - FOR FREE

Part	All	Version
R5401	No stuff	stuff
Q5106	No stuff	stuff
R5402	stuff	No stuff
R5403	No stuff	stuff
Q5107	stuff	No stuff
C5384	No stuff	stuff

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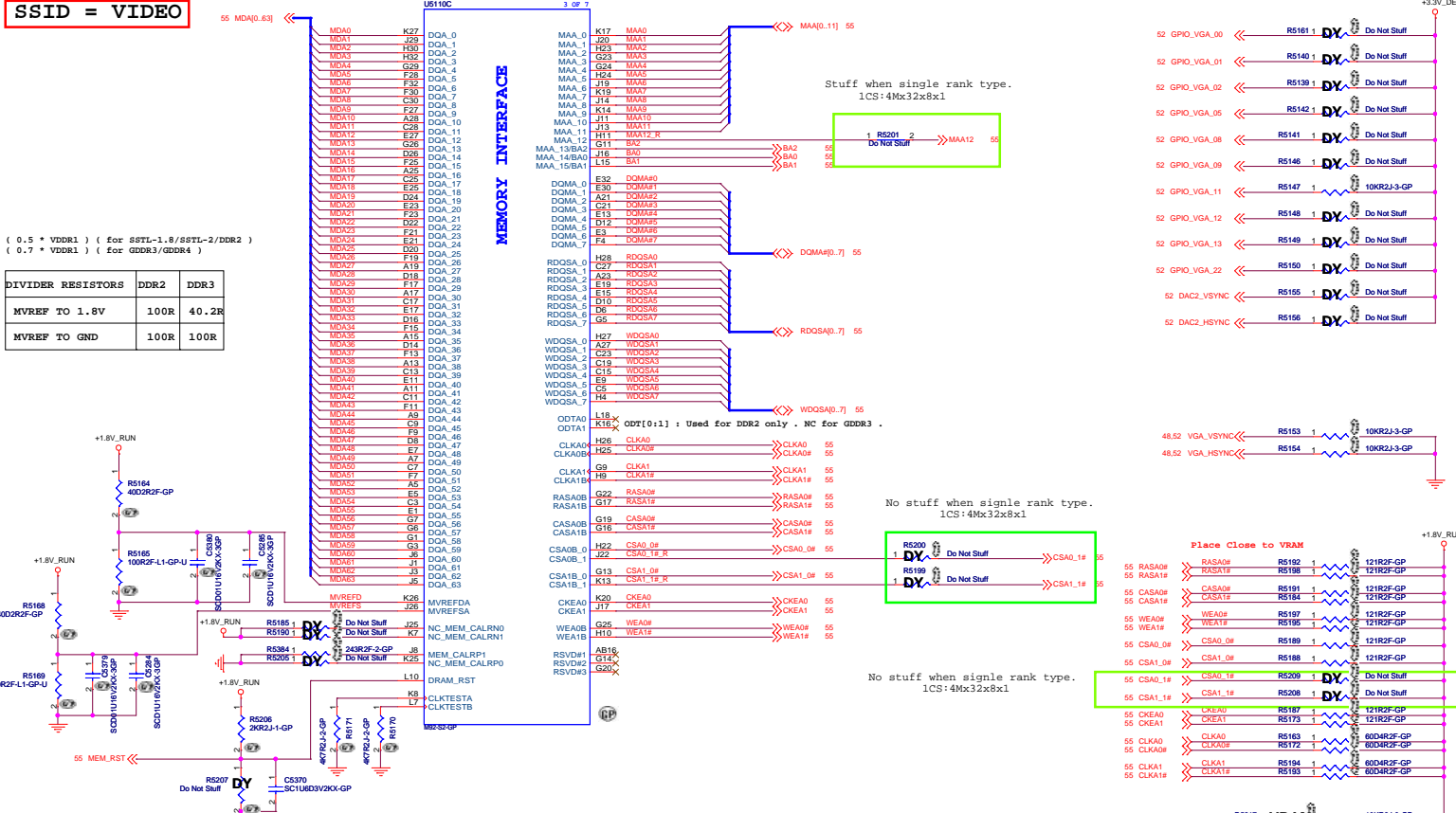
File: **VGA-POWER/GND(3/4)**

Rev: **1**

Author: **Roberts Discrete**

Date: 1/25/2007, May 15, 2009

**SSID = VIDEO**



( 0.5 \* VDDR1 ) ( For SSTL-1.8/SSTL-2/DDR2 )  
( 0.7 \* VDDR1 ) ( For GDDR3/GDDR4 )

DIVIDER RESISTORS	DDR2	DDR3
MVREF TO 1.8V	100R	40.2R
MVREF TO GND	100R	100R

Stuff when single rank type.  
1CS:4Mx32x8x1

No stuff when single rank type.  
1CS:4Mx32x8x1

No stuff when single rank type.  
1CS:4Mx32x8x1

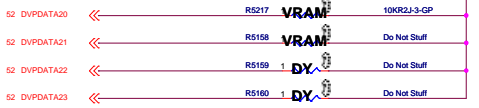
**ATI RESERVED CONFIGURATION STRAPS**  
ALLOW FOR PULLUP PADS FOR THESE STRAPS AND IF THESE GP10S ARE USED, THEY MUST NOT CONFLICT DURING RESE

GPIO3, H2SYNC, V2SYNC  
PULLUP PADS ARE NOT REQUIRED FOR THESE STRAPS BUT IF THESE GP10S ARE USED, THEY MUST NOT CONFLICT DURING RESE

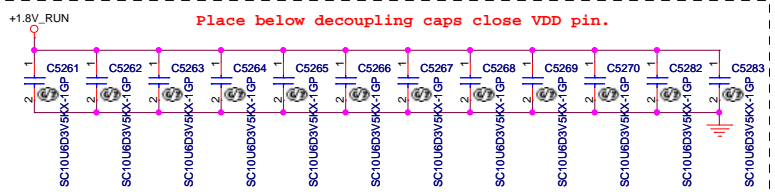
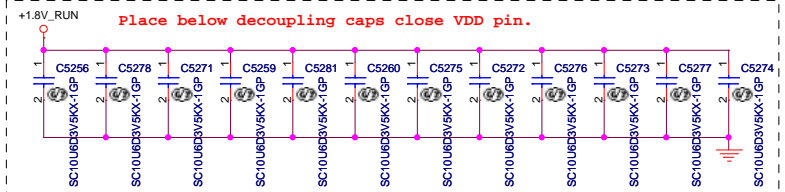
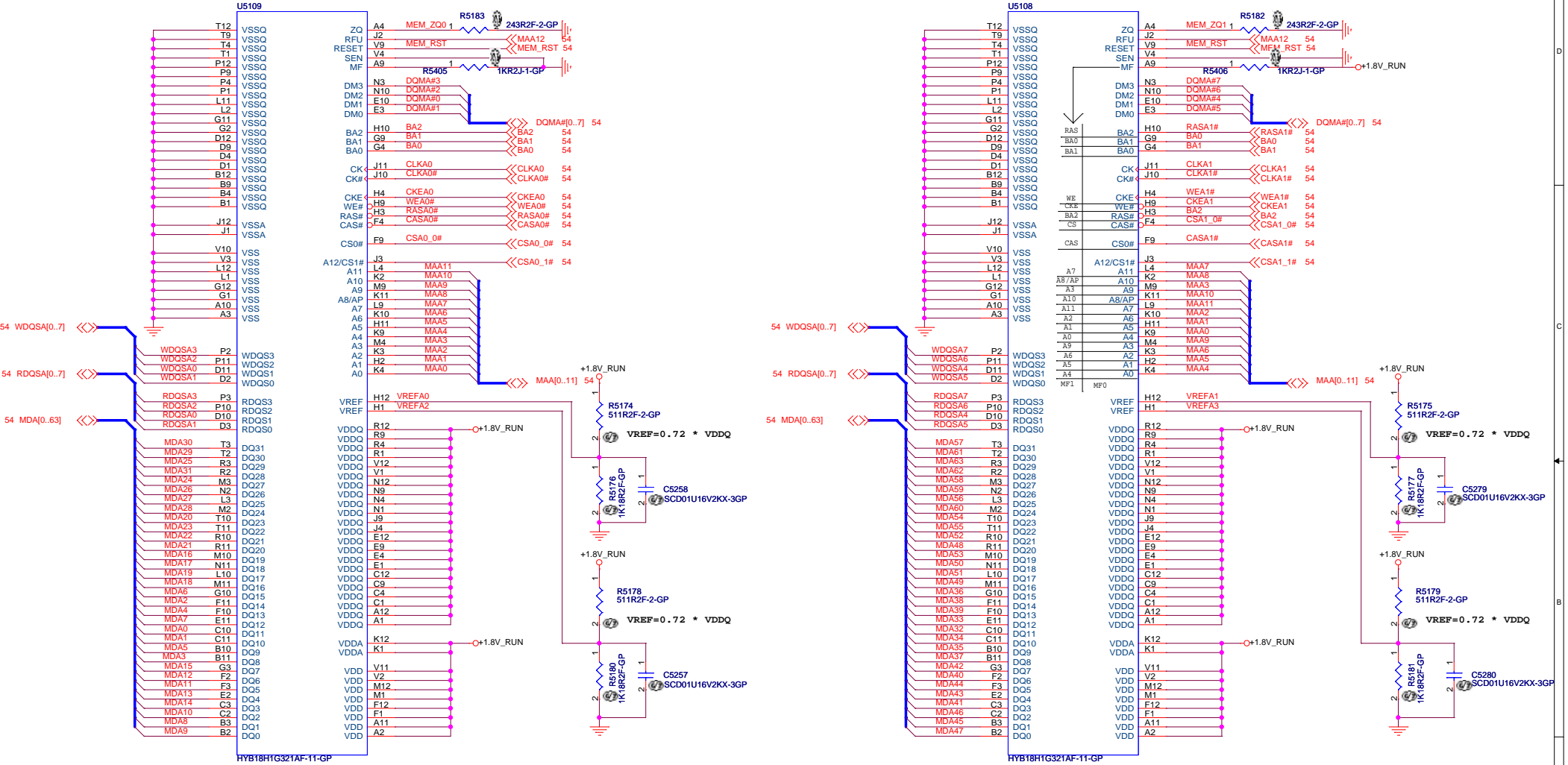
If BIOS_ROM_EN (GPIO22) = 0		If BIOS_ROM_EN (GPIO22) = 1		
Size of the primary memory apertures	GPIO[13,12,11]	Manufacturer	Part Number	GPIO[13,12,11]
128MB	x000	ST Microelectronics	M25P05A	0100
256MB	x001		M25P10A	0101
512MB	x010		M25P40	0101
1GB	x		M25P80	0101
2GB	x	Chingpio (formerly PMC)	Pm25LV012A	0100
4GB	x		Pm25LV010A	0101

STRAPS	PIN	DESCRIPTION
TX_PWRDS_ENB (Internal PD)	GPIO0	Transmitter Power Savings Enable V 0= 50% Tx output swing 1= Full Tx output swing
TX_DEEMPH_EN (Internal PD)	GPIO1	Transmitter De-emphasis Enable V 0= Tx de-emphasis disabled 1= Tx de-emphasis enabled
BIF_GEN2_EN_A	GPIO2	V 0 = Advertises the PCI-E device as 2.5GT/s 1 = Advertises the PCI-E device as 5.0GT/s
BIF_CLK_PM_EN	GPIO8	V 0= Disable CLKREQ#power management capability 1= Enable CLKREQ# power management capability
ROMIDCFG[3:0] (Internal PD)	GPIO[13,12,11]	if BIOS_ROM_EN=1, then Config[3:0] defines the ROM type if BIOS_ROM_EN=0, then Config[3:0] defines the primary memory aperture size
BIOS_ROM_EN (Internal PD)	GPIO_22_ROMCSB	Enable external BIOS ROM device V 0= Disable external BIOS ROM device 1= Enable external BIOS ROM device
AUD[1] (Internal PD)	VGA_HS_SYNC	AUD[1] 0:No audio function 1:Audio for DisplayPort and HDMI ( if adapter is detected)
AUD[0]	VGA_VS_SYNC	AUD[0] 10:Audio for DisplayPort only 11:Audio for both DisplayPort and HDMI

STRAPS	PIN	DESCRIPTION
MEM_TYPE	DVPPDATA(23:20) (Internal PD)	MEMORY TYPE, MAKE AND SIZE INFO 0000 - GDDR3 16Mx32 Qimonda 0001 - GDDR3 32Mx32 Qimonda 0010 - GDDR3 32Mx32 Hynix 0011 - GDDR3 32Mx32 Samsung



**SSID = VIDEO**

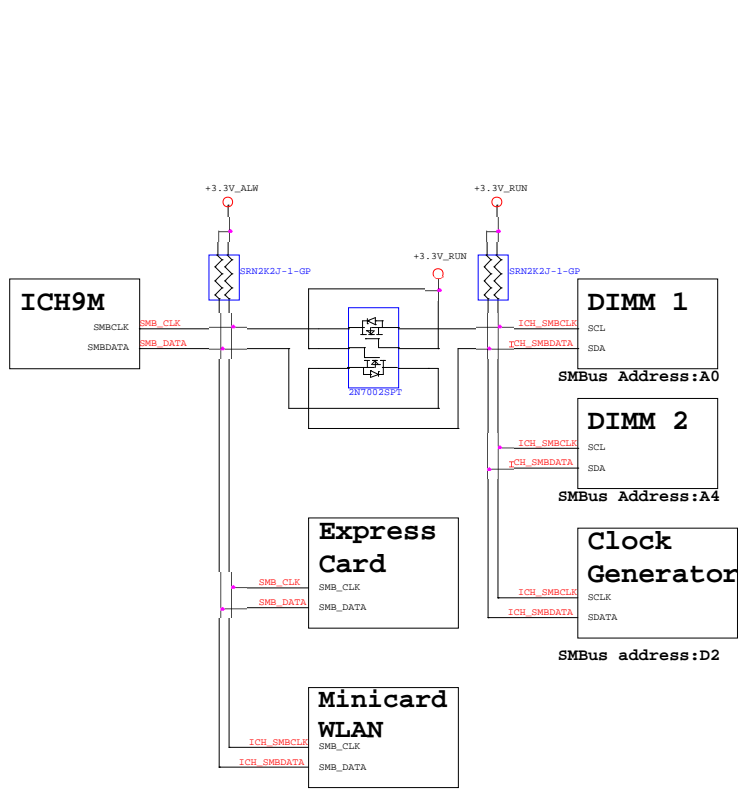


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**DELL** Wistron Corporation  
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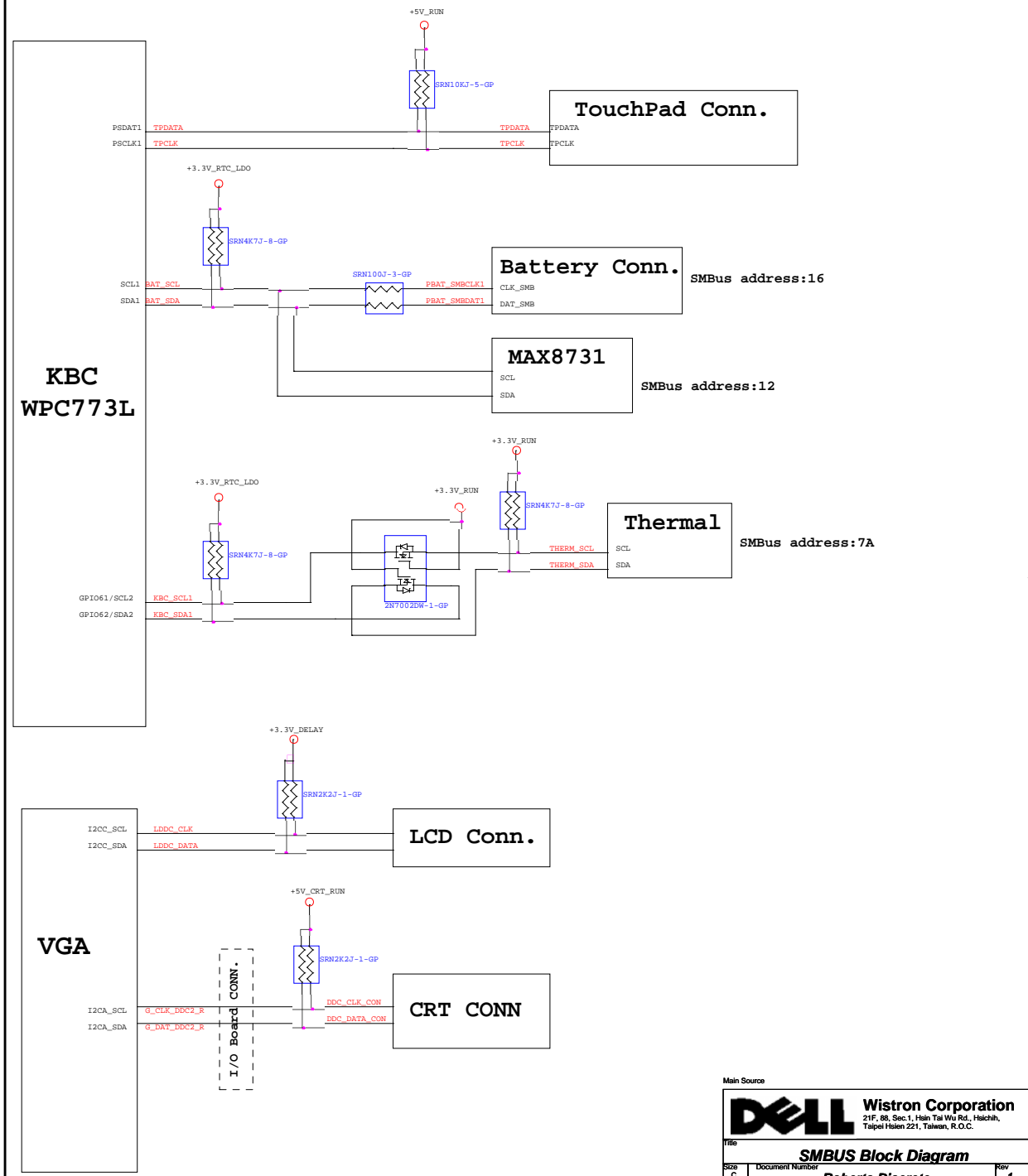
File  
**VRAM**

Size	Document Number	Rev
Custom	<b>Roberts Discrete</b>	-1
Date:	Tuesday, May 19, 2009	Sheet 55 of 60

# ICH9M SMBus Block Diagram

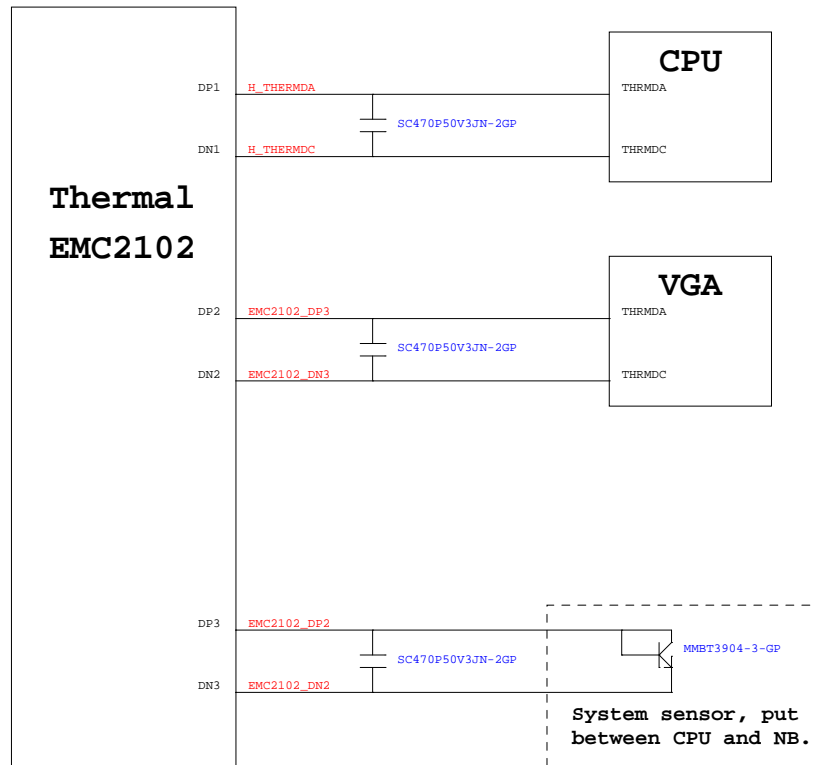


# KBC SMBus Block Diagram

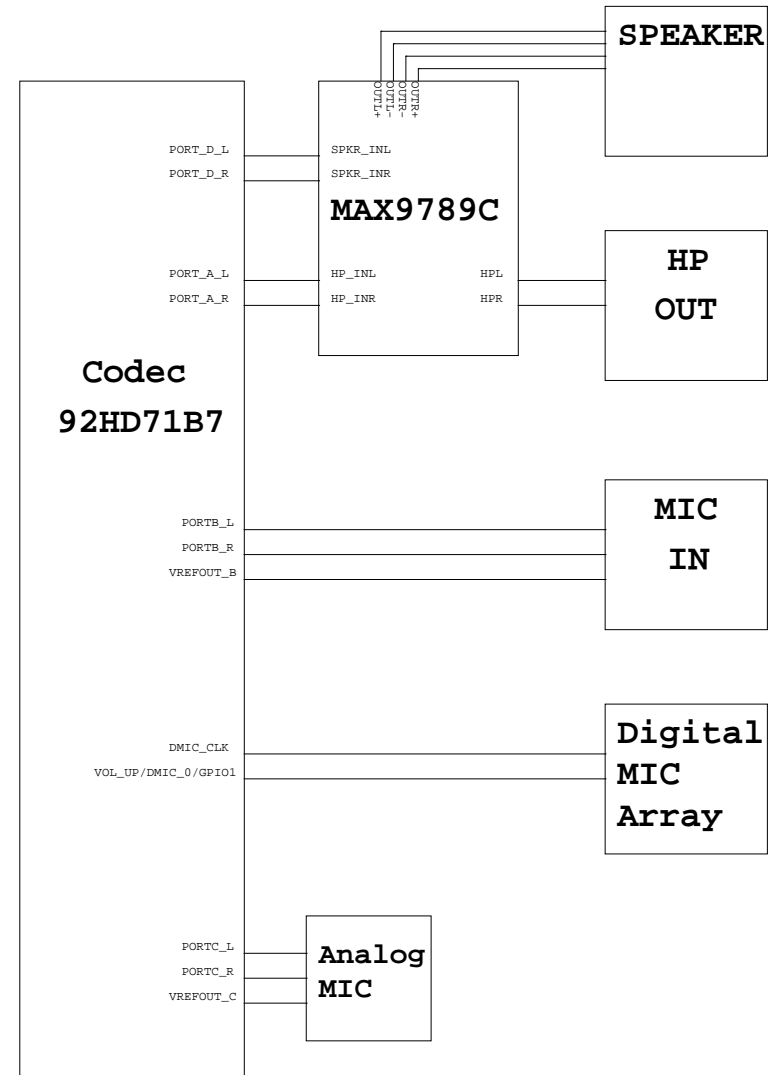




# Thermal Block Diagram

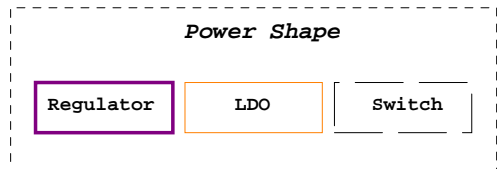
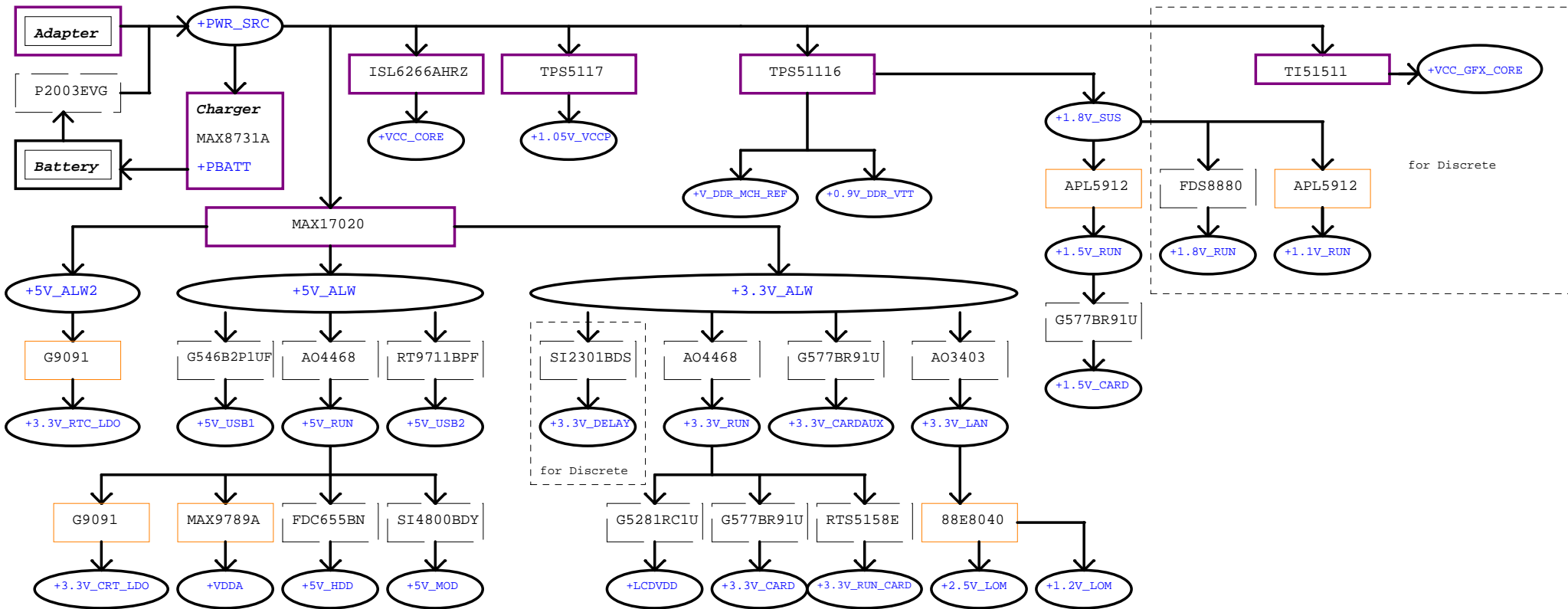


# Audio Block Diagram



Main Source

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File			
<b>Thermal/Audio Block Diagram</b>			
Size	Document Number	Rev	
Custom		-1	
Date: Tuesday, May 19, 2009		Sheet 57	of 60



DATE	VERSION	NO	PAGE	Modified List	Issue Description	OWNER
01/09	A00	1	29	Stuff R151, no stuff R150.	Change board ID from X02 to A00.	EE
		2	20	Add R5425.	Add resistor 100k ohm pull low to ground. To solve panel blinking issue.	EE
01/12		3	16	Delete R432, R433.	Delete zero ohm resistors for cost concern.	EE
		4	8,10, 11,16 19,29, 39,41, 43,44, 47	Replace R139, R125, R412, R384, R153, R329, R330, R127, R137, PR1, R351, R453, R5400, R365, R28, R30, R31, R32, RN42, RN43, RN44, RN45, RN48, RN22, RN23, RN54, RN53, RN51 with pads.	Replace zero ohm resistors with pad for cost concern.	EE
		5	44	Change PR9 from pad into 10k ohm resistor. Change C89 from dummy into 0.1u capacitor.	Adding RC circuit.	EE
		6	50	Dummy R3313, Q3301, R3320, C3315, R3327, R3321, R5418, R5419. Add R5431 and D3304. R3305 change to 37.4K ohm.	Changing Power Play voltage control.	EE
01/21		7	34,35	Use 84.27002.L04 for Q13 and Q23.	To prevent components being damaged by high voltages.	EE
01/22		8	41	Change R5413 into zero ohm resistor.		EE
02/02		9	50	Dummy D3304. Undummy R5419.		EE
02/04		11	45	Dummy C67.		EE
		12	29	Add circuit D3305, U5113, R5432, C5390, Q5113, but dummy all. Change R158 to zero ohm resistor.		EE
05/19		1	14 25 17 18 29 30 34 41 44 47 48 52	Change R167 R435 R158 R413 R501 R5412 R5413 PR17 R5212 R5214 R397 R399 R2 R481 R480 R54 R55 R56 R57 to short pad.		EE
	2	52	change circuit R5218 R5219 to short pad		EE	
	3	26	change G3330 G3331 gap type		EE	
	4	48	add circuit C4501 C4502		EE	
	5	31	Change EC78 0.1u to 1u, Change TC12 to 4.7u but DUMMY		EE	

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Title			
<b>Change List-EE</b>			
Size	Document Number	Rev	
Custom	<b>Roberts Discrete</b>	-1	
Date:	Tuesday, May 19, 2009	Sheet	59 of 60

DATE	VERSION	NO	PAGE	Modified List	Issue Description	OWNER

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Title			
<b>Change List Power</b>			
Size	Document Number		Rev
Custom	<b>Roberts Discrete</b>		<b>-1</b>
Date: Tuesday, May 19, 2009		Sheet 60 of	60