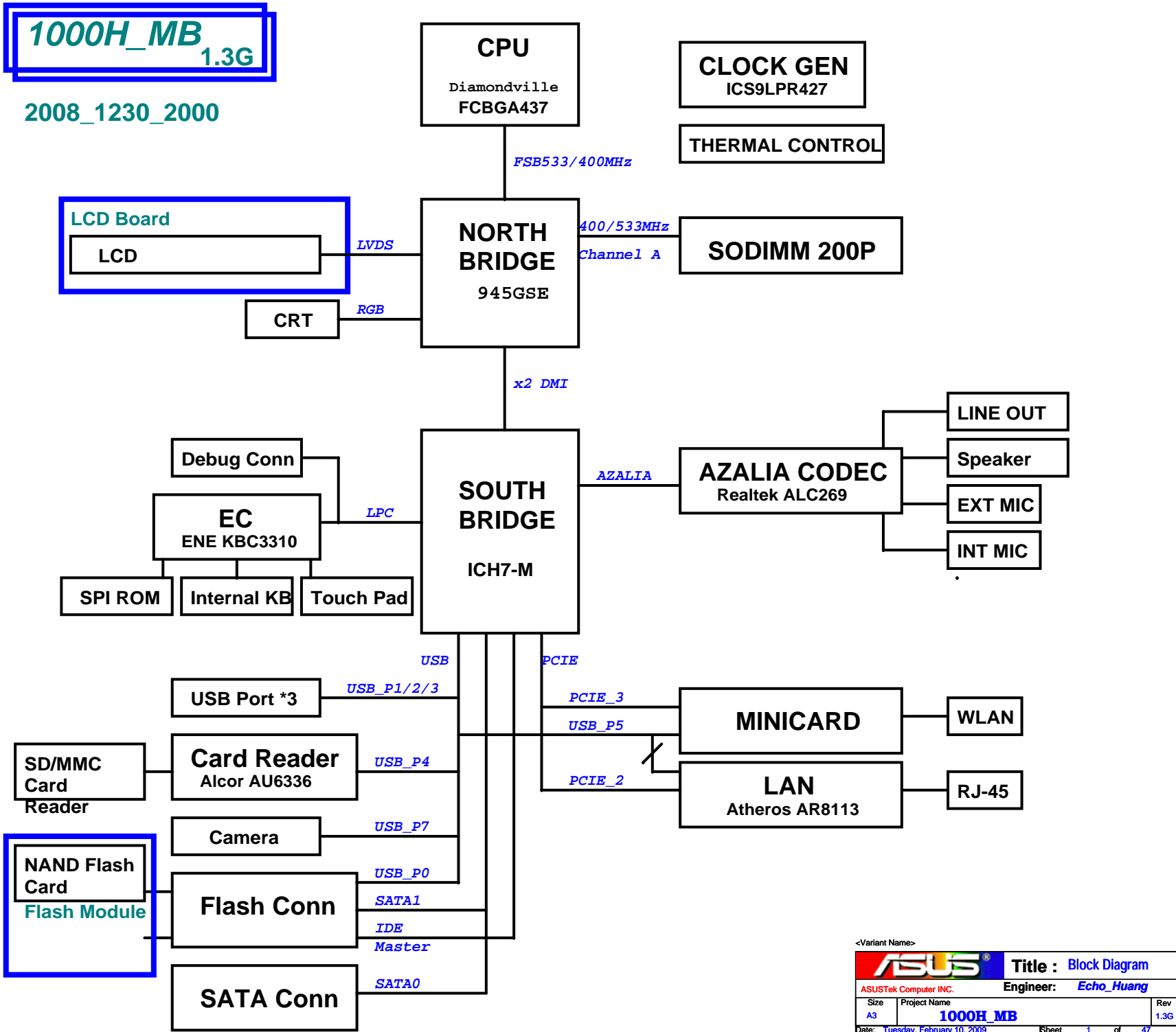



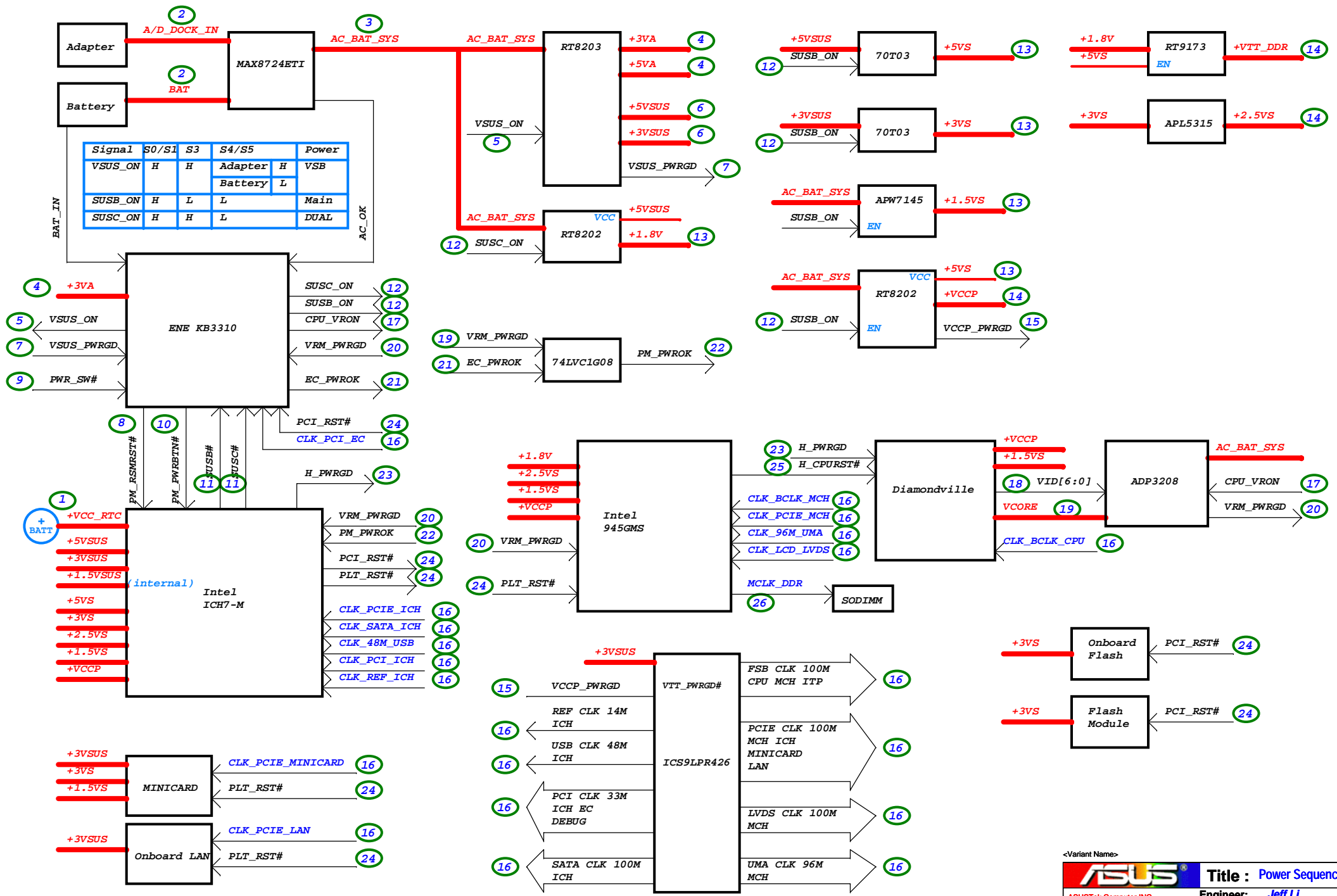
- 01\_Block Diagram
- 02\_System Setting
- 03\_Power Sequence
- 04\_Clock Gen\_IC9S9LPR426
- 05\_Diamondville\_BUS
- 06\_Diamondville\_PWR
- 07\_NB-945GMS(HOST)
- 08\_NB-945GMS(DMI)
- 09\_NB-945GMS(GRAPHIC)
- 10\_NB-945GMS(DDR2)
- 11\_NB-945GMS(PWR)
- 12\_NB-945GMS(PWR2)
- 13\_NB-945GMS(GND)
- 14\_SB-ICH7M(PWR)
- 15\_SB-ICH7M(1)
- 16\_SB-ICH7M(2)
- 17\_SB-ICH7M(3)
- 18\_DDR2 SODIMM
- 19\_DDR2 Termination
- 20\_Onboard VGA
- 21\_LCD Conn\_LID
- 22\_PCIEx 3.5G & Ext. Antenna
- 23\_Mini WiFi+ BT
- 24\_LAN\_Atheros AR8113
- 25\_MDC\_RJ11\_RJ45
- 26\_Flash Conn
- 27\_SATA Hdd
- 28\_USB Port
- 29\_Camera Conn
- 30\_Card Reader\_AU6336C52
- 31\_Codec\_ALC269
- 32\_Audio\_AMP\_Jack
- 33\_EC\_ENE KB3310
- 34\_EC\_UART controller
- 35\_Switch\_SPI ROM\_Debug Conn
- 36\_Thermal Sensor\_FAN
- 37\_KB\_Touch Pad
- 38\_LED\_THERMTRIP
- 39\_Discharge
- 40\_PWR Jack
- 41\_Srew Hole
- 42\_EMI
- 43\_POWER FLOW
- 44\_Vcore
- 45\_Power System
- 46\_Power\_+1.8V & VTTDDR
- 47\_Power\_VCCP
- 48\_Power\_+1.5VS & +2.5VS
- 49\_Power\_Charger
- 50\_EC Pin Define
- 51\_History





<Variant Name>

		<b>Title :</b> History
ASUSTek Computer INC.		<b>Engineer:</b> KingCa_Jin
Size	Project Name	Rev
A3	<b>1000H_MB</b>	1.0G
Date: Tuesday, February 10, 2009		Sheet 2 of 47



## EC KB3310 GPIO SETTING

Pin	Pin Name	Signal Name	Type	Note
1	GPIO00/GA20	A20GATE	O	
2	GPIO01/KBRST#	RC_IN#	O	
6	GPIO04	EMAIL_SW#	I	Internal pull high
13	GPIO05/PCIRST#	PCI_RST#	I	
14	GPIO07	BAT_OTP	I	Battery over temperature
15	GPIO08	EXTSM#	OD	10K pull high to +3VSB
16	GPIO0A	LID_EC#	I	Internal pull high
17	GPIO0B/ESB_CLK	NC	O	
18	GPIO0C/ESB_DAT	NC	O	
19	GPIO0D	DISTP_SW#	I	Internal pull high
20	GPIO0E/SC#	EXT_SC#	O	10K pull high to +3VSB
21	GPIO0F/PWM0	BL_PWM_DA	O	
23	GPIO10/PWM1	BAT_CRITICAL	I	Battery critical capacity
25	GPIO11/PWM2	PM_PWRBTN#	OD	Internal pull high in ICH
26	GPIO12/FANPWM1	FAN0_PWM	O	CPU Fan
27	GPIO13/FANPWM2	FAN1_PWM	O	VGA Fan
28	GPIO14/FANFB1	FAN0_TACH	I	CPU FanTach
29	GPIO15/FANFB2	FAN1_TACH	I	VGA FanTach
30	GPIO16/E51_TX	E51_TX	O	RS232 debug port
31	GPIO17/E51_RX	E51_RX	I	RS232 debug port
32	GPIO18	PWR_SW#	I	Internal pull high
34	GPIO19/PWM3	MAIL_LED#	O	
36	GPIO1A/NUMLED	NUM_LED#	O	
38	GPIO1D/CLKRUN#	NC	O	
39	GPIO20/KSO0/TP_TEST	KSO0	O	
40	GPIO21/KSO1/TP_PLL	KSO1	O	
41	GPIO22/KSO2	KSO2	O	
42	GPIO23/KSO3	KSO3	O	
43	GPIO24/KSO4	KSO4	O	
44	GPIO25/KSO5	KSO5	O	
45	GPIO26/KSO6	KSO6	O	
46	GPIO27/KSO7	KSO7	O	
47	GPIO28/KSO8	KSO8	O	
48	GPIO29/KSO9	KSO9	O	
49	GPIO2A/KSO10	KSO10	O	
50	GPIO2B/KSO11	KSO11	O	
51	GPIO2C/KSO12	KSO12	O	
52	GPIO2D/KSO13	KSO13	O	
53	GPIO2E/KSO14	KSO14	O	
54	GPIO2F/KSO15	KSO15	O	
55	GPIO30/KSI0	KSI0	I	Internal pull high
56	GPIO31/KSI1	KSI1	I	Internal pull high
57	GPIO32/KSI2	KSI2	I	Internal pull high
58	GPIO33/KSI3	KSI3	I	Internal pull high
59	GPIO34/KSI4	KSI4	I	Internal pull high
60	GPIO35/KSI5	KSI5	I	Internal pull high
61	GPIO36/KSI6	KSI6	I	Internal pull high
62	GPIO37/KSI7	KSI7	I	Internal pull high
63	GPI38/AD0	BAT_IJCHG	I	
64	GPI39/AD1	BAT_CONFIG	I	Battery configuration
65	GPIO3A/AD2	BAT_SENSE	I	Battery Voltage Sensor
66	GPIO3B/AD3	BAT_TS	I	Battery Thermal Sensor
68	GPO3C/DA0	DOC	O	Trigger Clock Gen

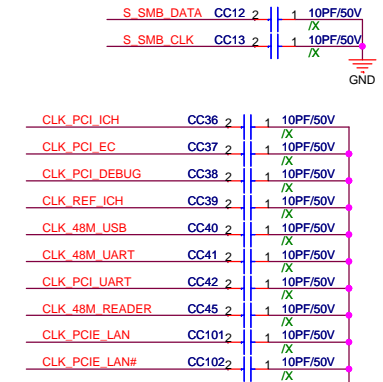
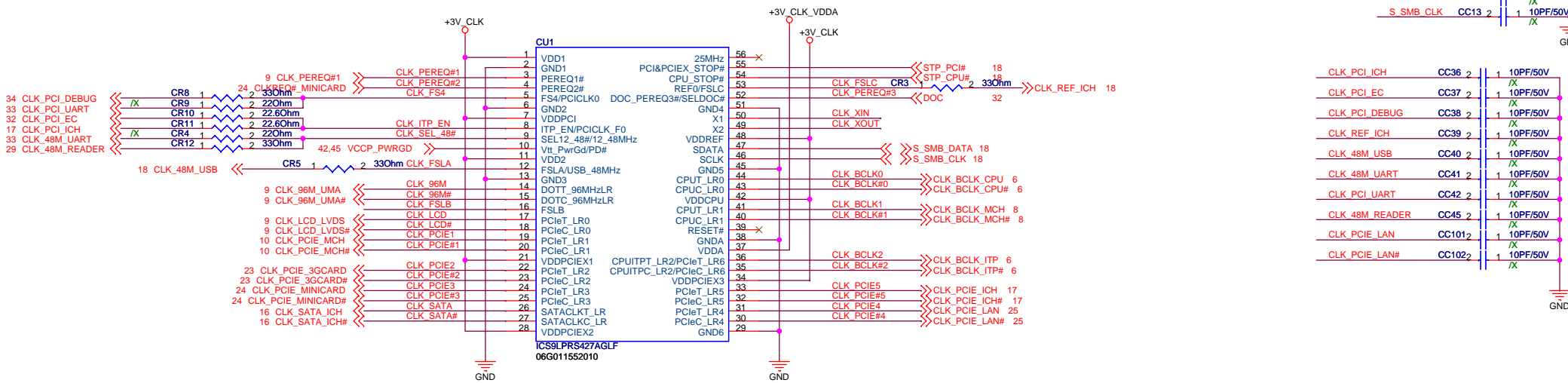
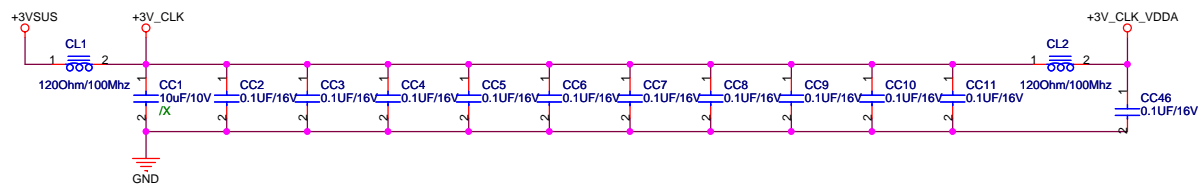
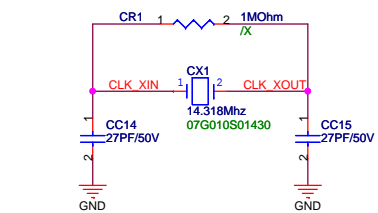
## EC KB3310 Other Pin SETTING

Pin	Pin Name	Signal Name	Type	Note
3	SERIRQ	INT_SERIRQ	I/OD	10K pull high to +3V
4	LFRAME#	LPC_FRAME#	I	
5	LAD3	LPC_AD3	I/O	
7	LAD2	LPC_AD2	I/O	
8	LAD1	LPC_AD1	I/O	
9	VCC	+3VA_EC	P	
10	LAD0	LPC_AD0	I/O	
11	GND	GND	P	
12	PCICLK	CLK_PCI_EC	I	
22	VCC	+3VA_EC	P	
24	GND	GND	P	
33	VCC	+3VA_EC	P	
35	GND	GND	P	
37	ECRST#	EC_RST#	I	100K pull high to +3VA_EC
67	AVCC	+3VACC	P	
69	AGND	AGND	P	
94	GND	GND	P	
96	VCC	+3VA_EC	P	
111	VCC	+3VA_EC	P	
113	GND	GND	P	
119	RD#/SPIDI	SPI_SO	I	
120	WR#/SPIDO	SPI_SI	O	
112	XCLKI	32KXCLKI	I	
123	XCLKO	32KXCLKO	O	
124	V18R	V18R	P	Reserved 1uF to GND
125	VCC	+3VA_EC	P	
128	SPICS#/SELMEM#	SPI_CE#	O	

Pin	Pin Name	Signal Name	Type	Note
70	GPO3D/DA1	LCD_BACKOFF#	O	
71	GPO3E/DA2	CLK_PWRSERVE#	O	
72	GPO3F/DA3	BAT_LL#	O	Battery Low Low
73	GPIO40	AC_OK	I	AC Adaptor Plug in
74	GPIO41	PM_RSMRST#	O	10K pull down to GND
75	GPI42	BAT_IN	I	
76	GPI43	CLRTC_EC	I	
77	GPIO44/SCL1	SMB0_CLK	I/OD	4.7K pull high to +3VA_EC
78	GPIO45/SDA1	SMB0_DAT	I/OD	4.7K pull high to +3VA_EC
79	GPIO46/SCL2	SMB1_CLK	I/OD	10K pull high to +3V
80	GPIO47/SDA2	SMB1_DAT	I/OD	10K pull high to +3V
81	GPIO48/KSO16	KB pin 28	I	for KB type detection
82	GPIO49/KSO17	KB pin 27	I	for KB type detection
83	GPIO4A/PSCLK1	AUO_SCL	O	for AUO, default H at S0
84	GPIO4B/PSDAT1	AUO_SDA	O	for AUO, default L at S0
85	GPIO4C/PSCLK2	AUO_CSB	O	for AUO, default H at S0
86	GPIO4D/PSDAT2	LVDD_EN	I	for AUO 7" Panel
87	GPIO4E/PSCLK3	TP_CLK	I/OD	10K pull high to +3V
88	GPIO4F/PSDAT3	TP_DAT	I/OD	10K pull high to +3V
89	GPIO50/SELIO#	BATSEL_3S	O	Battery series, H:3S, L:4S
90	GPIO52/E51_CS#	CHG_LED_UP#	O	
91	GPIO53/CAPLED	CAP_LED#	O	
92	GPIO54	PWR_LED_UP	O	
93	GPIO55/SCRLLED	SCRL_LED#	O	
95	GPIO56	PWR4G_SW#	I	Internal pull high
97	GPXOA00/SDICS#	SPI_MODE#	O	4.7K pull down to GND
98	GPXOA01/SDICLK	SUSC_ON	O	
99	GPXOA02/SDIDO	VSUS_ON	O	
100	GPXOA03	CPU_VRON	O	
101	GPXOA04	SUSB_ON	O	
102	GPXOA05	ICH_PWROK	O	
103	GPXOA06	VOLT_CTRL	O	
104	GPXOA07	CHG_EN#	O	Battery charging enabled
105	GPXOA08	PRECHG	O	
106	GPXOA09	SPI_WP#	O	
107	GPXOA10	OP_SD#	O	Audio OP
108	GPXOA11	BAT_LEARN	O	
109	GPXID0/SDIDI	BATSEL_2P#	O	Battery parallel, H:1P, L:2P-3P
110	GPXID1	NC	O	
112	GPXID2	THRO_CPU	O	Active if CPU temperature over spec
114	GPXID3	SUSB#	I	100K pull down to GND
115	GPXID4	SUSC#	I	100K pull down to GND
116	GPXID5	CPUPWR_GD	I	Pull high to +3V
117	GPXID6	VSUS_GD	I	
118	GPXID7	NC	O	
121	GPIO57	INTERNET#	I	Internal pull high
126	GPIO57/SPICLK	SPI_CLK	O	
127	GPIO59/TEST_CLK	NC	O	

<Variant Name>

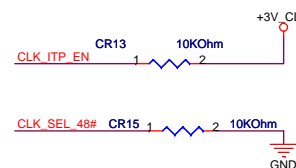
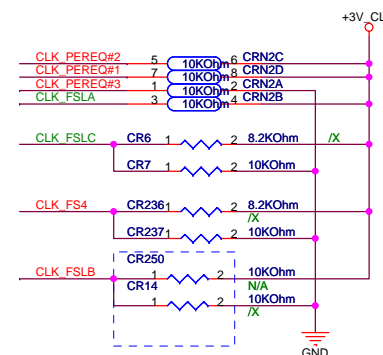
		<b>Title : EC Pin Define</b>	
ASUSTek Computer INC.		Engineer: <b>Jeff Li</b>	
Size	Project Name		Rev
A3	<b>1000H_MB</b>		1.3G
Date:	Tuesday, February 10, 2009	Sheet	4 of 47



1:Disable  
0:Enable

PEREQ1:PCIEx0 & PCIEx1  
PEREQ2:PCIEx2 & PCIEx3 & SATA  
PEREQ3:PCIEx4 & PCIEx5 & PCIEx6

FSC	FSB	FSA	CPU	PCIE	SATA
0	1	1	166	100	100
0	0	1	133	100	100
1	0	1	100	100	100

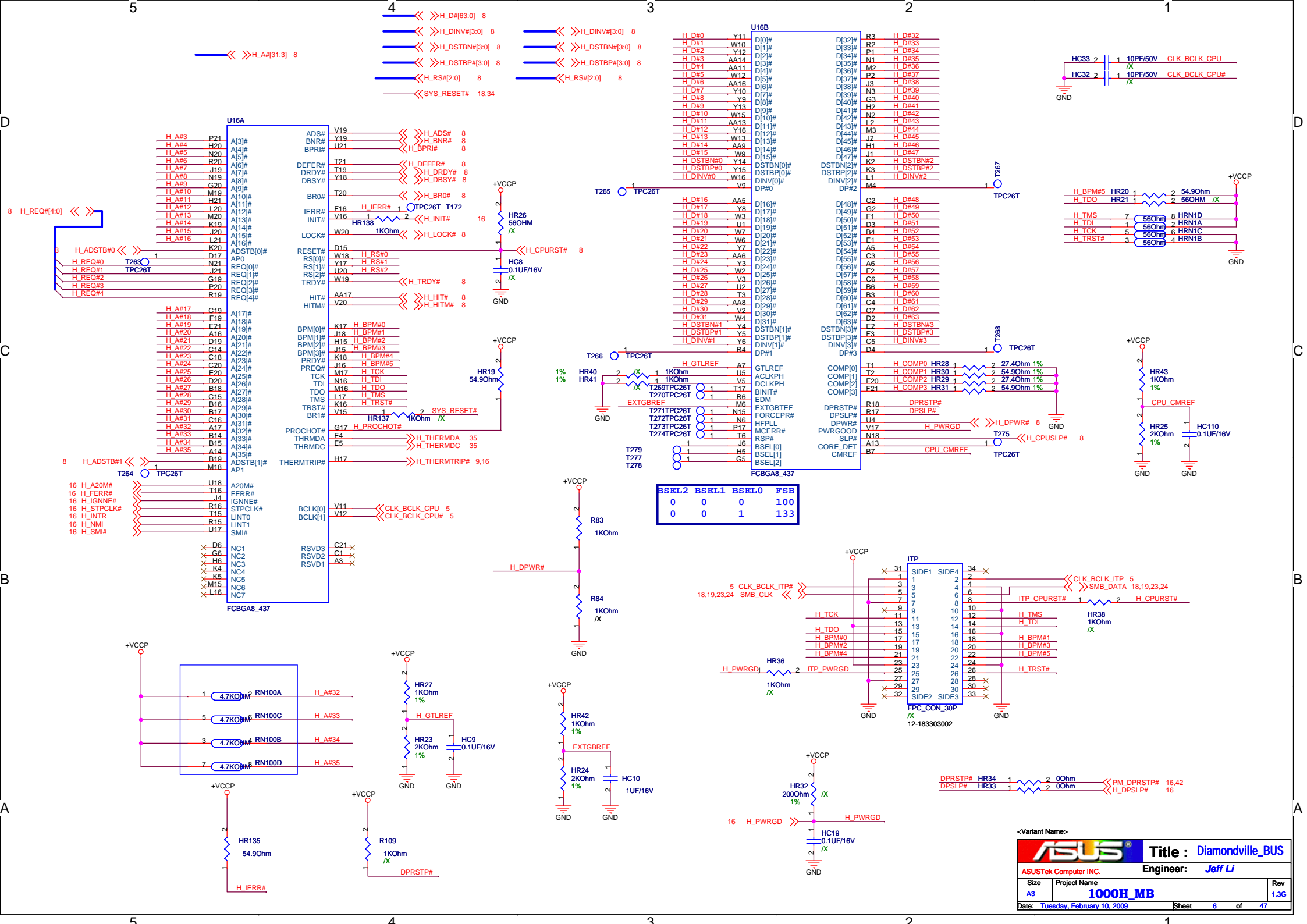


<Variant Name>

**ASUS** Title : Clock Gen\_ICS9LPRS427  
ASUSTek Computer INC. Engineer: Jeff Li

Size	Project Name	Rev
A3	1000H_MB	1.3G

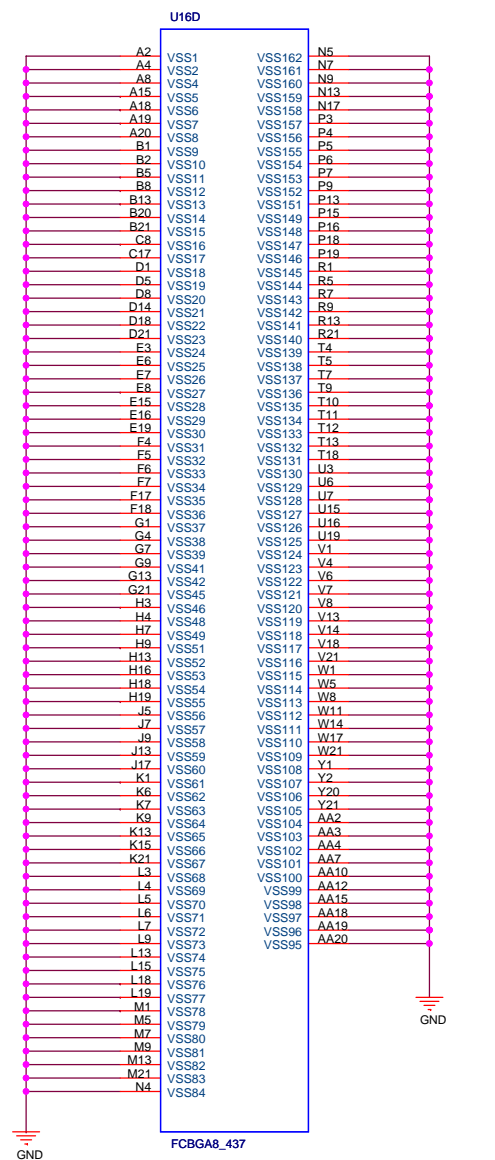
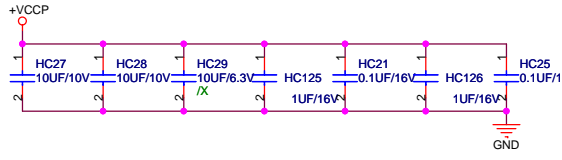
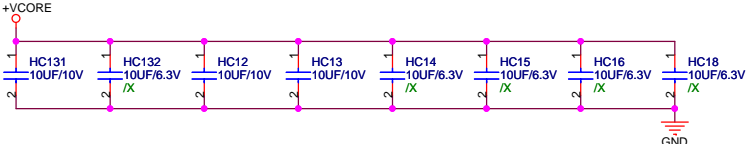
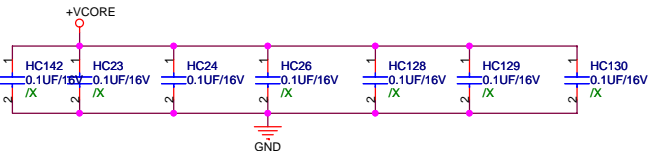
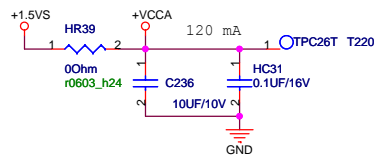
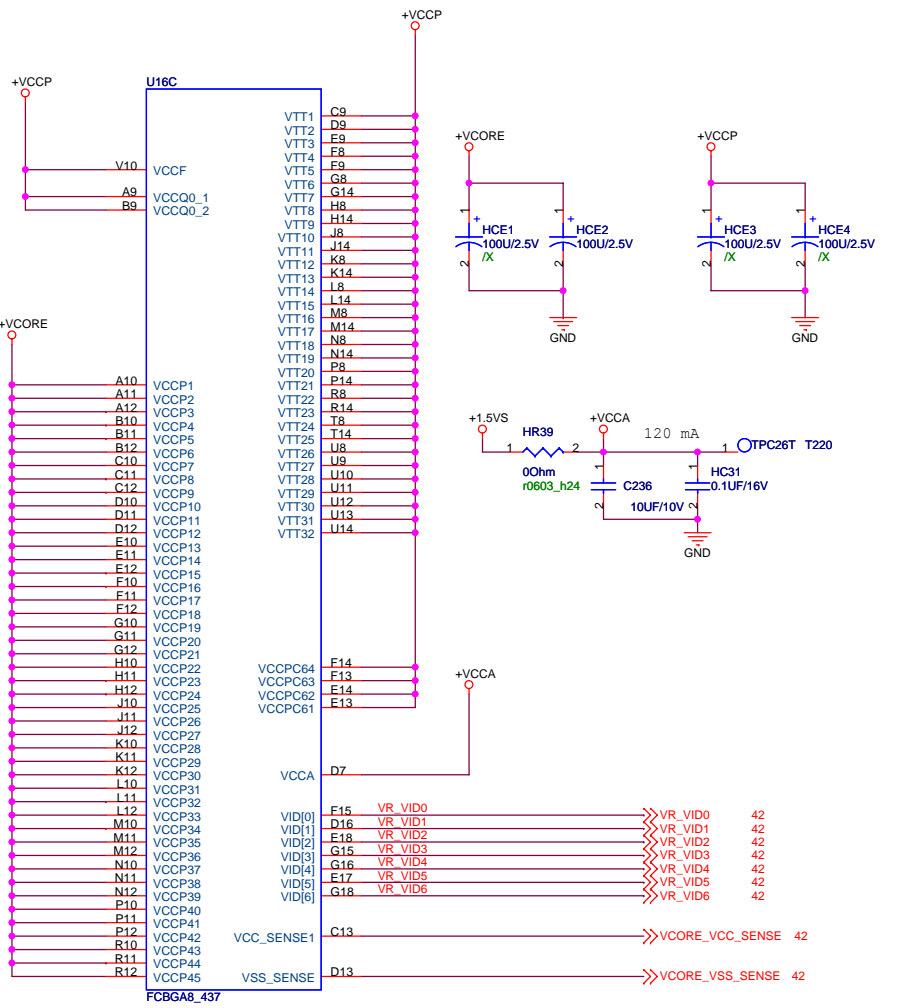
Date: Tuesday, February 10, 2009 Sheet 5 of 47



U16B

H D#0	Y11	D[0]#	R3	H D#32
H D#1	W10	D[1]#	R2	H D#33
H D#2	Y12	D[2]#	P1	H D#34
H D#3	AA14	D[3]#	N1	H D#35
H D#4	AA11	D[4]#	M2	H D#36
H D#5	W12	D[5]#	P2	H D#37
H D#6	AA16	D[6]#	N3	H D#38
H D#7	Y10	D[7]#	N3	H D#39
H D#8	Y9	D[8]#	G3	H D#40
H D#9	Y13	D[9]#	H2	H D#41
H D#10	W15	D[10]#	N2	H D#42
H D#11	AA13	D[11]#	L2	H D#43
H D#12	Y11	D[12]#	M3	H D#44
H D#13	W12	D[13]#	H1	H D#45
H D#14	AA9	D[14]#	J1	H D#46
H D#15	W9	D[15]#	D47	H D#47
H DSTBN#0	Y14	DSTBN[0]#	K2	H DSTBN#2
H DSTBP#0	Y15	DSTBP[0]#	K3	H DSTBP#2
H DINV#0	W16	DINV[0]#	M4	H DINV#2
	V9	DP#0		
H D#16	AA5	D[16]#	C2	H D#48
H D#17	Y8	D[17]#	G2	H D#49
H D#18	W3	D[18]#	F1	H D#50
H D#19	U1	D[19]#	D4	H D#51
H D#20	W7	D[20]#	B3	H D#52
H D#21	W8	D[21]#	E1	H D#53
H D#22	Y7	D[22]#	A5	H D#54
H D#23	AA6	D[23]#	C3	H D#55
H D#24	Y3	D[24]#	A6	H D#56
H D#25	W2	D[25]#	F2	H D#57
H D#26	U2	D[26]#	D55	H D#58
H D#27	V3	D[27]#	C6	H D#59
H D#28	T3	D[28]#	B3	H D#60
H D#29	AA8	D[29]#	C4	H D#61
H D#30	V2	D[30]#	C7	H D#62
H D#31	W4	D[31]#	D2	H D#63
H DSTBN#1	Y4	DSTBN[1]#	E2	H DSTBN#3
H DSTBP#1	V5	DSTBP[1]#	F3	H DSTBP#3
H DINV#1	Y8	DINV[1]#	C6	H DINV#3
	R4	DP#1	D4	

BSEL2	BSEL1	BSEL0	FSB
0	0	0	100
0	0	1	133

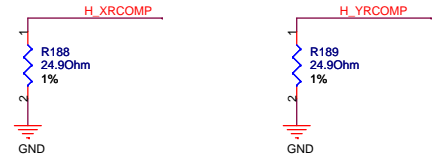


ASUS® Title: Diamondville\_PWR  
 ASUSTek Computer INC. Engineer: Jeff Li  
 Size: A3 Project Name: 1000H\_MB Rev: 1.3G  
 Date: Tuesday, February 10, 2009 Sheet: 7 of 47

**Power :  
+VCCP**

**RCOMP**

For Calibrating the FSB I/O Buffer



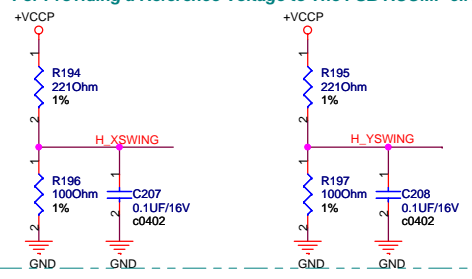
**SCOMP**

For Slew Rate Compensation on the FSB

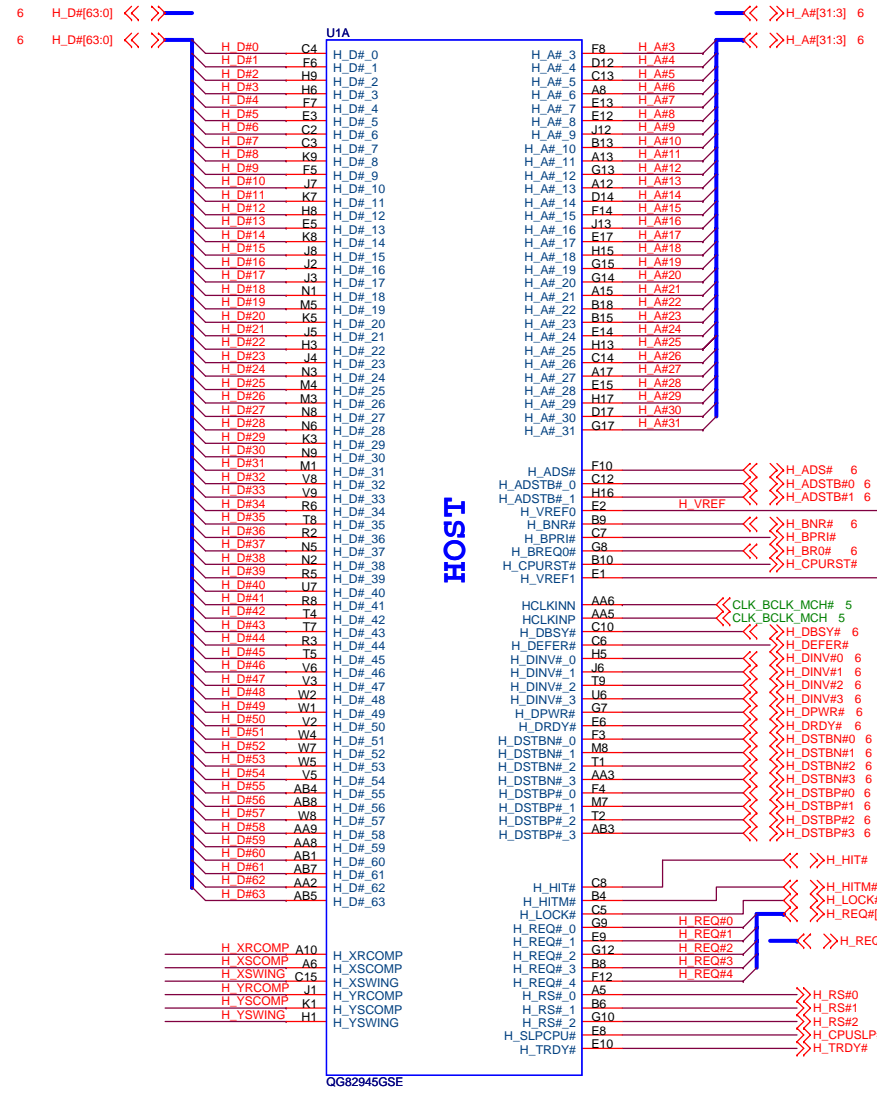


**Voltage Swing**

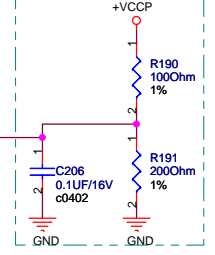
For Providing a Reference Voltage to The FSB RCOMP circuits



Signal voltage level =  
0.3125\*VCCP  
Trace should be 10 mil wide  
with 20 mil spacing



**AGTL+ I/O Voltage Reference**



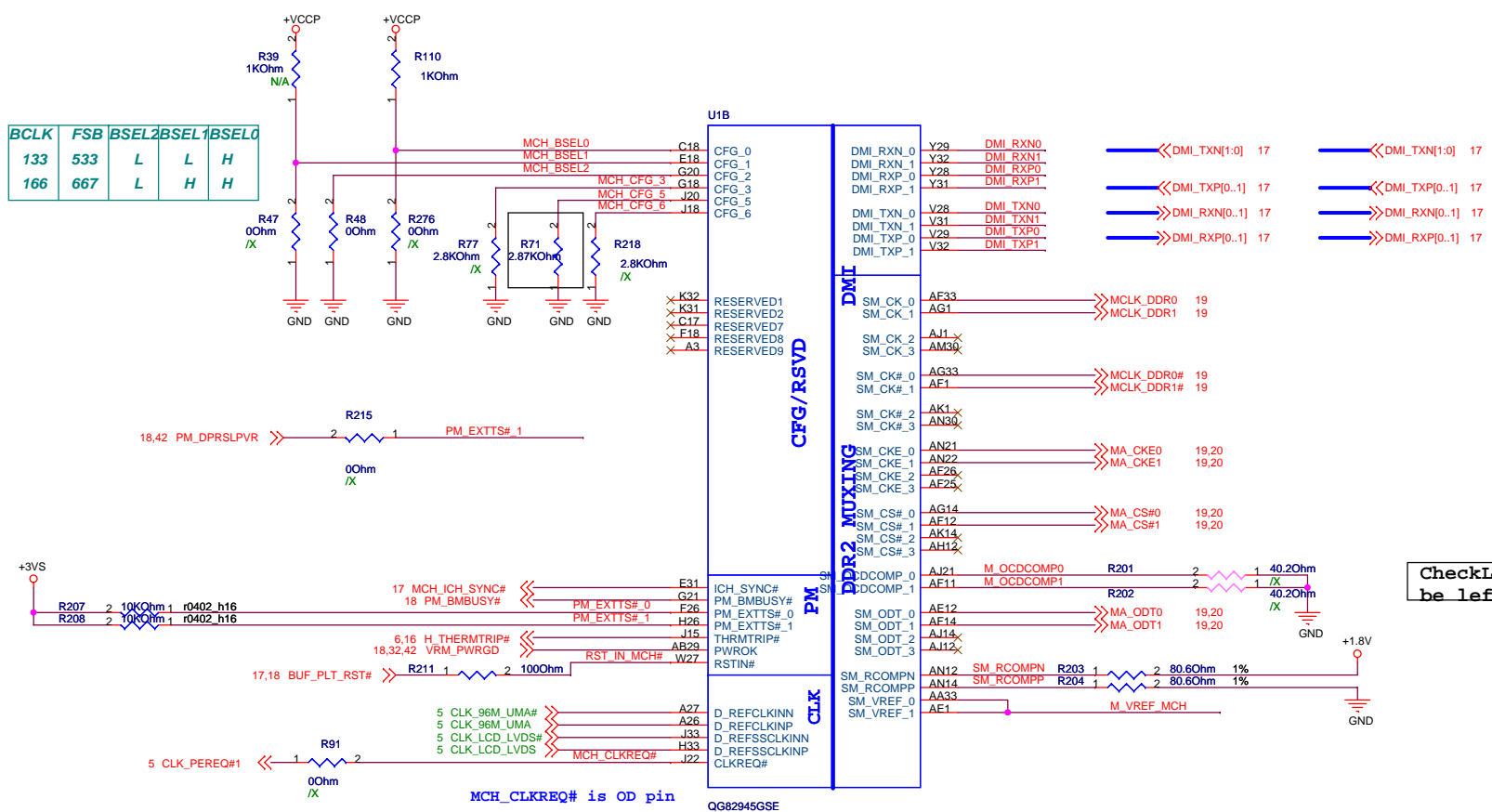
Layout Note:  
0.1uF should be placed 100mils or less from GMCH pin.

<Variant Name>

<b>ASUS</b>		<b>Title : NB-945GMS(HOST)</b>
ASUSTeK COMPUTER INC.		Engineer: <b>Jeff Li</b>
Size A3	Project Name <b>1000H_MB</b>	Rev 1.3G
Date: <b>Tuesday, February 10, 2009</b>		Sheet <b>8</b> of <b>47</b>



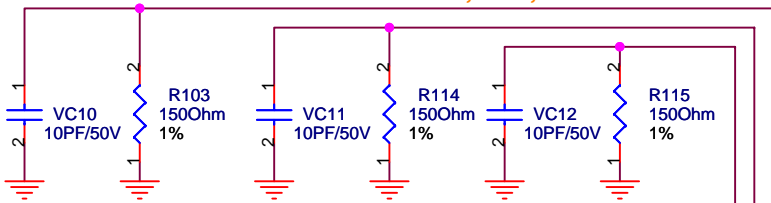
BCLK	FSB	BSEL2	BSEL1	BSEL0
133	533	L	L	H
166	667	L	H	H



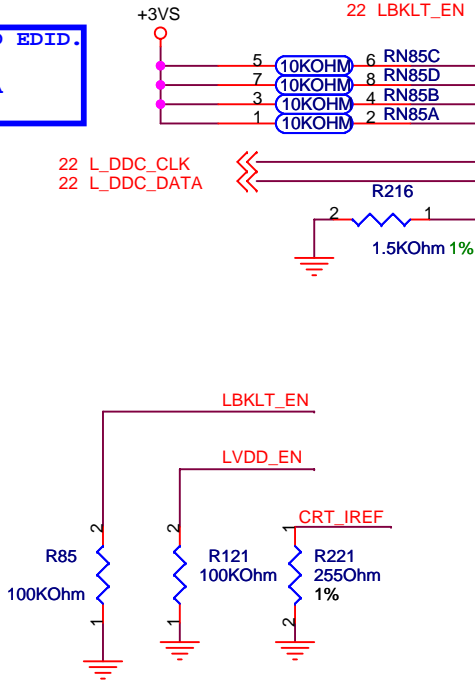
CheckList notes : Can be left as NC

MCH\_CLKREQ# is OD pin

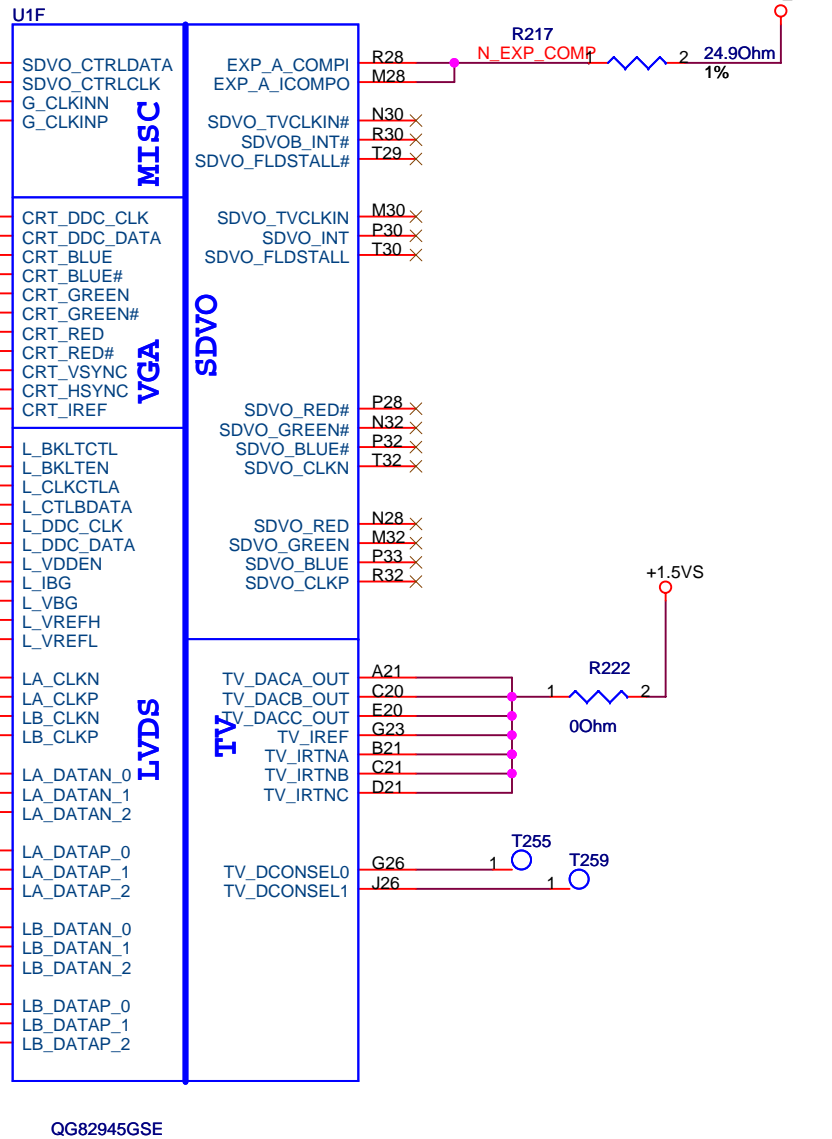
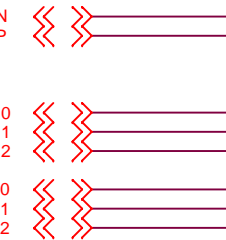
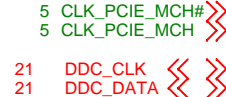
**Close to GMCH**  
R103,R114,R115



IF USE NB READ EDID,  
MUST CONNECT  
L\_DDC\_CLK&DATA



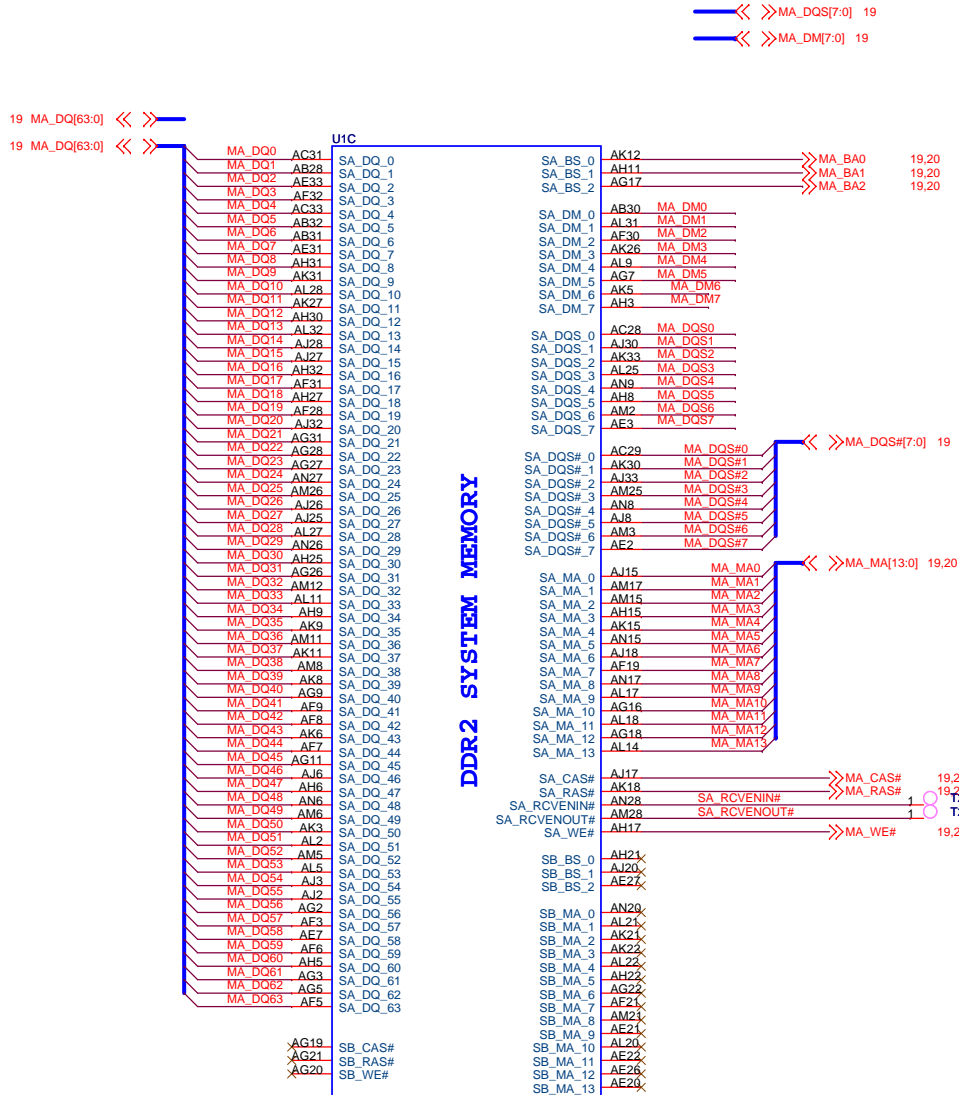
**Close to GMCH**



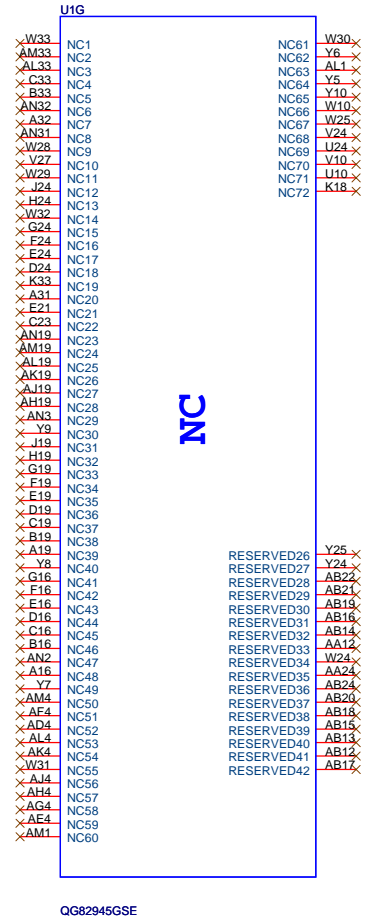
QG82945GSE

<Variant Name>

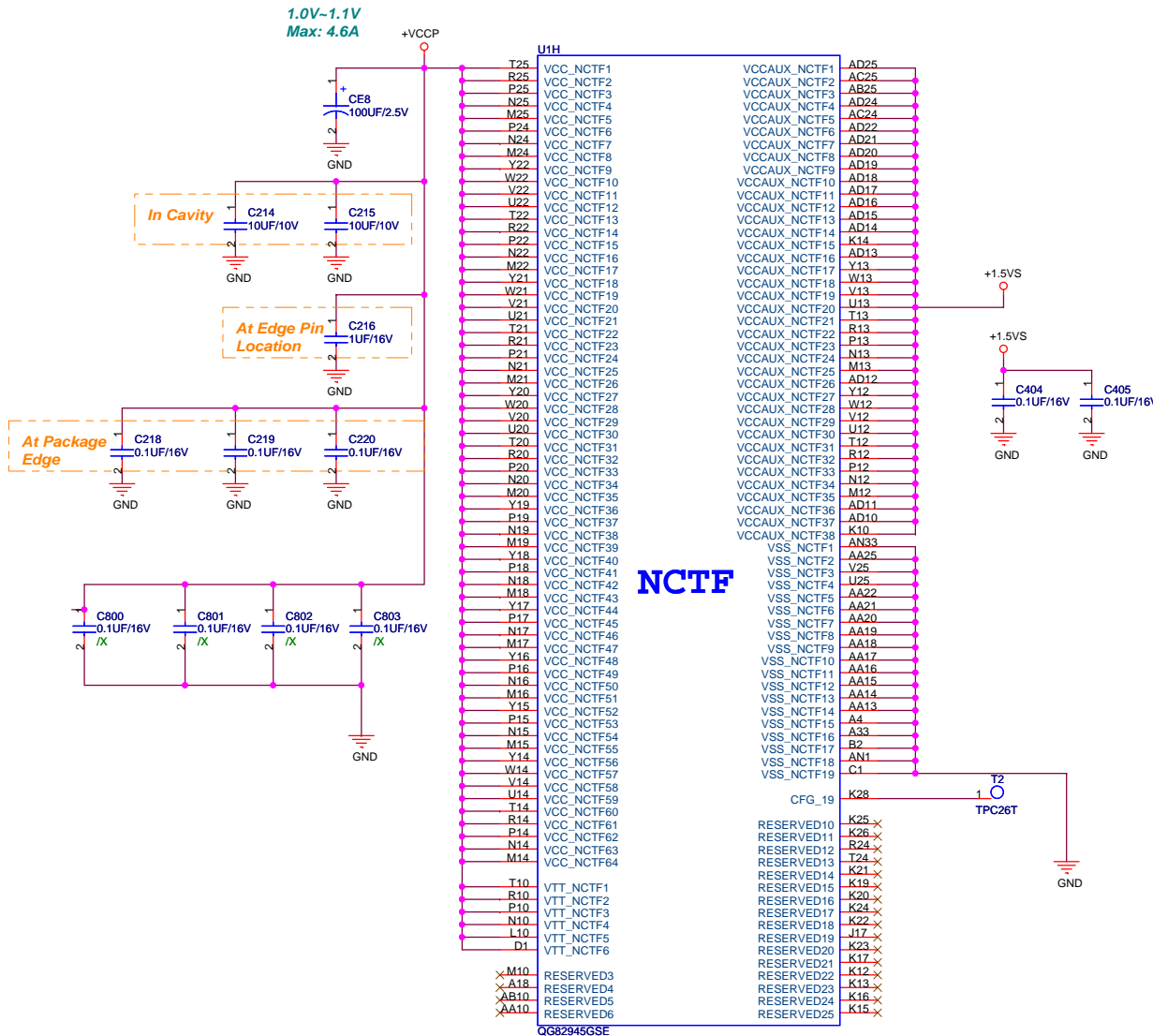
		<b>Title : NB-945GMS(GRAPHIC)</b>	
ASUSTeK COMPUTER INC.		Engineer: <b>Jeff Li</b>	
Size A4	Project Name <b>1000H_MB</b>	Rev 1.3G	
Date: <b>Tuesday, February 10, 2009</b>		Sheet <b>10</b> of <b>47</b>	



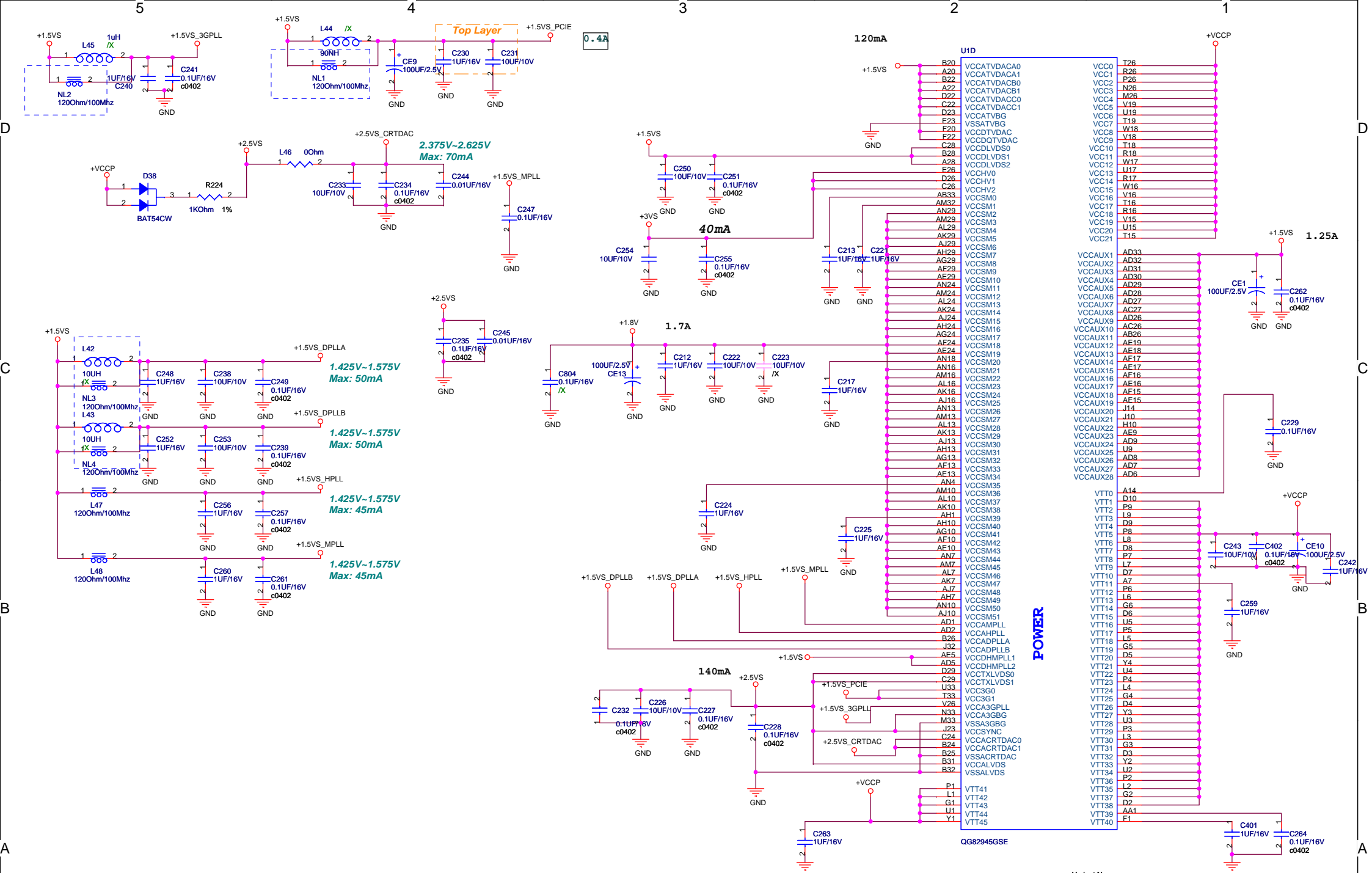
QG82945GSE

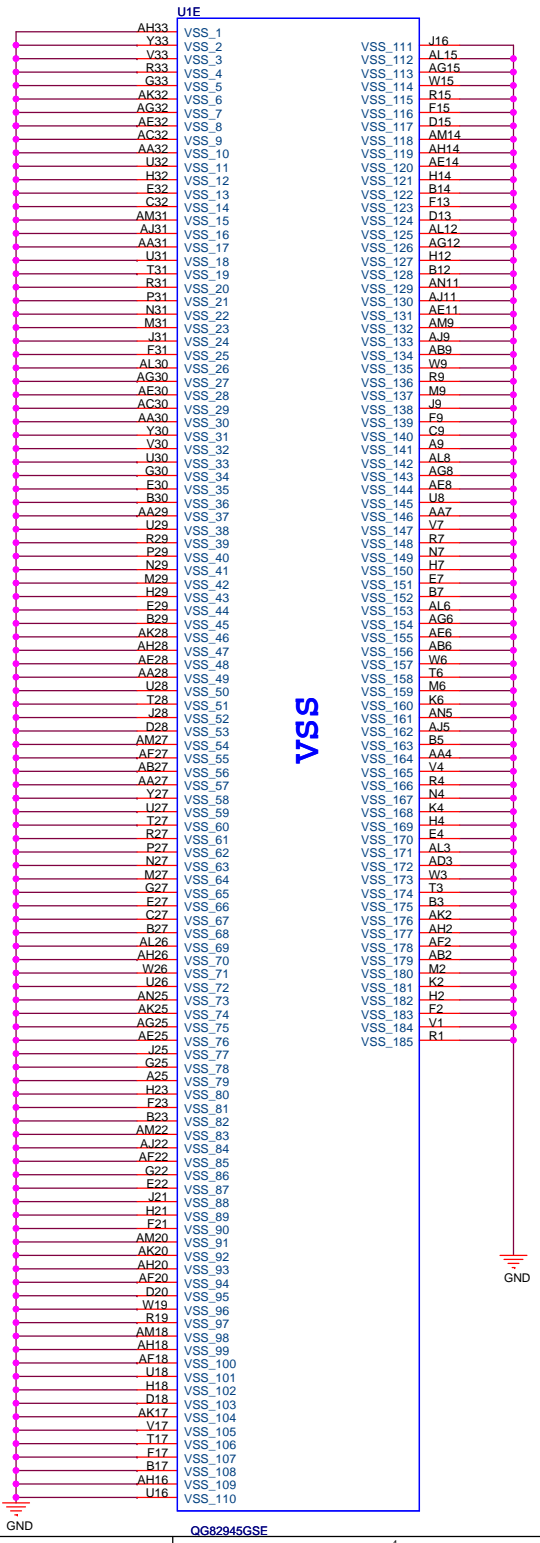


QG82945GSE



**CFG\_19(K28) Strapping :**  
**DMI LANE Reversal:**  
 0:Normal Operation (Default)  
 1.:Reversal Lanes, 3->0,2->1..etc  
 Note:945GMS doesn't support DMI Lane Reversal





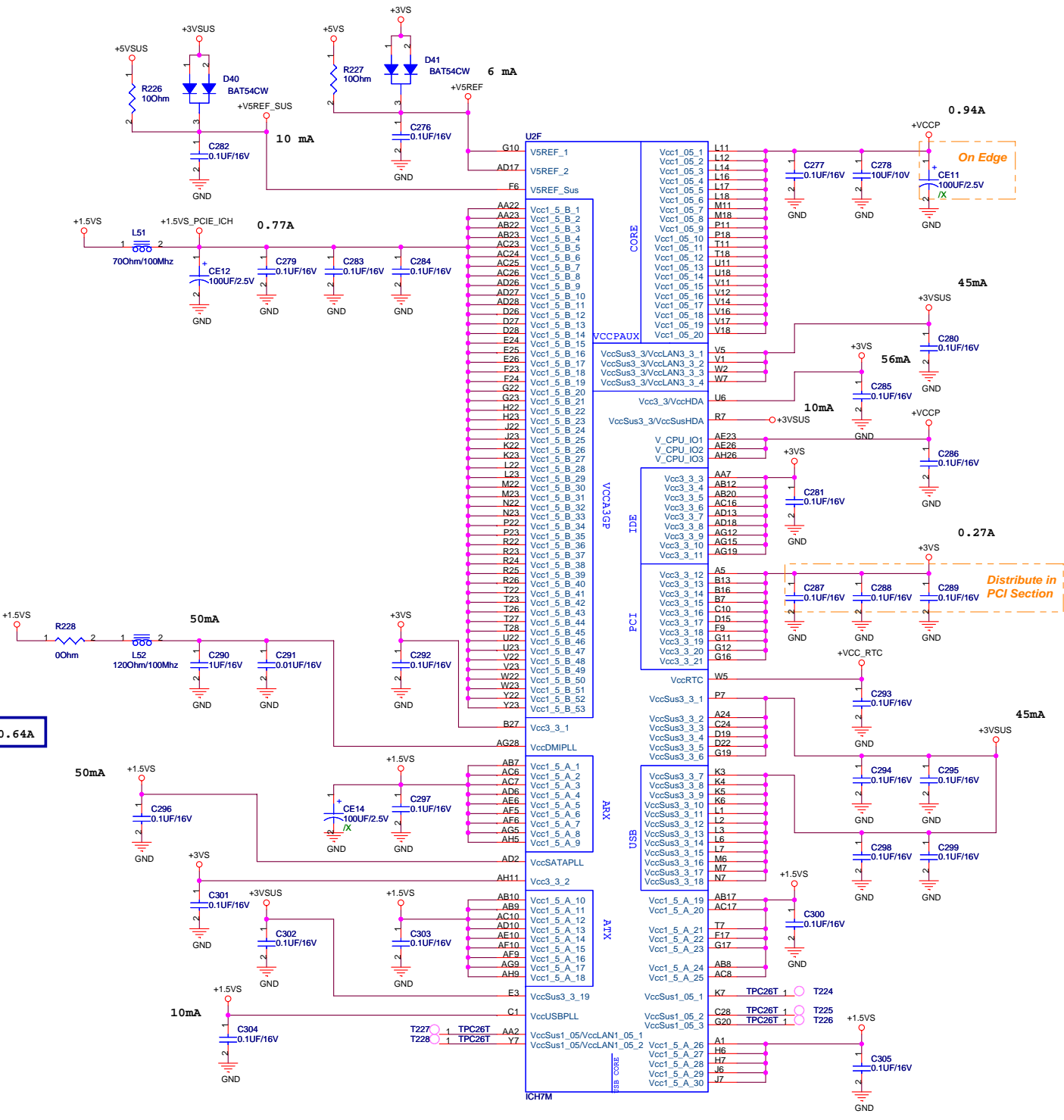
U1E

VSS

<Variant Name>

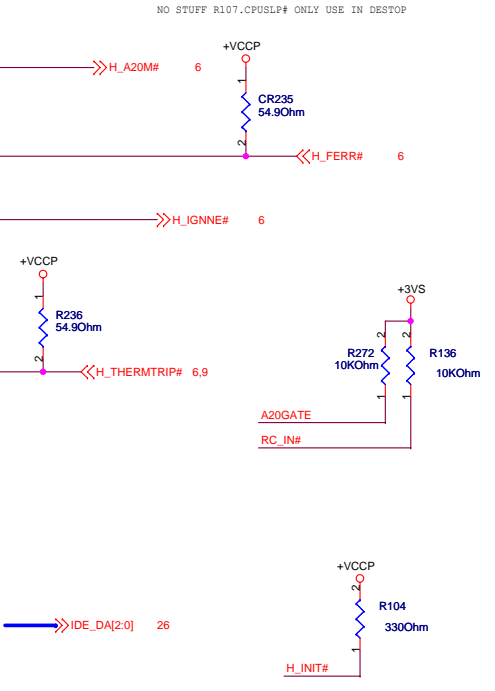
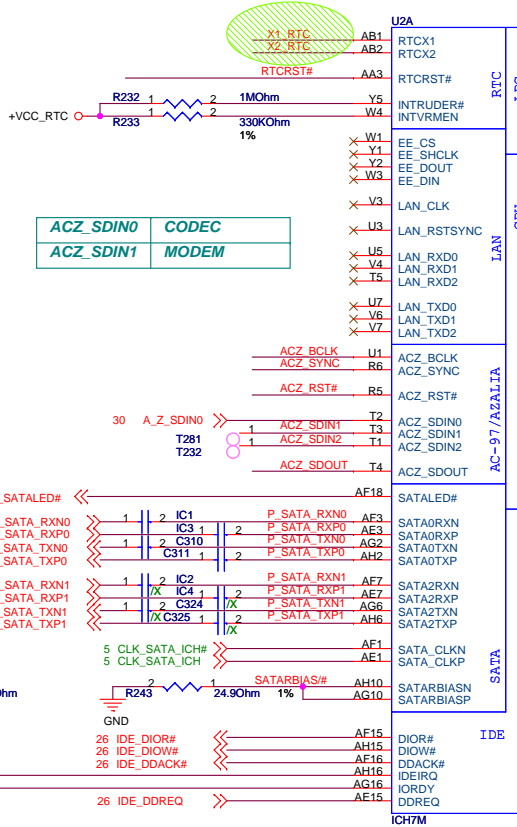
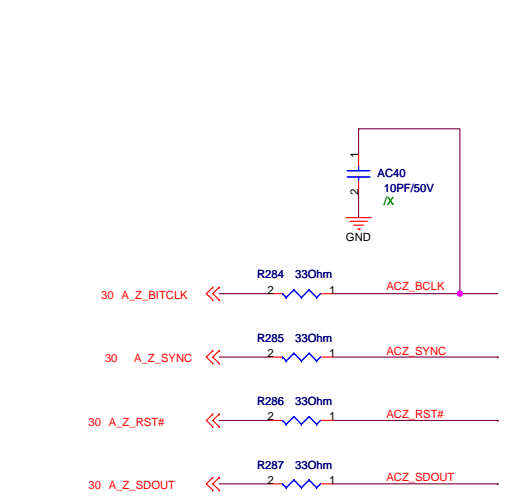
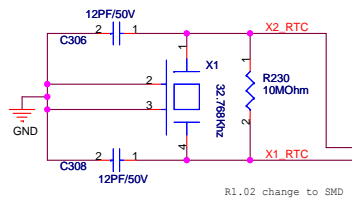
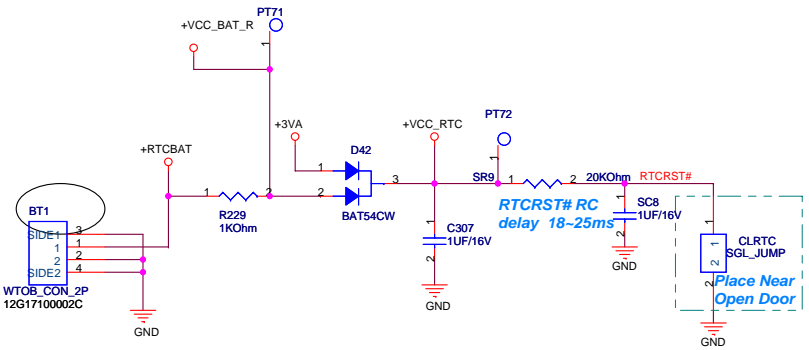
		<b>Title :</b> NB-945GMS(GND)	
ASUSTek COMPUTER INC.		Engineer: <i>Jeff Li</i>	
Size	Project Name	Rev	
A3	<b>1000H_MB</b>	1.3G	
Date: <b>Tuesday, February 10, 2009</b>		Sheet	14 of 47

Vcc1\_5\_A=0.64A

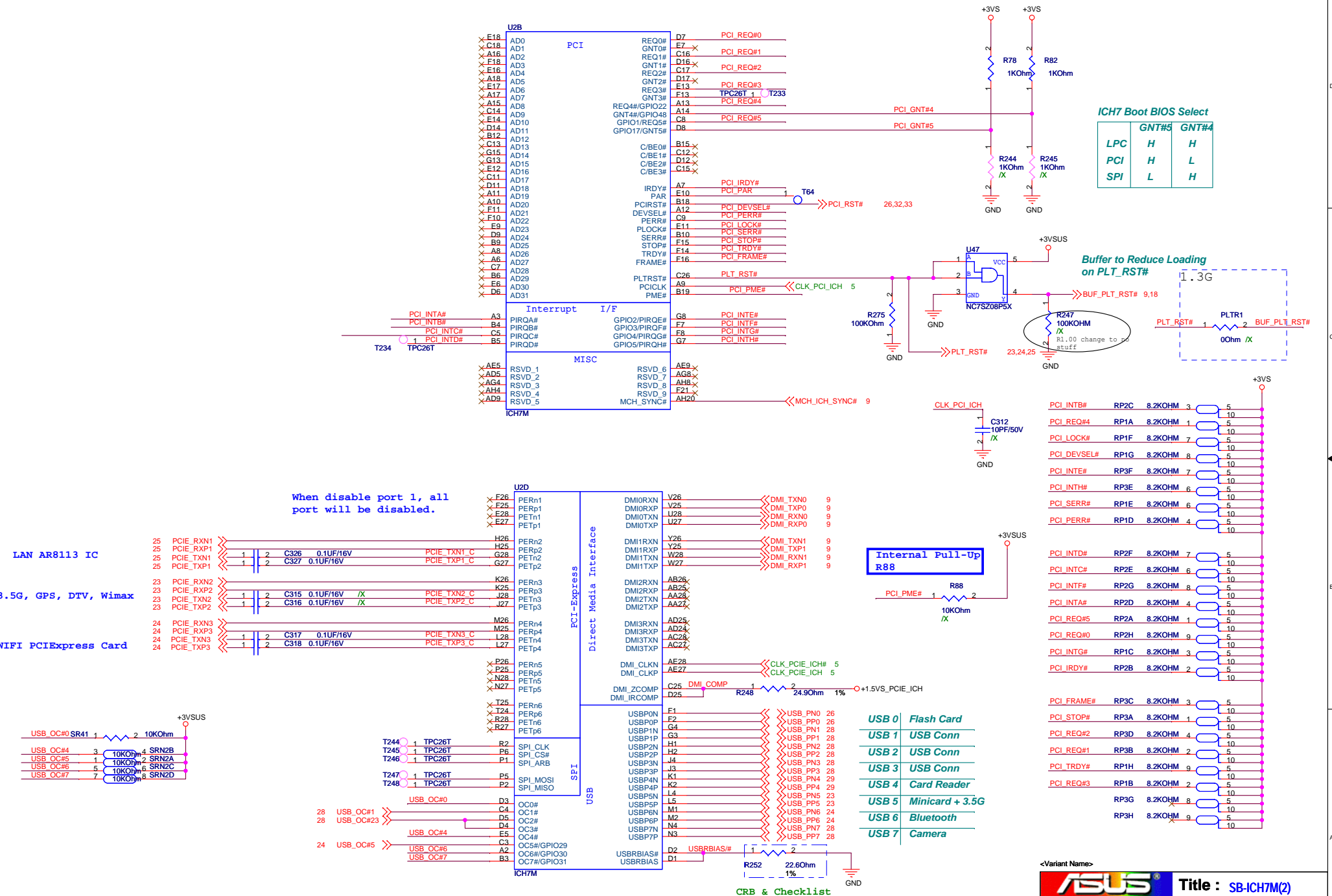


U2E		
A4	Vss1	Vss98
A23	Vss2	R1
B1	Vss3	R11
B8	Vss4	R12
B11	Vss5	R13
B14	Vss6	R14
B17	Vss7	R15
B20	Vss8	R16
B26	Vss9	R17
B28	Vss10	R18
C2	Vss11	T6
C6	Vss12	T12
C27	Vss13	T13
D10	Vss14	T14
D13	Vss15	T15
D18	Vss16	T16
D21	Vss17	T17
D24	Vss18	U4
E1	Vss19	U12
E2	Vss20	Vss117
F4	Vss21	Vss118
F8	Vss22	Vss119
F15	Vss23	U16
F3	Vss24	U17
F4	Vss25	U24
F26	Vss26	Vss123
F27	Vss27	Vss124
F28	Vss28	Vss125
G1	Vss29	Vss126
G2	Vss30	Vss127
G5	Vss31	Vss128
G6	Vss32	Vss129
G9	Vss33	Vss130
G14	Vss34	W6
G18	Vss35	W24
G21	Vss36	Vss132
G24	Vss37	W25
G25	Vss38	W26
G26	Vss39	Y3
H3	Vss40	Y24
H4	Vss41	Y27
H5	Vss42	Y28
H24	Vss43	AA1
H27	Vss44	AA24
H28	Vss45	AA25
J1	Vss46	AB4
J2	Vss47	AB6
J5	Vss48	AB11
J24	Vss49	AB14
J25	Vss50	AB15
J26	Vss51	AB19
K24	Vss52	AB21
K27	Vss53	AB24
K28	Vss54	AB27
L13	Vss55	AB28
L15	Vss56	Vss152
L24	Vss57	AC2
L25	Vss58	AC9
L26	Vss59	AC11
M3	Vss60	AD1
M5	Vss61	AD3
M12	Vss62	AD4
M13	Vss63	AD7
M14	Vss64	AD8
M15	Vss65	AD15
M16	Vss66	AD19
M17	Vss67	AD19
M24	Vss68	AD23
M27	Vss69	AE2
M28	Vss70	AE4
N1	Vss71	AE8
N2	Vss72	AE11
N5	Vss73	AE13
N6	Vss74	AE18
N11	Vss75	AE21
N12	Vss76	AE24
N13	Vss77	AE25
N14	Vss78	Vss174
N15	Vss79	Vss175
N16	Vss80	AF2
N17	Vss81	AF4
N18	Vss82	AF8
N24	Vss83	AF11
N25	Vss84	AF17
N26	Vss85	AF22
P3	Vss86	AF28
P4	Vss87	Vss180
P12	Vss88	Vss181
P13	Vss89	AG1
P14	Vss90	AG3
P15	Vss91	AG7
P17	Vss92	AG11
P24	Vss93	AG14
P27	Vss94	AG17
P27	Vss95	AG20
P27	Vss96	AG25
P27	Vss97	AG25
P27	Vss98	AG25
P27	Vss99	AG25
P27	Vss100	AG25
P27	Vss101	AG25
P27	Vss102	AG25
P27	Vss103	AG25
P27	Vss104	AG25
P27	Vss105	AG25
P27	Vss106	AG25
P27	Vss107	AG25
P27	Vss108	AG25
P27	Vss109	AG25
P27	Vss110	AG25
P27	Vss111	AG25
P27	Vss112	AG25
P27	Vss113	AG25
P27	Vss114	AG25
P27	Vss115	AG25
P27	Vss116	AG25
P27	Vss117	AG25
P27	Vss118	AG25
P27	Vss119	AG25
P27	Vss120	AG25
P27	Vss121	AG25
P27	Vss122	AG25
P27	Vss123	AG25
P27	Vss124	AG25
P27	Vss125	AG25
P27	Vss126	AG25
P27	Vss127	AG25
P27	Vss128	AG25
P27	Vss129	AG25
P27	Vss130	AG25
P27	Vss131	AG25
P27	Vss132	AG25
P27	Vss133	AG25
P27	Vss134	AG25
P27	Vss135	AG25
P27	Vss136	AG25
P27	Vss137	AG25
P27	Vss138	AG25
P27	Vss139	AG25
P27	Vss140	AG25
P27	Vss141	AG25
P27	Vss142	AG25
P27	Vss143	AG25
P27	Vss144	AG25
P27	Vss145	AG25
P27	Vss146	AG25
P27	Vss147	AG25
P27	Vss148	AG25
P27	Vss149	AG25
P27	Vss150	AG25
P27	Vss151	AG25
P27	Vss152	AG25
P27	Vss153	AG25
P27	Vss154	AG25
P27	Vss155	AG25
P27	Vss156	AG25
P27	Vss157	AG25
P27	Vss158	AG25
P27	Vss159	AG25
P27	Vss160	AG25
P27	Vss161	AG25
P27	Vss162	AG25
P27	Vss163	AG25
P27	Vss164	AG25
P27	Vss165	AG25
P27	Vss166	AG25
P27	Vss167	AG25
P27	Vss168	AG25
P27	Vss169	AG25
P27	Vss170	AG25
P27	Vss171	AG25
P27	Vss172	AG25
P27	Vss173	AG25
P27	Vss174	AG25
P27	Vss175	AG25
P27	Vss176	AG25
P27	Vss177	AG25
P27	Vss178	AG25
P27	Vss179	AG25
P27	Vss180	AG25
P27	Vss181	AG25
P27	Vss182	AG25
P27	Vss183	AG25
P27	Vss184	AG25
P27	Vss185	AG25
P27	Vss186	AG25
P27	Vss187	AG25
P27	Vss188	AG25
P27	Vss189	AG25
P27	Vss190	AG25
P27	Vss191	AG25
P27	Vss192	AG25
P27	Vss193	AG25
P27	Vss194	AG25

**ASUS** Title : SB-ICH7M(PWR)  
 ASUSTek COMPUTER INC. Engineer: Jeff Li  
 Size Custom Project Name 1000H MB Rev 1.3G  
 Date: Tuesday, February 10, 2009 Sheet 15 of 47



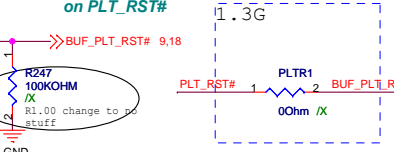




**ICH7 Boot BIOS Select**

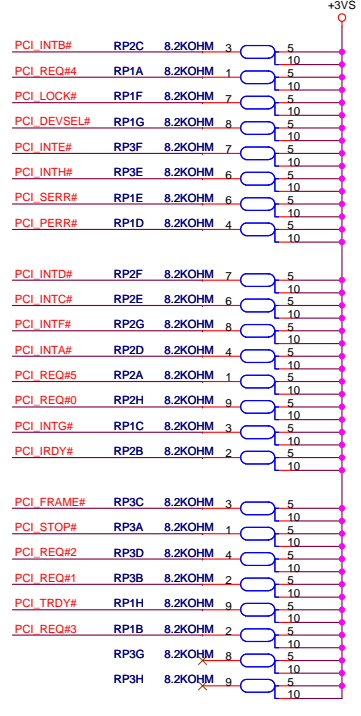
	GNT#5	GNT#4
LPC	H	H
PCI	H	L
SPI	L	H

Buffer to Reduce Loading on PLT\_RST#



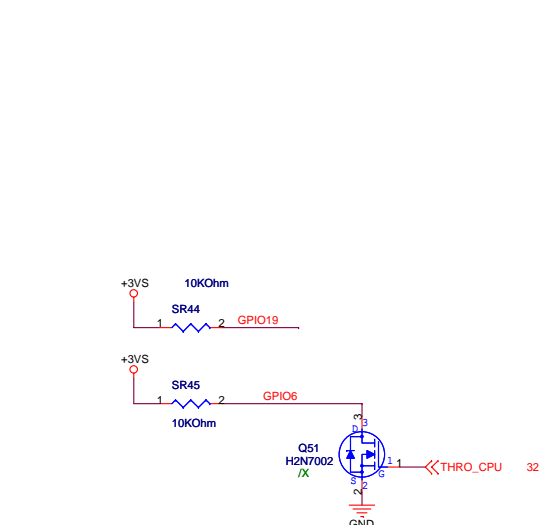
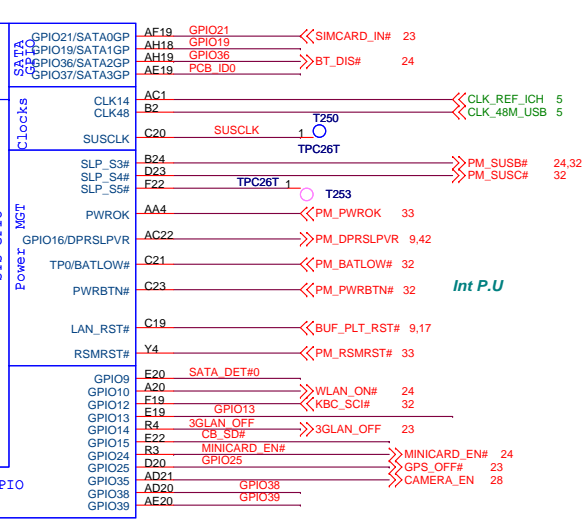
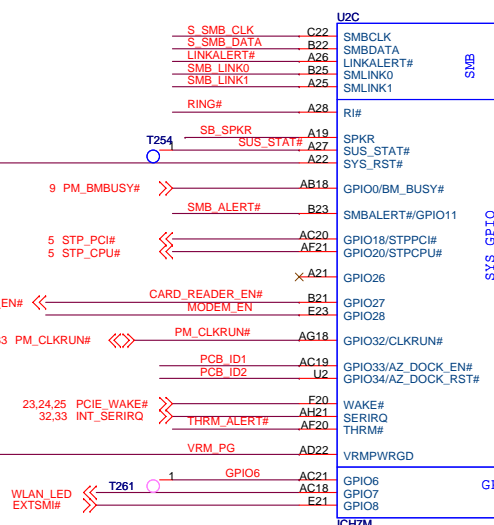
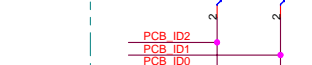
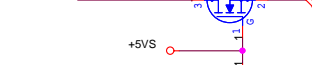
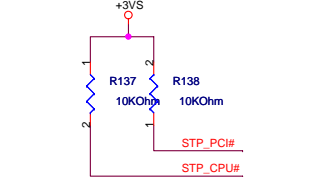
When disable port 1, all port will be disabled.

Internal Pull-Up R88



<Variant Name>

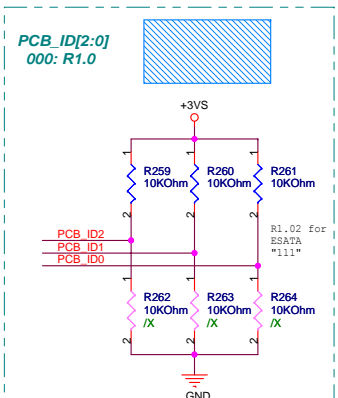
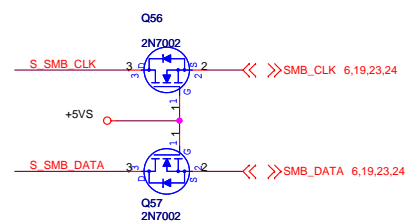
CRB & Checklist



05/12/30, refer Z96J R1.01 to delete and change net name from VRMPWRGD to VRM\_PWRGD.

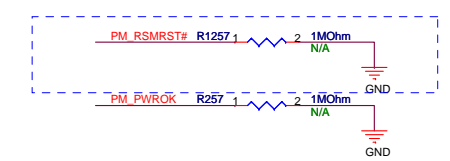
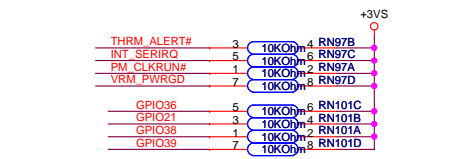
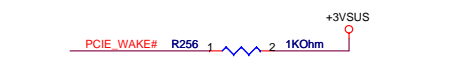
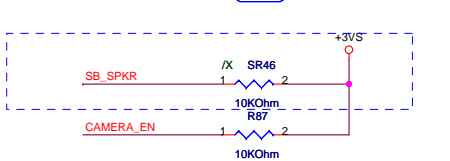
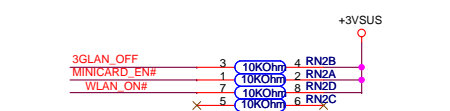
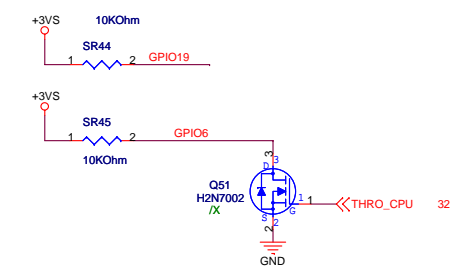
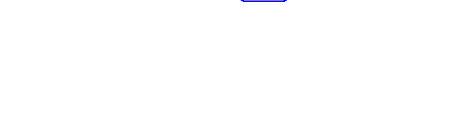
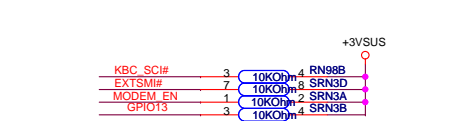
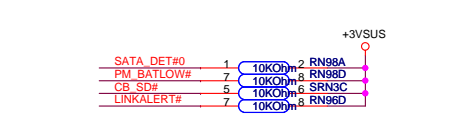
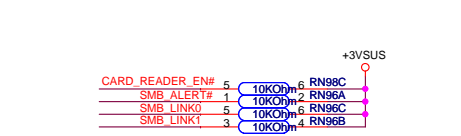
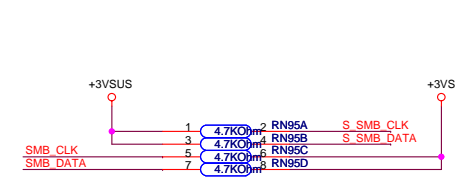
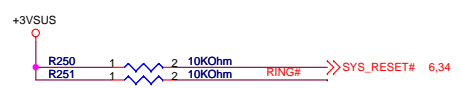


	WLAN_LED	WLAN	BT
High	v	v	v
High	v	v	x
High	x	x	v
Low	x	x	x



PCB\_VID3: PROJECT CODE

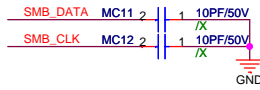
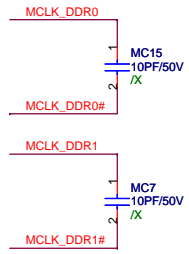
SKU	PCB ID2 SB GPIO 34	PCB ID1 SB GPIO 33	PCB ID0 SB GPIO 37
BASIC	1	1	1
3G	1	1	0
DTV	1	0	1
GPS	1	0	0
N280/BASIC	0	1	1
N280/3G	0	1	0
N280/DTV	0	0	1
N280/GPS	0	0	0



<Variant Name>

**ASUS** Title: SB-ICH7M(3)  
 ASUSTeK COMPUTER INC Engineer: Jeff Li

Size	Project Name	Rev
Custom	1000H MB	1.3G
Date: Tuesday, February 10, 2009	Sheet	18 of 47

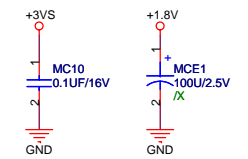
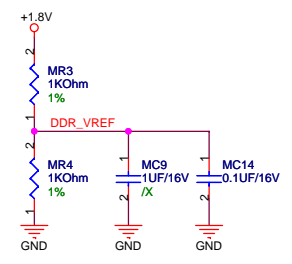
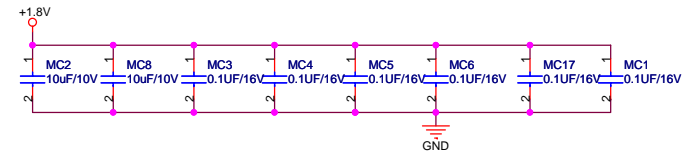


- MA\_DQ[63:0] 11
- MA\_DQS[7:0] 11
- MA\_DQS#[7:0] 11
- MA\_DM[7:0] 11
- MA\_MA[13:0] 11,20
- MA\_BA[2:0] 11,20

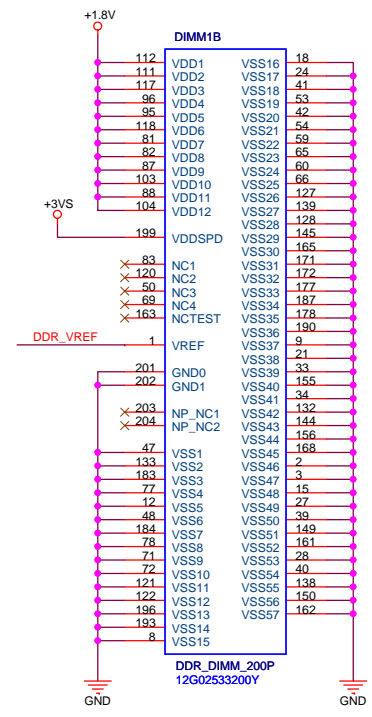
STD Type

DIMM1A			
MA_MA0	102	A0	DQ0
MA_MA1	101	A1	DQ1
MA_MA2	100	A2	DQ2
MA_MA3	99	A3	DQ3
MA_MA4	98	A4	DQ4
MA_MA5	97	A5	DQ5
MA_MA6	94	A6	DQ6
MA_MA7	92	A7	DQ7
MA_MA8	93	A8	DQ8
MA_MA9	105	A9	DQ9
MA_MA10	91	A10/AP	DQ10
MA_MA11	90	A11	DQ11
MA_MA12	89	A12	DQ12
MA_MA13	116	A13	DQ13
	86	A14	DQ14
	84	A15	DQ15
	85	A16_BA2	DQ16
MA_BA2		BA0	DQ17
MA_BA0	107	BA1	DQ18
MA_BA1	106	S0#	DQ19
	110	S1#	DQ20
	115	CK0	DQ21
9,20 MA_CS#0		CK0#	DQ22
9,20 MA_CS#1		CK1	DQ23
9 MCLK_DDR0		CK1#	DQ24
9 MCLK_DDR0#		CKE0	DQ25
9 MCLK_DDR1		CKE0#	DQ26
9 MCLK_DDR1#		CKE1	DQ27
9,20 MA_CKE0		CKE1#	DQ28
9,20 MA_CKE1		CAS#	DQ29
11,20 MA_CAS#		RAS#	DQ30
11,20 MA_RAS#		WE#	DQ31
11,20 MA_WE#		SA0	DQ32
	198	SA1	DQ33
	200	SCL	DQ34
	197	SDA	DQ35
	195	ODT0	DQ36
	114	ODT1	DQ37
	119	DM0	DQ38
	10	DM1	DQ39
	26	DM2	DQ40
	52	DM3	DQ41
	67	DM4	DQ42
	130	DM5	DQ43
	147	DM6	DQ44
	170	DM7	DQ45
	185	DQ46	DQ47
	154	DQ48	DQ49
	157	DQ50	DQ51
	158	DQ52	DQ53
	175	DQ54	DQ55
	158	DQ56	DQ57
	160	DQ58	DQ59
	174	DQ60	DQ61
	176	DQ62	DQ63
	179	DQ64	DQ65
	181	DQ66	DQ67
	189	DQ68	DQ69
	191	DQ70	DQ71
	180	DQ72	DQ73
	182	DQ74	DQ75
	192	DQ76	DQ77
	194	DQ78	DQ79

DDR\_DIMM\_200P  
12G02533200Y



GROUP1  
GROUP2  
SWAP



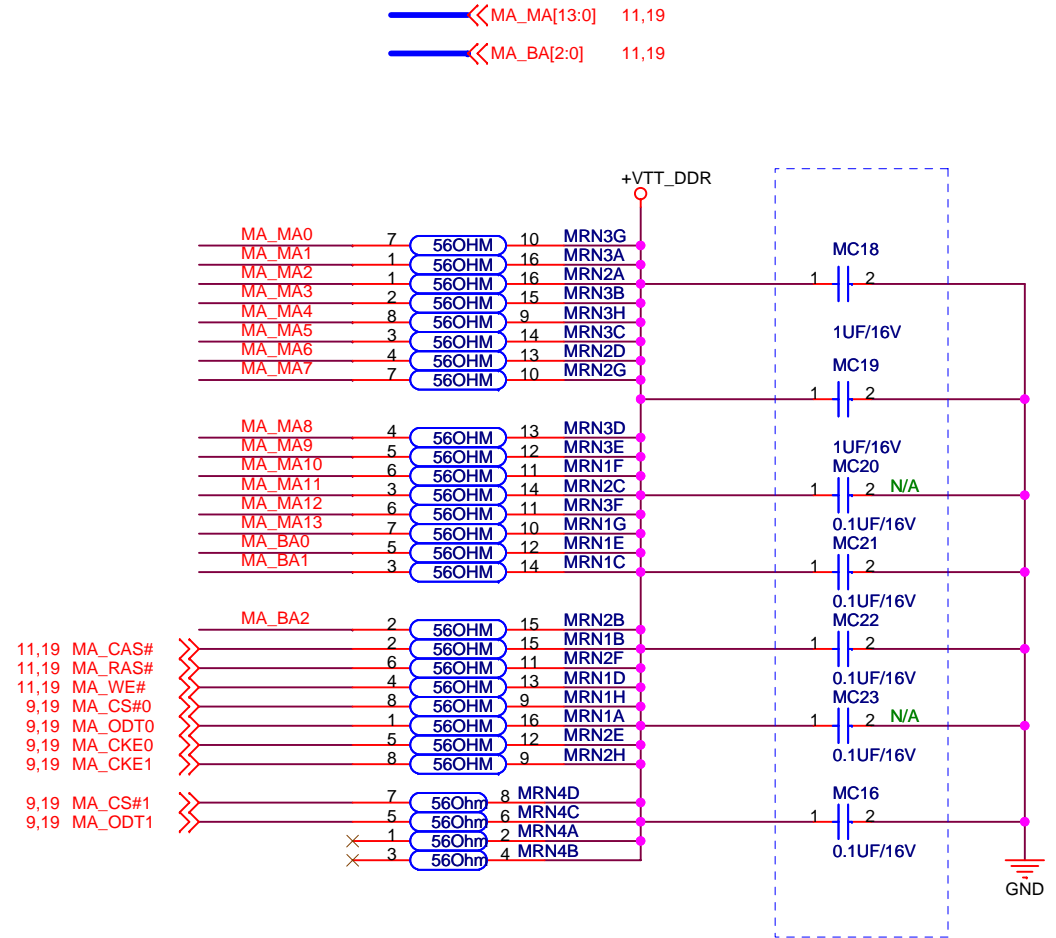
<Variant Name>

**ASUS** Title : **DDR2 SODIMM**

ASUSTek Computer INC. Engineer: **Jeff Li**

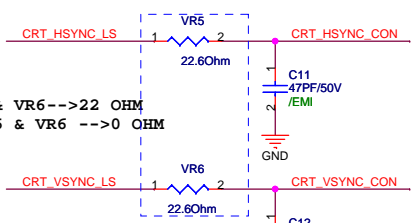
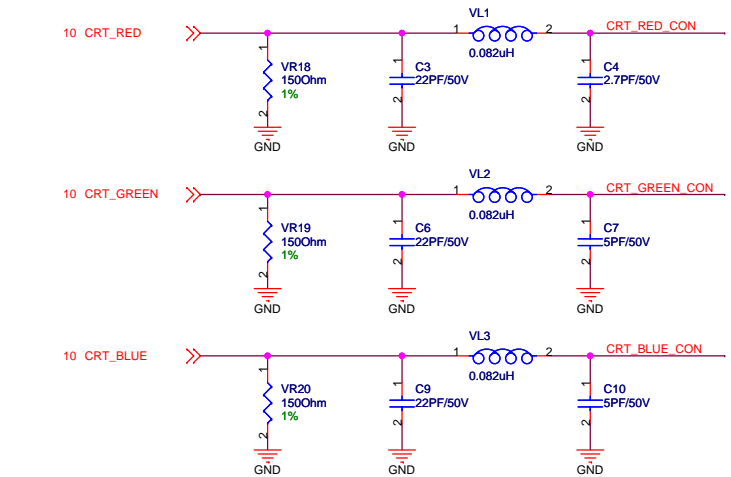
Size	Project Name	Rev
A3	<b>1000H_MB</b>	1.3G

Date: **Tuesday, February 10, 2009** Sheet **19** of **52**

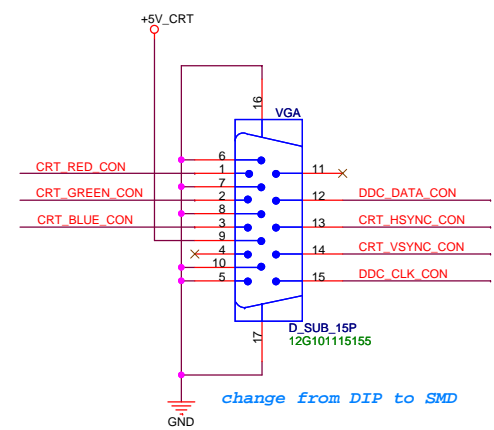
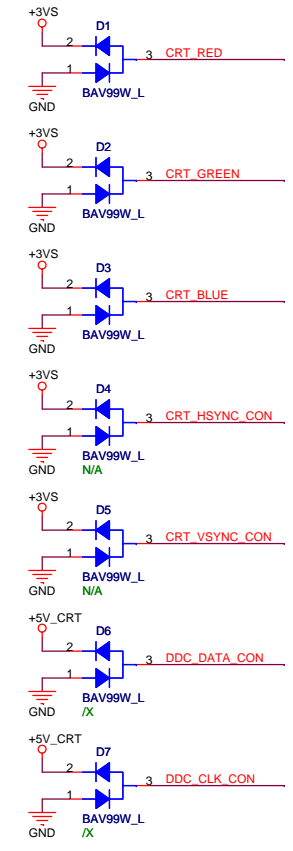
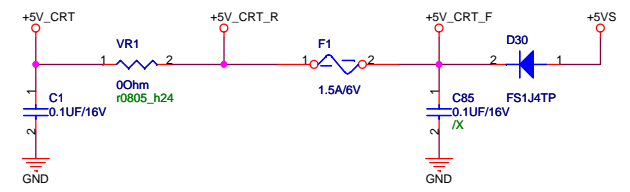
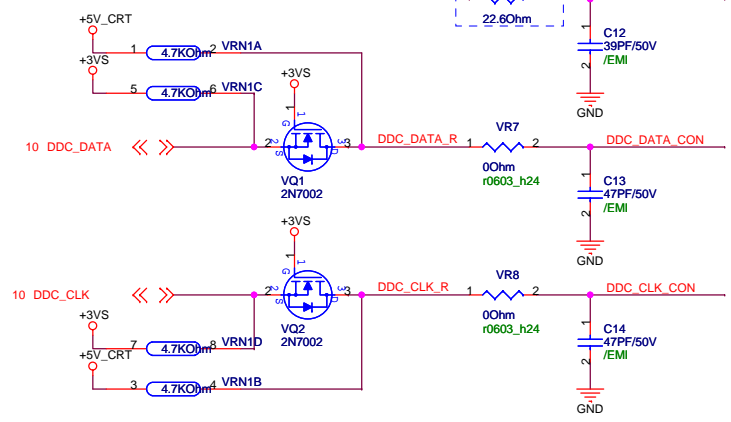


<Variant Name>

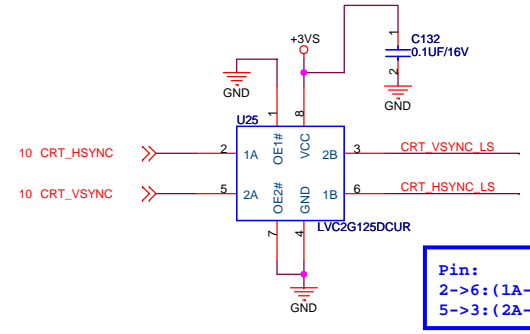
		<b>Title :</b> DDR2_Termination
ASUSTek Computer INC.		<b>Engineer:</b> Jeff Li
Size A4	Project Name <b>1000H_MB</b>	Rev 1.3G
Date: Tuesday, February 10, 2009	Sheet 20	of 52



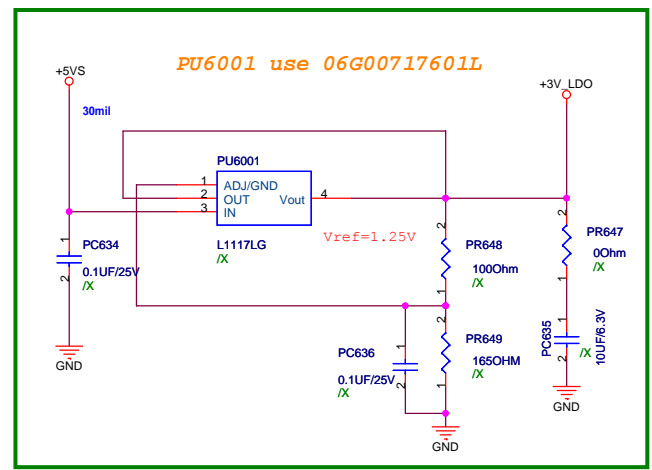
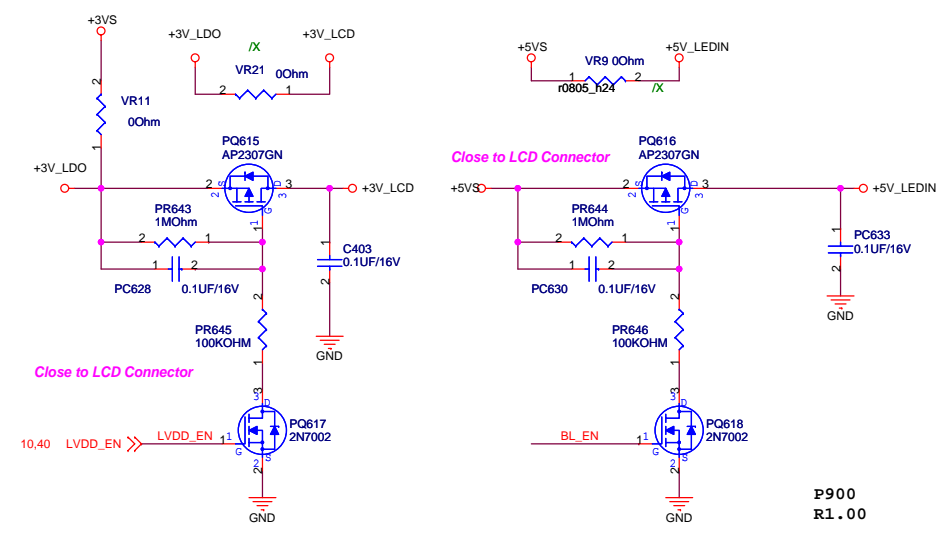
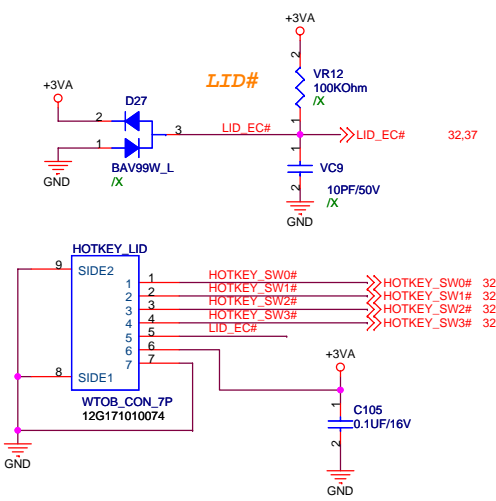
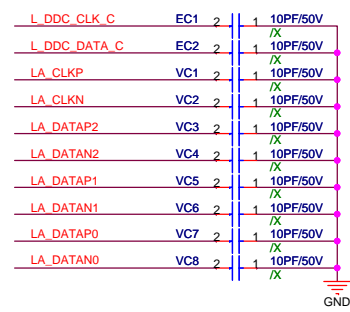
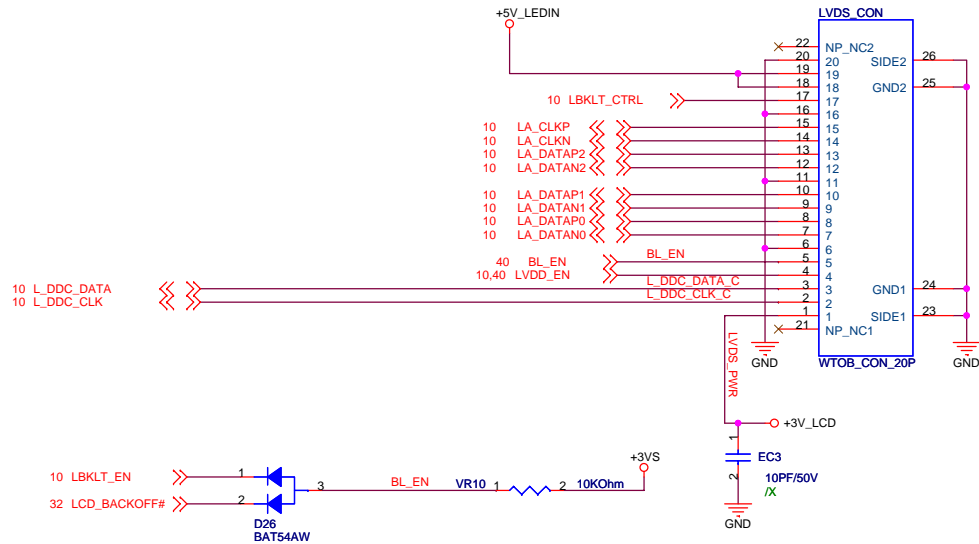
U25 : VR5 & VR6 --> 22 OHM  
 U25 /X : VR5 & VR6 --> 0 OHM

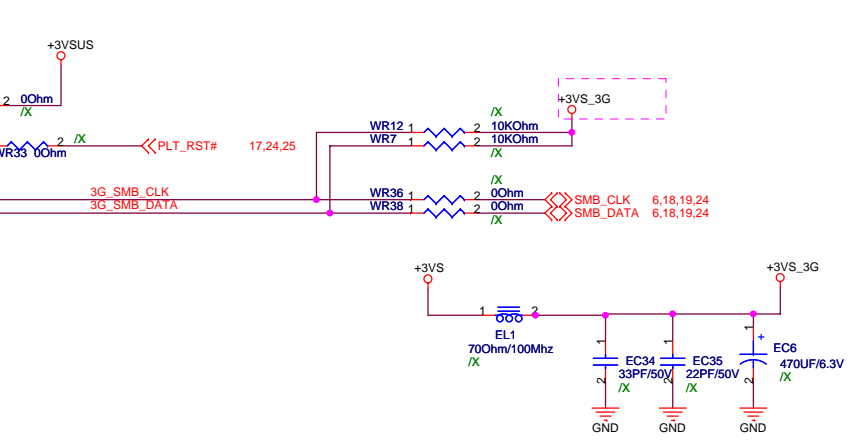
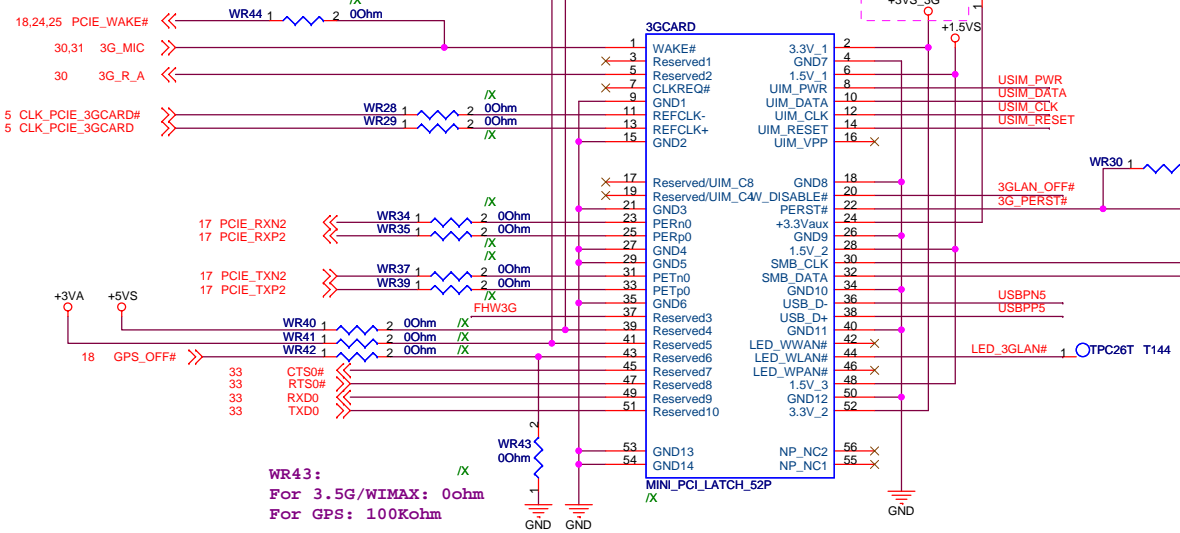
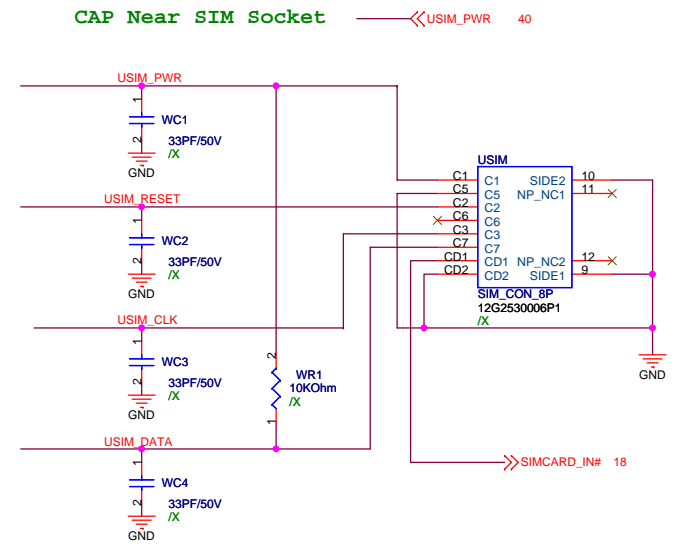
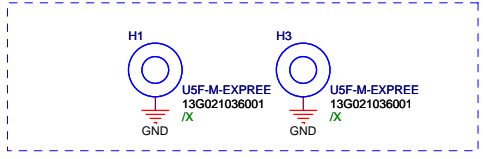
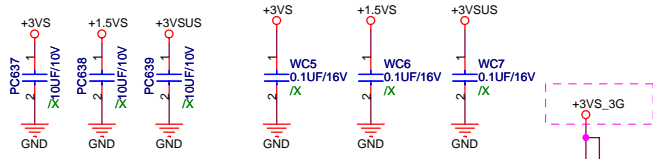
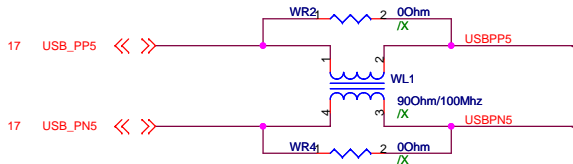


VGA use 12G10110015W & 12G10110015N

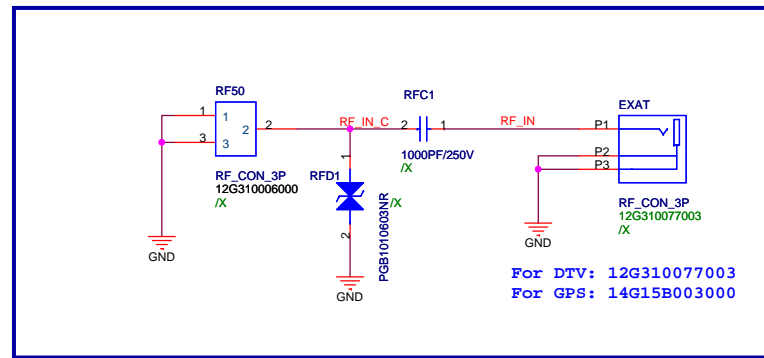


Pin:  
 2->6: (1A->1B)  
 5->3: (2A->2B)

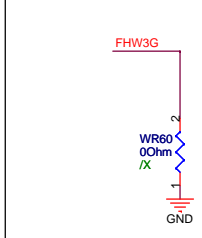




**External Antenna**



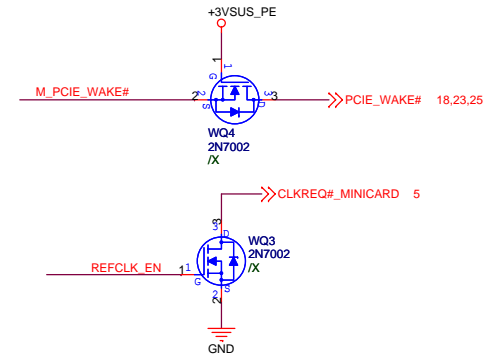
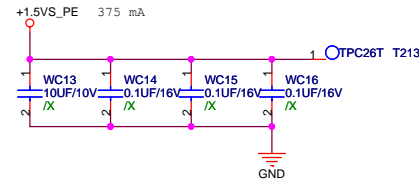
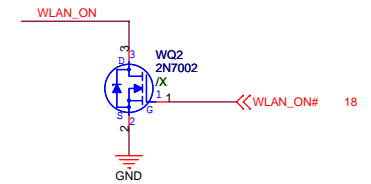
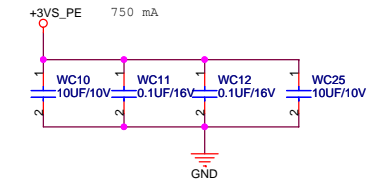
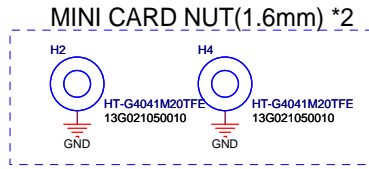
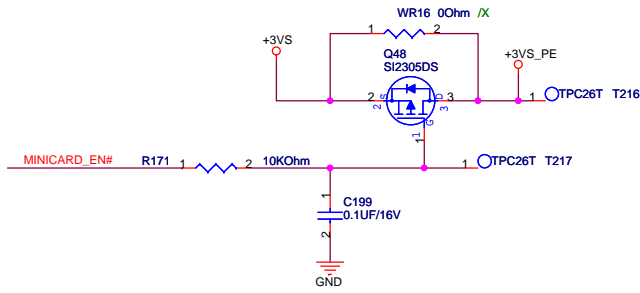
**For HuaWei 3G card**



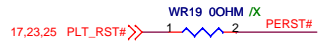
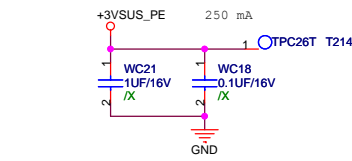
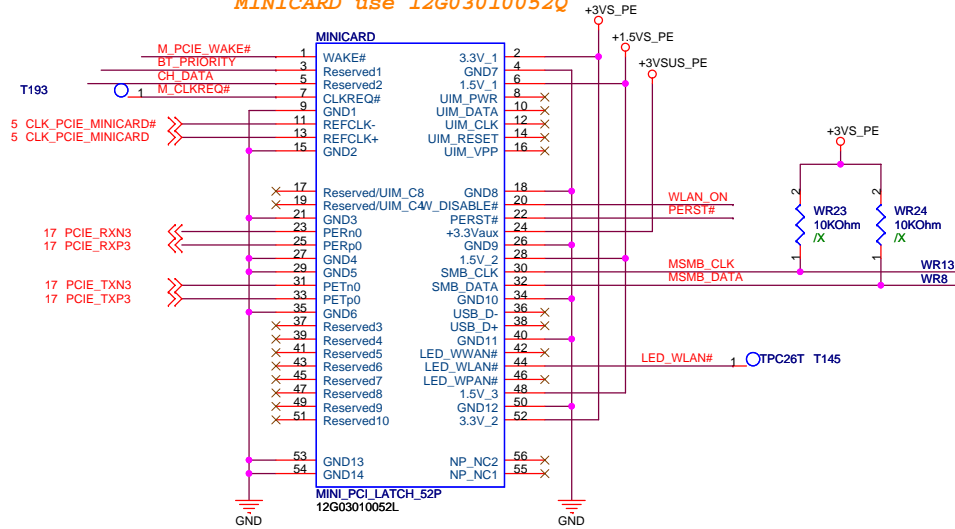
MINICARD use 12G03010052K

**3.5G Module & External Antenna**

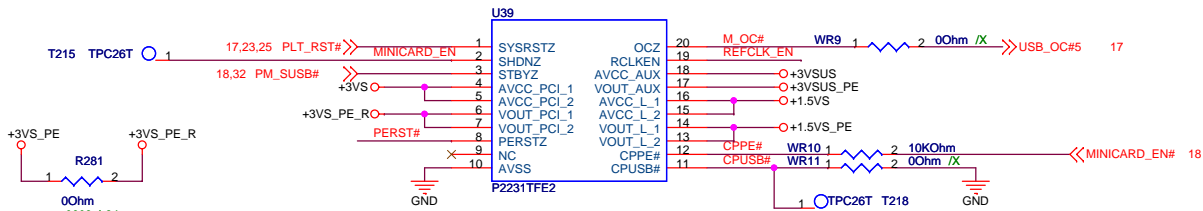
		<b>Title :</b>	
ASUSTek Computer INC.		Engineer: <b>Jeff Li</b>	
Size	Project Name	Rev	
A3	<b>1000H_MB</b>	1.3G	
Date: Tuesday, February 10, 2009	Sheet	23	of 52



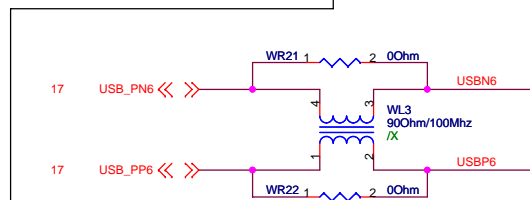
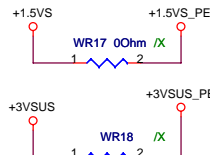
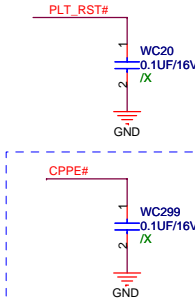
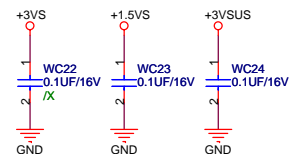
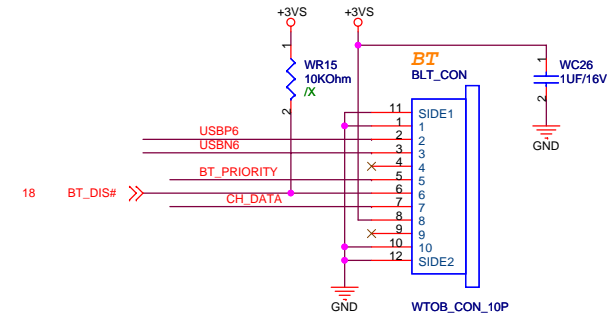
MINICARD use 12G03010052Q



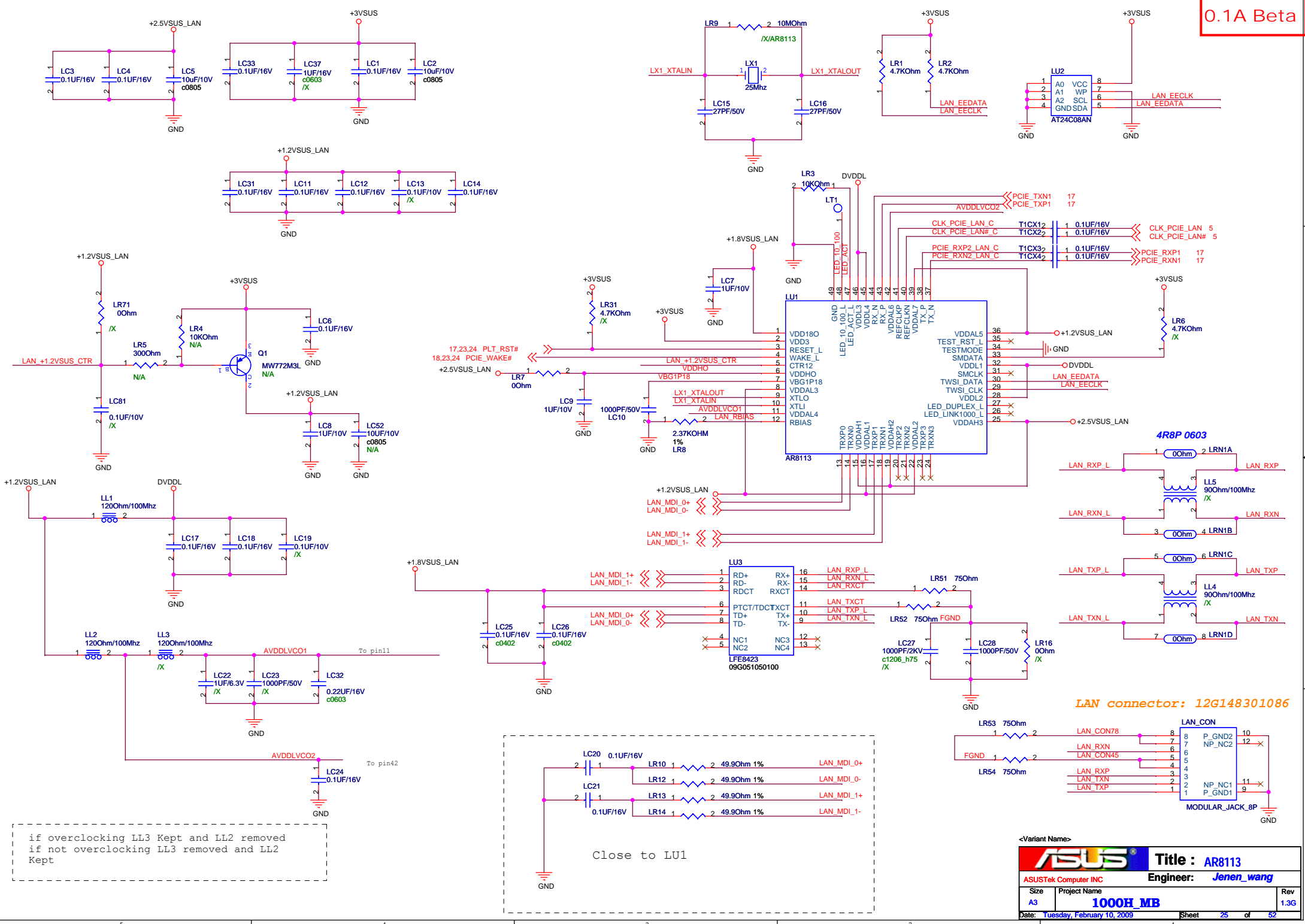
U39 use 06G030057013



BlueTooth







if overclocking LL3 Kept and LL2 removed  
 if not overclocking LL3 removed and LL2 Kept

Close to LU1

LAN connector: 12G148301086

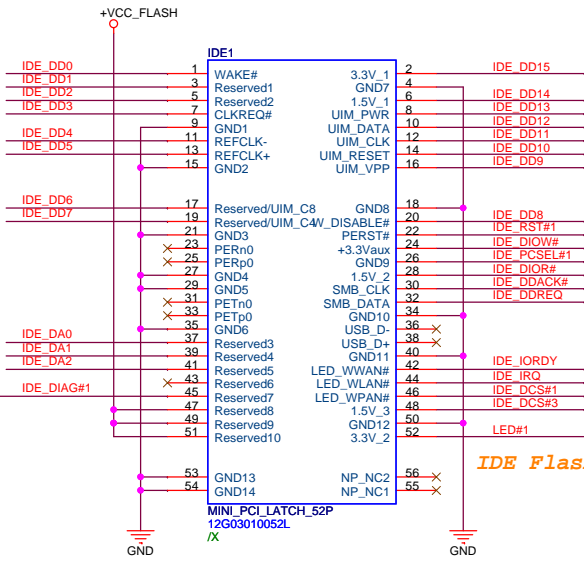
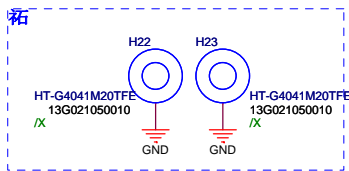
<Variant Name>

**ASUS** Title: AR8113

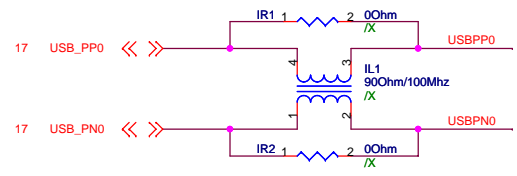
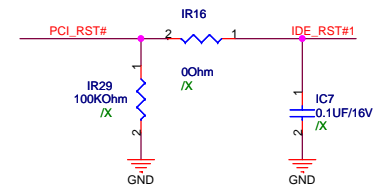
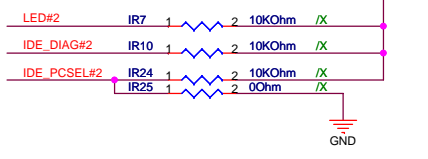
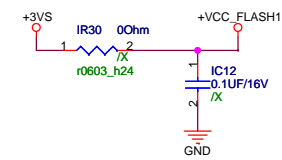
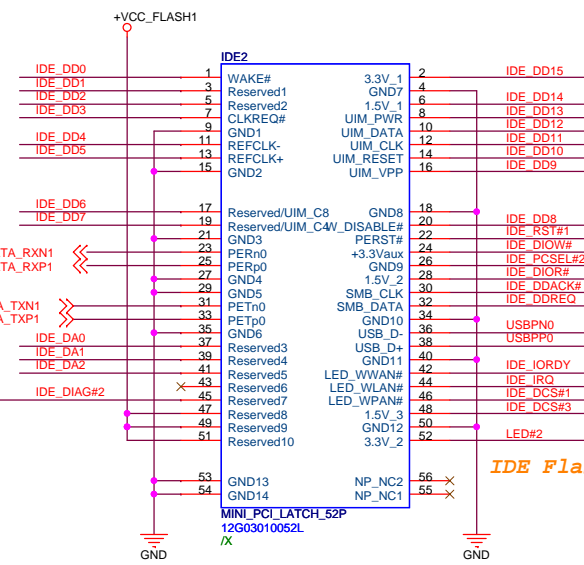
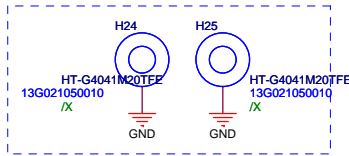
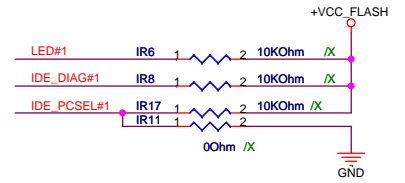
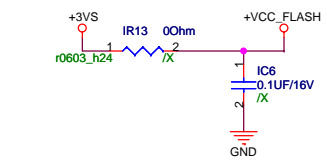
ASUSTek Computer INC Engineer: Jenen\_wang

Size	Project Name	Rev
A3	1000H_MB	1.3G

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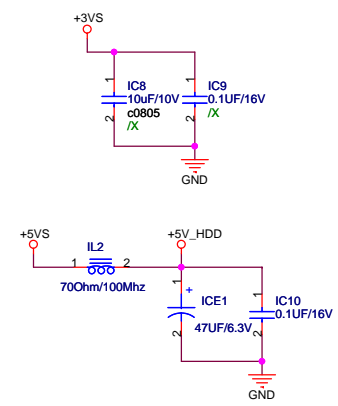
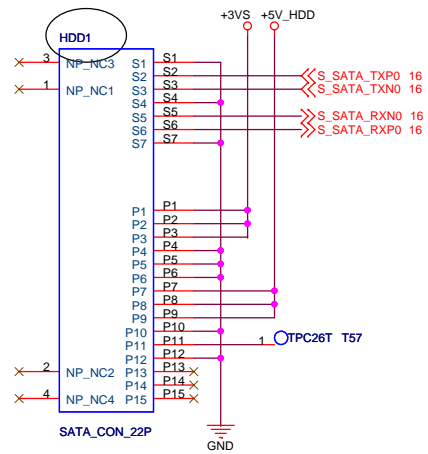


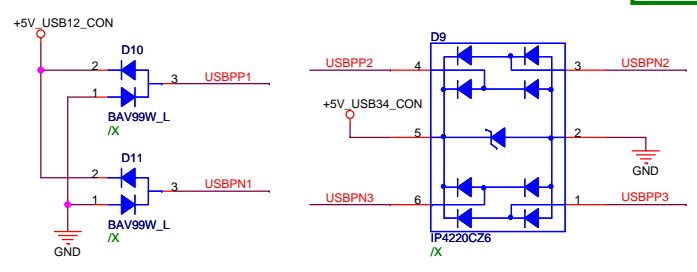
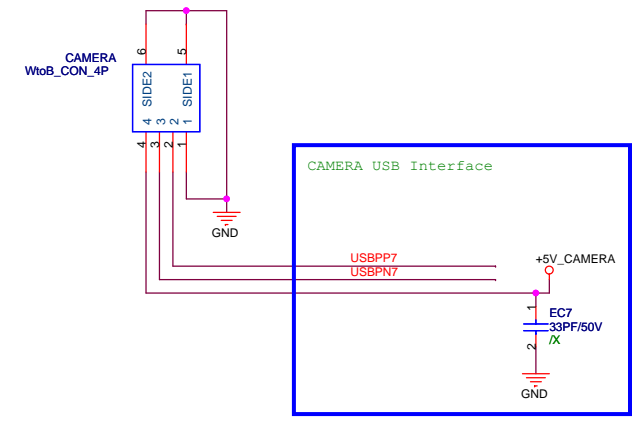
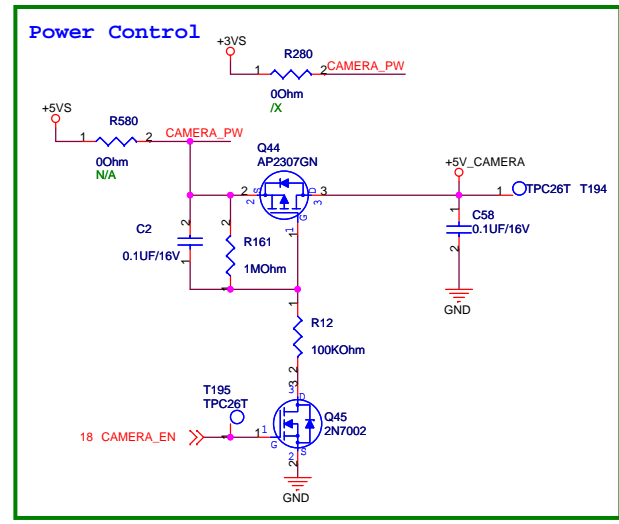
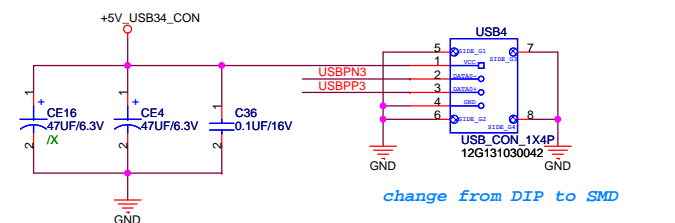
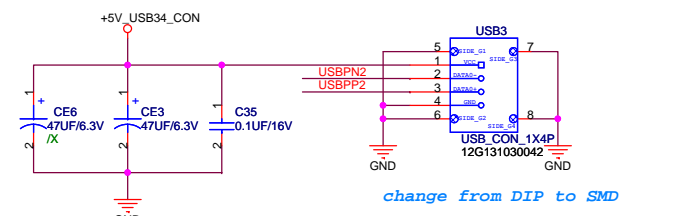
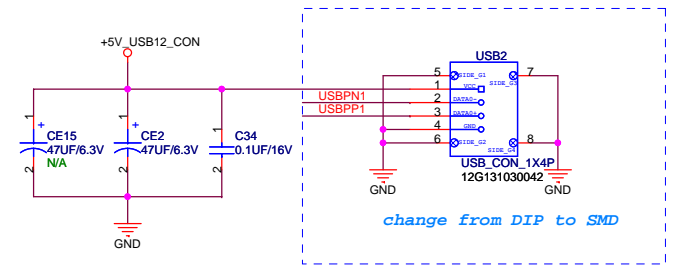
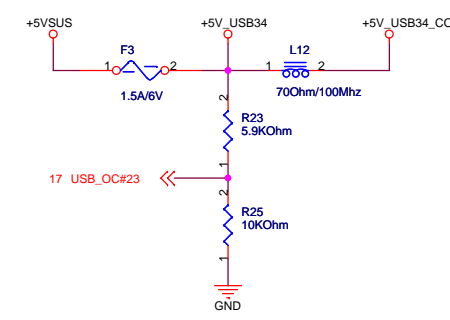
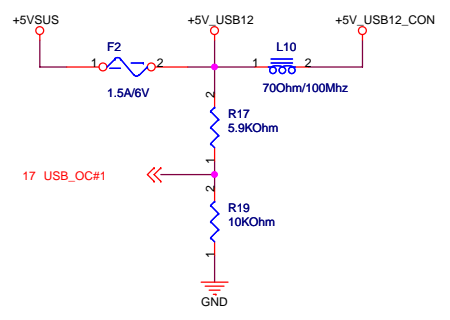
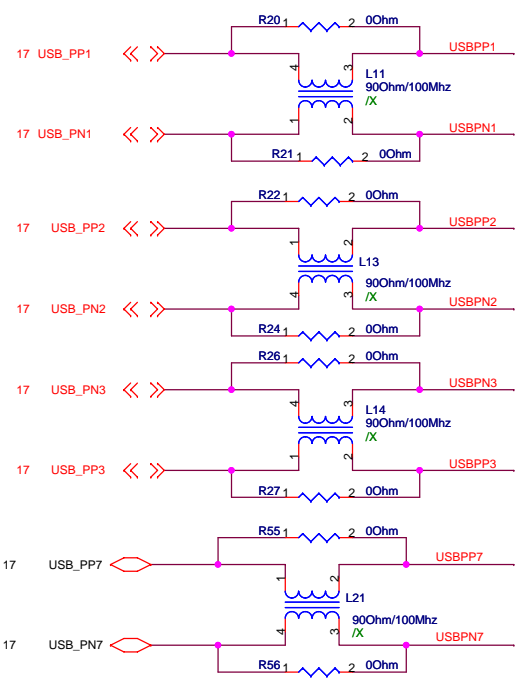
- << IDE\_DD[15:0] 16
- >> IDE\_DA[2:0] 16
- << IDE\_DDACK# 16
- >> IDE\_DDREQ 16
- << IDE\_DIOR# 16
- >> IDE\_DIOR# 16
- << IDE\_DIOV# 16
- >> IDE\_IORDY 16
- << IDE\_DCS#1 16
- >> IDE\_DCS#3 16
- >> IDE\_IRQ 16
- << PCI\_RST# 17,32,33

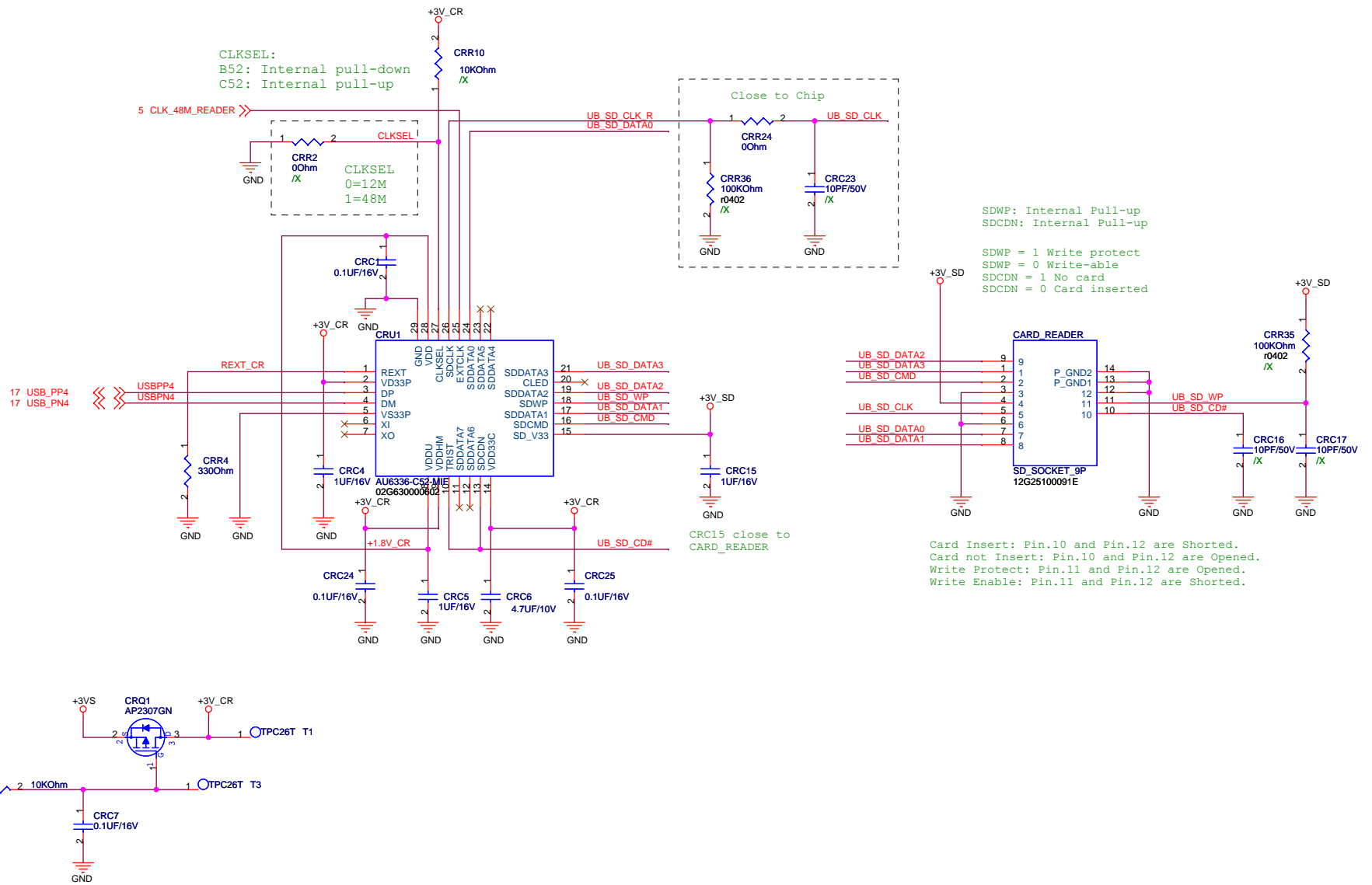


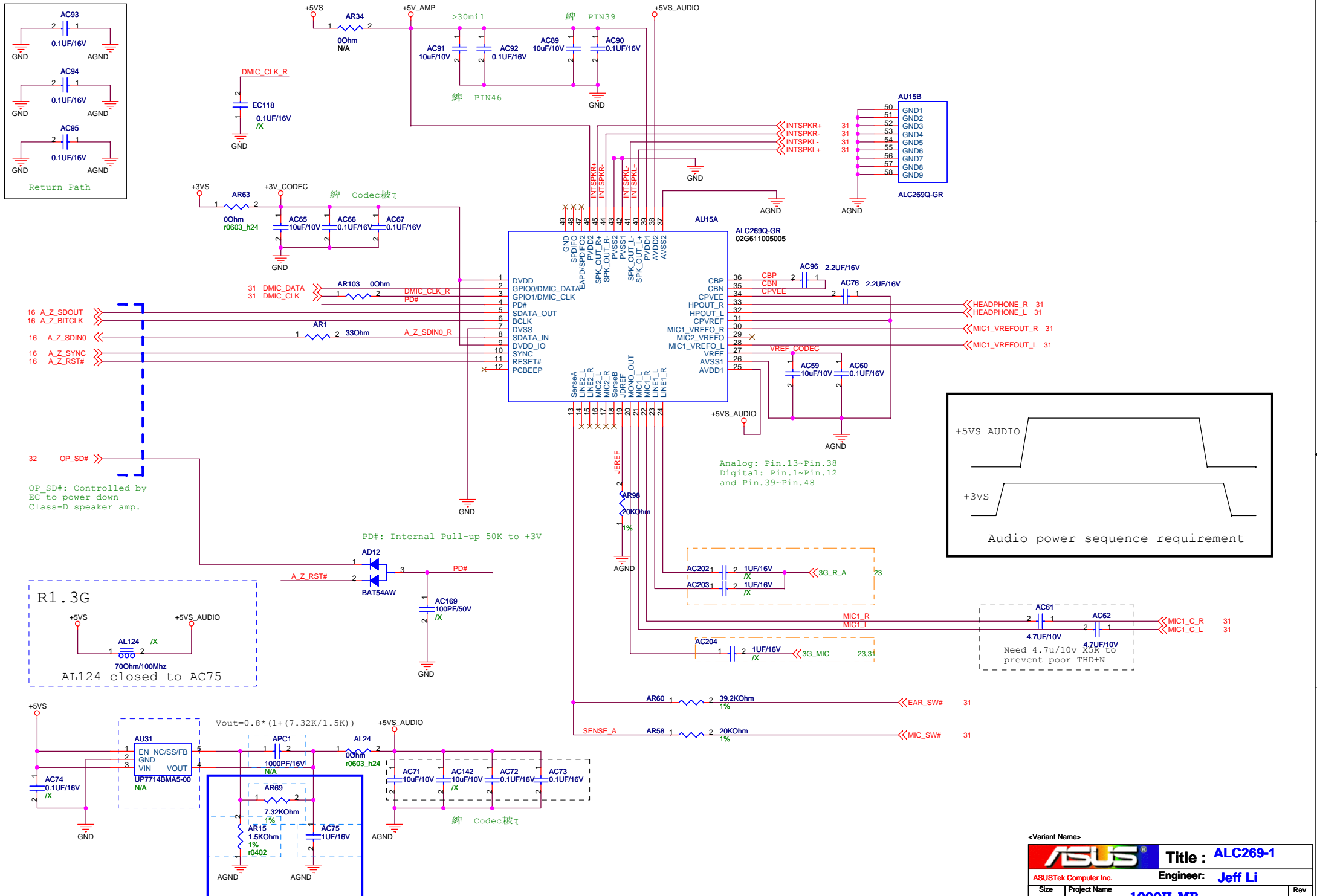
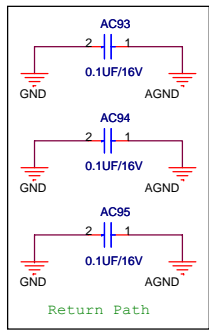
**Naming Rule:**  
 IC: IU?  
 R: IR?  
 C: IC?  
 L: IL?

# SATA HDD Connector



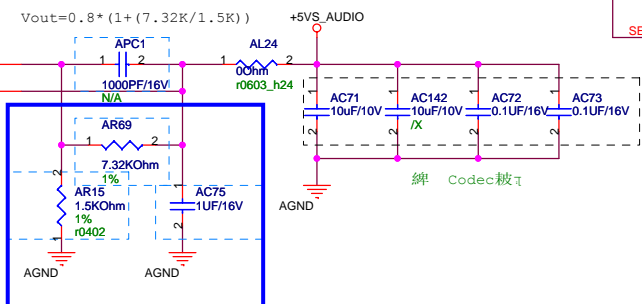
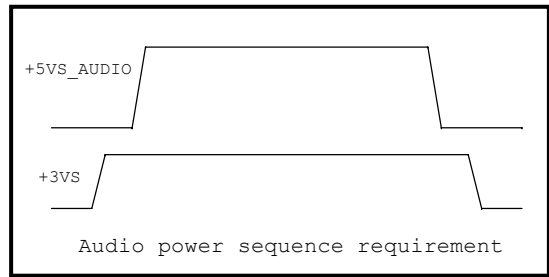
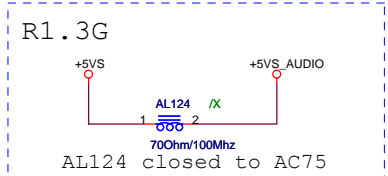


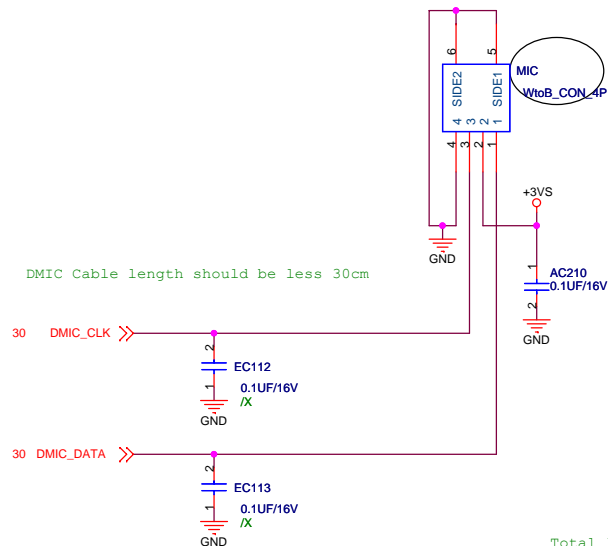




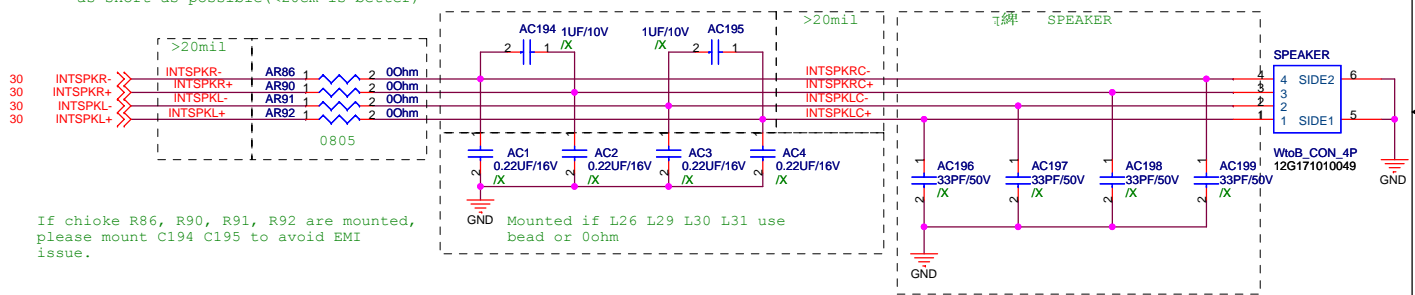
OP\_SD#: Controlled by EC to power down Class-D speaker amp.

PD#: Internal Pull-up 50K to +3V

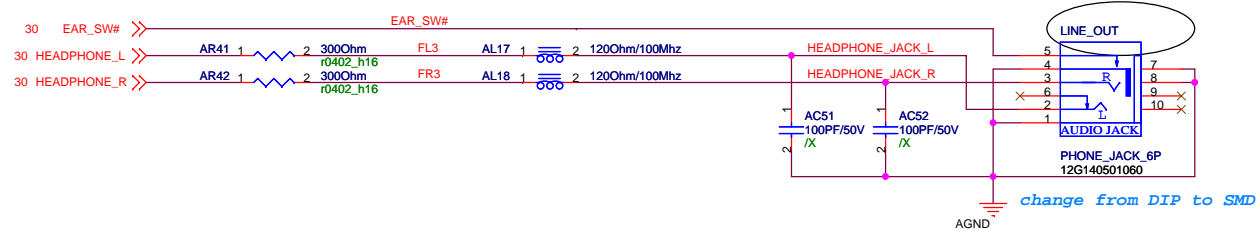




Total length from speakerR+- L+- (pin40 41 44 45) to internal speaker please as short as possible (<20cm is better)

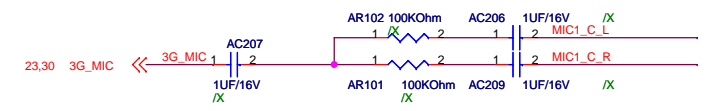
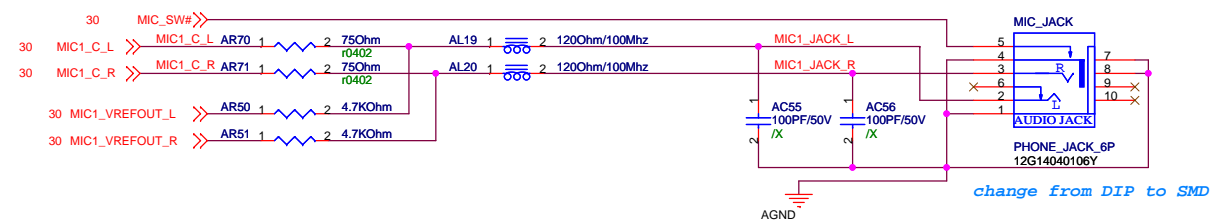


**LINE\_OUT use 12G140501060**



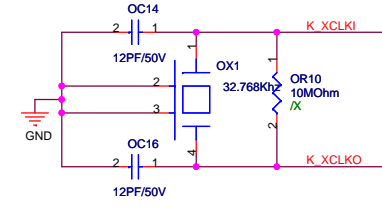
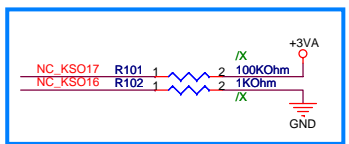
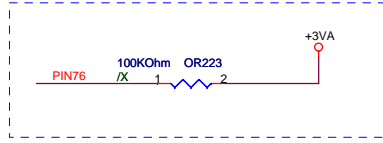
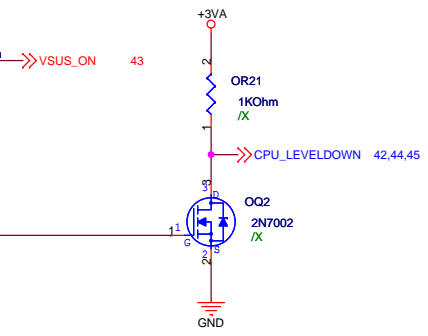
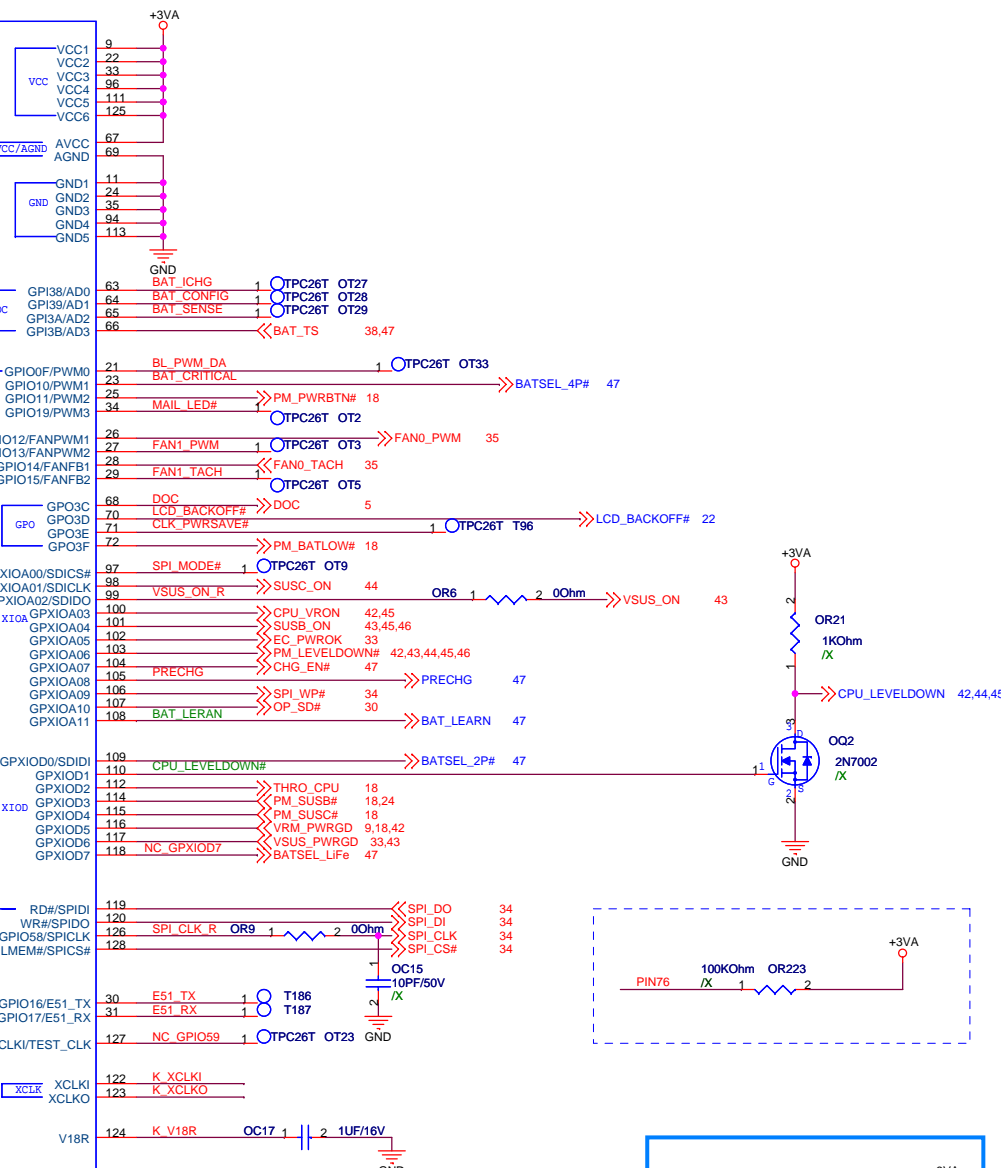
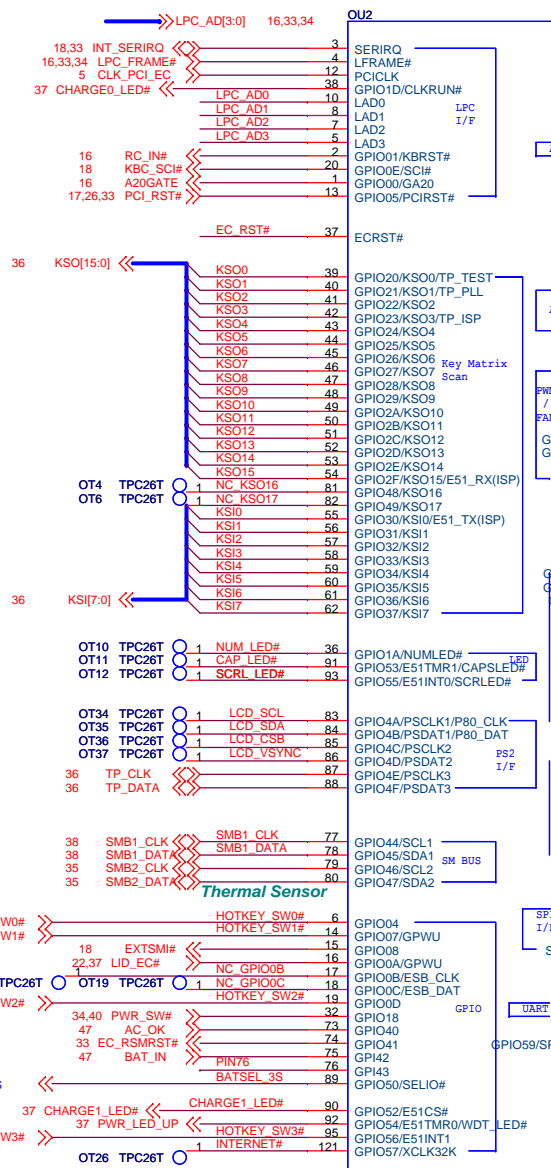
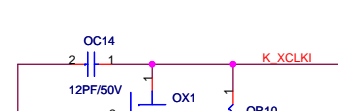
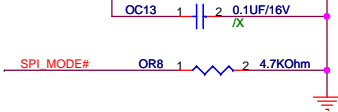
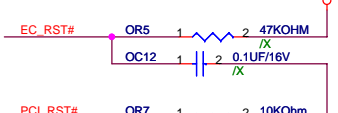
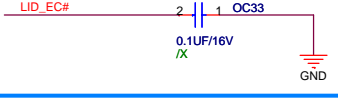
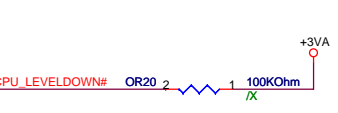
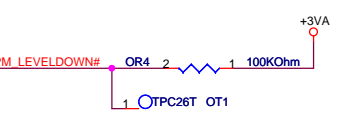
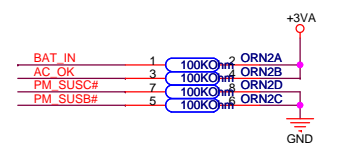
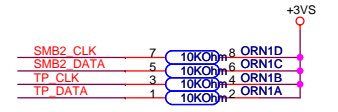
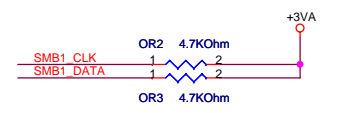
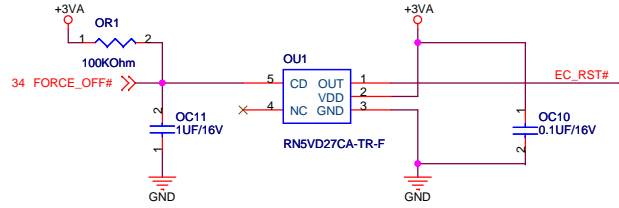
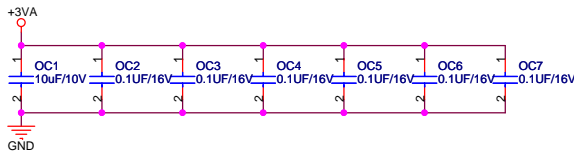
R70 and R71: If don't need retasking function, change to 1K.

**MIC\_JACK use 12G14040106Y**



<Variant Name>

<b>ASUS</b>		<b>Title : ALC269-2</b>	
ASUSTek Computer Inc.		Engineer: Jeff Li	
Size A3	Project Name	<b>1000H_MB</b>	Rev 1.3G
Date: Tuesday, February 10, 2009	Sheet	31	of 47



<Variant Name>

**Title : EC\_ENE KB3310**

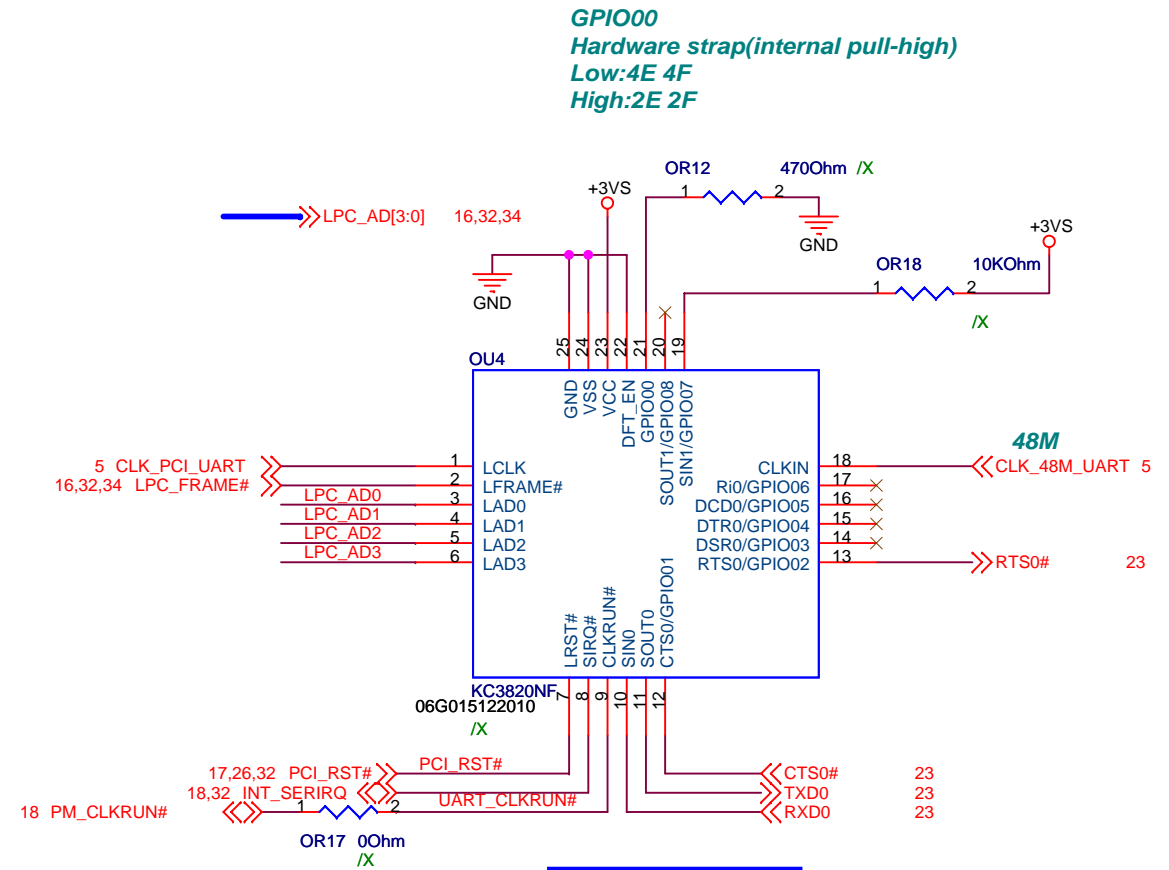
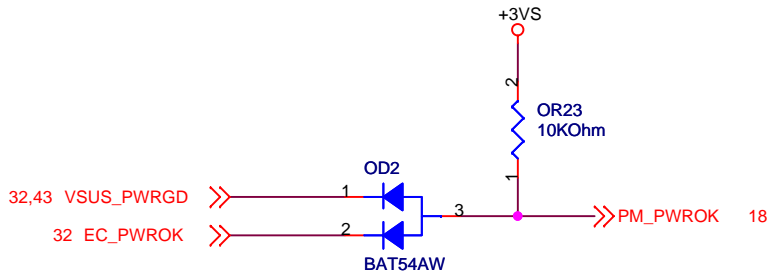
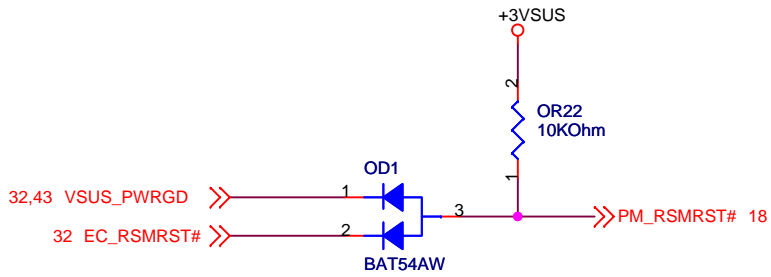
ASUSTek Computer INC. **Engineer: Jeff Li**

Size	Project Name	Rev
A3	1000H_MB	1.3G

Date: Tuesday, February 10, 2009 Sheet 32 of 47

KB3310QF  
N/A  
02G890000700

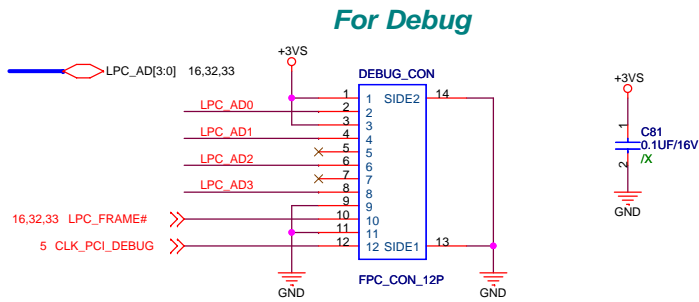
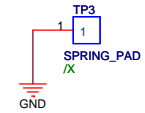
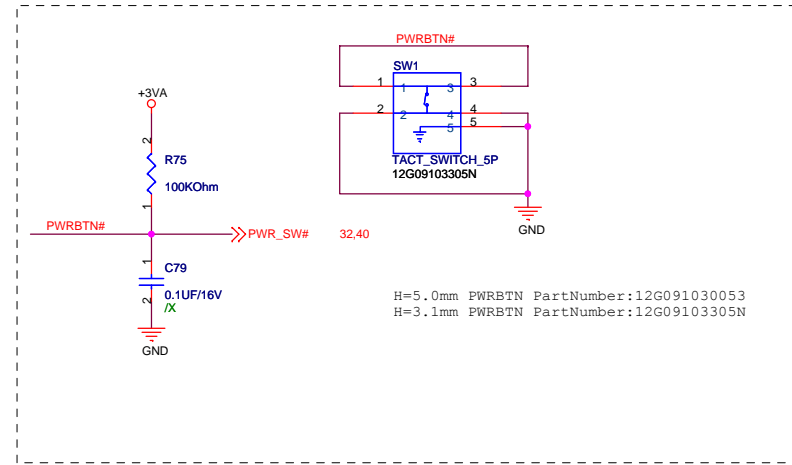
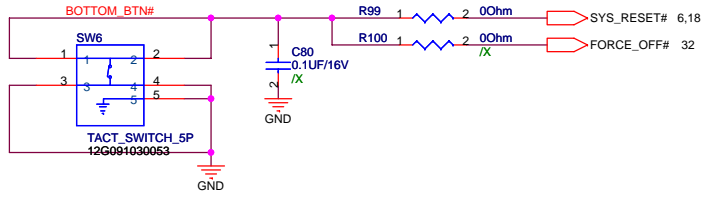




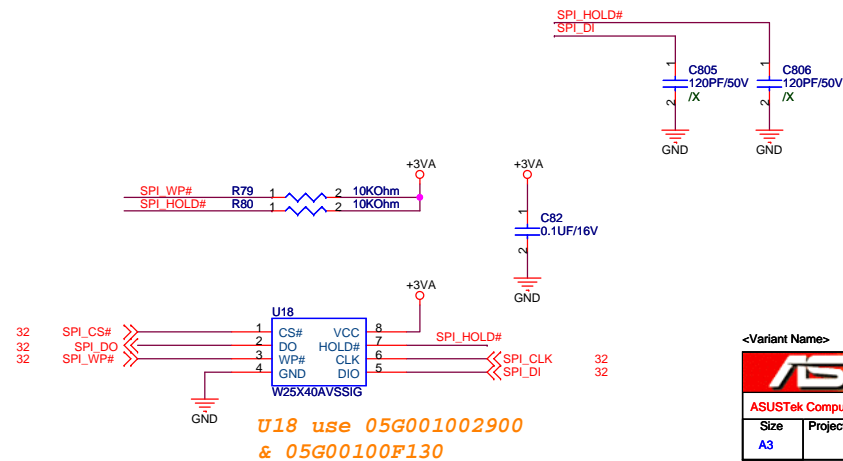
UART Control  
IC for using  
GPS module due  
to no UART on  
ENE EC

<Variant Name>

<b>ASUS</b>		<b>Title : EC_UART_KC3820</b>	
ASUSTek Computer INC.		Engineer: <i>Jeff Li</i>	
Size A4	Project Name <b>1000H_MB</b>	Rev 1.3G	
Date: <b>Tuesday, February 10, 2009</b>		Sheet <b>33</b> of <b>47</b>	

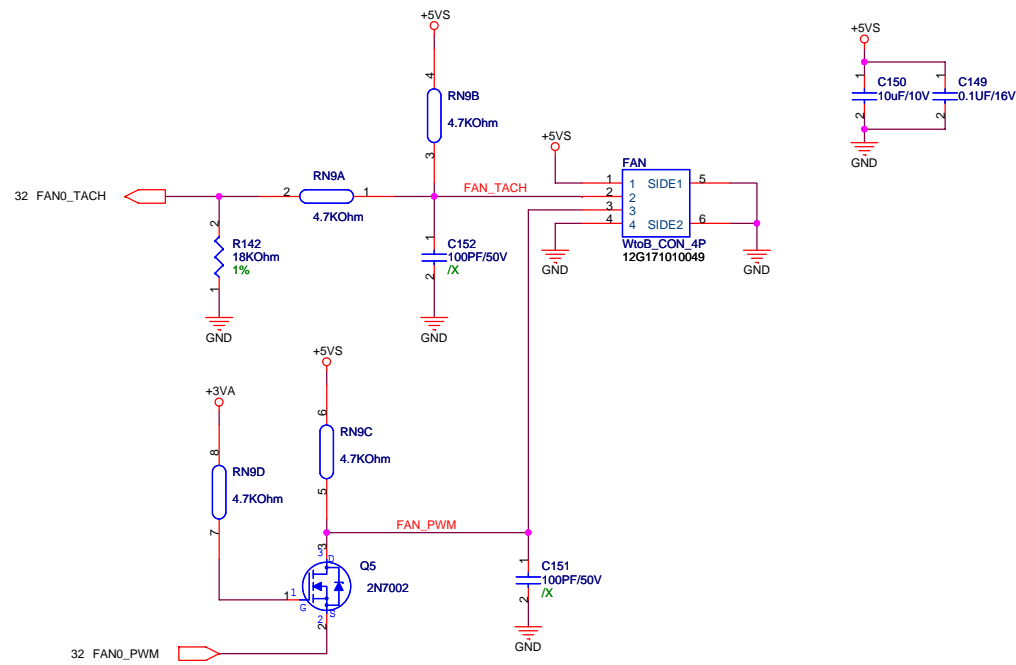
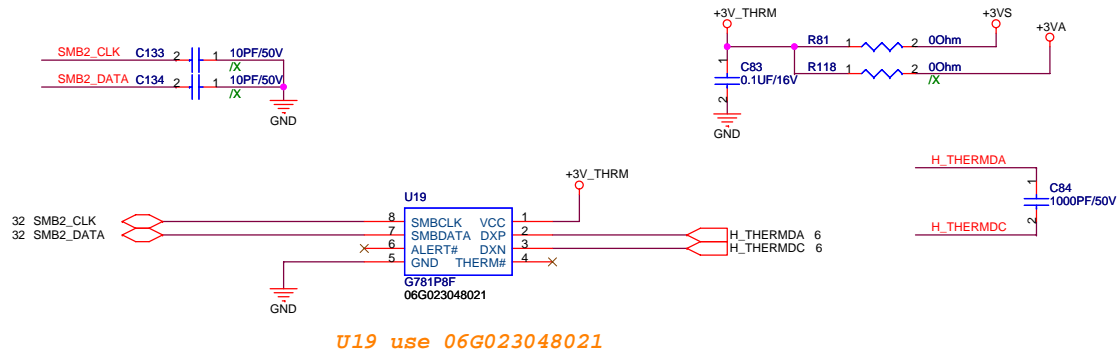


Debug Card cable use Z96 Touch Pad cable, P/N:  
14G124110126, 14G124110120, 14G124110121  
14G124110124, 14G124110125



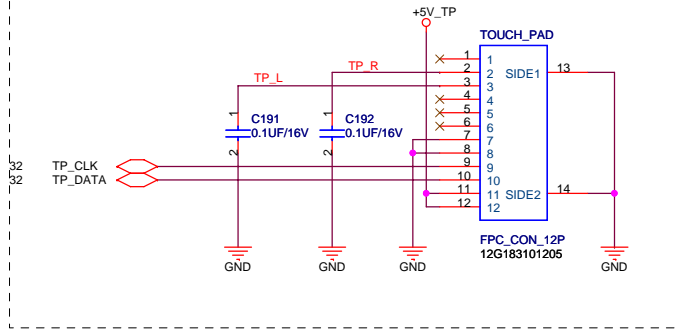
<Variant Name>

		Title : Switch_SPI ROM_Debug	
ASUSTek Computer INC.		Engineer: Jeff Li	
Size	Project Name		Rev
A3	1000H_MB		1.3G
Date:	Tuesday, February 10, 2009	Sheet	34 of 52



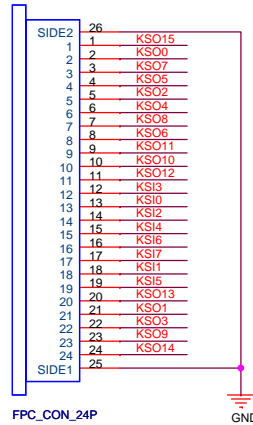
### For Touch-Pad

P900 R1.0G

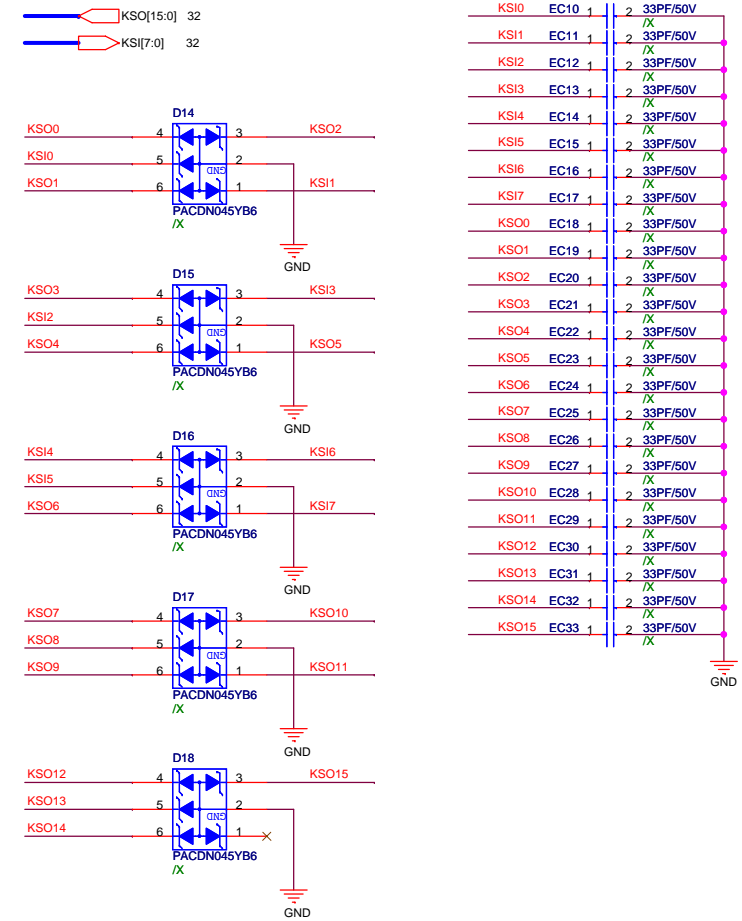
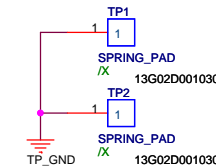
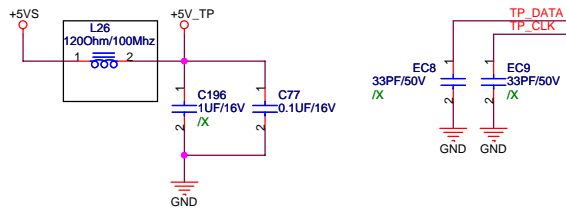
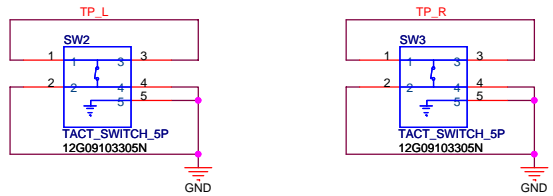


### For Keyboard Connector

KB



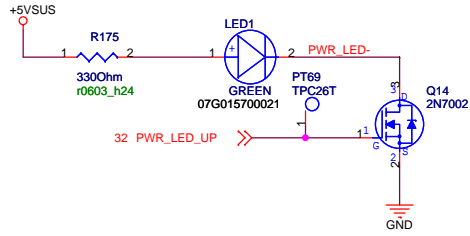
SW2, SW3 use 12G09103305N



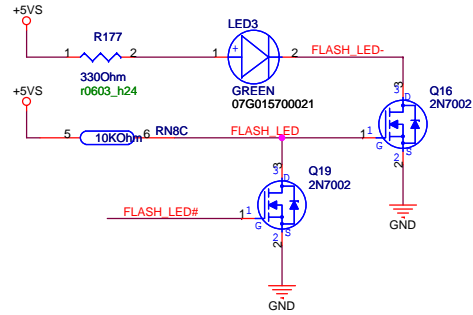
<Variant Name>

		<b>Title : KB_Touch Pad</b>	
ASUSTek Computer INC.		Engineer: <b>Jeff Li</b>	
Size	Project Name	Rev	
A3	<b>1000H_MB</b>	1.3G	
Date: Tuesday, February 10, 2009	Sheet	26	of 52

for POWER LED

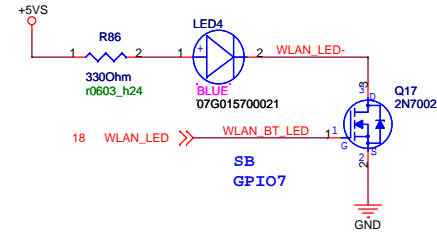


for FLASH LED

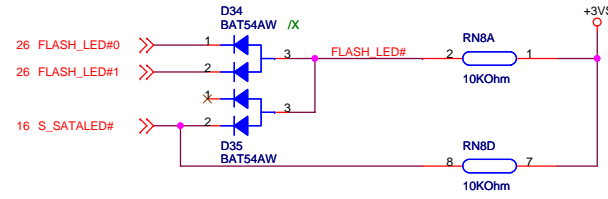
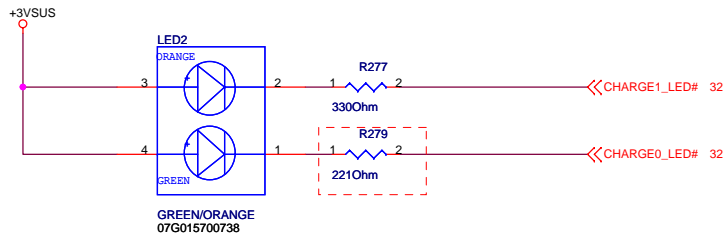


for WLAN/BlueTooth LED

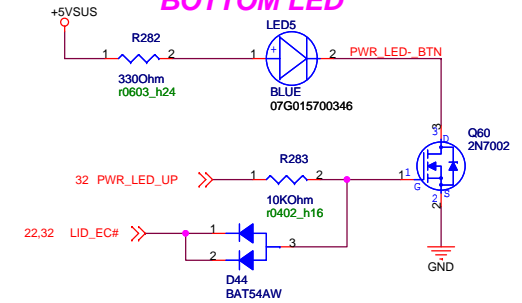
R86 use 4.7K OHm 10G213472003030



for CHARGE LED



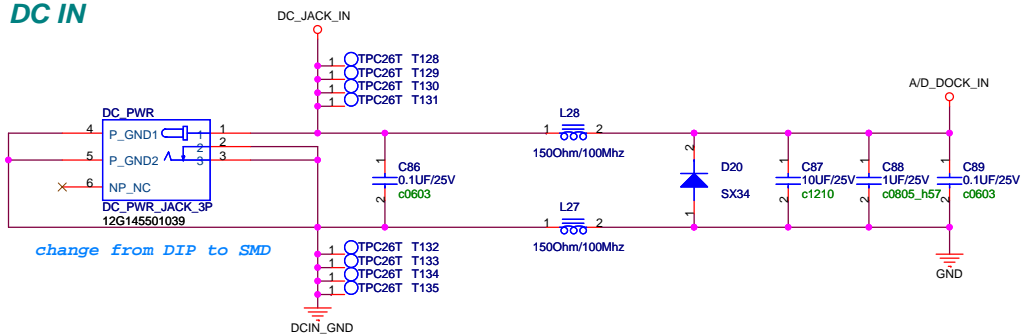
for POWER BOTTOM LED



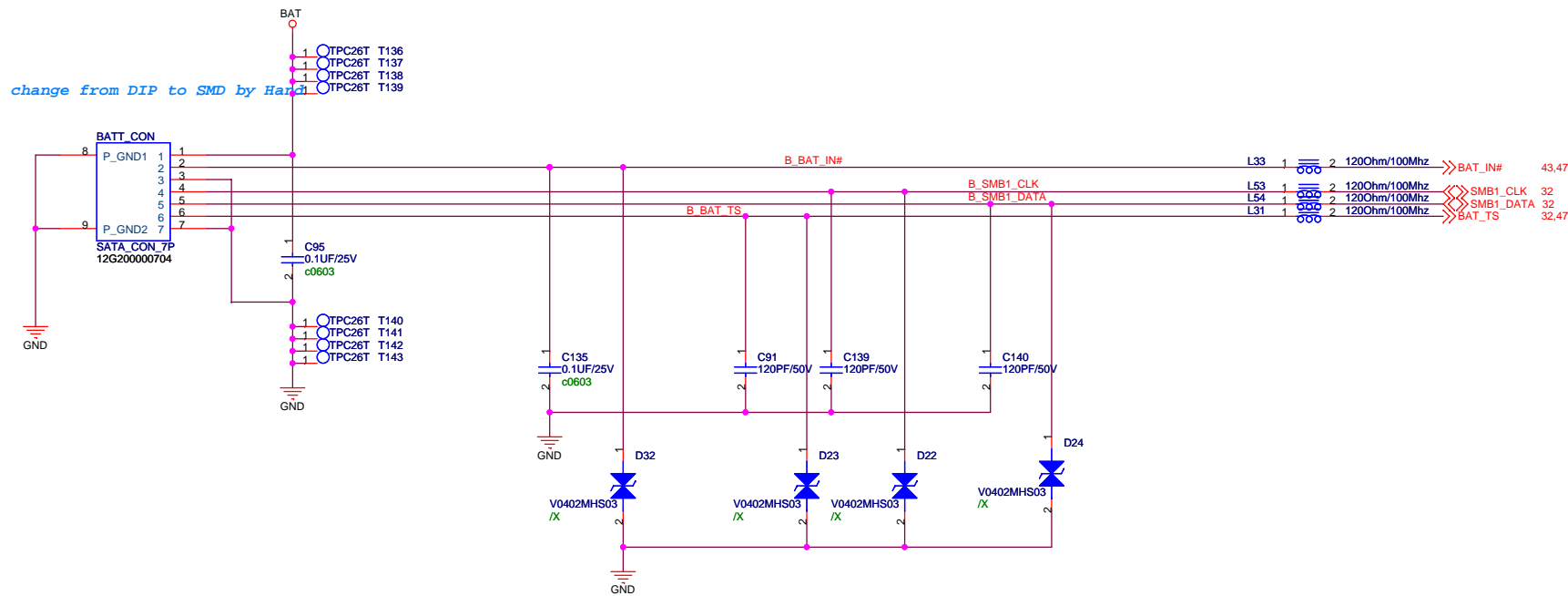
<Variant Name>

		Title : LED	
ASUSTek Computer INC.		Engineer: Keil_Huang	
Size	Project Name		Rev
A3	1000H_MB		1.3G
Date: Tuesday, February 10, 2009	Sheet	37	of 47

### DC IN

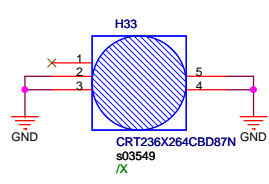
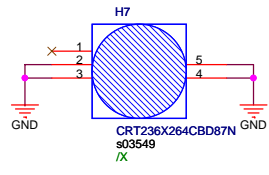
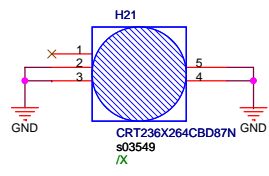
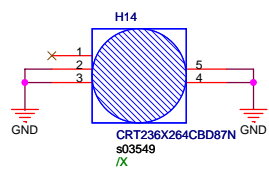
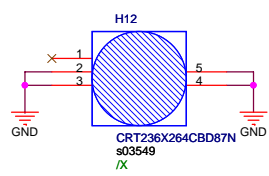
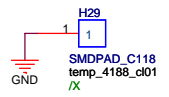
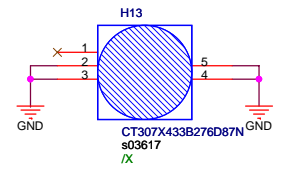
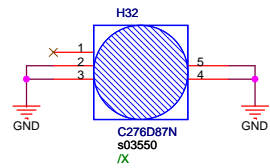
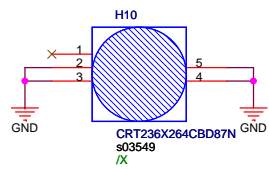
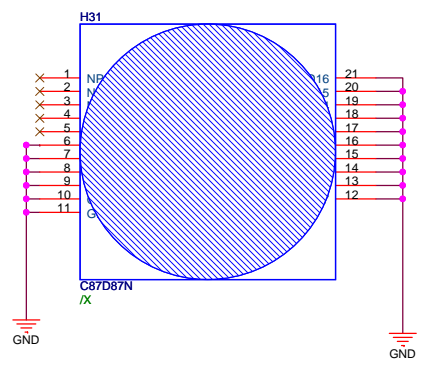
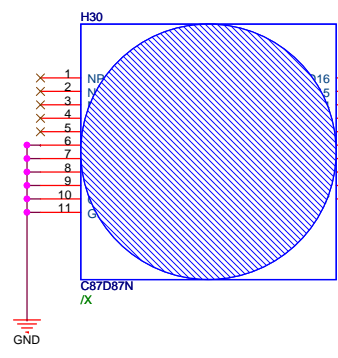
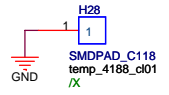
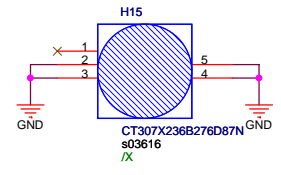
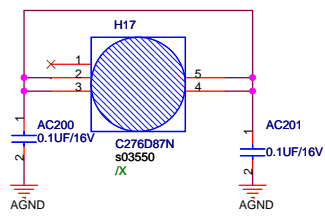
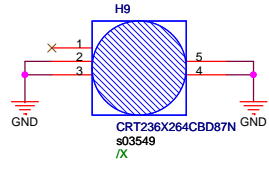
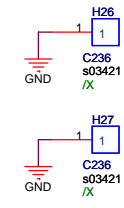
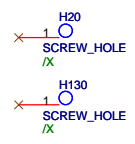
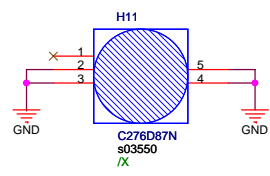
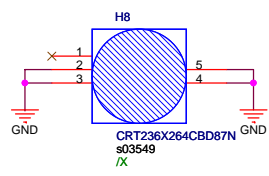


### BAT IN



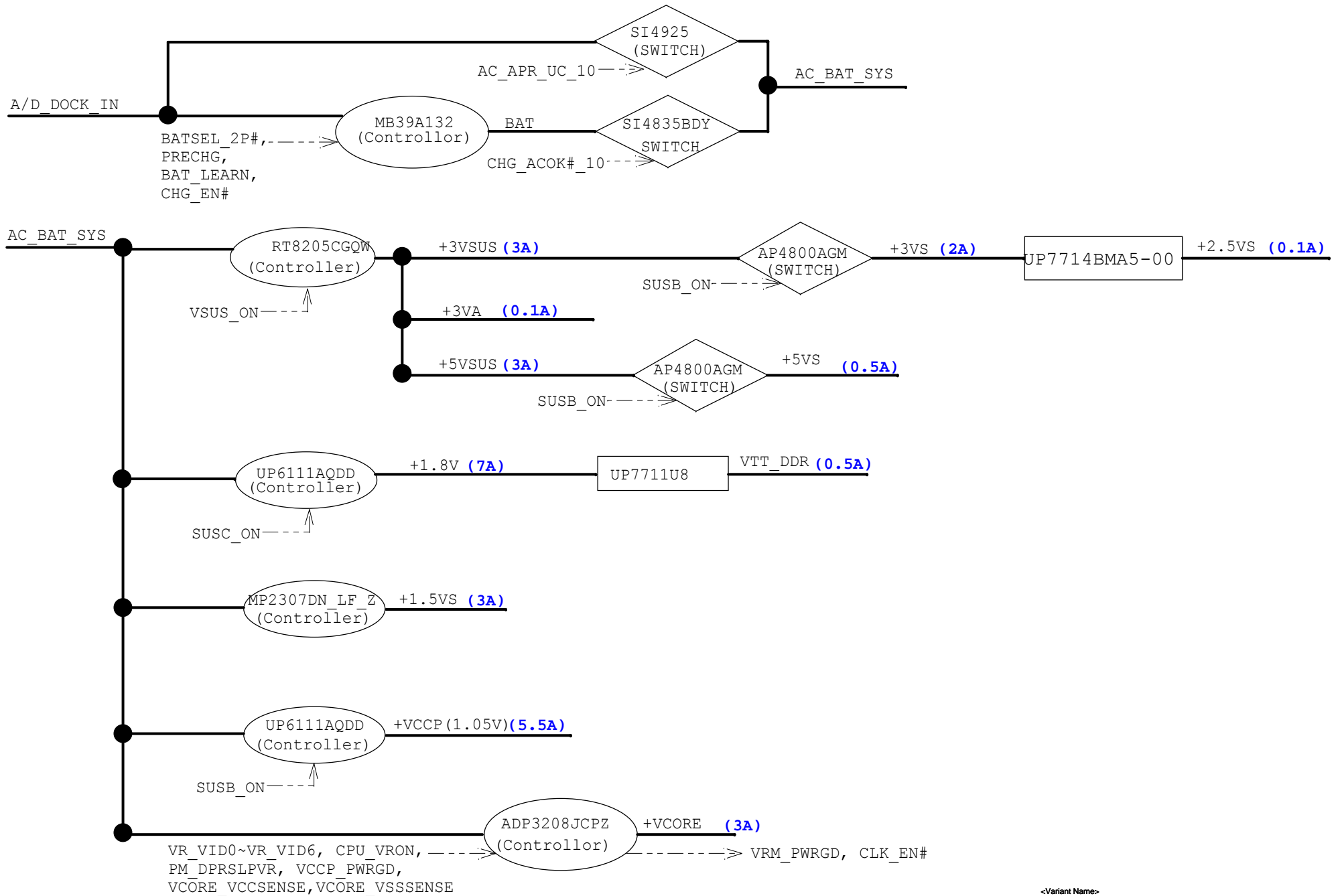
<Variant Name>

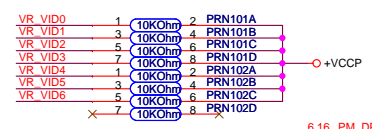
<b>ASUS</b>		<b>Title : PWR Jack</b>	
ASUSTek Computer INC.		Engineer: <b>Jeff Li</b>	
Size A3	Project Name <b>1000H_MB</b>	Rev 1.3G	
Date: <b>Tuesday, February 10, 2009</b>	Sheet	38	of 52











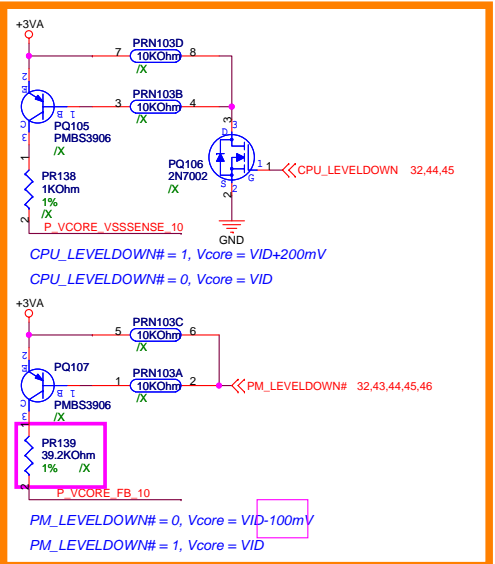
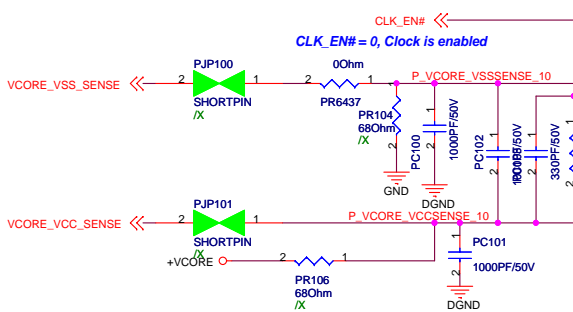
6.16 PM\_DPRSTP# >>>  
**STP\_CPU# = 0, CPU is in Deep Sleep Mode**

9.18 PM\_DPRSLPVR >>>  
**PM\_DPRSLPVR = 1, CPU Deeper Sleep Mode is enabled**

32.45 CPU\_VRON >>>  
**CPU\_VRON = 1, Vcore Reglator Enabled**

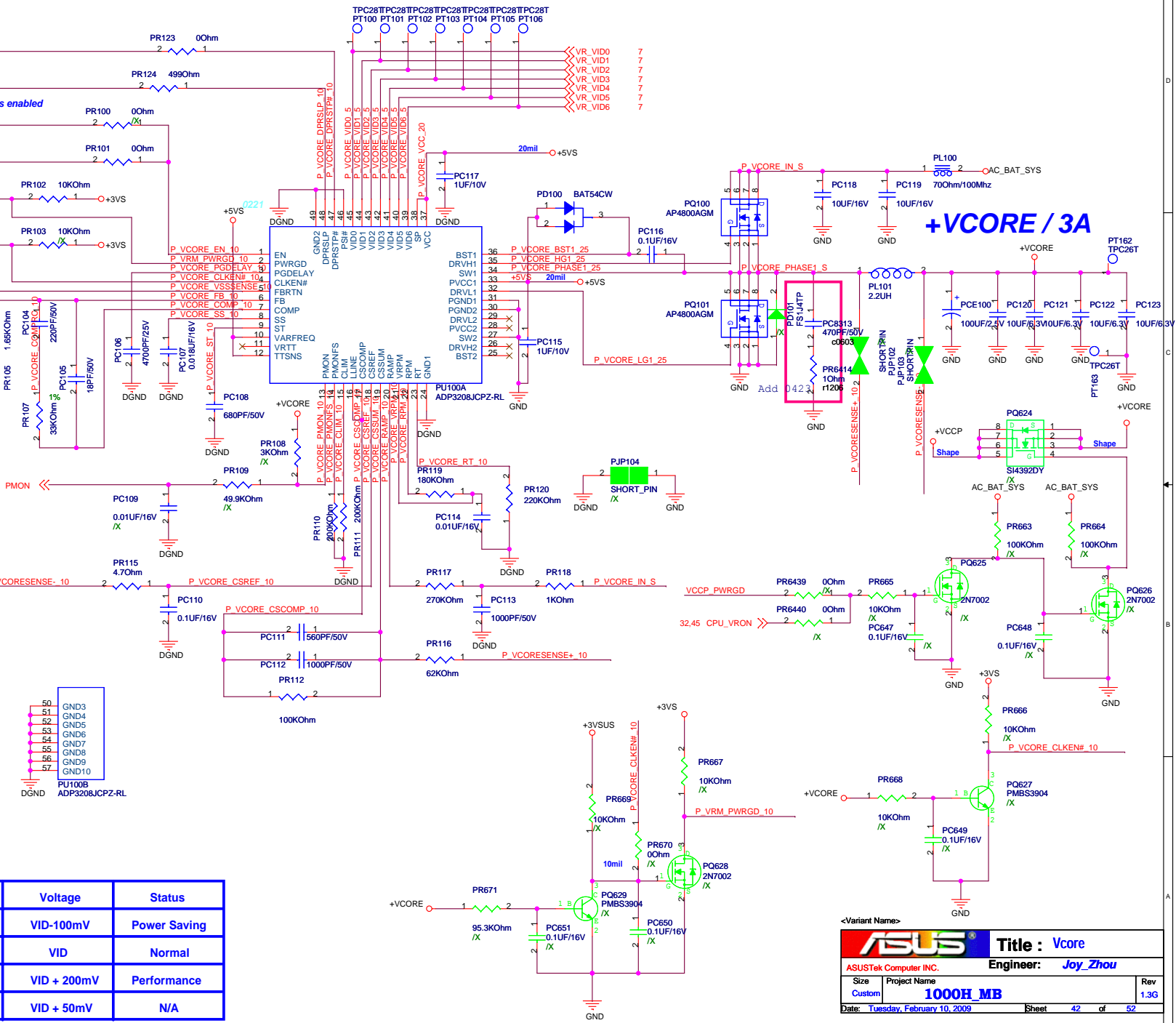
5.45 VCCP\_PWRGD >>>  
**VCCP\_PWRGD = 1, Vcore Reglator Enabled**

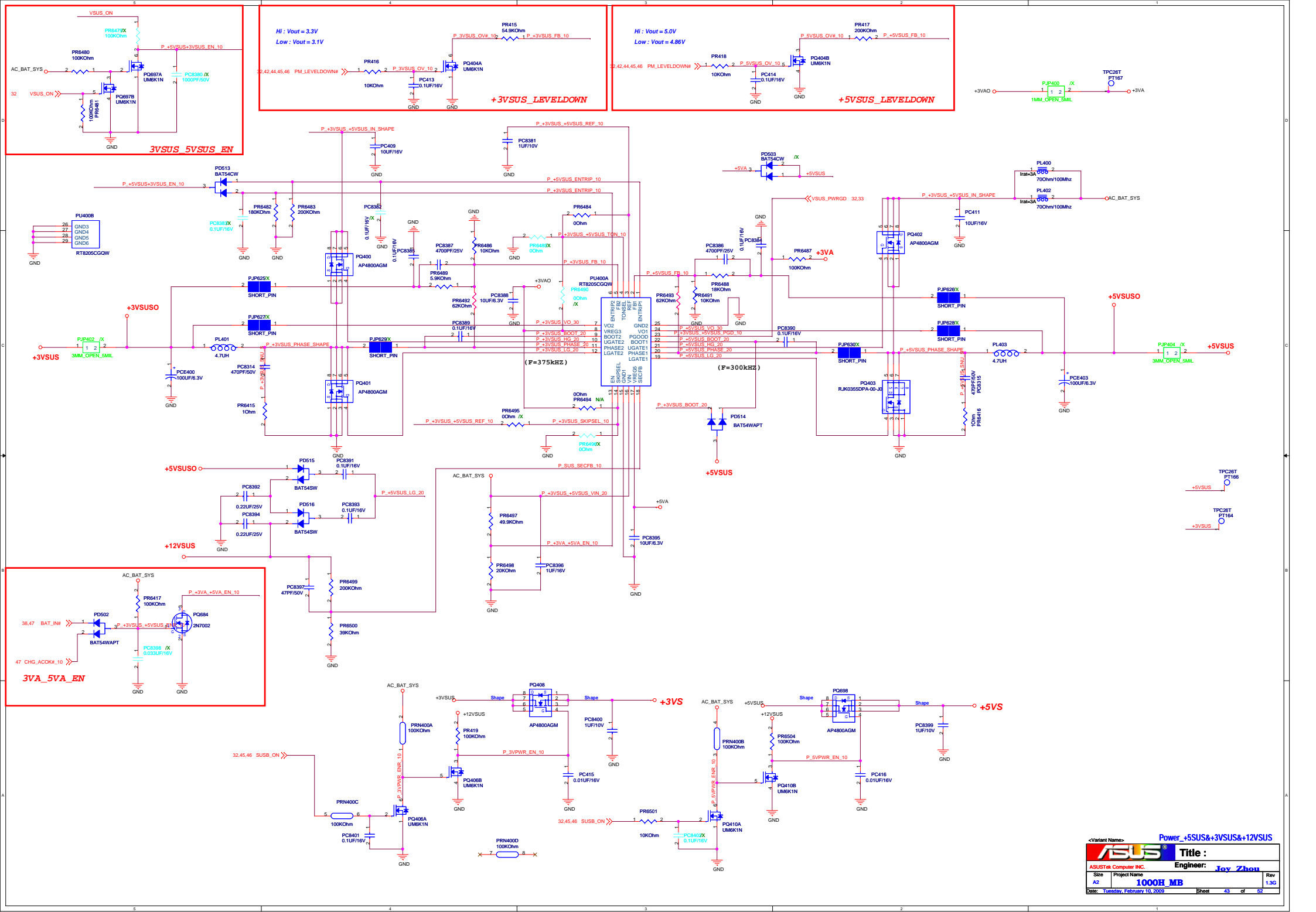
9.18.32 VRM\_PWRGD <<<  
**VRM\_PWRGD = 1, Vcore Power OK**

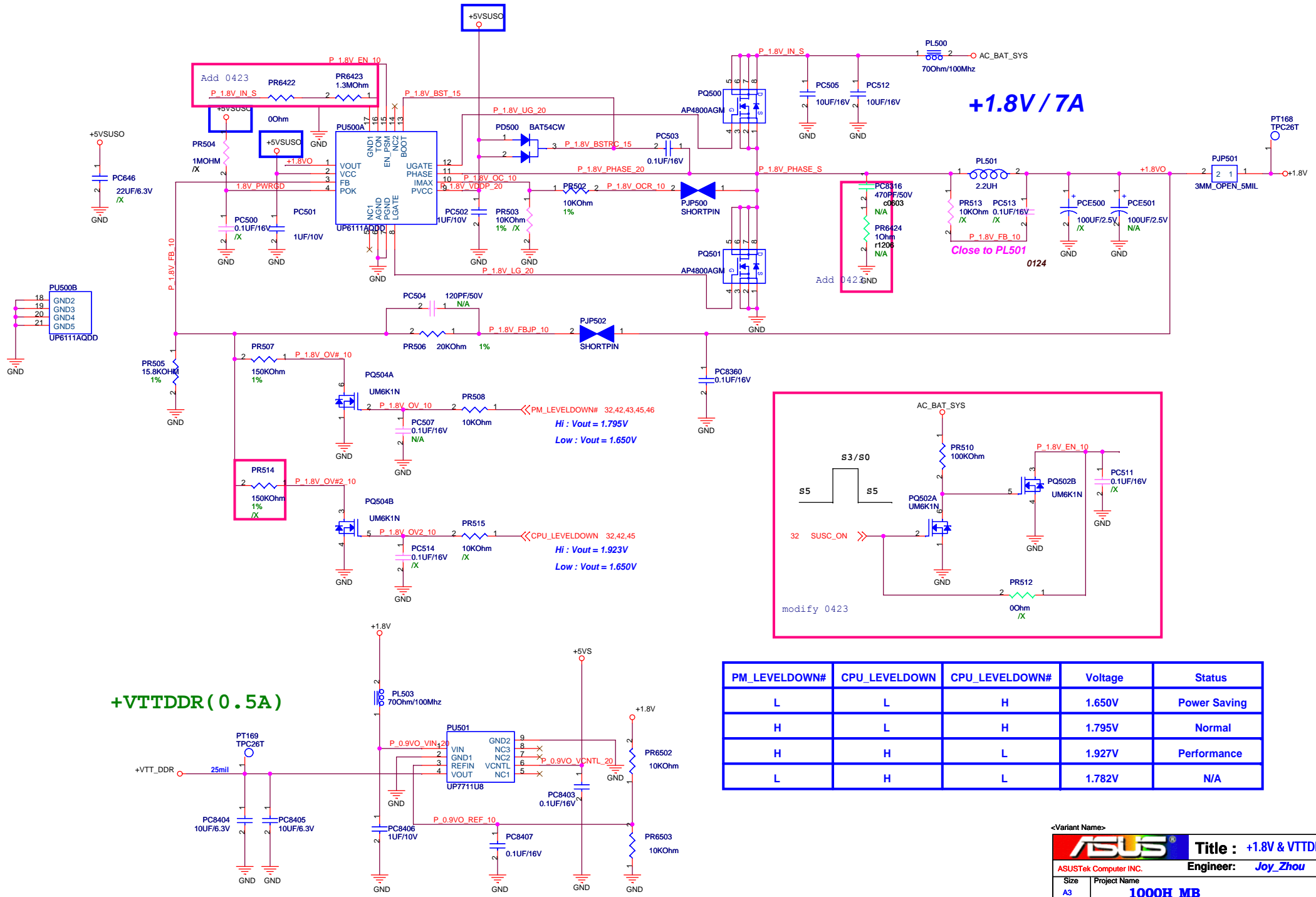


R1.1G

PM_LEVELDOWN#	CPU_LEVELDOWN	CPU_LEVELDOWN#	Voltage	Status
L	L	H	VID-100mV	Power Saving
H	L	H	VID	Normal
H	H	L	VID + 200mV	Performance
L	H	L	VID + 50mV	N/A

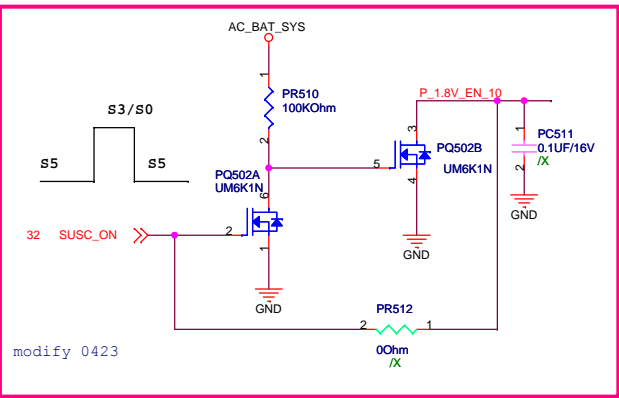






# +1.8V / 7A

## +VTTDDR (0.5A)



PM_LEVELDOWN#	CPU_LEVELDOWN	CPU_LEVELDOWN#	Voltage	Status
L	L	H	1.650V	Power Saving
H	L	H	1.795V	Normal
H	H	L	1.927V	Performance
L	H	L	1.782V	N/A

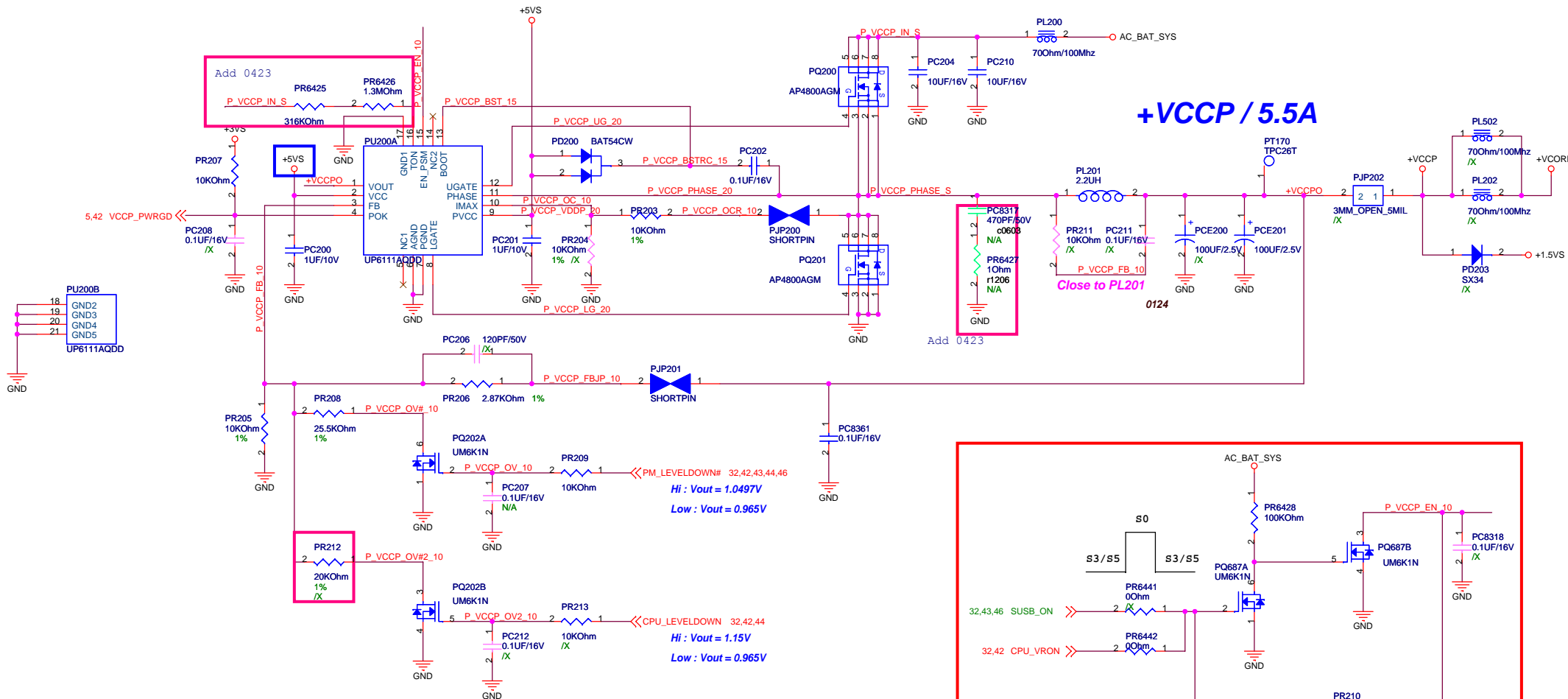
<Variant Name>

**Title : +1.8V & VTTDDR**

ASUSTek Computer INC. **Engineer: Joy\_Zhou**

Size	Project Name	Rev
A3	<b>1000H_MB</b>	1.3G

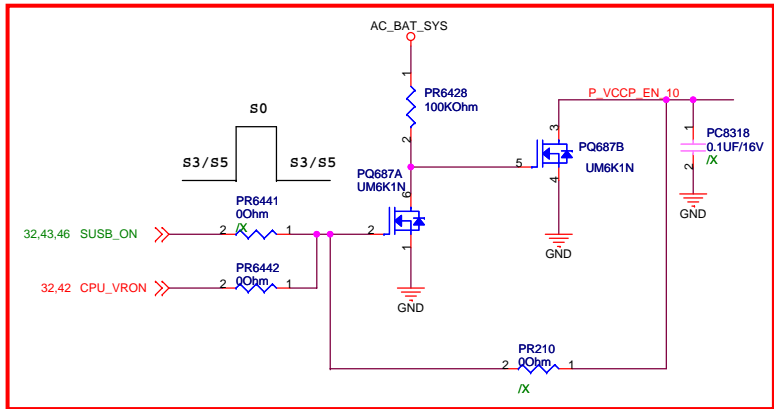
Date: Tuesday, February 10, 2009 Sheet 44 of 52



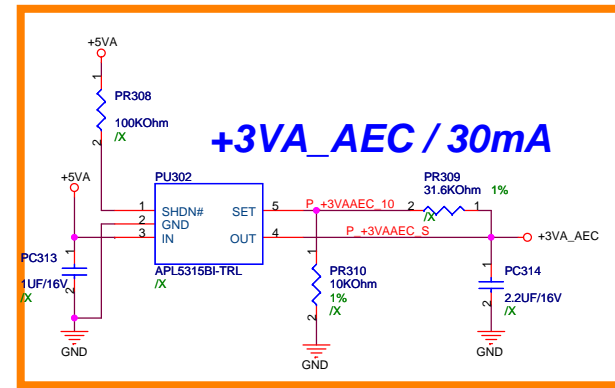
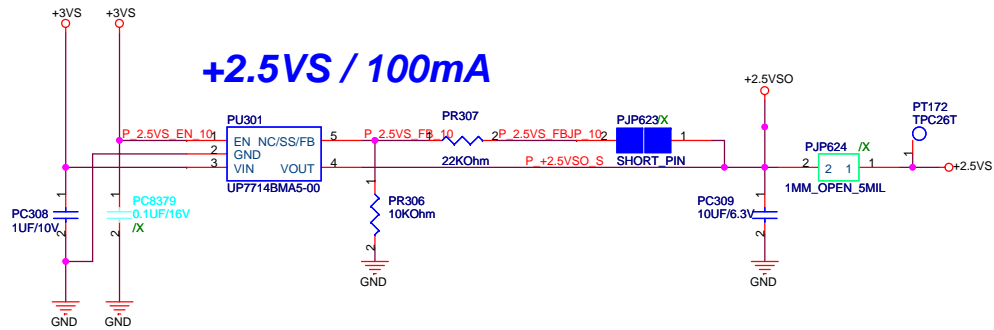
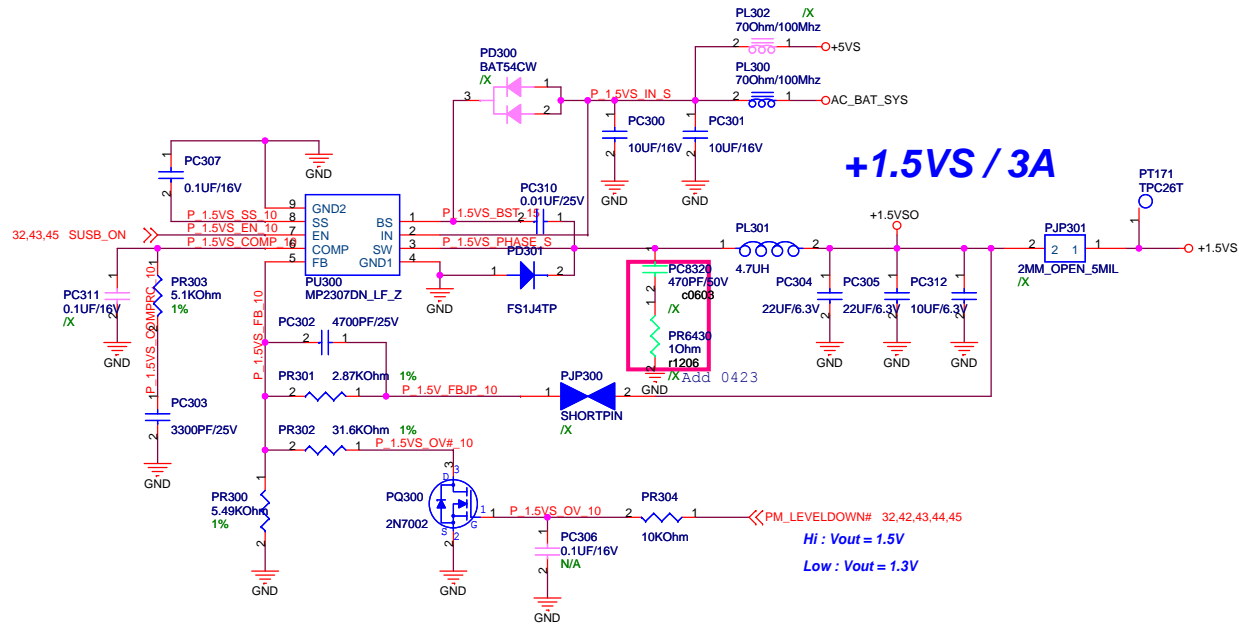
**+VCCP / 5.5A**

PM\_LEVELDOWN# 32,42,43,44,46  
 Hi : Vout = 1.0497V  
 Low : Vout = 0.965V

CPU\_LEVELDOWN# 32,42,44  
 Hi : Vout = 1.15V  
 Low : Vout = 0.965V

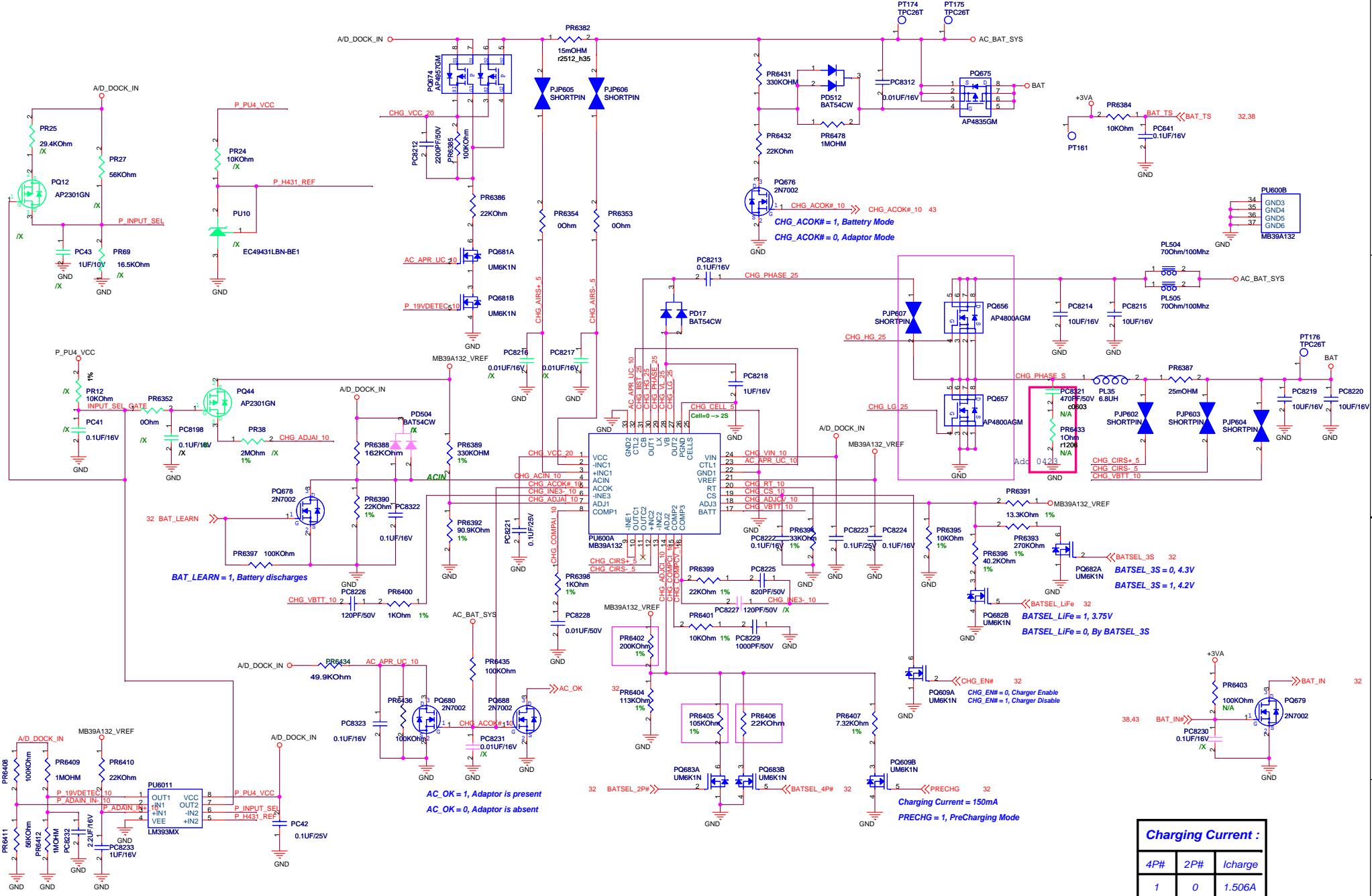


PM_LEVELDOWN#	CPU_LEVELDOWN	CPU_LEVELDOWN#	Voltage	Status
L	L	H	0.965V	Power Saving
H	L	H	1.048V	Normal
H	H	L	1.157V	Performance
L	H	L	1.072V	N/A



<Variant Name>

<b>ASUS</b>		<b>Title : +1.5VS &amp; +2.5VS</b>	
ASUSTek Computer INC.		Engineer: <b>Joy_Zhou</b>	
Size	Project Name	Rev	
A3	<b>1000H_MB</b>	1.3G	
Date:	Tuesday, February 10, 2009	Sheet	46 of 52



**Battery Charging Voltage :**  
 $V_{adj3} > 4.1V \implies V_{bat} = 4.2V / cell$   
 $2.2V > V_{adj3} > 1.1V \implies V_{bat} = 2 * V_{adj3}$

**Battery Charging Current :**  
 $4.4V > V_{adj2} \geq 0V \implies I_{chg} = (V_{adj2} - 0.075V) / (25 * R_s)$

**Input Adaptor Max. Current Limit :**  
 $I_{limit\_current} = (V_{adj1} - 0.075V) / (25 * R_s)$

**Pre-Charging Mode :**  
 Precharging current = 150mA  
 $V_{adj2} = 168.75mV$

**Adaptor Max. Current :**  
 $PR600 = 235.8K; I_{limit} = 2.170A; 20.615W (9.5V/22V)$   
 $PR600 = 185.3K; I_{limit} = 2.677A; 32.124W (12V/36W)$

**ACIN Threshold = 1.25V**  
 Adaptor > 8.63V, System Powered by Adaptor  
 Adaptor < 8.63V, System Powered by Battery

**Prevent Input from 19V :**  
 Adaptor > 13.06V, PQ603B Turn-off  
 Adaptor < 13.06V, PQ603B Turn-on

**Battery Cell Selection :**  
 $BAT\_ID = 1, 2 \text{ Cells}; V_{adj2} = 0.998V \implies I_{charge} = 1.477A$   
 $BAT\_ID = 0, 4/6 \text{ Cells}; V_{adj2} = 1.648V \implies I_{charge} = 2.517A$

**VREF = 5.0V**  
 $f_{osc}(KHz) = 17000 / RT (KOhm)$   
 Soft start:  $t_s(s) = 0.13 * CS (\mu F)$

VTH of -IN1:  $5V / 62 * (100+62) = 13.06V$

VTH of ACIN:  $1.25V / 25 * (185+25) = 10.5V$   
 Change PR607 and PR608 value

**Charging Current :**

4P#	2P#	Icharge
1	0	1.506A
0	1	2.502A
0	0	3.589A

## EC KB3310 GPIO SETTING

Pin	Pin Name	Signal Name	Type	Note
1	GPIO00/GA20	A20GATE	O	
2	GPIO01/KBRST#	RC_IN#	O	
6	GPIO04	EMAIL_SW#	I	Internal pull high
13	GPIO05/PCIRST#	PCI_RST#	I	
14	GPIO07	BAT_OTP	I	Battery over temperature
15	GPIO08	EXTSM#	OD	10K pull high to +3VSB
16	GPIO0A	LID_EC#	I	Internal pull high
17	GPIO0B/ESB_CLK	NC	O	
18	GPIO0C/ESB_DAT	NC	O	
19	GPIO0D	DISTP_SW#	I	Internal pull high
20	GPIO0E/SC#	EXT_SC#	O	10K pull high to +3VSB
21	GPIO0F/PWM0	BL_PWM_DA	O	
23	GPIO10/PWM1	BAT_CRITICAL	I	Battery critical capacity
25	GPIO11/PWM2	PM_PWRBTN#	OD	Internal pull high in ICH
26	GPIO12/FANPWM1	FAN0_PWM	O	CPU Fan
27	GPIO13/FANPWM2	FAN1_PWM	O	VGA Fan
28	GPIO14/FANFB1	FAN0_TACH	I	CPU FanTach
29	GPIO15/FANFB2	FAN1_TACH	I	VGA FanTach
30	GPIO16/E51_TX	E51_TX	O	RS232 debug port
31	GPIO17/E51_RX	E51_RX	I	RS232 debug port
32	GPIO18	PWR_SW#	I	Internal pull high
34	GPIO19/PWM3	MAIL_LED#	O	
36	GPIO1A/NUMLED	NUM_LED#	O	
38	GPIO1D/CLKRUN#	NC	O	
39	GPIO20/KSO0/TP_TEST	KSO0	O	
40	GPIO21/KSO1/TP_PLL	KSO1	O	
41	GPIO22/KSO2	KSO2	O	
42	GPIO23/KSO3	KSO3	O	
43	GPIO24/KSO4	KSO4	O	
44	GPIO25/KSO5	KSO5	O	
45	GPIO26/KSO6	KSO6	O	
46	GPIO27/KSO7	KSO7	O	
47	GPIO28/KSO8	KSO8	O	
48	GPIO29/KSO9	KSO9	O	
49	GPIO2A/KSO10	KSO10	O	
50	GPIO2B/KSO11	KSO11	O	
51	GPIO2C/KSO12	KSO12	O	
52	GPIO2D/KSO13	KSO13	O	
53	GPIO2E/KSO14	KSO14	O	
54	GPIO2F/KSO15	KSO15	O	
55	GPIO30/KSI0	KSI0	I	Internal pull high
56	GPIO31/KSI1	KSI1	I	Internal pull high
57	GPIO32/KSI2	KSI2	I	Internal pull high
58	GPIO33/KSI3	KSI3	I	Internal pull high
59	GPIO34/KSI4	KSI4	I	Internal pull high
60	GPIO35/KSI5	KSI5	I	Internal pull high
61	GPIO36/KSI6	KSI6	I	Internal pull high
62	GPIO37/KSI7	KSI7	I	Internal pull high
63	GPI38/AD0	BAT_IJCHG	I	
64	GPI39/AD1	BAT_CONFIG	I	Battery configuration
65	GPIO3A/AD2	BAT_SENSE	I	Battery Voltage Sensor
66	GPIO3B/AD3	BAT_TS	I	Battery Thermal Sensor
68	GPO3C/DA0	DOC	O	Trigger Clock Gen

## EC KB3310 Other Pin SETTING

Pin	Pin Name	Signal Name	Type	Note
3	SERIRQ	INT_SERIRQ	I/OD	10K pull high to +3V
4	LFRAME#	LPC_FRAME#	I	
5	LAD3	LPC_AD3	I/O	
7	LAD2	LPC_AD2	I/O	
8	LAD1	LPC_AD1	I/O	
9	VCC	+3VA_EC	P	
10	LAD0	LPC_AD0	I/O	
11	GND	GND	P	
12	PCICLK	CLK_PCI_EC	I	
22	VCC	+3VA_EC	P	
24	GND	GND	P	
33	VCC	+3VA_EC	P	
35	GND	GND	P	
37	ECRST#	EC_RST#	I	100K pull high to +3VA_EC
67	AVCC	+3VACC	P	
69	AGND	AGND	P	
94	GND	GND	P	
96	VCC	+3VA_EC	P	
111	VCC	+3VA_EC	P	
113	GND	GND	P	
119	RD#/SPIDI	SPI_SO	I	
120	WR#/SPIDO	SPI_SI	O	
112	XCLKI	32KXCLKI	I	
123	XCLKO	32KXCLKO	O	
124	V18R	V18R	P	Reserved 1uF to GND
125	VCC	+3VA_EC	P	
128	SPICS#/SELMEM#	SPI_CE#	O	

Pin	Pin Name	Signal Name	Type	Note
70	GPO3D/DA1	LCD_BACKOFF#	O	
71	GPO3E/DA2	CLK_PWRSERVE#	O	
72	GPO3F/DA3	BAT_LL#	O	Battery Low Low
73	GPIO40	AC_OK	I	AC Adaptor Plug in
74	GPIO41	PM_RSMRST#	O	10K pull down to GND
75	GPI42	BAT_IN	I	
76	GPI43	CLRTC_EC	I	
77	GPIO44/SCL1	SMB0_CLK	I/OD	4.7K pull high to +3VA_EC
78	GPIO45/SDA1	SMB0_DAT	I/OD	4.7K pull high to +3VA_EC
79	GPIO46/SCL2	SMB1_CLK	I/OD	10K pull high to +3V
80	GPIO47/SDA2	SMB1_DAT	I/OD	10K pull high to +3V
81	GPIO48/KSO16	KB pin 28	I	for KB type detection
82	GPIO49/KSO17	KB pin 27	I	for KB type detection
83	GPIO4A/PSCLK1	AUO_SCL	O	for AUO, default H at S0
84	GPIO4B/PSDAT1	AUO_SDA	O	for AUO, default L at S0
85	GPIO4C/PSCLK2	AUO_CSB	O	for AUO, default H at S0
86	GPIO4D/PSDAT2	LVDD_EN	I	for AUO 7" Panel
87	GPIO4E/PSCLK3	TP_CLK	I/OD	10K pull high to +3V
88	GPIO4F/PSDAT3	TP_DAT	I/OD	10K pull high to +3V
89	GPIO50/SELIO#	BATSEL_3S	O	Battery series, H:3S, L:4S
90	GPIO52/E51_CS#	CHG_LED_UP#	O	
91	GPIO53/CAPLED	CAP_LED#	O	
92	GPIO54	PWR_LED_UP	O	
93	GPIO55/SCRLLED	SCRL_LED#	O	
95	GPIO56	PWR4G_SW#	I	Internal pull high
97	GPXOA00/SDICS#	SPI_MODE#	O	4.7K pull down to GND
98	GPXOA01/SDICLK	SUSC_ON	O	
99	GPXOA02/SDIDO	VSUS_ON	O	
100	GPXOA03	CPU_VRON	O	
101	GPXOA04	SUSB_ON	O	
102	GPXOA05	ICH_PWROK	O	
103	GPXOA06	VOLT_CTRL	O	
104	GPXOA07	CHG_EN#	O	Battery charging enabled
105	GPXOA08	PRECHG	O	
106	GPXOA09	SPI_WP#	O	
107	GPXOA10	OP_SD#	O	Audio OP
108	GPXOA11	BAT_LEARN	O	
109	GPXID0/SDIDI	BATSEL_2P#	O	Battery parallel, H:1P, L:2P-3P
110	GPXID1	NC	O	
112	GPXID2	THRO_CPU	O	Active if CPU temperature over spec
114	GPXID3	SUSB#	I	100K pull down to GND
115	GPXID4	SUSC#	I	100K pull down to GND
116	GPXID5	CPUPWR_GD	I	Pull high to +3V
117	GPXID6	VSUS_GD	I	
118	GPXID7	NC	O	
121	GPIO57	INTERNET#	I	Internal pull high
126	GPIO57/SPICLK	SPI_CLK	O	
127	GPIO59/TEST_CLK	NC	O	


<Variant Name>

		<b>Title : EC Pin Define</b>	
ASUSTek Computer INC.		Engineer: <b>Satan He</b>	
Size	Project Name		Rev
A3	<b>1000H_MB</b>		1.1G
Date: <b>Tuesday, February 10, 2009</b>		Sheet	50 of 52





<Variant Name>

		<b>Title :</b> History
ASUSTek Computer INC.		<b>Engineer:</b> KingCa_Jin
Size	Project Name	Rev
A3	<b>1000H_MB</b>	1.3G
Date: Tuesday, February 10, 2009		Sheet 51 of 52

5

4

3

2

1

D

D

C

C


B

B

A

A

<Variant Name>

		<b>Title :</b> History	
ASUSTek Computer INC.		<b>Engineer:</b> KingCa_Jin	
Size	Project Name		Rev
A3	<b>1000H_MB</b>		1.3G
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4

3

2

1