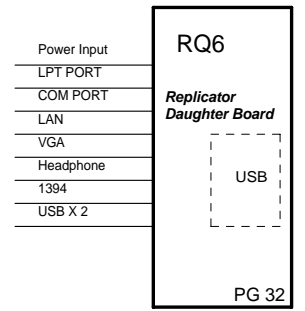
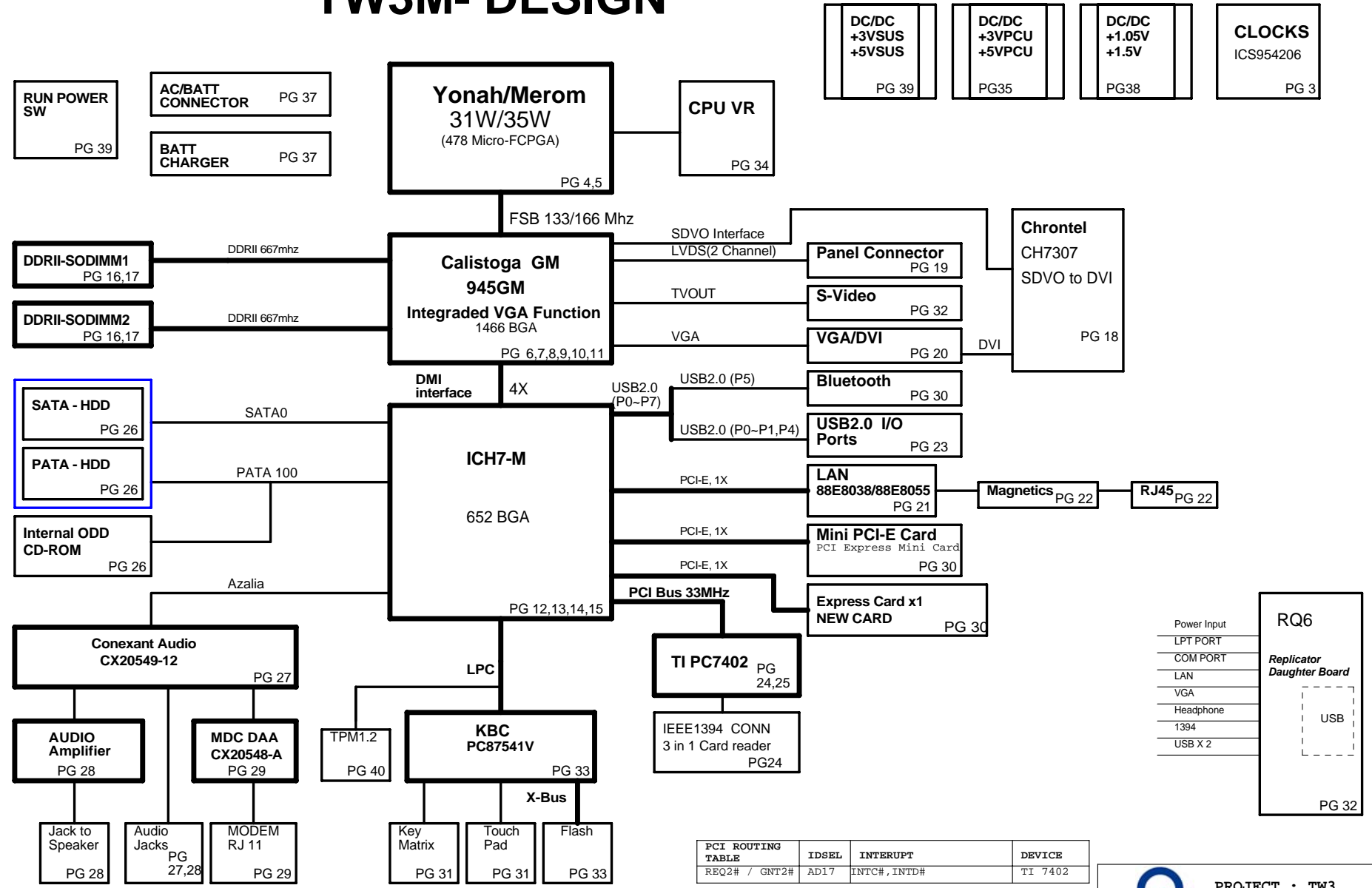


**PCB STACK UP**

- LAYER 1 : TOP
- LAYER 2 : SGND1
- LAYER 3 : IN1
- LAYER 4 : IN2
- LAYER 5 : VCC
- LAYER 6 : IN3
- LAYER 7 : SGND2
- LAYER 8 : BOT

# TW3M- DESIGN



PCI ROUTING TABLE	IDSEL	INTERUPT	DEVICE
REQ2# / GNT2#	AD17	INTC#, INTD#	TI 7402

**PROJECT : TW3**  
**Quanta Computer Inc.**

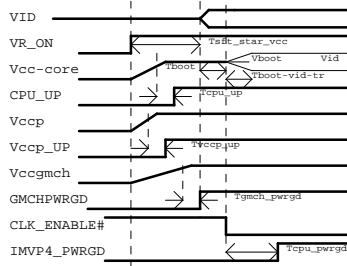
Size	Document Number	Rev
	Block Diagram	B2A
Date: Tuesday, April 18, 2006	Sheet 1 of 48	

Board Stack up Description

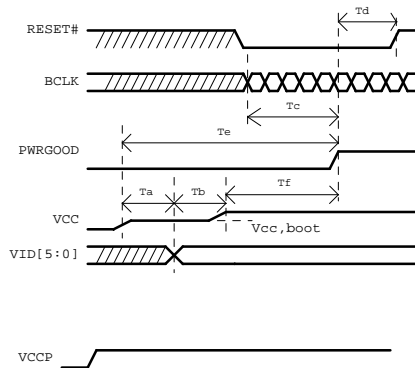
PCB Layers

- Layer 1 TOP (Component, Other)
- Layer 2 Ground Plane
- Layer 3 IN1
- Layer 4 IN2
- Layer 5 Power Plane
- Layer 6 IN3
- Layer 7 Ground Plane
- Layer 8 BOTTOM

Power On Sequencing Timing Diagram



Dothan Power-up Timing Specifications

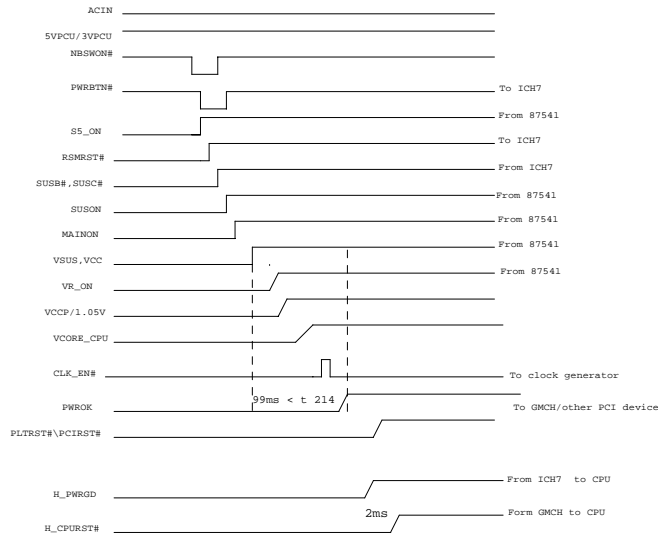


Ta=VCC and VCCP assertion to VID[5:0] valid  
 Tb=VID[5:0] stable to VCC valid  
 Tc=BCLK stable to PWRGOOD assertion  
 Te=PWRGOOD to RESET# de-assertion time  
 Tf=Vcc,boot valid to PWRGOOD assertion time

Voltage Rails

Voltage Rails	ON S0-S2	ON S3	ON S4	ON S5	Control signal
VCC_CORE Core voltage for Processor	X				VR_ON 0.726V-0.94V
VCCP Core voltage for CPU / NB	X				VR_ON
SMDRR_VTERM 0.9V for DDR2 Termination voltage	X				MAINON
RVCC1.5	X	X	X		RVCC_ON
RVCC3	X	X	X		RVCCD
VCC1.5	X				MAIND
VCC2.5	X				MAINON
VCC3	X				MAIND
VCC5	X				MAIND
1.8VSUS	X	X			SUSON
3VSUS	X	X			SUSD
5VSUS	X	X			SUSD
3VPCU	X	X	X	X	VL
5VPCU	X	X	X	X	VL
9VPCU	X	X	X	X	5VPCU

ACIN POWER ON TIMING

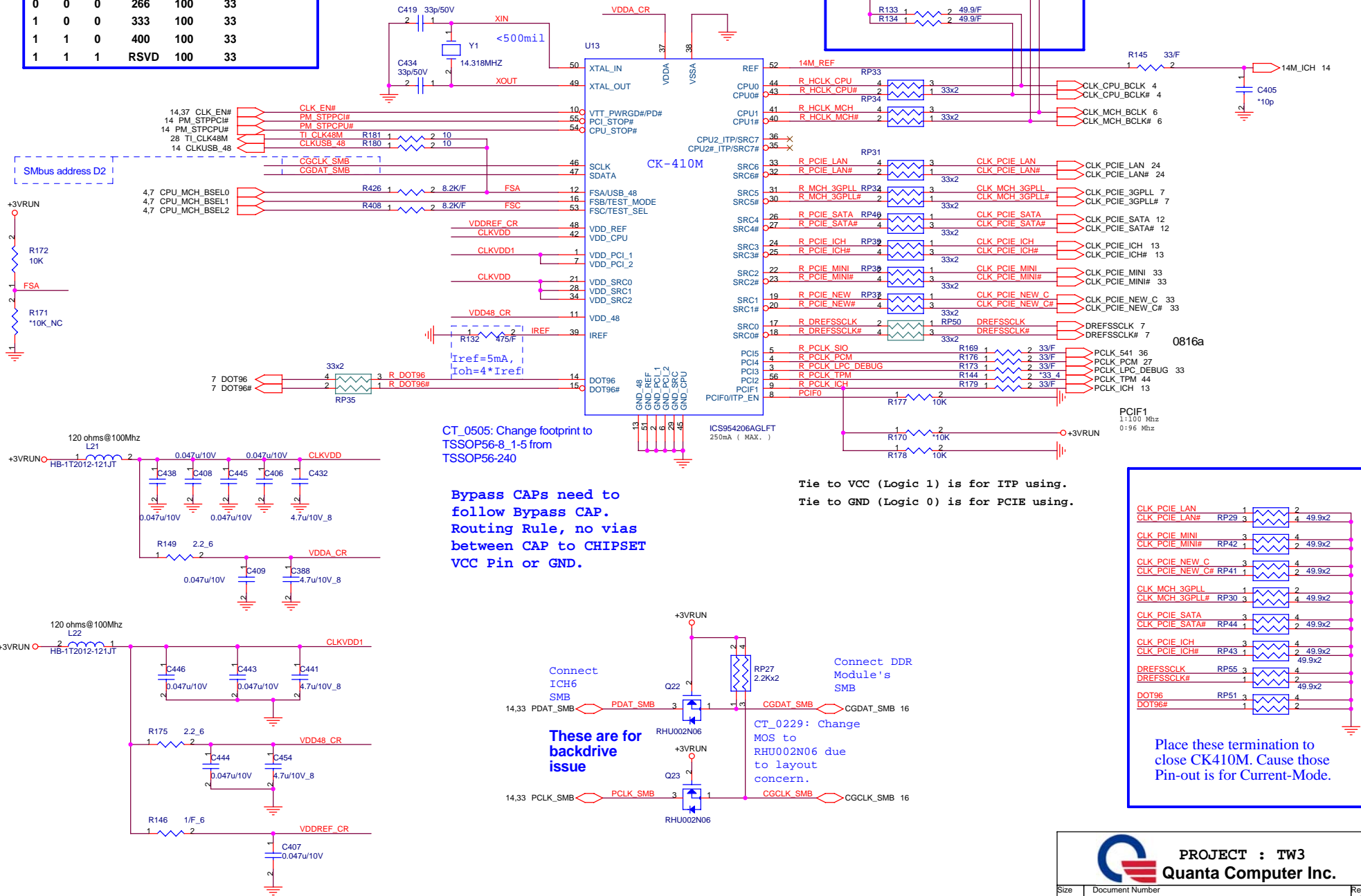


Voltage Rails	ON S0-S1	ON S3	ON S4	ON S5	Control signal
VCC_CORE Core voltage for Processor	X				VRON
GMCH_VTT Core voltage for GMCH 1.05V	X				MAINON
SMDRR_VTERM 0.9V for DDR II Termination voltage	X				MAINON
SMDRR_VREF 0.9V for DDR II Reference Voltage	X				MAINON
GMCH 1.5V	X				MAINON
1.8VSUS 1.8V for DDR II voltage	X	X			SUSON
2.5V	X				MAINON
3VPCU	X	X	X	X	VL
5VPCU	X	X	X	X	SUSON
9V	X				MAINON
3V	X	X	X	X	VL
1.8VSUS	X	X			SUSON
5V	X				MAINON
POWER SOURCE	X	X	X	X	

PCI DEVICE	IDSEL#	REQ# / GNT#	Interrupts
PCI7402	AD17	REQ2# / GNT2#	PIRQ CD

FSC	FSB	FSA	CPU	SRC	PCI
1	0	1	100	100	33
0	0	1	133	100	33
0	1	1	166	100	33
0	1	0	200	100	33
0	0	0	266	100	33
1	0	0	333	100	33
1	1	0	400	100	33
1	1	1	RSVD	100	33

Place these termination to close CK410M. Cause those Pin-out is for Current-Mode.



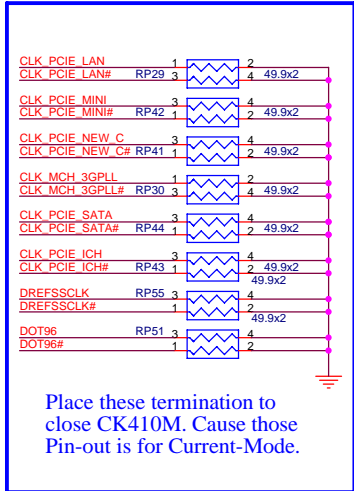
CT\_0505: Change footprint to TSSOP56-8..1-5 from TSSOP56-240

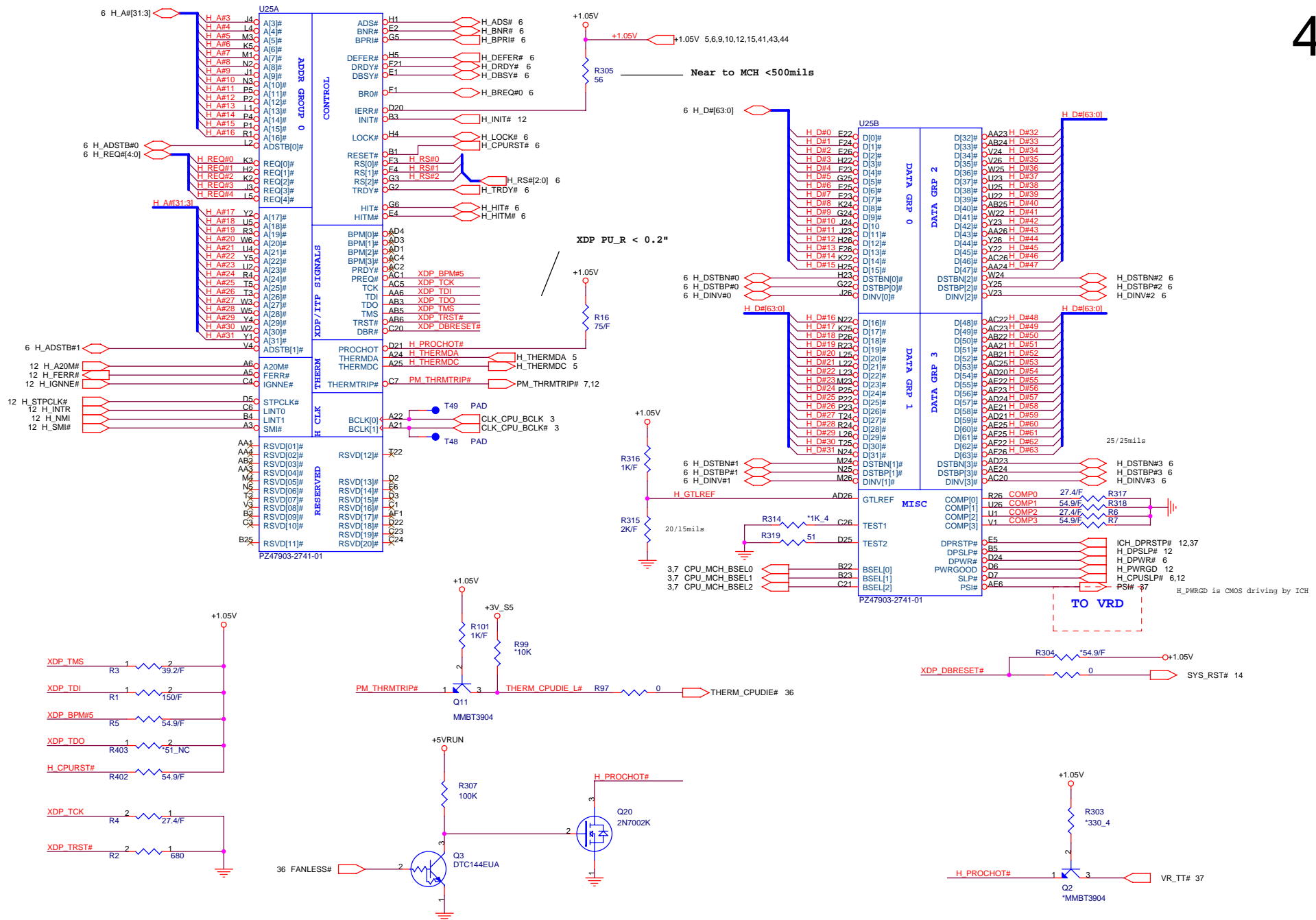
Bypass CAPs need to follow Bypass CAP. Routing Rule, no vias between CAP to CHIPSET VCC Pin or GND.

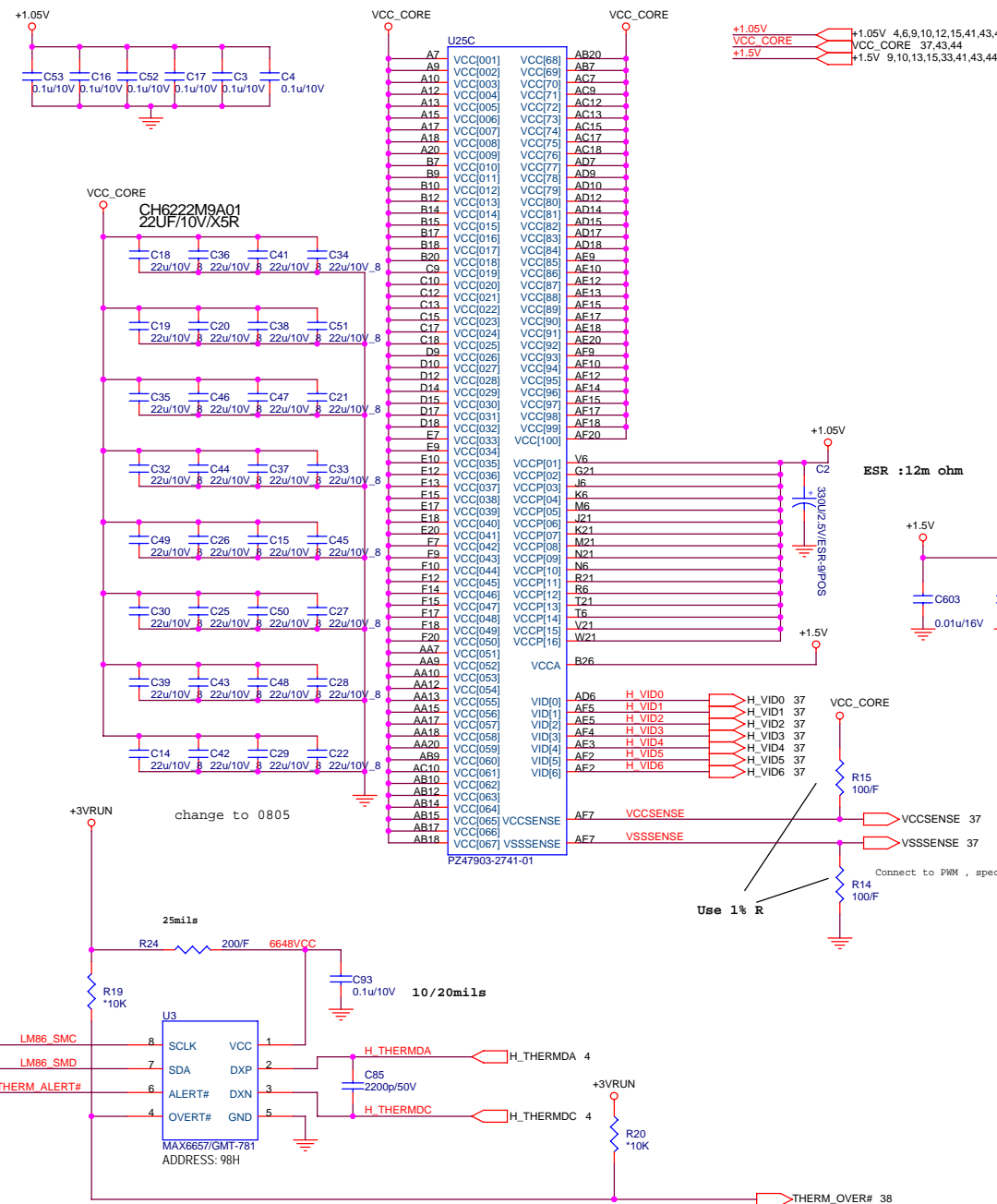
Tie to VCC (Logic 1) is for ITP using. Tie to GND (Logic 0) is for PCIE using.

Connect ICH6 SMB. These are for backdrive issue.

Connect DDR Module's SMB. CT\_0229: Change MOS to RHY002N06 due to layout concern.







+1.05V  
 VCC\_CORE 4,6,9,10,12,15,41,43,44  
 +1.5V  
 VCC\_CORE 37,43,44

ESR :1.2m ohm

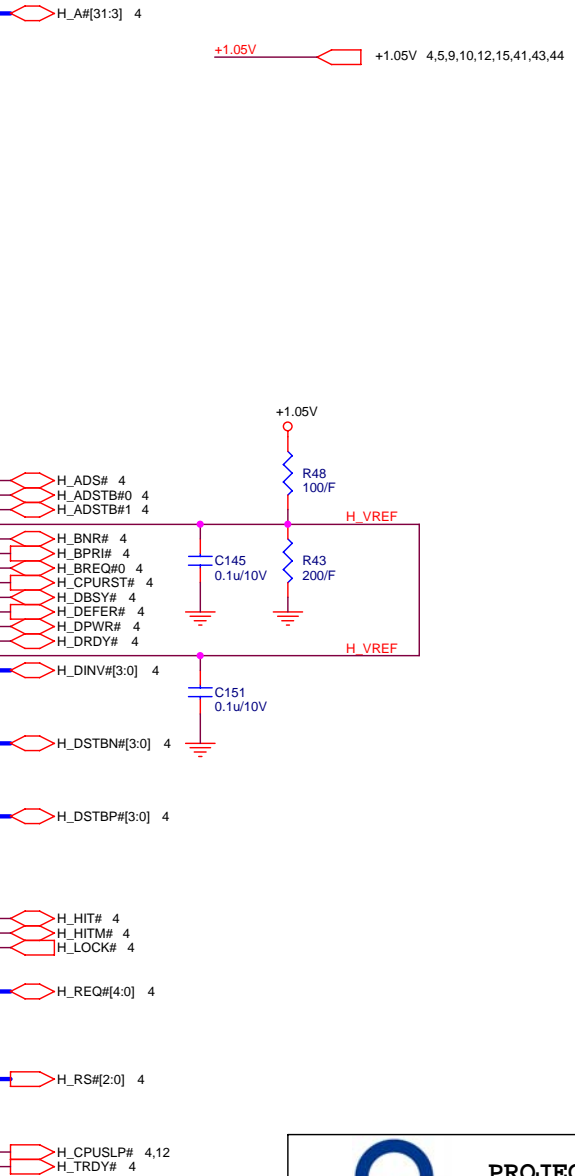
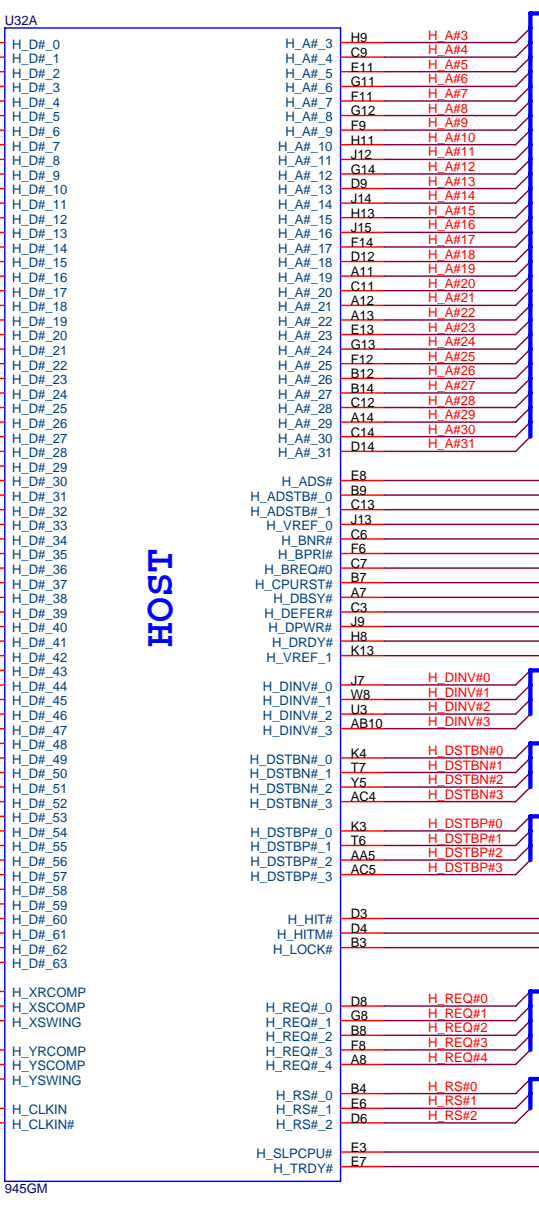
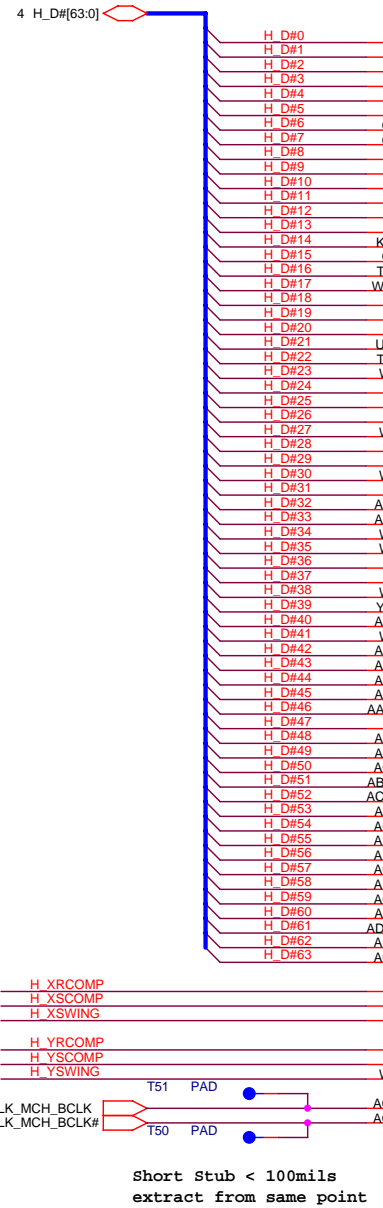
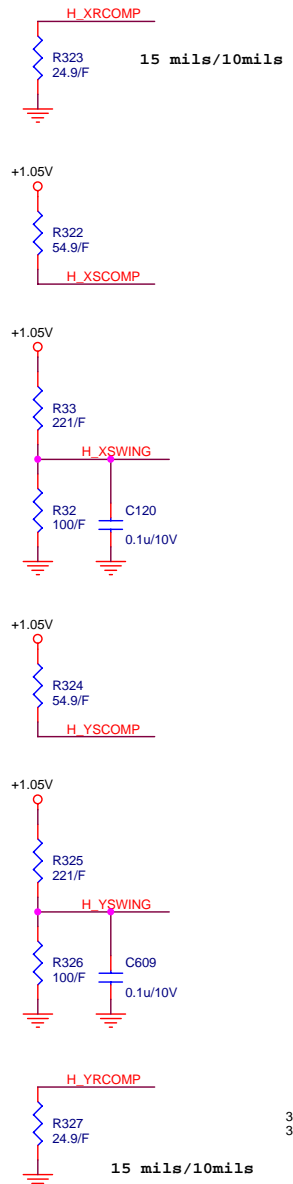
Use 1% R

add hardware protect

Uninstall R267 , Q28 , Q26 for Intel sighting -> CPU thermal die bug /0506

**PROJECT : TW3**  
**Quanta Computer Inc.**

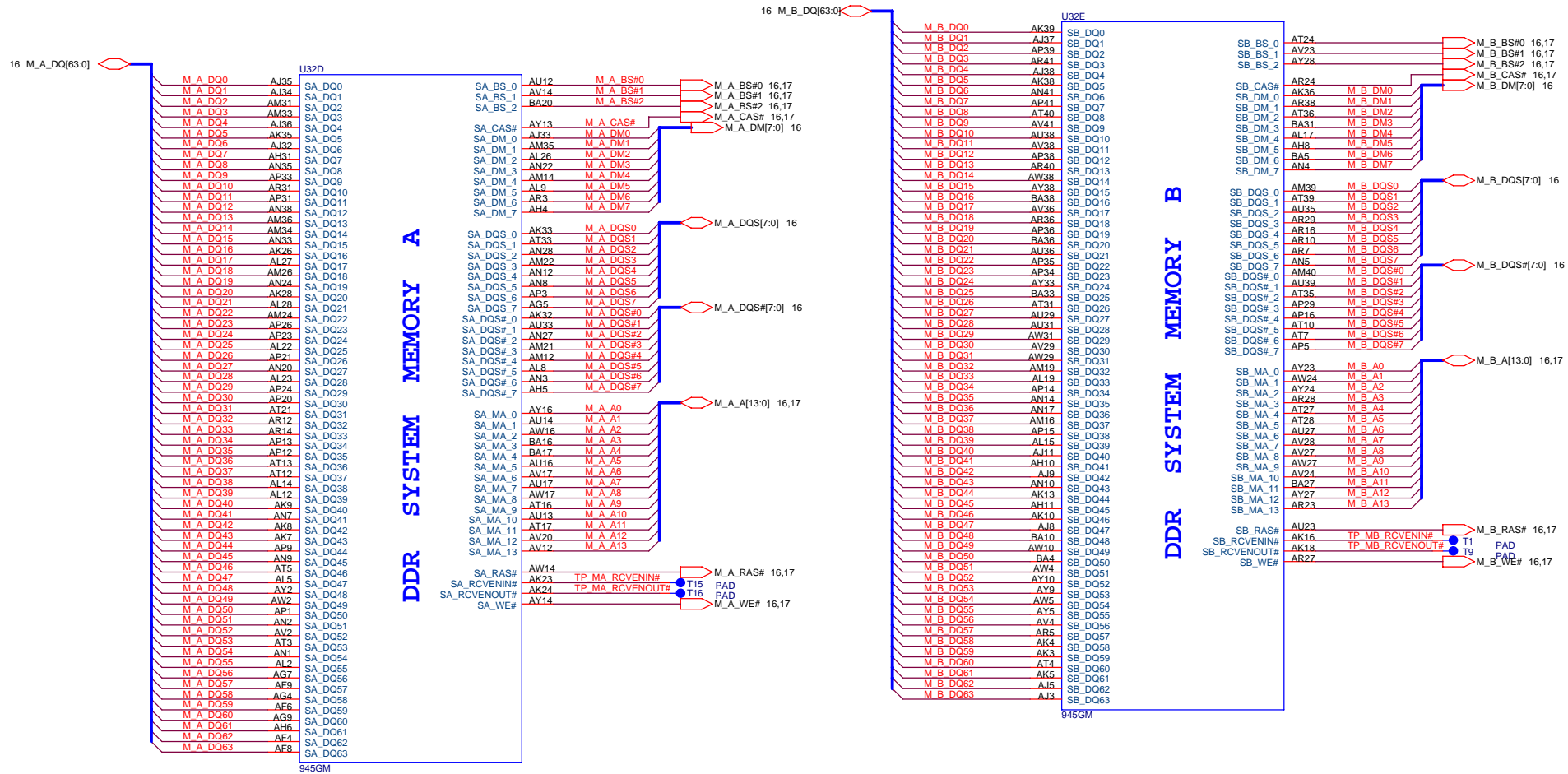
Size	Document Number	Rev
	Yonah/Merom (Power/NC)	B2A
Date:	Tuesday, April 18, 2006	Sheet 5 of 48



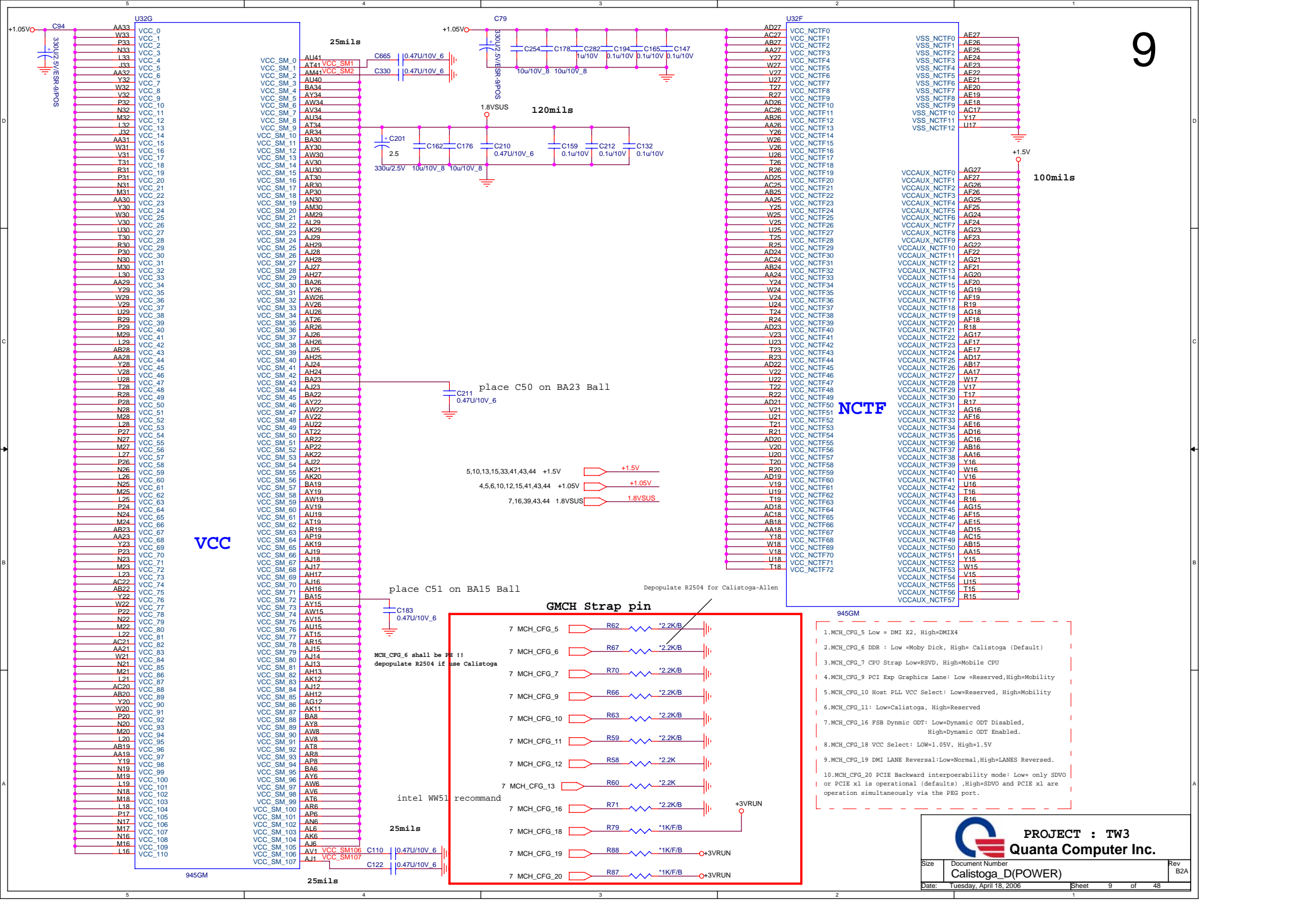
**PROJECT : TW3**  
**Quanta Computer Inc.**

Size	Document Number	Rev
	Calistoga_A(Host)	B2A
Date:	Tuesday, April 18, 2006	Sheet 6 of 48









VCC

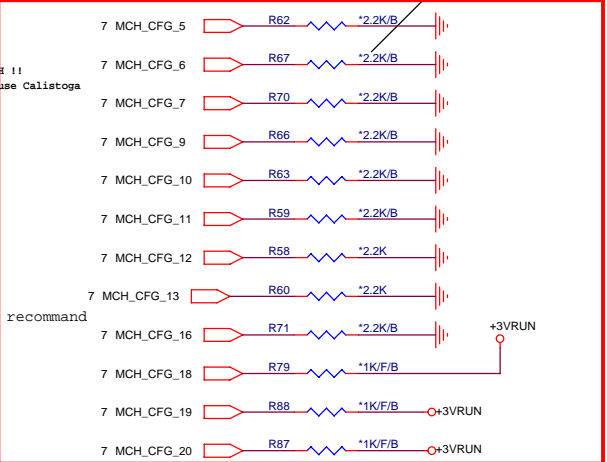
NCTF

place C51 on BA15 Ball

Depopulate R2504 for Calistoga-Allen

GMCH Strap pin

MCH\_CFG\_6 shall be PH !!  
depopulate R2504 if use Calistoga



- 945GM
- 1.MCH\_CFG\_5 Low = DMI X2, High=DMIX4
  - 2.MCH\_CFG\_6 DDR : Low =Moby Dick, High= Calistoga (Default)
  - 3.MCH\_CFG\_7 CPU Strap Low=RSVD, High=Mobile CPU
  - 4.MCH\_CFG\_9 PCI Exp Graphics Lane: Low =Reserved,High=Mobility
  - 5.MCH\_CFG\_10 Host PLL VCC Select: Low=Reserved, High=Mobility
  - 6.MCH\_CFG\_11: Low=Calistoga, High=Reserved
  - 7.MCH\_CFG\_16 FSB Dymic ODT: Low=Dynamic ODT Disabled, High=Dynamic ODT Enabled.
  - 8.MCH\_CFG\_18 VCC Select: LOW=1.05V, High=1.5V
  - 9.MCH\_CFG\_19 DMI Lane Reversal:Low=Normal,High=LANES Reversed.
  - 10.MCH\_CFG\_20 PCIe Backward interoperability mode: Low only SDVO or PCIe x1 is operational (defaults),High=SDVO and PCIe x1 are operation simultaneously via the PEG port.

**PROJECT : TW3**  
**Quanta Computer Inc.**

Size	Document Number	Rev
	Calistoga_D(POWER)	B2A
Date:	Tuesday, April 18, 2006	Sheet 9 of 48



U32I

AC41	VSS_0	VSS_97	AK34
AA41	VSS_1	VSS_98	AC34
W41	VSS_2	VSS_99	AF34
T41	VSS_3	VSS_100	AE34
P41	VSS_4	VSS_101	AC34
M41	VSS_5	VSS_102	C34
J41	VSS_6	VSS_103	AW33
F41	VSS_7	VSS_104	AV33
AV40	VSS_8	VSS_105	AR33
AP40	VSS_9	VSS_106	AE33
AN40	VSS_10	VSS_107	AB33
AK40	VSS_11	VSS_108	Y33
AM40	VSS_12	VSS_109	T33
AH40	VSS_13	VSS_110	R33
AG40	VSS_14	VSS_111	M33
AF40	VSS_15	VSS_112	H33
AE40	VSS_16	VSS_113	G33
A40	VSS_17	VSS_114	F33
AY39	VSS_18	VSS_115	D33
AW39	VSS_19	VSS_116	B33
AV39	VSS_20	VSS_117	AH32
AR39	VSS_21	VSS_118	AG32
AN39	VSS_22	VSS_119	AF32
AK39	VSS_23	VSS_120	Y21
AM39	VSS_24	VSS_121	P21
AH39	VSS_25	VSS_122	K21
AG39	VSS_26	VSS_123	J21
AF39	VSS_27	VSS_124	HP1
AE39	VSS_28	VSS_125	C21
A40	VSS_29	VSS_126	AW20
Y39	VSS_30	VSS_127	AR20
W39	VSS_31	VSS_128	AM20
V39	VSS_32	VSS_129	AG20
T39	VSS_33	VSS_130	AB31
R39	VSS_34	VSS_131	Y31
P39	VSS_35	VSS_132	AB30
M39	VSS_36	VSS_133	E30
J39	VSS_37	VSS_134	AN29
F39	VSS_38	VSS_135	W19
AV38	VSS_39	VSS_136	K19
AP38	VSS_40	VSS_137	G19
AN38	VSS_41	VSS_138	C19
AK38	VSS_42	VSS_139	AM18
AM38	VSS_43	VSS_140	P18
AH38	VSS_44	VSS_141	H18
AG38	VSS_45	VSS_142	D18
AF38	VSS_46	VSS_143	B29
AE38	VSS_47	VSS_144	A29
A40	VSS_48	VSS_145	AW28
Y37	VSS_49	VSS_146	AR17
W37	VSS_50	VSS_147	AP17
V37	VSS_51	VSS_148	AM17
T37	VSS_52	VSS_149	AK17
R37	VSS_53	VSS_150	AV16
P37	VSS_54	VSS_151	AD28
M37	VSS_55	VSS_152	AL16
J37	VSS_56	VSS_153	J16
F37	VSS_57	VSS_154	F16
AV36	VSS_58	VSS_155	C16
AP36	VSS_59	VSS_156	AN15
AN36	VSS_60	VSS_157	AM15
AK36	VSS_61	VSS_158	AK15
AM36	VSS_62	VSS_159	J27
AH36	VSS_63	VSS_160	G27
AG36	VSS_64	VSS_161	F27
AF36	VSS_65	VSS_162	C27
AE36	VSS_66	VSS_163	B27
A40	VSS_67	VSS_164	AN26
Y35	VSS_68	VSS_165	M26
W35	VSS_69	VSS_166	K26
V35	VSS_70	VSS_167	D26
T35	VSS_71	VSS_168	AA14
R35	VSS_72	VSS_169	AK25
P35	VSS_73	VSS_170	P25
M35	VSS_74	VSS_171	K25
J35	VSS_75	VSS_172	H25
F35	VSS_76	VSS_173	E25
AV35	VSS_77	VSS_174	D25
AP35	VSS_78	VSS_175	A25
AN35	VSS_79	VSS_176	BA24
AK35	VSS_80	VSS_177	AL24
AM35	VSS_81	VSS_178	AW23
AH35	VSS_82	VSS_179	
AG35	VSS_83		
AF35	VSS_84		
AE35	VSS_85		
A40	VSS_86		
Y34	VSS_87		
W34	VSS_88		
V34	VSS_89		
T34	VSS_90		
R34	VSS_91		
P34	VSS_92		
M34	VSS_93		
J34	VSS_94		
F34	VSS_95		
AV34	VSS_96		

945GM

VSS

U32J

AT23	VSS_180	VSS_273	J11
AN23	VSS_181	VSS_274	D11
AM23	VSS_182	VSS_275	B11
AH23	VSS_183	VSS_276	AV10
AG23	VSS_184	VSS_277	AP10
AF23	VSS_185	VSS_278	AL10
A40	VSS_186	VSS_279	AG10
Y39	VSS_187	VSS_280	AC10
W39	VSS_188	VSS_281	W10
V39	VSS_189	VSS_282	U10
T39	VSS_190	VSS_283	BA9
R39	VSS_191	VSS_284	AW9
P39	VSS_192	VSS_285	AR9
M39	VSS_193	VSS_286	AH9
J39	VSS_194	VSS_287	AH9
F39	VSS_195	VSS_288	AY9
AV38	VSS_196	VSS_289	R9
AP38	VSS_197	VSS_290	G9
AN38	VSS_198	VSS_291	E9
AK38	VSS_199	VSS_292	AG9
AM38	VSS_200	VSS_293	AD9
AH38	VSS_201	VSS_294	AD8
AG38	VSS_202	VSS_295	AA8
AF38	VSS_203	VSS_296	UA8
AE38	VSS_204	VSS_297	K8
A40	VSS_205	VSS_298	BA7
Y37	VSS_206	VSS_299	AV7
W37	VSS_207	VSS_300	AP7
V37	VSS_208	VSS_301	AL7
T37	VSS_209	VSS_302	AJ7
R37	VSS_210	VSS_303	AH7
P37	VSS_211	VSS_304	AF7
M37	VSS_212	VSS_305	AC7
J37	VSS_213	VSS_306	R7
F37	VSS_214	VSS_307	G7
AV36	VSS_215	VSS_308	D7
AP36	VSS_216	VSS_309	AG6
AN36	VSS_217	VSS_310	AD6
AK36	VSS_218	VSS_311	AB6
AM36	VSS_219	VSS_312	Y6
AH36	VSS_220	VSS_313	U6
AG36	VSS_221	VSS_314	N6
AF36	VSS_222	VSS_315	K6
AE36	VSS_223	VSS_316	H6
A40	VSS_224	VSS_317	B6
Y35	VSS_225	VSS_318	AV5
W35	VSS_226	VSS_319	AD5
V35	VSS_227	VSS_320	AY4
T35	VSS_228	VSS_321	AR4
R35	VSS_229	VSS_322	AP4
P35	VSS_230	VSS_323	AL4
M35	VSS_231	VSS_324	AJ4
J35	VSS_232	VSS_325	U4
F35	VSS_233	VSS_326	R4
AV34	VSS_234	VSS_327	J4
AP34	VSS_235	VSS_328	C4
AN34	VSS_236	VSS_329	F4
AK34	VSS_237	VSS_330	AY3
AM34	VSS_238	VSS_331	AV3
AH34	VSS_239	VSS_332	AL3
AG34	VSS_240	VSS_333	AH3
AF34	VSS_241	VSS_334	AG3
AE34	VSS_242	VSS_335	AF3
A40	VSS_243	VSS_336	AD3
Y33	VSS_244	VSS_337	AC3
W33	VSS_245	VSS_338	G3
V33	VSS_246	VSS_339	AT2
T33	VSS_247	VSS_340	AR2
R33	VSS_248	VSS_341	AK2
P33	VSS_249	VSS_342	AJ2
M33	VSS_250	VSS_343	AD2
J33	VSS_251	VSS_344	Y2
F33	VSS_252	VSS_345	U2
AV32	VSS_253	VSS_346	T2
AP32	VSS_254	VSS_347	N2
AN32	VSS_255	VSS_348	J2
AK32	VSS_256	VSS_349	H2
AM32	VSS_257	VSS_350	F2
AH32	VSS_258	VSS_351	C2
AG32	VSS_259	VSS_352	AL1
AF32	VSS_260	VSS_353	
AE32	VSS_261	VSS_354	
A40	VSS_262	VSS_355	
Y31	VSS_263	VSS_356	
W31	VSS_264	VSS_357	
V31	VSS_265	VSS_358	
T31	VSS_266	VSS_359	
R31	VSS_267	VSS_360	
P31	VSS_268		
M31	VSS_269		
J31	VSS_270		
F31	VSS_271		
AV30	VSS_272		

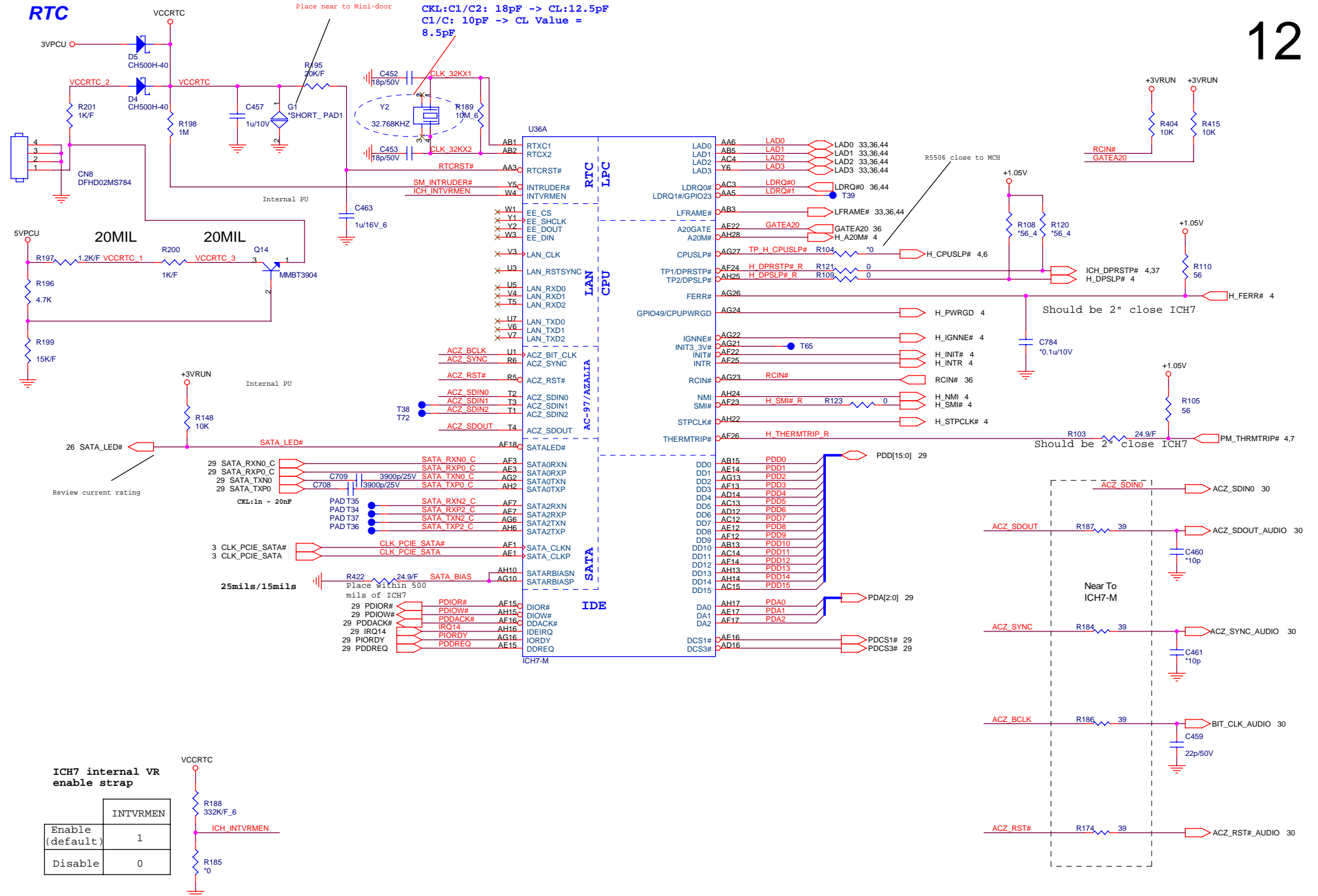
945GM

VSS

**PROJECT : TW3**  
**Quanta Computer Inc.**

Size	Document Number	Rev
	Calistoga_F(VSS, NCTF)	B2A
Date:	Tuesday, April 18, 2006	Sheet 11 of 48

## RTC



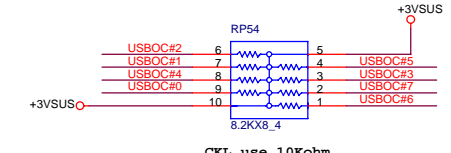
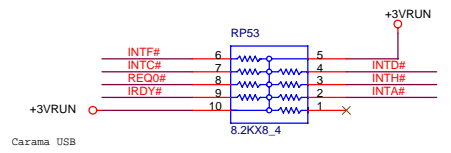
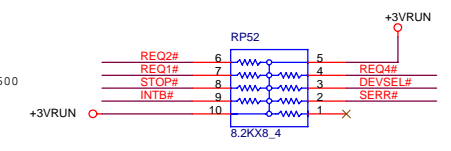
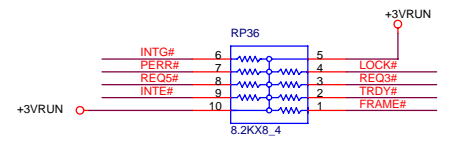
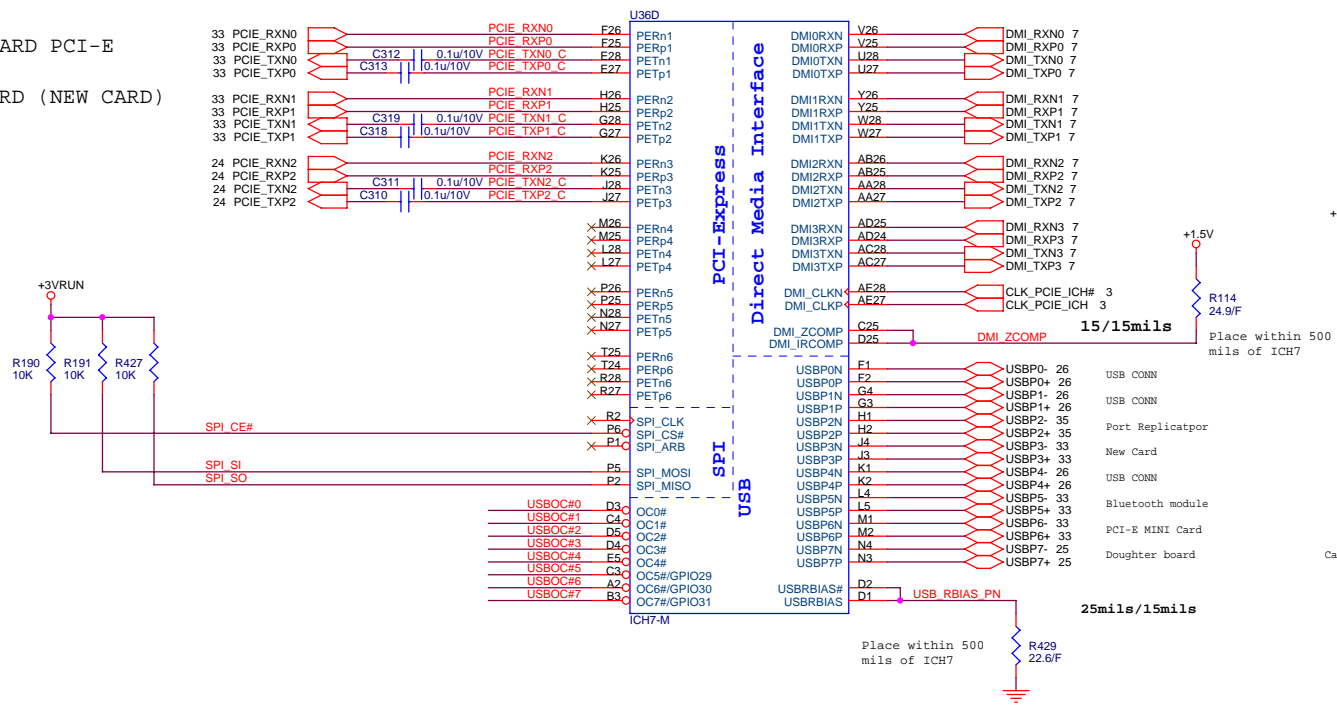
ICH7 internal VR enable strap

	INTVRMEN
Enable (default)	1
Disable	0

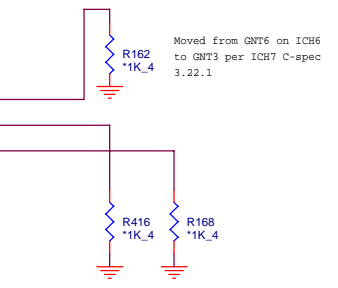
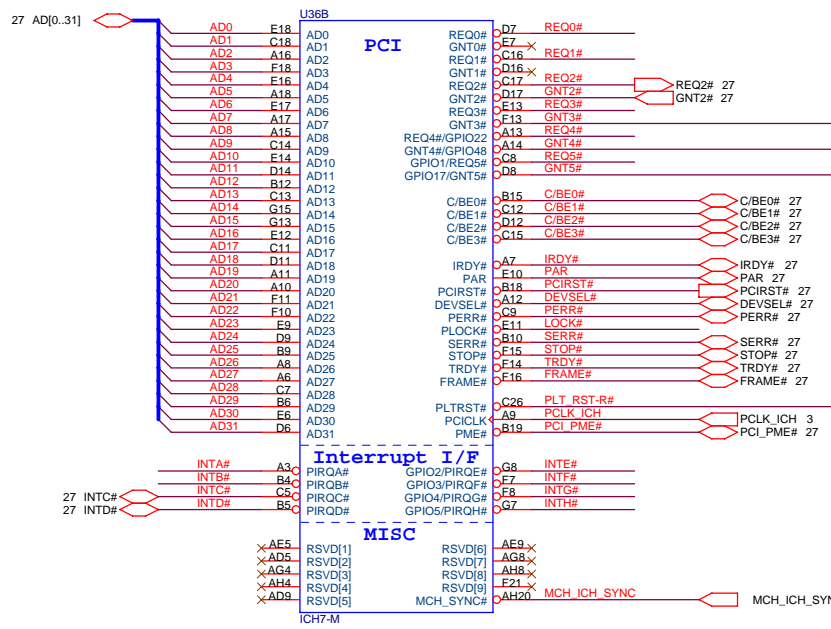
**PROJECT : TW3**  
**Quanta Computer Inc.**

Size	Document Number	Rev
	ICH7-M HOST(1 of 4)	B2A
Date:	Tuesday, April 18, 2006	Sheet 12 of 48

MINI CARD PCI-E  
EXPRESS CARD (NEW CARD)

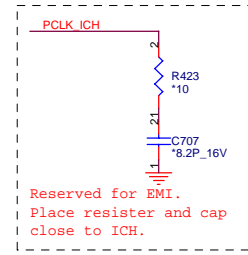


CKL use 10Kohm

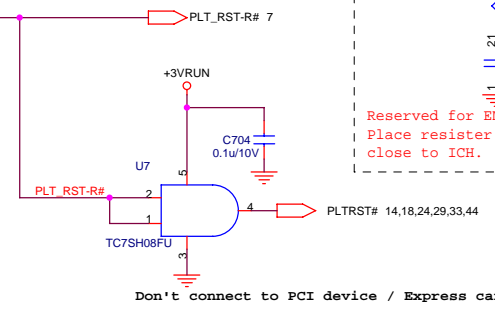


ICH7 Boot BIOS select

	STRAP	GNT5# R1	GNT4# R2
LPC (default)	11	UNSTUFF	UNSTUFF
PCI	10	UNSTUFF	STUFF
SPI	01	STUFF	UNSTUFF



Reserved for EMI.  
Place resistor and cap  
close to ICH.

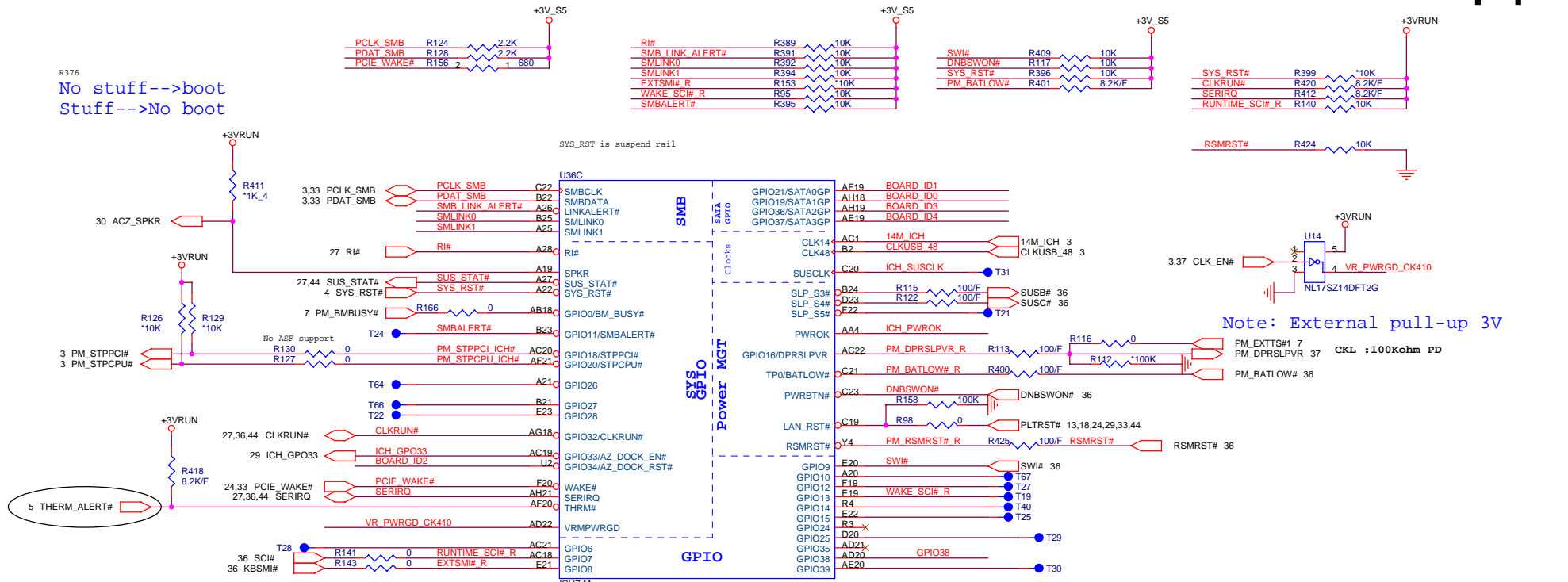


Don't connect to PCI device / Express card

**PROJECT : TW3**  
**Quanta Computer Inc.**

Size	Document Number	Rev
	ICH7-M PCI E(2 of 4)	B2A
Date:	Tuesday, April 18, 2006	Sheet 13 of 48

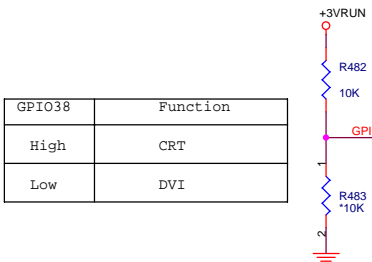
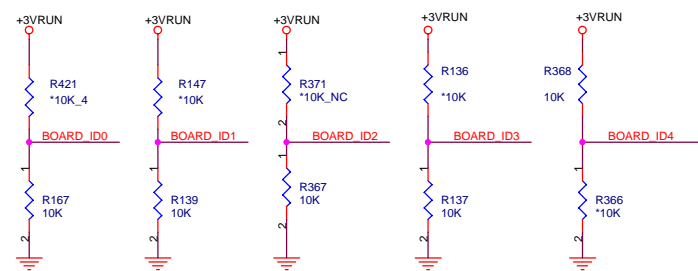
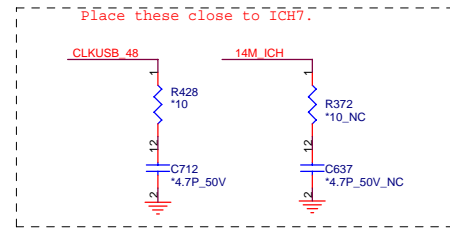
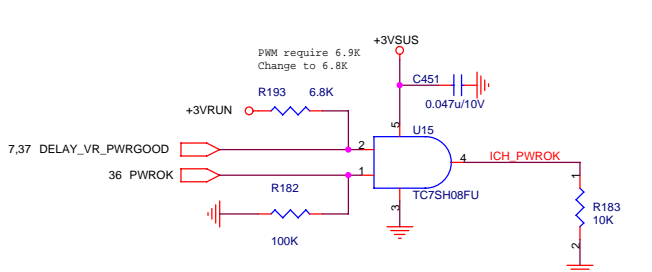
R376  
No stuff-->boot  
Stuff-->No boot



Note: External pull-up 3V

CKL :100Kohm PD

GPIO25 /Suspend rail is a HW strap , don't pull down .

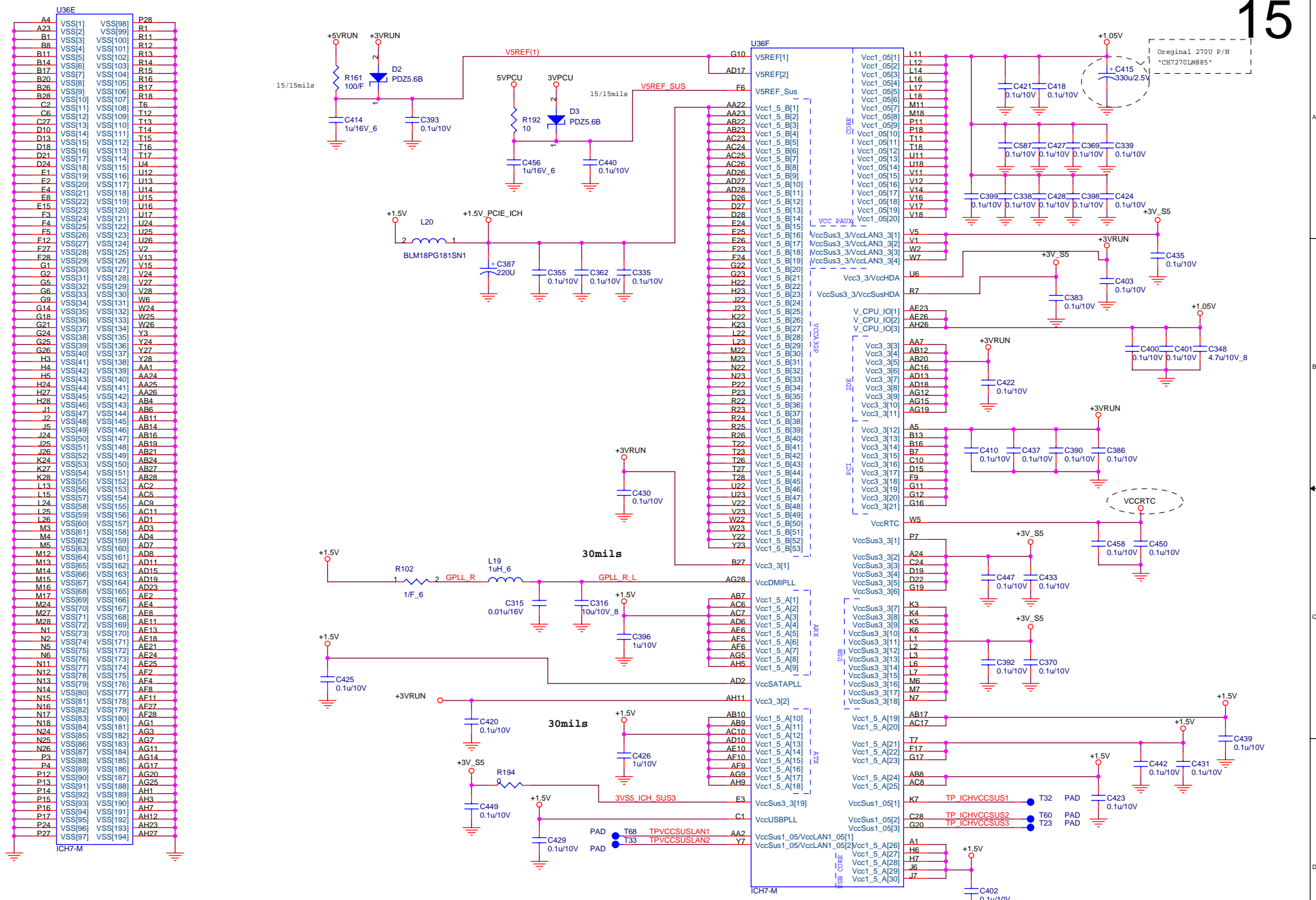


GPIO38	Function
High	CRT
Low	DVI

Board ID	Function
ID [1:0]	00: TW3 01: DW1
ID2	0: SATA HDD 1: PATA HDD
ID3	Reserve
ID4	0: No docking. 1: w/ docking

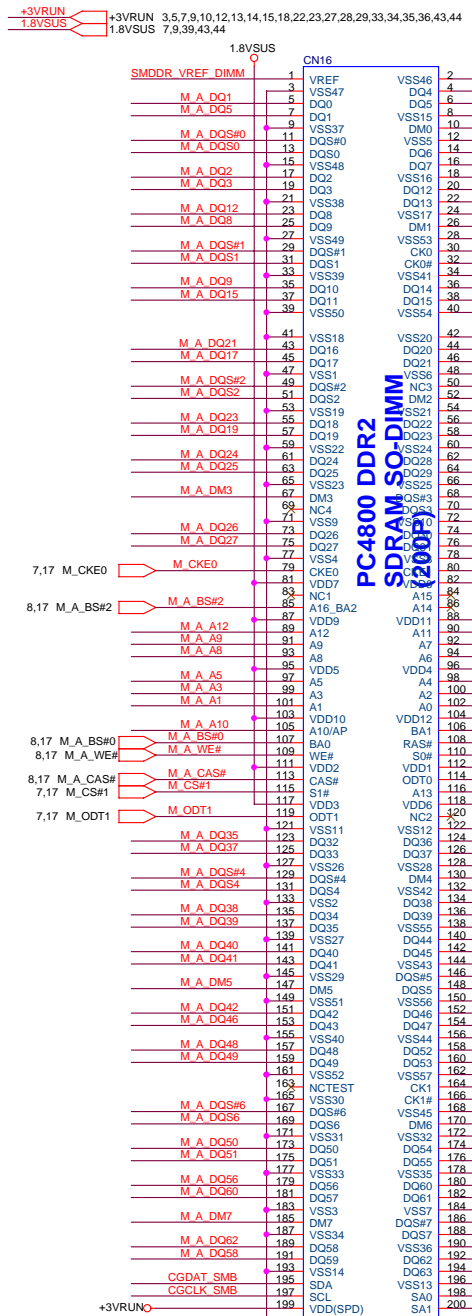
**PROJECT : TW3**  
**Quanta Computer Inc.**

Size	Document Number	Rev
	ICH7-M GPIO(3 of 4)	B2A
Date:	Tuesday, April 18, 2006	Sheet 14 of 48



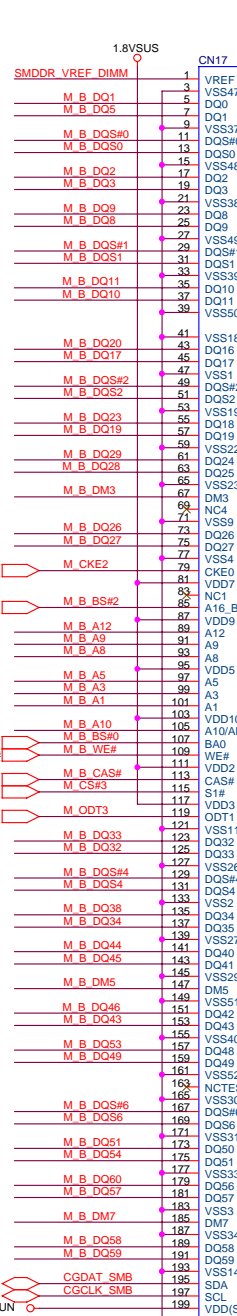
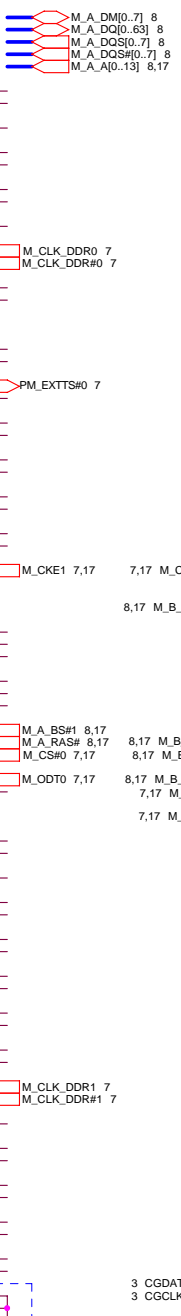
**PROJECT : TW3**  
**Quanta Computer Inc.**

Size	Document Number	Rev
	<b>ICH7-M POWER(4 of 4)</b>	B2A
Date:	Tuesday, April 18, 2006	Sheet 15 of 48



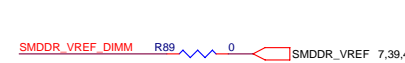
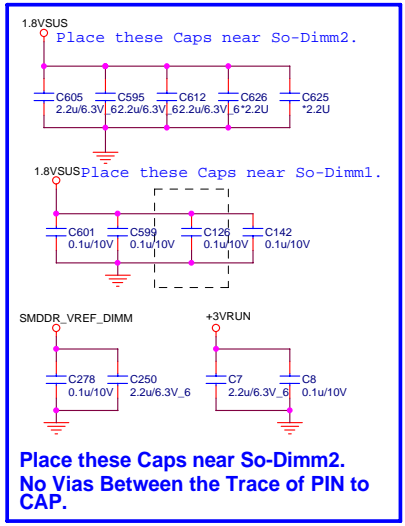
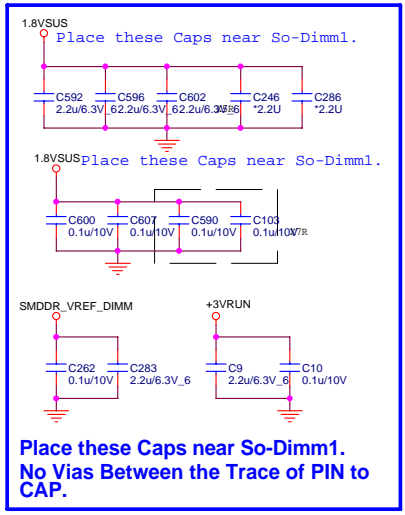
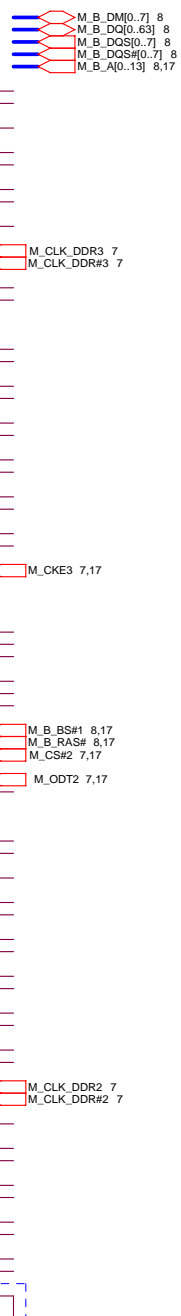
**PC4800 DDR2  
SDRAM SO-DIMM**

CLOCK 0,1  
CKE 0,1 H 5.2  
SMBus address A0



**PC4800 DDR2  
SDRAM SO-DIMM**

CLOCK 3,4  
CKE 2,3 H 9.2  
SMBus address A4



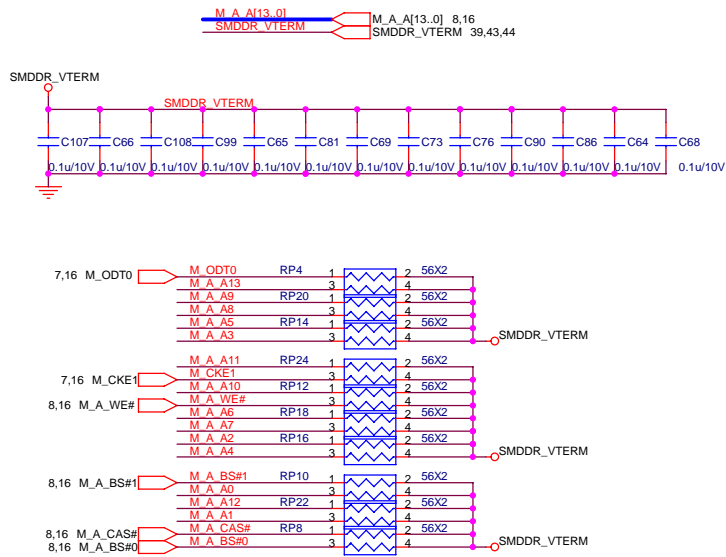
Add for memory margin --Allen /0228

**PROJECT : TW3**  
**Quanta Computer Inc.**  
 Size Document Number Rev B2A  
**DDRII SO-DIMM(200P)**  
 Date: Tuesday, April 18, 2006 Sheet 16 of 48

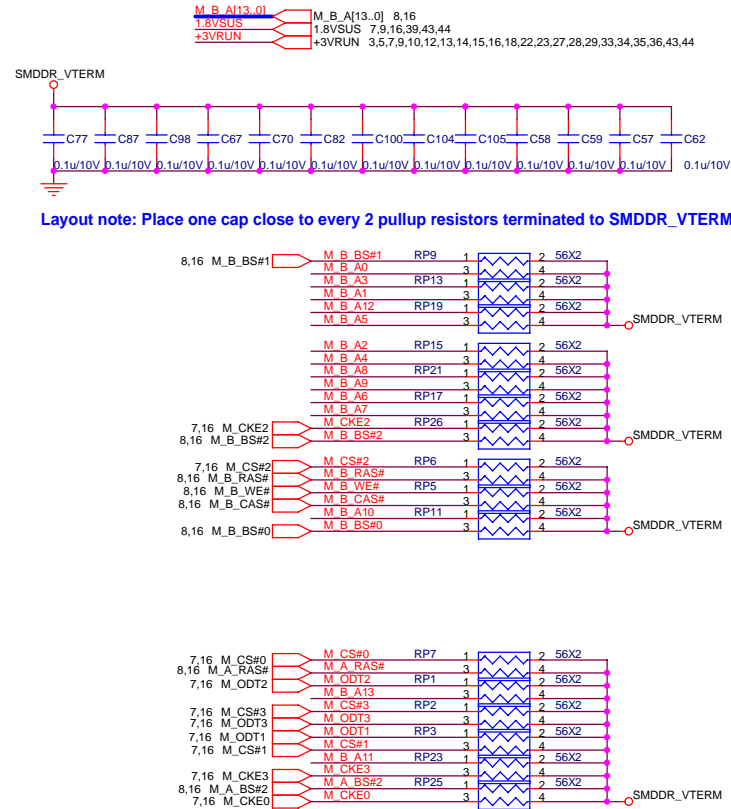


# DDRII DUAL CHANNEL A,B.


## DDRII A CHANNEL



## DDRII B CHANNEL

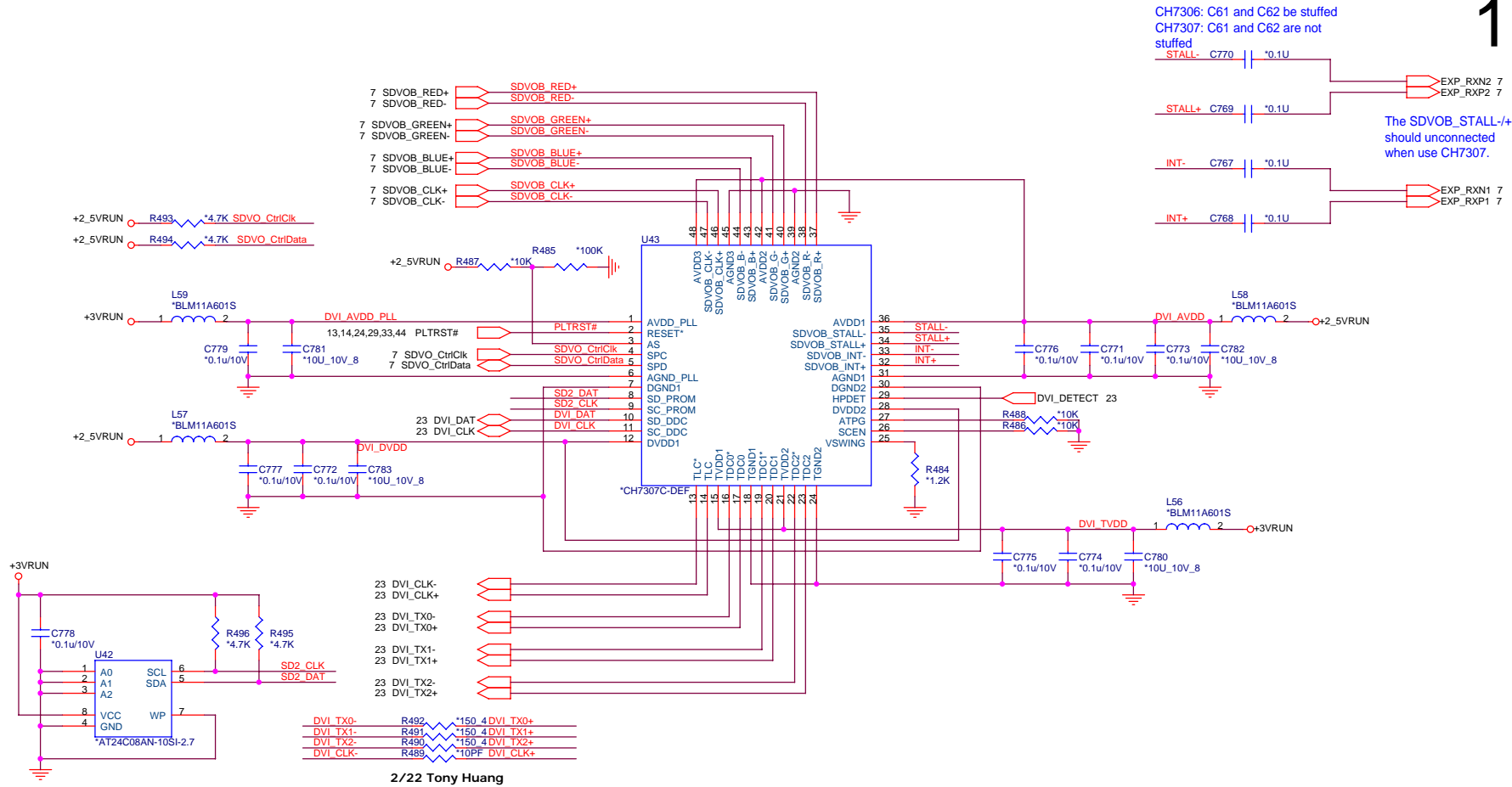


Layout note: Place one cap close to every 2 pullup resistors terminated to SMDDDR\_VTERM


**PROJECT : TW3**  
**Quanta Computer Inc.**

Size	Document Number	Rev
	DDRII TERMINATION	B2A
Date:	Tuesday, April 18, 2006	Sheet 17 of 48

# GMCH SDVO Signal to DVI Signal Bridge





PROJECT : TW3  
Quanta Computer Inc.

Size	Document Number	Rev
Empty		B2A
Date:	Tuesday, April 18, 2006	Sheet 19 of 48

5

4

3

2

1

D

D

C


C

B

B

A

A

		<b>PROJECT : TW3</b> <b>Quanta Computer Inc.</b>	
Date: Tuesday, April 18, 2006		Sheet 20 of 48	

5

4

3

2

1

5

4

3

2

1

D

D

C


C

B

B

A

A

 <b>PROJECT : TW3</b> <b>Quanta Computer Inc.</b>		Rev
		B2A
Size	Document Number	
	Empty	
Date:	Tuesday, April 18, 2006	Sheet 21 of 48

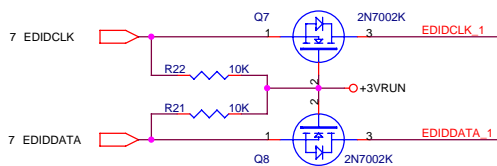
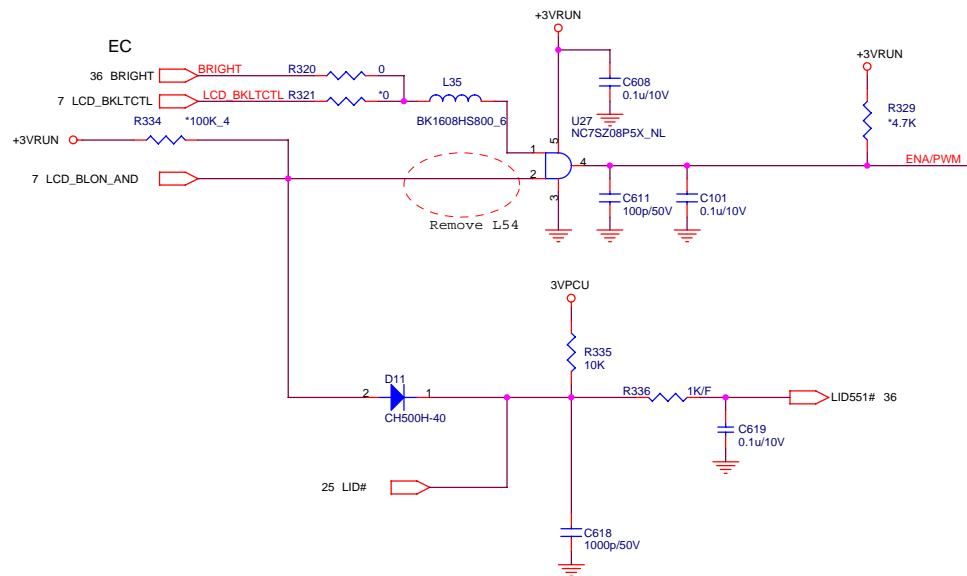
5

4

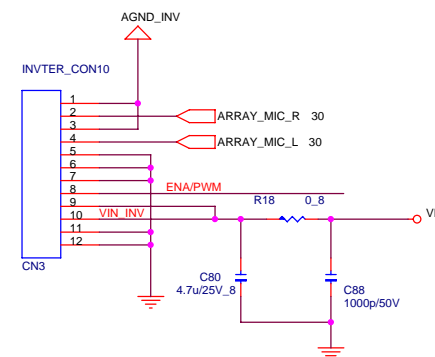
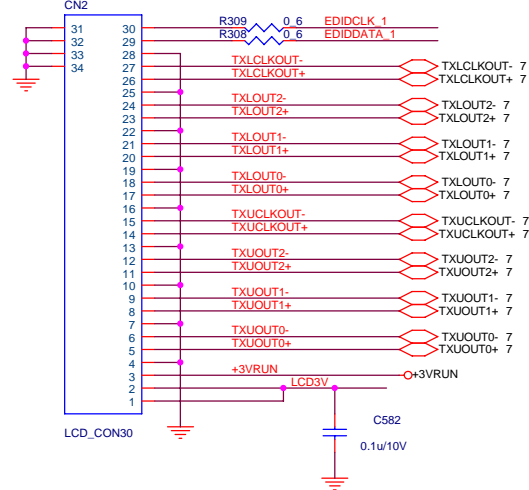
3

2

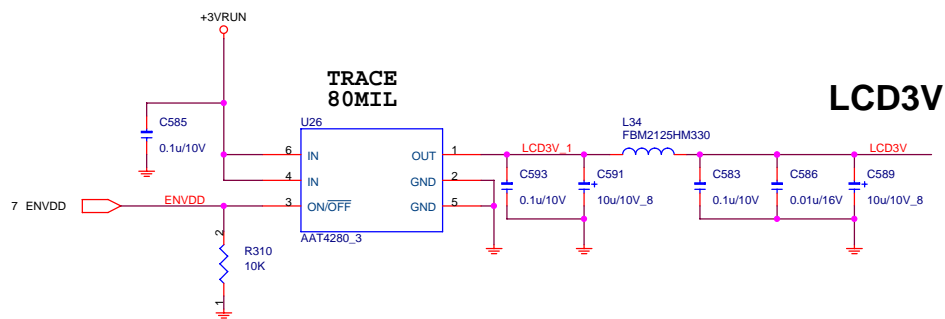
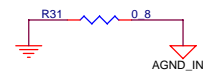
1



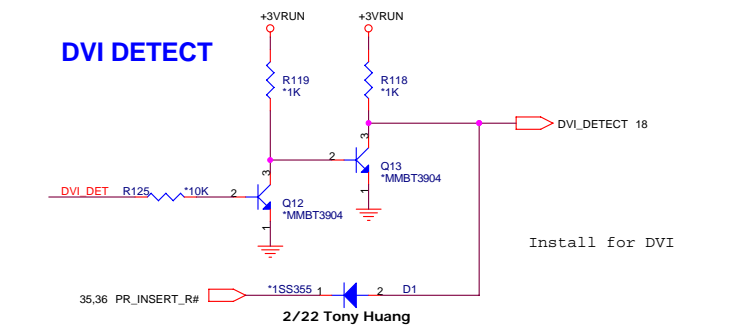
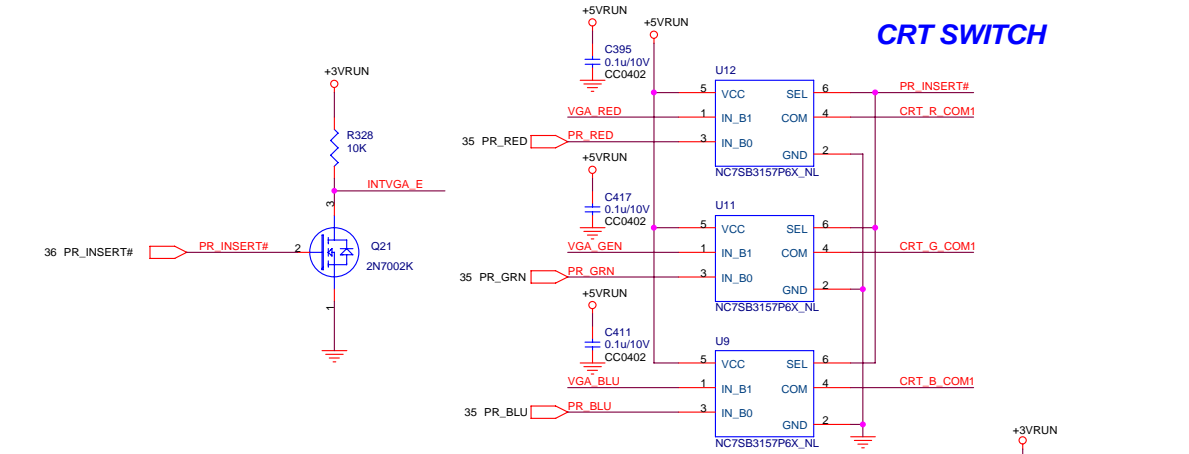
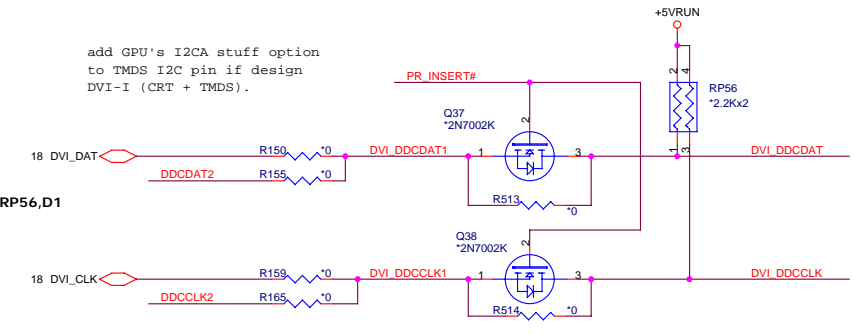
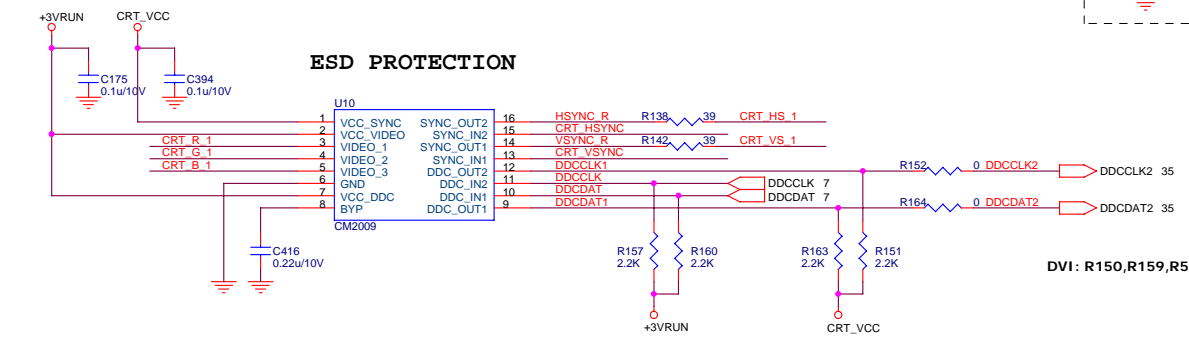
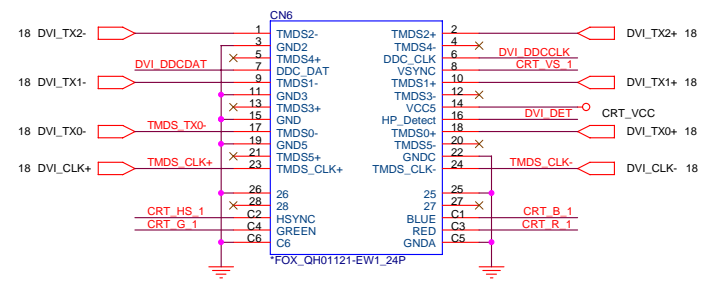
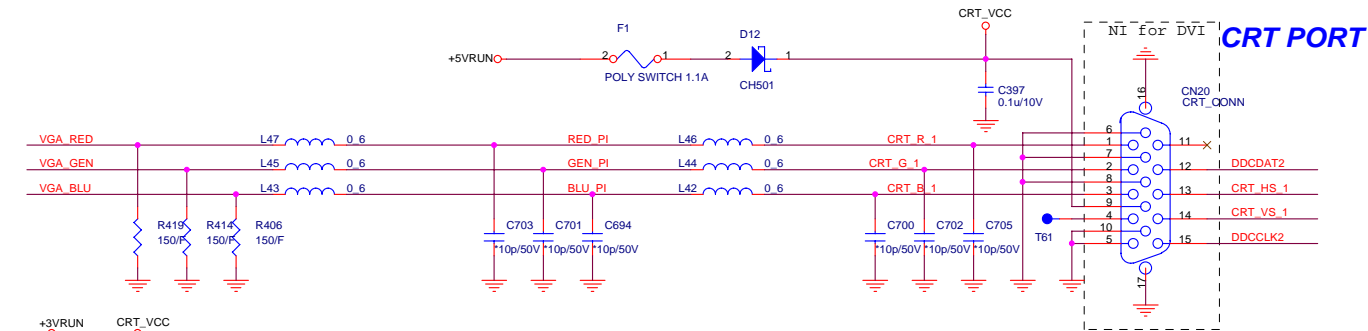
## LVDS Interface



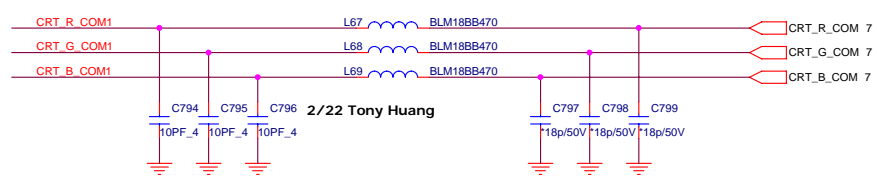
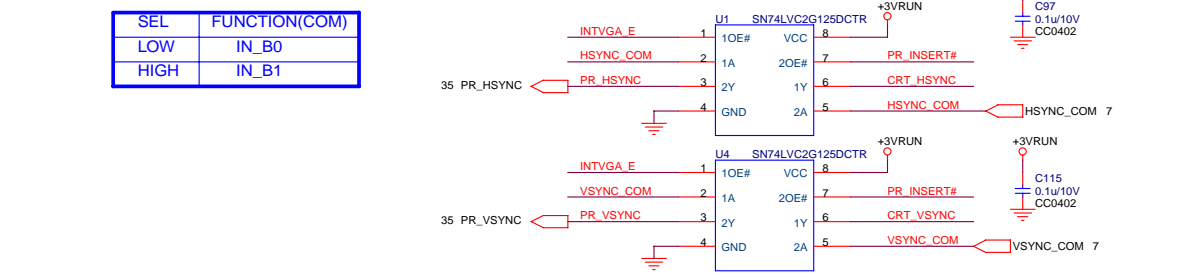
Inverter Interface



## LCD3V



SEL	FUNCTION(COM)
LOW	IN_B0
HIGH	IN_B1

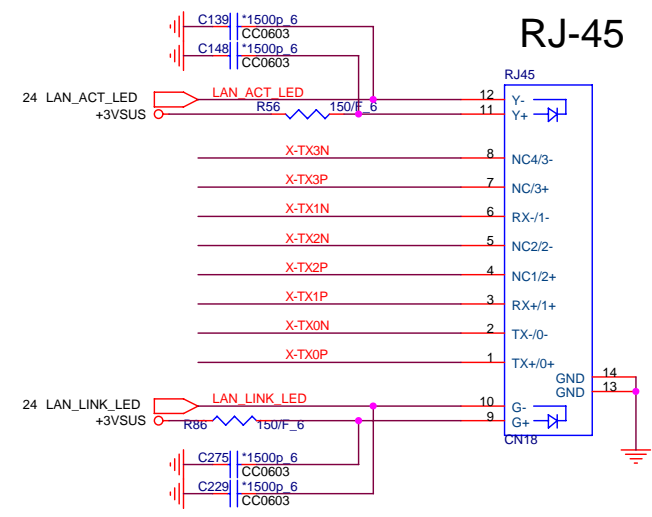
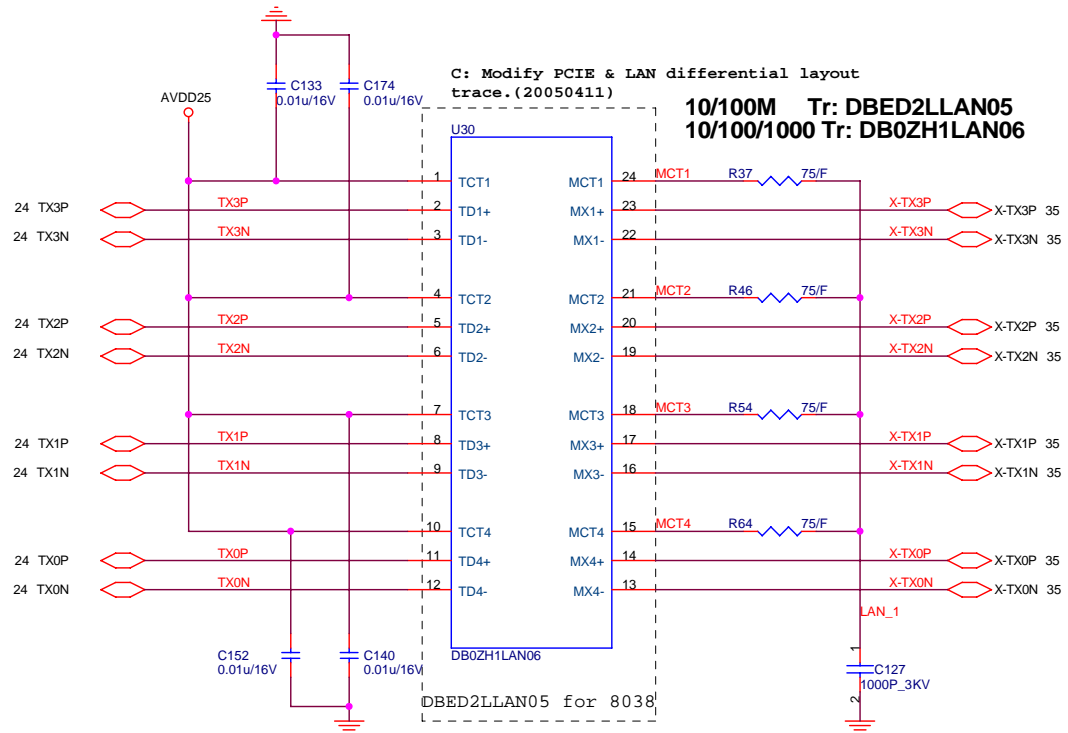


**PROJECT : TW3**  
**Quanta Computer Inc.**

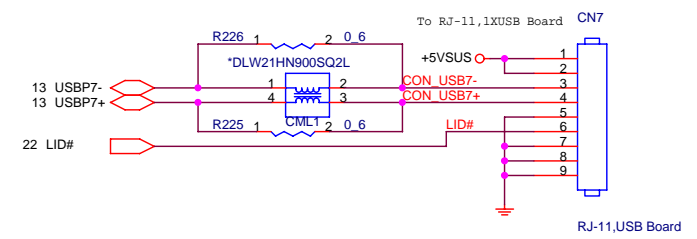
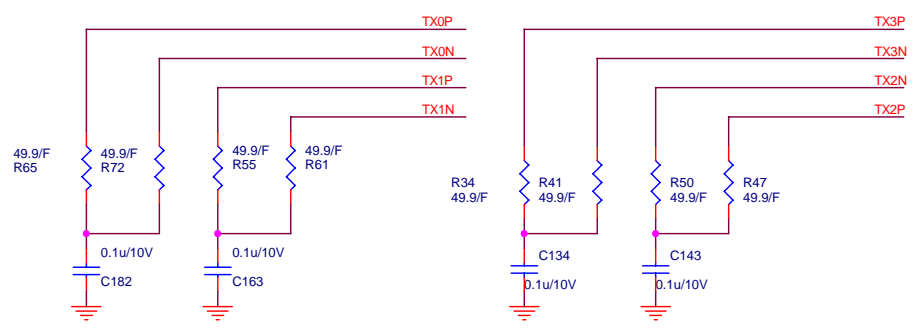
Size: Document Number: CRT\_TV-OUT,DVI\_CONN Rev: B2A  
 Date: Tuesday, April 18, 2006 Sheet: 23 of 48





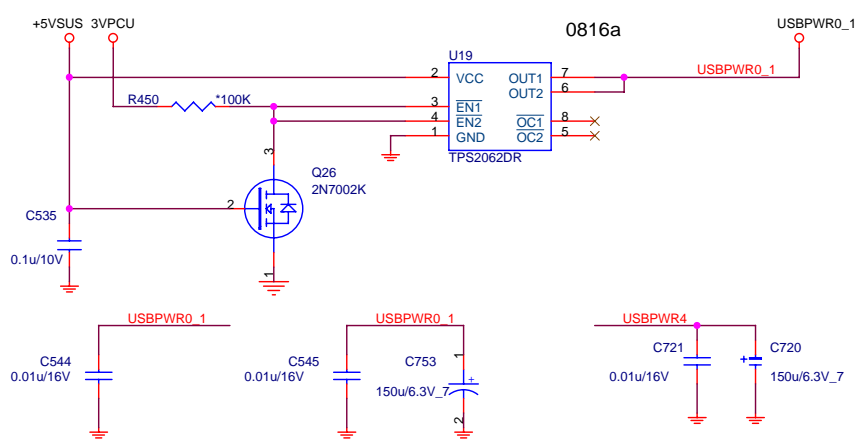


**GigaLAN transformer**

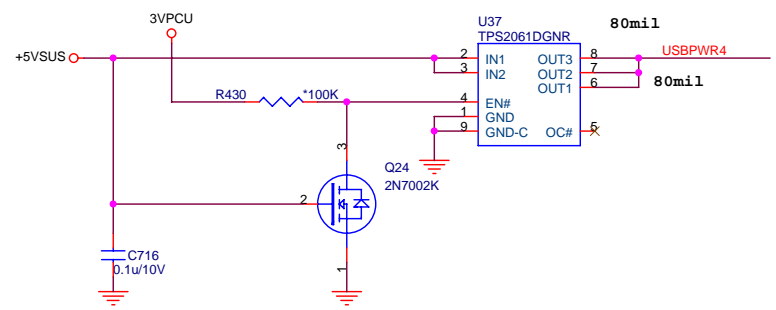


**PROJECT : TW3**  
**Quanta Computer Inc.**

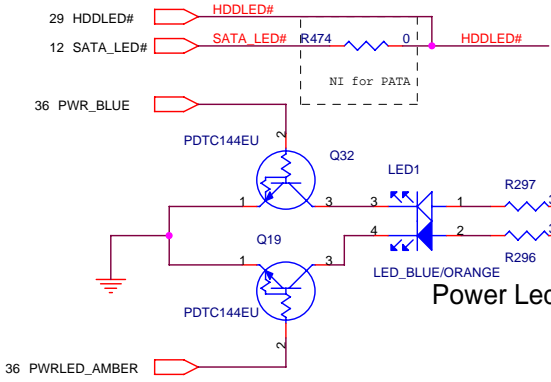
Size	Document Number	Rev
	<b>LAN SW CONN&amp; MDC CONN</b>	B2A
Date:	Tuesday, April 18, 2006	Sheet 25 of 48



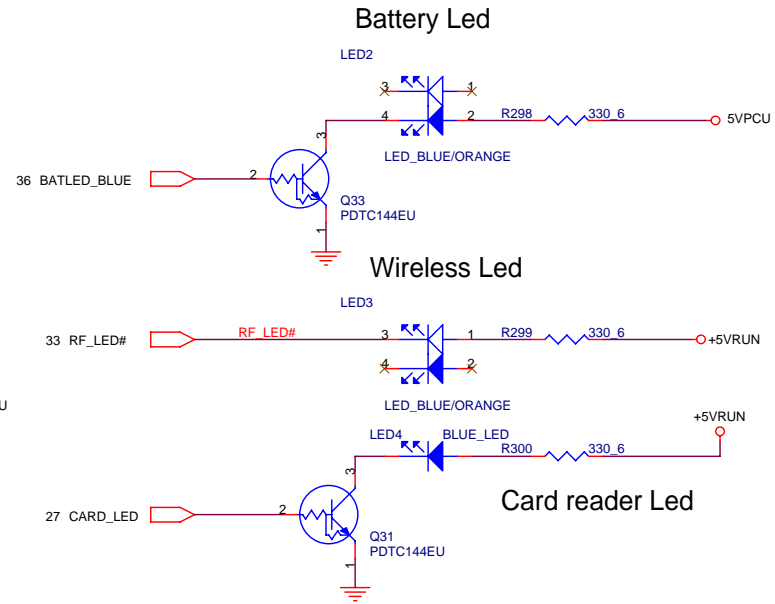
C:Change U1 from G528 to TPS2061



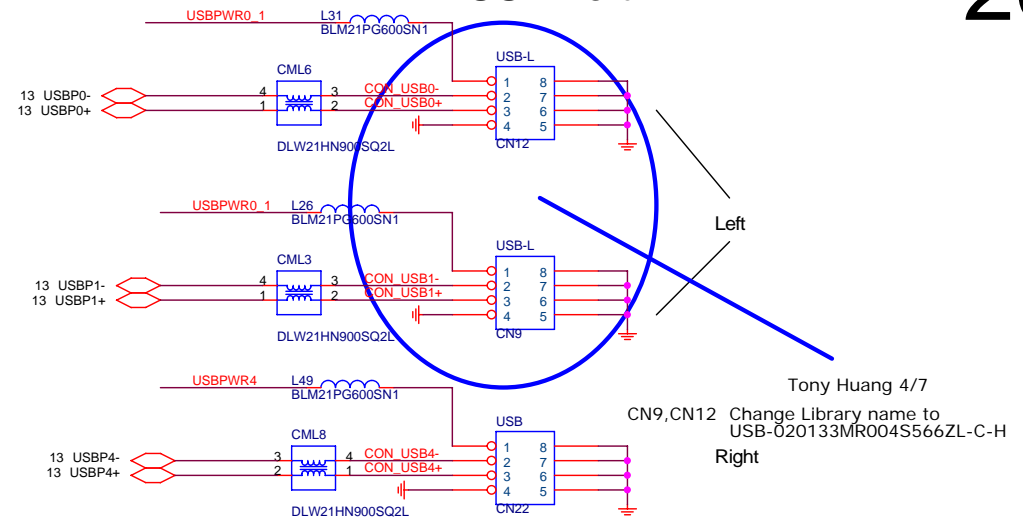
### HDD,SATA Led



### Power Led

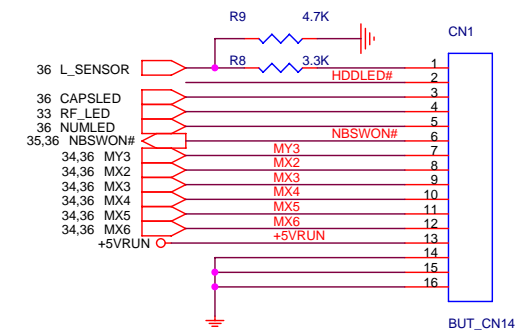


### USB Port



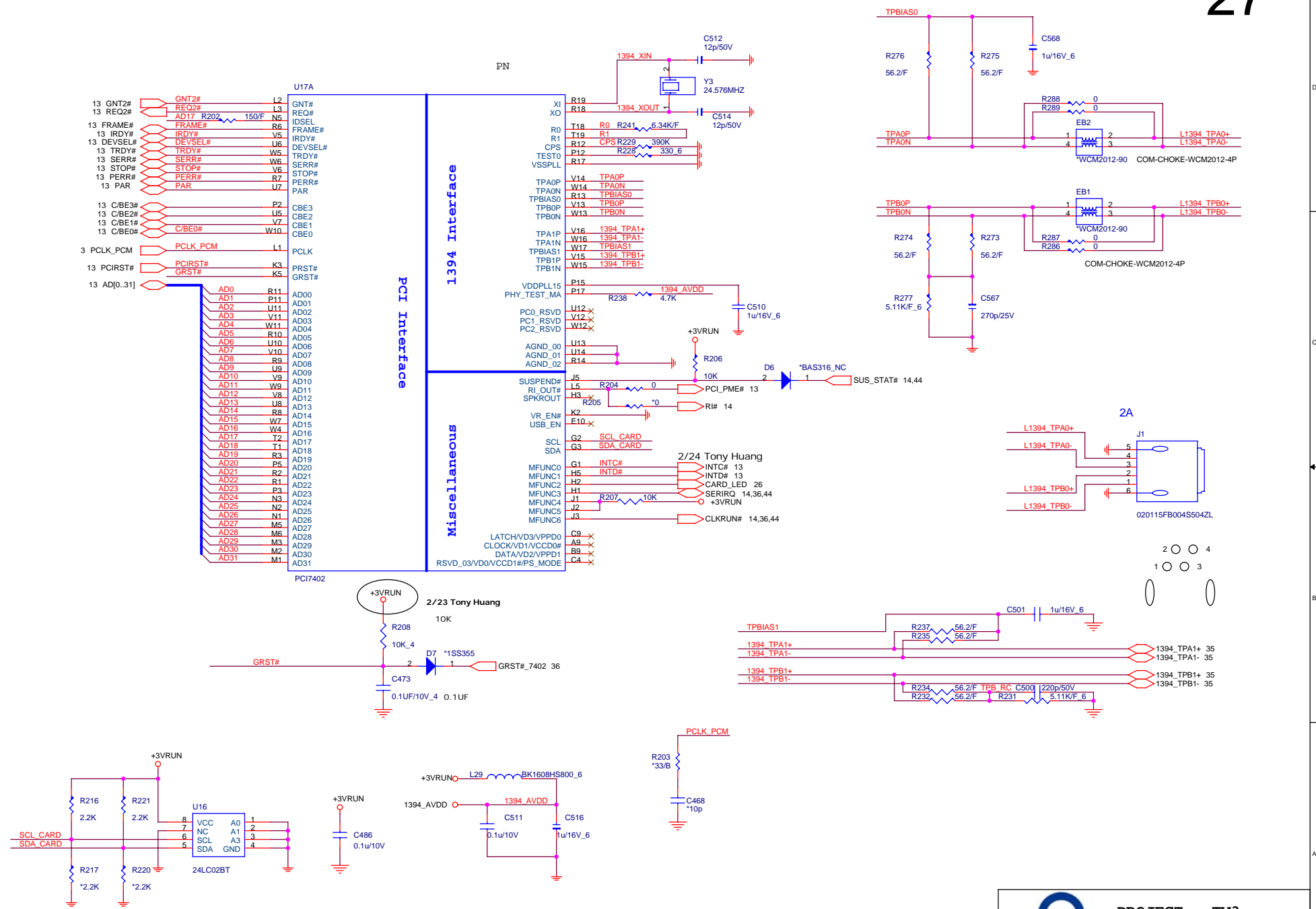
Tony Huang 4/7  
 CN9,CN12 Change Library name to  
 USB-020133MR004S566ZL-C-H  
 Right

### For Botton Board



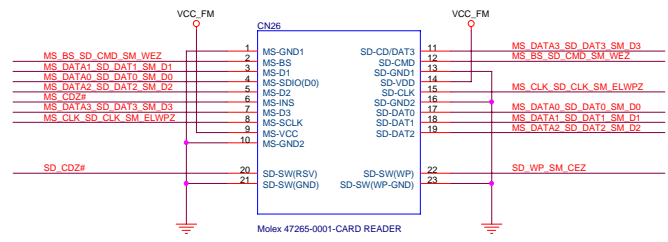
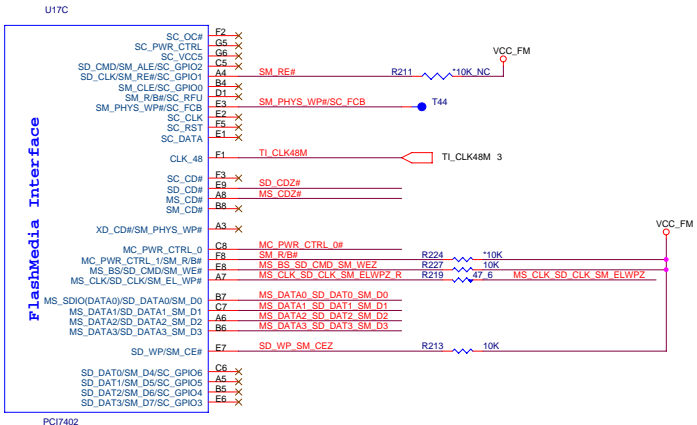
**PROJECT : TW3**  
**Quanta Computer Inc.**

Size	Document Number	Rev
	<b>USB,LED,Buttom/B</b>	B2A
Date:	Tuesday, April 18, 2006	Sheet 26 of 48

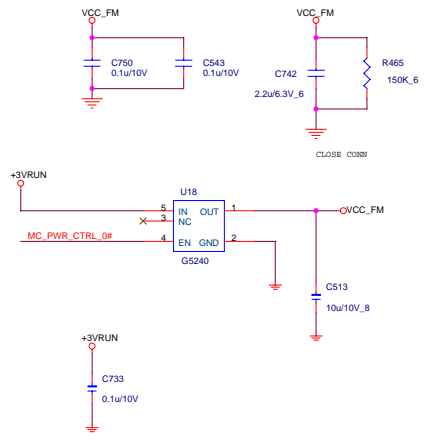
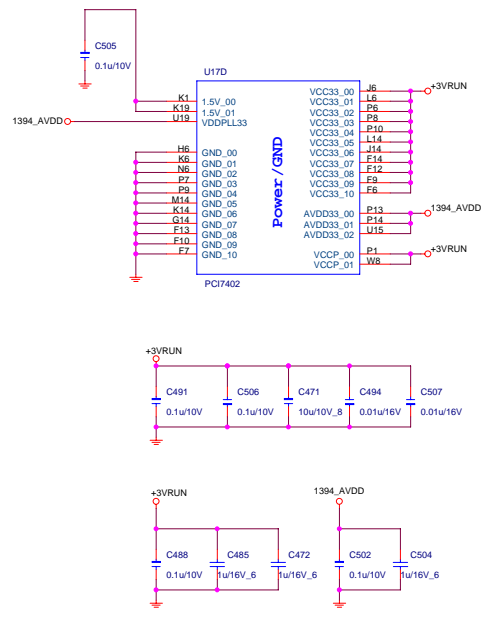
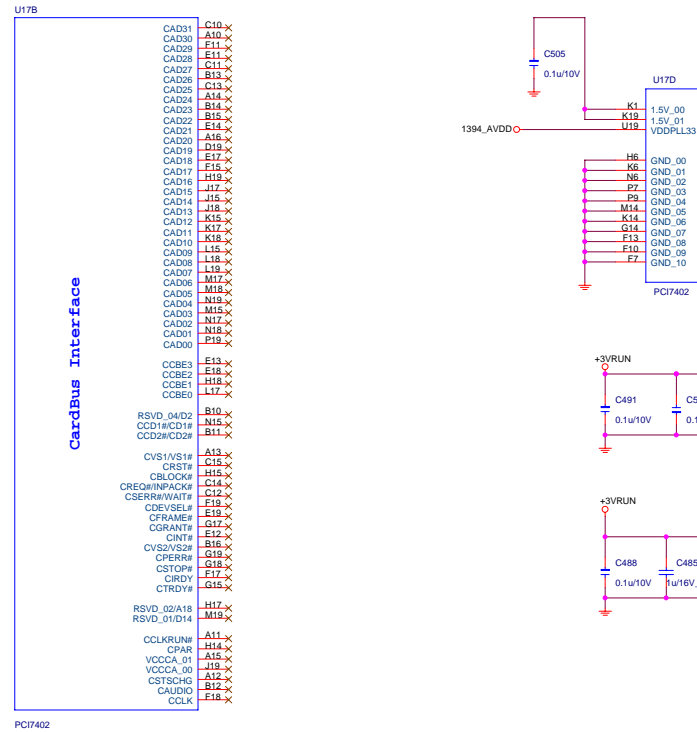


DO NOT INSERT SD/MMC, MEMORYSTICK AND XD SIMULTANEOUSLY.

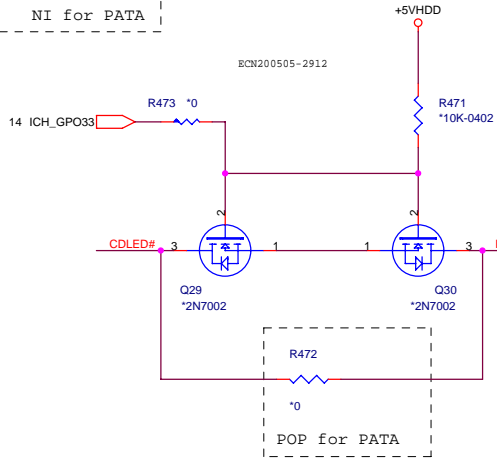
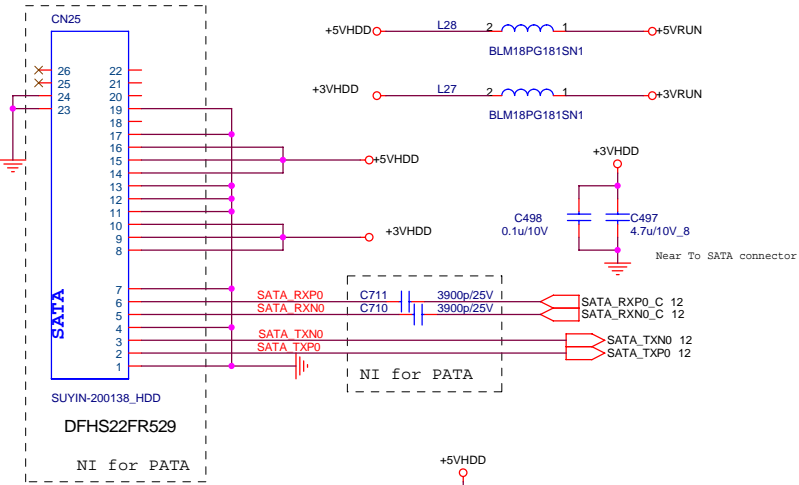
### 3 IN1 CARD READER (push-push)



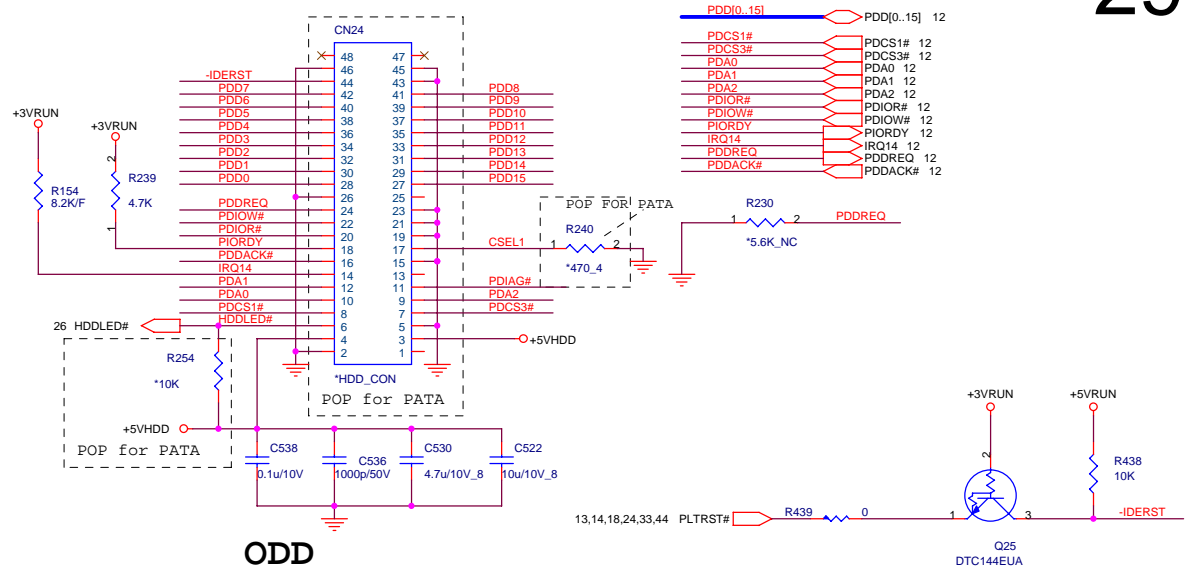
Supporting MMC/SD/MS Cards  
 M01EX P7/N7/DF/ID.2.3MS/UB6



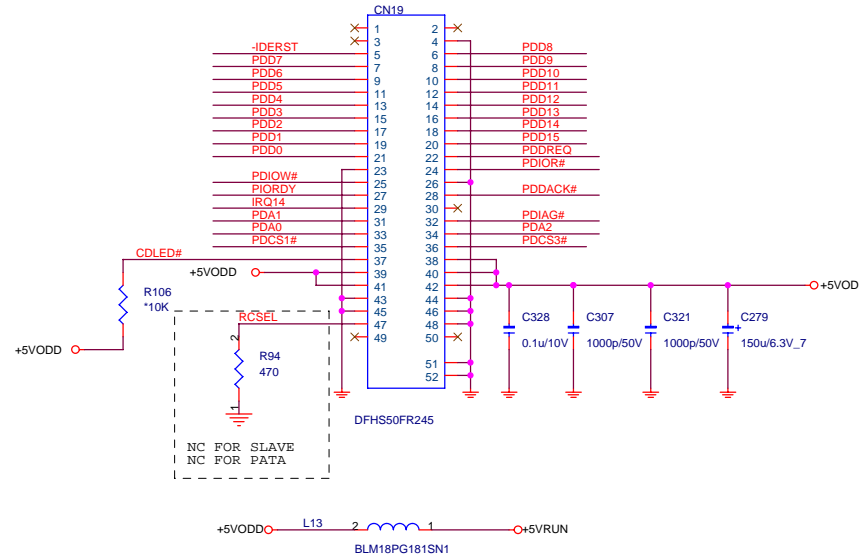
## SATA HDD



## PATA HDD

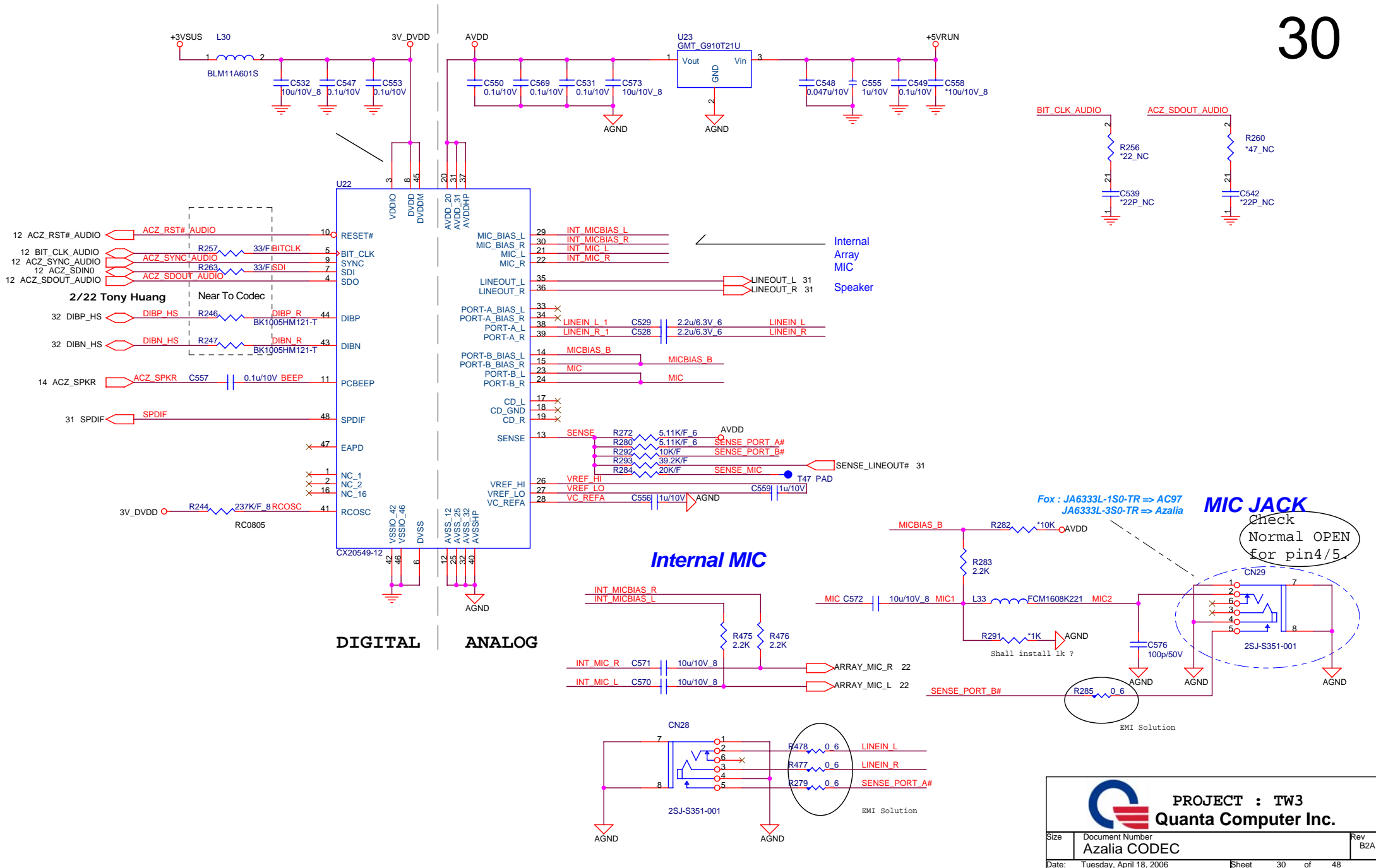


## ODD



FOR PATA HDD

CN19	NI
C730	NI
C729	NI
CN18	HDD CON
R517	NI
Q25	2N7002
Q26	2N7002
R513	10K
R512	0
R168	470



Fox : JA6333L-1S0-TR => AC97  
 JA6333L-3S0-TR => Azalia

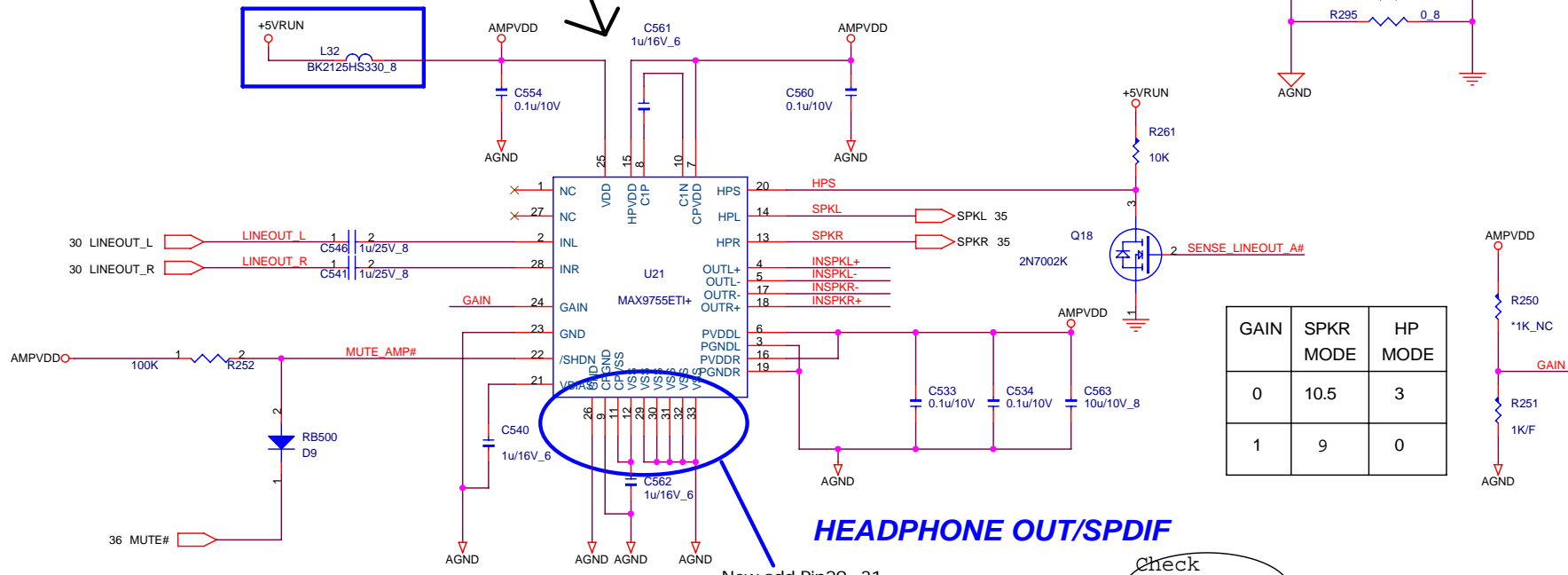
**PROJECT : TW3**  
**Quanta Computer Inc.**

Size	Document Number	Rev
	Azalia CODEC	B2A
Date:	Tuesday, April 18, 2006	Sheet 30 of 48

Modify Library to QFN28-5X5-5-33P(Add thermal Pad) 04/06/2006 by Tony Huang

04062006

EAPD  
low:mute

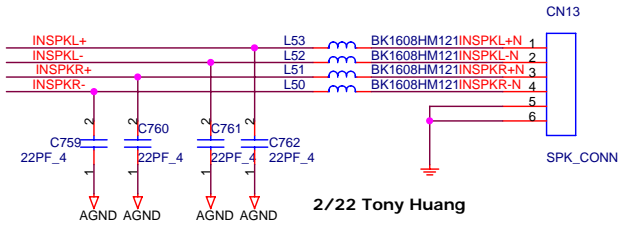


**HEADPHONE OUT/SPDIF**

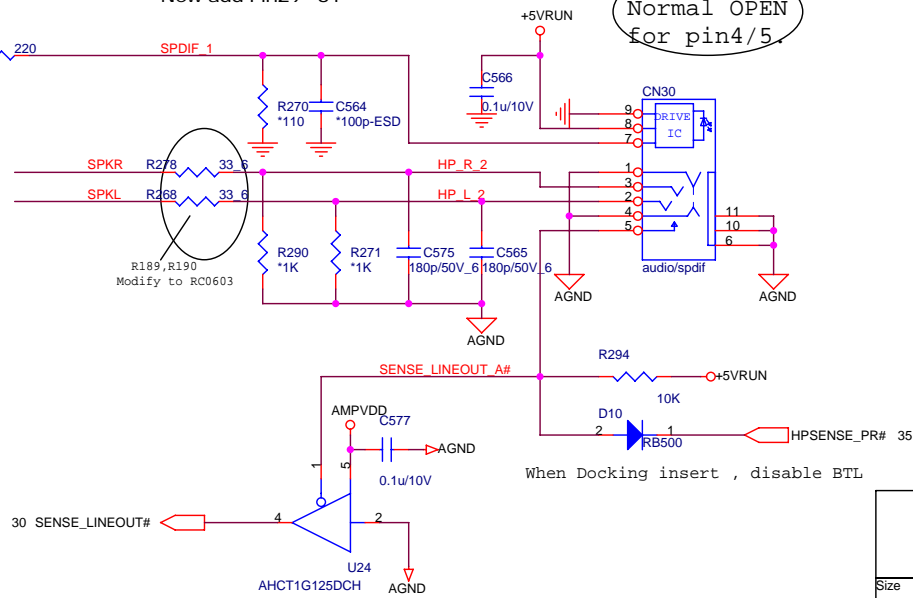
New add Pin29~31

Check Normal OPEN for pin4/5.

**SPEAKER CON.**



2/22 Tony Huang



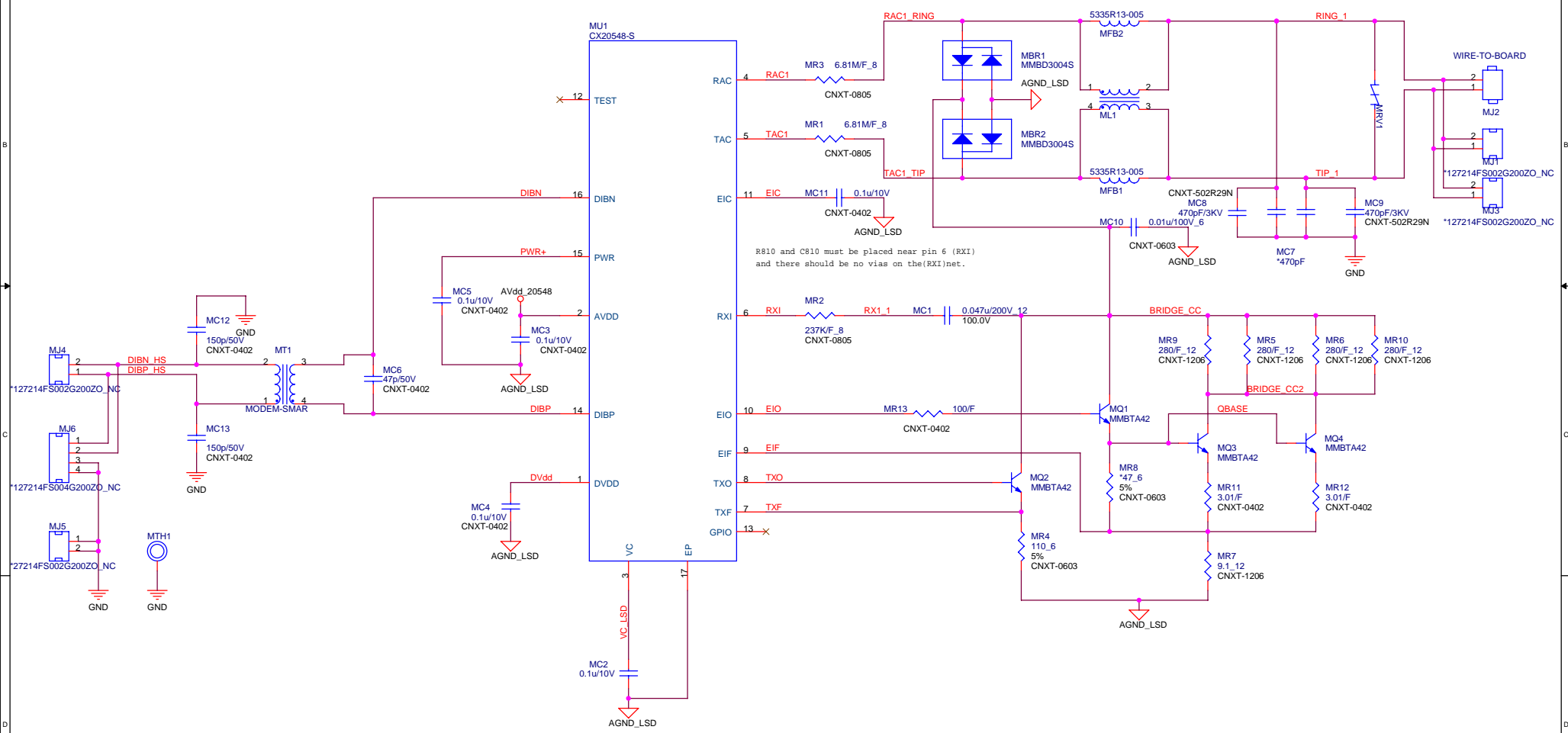
**PROJECT : TW3**  
**Quanta Computer Inc.**

Size	Document Number	Rev
	<b>AUDIO AMPLIFIER</b>	B2A
Date:	Tuesday, April 18, 2006	Sheet 31 of 48

## Revision History

REV	Description	Date
0	Initial Release	April 26, 2005

30 DIBN\_HS  
30 DIBP\_HS



**PROJECT : TW3**

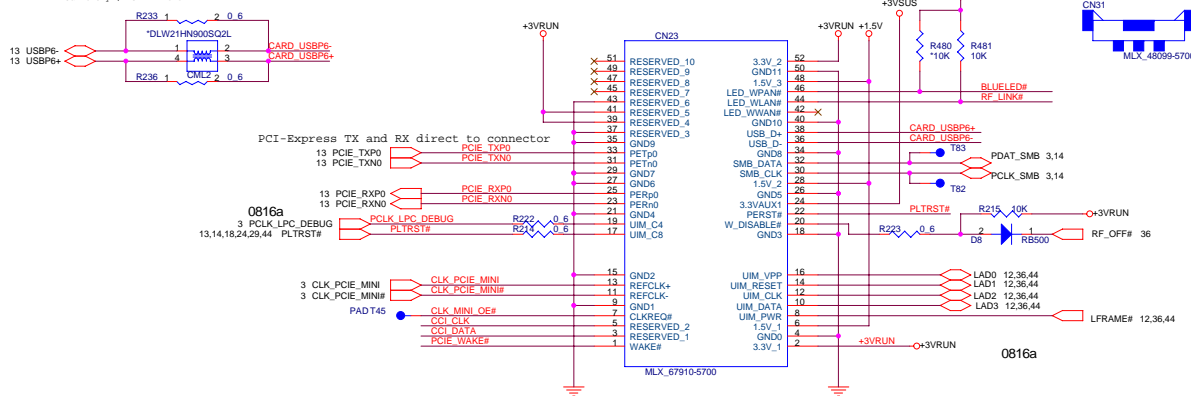
**Quanta Computer Inc.**

Size	Document Number	Rev
<b>Conexant Modem</b>		B2A
Date:	Tuesday, April 18, 2006	Sheet 32 of 48

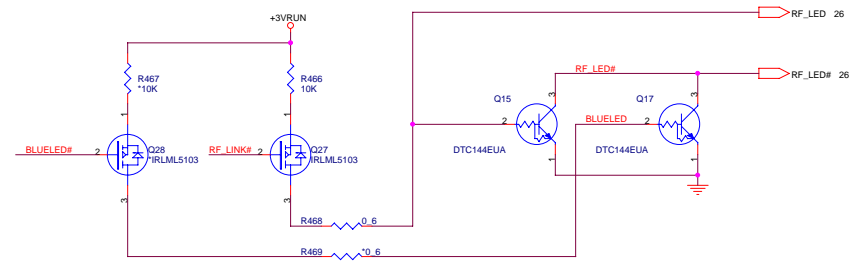
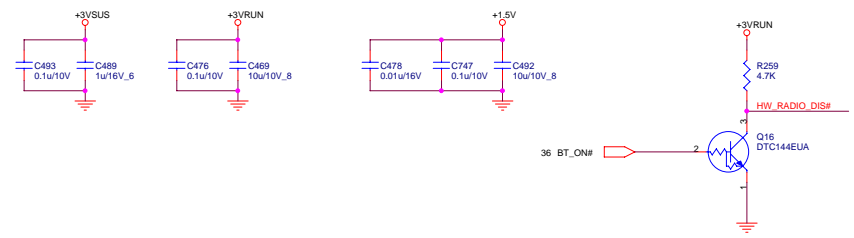
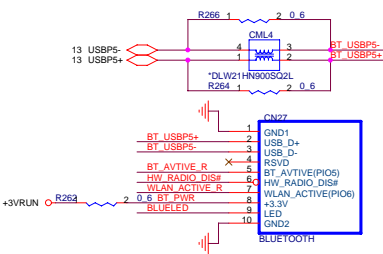


PCI-E Mini Card

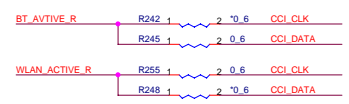
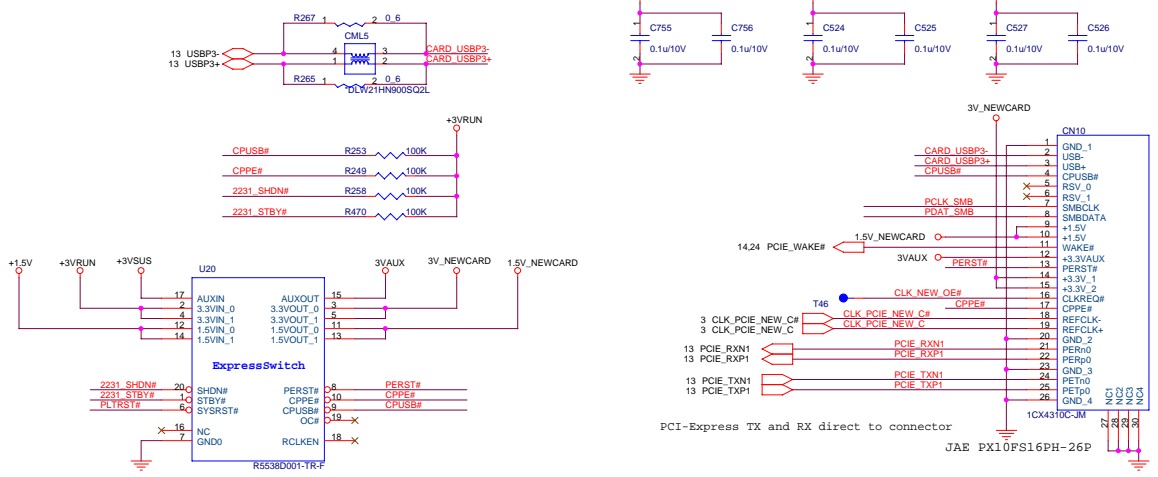
Need one more wireless LED /mini card on MB ? currently , No LED here



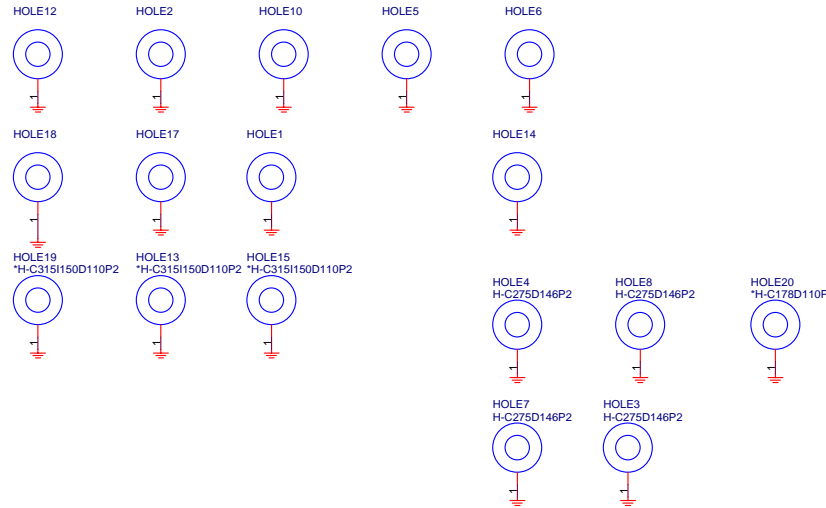
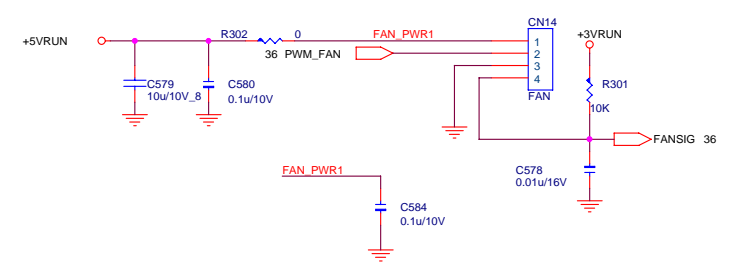
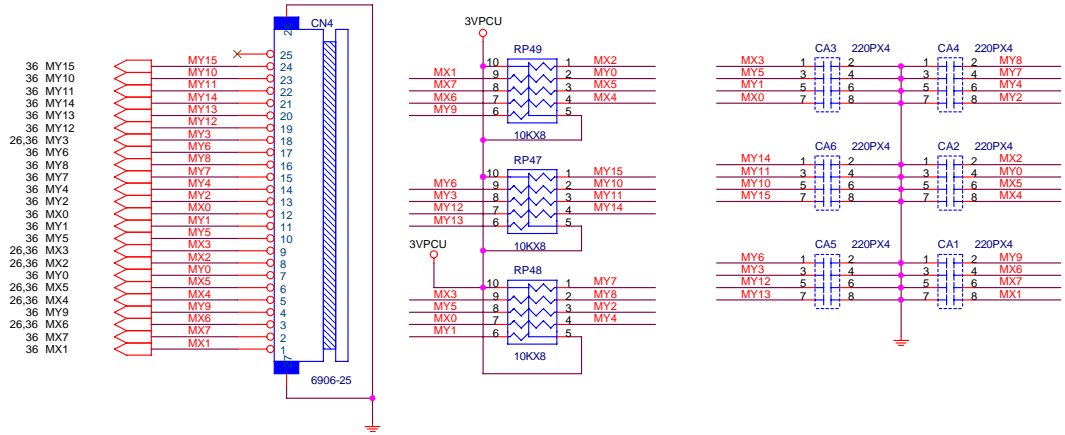
BLUETOOTH CONNECTOR



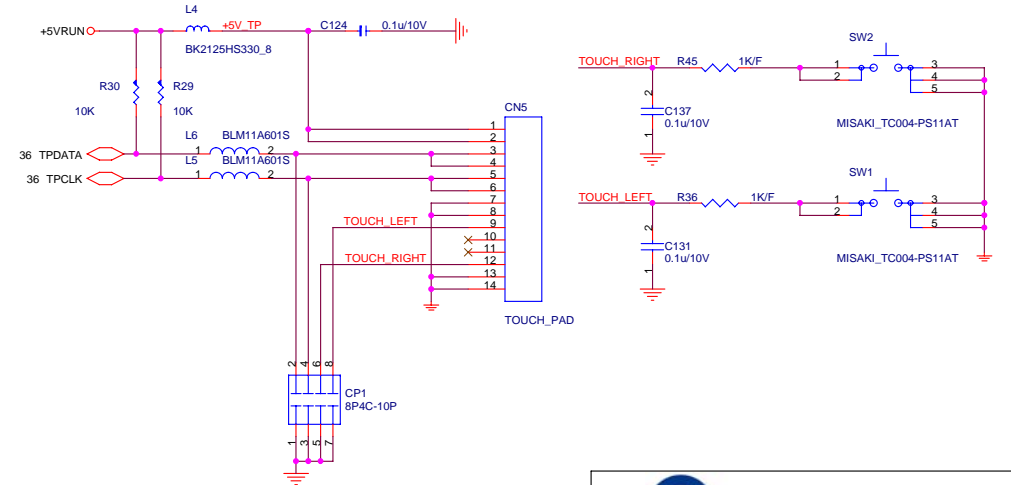
NEWCARD (PCIEXPRESS\*1 + USB\*1)

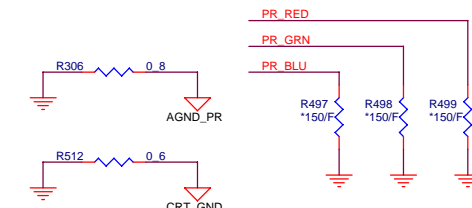
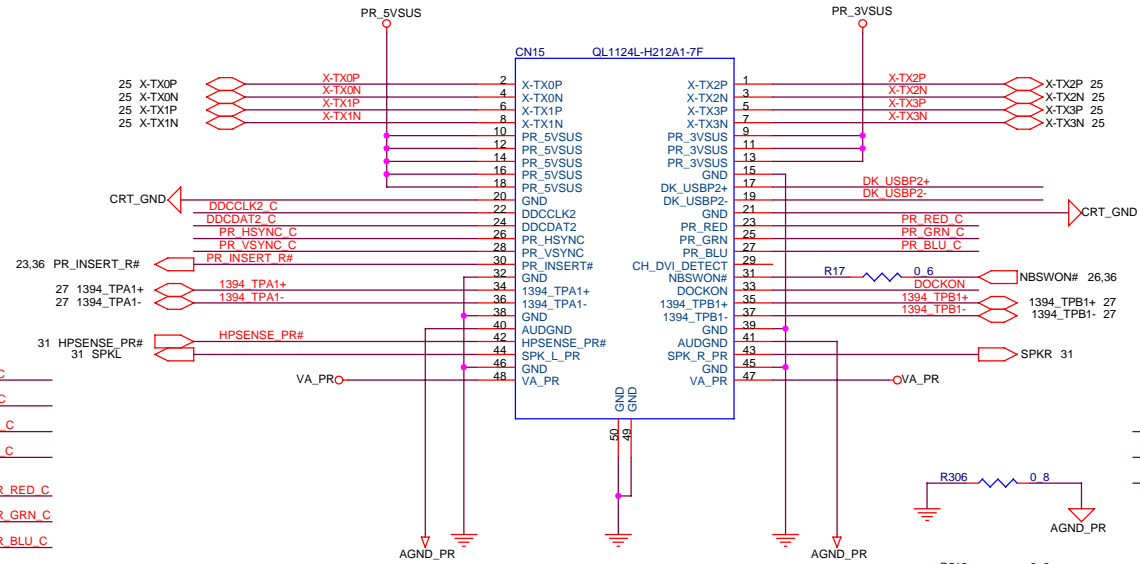
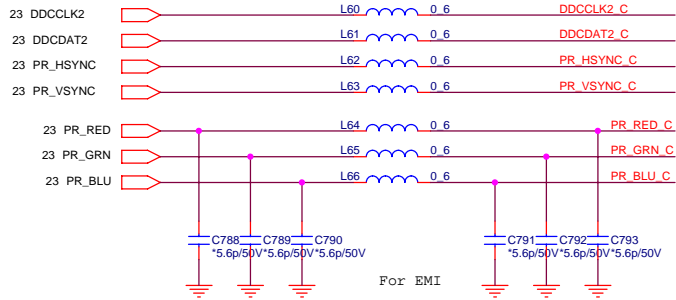
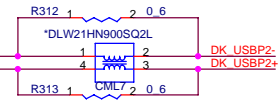
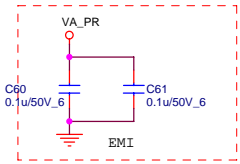


# KeyBoard Interface

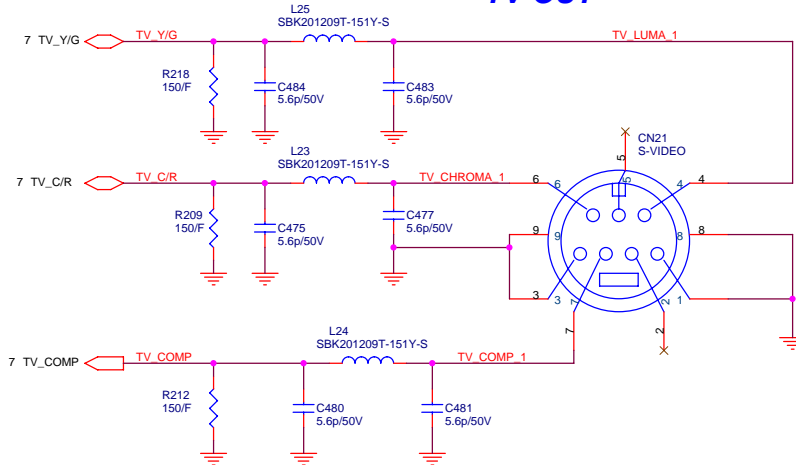


# TOUCH PAD





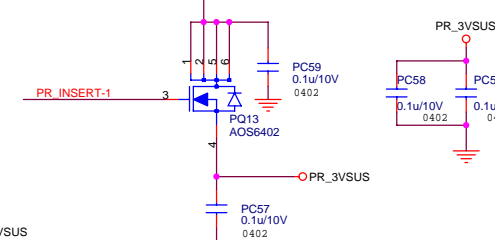
## TV-OUT



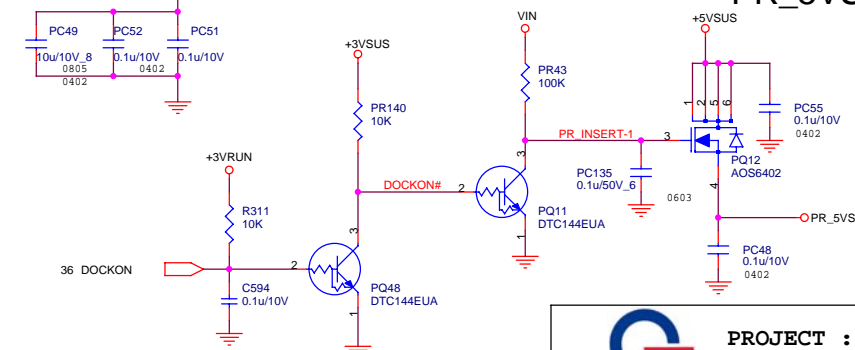
Intel CRB  
150 ohm @ 100MHZ  
(100mA)  
6pf 16V

CX8PG181001(180 ohm, 1.5A)  
CH00606TB04 CH00606TB04

## PR\_3VSUS

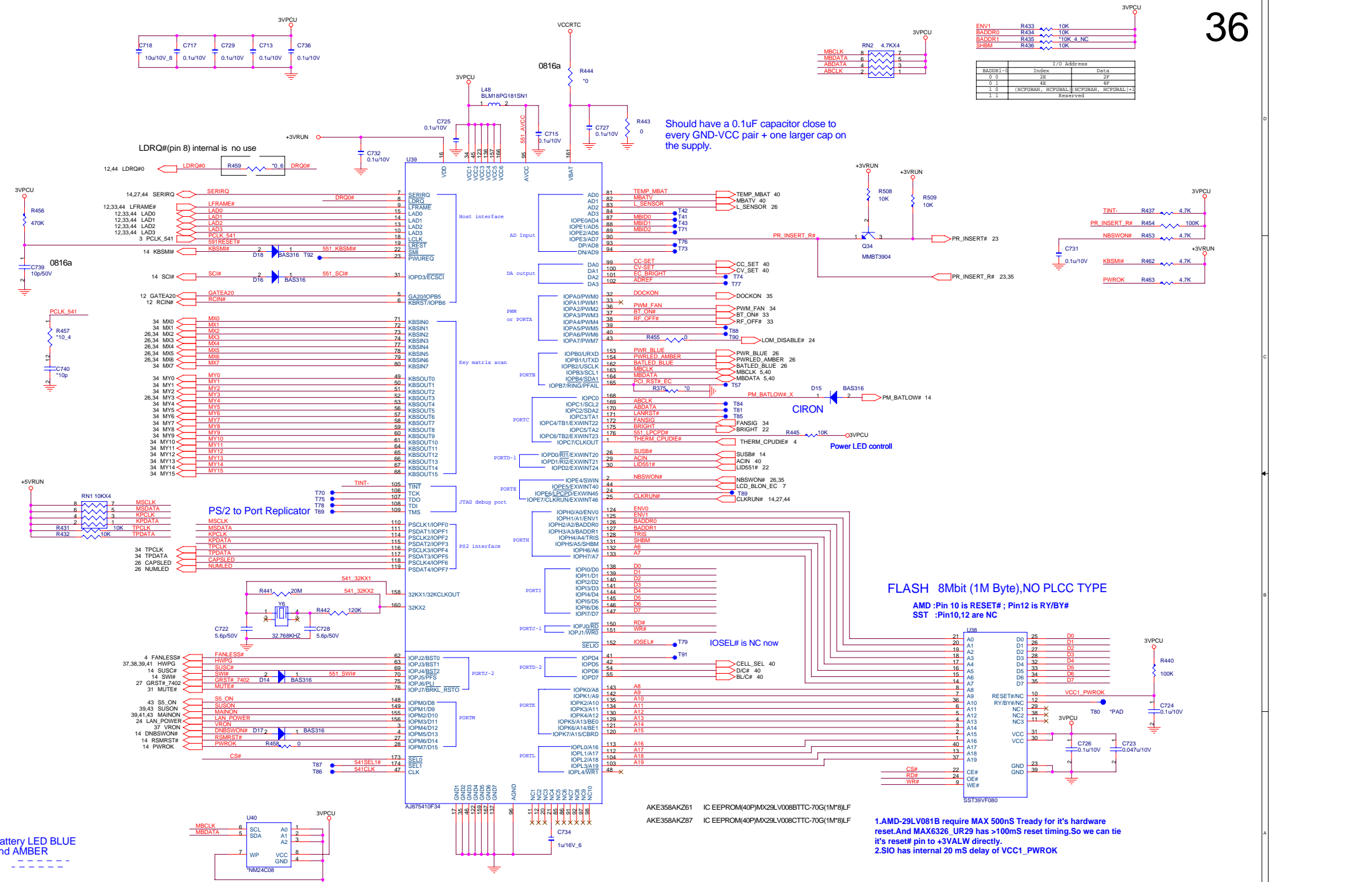


## PR\_5VSUS



**PROJECT : TW3**  
**Quanta Computer Inc.**

Size	Document Number	Rev
	PORT REPLICATOR	B2A
Date:	Tuesday, April 18, 2006	Sheet 35 of 48



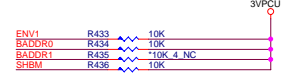
Should have a 0.1uF capacitor close to every GND-VCC pair + one larger cap on the supply.

FLASH 8Mbit (1M Byte), NO PLCC TYPE

AMD : Pin 10 is RESET# ; Pin12 is RY/BY#  
SST : Pin10,12 are NC

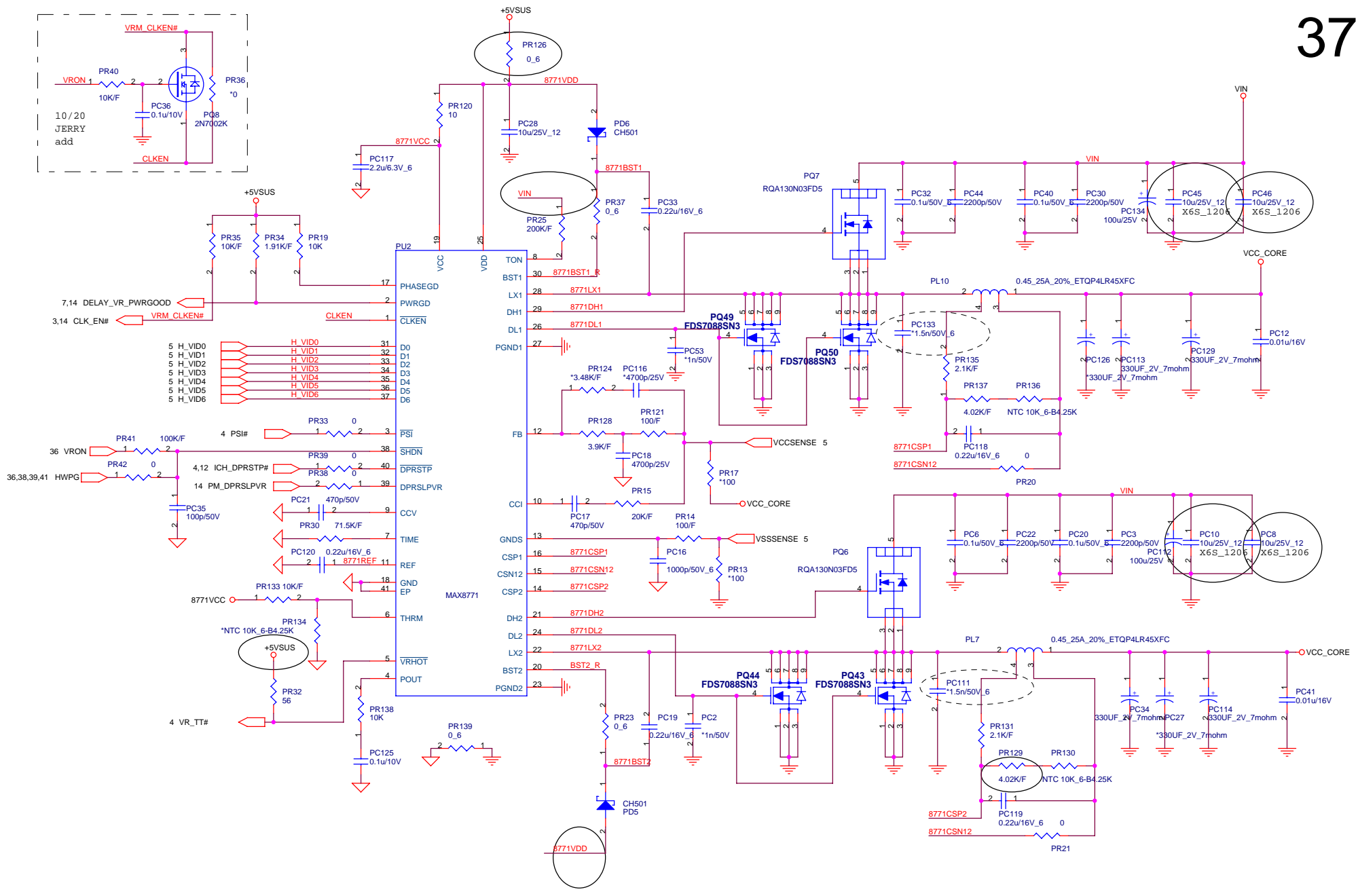
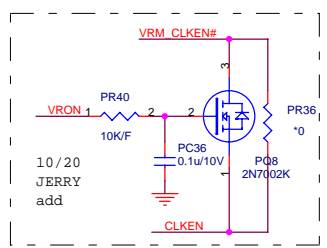
1.AMD-29LV081B require MAX 500nS Tready for it's hardware reset. And MAX6326 UR29 has >100mS reset timing. So we can tie it's reset# pin to +3VALW directly.  
2.SIO has internal 20 mS delay of VCC1\_PWROK

I/O Address		
BA000-1	Index	Data
0 0	2E	F
0 1	4E	4F
1 0	HC0FBAB, HC0FBAL, HC0FBAB, HC0FBAL	
1 1	Reserved	

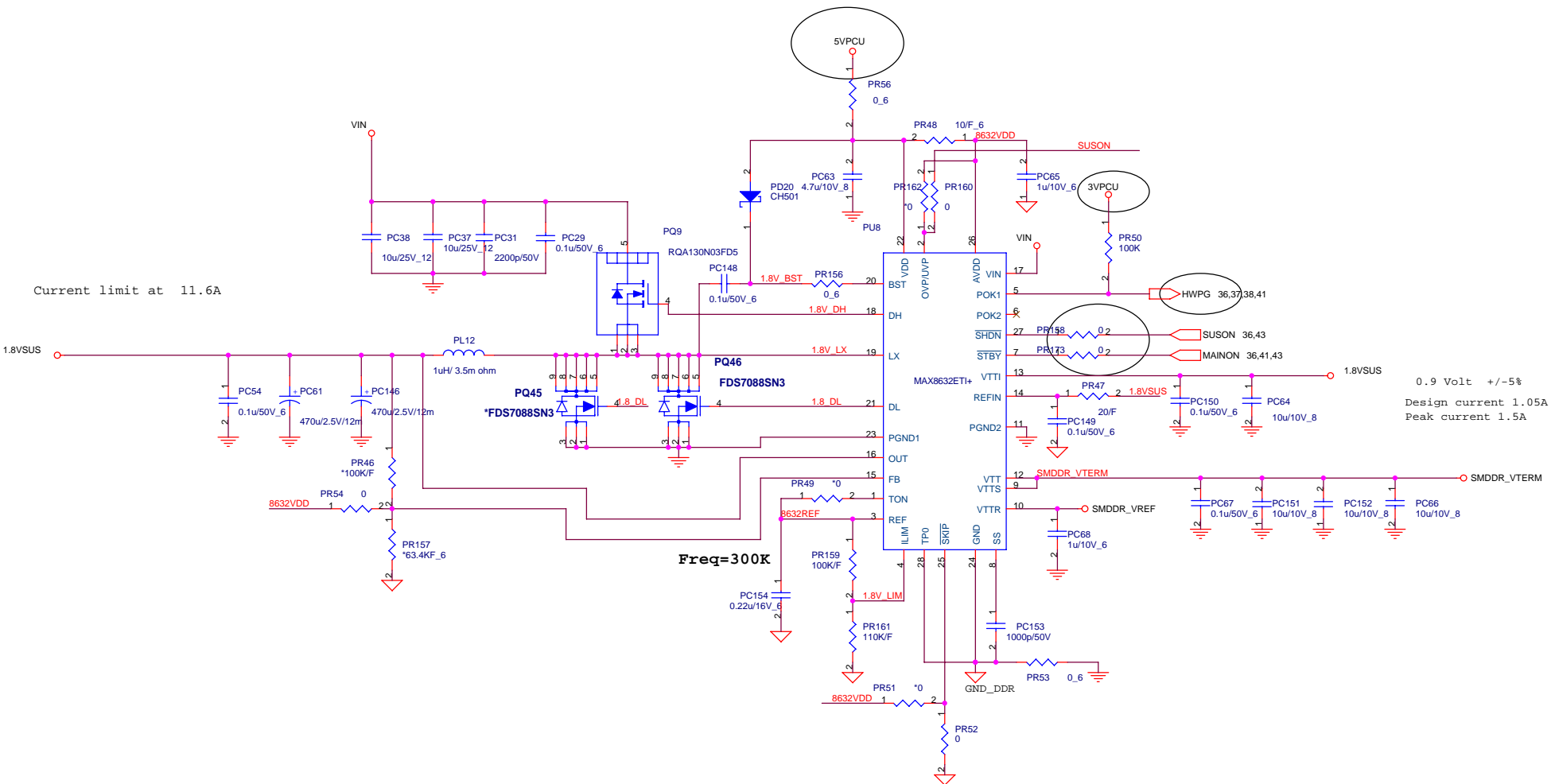


I/O Address		
BA000-1	Index	Data
0 0	2E	F
0 1	4E	4F
1 0	HC0FBAB, HC0FBAL, HC0FBAB, HC0FBAL	
1 1	Reserved	

Battery LED BLUE and AMBER







Current limit at 11.6A

0.9 Volt +/-5%  
Design current 1.05A  
Peak current 1.5A

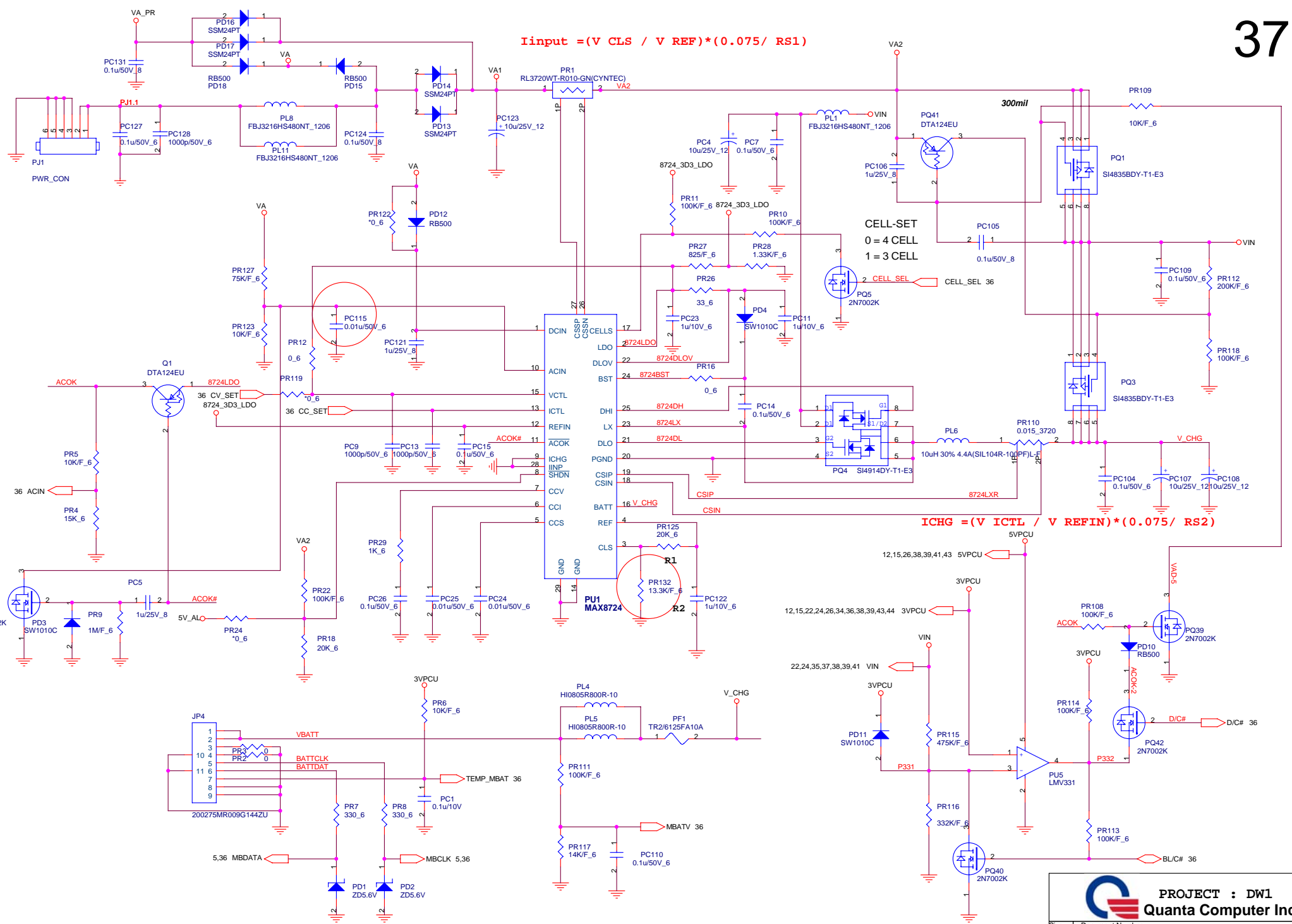
**PROJECT : TW3**  
**Quanta Computer Inc.**

Size	Document Number	Rev
	1.8VSUS/+0.9TERM/+2.5VSUS	B2A
Date:	Tuesday, April 18, 2006	Sheet 39 of 48

$I_{input} = (V_{CLS} / V_{REF}) * (0.075 / RS1)$

CELL-SET  
0 = 4 CELL  
1 = 3 CELL

$ICHG = (V_{ICTL} / V_{REFIN}) * (0.075 / RS2)$

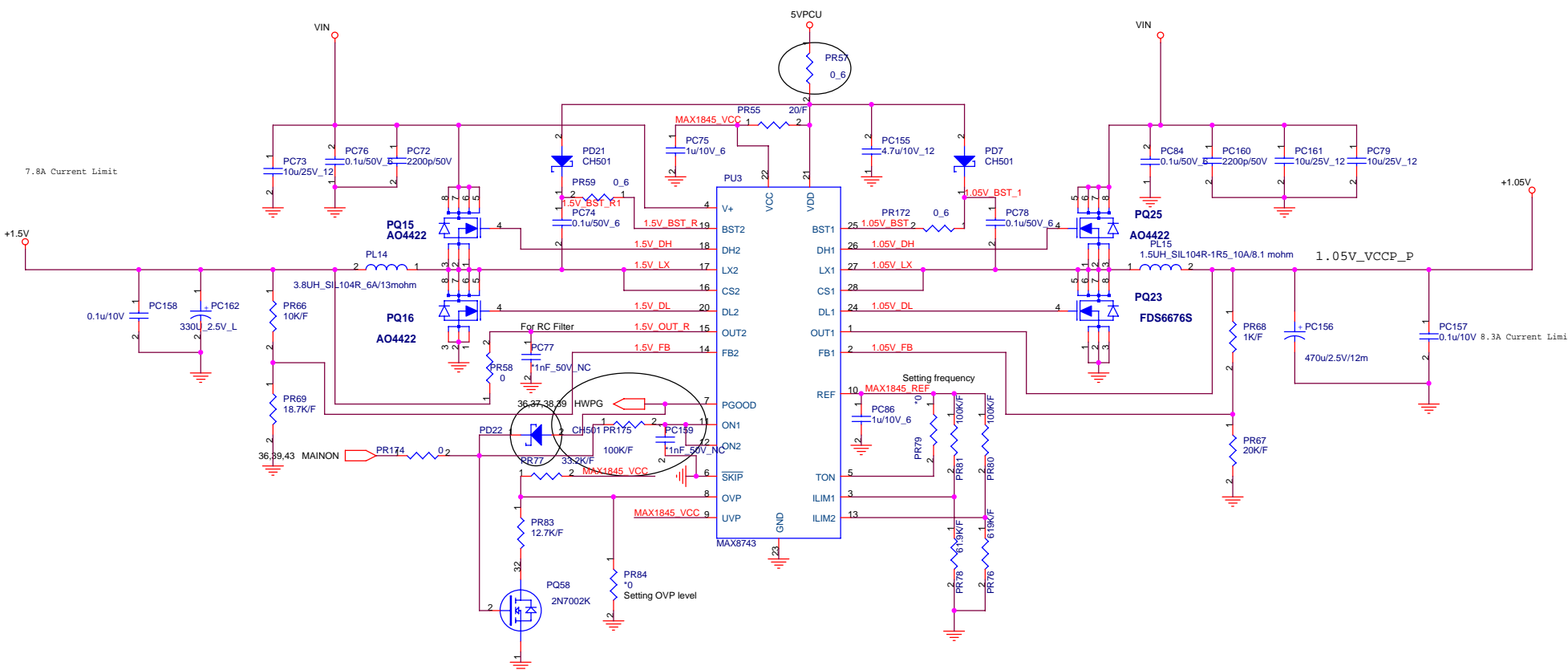


**PROJECT : DW1**  
**Quanta Computer Inc.**

Size Custom	Document Number <b>CHARGER</b>	Rev B2A
Date: Tuesday, April 18, 2006	Sheet 40 of 48	



AO4422:  $I_d = 11A$ ,  $R_{ds(on)} = 24m\ \Omega$ ,  $Q_g = 19.8nC$   
 FDS6676S:  $I_d = 14.5A$ ,  $R_{ds(on)} = 7.25m\ \Omega$ ,  $Q_g = 43\ nC$



5

4

3

2

1

D

D

C

C

B

B

A

A

5

4

3

2

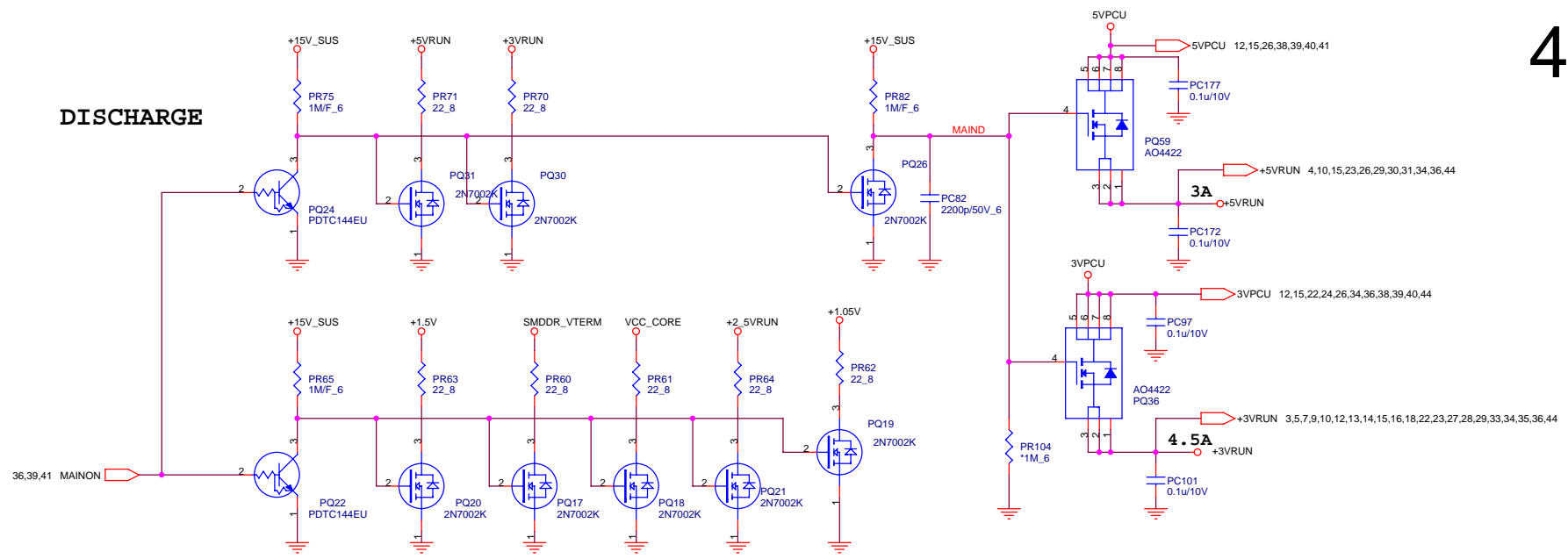
1



**PROJECT : TW3**  
**Quanta Computer Inc.**

Size	Document Number	Rev
	Empty	B2A
Date:	Tuesday, April 18, 2006	Sheet 42 of 48

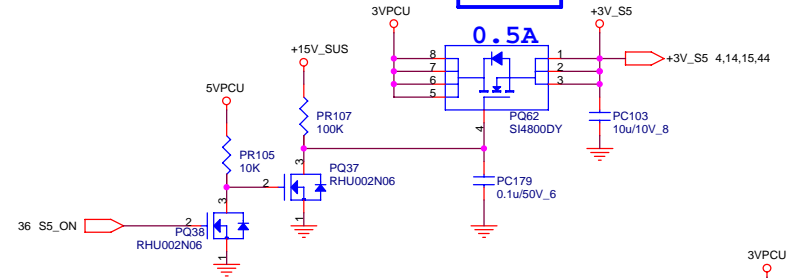
DISCHARGE



200mils

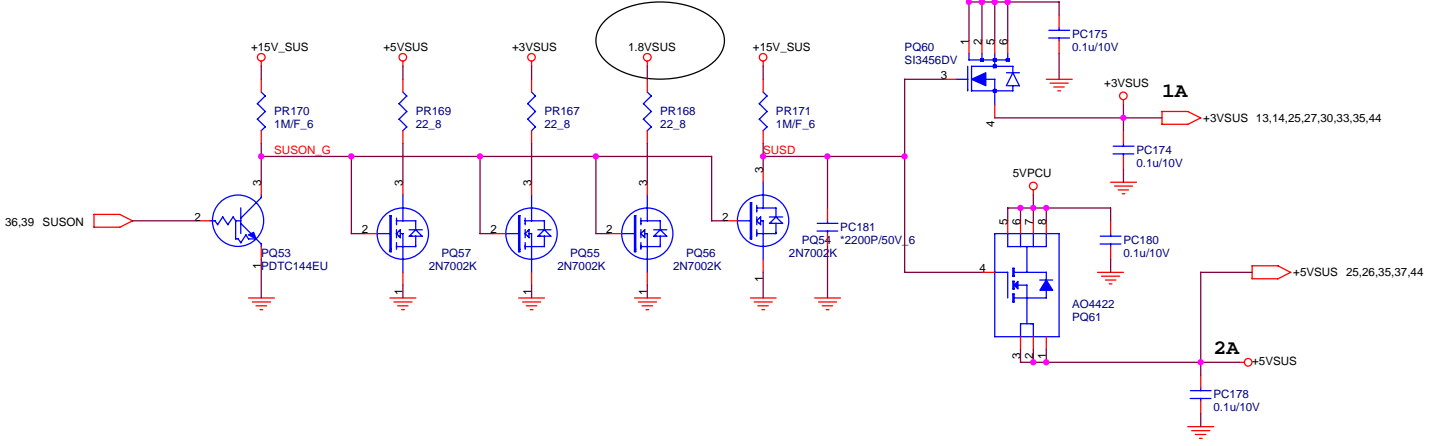
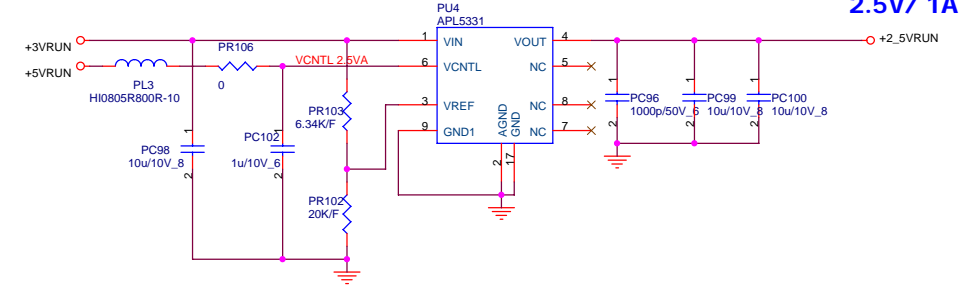
S0-S5

0.5A



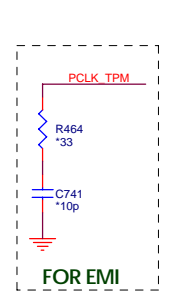
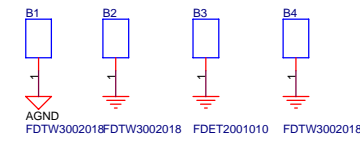
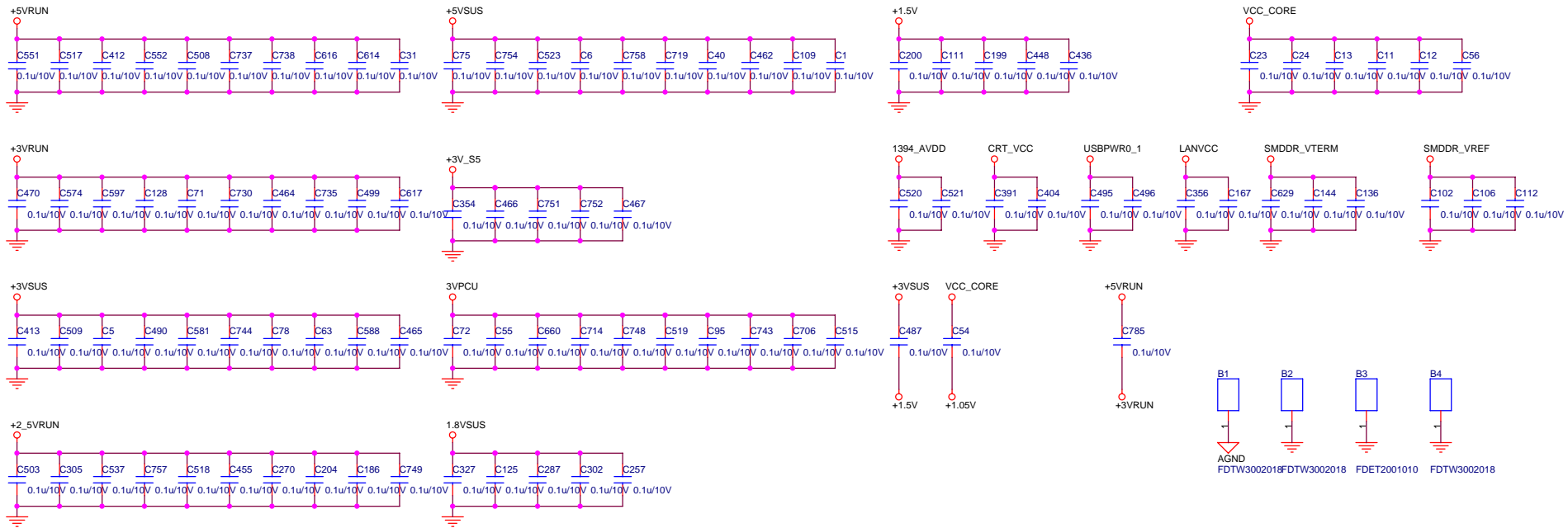
+2\_5VRUN

2.5V/ 1A



**PROJECT : TW3**  
**Quanta Computer Inc.**

Size	Document Number	Rev
	Discharge Circuit	B2A
Date:	Tuesday, April 18, 2006	Sheet 43 of 48

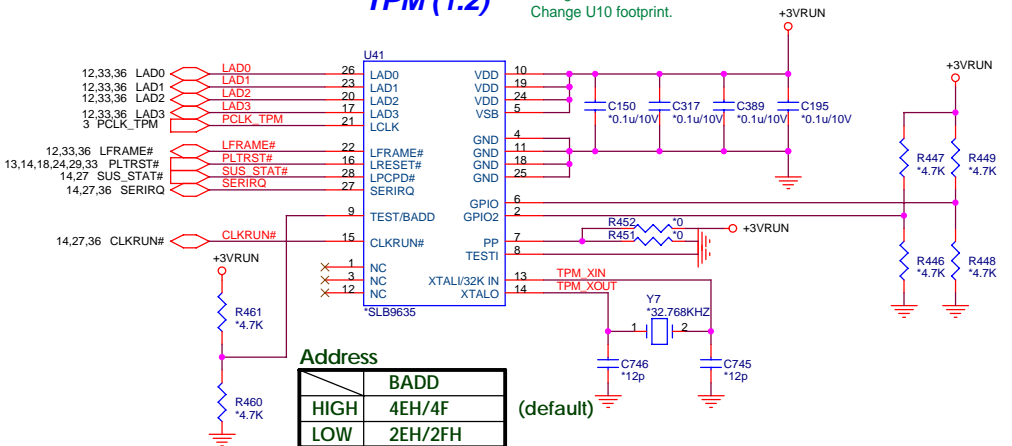


FOR EMI

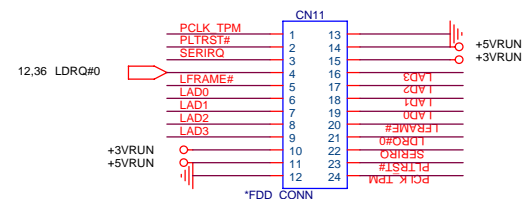
B stage:  
Change U10 Footprint


### TPM (1.2)

B stage:  
Change U10 footprint.



### Debug Conn.






**PROJECT : TW3**  
**Quanta Computer Inc.**

Size	Document Number	Rev
	<b>EMI &amp; TPM &amp; Debug Conn</b>	B2A
Date:	Tuesday, April 18, 2006	Sheet 44 of 48

MODEL	REV	CHANGE LIST		Model	TW3 M/B	
				Page	From	To
TW3M M/B	B to 1223	Page 29	Change R472 to NI for SATA,install for PATA to solve sometimes ODD can't be detected and slow boot..	1	1A	
		Page 33	Add R481,R480 to solve WLAN LED light leakage.	2	1A	
		Page 3	Change R177 to install and pull low to set VGA clock to 100MHz.	3	1A	
		Page 29	Change R254 to NI for SATA,install for PATA.	4	1A	
		Page 14	Add R482,R483 for CRT/DVI option.	5	1A	
		Page 24	Change C645 to 10uF for LAN 1.2V per Marvell recommendation.	6	1A	
		Page 30	3V_DVDD connect to +3VSUS to solve WOR.	7	1A	
				8	1A	
				9	1A	
				10	1A	
				11	1A	
	1223 to 1224	Page 32	Change MQ1,MQ2,MQ3,MQ4 to BA000420Z07 to solve MODEM low performance.	12	1A	
		Page 37	Delete short pad.	13	1A	
		Page 38	Delete short pad.PC92 change to install.	14	1A	
		Page 39	Delete short pad.	15	1A	
		Page 41	Delete short pad.	16	1A	
		Page 43	Delete short pad.	17	1A	
		Page 5	R19 change to NI for solving power-on shutdown.	18	1A	
		Page 40	PR132 change to 13.3K.PR110 change to CS+0158JL11.	19	1A	
		Page 34	HOLE3,HOLE4,HOLE7,HOLE8 change to MBRW1003011.	20	1A	
		Page 37	PC34,PC113,PC114,PC129 change to CH733RM8831.	21	1A	
		Page 23	F1 change to DK100TPU028.	22	1A	
		Page 33	Q17 change to install for BT LED control.	23	1A	
		Page 34	Change CN4 footprint to "afn250-a2g1t-25p-I" for SMT issue.	24	1A	
		Page 26	Change CN1.4 connection to RF_LED.	25	1A	
		Page 33	Add NET RF_LED.	26	1A	
		Page 36	Delete NET TUCHLED.	27	1A	
		Page 31	Change C541,C546 to X7R for audio precision.	28	1A	
		1223 to 1226	Page 38	Change PC93,PD9,PC168 to install. Delete NET 10V.	29	1A
	Page 41		Change NET 10V to +15V_SUS.	30	1A	
	Page 26		LED2,LED3 change to dual color type(cost down and unify brightness and color).	31	1A	
	Page 12		Reserve C784 on THERMTRIP for ESD.	32	1A	
	Page 35		Reserve R497,R498,R499 for TW2 PR.	33	1A	
	Page 33		Delete RP45,RP46,R210 for layout problem.	34	1A	
	Page 33		Change CN23 to Molex (same as SW1). Add CN31 PCIE latch.	35	1A	
	1226 to 1227	Page 44	Add EMI spring B1,B2,B3.	36	1A	
		Page 32	Install MC8,MC9 for EMI.	37	1A	
		Page 12	Change C459 TO 22pF for EMI.	38	1A	
		Page 31	R479,R281,R295 change to install for EMI.	39	1A	
		Page 3	Change Y1 P/N to BG614318081(CL=20pF) for solving system time delay issue.	40	1A	
	1227 to 1228	Page 44	Add B4 for EMI.	41	1A	
		Page 23	Change C694,C701,C703 to 10pF for signal quality.	42	1A	
		Page 36	RN2 change to 4.7K for IIC signal quality.	43	1A	
		Page 30	C528,C529 change to 1uF/10V X5R for audio precision.	44	1A	
		Page 35	Add L60-L66,C788-C793 for EMI.	45	1A	
Page 26		Change CN9,CN12 P/N to DFHS04FRE80.				
1227 to 1230	Page 36	Delete D13, add R508,R509,Q34 for PR leakage current. R454 change to 100K.				




**PROJECT : TW3**  
**Quanta Computer Inc.**

Size Document Number Rev  
Change List (B2A) B2A

Date: Tuesday, April 18, 2006 Sheet 45 of 48

MODEL	REV	CHANGE LIST		Model	TW3 M/B		
				Page	From	To	
TW3M	1230 to 0102	Page 38	PC173 change to 470uF.	1	1A		
		Page 39	PC66 change to install.	2	1A		
		Page 41	PD7,PD21,PD22 change to CH501.	3	1A		
		Page 37	PD6,PD5 change to CH501.	4	1A		
		Page 26	CN12,CN9 USB connector change to DIP type.	5	1A		
		Page 29	CN25 pin25,26 and CN24 pin47,48 disconnect to GND.	6	1A		
		Page 23	CN6 pin27,28 disconnect to GND.	7	1A		
		Page 34	SW1,SW2 P/N change to DHP00FC1G16.	8	1A		
		Page 36	Change R454 to 100K,R508,R509 to 10K.	9	1A		
		0102 to 0103	Page 4	R101,R97,Q11 change to install.	10	1A	
			Page 6,7,8,9,10,11	Change U32 P/N to AJSL8Z20T17.(945GM)	11	1A	
			Page 12,13,14,15	Change U36 P/N to AJSL8YB0T12.(ICH7M)	12	1A	
			Page 44	Add C785 for EMI.	13	1A	
			Page 37	PR128 change to 3.9K.	14	1A	
			0103 to 0105	Page 45,46	Update change list.	15	1A
	Page 27			Change J1 P/N to DFHS04FRE47.	16	1A	
	Page 35			Change CN15 to install and P/N to DFHS48FR001	17	1A	
	Page 44			Change B1,B2,B4 P/N to FDTW3002018.	18	1A	
	Page 36			U38 P/N change to AKE35ZAKK17.	19	1A	
	0105 to 0111	Page 30		Change C528,C529 to 2.2uF/6.3V for audio precision.	20	1A	
		0111 to 0119		Page 23	Q21 mirror vertical.	21	1A
			Page 23	Add C794-C799, L67-L69 for EMI.	22	1A	
			Page 23	Add and R513,R514 for DVI.	23	1A	
			Page 23	L46,L44,L42 change to 0 ohm. C701,C703,C694,C700,C702,C705 change to NI for EMI.	24	1A	
			Page 32	Change MR5,MR6,MR,MR10 to 280ohm. Add MR11,MR12,MR13. Change MR8 to NI.	25	1A	
			Page 35	R17 change to install.	26	1A	
			Page 35	CN15.21,22 change to CRT_GND. Add R512.	27	1A	
			Page 35	Change D1 to page23 and its connection and to NI.	28	1A	
			Page 41	PL14 P/N change to DC-38600001.	29	1A	
	Page 43		PQ59,PQ61,PQ36 P/N change to BAM44220002.	30	1A		
	0119 to 0120	Page 36	RN2 P/N change to CJ247084N25.	31	1A		
		Page 26	LED4 P/N change to BEBL0002Z62. LED1-3 P/N change to BEAB0013ZA1.	32	1A		
		Page 33	CN10 P/N change to DFHS26FR489.	33	1A		
		Page 14	Change R368 to install,R366 to NI to set w/ docking.	34	1A		
		Page 27	Change D7 to install to solve 7402 does not work.	35	1A		
		Page 23	Correct CN6 C1-C4 pin define.	36	1A		
		Page 23	Reserve Q37,Q38,RP56,R513,R514 for DVI disable when docking attach.	37	1A		
		Page 29	CN25 footprint change to "SATA-C16647-122A4-B-22P-R-V" for SMT issue.	38	1A		
		0120 to 0209A	Page 25	LAN active/link LED change to +3VSUS.	39	1A	
					40	1A	
				41	1A		
				42	1A		
				43	1A		
				44	1A		
				45	1A		


**PROJECT : TW3**  
**Quanta Computer Inc.**

Size	Document Number	Rev
Change List (B2A)		B1A
Date: Tuesday, April 18, 2006		Sheet 46 of 48

PROJECT: TW3	PCBA NO.	REV: 2B	DOC. NO :
APPROVED BY : Johnson Hsu	CHECK BY : Titan Chiang	DRAWING BY : Tony Huang	DATE :05/05/2005 SHEET 1

MODEL

REV

CHANGE LIST

Page	TW3 M/B	
	From	To
1	1A	
2	1A	
3	1A	
4	1A	
5	1A	
6	1A	
7	1A	
8	1A	
9	1A	
10	1A	
11	1A	
12	1A	
13	1A	
14	1A	
15	1A	
16	1A	
17	1A	
18	1A	
19	1A	
20	1A	
21	1A	
22	1A	
23	1A	
24	1A	
25	1A	
26	1A	
27	1A	
28	1A	
29	1A	
30	1A	
31	1A	
32	1A	
33	1A	
34	1A	
35	1A	
36	1A	
37	1A	
38	1A	
39	1A	
40	1A	
41	1A	
42	1A	
43	1A	
44	1A	
45	1A	

TW3A  
C2 to C3

0209 to 0222A

0222A to 0407A

Page	Description
Page 18	(1)Change to Install when DVI mode(R486 ->CS31002JB28) (2)Change R489,R490,R491,R492 to install R489: From CS13302JB21 to CH01006JB08 R490,R491,R492: From CS13302JB21 to CS11502FB21
Page 23	(1) R150,R159,Q37,Q38,RP56 Change to install for DVI (2)Change L67,L68,L69 P/N from CX8BB121002 to CX8BB470007 (3) Change C794,C795,C796 P/N from CH01806JB07 to CH01006JB08
Page 27	(1) Change R208 pin1 contact to +3VRUN Change R208 P/N to CS31002JB28,C473 change to CH4102K1B03 ,D7 change to NI.
Page 30	(1) Change R246,R247 P/N from CS00002JB38 to CX5HM121104
Page 31	(1) Change L50,L51,L52,L53 P/N from CS00003J951 to CX0HM121008 (2) Add C759,C760,C761,C762 to install (CH02206GB02)
Page 26	(1) Change CN9,CN12 layout footprint to usb-020133mr004s566zl-c-h
Page 31	(1) Change U21 layout footprint to QFN28-5X5-5-33P(add thermal Pad

**PROJECT : TW3**  
**Quanta Computer Inc.**

Size	Document Number	Rev
Change List (B2A)		B1A
Date: Tuesday, April 18, 2006		Sheet 47 of 48

PROJECT: TW3	PCBA NO.	REV: 2B	DOC. NO :
APPROVED BY : Johnson Hsu	CHECK BY : Titan Chiang	DRAWING BY : Tony Huang	DATE :05/05/2005 SHEET 1

A. G72M to G72MV

1. change P/N to G72MV (AJ073000T14)
2. Set VGA core to 1.0V fix.
3. Change PCI\_DEVID.

B. VRAM 128MB to 64MB

1. follow config table to set RAM\_CFG.
2. Change VRAM P/N to HYNIX.
3. VRAMx2

C. LAN GIGA to 10/100.

1. Change LAN chip to 8038(AJ080380000).
2. Change Rset resistor.
3. Change transformer.

D. SATA to PATA

1. Set ODD to slave.
2. Set HDD to master.
3. Remove SATA conn.
4. Add PATA conn.
5. Change board ID to PATA.
6. Install resistor to connect ODD and HDD LED.
7. NI resistor of SATA LED.



PROJECT : TW3  
Quanta Computer Inc.