ZZZ

PCB

Part Number = DAZ0K400100

Compal Confidential

K73TA Schematics Document

AMD Sabine

APU Llano / Hudson M3 / Whistler

DIS only

2011-03-08

LA-7553P REV: 0.2

Security Classification	Compal Secret Data		Compal Electronics, Inc.
Issued Date	2010/08/04	Deciphered Date 2010/08/04	Title: Cover Page
Size: B	Document Number: QBL70 LA-7553P		Rev: 0.22
Date: Friday, April 29, 2011	Sheet 1 of 51		

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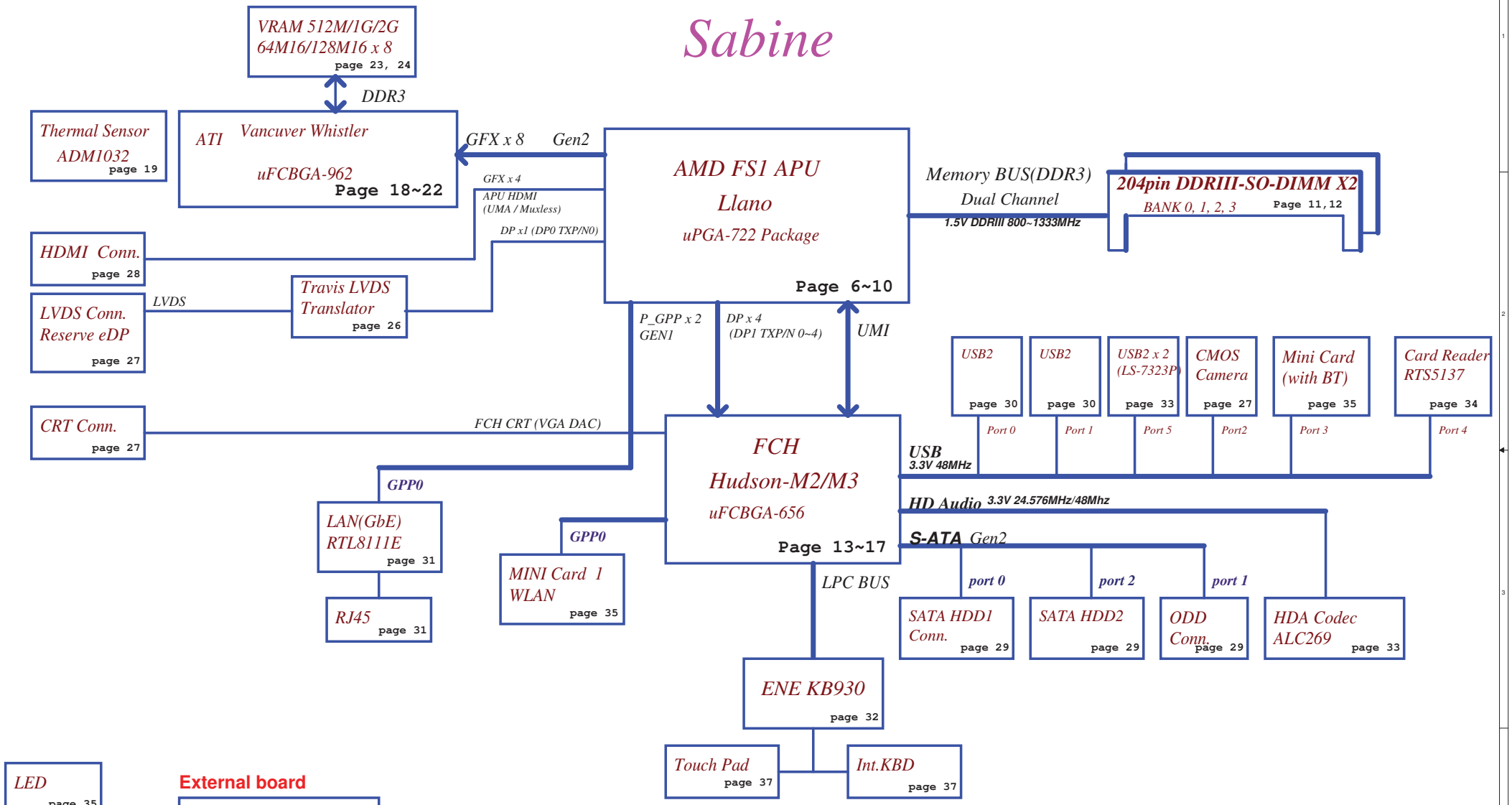
Model Name : QBL70



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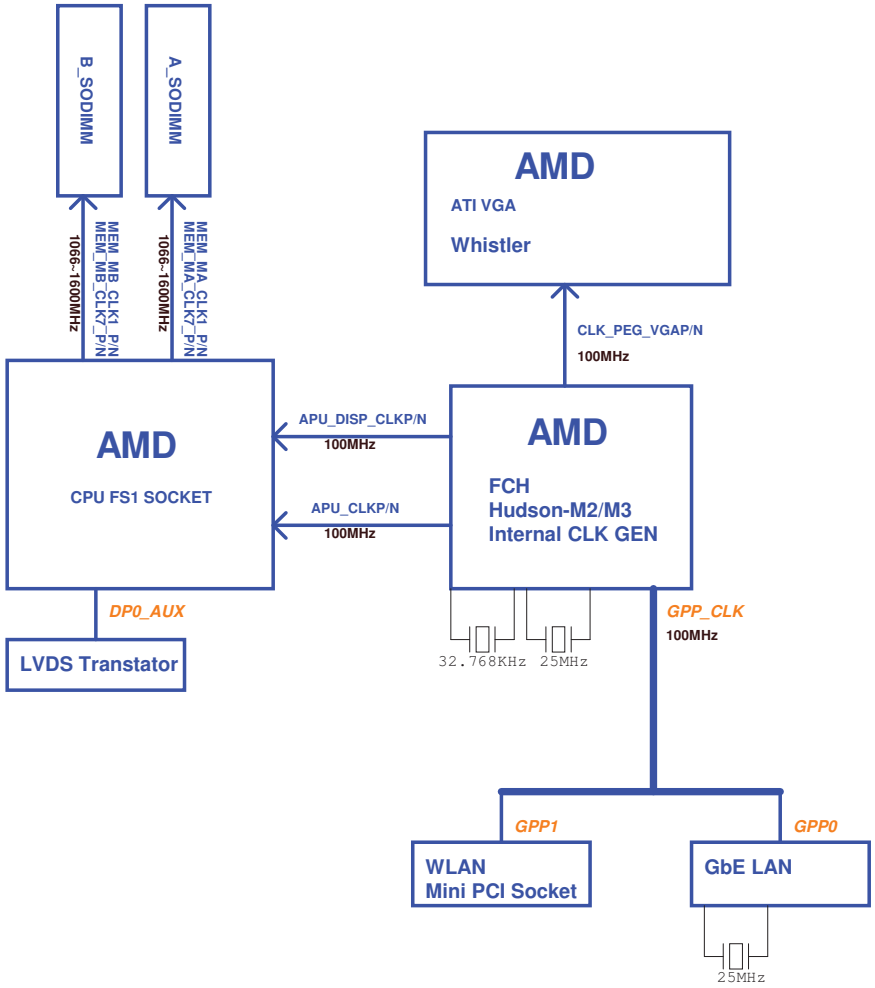
Title	Block Diagrams
Size: B	Document Number: QBL70 LA-7553P
Rev	0.22
Date:	Friday, April 29, 2011
Sheet	2 of 51

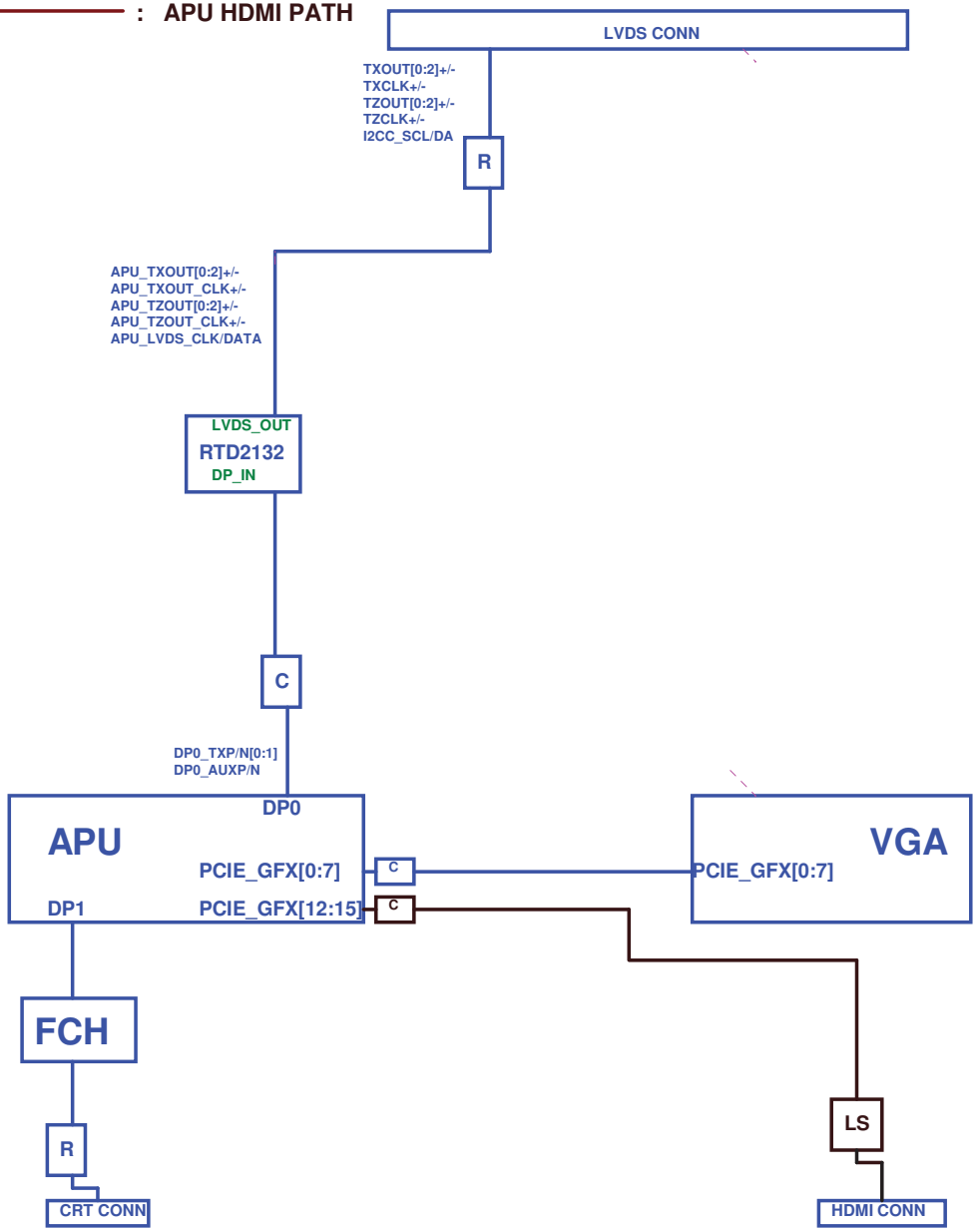
CLOCK DISTRIBUTION



DISPLAY DISTRIBUTION

: LVDS PATH

: APU HDMI PATH



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Issued Date	2010/08/04	Deciphered Date	2010/08/04

Title	CLOCK / DISPLAY DISTRIBUTION		
Size: Custom	Document Number: QBL70 LA-7553P		Rev: 0.22
Date: Friday, April 29, 2011	Sheet 3 of 51		

Voltage Rails

Power Plane	Description	S1	S3	S5
VIN	Adapter power supply (19V)	N/A	N/A	N/A
B+	AC or battery power rail for power circuit.	N/A	N/A	N/A
+CPU_CORE	Core voltage for CPU	ON	OFF	OFF
+CPU_CORE_1	Core voltage for CPU (0.7-1.2V)	ON	OFF	OFF
+CPU_CORE_NB	Voltage for On-die VGA of APU	ON	OFF	OFF
+VGA_CORE	0.95-1.2V switched power rail	ON	OFF	OFF
+0.75VS	0.75V switched power rail for DDR terminator	ON	ON	OFF
+1.0VSG	1.0V switched power rail for VGA	ON	OFF	OFF
+1.1ALW	1.1V switched power rail for FCH	ON	ON	ON*
+1.1VS	1.1V switched power rail for FCH	ON	OFF	OFF
+1.2VS	1.2V switched power rail for APU	ON	OFF	OFF
+1.5V	1.5V power rail for CPU VDDIO and DDR	ON	ON	OFF
+1.5VS	1.5V switched power rail	ON	OFF	OFF
+1.8VSG	1.8V switched power rail	ON	OFF	OFF
+2.5VS	2.5V for CPU_VDDA	ON	OFF	OFF
+3VALW	3.3V always on power rail	ON	ON	ON*
+3V_LAN	3.3V power rail for LAN	ON	ON	ON
+3VS	3.3V switched power rail	ON	OFF	OFF
+5VALW	5V always on power rail	ON	ON	ON*
+5VS	5V switched power rail	ON	OFF	OFF
+VSB	VSB always on power rail	ON	ON	ON*
+RTCVCC	RTC power	ON	ON	ON

Note : ON* means that this power plane is ON only with AC power available, otherwise it is OFF.

STATE \ SIGNAL	SLP_S1#	SLP_S3#	SLP_S4#	SLP_S5#	+VALW	+V	+VS	Clock
Full ON	HIGH	HIGH	HIGH	HIGH	ON	ON	ON	ON
S1(Power On Suspend)	LOW	HIGH	HIGH	HIGH	ON	ON	ON	LOW
S3 (Suspend to RAM)	LOW	LOW	HIGH	HIGH	ON	ON	OFF	OFF
S4 (Suspend to Disk)	LOW	LOW	LOW	HIGH	ON	OFF	OFF	OFF
S5 (Soft OFF)	LOW	LOW	LOW	LOW	ON	OFF	OFF	OFF

Board ID / SKU ID Table for AD channel

Vcc	3.3V +/- 5%
Ra/Rc/Re	100K +/- 5%

Board ID	Rb / Rd / Rf	V_{AD_BID} min	V_{AD_BID} typ	V_{AD_BID} max
0	0	0 V	0 V	0 V
1	8.2K +/- 5%	0.216 V	0.250 V	0.289 V
2	18K +/- 5%	0.436 V	0.503 V	0.538 V
3	33K +/- 5%	0.712 V	0.819 V	0.875 V
4	56K +/- 5%	1.036 V	1.185 V	1.264 V
5	100K +/- 5%	1.453 V	1.650 V	1.759 V
6	200K +/- 5%	1.935 V	2.200 V	2.341 V
7	NC	2.500 V	3.300 V	3.300 V

BOARD ID Table

Board ID	PCB Revision
0	NA
1	P5WS5
2	P5WH5
3	P7YE5
4	P7YS5
5	NA
6	NA
7	NA

BTO Option Table

BOM Structure	BTO Item
TL@	Translator
VGA@	Use VGA (Mux)
128@	Use VRAM channel A&B
X76@	VRAM ID Table
M2@	Use Hudson-M2
M3@	Use Hudson-M3
USB30@	USB30 on M/B
USB20@	USB20 on M/B

M3@ U25

FCH M3
Part Number = SA000043ID0

BOM Config

x = 1 is read cmd, x= 0 is writee cmd.

External PCI Devices

Device	IDSEL#	REQ#/GNT#	Interrupts

EC SM Bus1 address

Device	Address	HEX
Smart Battery	0001 011X b	16H

EC SM Bus2 address

Device	Address	HEX
ADI ADM1032 (VGA)	1001 101X b	9AH

FCH SM Bus 0 address

Device	Address	HEX
DDR DIMM1	1101 000X b	D0
DDR DIMM2	1101 001X b	D2

FCH SM Bus 1 address

Device	Address	HEX

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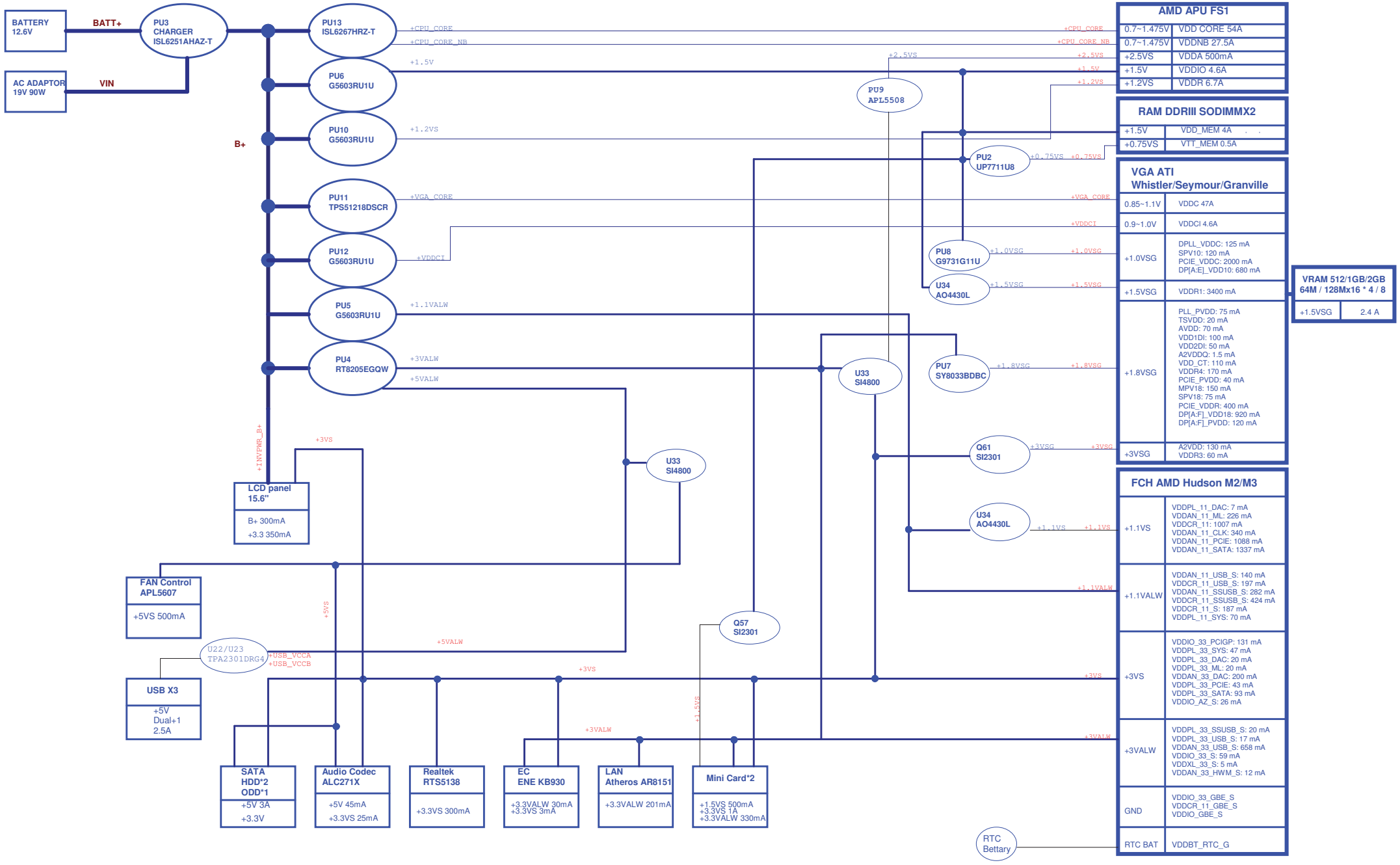
Title: Notes List

Size: B | Document Number: QBL70 LA-7553P | Rev: 0.22

Date: Friday, April 29, 2011 | Sheet 4 of 51



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Issued Date	2010/08/04	Deciphered Date	2010/08/04

Title: POWER DELIVERY CHART

Size	Document Number	Rev
Custom	QBL70 LA-7553P	0.22

Date: Friday, April 29, 2011 Sheet 5 of 51

18 PCIE_GTX_C_FRX_P[0..7]
18 PCIE_GTX_C_FRX_N[0..7]

PCIE_FTX_C_GRX_P[0..7] 18
PCIE_FTX_C_GRX_N[0..7] 18

APU To HDMI

PCIE_FTX_GRX_P[12..15] 28
PCIE_FTX_GRX_N[12..15] 28

JCPU1A — CONN@ — PCI EXPRESS — GRAPHICS

PCIE_GTX_C_FRX_P0	AA8	P_GFX_RXP0	P_GFX_TXP0	AA2	PCIE_FTX_GRX_P0	C917	1	2 0.1U 0402 16V7K	PCIE_FTX_C_GRX_P0
PCIE_GTX_C_FRX_N0	AA9	P_GFX_RXN0	P_GFX_TXN0	AA3	PCIE_FTX_GRX_N0	C918	1	2 0.1U 0402 16V7K	PCIE_FTX_C_GRX_N0
PCIE_GTX_C_FRX_P1	Y7	P_GFX_RXP1	P_GFX_TXP1	Y2	PCIE_FTX_GRX_P1	C919	1	2 0.1U 0402 16V7K	PCIE_FTX_C_GRX_P1
PCIE_GTX_C_FRX_N1	Y8	P_GFX_RXN1	P_GFX_TXN1	Y1	PCIE_FTX_GRX_N1	C920	1	2 0.1U 0402 16V7K	PCIE_FTX_C_GRX_N1
PCIE_GTX_C_FRX_P2	W5	P_GFX_RXP2	P_GFX_TXP2	Y4	PCIE_FTX_GRX_P2	C921	1	2 0.1U 0402 16V7K	PCIE_FTX_C_GRX_P2
PCIE_GTX_C_FRX_N2	W6	P_GFX_RXN2	P_GFX_TXN2	Y5	PCIE_FTX_GRX_N2	C922	1	2 0.1U 0402 16V7K	PCIE_FTX_C_GRX_N2
PCIE_GTX_C_FRX_P3	W8	P_GFX_RXP3	P_GFX_TXP3	W2	PCIE_FTX_GRX_P3	C923	1	2 0.1U 0402 16V7K	PCIE_FTX_C_GRX_P3
PCIE_GTX_C_FRX_N3	W9	P_GFX_RXN3	P_GFX_TXN3	W3	PCIE_FTX_GRX_N3	C924	1	2 0.1U 0402 16V7K	PCIE_FTX_C_GRX_N3
PCIE_GTX_C_FRX_P4	V7	P_GFX_RXP4	P_GFX_TXP4	V2	PCIE_FTX_GRX_P4	C925	1	2 0.1U 0402 16V7K	PCIE_FTX_C_GRX_P4
PCIE_GTX_C_FRX_N4	V8	P_GFX_RXN4	P_GFX_TXN4	V1	PCIE_FTX_GRX_N4	C926	1	2 0.1U 0402 16V7K	PCIE_FTX_C_GRX_N4
PCIE_GTX_C_FRX_P5	U5	P_GFX_RXP5	P_GFX_TXP5	V4	PCIE_FTX_GRX_P5	C927	1	2 0.1U 0402 16V7K	PCIE_FTX_C_GRX_P5
PCIE_GTX_C_FRX_N5	U6	P_GFX_RXN5	P_GFX_TXN5	V5	PCIE_FTX_GRX_N5	C928	1	2 0.1U 0402 16V7K	PCIE_FTX_C_GRX_N5
PCIE_GTX_C_FRX_P6	U8	P_GFX_RXP6	P_GFX_TXP6	U2	PCIE_FTX_GRX_P6	C929	1	2 0.1U 0402 16V7K	PCIE_FTX_C_GRX_P6
PCIE_GTX_C_FRX_N6	U9	P_GFX_RXN6	P_GFX_TXN6	U3	PCIE_FTX_GRX_N6	C930	1	2 0.1U 0402 16V7K	PCIE_FTX_C_GRX_N6
PCIE_GTX_C_FRX_P7	T7	P_GFX_RXP7	P_GFX_TXP7	T2	PCIE_FTX_GRX_P7	C931	1	2 0.1U 0402 16V7K	PCIE_FTX_C_GRX_P7
PCIE_GTX_C_FRX_N7	T8	P_GFX_RXN7	P_GFX_TXN7	T1	PCIE_FTX_GRX_N7	C932	1	2 0.1U 0402 16V7K	PCIE_FTX_C_GRX_N7

For UMA Mux.

R5	P_GFX_RXP8	P_GFX_TXP8	T4						
R6	P_GFX_RXN8	P_GFX_TXN8	T5						
R8	P_GFX_RXP9	P_GFX_TXP9	R2						
R9	P_GFX_RXN9	P_GFX_TXN9	R3						
P7	P_GFX_RXP10	P_GFX_TXP10	P2						
P8	P_GFX_RXN10	P_GFX_TXN10	P1						
N5	P_GFX_RXP11	P_GFX_TXP11	P4						
N6	P_GFX_RXN11	P_GFX_TXN11	P5						
N8	P_GFX_RXP12	P_GFX_TXP12	N2	PCIE_FTX_GRX_P12					
N9	P_GFX_RXN12	P_GFX_TXN12	N3	PCIE_FTX_GRX_N12					
M7	P_GFX_RXP13	P_GFX_TXP13	M2	PCIE_FTX_GRX_P13					
M8	P_GFX_RXN13	P_GFX_TXN13	M1	PCIE_FTX_GRX_N13					
L5	P_GFX_RXP14	P_GFX_TXP14	M4	PCIE_FTX_GRX_P14					
L6	P_GFX_RXN14	P_GFX_TXN14	M5	PCIE_FTX_GRX_N14					
L8	P_GFX_RXP15	P_GFX_TXP15	L2	PCIE_FTX_GRX_P15					
L9	P_GFX_RXN15	P_GFX_TXN15	L3	PCIE_FTX_GRX_N15					

2 / 1 / 0 / CK — *To HDMI*

GFP

31 PCIE_DTX_C_FRX_P0	AC5	P_GPP_RXP0	P_GPP_TXP0	AD4	PCIE_FTX_DRX_P0	C950	1	2 0.1U 0402 16V7K	PCIE_FTX_C_DRX_P0 31
31 PCIE_DTX_C_FRX_N0	AC6	P_GPP_RXN0	P_GPP_TXN0	AD5	PCIE_FTX_DRX_N0	C951	1	2 0.1U 0402 16V7K	PCIE_FTX_C_DRX_N0 31
	AC8	P_GPP_RXP1	P_GPP_TXP1	AC2					
	AC9	P_GPP_RXN1	P_GPP_TXN1	AC3					
	AB7	P_GPP_RXP2	P_GPP_TXP2	AB2					
	AB8	P_GPP_RXN2	P_GPP_TXN2	AB1					
	AA5	P_GPP_RXP3	P_GPP_TXP3	AB4					
	AA6	P_GPP_RXN3	P_GPP_TXN3	AB5					

GLAN

UMI-LINK

13 UMI_MTX_C_FRX_P0	AF8	P_UMI_RXP0	P_UMI_TXP0	AF1	UMI_FTX_MRX_P0	C956	1	2 0.1U 0402 16V7K	UMI_FTX_C_MRX_P0 13
13 UMI_MTX_C_FRX_N0	AF7	P_UMI_RXN0	P_UMI_TXN0	AF2	UMI_FTX_MRX_N0	C957	1	2 0.1U 0402 16V7K	UMI_FTX_C_MRX_N0 13
13 UMI_MTX_C_FRX_P1	AE6	P_UMI_RXP1	P_UMI_TXP1	AF5	UMI_FTX_MRX_P1	C958	1	2 0.1U 0402 16V7K	UMI_FTX_C_MRX_P1 13
13 UMI_MTX_C_FRX_N1	AE5	P_UMI_RXN1	P_UMI_TXN1	AF4	UMI_FTX_MRX_N1	C959	1	2 0.1U 0402 16V7K	UMI_FTX_C_MRX_N1 13
13 UMI_MTX_C_FRX_P2	AE9	P_UMI_RXP2	P_UMI_TXP2	AE3	UMI_FTX_MRX_P2	C960	1	2 0.1U 0402 16V7K	UMI_FTX_C_MRX_P2 13
13 UMI_MTX_C_FRX_N2	AE8	P_UMI_RXN2	P_UMI_TXN2	AE2	UMI_FTX_MRX_N2	C961	1	2 0.1U 0402 16V7K	UMI_FTX_C_MRX_N2 13
13 UMI_MTX_C_FRX_P3	AD8	P_UMI_RXP3	P_UMI_TXP3	AD1	UMI_FTX_MRX_P3	C962	1	2 0.1U 0402 16V7K	UMI_FTX_C_MRX_P3 13
13 UMI_MTX_C_FRX_N3	AD7	P_UMI_RXN3	P_UMI_TXN3	AD2	UMI_FTX_MRX_N3	C963	1	2 0.1U 0402 16V7K	UMI_FTX_C_MRX_N3 13

+1.2VS — R1802 1 2 P_ZVDDP — 196_0402_1% — K5 P_ZVDDP
K4 P_ZVSS — R1803 1 2 — 196_0402_1%

AMD_TOPEDO_FS-1

CPU TSI interface level shift

BSH111, the Vgs is:
min = 0.4V
Max = 1.3V

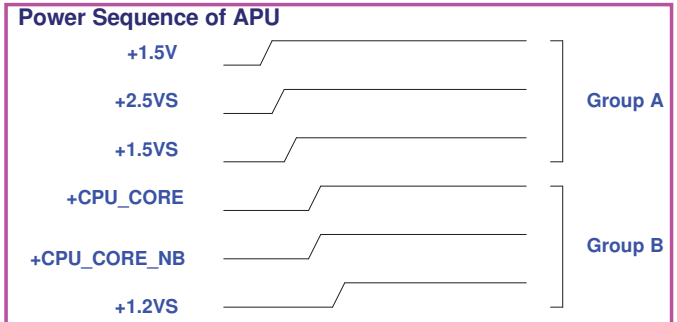
C935 1 2 0.1U 0402 16V4Z
+3VS — R1798 1 2 31.6K_0402_1% — R1799 1 2 30K_0402_1%

Q9
8,14 APU_SID — APU_SID — EC_SMB_DA — R1800 0_0402_5% — EC_SMB_DA2 19,32
BSH111 1N_SOT23-3

Q10
8,14 APU_SIC — APU_SIC — EC_SMB_CK — R1801 0_0402_5% — EC_SMB_CK2 19,32
BSH111 1N_SOT23-3

To EC

Power Sequence of APU



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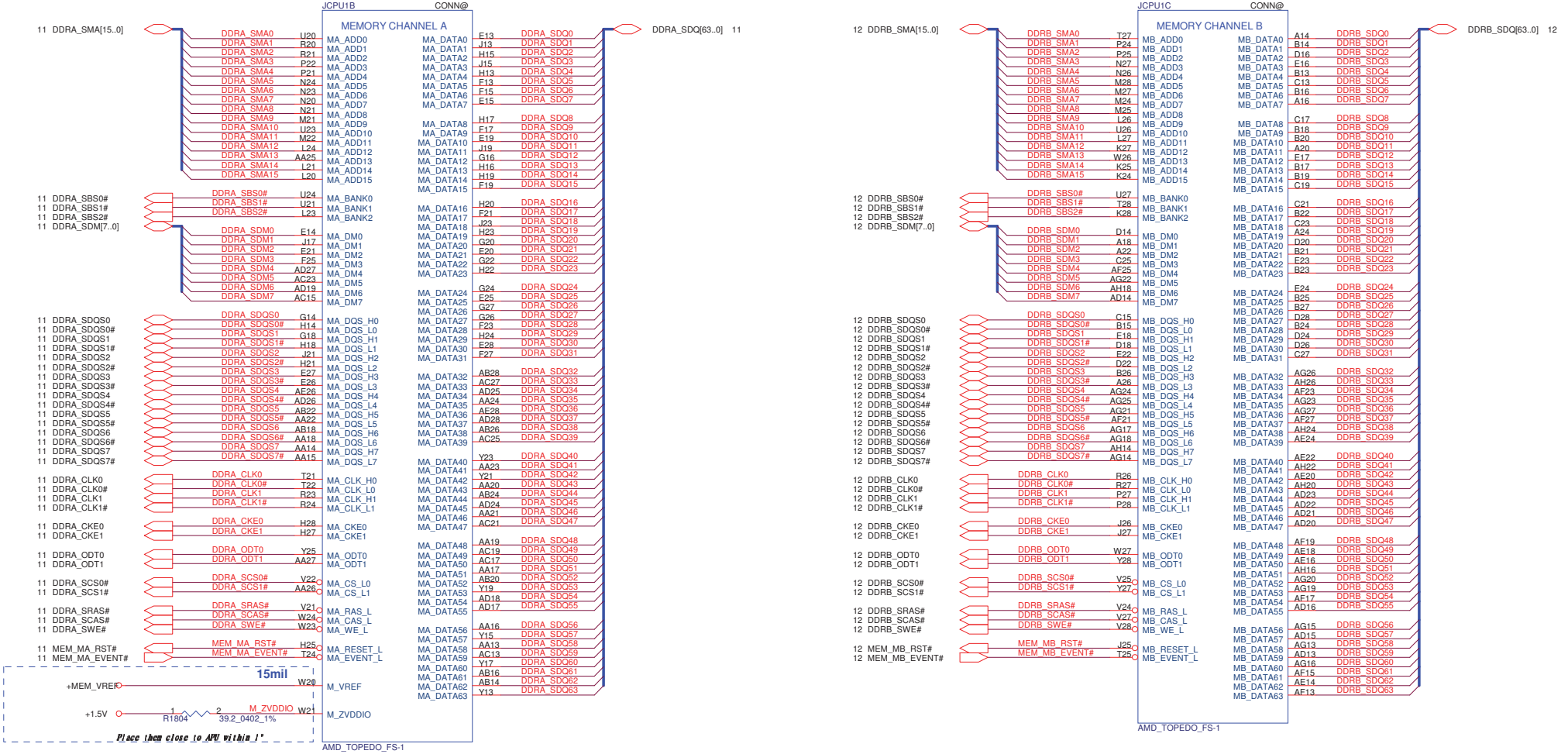
Compal Electronics, Inc.

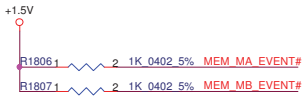
Title: AMD FS1 PCIE / UMI / TSI

Size: Custom | Document Number: QBL70 LA-7553P | Rev: 0.22

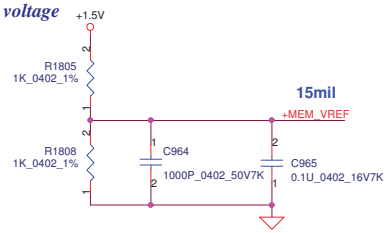
Date: Friday, April 29, 2011 | Sheet 6 of 51



EVENT# pull high



0.75V reference voltage



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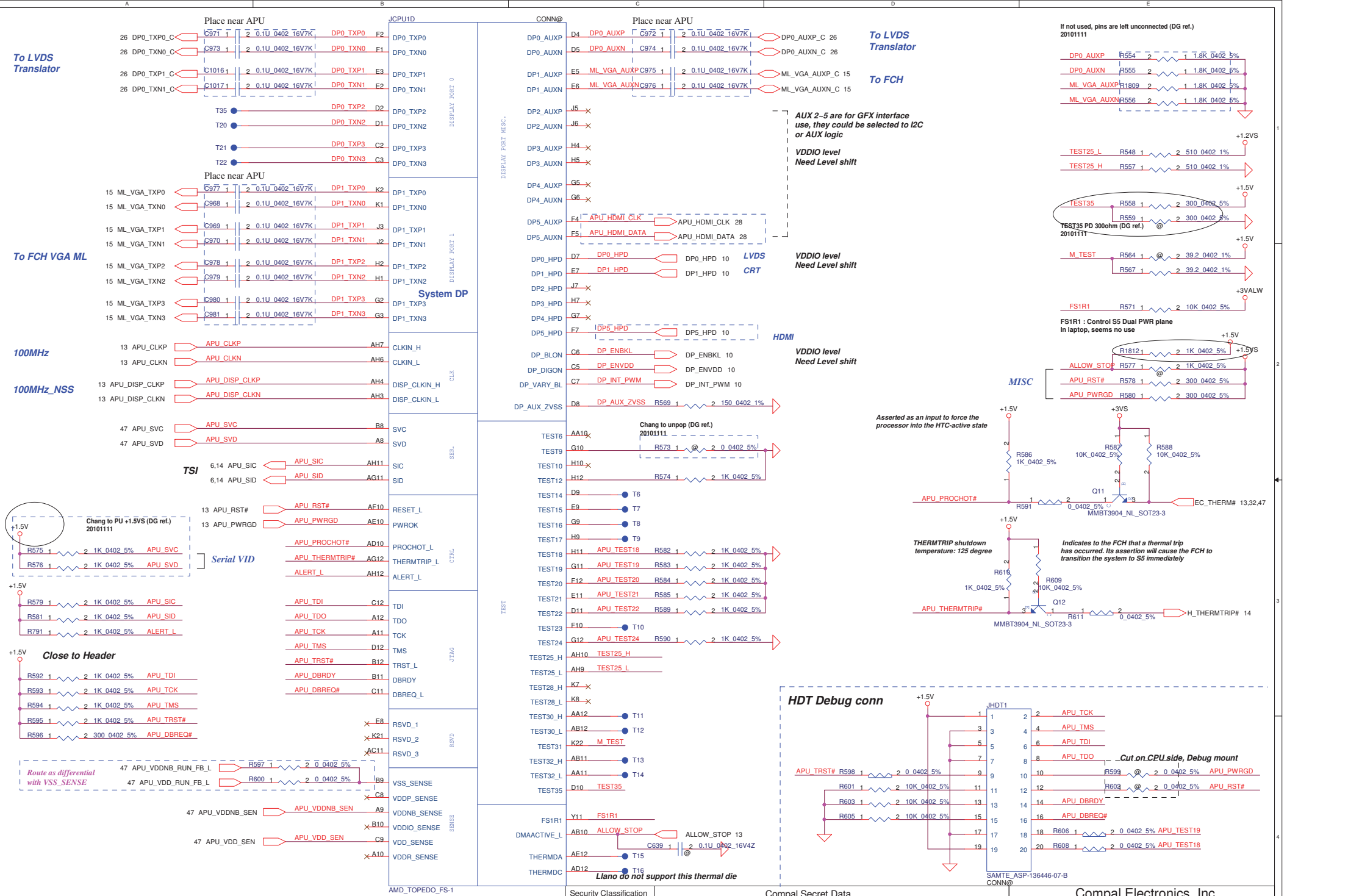
Issued Date	2010/08/04	Deciphered Date	2010/08/04

Compal Electronics, Inc.

Title: AMD FS1 DDRIII I/F

Size: B(28 Custom) | Document Number: QBL70 LA-7553P | Rev: 0.22

Date: Friday, April 29, 2011 | Sheet 7 of 51



Security Classification	Compal Secret Data		
Issued Date	2010/08/04	Deciphered Date	2010/08/04

Compal Electronics, Inc.

Title: AMD FS1 Display / MISC / HDT

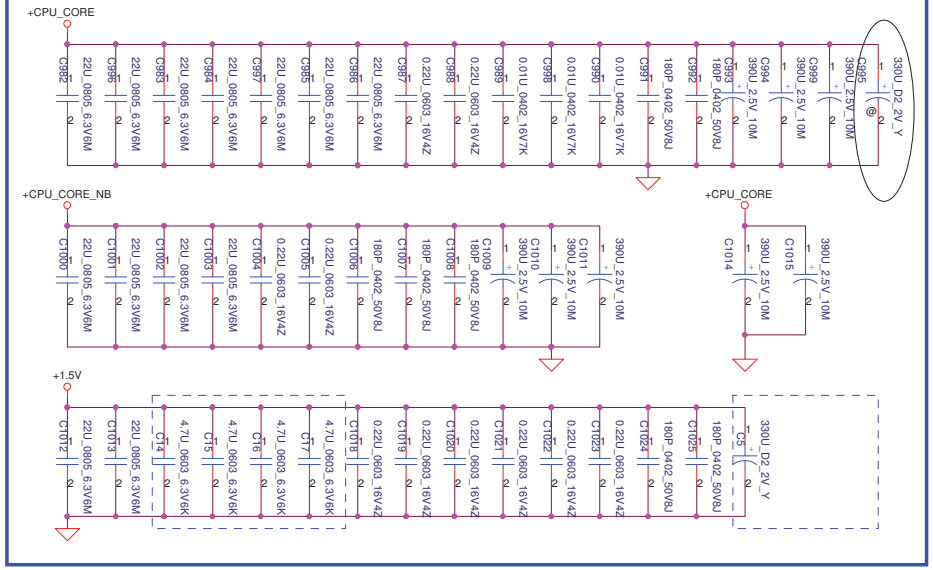
Size: B(28) Custom | Document Number: QBL70 LA-7553P | Rev: 0.22

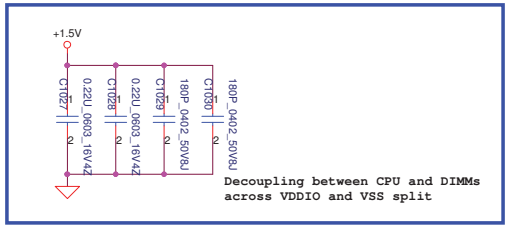
Date: Friday, April 29, 2011 | Sheet 8 of 51

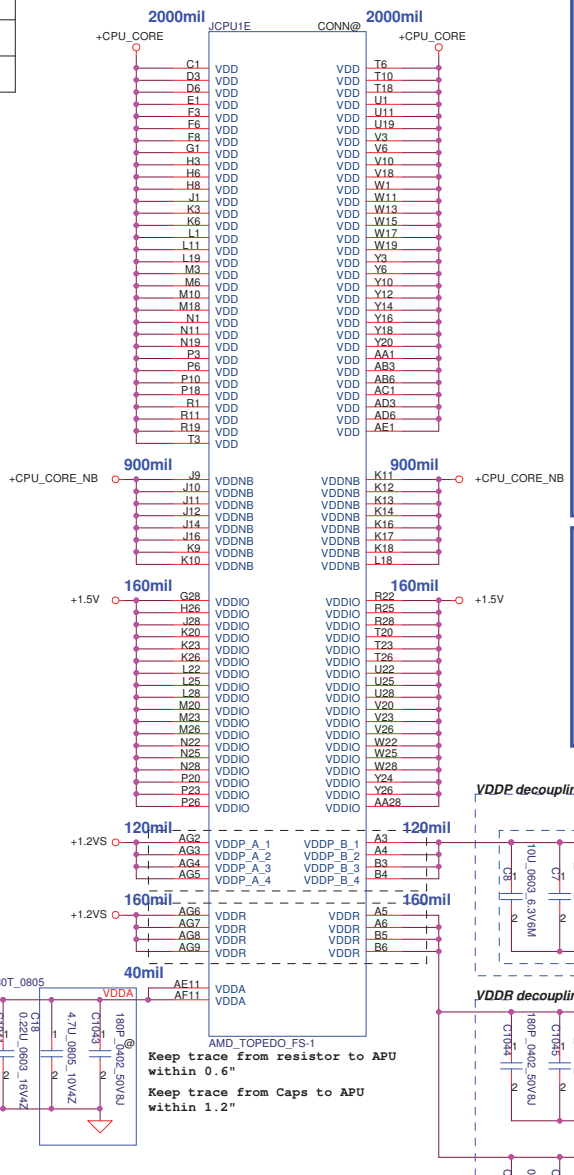
Power Name	Consumption
VDD +CPU_CORE	50A
VDDNB +CPU_CORE_NB	22.5A
VDDIO +1.5V	4A
VDDP / VDDR +1.2VS	3A / 3.5A
VDDA +2.5VS	0.75A

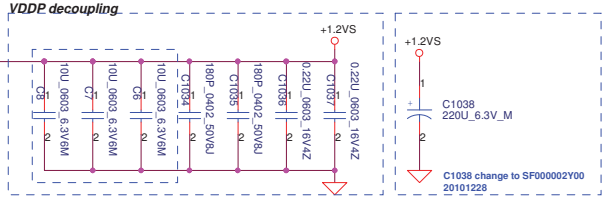
CORE_NB	CPU_CORE
330uF X 2	330uF X 4
22uF X 4	22uF X 11

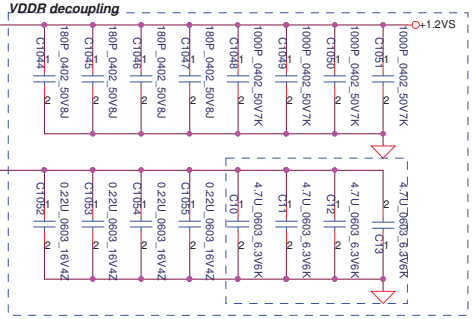
CPU BOTTOM SIDE DECOUPLING

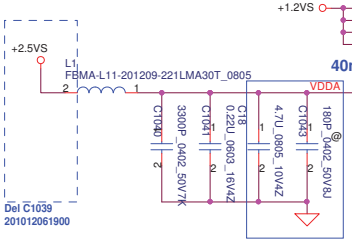






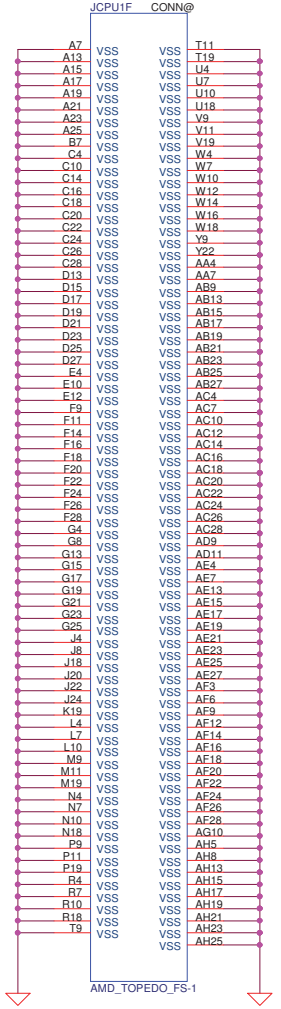






Keep trace from resistor to APU within 0.6"

Keep trace from Caps to APU within 1.2"



Demo Board Capacitor (include PWM side)

CPU_CORE	CORE_NB	VDDIO_SUS (CPU side)	VDDIO_SUS (DIMM x2)	VDDP/R_PWM	VDDP	VDDR
470uF x 6	470uF x 4	680uF x 1	100uF x 4	470uF x 2	10uF x 3	4.7uF x 4
22uF x 9	22uF x 6	330uF x 1	0.1uF	10uF x 1	0.22uF x 2	0.22uF x 4
0.22uF x 2	0.22uF x 2	22uF x 3			180pF x 2	1nF x 4
180pF x 2	180uF x 3	4.7uF x 4				180pF x 4
10nF x 3		0.22uF x 6				
		180pF x 4				

Security Classification	Compal Secret Data		
Issued Date	2010/08/04	Deciphered Date	2010/08/04

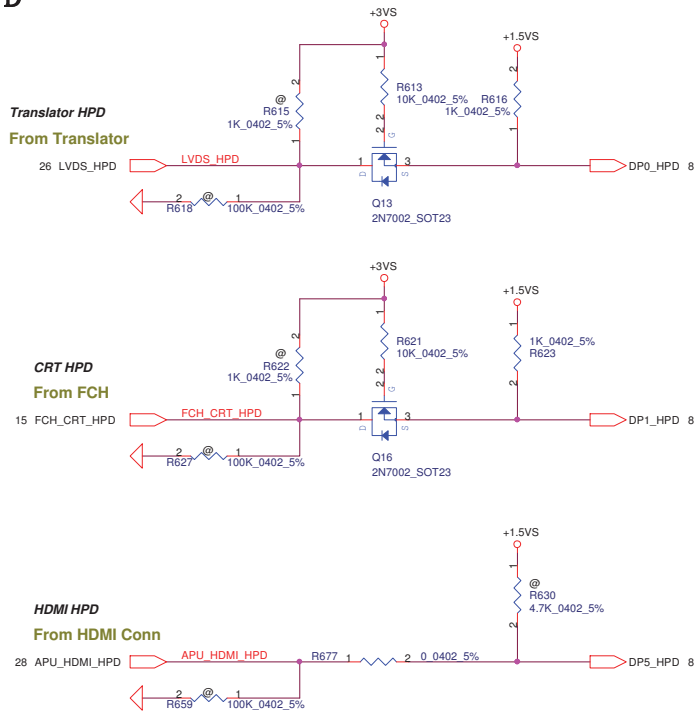
Compal Electronics, Inc.

Title: AMD FS1 PWR / GND

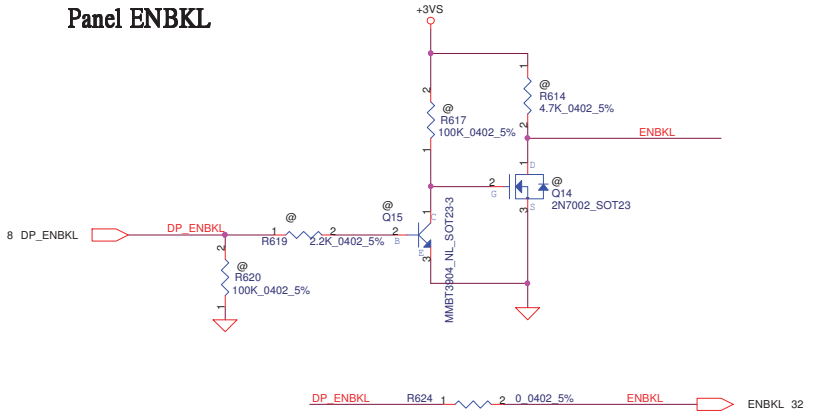
Size: Custom | Document Number: QBL70 LA-7553P | Rev: 0.22

Date: Friday, April 29, 2011 | Sheet 9 of 51

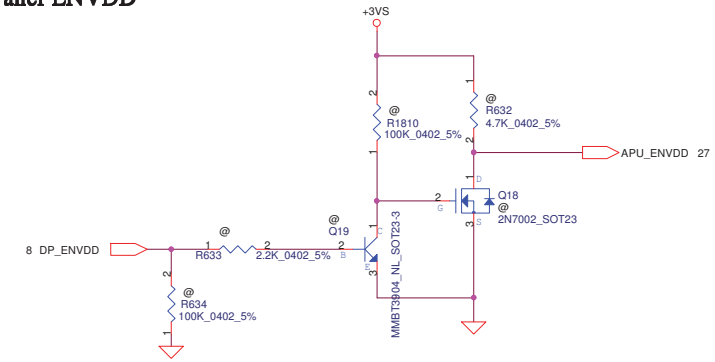
HPD



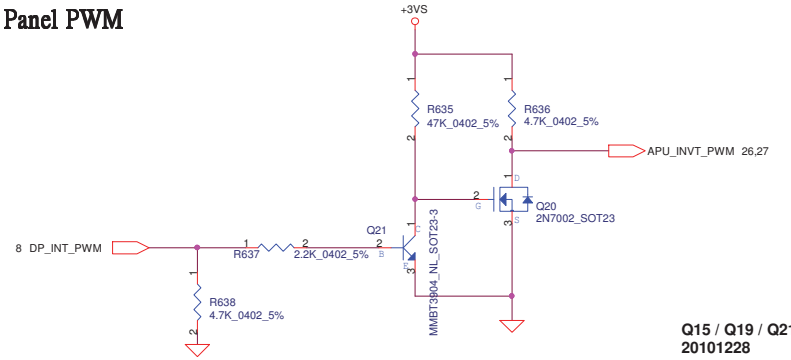
Panel ENBKL



Panel ENVDD



Panel PWM



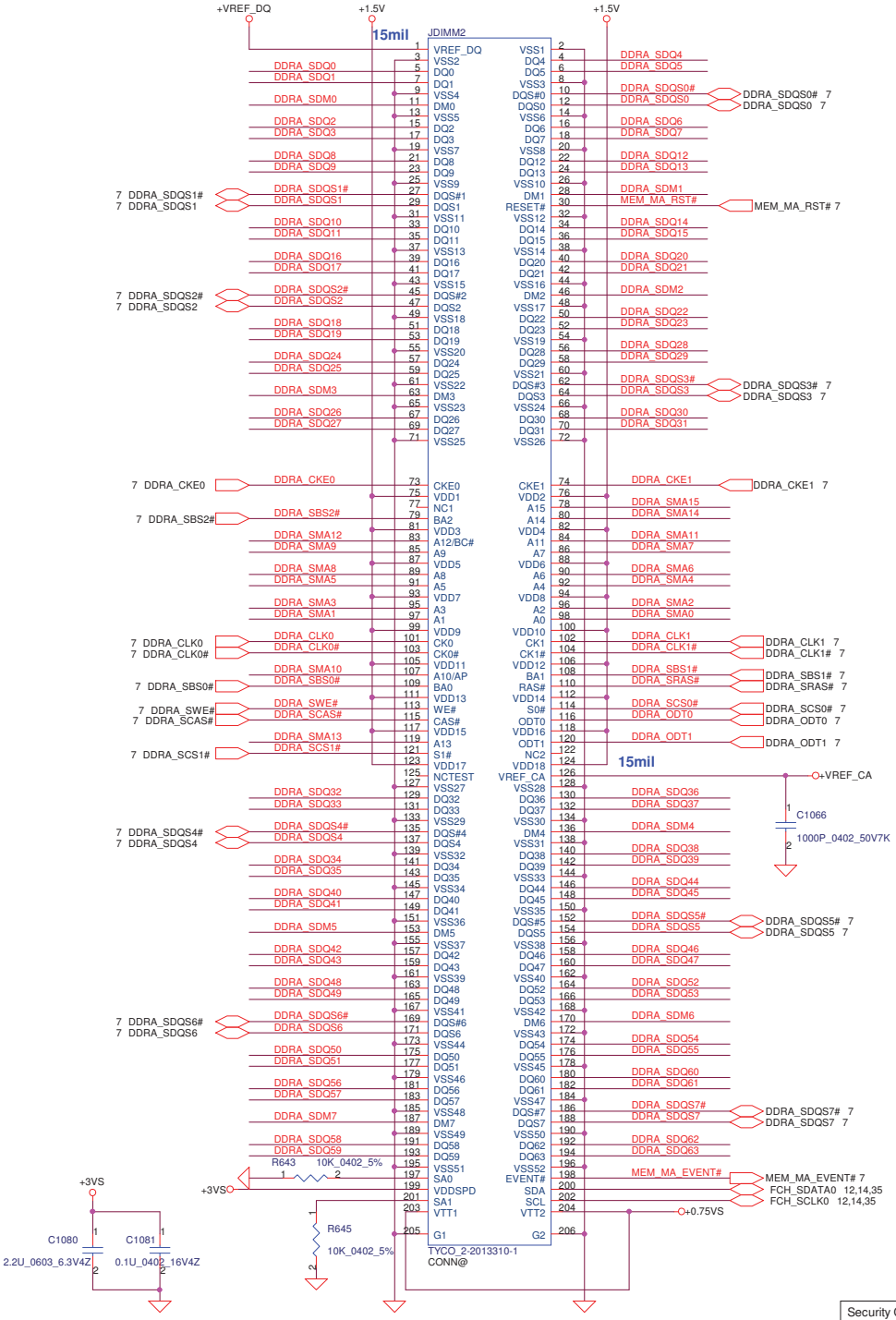
Q15 / Q19 / Q21 change to SB000006A00 20101228

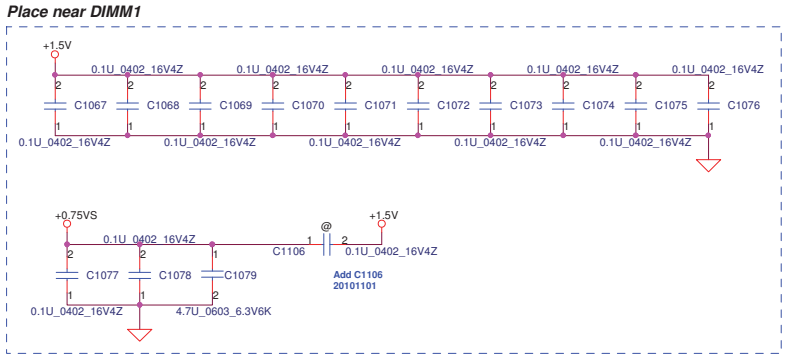
Security Classification	Compal Secret Data		
Issued Date	2010/08/04	Deciphered Date	2010/08/04

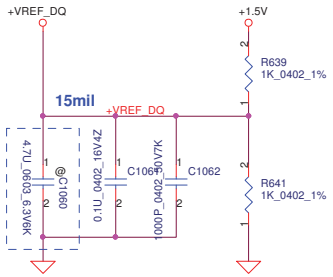
Title: AMD FS1 Singal Level Shifter

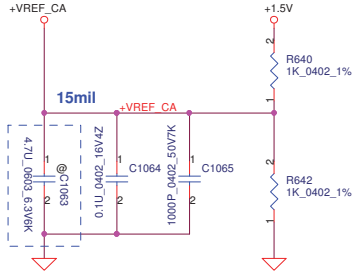
Size: Custom | Document Number: QBL70 LA-7553P | Rev: 0.22

Date: Friday, April 29, 2011 | Sheet 10 of 51









DIMM_A STD H:9.2mm

<Address: 00>

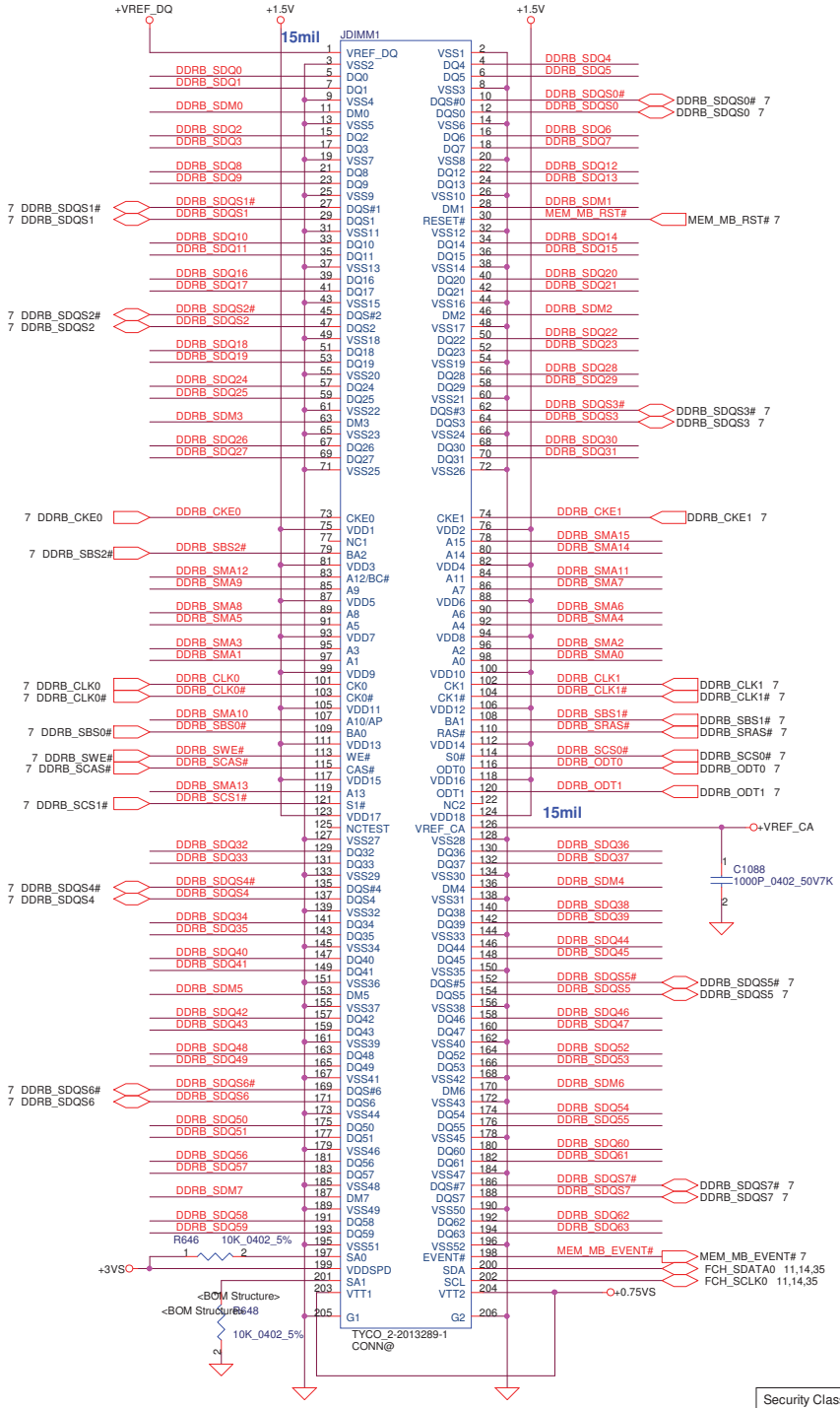
Security Classification	Compal Secret Data		
Issued Date	2010/08/04	Deciphered Date	2010/08/04

Compal Electronics, Inc.

Title: DDRIII SO-DIMM 2

Size: B (Custom) | Document Number: QBL70 LA-7553P | Rev: 0.22

Date: Friday, April 29, 2011 | Sheet 11 of 51



DIMM_B STD H:5.2mm

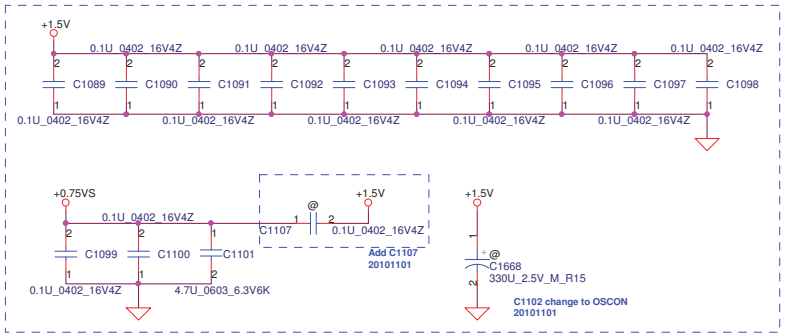
<Address: 01>

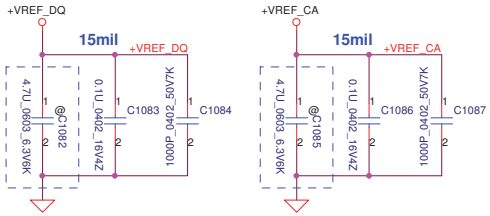
DDRB_SDQ[0..63] → DDRB_SDQ[0..63] 7

DDRB_SDM[0..7] → DDRB_SDM[0..7] 7

DDRB_SMA[0..15] → DDRB_SMA[0..15] 7

Place near DIMM2





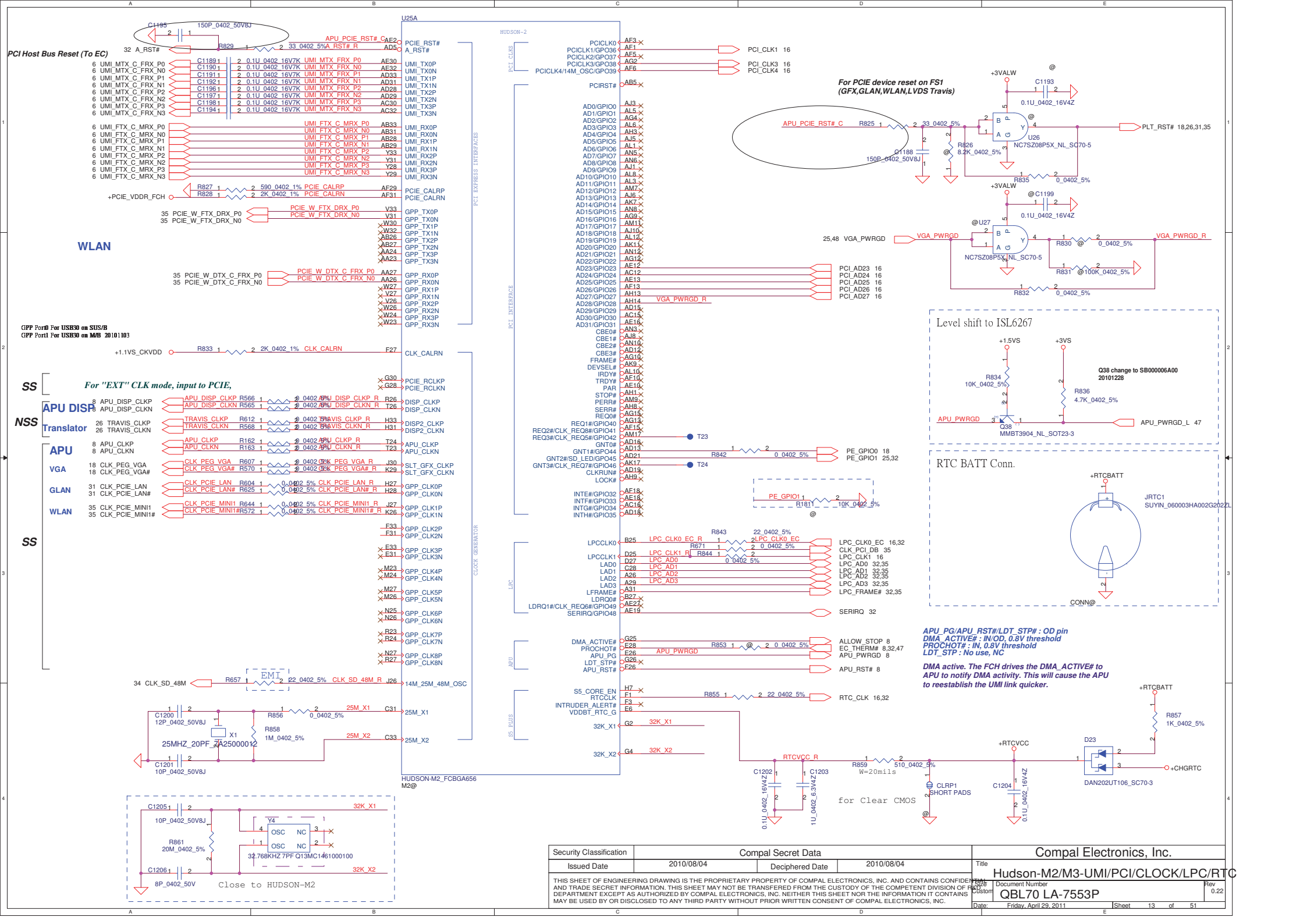
Security Classification	Compal Secret Data		
Issued Date	2010/08/04	Deciphered Date	2010/08/04

Compal Electronics, Inc.

Title: DDRIII SO-DIMM 1

Size: B (Custom) | Document Number: QBL70 LA-7553P | Rev: 0.22

Date: Friday, April 29, 2011 | Sheet 12 of 51



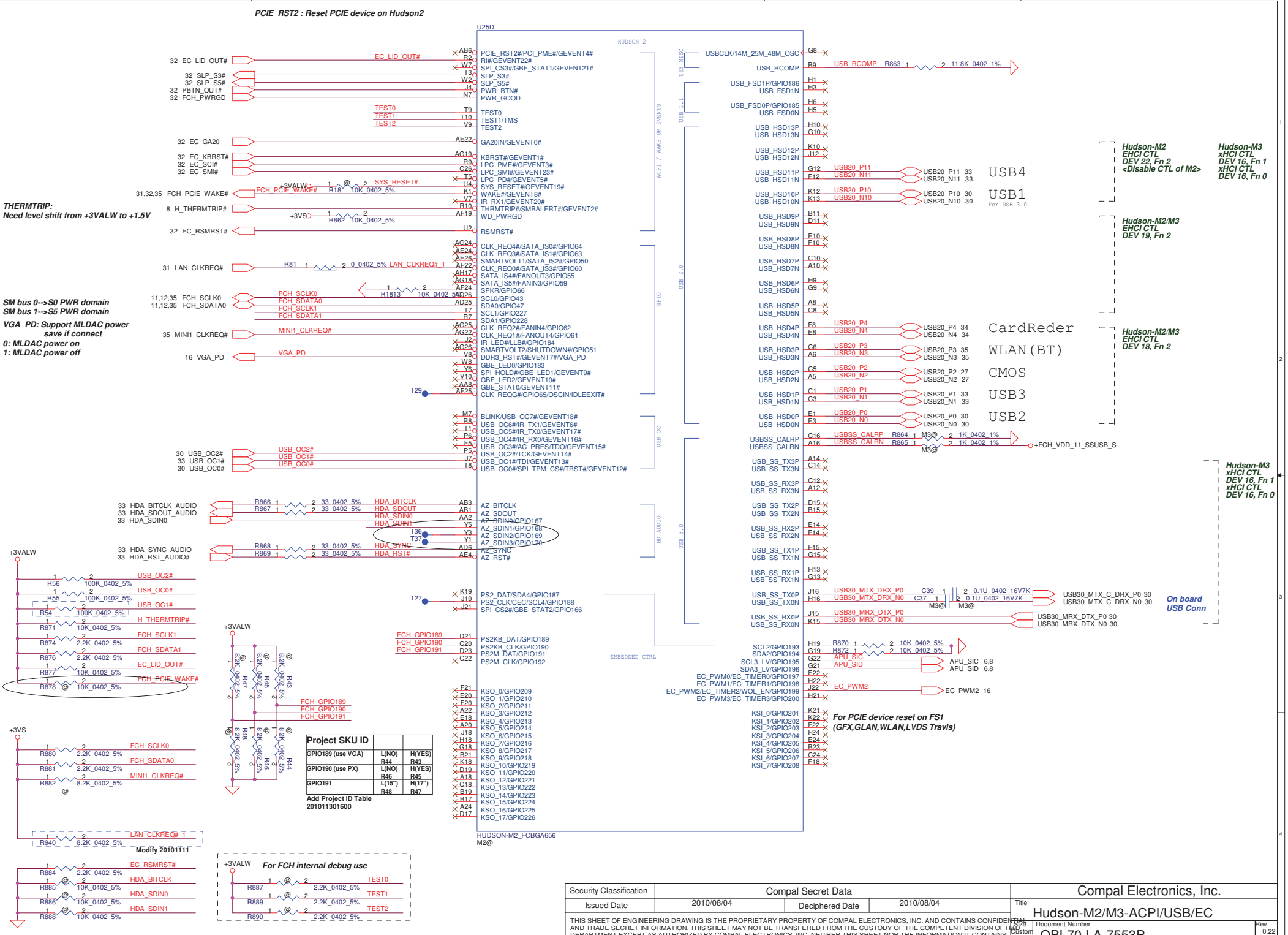
Security Classification	Compal Secret Data		
Issued Date	2010/08/04	Deciphered Date	2010/08/04

Compal Electronics, Inc.

Title: Hudson-M2/M3-UMI/PCI/CLOCK/LPC/RTC

Size: B2B | Document Number: QBL70 LA-7553P | Rev: 0.22

Date: Friday, April 29, 2011 | Sheet 13 of 51



Security Classification	Compal Secret Data		
Issued Date	2010/08/04	Deciphered Date	2010/08/04

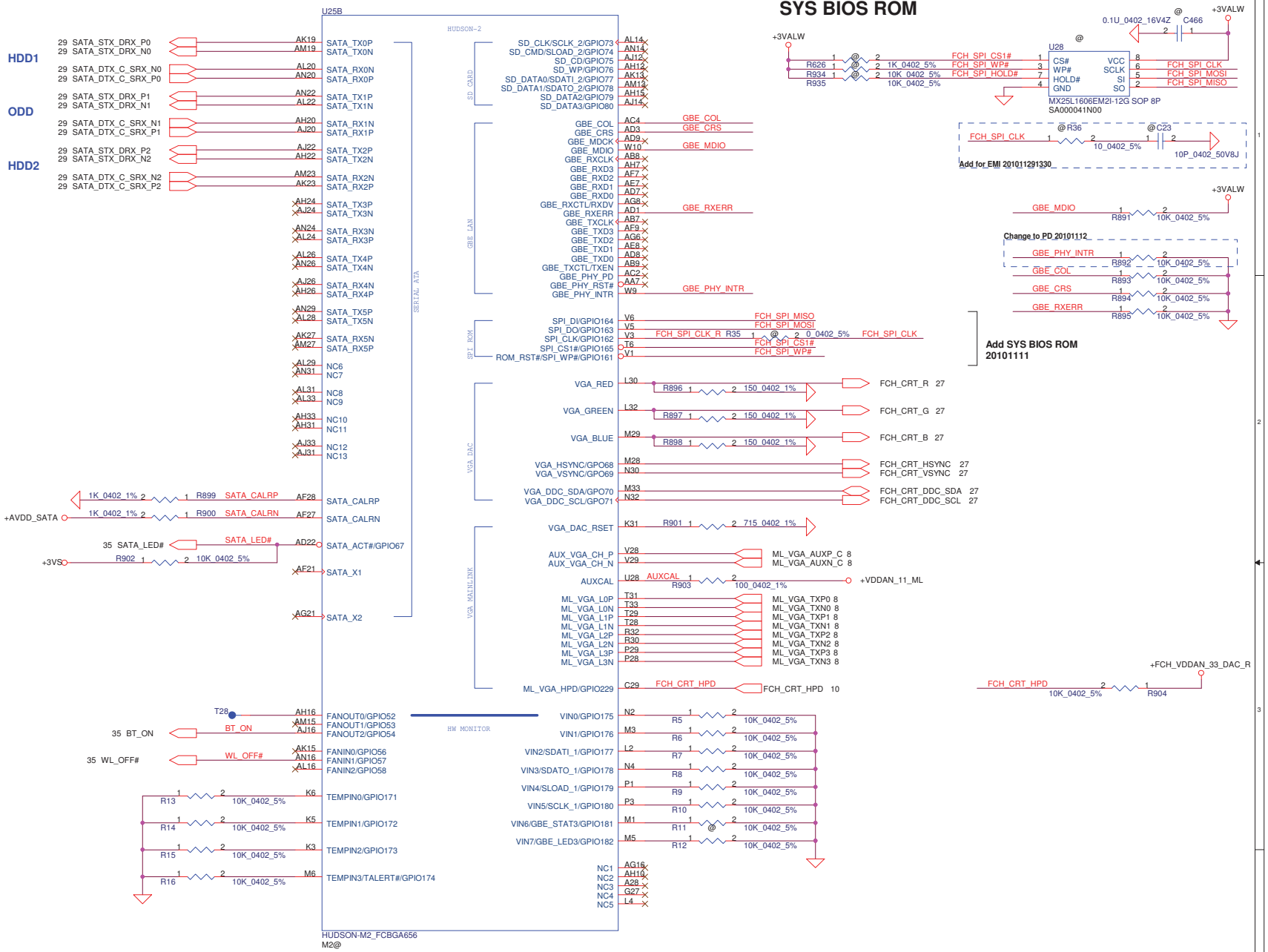
Compal Electronics, Inc.

Title: Hudson-M2/M3-ACPI/USB/EC

Size: B(28 Custom) | Document Number: QBL70 LA-7553P | Rev: 0.22

Date: Friday, April 29, 2011 | Sheet 14 of 51

SYS BIOS ROM



Security Classification	Compal Secret Data		
Issued Date	2010/08/04	Deciphered Date	2010/08/04

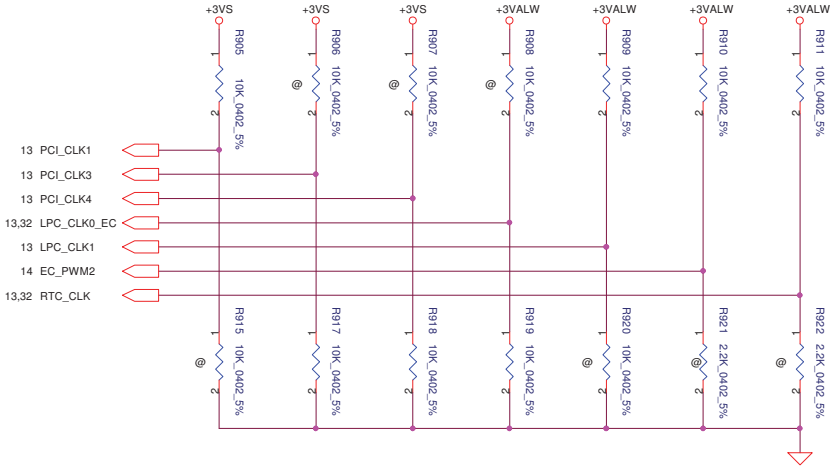
Compal Electronics, Inc.

Title: Hudson-M2/M3-SATA/GBE/HWM

Size: C (Custom)	Document Number: QBL70 LA-7553P	Rev: 0.22
Date: Friday, April 29, 2011	Sheet 15 of 51	

STRAP PINS

	PCI_CLK1	PCI_CLK3	PCI_CLK4	LPC_CLK0	LPC_CLK1	EC_PWM2	RTC_CLK
PULL HIGH	ALLOW PCIE GEN2 DEFAULT	USE DEBUG STRAPS	NON_FUSION CLOCK MODE	EC ENABLED	CLKGEN ENABLED DEFAULT	LPC ROM DEFAULT	S5 PLUS MODE DISABLED DEFAULT
PULL LOW	FORCE PCIE GEN1	IGNORE DEBUG STRAP DEFAULT	FUSION CLOCK MODE DEFAULT	EC DISABLED DEFAULT	CLKGEN DISABLE	SPI ROM	S5 PLUS MODE ENABLED

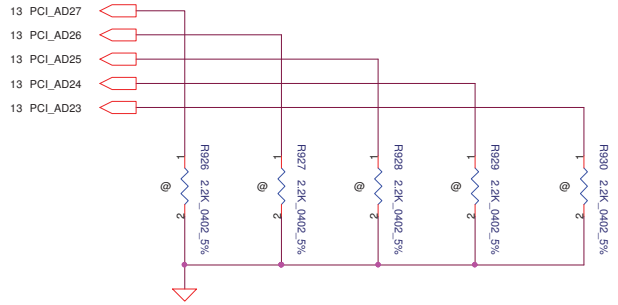


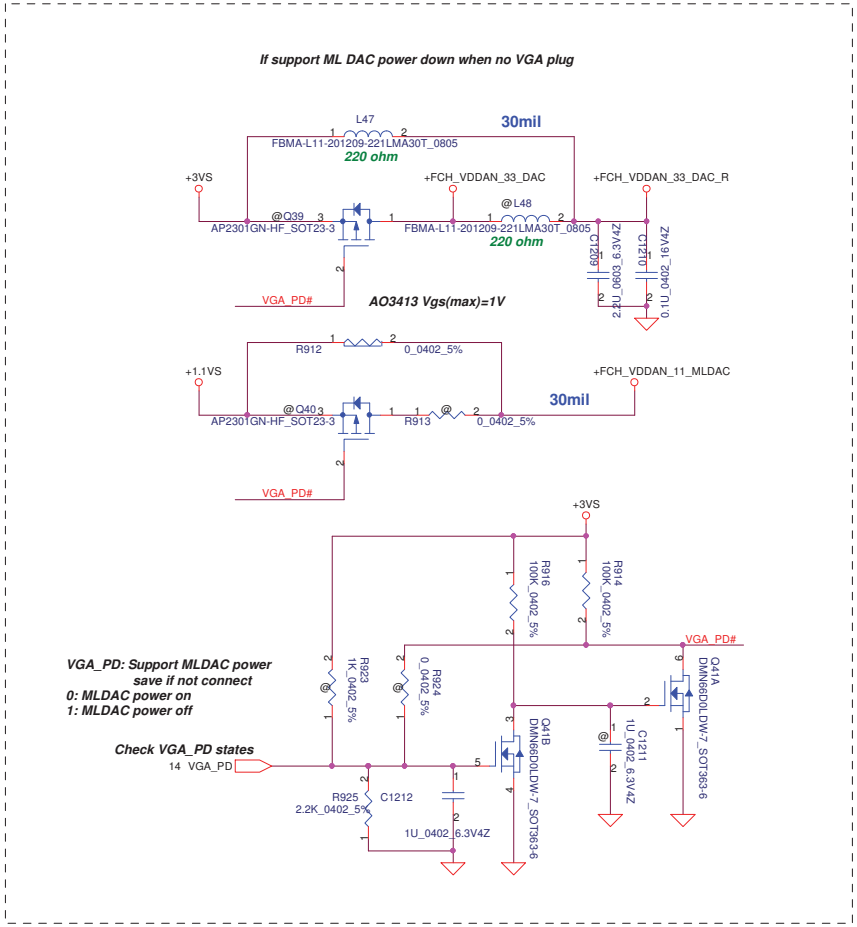
DEBUG STRAPS

FCH HAS 15K INTERNAL PU FOR PCI_AD[27:23]

PCI_AD26

	PCI_AD27		PCI_AD25	PCI_AD24	PCI_AD23
PULL HIGH	USE PCI PLL DEFAULT	DISABLE ILA AUTORUN DEFAULT	USE FC PLL DEFAULT	USE DEFAULT PCIE STRAPS DEFAULT	DISABLE PCI MEM BOOT DEFAULT
PULL LOW	BYPASS PCI PLL	ENABLE ILA AUTORUN	BYPASS FC PLL	USE EEPROM PCIE STRAPS	ENABLE PCI MEM BOOT





Security Classification	Compal Secret Data		
Issued Date	2010/08/04	Deciphered Date	2010/08/04

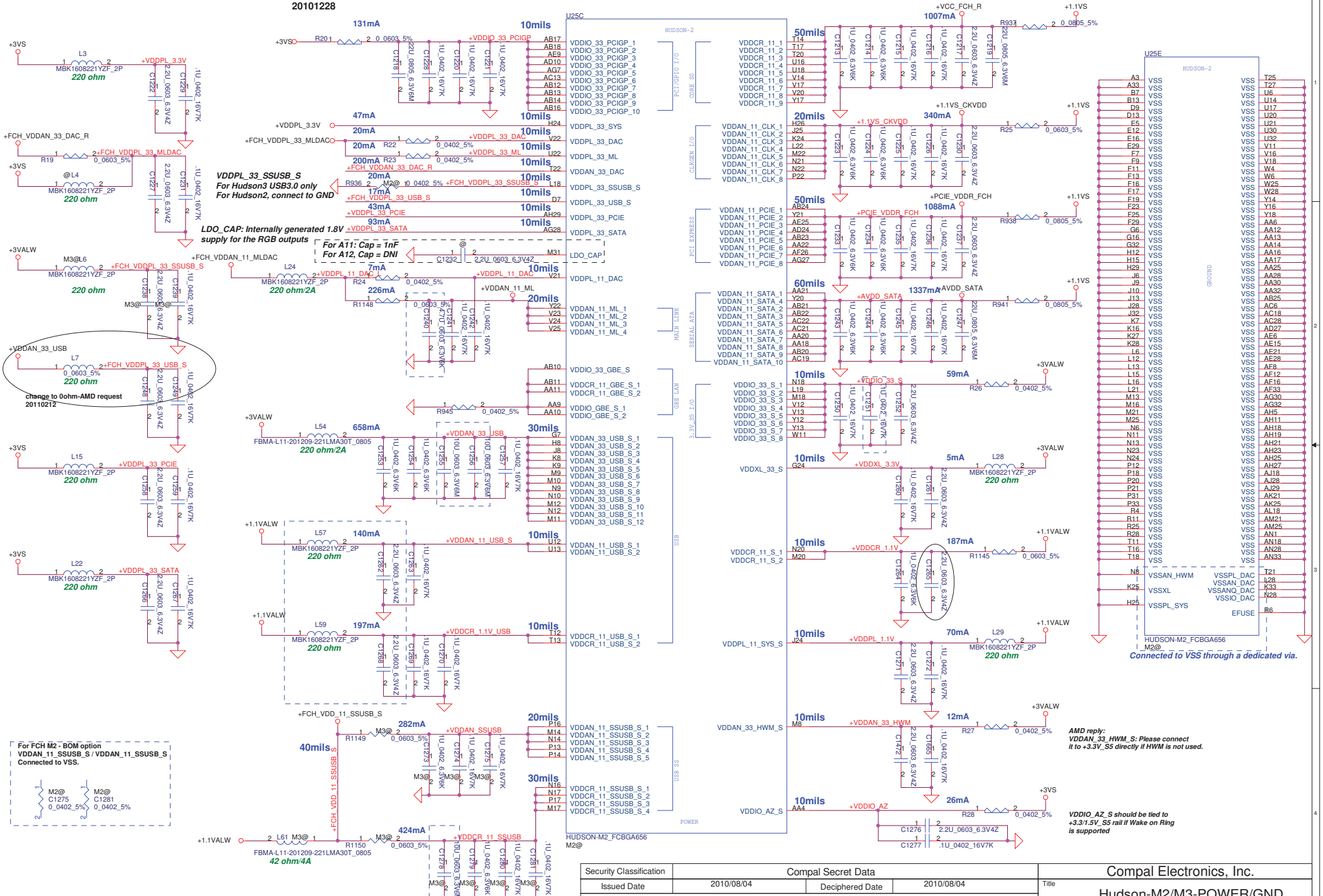
Compal Electronics, Inc.

Title: Hudson-M2/M3-STRAP

Size: B28 Custom | Document Number: QBL70 LA-7553P | Rev: 0.22

Date: Friday, April 29, 2011 | Sheet 16 of 51

C1218 / C1219 / C1247 Change to SE00000I10
20101228



Security Classification	Compal Secret Data		
Issued Date	2010/08/04	Deciphered Date	2010/08/04

Compal Electronics, Inc.

Title: Hudson-M2/M3-POWER/GND

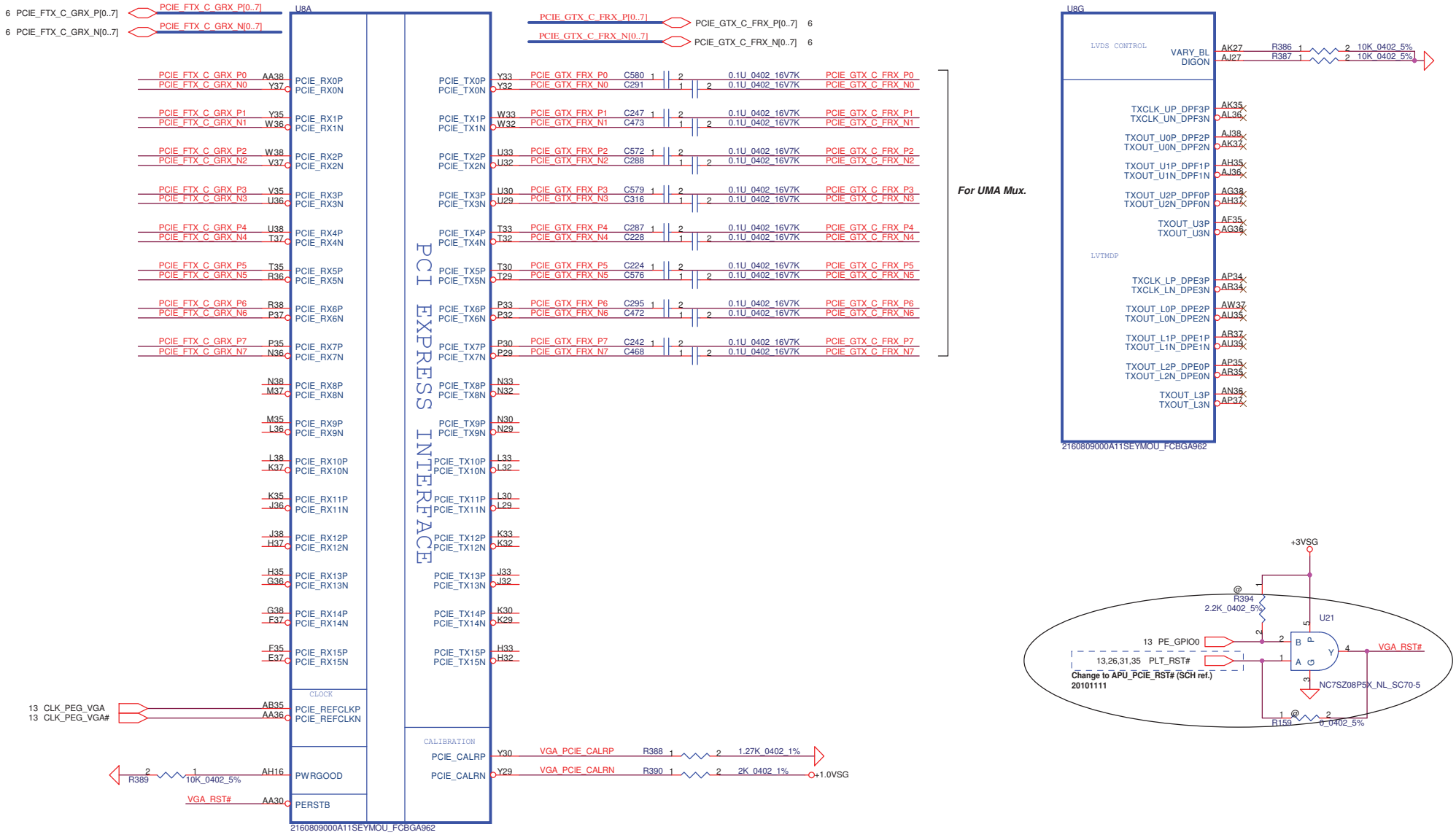
Size: Custom | Document Number: QBL70 LA-7553P | Rev: 0.22

Date: Friday, April 29, 2011 | Sheet 17 of 51

GFX PCIE LANE REVERSAL

<DIGON>
Controls panel digital power on/off.
Active High ,external PD need

<VARY_BL>
LCD PWM (pulse width modulated) output to adjust LCD brightness
Active High ,external PD need



Security Classification	Compal Secret Data		
Issued Date	2010/07/12	Deciphered Date	2012/07/12

Compal Electronics, Inc.

Title: Vancouver_ PCIE / LVDS

Size: Custom | Document Number: QBL70 LA-7553P | Rev: 0.22

Date: Friday, April 29, 2011 | Sheet 18 of 51

Strap Name		Pin Straps description <all internal PD>	Setting
VIP_DEVICE_EN	V2SYNC (GENLK_VSYNC)	VIP Device Strap Enable indicates to the software driver (Internal PD) 0: Driver would ignore the value sampled on VHAD_0 during reset 1: VHAD_0 to determine whether or not a VIP slave device	0
VGA_DIS	GPIO9	VGA Disable determines (Internal PD) 0: VGA Controller capacity enabled 1: The device will not be recognized as the system's VGA controller	0
TX_PWRS_ENB	GPIO0	Transmitter Power Saving Enable (Internal PD) 0: 50% Tx output swing 1: full Tx output swing	1
TX_DEEMPH_EN	GPIO1	PCI Express Transmitter De-emphasis Enable (Internal PD) 0: Tx de-emphasis diabled 1: Tx de-emphasis enabled	1
CONFIG[2] CONFIG[1] CONFIG[0]	GPIO13 GPIO12 GPIO11	GPIO13,12,11 (config 2,1,0) : (Internal PD) memory apertures a) If BIOS_ROM_EN = 1, then Config[2:0] defines CONFIG[3:0] the ROM type. 128 MB 000 b) If BIOS_ROM_EN = 0, then Config[2:0] defines 256 MB 001 * the primary memory aperture size. 64 MB 010	001
BIOS_ROM_EN	GPIO22	Enable external BIOS ROM device (Internal PD) 0: Diable, 1: Enable	0
AUD[1] AUD(0)	HSYNC VSYNC	00: No audio function; 10: Audio for DisplayPort only; 01: Audio for DisplayPort and HDMI if adapter is detected; 11: Audio for both DisplayPort and HDMI	00
BIF_GEN2_EN	GPIO2	0= Advertises the PCI-E device as 2.5 GT/s capable at power-on 1= Advertises the PCI-E device as 5.0 GT/s capable at power-on 5.0 GT/s capability will be controlled by software	1
RESERVED	H2SYNC (GENLK_CLK) GPIO8 GPIO21	Internal use only. THIS PAD HAS AN INTERNAL PULL-DOWN AND MUST BE 0 V AT RESET. The pad may be left unconnected	DNI

Don't have this strap on Whistler and Seymour

NC on Park, Robson and Seymour
NC on Park, Robson

NC on Park, Robson and Seymour

Global Swap Lock on Multiple GPUs

NC on Park, Robson and Seymour

Not share via for other GND

External VGA Thermal Sensor

U9 @ ADM1032ARMZ-2REEL_MSOP8

VGA_SMB_CK2, VGA_SMB_DA2, THM_ALERT#, GPU_THERM_D+, GPU_THERM_D-, +3VSG

Q8A DMN66D0LDW-7_SOT363-6 — EC_SMB_CK2 6,32
Q8B DMN66D0LDW-7_SOT363-6 — EC_SMB_DA2 6,32

SM_DA2 R1816 0_0402_5% VGA_GPIO3
SM_CK2 R1817 0_0402_5% VGA_GPIO4

VRAM ID

VRAM_ID0, VRAM_ID1, VRAM_ID2, VRAM_ID3

GPIO5 fast-power reduction:
HW control will casue display disturb should use SW method control
GPIO6 voltage control signal ,No use can NC

Move to DDCCLK_AUX3P,DDCDATA_AUX3N

GPIO7 Controls backlight on/off.
Active High ,need external PD
If GPIO22 High ,GPIO 11-13->CFG[0:2]
Config ROM type ,GPU has internal PD

GPIO6,15,16,20
Voltage control signal
GPIO6,15 no use can NC
Thermal monitor interrupt

Critical temperature fault

Reserved

External BIOS device
ON(1)/OFF(0) inter PD

Internal Debug
no use can floating
ON(1)/OFF(0)

Stereo Sync
no use can NC

For ATI Cross fire
no use can NC

VGA_ENBKL, ROM, GPU_VID0, GPU_VID1, THM_ALERT#, GPIO_22_ROMCSB

SM010030010
200ma 120ohm@100mhz DCR 0.2

Future ASIC call MLPS.
OLD ASIC is Fan PWM

120ohm/0.3A

HSYNC:VSYNC
11: Audio for both DisplayPort and HDMI

AUD Strap

70mA AVDD/AVSSQ
100mA VDD1DI/VSS1DI
AMD ref:120ohm/0.3A

NC on Whistler and Seymour
BLM18AG121SN1D_0603
AMD ref:120ohm/0.3A
SM010030010
200ma 120ohm@100mhz DCR 0.2

Back compatibility(Manhattan)

Whistler and Seymour
Except A2VSSQ change to TSVSSQ, others are NC

100mA VDDQ2DI/VSS2DI
100mA A2VDD
2mA A2VDDQ/A2VSSQ

75mA DPLL_PVDD/DPLL_PVSS
125mA DPLL_VDDC
20mA TSVDD/TSVSS

NC on Park, Robson and Seymour

GPIO8 Serial-ROM output from ROM. GPIO9 Serial-ROM input to ROM. GPIO10 Serial-ROM clock to ROM. GPIO22 erternal BIOS-ROM enable	if GPIO22 High ,GPIO 11-13->CFG[0:2] Config ROM type ,GPU has internal PD if GPIO22 Low ,GPIO 11-13->CFG[0:2] Config Primary memory-aperture size CFG[3:0] 128MB 000 256MB 001 * 64MB 010
GPIO8,GPIO9,GPIO10 no use can NC GPIO22 Enable need 3K PH ,no use must NC	

Seymour(XT)

VRAM \ Location	VRAM_ID3	VRAM_ID2	VRAM_ID1	VRAM_ID0
Samsung SA00004G530 64M16 K4W1G1646G-BC11	0	0	0	0
Samsung SA000047QA0 128M16 K4W2G1646C-HC11	0	0	0	1
Hynix SA000041S60 64M16 H5TQ1G63DFR-11C	0	1	0	0
Hynix SA00003YO30 128M16 H5TQ2G63BFR-11C	0	1	0	1

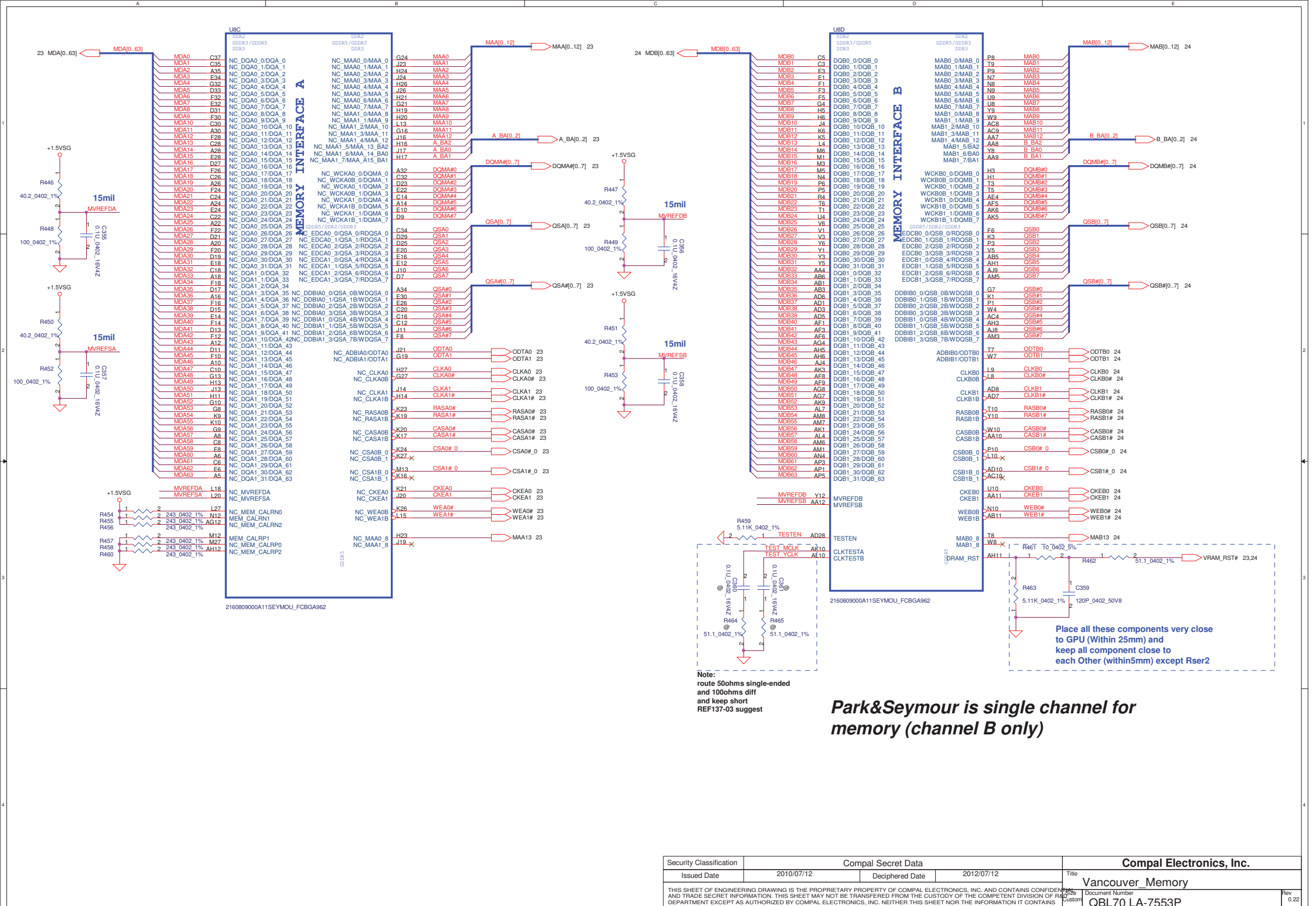
Security Classification	Compal Secret Data		
Issued Date	2010/07/12	Deciphered Date	2012/07/12

Compal Electronics, Inc.

Title: Vancouver_Strape/DP/HDMI//CRT

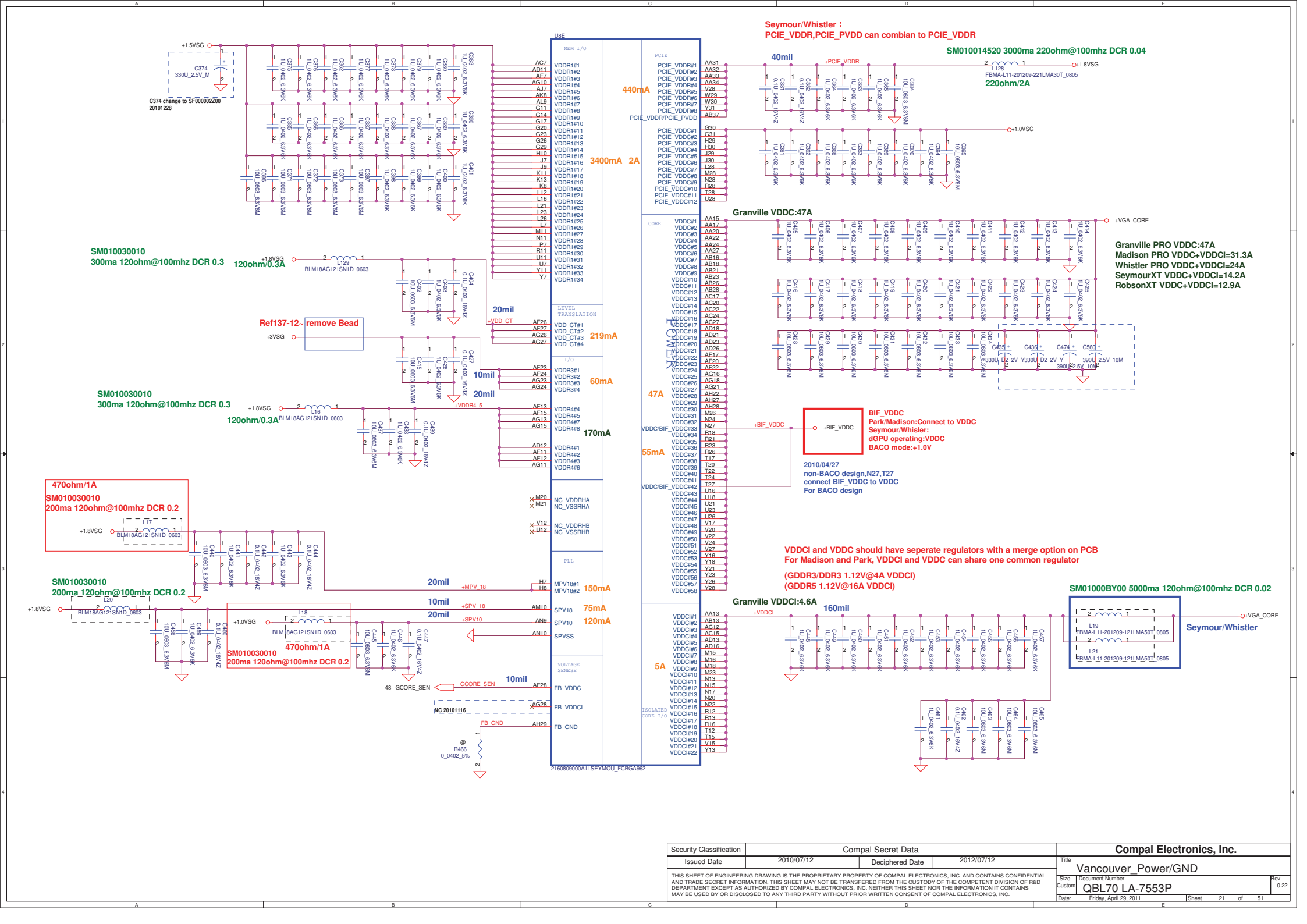
Size: Custom | Document Number: QBL70 LA-7553P | Rev: 0.22

Date: Friday, April 29, 2011 | Sheet 19 of 51



Security Classification	Compal Secret Data		
Issued Date	2010/07/12	Deciphered Date	2012/07/12

Compal Electronics, Inc.	
Title	Vancouver_Memory
Size: Custom	Document Number: QBL70 LA-7553P
Rev	0.22
Date: Friday, April 29, 2011	Sheet 20 of 51



Security Classification	Compal Secret Data		
Issued Date	2010/07/12	Deciphered Date	2012/07/12

Compal Electronics, Inc.

Title	Vancouver_Power/GND		
Size	Document Number		Rev
Custom	QBL70 LA-7553P		0.22
Date:	Friday, April 29, 2011	Sheet	21 of 51

DPA_VDD18,DPA_PVDD,DPB_VDD18,DPB_PVDD
can combian to DPAB_VDD18
DPC_VDD18,DPC_PVDD,DPD_VDD18,DPD_PVDD
can combian to DPCD_VDD18
(DPD_VDD18,DPD_PVDD not applicable on Robson/Park)
DPE_VDD18,DPE_PVDD,DPF_VDD18,DPF_PVDD
can combian to DPEF_VDD18

DPx-VSSR,DPx_PVSS can combian to DP_VSSR
(Manhatann should have individual GND)
where x is A,B,C,D,E,F

Seymour/Whistler :
DPA_VDD10,DPB_VDD10
can combian to DPAB_VDD10
DPC_VDD10,DPD_VDD10
can combian to DPCD_VDD10
DPE_VDD10,DPD_VDD10
can combian to DPEF_VDD10

U8F

GND

PCIE_VSS#1 AB39
PCIE_VSS#2 E39
PCIE_VSS#3 F34
PCIE_VSS#4 F39
PCIE_VSS#5 G33
PCIE_VSS#6 G34
PCIE_VSS#7 H31
PCIE_VSS#8 H34
PCIE_VSS#9 H39
PCIE_VSS#10 J31
PCIE_VSS#11 J34
PCIE_VSS#12 K31
PCIE_VSS#13 K34
PCIE_VSS#14 K39
PCIE_VSS#15 L31
PCIE_VSS#16 L34
PCIE_VSS#17 M34
PCIE_VSS#18 M39
PCIE_VSS#19 N31
PCIE_VSS#20 N34
PCIE_VSS#21 P31
PCIE_VSS#22 P34
PCIE_VSS#23 P39
PCIE_VSS#24 R34
PCIE_VSS#25 T31
PCIE_VSS#26 T34
PCIE_VSS#27 T39
PCIE_VSS#28 U31
PCIE_VSS#29 U34
PCIE_VSS#30 V34
PCIE_VSS#31 V39
PCIE_VSS#32 W31
PCIE_VSS#33 W34
PCIE_VSS#34 Y34
PCIE_VSS#35 Y39

GND#1 A3
GND#2 A37
GND#3 AA16
GND#4 AA18
GND#5 AA2
GND#6 AA21
GND#7 AA23
GND#8 AA26
GND#9 AA28
GND#10 AA6
GND#11 AB12
GND#12 AB15
GND#13 AB17
GND#14 AB20
GND#15 AB22
GND#16 AB24
GND#17 AB27
GND#18 AC11
GND#19 AC13
GND#20 AC16
GND#21 AC18
GND#22 AC2
GND#23 AC21
GND#24 AC23
GND#25 AC26
GND#26 AC28
GND#27 AC6
GND#28 AD15
GND#29 AD17
GND#30 AD20
GND#31 AD22
GND#32 AD24
GND#33 AD27
GND#34 AD9
GND#35 AE2
GND#36 AE6
GND#37 AF10
GND#38 AF16
GND#39 AF18
GND#40 AF21
GND#41 AG17
GND#42 AG2
GND#43 AG20
GND#44 AG22
GND#45 AG6
GND#46 AG9
GND#47 AH21
GND#48 AJ10
GND#49 AJ11
GND#50 AJ2
GND#51 AJ28
GND#52 AJ6
GND#53 AK11
GND#54 AK31
GND#55 AK7
GND#56 AL11
GND#57 AL14
GND#58 AL17
GND#59 AL2
GND#60 AL20
GND/PX_EN#61 AL21
GND#62 AL23
GND#63 AL26
GND#64 AL32
GND#65 AL6
GND#66 AL8
GND#67 AM11
GND#68 AM31
GND#69 AM9
GND#70 AN11
GND#71 AN2
GND#72 AN30
GND#73 AN6
GND#74 AN8
GND#75 AP11
GND#76 AP7
GND#77 AP9
GND#78 AR5
GND#79 B11
GND#80 B13
GND#81 B15
GND#82 B17
GND#83 B19
GND#84 B21
GND#85 B23
GND#86 B25
GND#87 B27
GND#88 B29
GND#89 B31
GND#90 B33
GND#91 B7
GND#92 B9
GND#93 C1
GND#94 C39
GND#95 E35
GND#96 E5
GND#97 F11
GND#98 F13

VSS_MECH#1 A39
VSS_MECH#2 AW1
VSS_MECH#3 AW39

GND#100 F15
GND#101 F17
GND#102 F19
GND#103 F21
GND#104 F23
GND#105 F25
GND#106 F27
GND#107 F29
GND#108 F31
GND#109 F33
GND#110 F7
GND#111 F9
GND#112 G2
GND#113 G6
GND#114 H9
GND#115 J2
GND#116 J27
GND#117 J6
GND#118 J8
GND#119 K14
GND#120 K7
GND#121 L11
GND#122 L17
GND#123 L2
GND#124 L22
GND#125 L24
GND#126 L6
GND#127 M17
GND#128 M22
GND#129 M24
GND#130 N16
GND#131 N18
GND#132 N2
GND#133 N21
GND#134 N23
GND#135 N26
GND#136 N6
GND#137 R15
GND#138 R17
GND#139 R2
GND#140 R20
GND#141 R22
GND#142 R24
GND#143 R27
GND#144 R6
GND#145 T11
GND#146 T13
GND#147 T16
GND#148 T18
GND#149 T21
GND#150 T23
GND#151 T26
GND#153 U15
GND#154 U17
GND#155 U2
GND#156 U20
GND#157 U22
GND#158 U24
GND#159 U27
GND#160 U6
GND#161 V11
GND#163 V16
GND#164 V18
GND#165 V21
GND#166 V23
GND#167 V26
GND#168 W2
GND#169 W6
GND#170 Y15
GND#171 Y17
GND#172 Y20
GND#173 Y22
GND#174 Y24
GND#175 Y27
GND#152 U13
GND#162 V13

2160809000A11SEYMOU_FCBGA962

REF137-13 update

PX_EN
PX_EN 25,32

PX_EN: PU at P.20
SBIOS will control VGA power on/off.
High :BACO mode enable
LOW:BACO disable

U8H

DP C/D POWER
DP A/B POWER
DP E/F POWER
DP PLL POWER

Manhatann:300mA
Seymour:150mA
20mil
+DPABCD_VDD18
AP20 AP21
DPCD/DPC_VDD18#1 DPCD/DPC_VDD18#2
DPAB/DPA_VDD18#1 DPAB/DPA_VDD18#2
AN24 AP24
20mil
+DPABCD_VDD18
300mA
SM01000BL00
1000ma 470ohm@100mhz DCR 0.2
L23
MBK1608221YZF_2P
+1.8VSG
FootPrint
C469 10U_0603_6.3V6M
C470 0.1U_0402_16V4Z
C471 1U_0402_6.3V6K

20mil
+DPABCD_VDD10
AP13 AT13
DPCD/DPC_VDD10#1 DPCD/DPC_VDD10#2
DPAB/DPA_VDD10#1 DPAB/DPA_VDD10#2
AN31 AP32
20mil
+DPABCD_VDD10

AN17 AP16 AP17 AW14 AW16
DP/DPC_VSSR#1 DP/DPC_VSSR#2 DP/DPC_VSSR#3 DP/DPC_VSSR#4 DP/DPC_VSSR#5
DP/DPA_VSSR#1 DP/DPA_VSSR#2 DP/DPA_VSSR#3 DP/DPA_VSSR#4 DP/DPA_VSSR#5
AN27 AP27 AP28 AW24 AW26

20mil
+DPABCD_VDD18
AP22 AP23
DPCD/DPD_VDD18#1 DPCD/DPD_VDD18#2
DPAB/DPB_VDD18#1 DPAB/DPB_VDD18#2
AP25 AP26
20mil
+DPABCD_VDD18

Manhatann:220mA
Seymour:110mA
20mil
+DPABCD_VDD10
AP14 AP15
DPCD/DPD_VDD10#1 DPCD/DPD_VDD10#2
DPAB/DPB_VDD10#1 DPAB/DPB_VDD10#2
AN33 AP33
20mil
+DPABCD_VDD10
220mA
SM01000BL00
1000ma 470ohm@100mhz DCR 0.2
L25
MBK1608221YZF_2P
+1.0VSG
FootPrint
C475 0.1U_0402_16V4Z
C476 1U_0402_6.3V6K
C477 10U_0603_6.3V6M

AN19 AP18 AP19 AW20 AW22
DP/DPD_VSSR#1 DP/DPD_VSSR#2 DP/DPD_VSSR#3 DP/DPD_VSSR#4 DP/DPD_VSSR#5
DP/DPB_VSSR#1 DP/DPB_VSSR#2 DP/DPB_VSSR#3 DP/DPB_VSSR#4 DP/DPB_VSSR#5
AN29 AP29 AP30 AW30 AW32

R467 150_0402_1%
R468 150_0402_1%

DP mode:300mA
LVDS mode:440mA
SM01000BL00
1000ma 470ohm@100mhz DCR 0.2
L26
MBK1608221YZF_2P
+1.8VSG
FootPrint
C478 10U_0603_6.3V6M
C479 1U_0402_6.3V6K
C480 0.1U_0402_16V4Z

DPCD_CALR
DPAB_CALR
AW18
AW28

20mil
+DPEF_VDD18
AH34 AJ34
DPEF/DPE_VDD18#1 DPEF/DPE_VDD18#2
DPAB_VDD18/DPA_PVDD DP_VSSR/DPA_PVSS
AU28 AV27
20mA
10mil
+DPABCD_VDD18

20mil
+DPEF_VDD10
AL33 AM33
DPEF/DPE_VDD10#1 DPEF/DPE_VDD10#2
DPAB_VDD18/DPB_PVDD DP_VSSR/DPB_PVSS
AV29 AR28
20mA
10mil
+DPABCD_VDD18

AN34 AP39 AR39 AU37
DP/DPE_VSSR#1 DP/DPE_VSSR#2 DP/DPE_VSSR#3 DP/DPE_VSSR#4
DPCD_VDD18/DPC_PVDD DP_VSSR/DPC_PVSS
AU18 AV17
20mA
10mil
+DPABCD_VDD18

DPCD_VDD18/DPD_PVDD DP_VSSR/DPD_PVSS
AV19 AR18
20mA
10mil
+DPABCD_VDD18

SM01000BL00
1000ma 470ohm@100mhz DCR 0.2
L27
MBK1608221YZF_2P
+1.0VSG
FootPrint
C481 10U_0603_6.3V6M
C482 1U_0402_6.3V6K
C483 0.1U_0402_16V4Z

DP mode:220mA
LVDS mode:240mA
20mil
+DPEF_VDD18
AF34 AG34
DPEF/DPF_VDD18#1 DPEF/DPF_VDD18#2
DPEF_VDD18/DPE_PVDD DP_VSSR/DPE_PVSS
AM37 AN38
20mA
10mil
+DPEF_VDD18

20mil
+DPEF_VDD10
AK33 AK34
DPEF/DPF_VDD10#1 DPEF/DPF_VDD10#2
DPEF_VDD18/DPF_PVDD DP_VSSR/DPF_PVSS
AL38 AM35
20mA
10mil
+DPEF_VDD18

AF39 AH39 AK39 AL34 AM34
DP/DPF_VSSR#1 DP/DPF_VSSR#2 DP/DPF_VSSR#3 DP/DPF_VSSR#4 DP/DPF_VSSR#5

R470 150_0402_1%
AM39
DPEF_CALR

2160809000A11SEYMOU_FCBGA962

Park/Madison :AL21left NC

Seymour/Whistler:
AL21:PX_EN
use to control discreate GPU regulators
for power express BACO mode
Support BACO:
output High3.3V:turn off regulators (BACO mode on)
output Low0V:turn on regulators (BACO mode off)
need PD resistor
No support BACO:
left NC

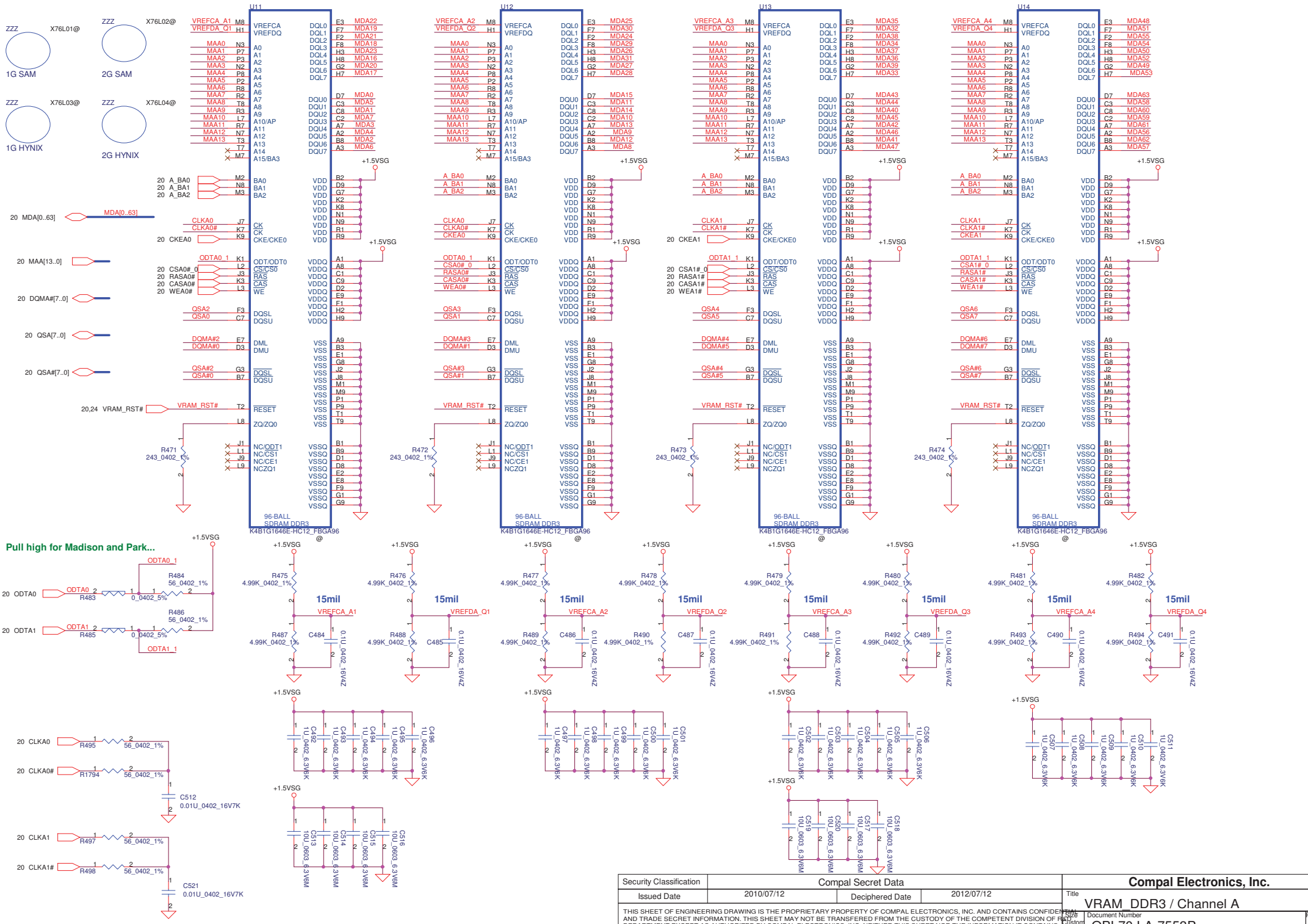
Security Classification	Compal Secret Data		
Issued Date	2010/07/12	Deciphered Date	2012/07/12

Compal Electronics, Inc.

Title: Vancouver_Power/GND

Size: Custom | Document Number: QBL70 LA-7553P | Rev: 0.22

Date: Friday, April 29, 2011 | Sheet 22 of 51



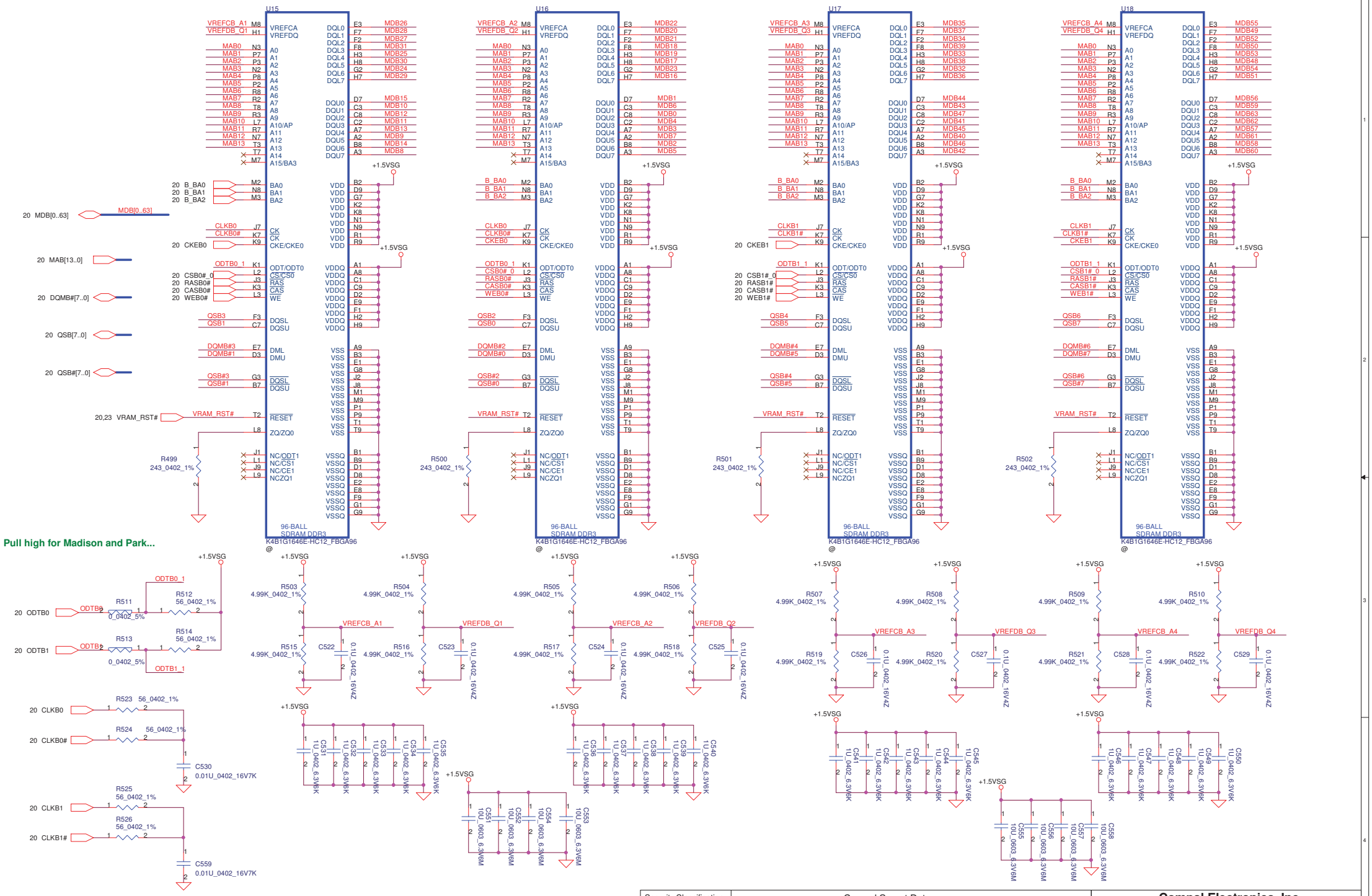
Security Classification	Compal Secret Data		
Issued Date	2010/07/12	Deciphered Date	2012/07/12

Compal Electronics, Inc.

Title: VRAM_DDR3 / Channel A

Size: Custom | Document Number: QBL70 LA-7553P | Rev: 0.22

Date: Friday, April 29, 2011 | Sheet 23 of 51



Security Classification	Compal Secret Data		
Issued Date	2010/07/12	Deciphered Date	2012/07/12

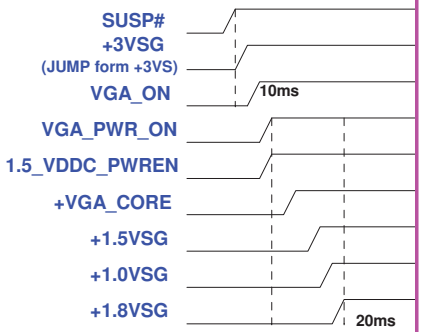
Compal Electronics, Inc.

Title: VRAM_DDR3 / Channel B

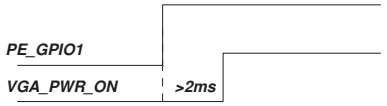
Size: Custom | Document Number: QBL70 LA-7553P | Rev: 0.22

Date: Friday, April 29, 2011 | Sheet 24 of 51

Power Sequence of Whistler and Seymour

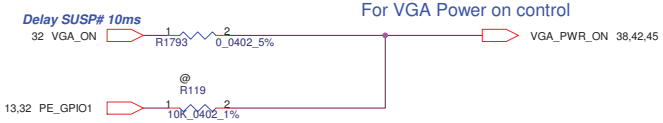


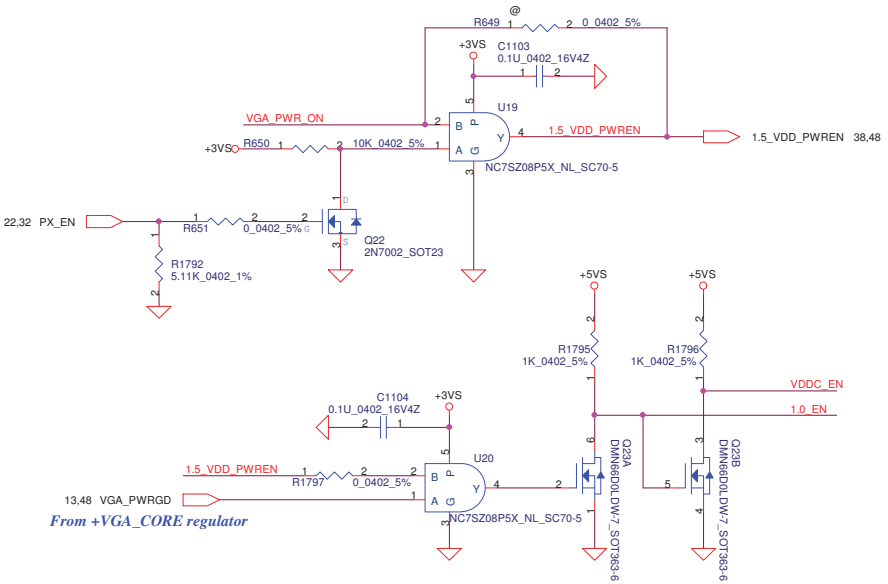
For PX sequence, >2mS delay is required between PE_GPIO1 and VGA_PWR_ON

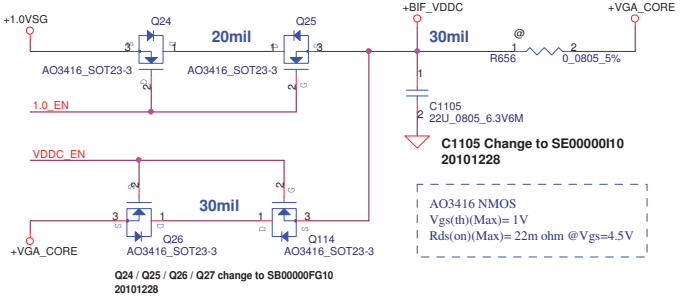


VGA Muxless with BACO Status Mapping table		
	Normal mode	BACO mode
PX_EN	0	1
1.5_VDDC_PWREN	1	0
VDDC_EN	1	0
1.0_EN	0	1
+3.3VSG	ON	ON
+1.8VSG	ON	ON
+1.0VSG	ON	ON
+VGA_CORE	ON	OFF
+1.5VSG	ON	OFF
+BIF_VDDC	+VGA_CORE	+1.0VSG

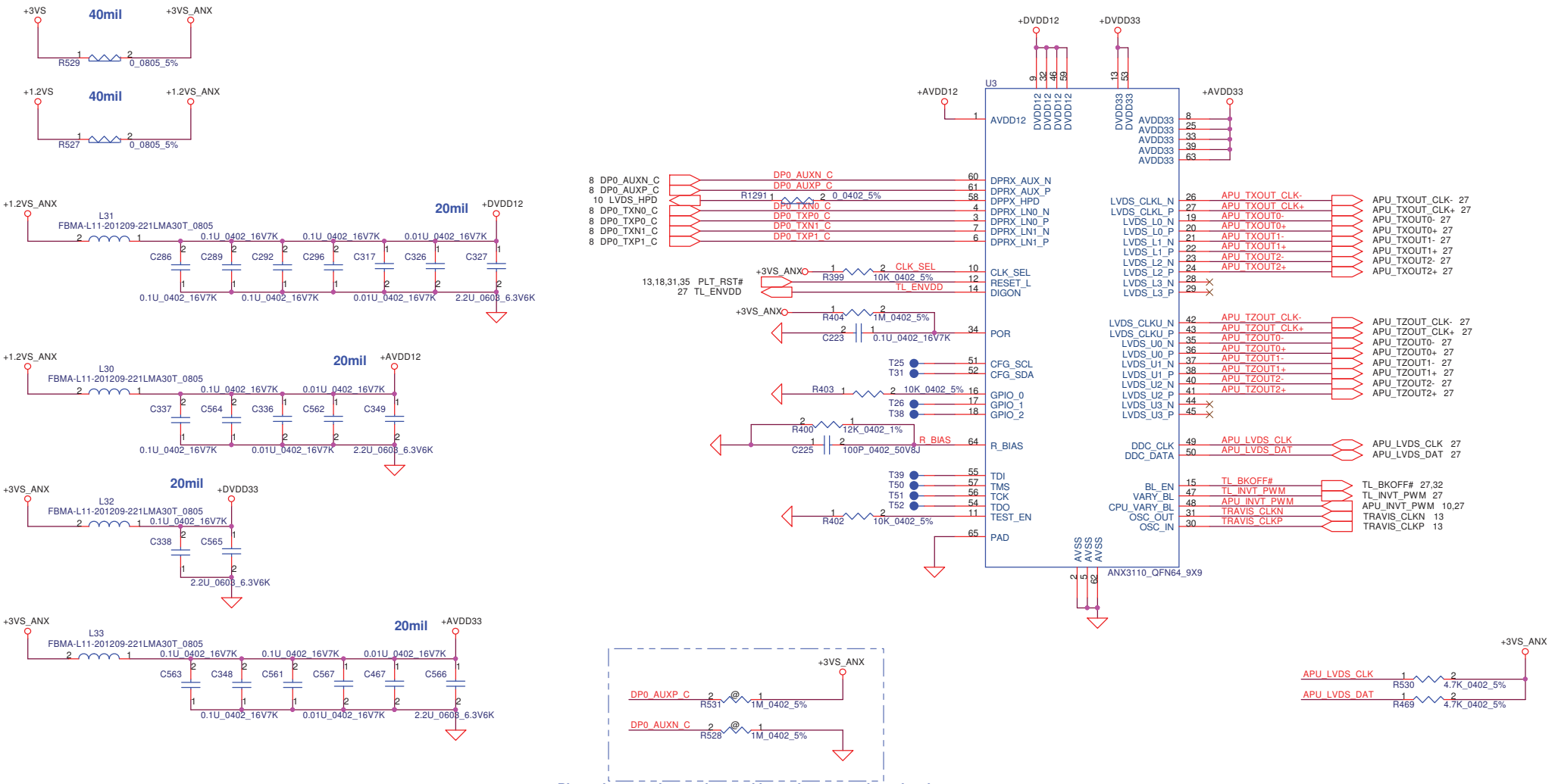
VGA Power Enable Signal Mapping table	
	Whislter
VGA_PWR_ON source signal	VGA_ON
+3.3VSG	SUSP#
+1.8VSG	VGA_PWR_ON
+1.0VSG	VGA_PWR_ON
+VDDCI	Combine with +VGA_CORE
+VGA_CORE	1.5_VDDC_PWREN
+1.5VSG	1.5_VDDC_PWREN







Security Classification	Compal Secret Data		Compal Electronics, Inc.
Issued Date	2010/08/04	Deciphered Date 2010/08/04	Title: VGA power sequence and BACO
Size: Custom	Document Number: QBL70 LA-7553P		Rev: 0.22
Date: Friday, April 29, 2011	Sheet 25 of 51		



Place via on each trace bus and let resistor very close the via

Security Classification	Compal Secret Data		
Issued Date	2010/11/11	Deciphered Date	2011/11/11

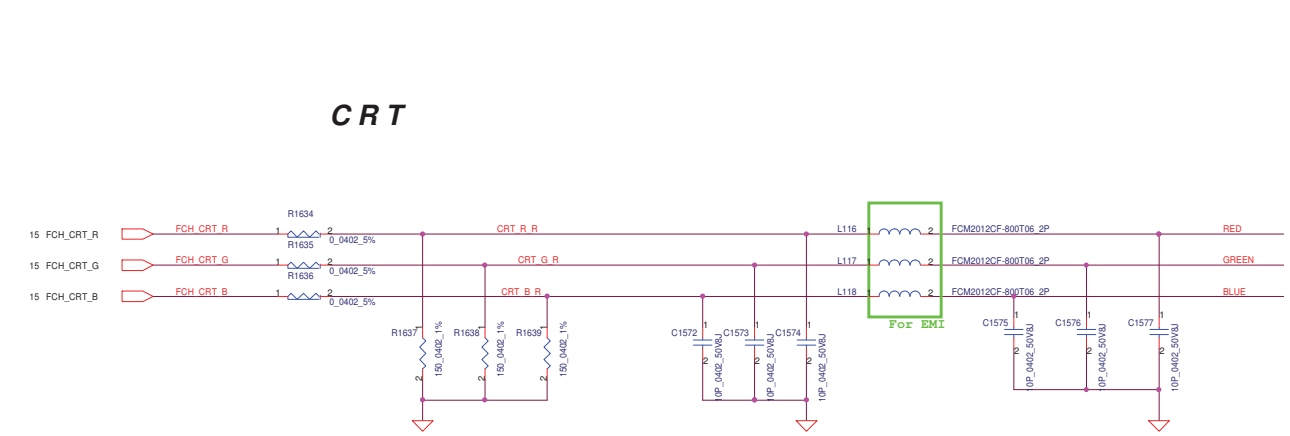
Compal Electronics, Inc.

Title: ***LVDS Translator-ANX3110***

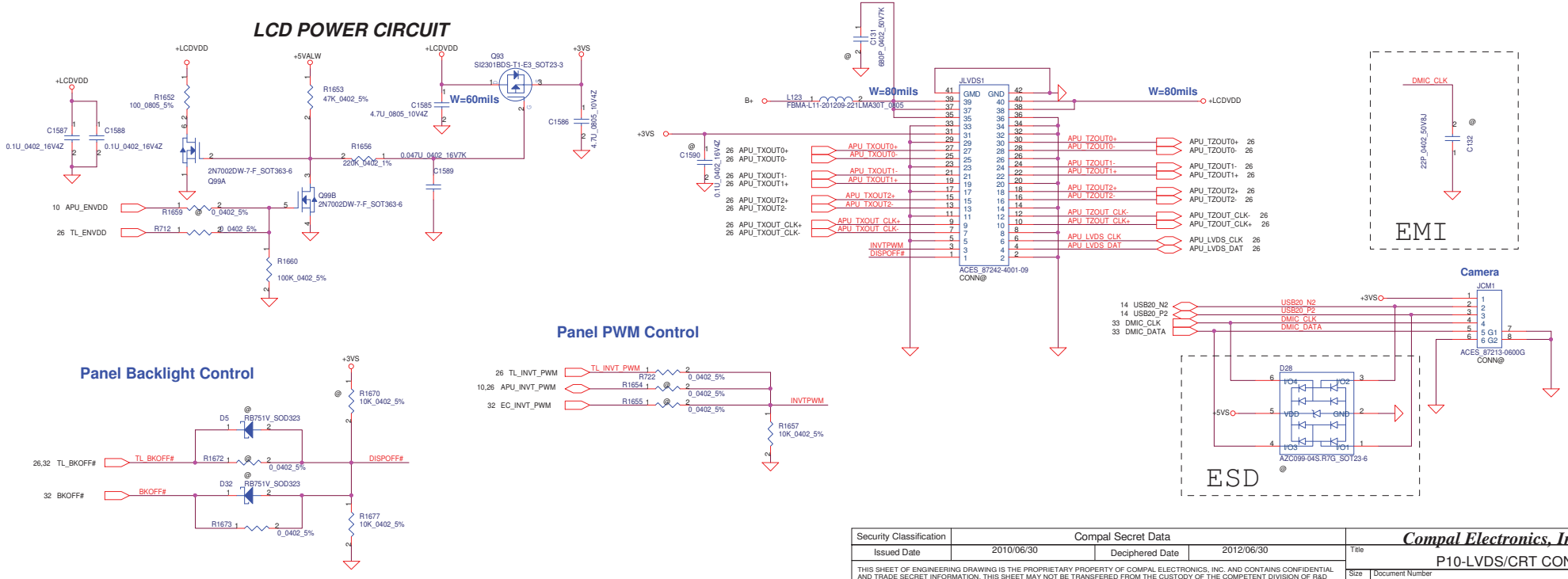
Size: Custom | Document Number: **PEQAE LA-7291P M/B** | Rev: 0.22

Date: Friday, April 29, 2011 | Sheet 26 of 51

CRT



LCD POWER CIRCUIT



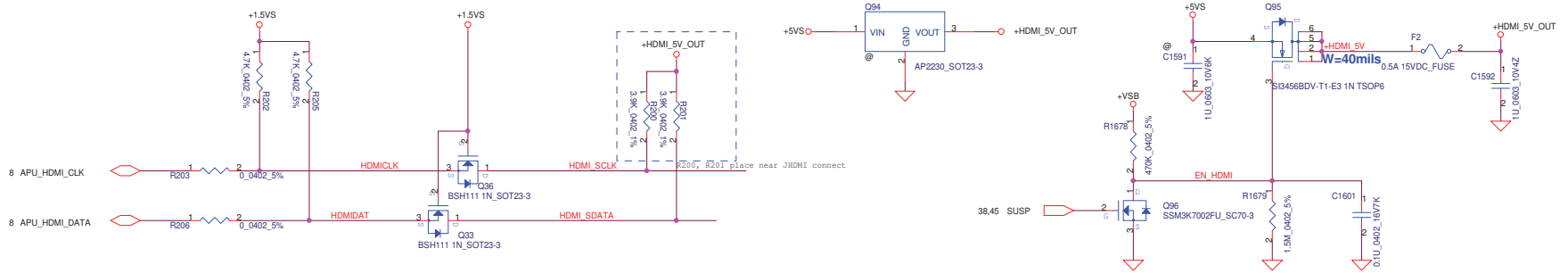
Security Classification	Compal Secret Data		
Issued Date	2010/06/30	Deciphered Date	2012/06/30

Compal Electronics, Inc.

Title: P10-LVDS/CRT CONN

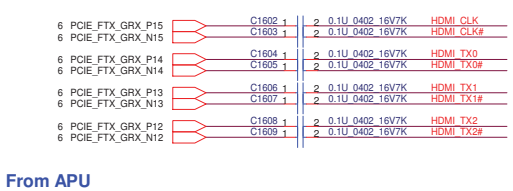
Size	Document Number	Rev
C	QBL70 LA-7553P	0.22

Date: Friday, April 29, 2011 Sheet 27 of 51

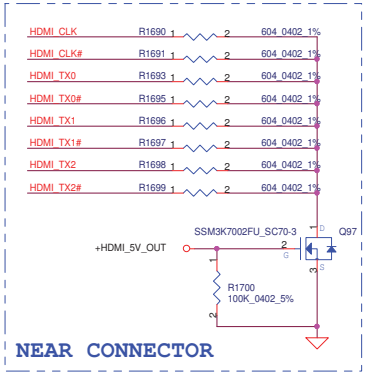


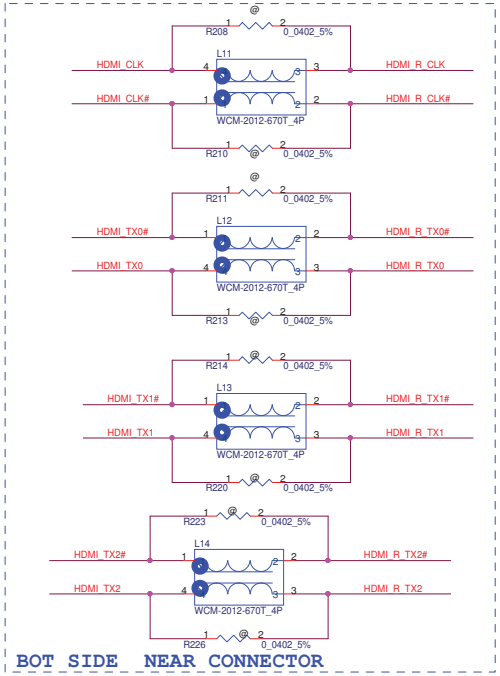
5V PULL UP IN CONNECTOR SIDE

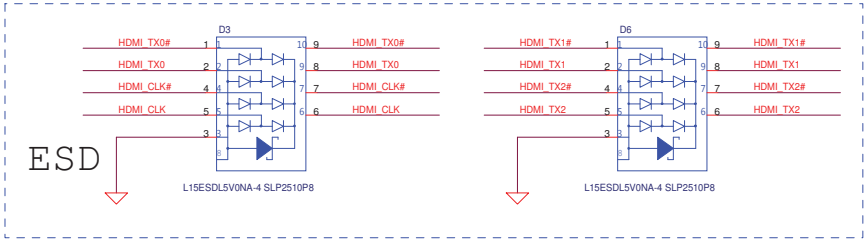
Near the connector

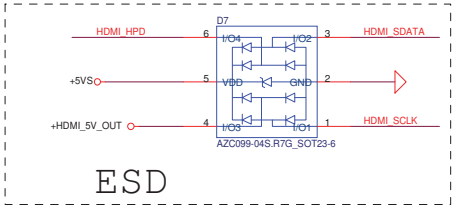


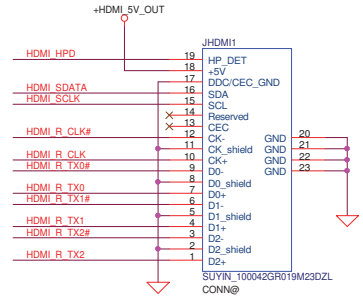
From APU

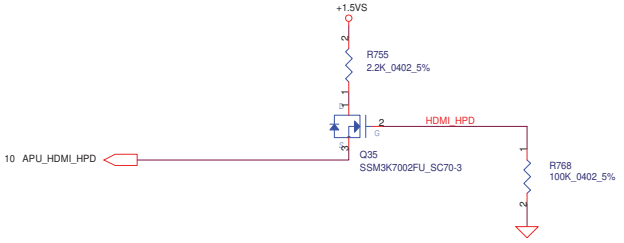












Security Classification	Compal Secret Data		
Issued Date	2010/06/30	Deciphered Date	2012/06/30

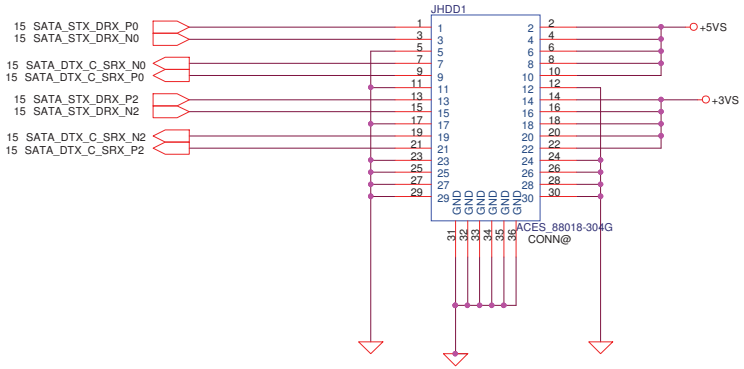
Compal Electronics, Inc.

Title: P11-HDMI CONN

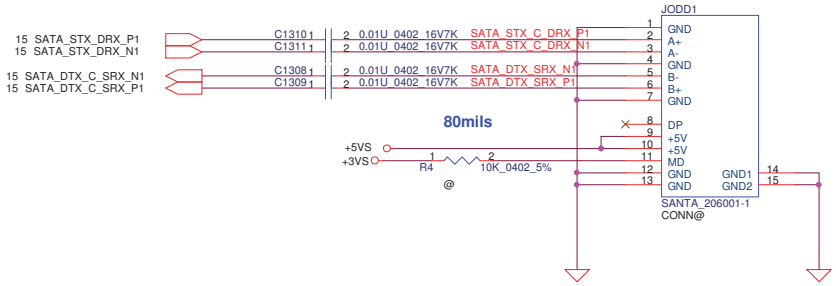
Size: Custom | Document Number: QBL70 LA-7553P | Rev: 0.22

Date: Friday, April 29, 2011 | Sheet 28 of 51

SATA HDD BTB Conn.



SATA ODD FFC Conn.

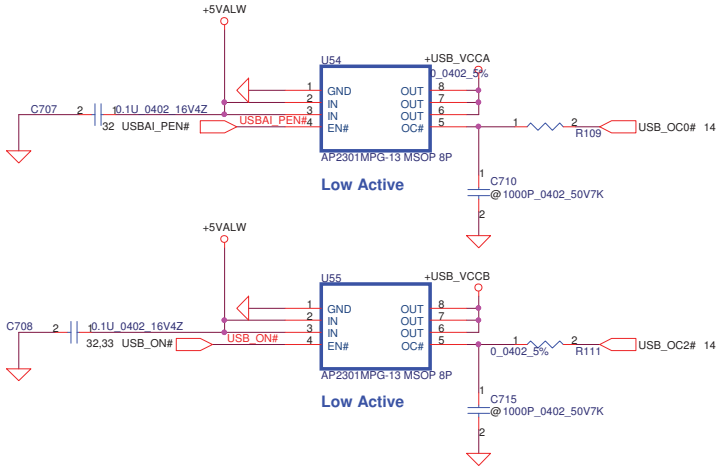


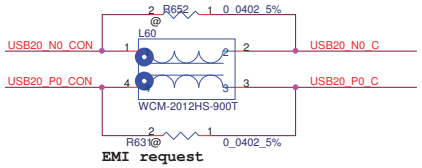
Security Classification	Compal Secret Data		
Issued Date	2010/08/20	Deciphered Date	2012/06/30

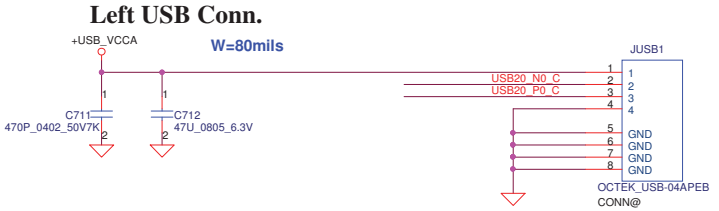
Compal Electronics, Inc.

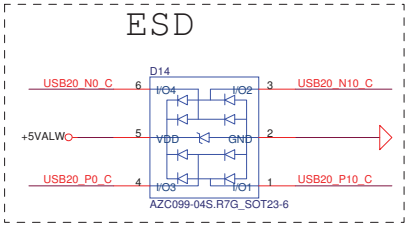
Title: P28-HDD & ODD CONN

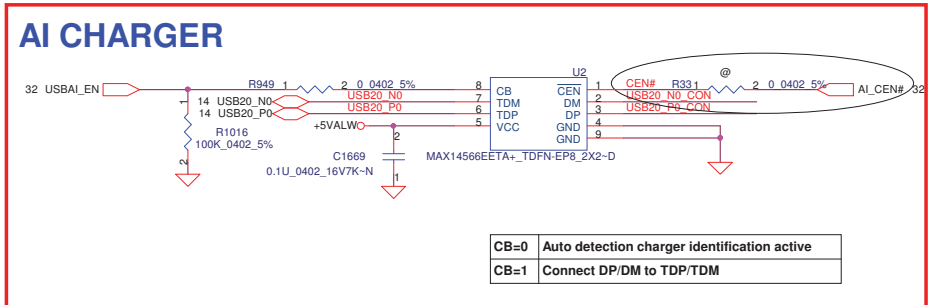
Size: B	Document Number: QBL70 LA-7553P	Rev: 0.22
Date: Friday, April 29, 2011	Sheet 29 of 51	



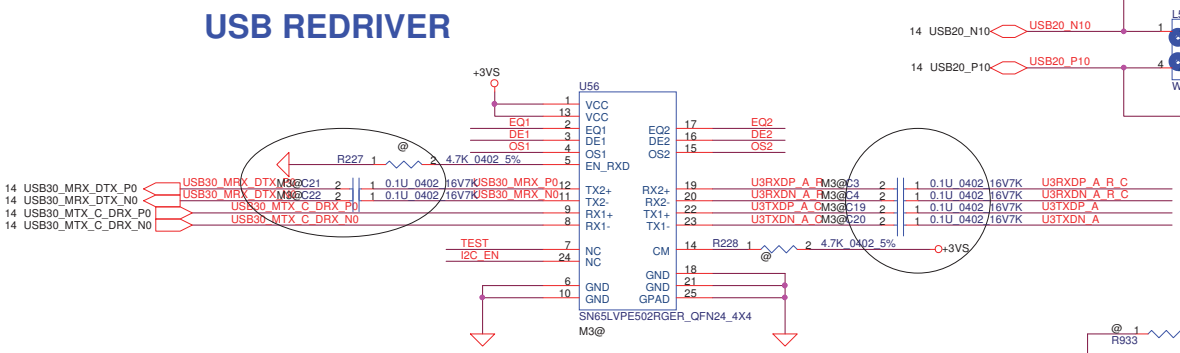


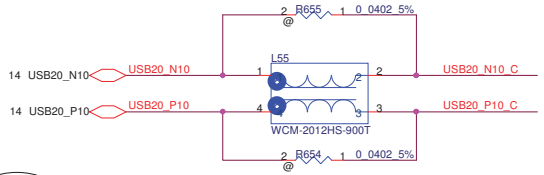


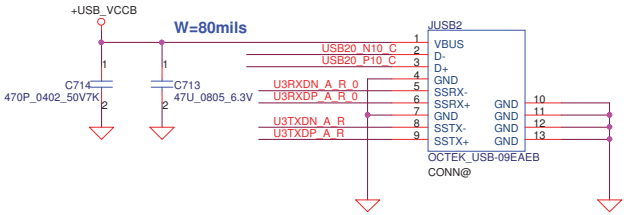


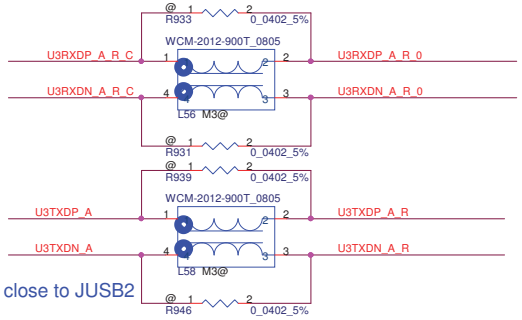


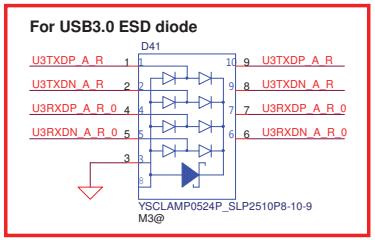
CB=0	Auto detection charger identification active
CB=1	Connect DP/DM to TDP/TDM

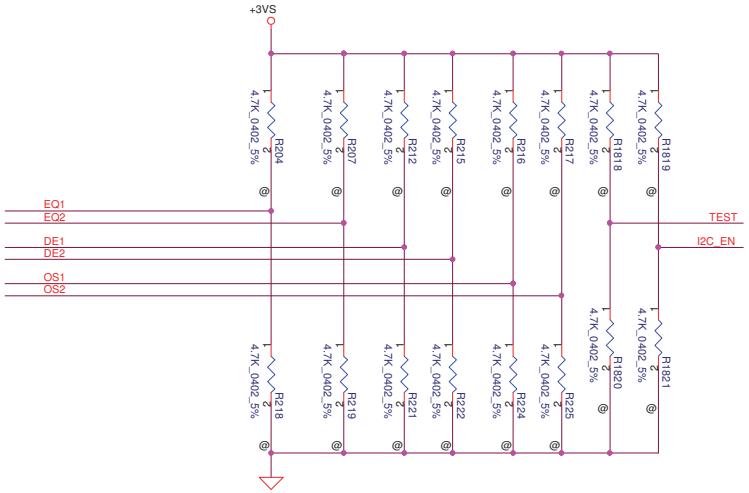












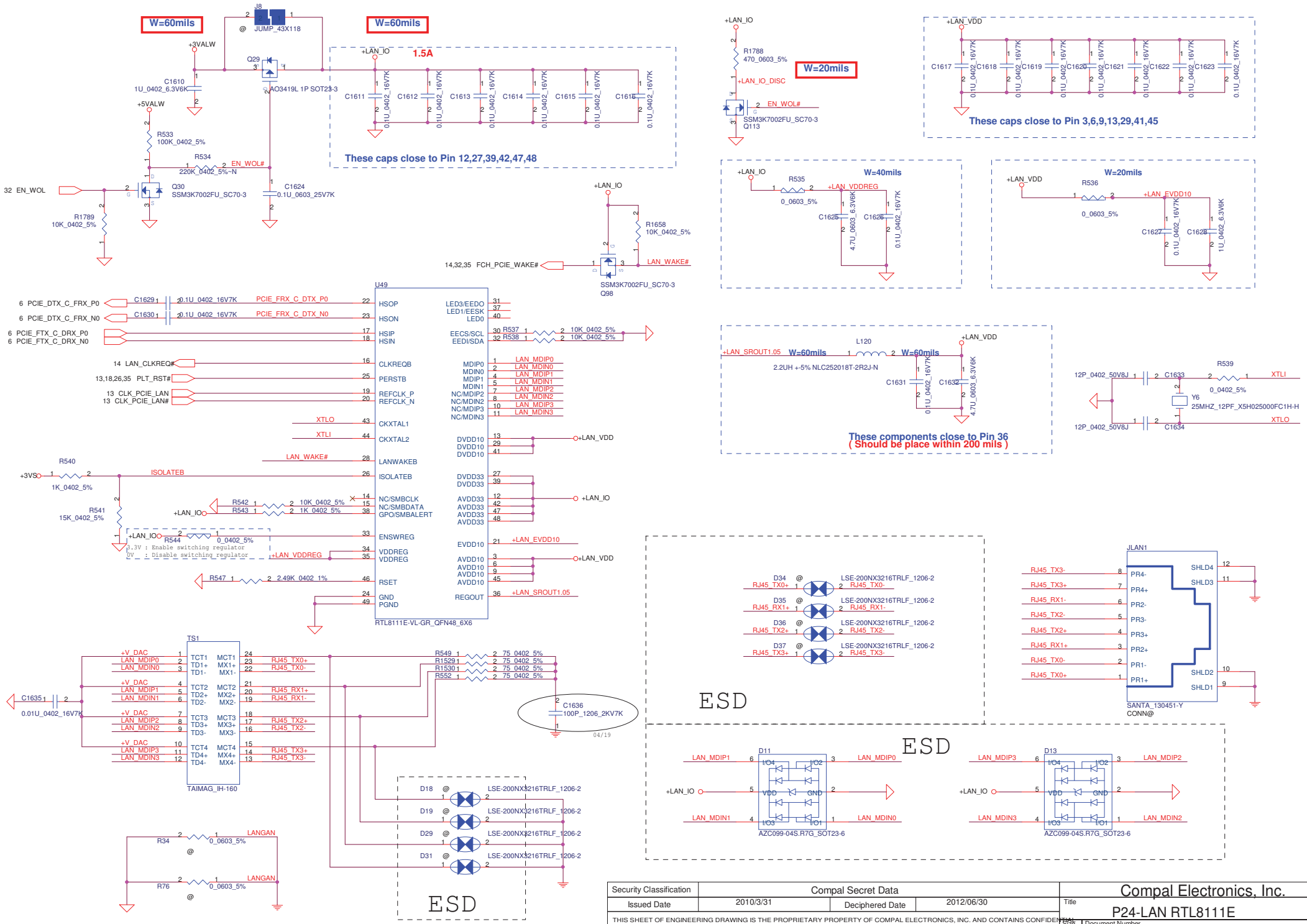
Security Classification	Compal Secret Data		
Issued Date	2010/08/20	Deciphered Date	2012/06/30

Compal Electronics, Inc.

Title: P31-USB/BT/USBsub

Size: Custom | Document Number: QBL70 LA-7553P | Rev: 0.22

Date: Friday, April 29, 2011 | Sheet 30 of 51



Security Classification	Compal Secret Data		
Issued Date	2010/3/31	Deciphered Date	2012/06/30

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Compal Electronics, Inc.

Title: P24-LAN RTL8111E

Size: Custom | Document Number: QBL70 LA-7553P | Rev: 0.22

Date: Friday, April 29, 2011 | Sheet 31 of 51

ID	BRD ID	Ra	Rb	Vab
0	R01 SR	100K	115K	1.6613V
1	R02 ER	100K	154K	1.8857V
2	R10 PR	100K	215K	2.1261V

U31

LPC & MISC
PWM Output
AD Input
DA Output
PS2 Interface
Int. K/B Matrix
SPI Device Interface
SPI Flash ROM
GPIO
SM Bus
GPO
GPI

VGA_DBCLK
EC must program to 500KHZ output
Start and stop follow SUP high/Low

Delay EC_PWROK 50ms
for VGA criterial

20mils

EMI

KB930QF A1 LQFP 128P
20mil

32.768KHZ_12.5PF_Q13MC14610002

MX25L1606EM2I-12G SOP 8P
SA000041N00

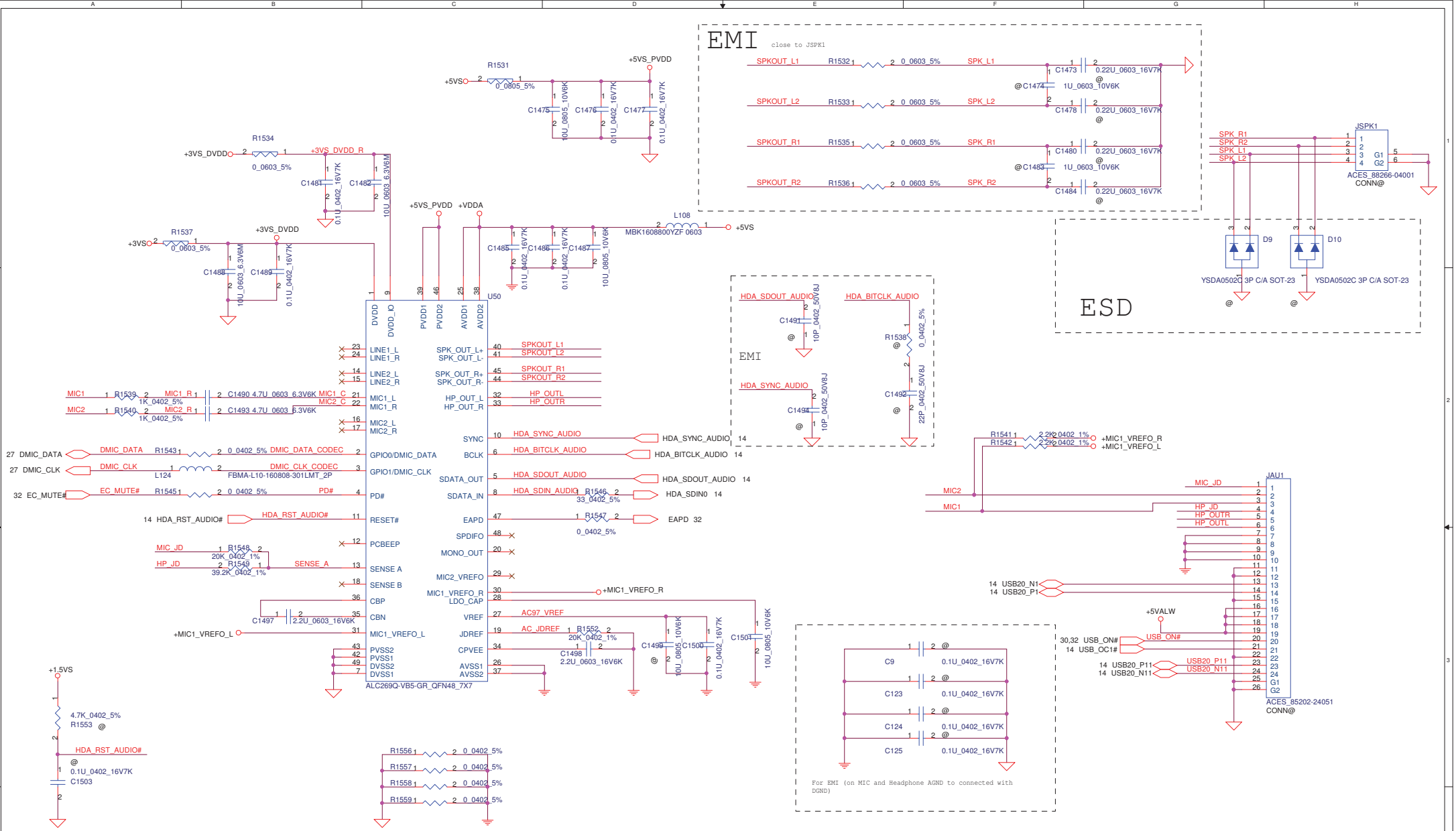
Security Classification	Compal Secret Data		
Issued Date	2010/08/04	Deciphered Date	2010/08/04

Compal Electronics, Inc.

Title: EC ENE KB930

Size: B | Document Number: QBL70 LA-7553P | Rev: 0.22

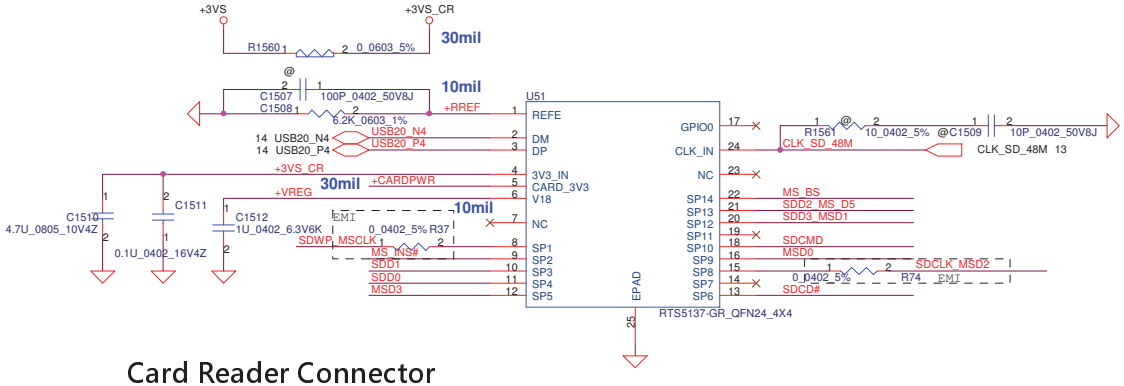
Date: Friday, April 29, 2011 | Sheet 32 of 51



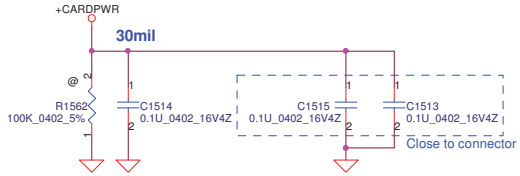
Security Classification	Compal Secret Data		Compal Electronics, Inc.
Issued Date	2010/3/31	Deciphered Date 2012/06/30	Title P25-HD CODEC ALC259

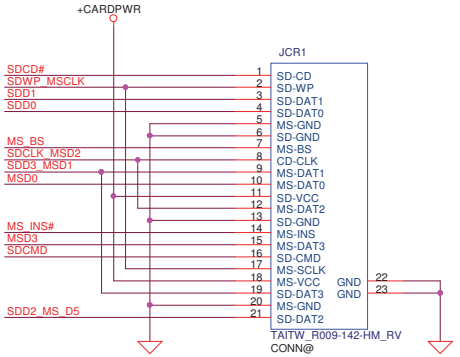
Size Custom	Document Number QBL70 LA-7553P		Rev 0.22
Date: Friday, April 29, 2011		Sheet 33 of 51	

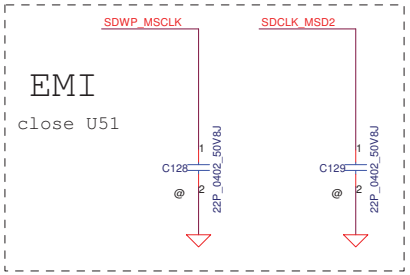
Card Reader RTS5137
(only SD/MMC/MS function)



Card Reader Connector

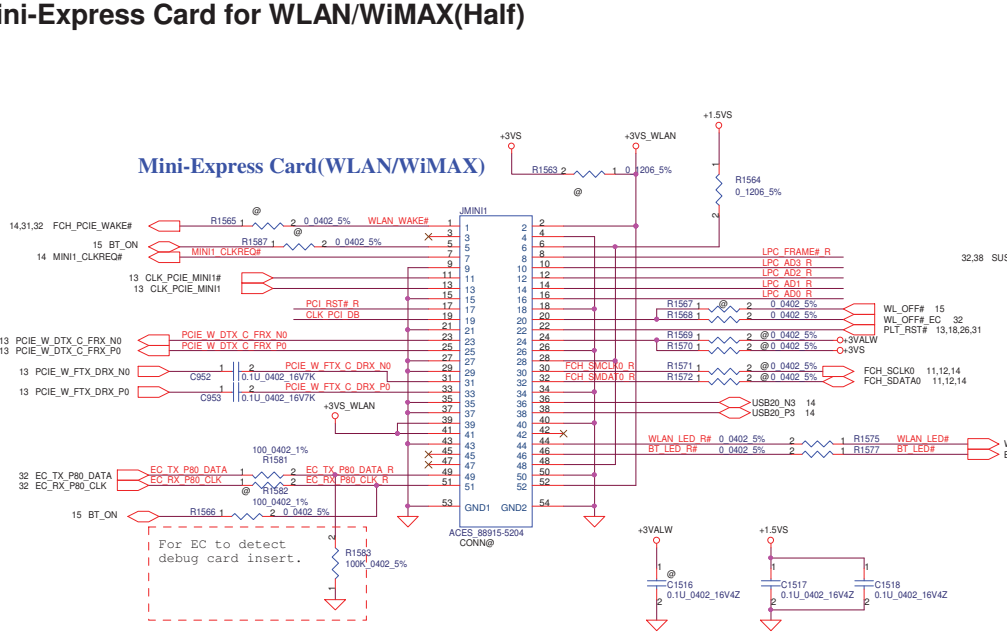


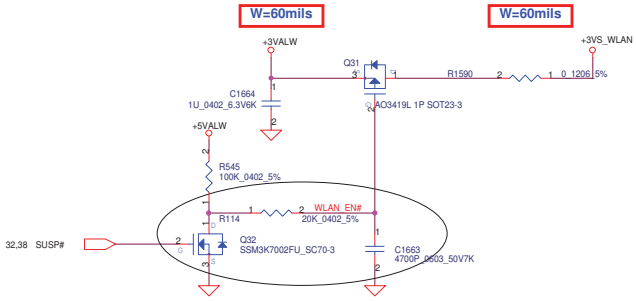




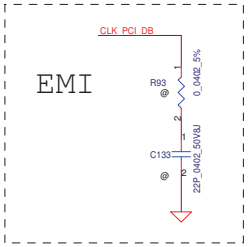
Security Classification	Compal Secret Data		Compal Electronics, Inc.
Issued Date	2009/10/08	Deciphered Date 2012/06/30	Title P26-RTS5137 Media Card Controller
Size Custom	Document Number QBL70 LA-7553P		Rev 0.22
Date: Friday, April 29, 2011	Sheet 34 of 51		

Mini-Express Card for WLAN/WiMAX(Half)

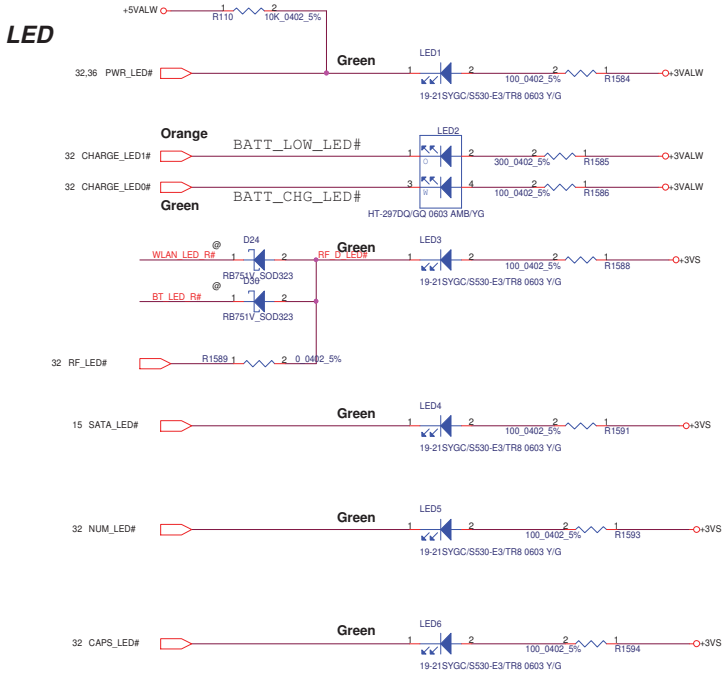


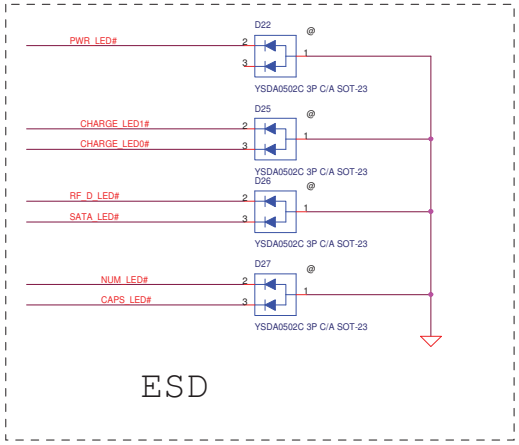


Reserve for SW mini-pcie debug card.
Series resistors closed to KBC side.



LED



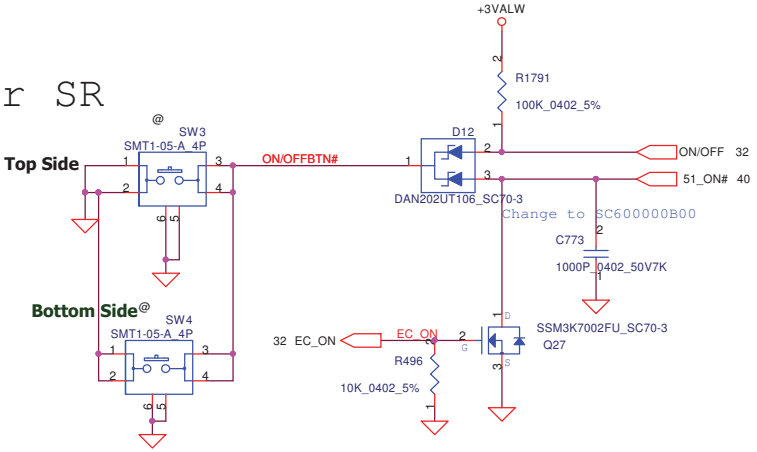


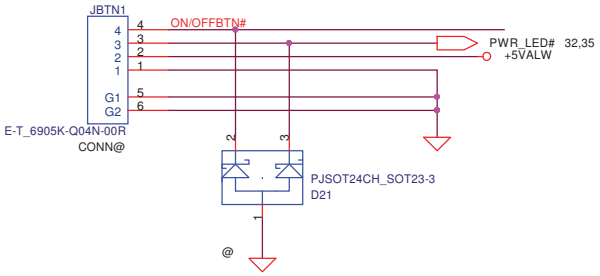
Security Classification	Compal Secret Data		
Issued Date	2010/06/30	Deciphered Date	2012/06/30

Compal Electronics, Inc.
Title: P27-Mini PCIE/LED
Size | Document Number: QBL70 LA-7553P | Rev: 0.22
Date: Friday, April 29, 2011 | Sheet 35 of 51

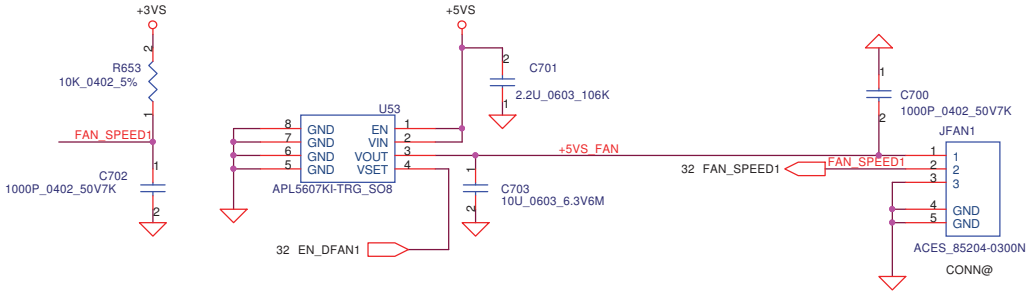
ON/OFF switch **Power Button**

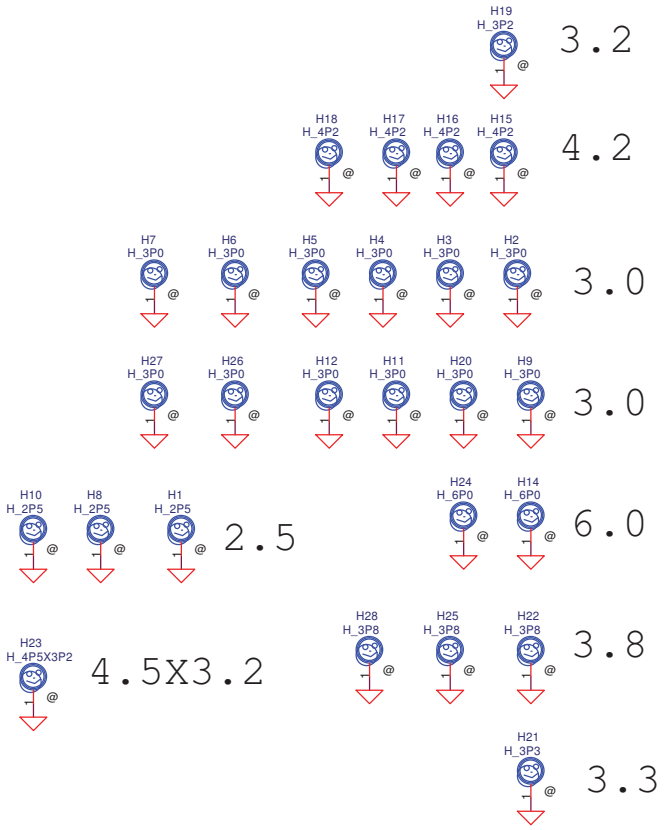
For SR





Fan Control Circuit





Security Classification	Compal Secret Data		
Issued Date	2010/08/20	Deciphered Date	2012/06/30

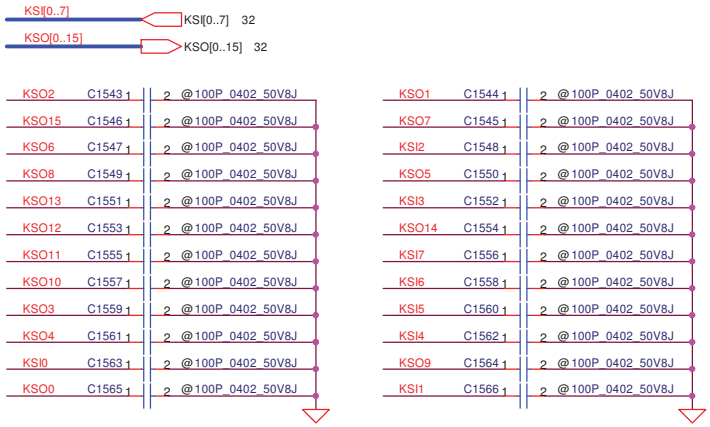
Compal Electronics, Inc.

Title: P33-Other IO/USB (right)

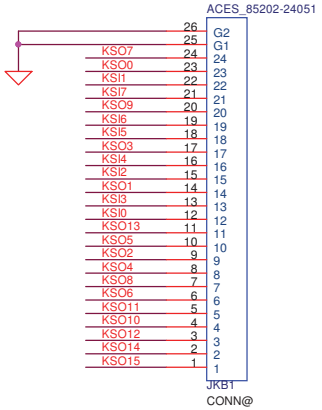
Size: Custom | Document Number: QBL70 LA-7553P | Rev: 0.22

Date: Friday, April 29, 2011 | Sheet 36 of 51

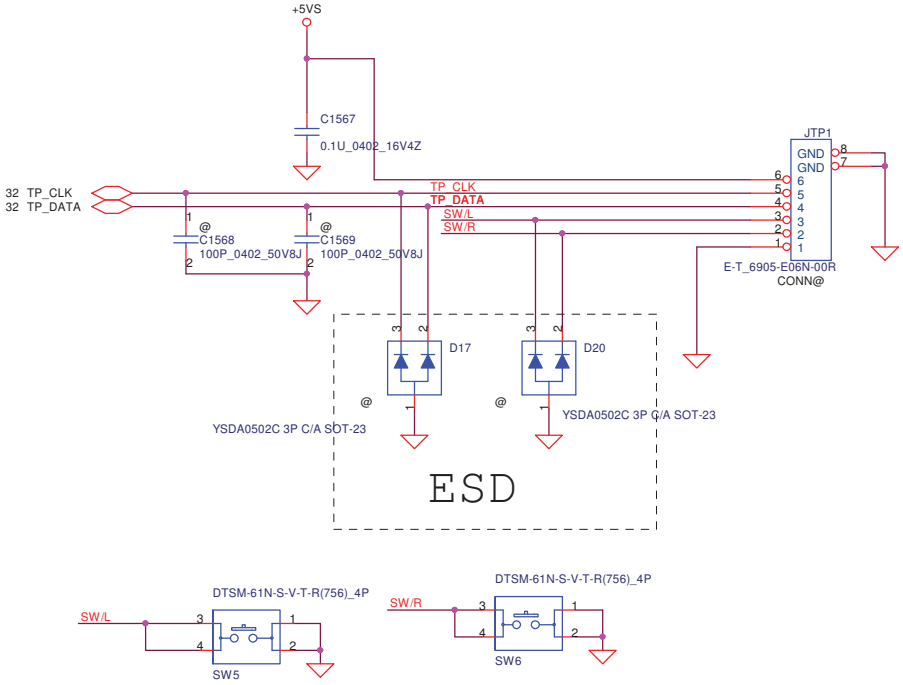
INT_KBD Conn.

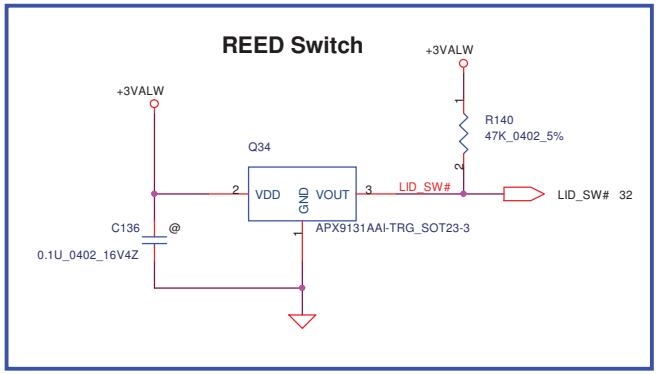


CONN PIN define need double check



To TP/B Conn.





Security Classification	Compal Secret Data		
Issued Date	2010/06/30	Deciphered Date	2012/06/30

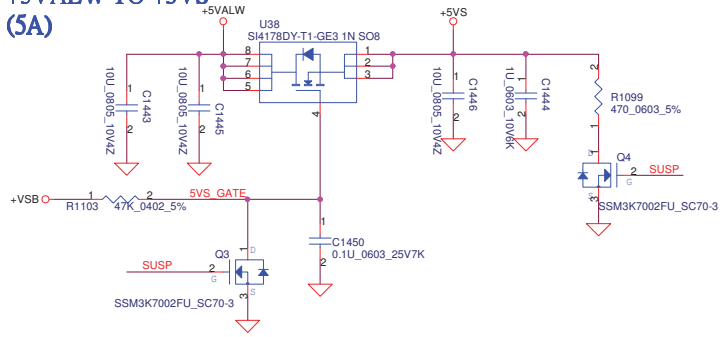
Compal Electronics, Inc.

Title: P30-KB /SW/TP/Lid

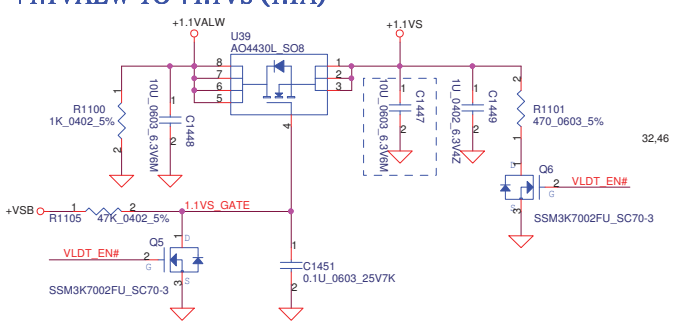
Size: B | Document Number: QBL70 LA-7553P | Rev: 0.22

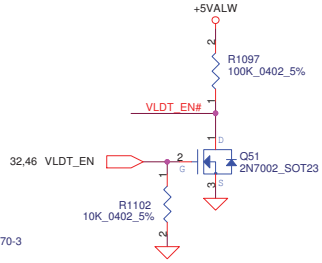
Date: Friday, April 29, 2011 | Sheet 37 of 51

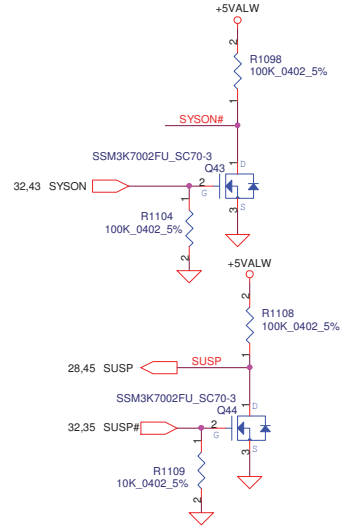
+5VALW TO +5VS (5A)



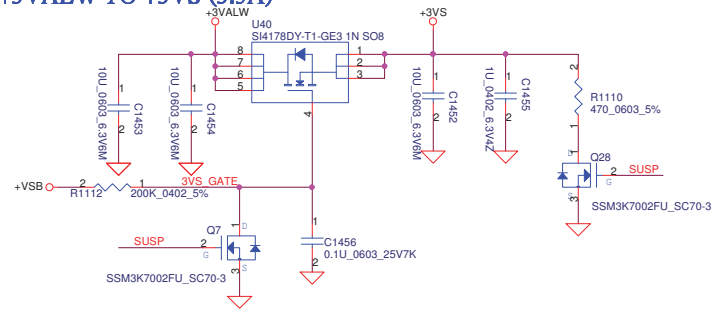
+1.1VALW TO +1.1VS (1.1A)



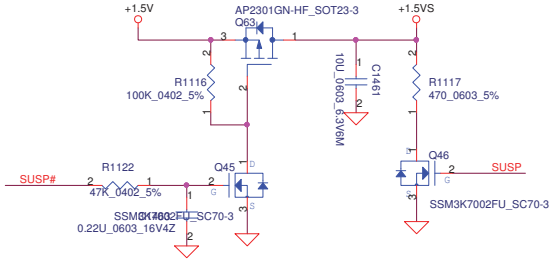




+3VALW TO +3VS (3.3A)

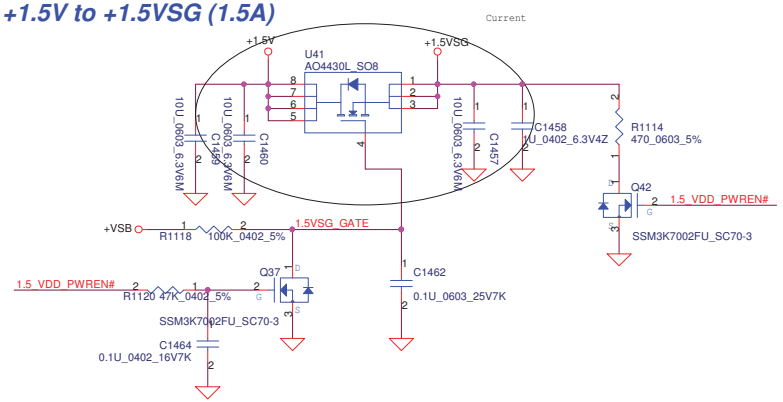


+1.5V TO +1.5VS (1.5A)

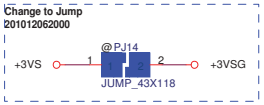


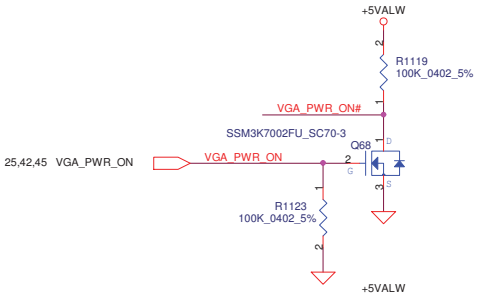
VGA Power

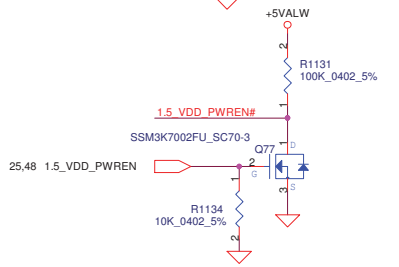
+1.5V to +1.5VSG (1.5A)

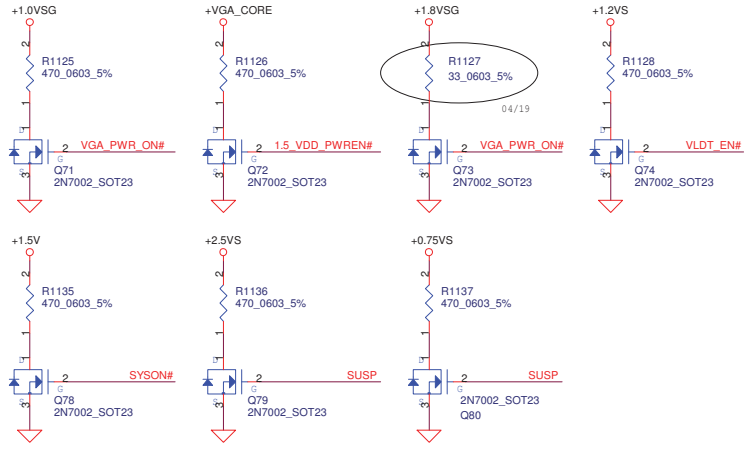


+3VS to +3VSG (3.3A)









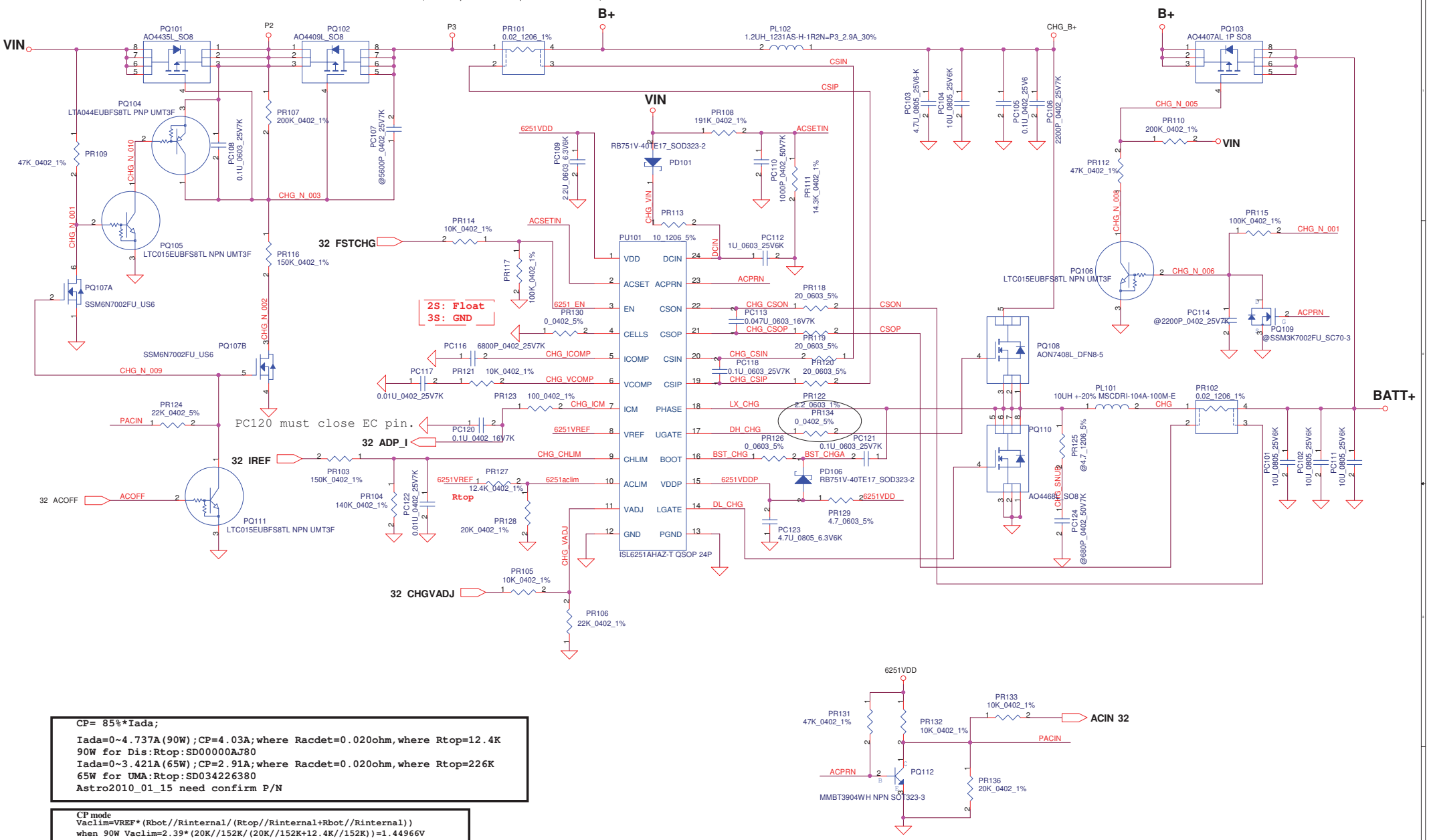
Security Classification	Compal Secret Data		
Issued Date	2010/08/04	Deciphered Date	2010/08/04

Compal Electronics, Inc.

Title: DC Interface

Size: B | Document Number: QBL70 LA-7553P | Rev: 0.22

Date: Friday, April 29, 2011 | Sheet 38 of 51



CP= 85%*Iada;

Iada=0~4.737A(90W);CP=4.03A;where Racdet=0.020ohm,where Rtop=12.4K
90W for Dis:Rtop:SD00000AJ80
Iada=0~3.421A(65W);CP=2.91A;where Racdet=0.020ohm,where Rtop=226K
65W for UMA:Rtop:SD034226380
Astro2010_01_15 need confirm P/N

CP mode
Vaclim=VREF*(Rbot//Rinternal/(Rtop//Rinternal+Rbot//Rinternal))
when 90W Vaclim=2.39*(20K//152K/(20K//152K+12.4K//152K))=1.44966V
when 65W Vaclim=2.39*(20K//152K/(20K//152K+226K//152K))=0.38914V
Iinput=(1/Racdet)*((0.05*Vaclim/VREF+0.05))
when 90W,Iinput=(1/0.02)*(0.05*1.44966/2.39+0.05)=4.02A
when 65W,Iinput=(1/0.02)*(0.05*0.38914/2.39+0.05)=2.92A

CC=0.25A~3A
IREF=1.016*Icharge
IREF=0.254V~3.048V
VCHLIM need over 95mV

CHGVADJ=(Vcell-4)/0.10627

Vcell	CHGVADJ
4V	0V
4.2V	1.882V

Security Classification	Compal Secret Data		
Issued Date	2009/01/23	Deciphered Date	2010/01/23

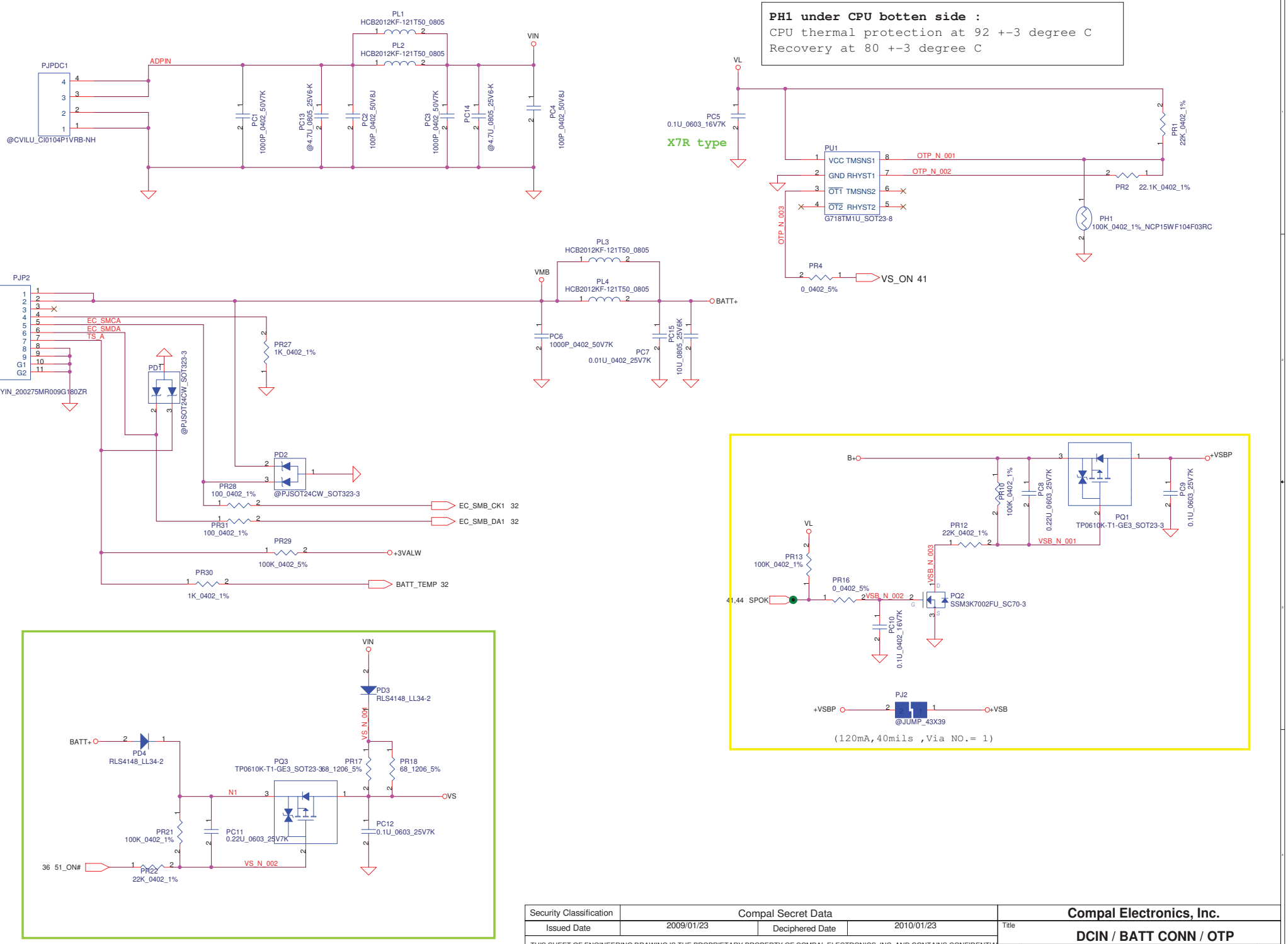
Compal Electronics, Inc.

Title: CHARGER

Size | Document Number: NCL61 LA-6321P M/B | Rev: 0.1

Date: Friday, April 29, 2011 | Sheet 39 of 49

PH1 under CPU botten side :
CPU thermal protection at 92 +-3 degree C
Recovery at 80 +-3 degree C



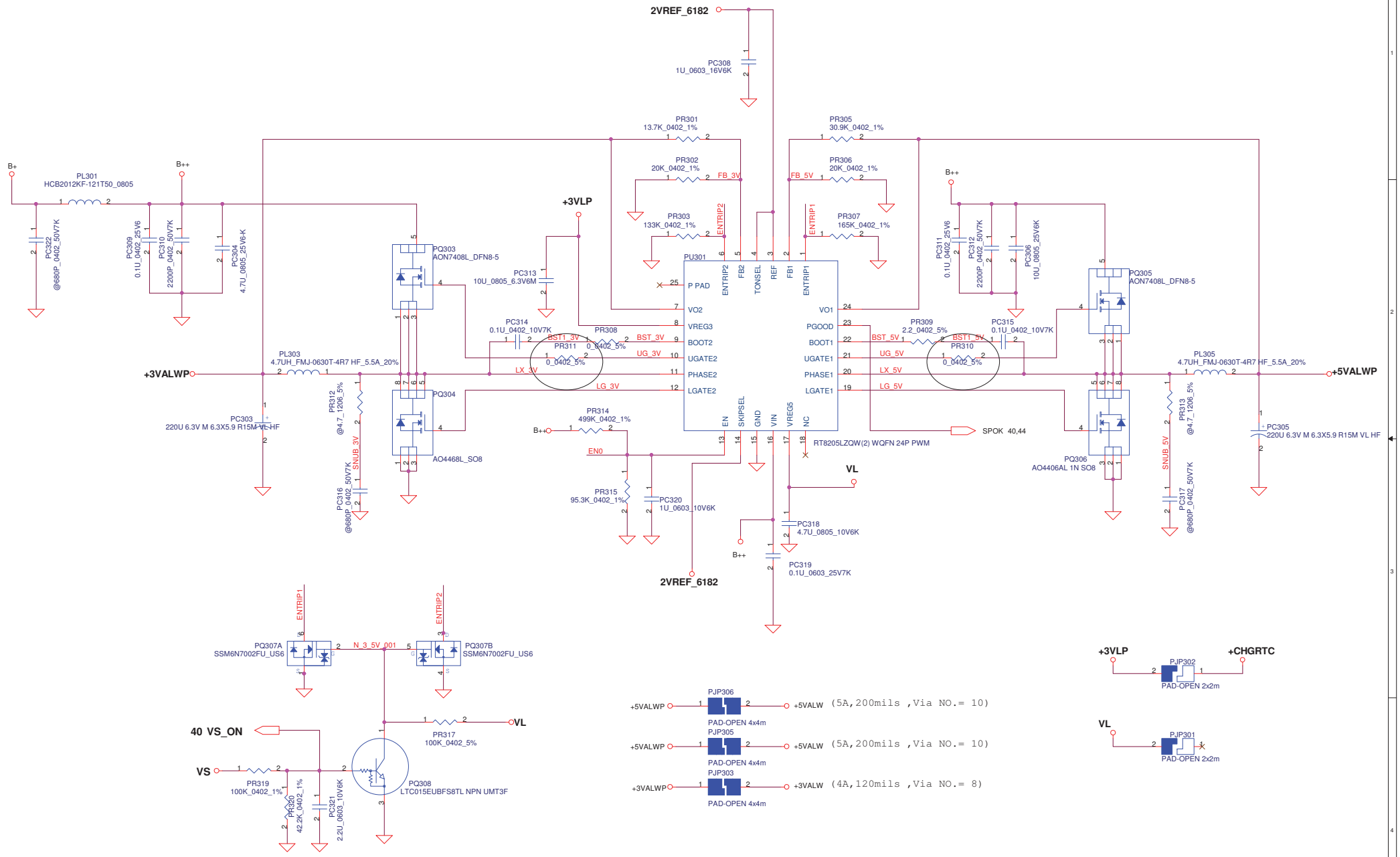
Security Classification	Compal Secret Data		
Issued Date	2009/01/23	Deciphered Date	2010/01/23

Compal Electronics, Inc.

Title: **DCIN / BATT CONN / OTP**

Size	Document Number	Rev
	NCL61 LA-6321P M/B	0.1

Date: Friday, April 29, 2011 Sheet 40 of 49



EC:+3VL, reserve PR319, install PR318, PR320 100K
EC:+3VALW, reserve PR318, install PR319, PR320 42.2K

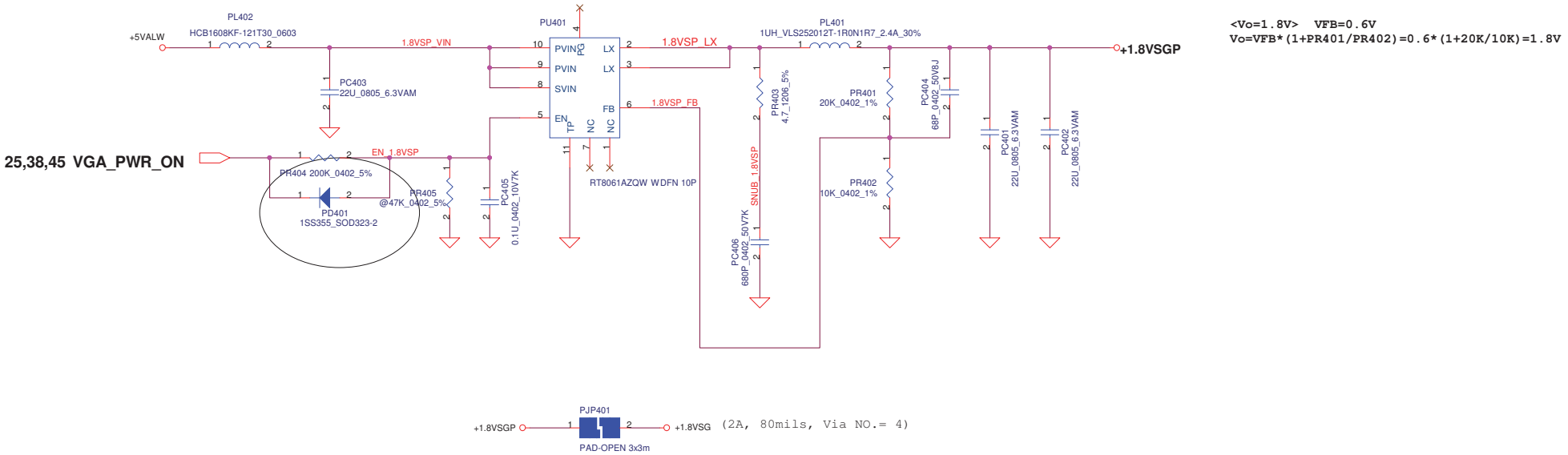
Security Classification	Compal Secret Data		
Issued Date	2007/08/02	Deciphered Date	2008/08/02

Compal Electronics, Inc.

Title: 3.3VALWP/5VALWP

Size: Custom | Document Number: LAXXXX | Rev: 0.1

Date: Friday, April 29, 2011 | Sheet 41 of 49



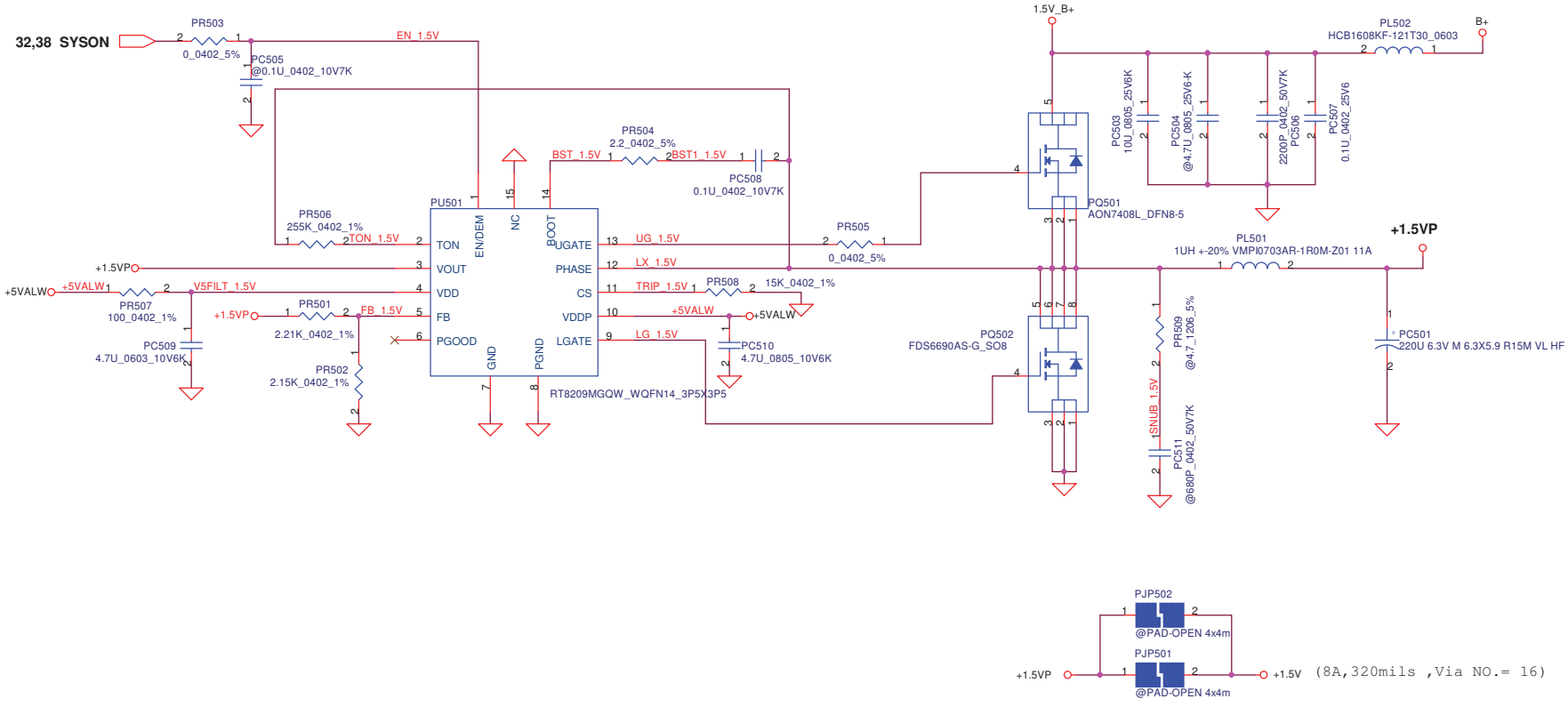
Security Classification	Compal Secret Data		
Issued Date	2009/01/23	Deciphered Date	2010/01/23

Compal Electronics, Inc.

Title: **+1.8VSGP**

Size	Document Number	Rev
	NCL61 LA-6321P M/B	0.1

Date: Friday, April 29, 2011 | Sheet 42 of 49



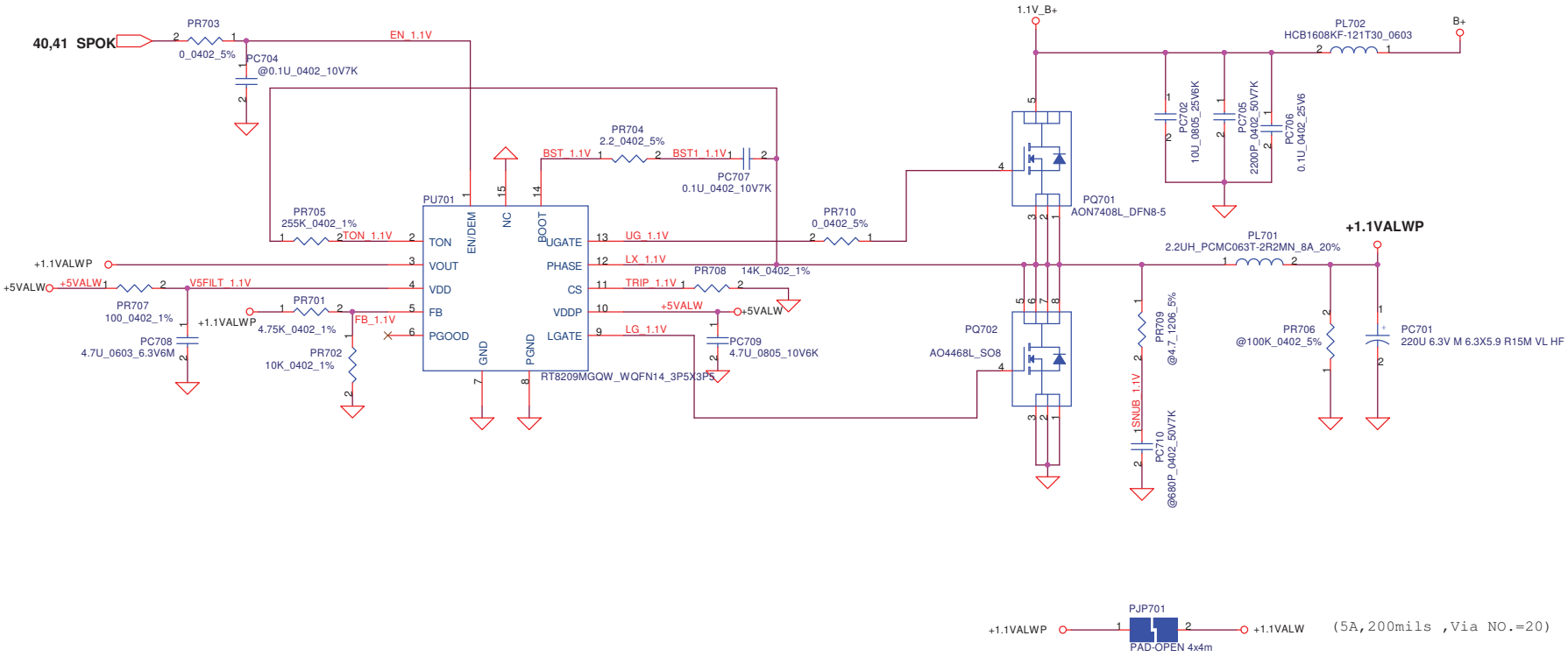
Security Classification	Compal Secret Data		
Issued Date	2007/05/29	Deciphered Date	2008/05/29

Compal Electronics, Inc.

Title: **+1.5VP**

Size	Document Number	Rev
	LAXXXX	0.1

Date: Friday, April 29, 2011 | Sheet 43 of 49



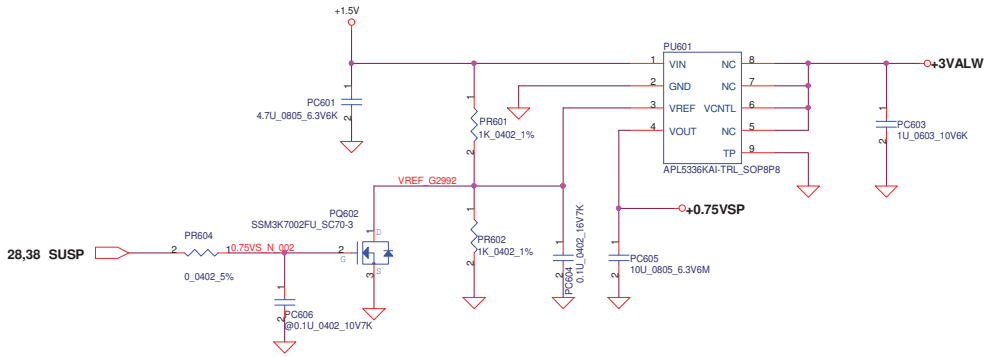
Security Classification	Compal Secret Data		
Issued Date	2009/12/01	Deciphered Date	2010/12/31

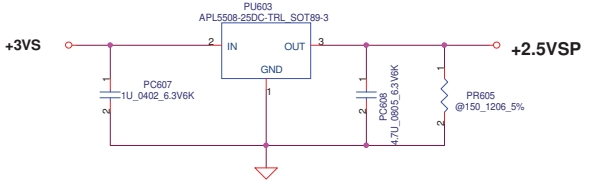
Compal Electronics, Inc.

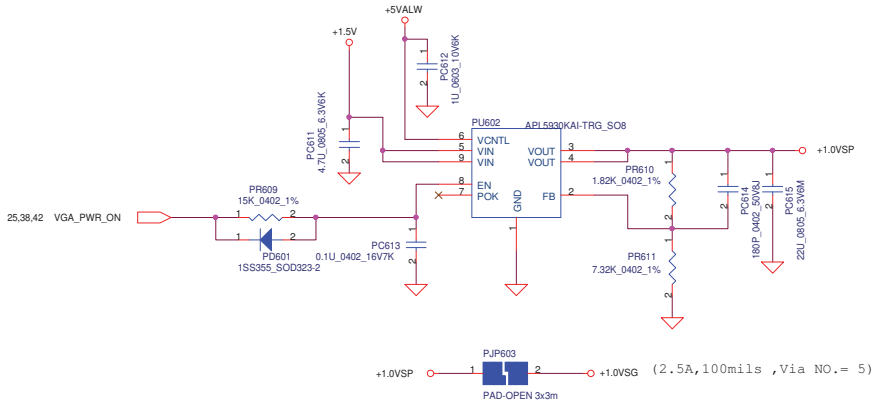
Title: **PWR+1.1VALWP**

Size	Document Number	Rev
Custom	LAXXXX	0.1

Date: Friday, April 29, 2011 | Sheet 44 of 49







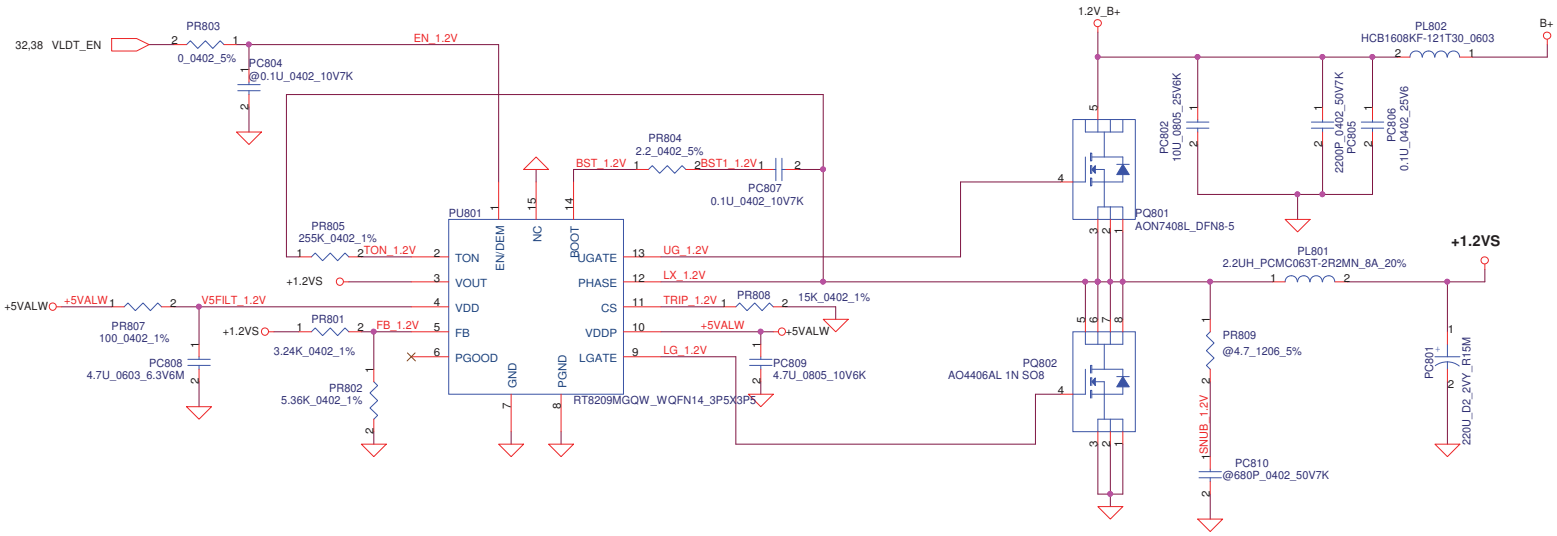
Security Classification	Compal Secret Data		
Issued Date	2006/11/23	Deciphered Date	2007/11/23

Compal Electronics, Inc.

Title: PWR 0.75VSP/1.0VSP/2.5VSP

Size | Document Number: LAXXXX | Rev: 0.1

Date: Friday, April 29, 2011 | Sheet 45 of 49



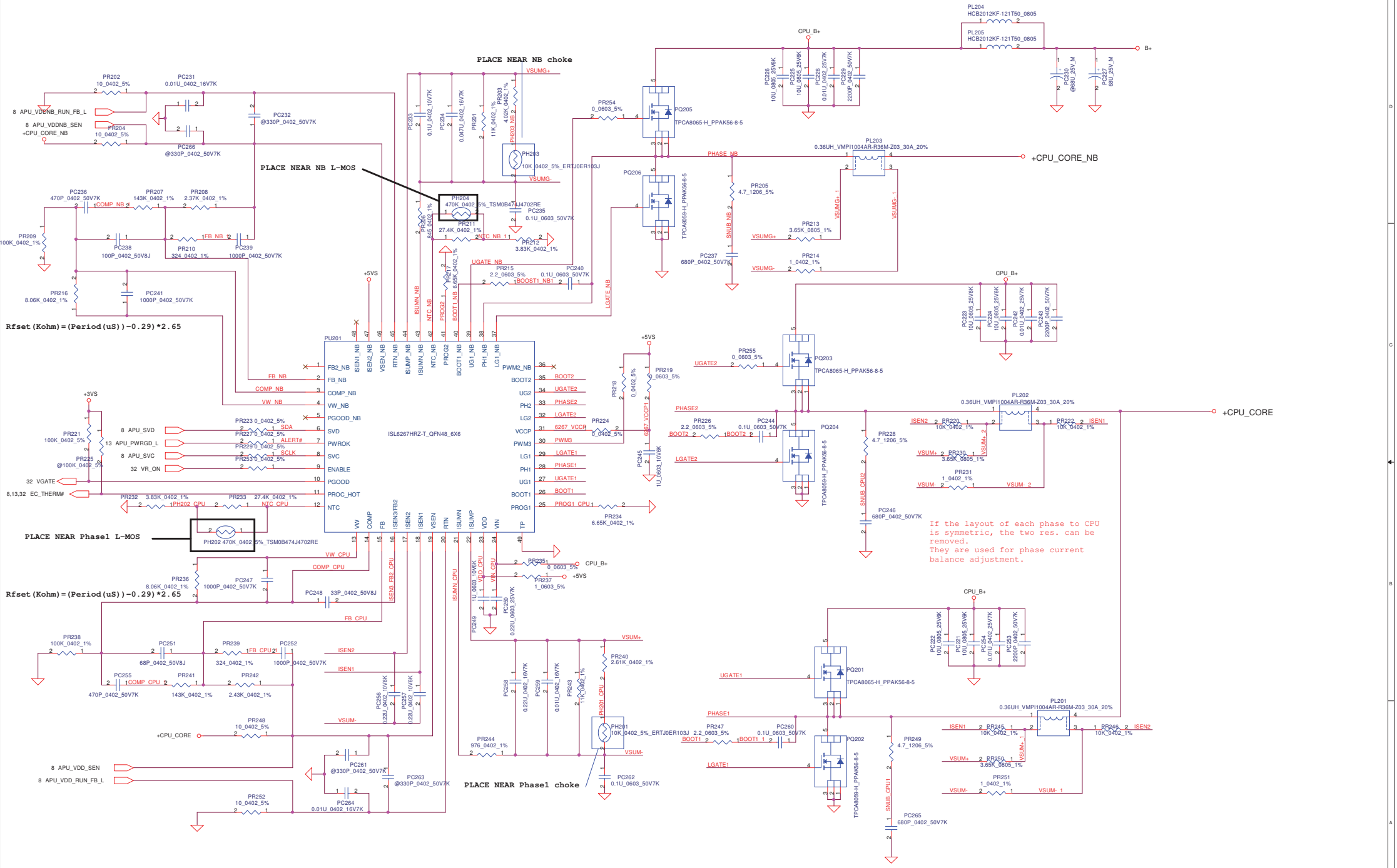
Security Classification	Compal Secret Data		
Issued Date	2009/01/23	Deciphered Date	2010/01/23

Compal Electronics, Inc.

Title: **+1.2VSP**

Size	Document Number	Rev
	NCL61 LA-6321P M/B	0.1

Date: Friday, April 29, 2011 | Sheet 46 of 49



Security Classification	Compal Secret Data		
Issued Date	2010/11/11	Deciphered Date	2011/11/11

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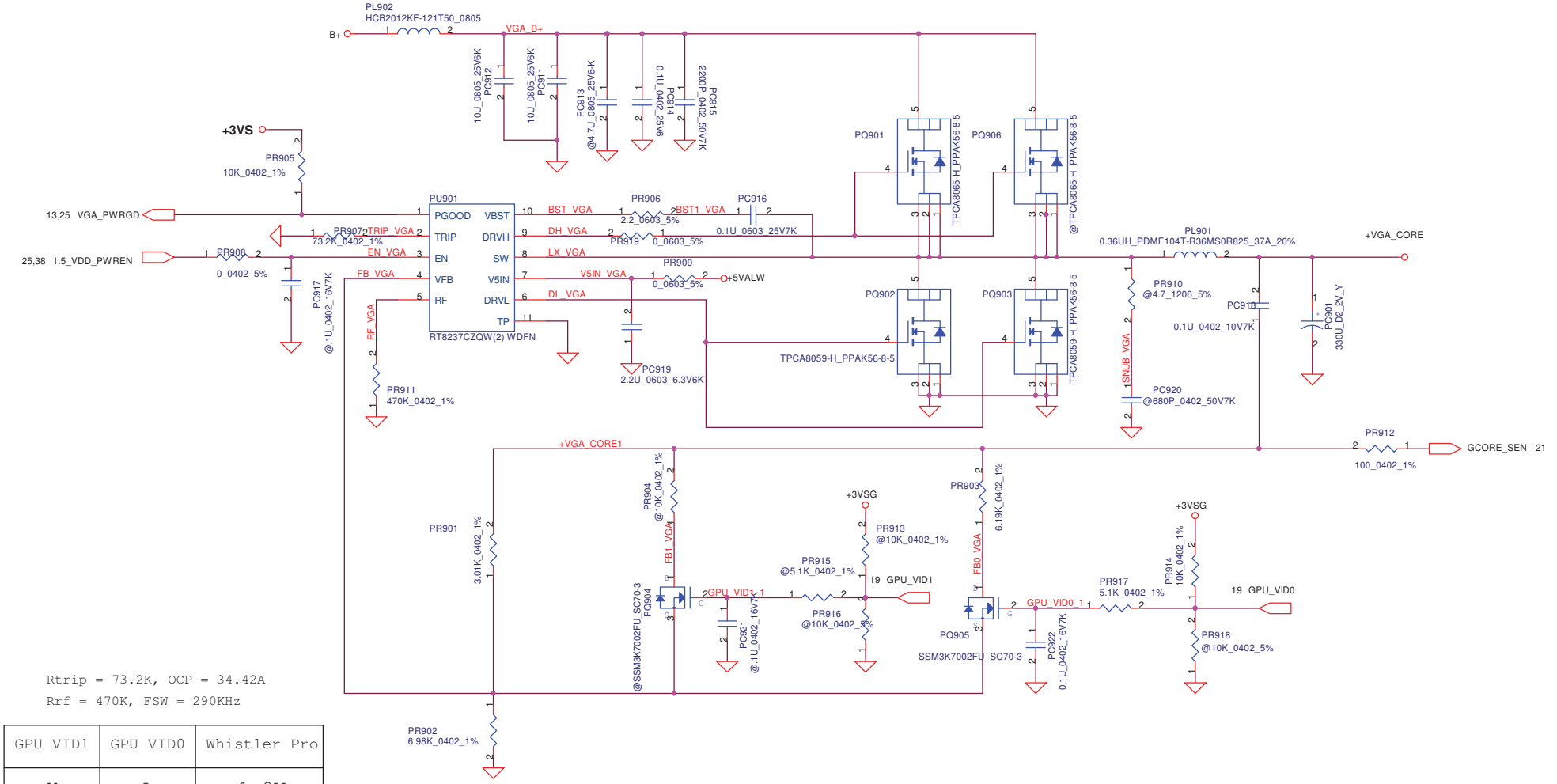
Compal Electronics, Inc.	
Title	PWR_+CPU_CORE/+CPU_CORE_NB
Size	Document Number: PEQAE LA-7291P M/B
Rev	0.1
Date: Friday, April 29, 2011	Sheet 47 of 49



Rtrip = 73.2K, OCP = 34.42A

Rrf = 470K, FSW = 290KHz

GPU VID1	GPU VID0	Whistler Pro
X	L	1.0V
X	H	0.9V
H	L	
H	H	

Security Classification	Compal Secret Data		
Issued Date	2007/05/29	Deciphered Date	200810/11

Compal Electronics, Inc.

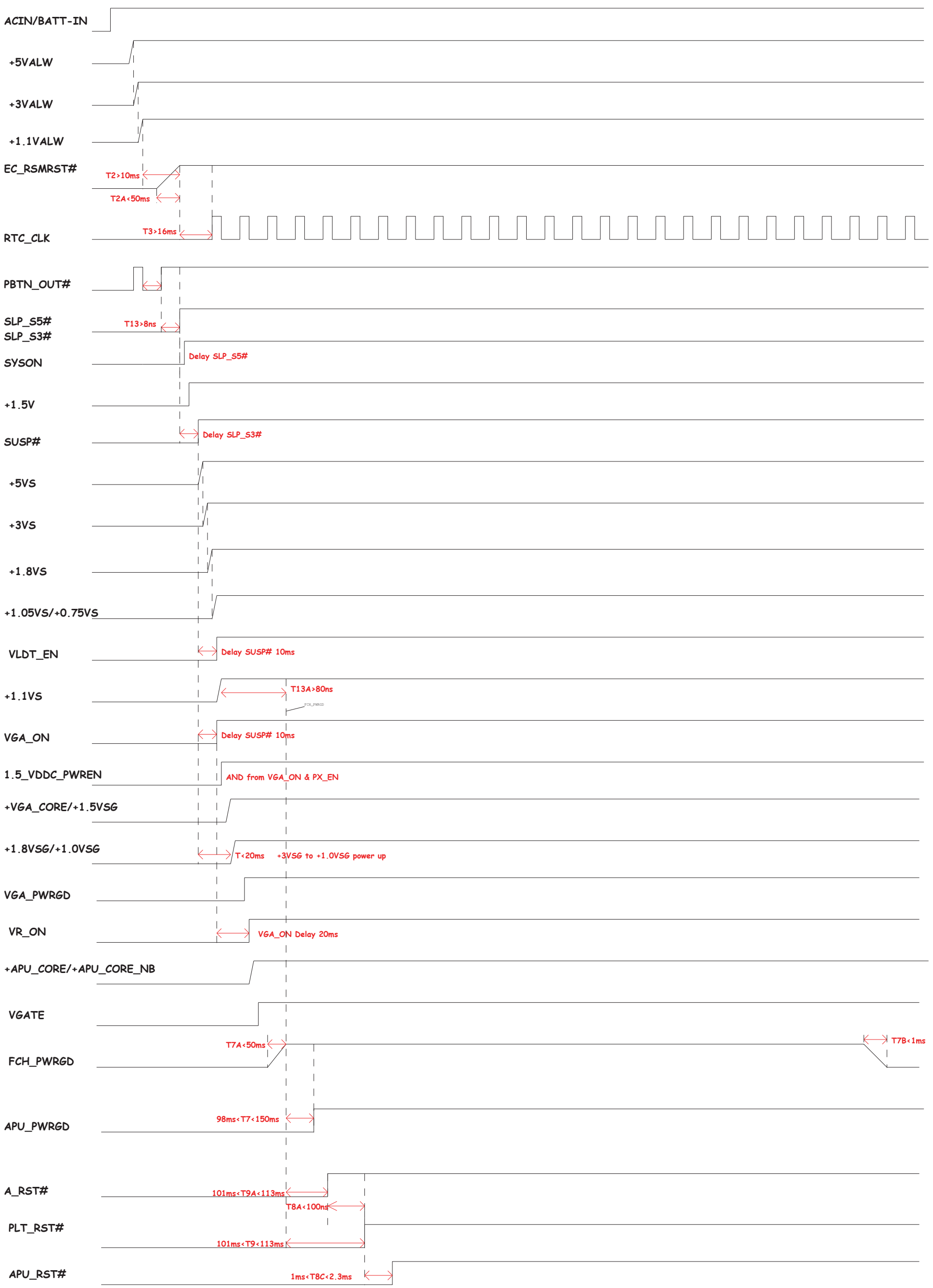
Title: VGA_CORE

Size | Document Number: LAXXXX | Rev: 0.1

Date: Friday, April 29, 2011 | Sheet 48 of 49

Item	Reason for change	PG#	Modify List	Date	Phase
1					
2					
3					
4					
5					
6					
7					

POWER SEQUENCE



Security Classification	Compal Secret Data		
Issued Date	2010/06/30	Deciphered Date	2012/06/30

Title: Power Sequence
Size | Document Number: LA-7553P | Rev: 0.22
Date: Friday, April 29, 2011 | Sheet 50 of 51

Version change list (P.I.R. List)

Item	Fixed Issue	Reason for change	Rev.	PG#	Modify List	Date	Phase
1		For AMD reuqest	0.11	PG#26	Translator change to ANX3110	03/15	ER
2		For AI charge function	0.11	PG#34	Add U2 & U55	03/15	ER
3		For PBL70 MEMO	0.11	PG#32	Change LED1 to Green color.	03/15	ER
4		For LED brightness.	0.11	PG#32	Change R1584 to 100 ohm. Change R1586,R1588,R1591,R1592,R1593 to 100 ohm	03/15	ER
5		For LED1 brightness.	0.11	PG#32	Change LED1 power to 3VALW	03/15	ER
6		For USB3.0 & AI charger	0.12	PG#30	USBP0 connect to JUSB1 and USBP10 connect to JUSB2	03/22	ER
7		For LED1	0.12	PG#35	LED1 connect to +3VALW	03/22	ER
8		For +5VS rising time	0.2	PG#38	R1103 change to 47K	03/25	ER
9		For AI charger	0.2	PG#30	U2 reserve CEN# to EC	03/25	ER
10		For AMD spec	0.2	PG#27	R1642 & R1646 change to 4.7K ohm	03/25	ER
11		For share ROM request	0.2	PG#15 PG#16	Unpop U28,R626,R935,R934,R35,C466 Pop R910,unpop R921	03/25	ER
12		For +3VS leakage from CRT	0.21	PG#27	Add Q101,R1644,R1645 Delete R17,R31	03/31	PR
13		For Crystal EA	0.21	PG#13	Y4 change to SJ100007N00	03/31	PR
14		For EMI ISN	0.22	PG#31	C1636 change to 100P	04/19	PR
15		For thermal team recommand	0.22	PG#19	Add R1816,R1817 reserve R1814,R1815	04/19	PR
16		For BRD ID	0.22	PG#32	Change R1606 to 215K.	04/19	PR
17		Reserve PX_EN signal	0.22	PG#32	Reserve PX_EN signal to EC pin74	04/19	PR
18		For JDIMM1 and JDIMM2 location definition	0.22	PG#11 PG#12	Swap JDIMM1 and JDIMM2 location	04/19	PR
19		Prevent the leakage from CRT monitor.	0.23	PG#27	Add R1644, R1645, Q2 and Del R17, R31.	04/22	PR
20		for EMI request	0.23	PG#31	H1 change to connect to GND	04/22	PR
21		Don't use for MP	0.23	PG#13	Unpop C1193	04/22	PR
22		For VGA Sequence.	0.23	PG#38	Change R1127 from 470 ohm to 33 ohm.	04/22	PR
23		for EMI request	1.0	PG#30	modify USB3.0 redriver schemaitc	04/25	PR
24		For de-emphasis USB3.0 signal	1.0	PG#30	reserve TEST and I2C_EN net	04/25	PR
25		For some HDMI device detect error	1.0	PG#28	Change R200,R201 to 3.9K ohm	04/25	PR
26		For WLAN module rising time specification	1.0	PG#35	Change R114 to 20K ohm C1663 change to 4700P	04/25	PR
27							

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Title: HW-PIR

Size: Custom | Document Number: LA-7322P | Rev: 0.22

Date: Friday, April 29, 2011 | Sheet 51 of 51

Item	Fixed Issue	Reason for change	Rev.	PG#	Modify List	Date	Phase
1		Reduce the component count for MP.	1.0		Change below the footprints from 0 ohm to R short.	04/25	PR

Reference	Value	Source Part	Source Library	Page	Schematic
R1800	0_0402_5%	R-SHORT	X:\CIS_SYM...	P06-FS1 P...	SCHEMAT...
R1801	0_0402_5%	R-SHORT	X:\CIS_SYM...	P06-FS1 P...	SCHEMAT...
R591	0_0402_5%	R-SHORT	X:\CIS_SYM...	P08-FS1 Di...	SCHEMAT...
R598	0_0402_5%	R-SHORT	X:\CIS_SYM...	P08-FS1 Di...	SCHEMAT...
R606	0_0402_5%	R-SHORT	X:\CIS_SYM...	P08-FS1 Di...	SCHEMAT...
R608	0_0402_5%	R-SHORT	X:\CIS_SYM...	P08-FS1 Di...	SCHEMAT...
R611	0_0402_5%	R-SHORT	X:\CIS_SYM...	P08-FS1 Di...	SCHEMAT...
R162	0_0402_5%	R-SHORT	X:\CIS_SYM...	P13-HUDS...	SCHEMAT...
R163	0_0402_5%	R-SHORT	X:\CIS_SYM...	P13-HUDS...	SCHEMAT...
R565	0_0402_5%	R-SHORT	X:\CIS_SYM...	P13-HUDS...	SCHEMAT...
R566	0_0402_5%	R-SHORT	X:\CIS_SYM...	P13-HUDS...	SCHEMAT...
R568	0_0402_5%	R-SHORT	X:\CIS_SYM...	P13-HUDS...	SCHEMAT...
R570	0_0402_5%	R-SHORT	X:\CIS_SYM...	P13-HUDS...	SCHEMAT...
R607	0_0402_5%	R-SHORT	X:\CIS_SYM...	P13-HUDS...	SCHEMAT...
R612	0_0402_5%	R-SHORT	X:\CIS_SYM...	P13-HUDS...	SCHEMAT...
R81	0_0402_5%	R-SHORT	X:\CIS_SYM...	P14-HUDS...	SCHEMAT...
R912	0_0402_5%	R-SHORT	X:\CIS_SYM...	P16-HUDS...	SCHEMAT...
R1145	0_0603_5%	R-SHORT	X:\CIS_SYM...	P17-HUDS...	SCHEMAT...
R1148	0_0603_5%	R-SHORT	X:\CIS_SYM...	P17-HUDS...	SCHEMAT...
R19	0_0603_5%	R-SHORT	X:\CIS_SYM...	P17-HUDS...	SCHEMAT...
R20	0_0603_5%	R-SHORT	X:\CIS_SYM...	P17-HUDS...	SCHEMAT...
R22	0_0402_5%	R-SHORT	X:\CIS_SYM...	P17-HUDS...	SCHEMAT...
R23	0_0402_5%	R-SHORT	X:\CIS_SYM...	P17-HUDS...	SCHEMAT...
R24	0_0402_5%	R-SHORT	X:\CIS_SYM...	P17-HUDS...	SCHEMAT...
R25	0_0603_5%	R-SHORT	X:\CIS_SYM...	P17-HUDS...	SCHEMAT...
R26	0_0402_5%	R-SHORT	X:\CIS_SYM...	P17-HUDS...	SCHEMAT...
R27	0_0402_5%	R-SHORT	X:\CIS_SYM...	P17-HUDS...	SCHEMAT...
R28	0_0402_5%	R-SHORT	X:\CIS_SYM...	P17-HUDS...	SCHEMAT...
R937	0_0805_5%	R-SHORT	X:\CIS_SYM...	P17-HUDS...	SCHEMAT...
R938	0_0805_5%	R-SHORT	X:\CIS_SYM...	P17-HUDS...	SCHEMAT...
R941	0_0805_5%	R-SHORT	X:\CIS_SYM...	P17-HUDS...	SCHEMAT...
R945	0_0402_5%	R-SHORT	X:\CIS_SYM...	P17-HUDS...	SCHEMAT...
R483	0_0402_5%	R-SHORT	X:\CIS_SYM...	P23-VRA...	SCHEMAT...
R485	0_0402_5%	R-SHORT	X:\CIS_SYM...	P23-VRA...	SCHEMAT...
R511	0_0402_5%	R-SHORT	X:\CIS_SYM...	P24-VRA...	SCHEMAT...
R513	0_0402_5%	R-SHORT	X:\CIS_SYM...	P24-VRA...	SCHEMAT...
R1291	0_0402_5%	R-SHORT	X:\CIS_SYM...	P26-LVDS ...	SCHEMAT...
R527	0_0805_5%	R-SHORT	X:\CIS_SYM...	P26-LVDS ...	SCHEMAT...
R529	0_0805_5%	R-SHORT	X:\CIS_SYM...	P26-LVDS ...	SCHEMAT...
R1634	0_0402_5%	R-SHORT	X:\CIS_SYM...	P27-LVDS ...	SCHEMAT...
R1635	0_0402_5%	R-SHORT	X:\CIS_SYM...	P27-LVDS ...	SCHEMAT...
R1636	0_0402_5%	R-SHORT	X:\CIS_SYM...	P27-LVDS ...	SCHEMAT...
R1641	0_0402_5%	R-SHORT	X:\CIS_SYM...	P27-LVDS ...	SCHEMAT...
R1643	0_0603_5%	R-SHORT	X:\CIS_SYM...	P27-LVDS ...	SCHEMAT...
R1650	0_0603_5%	R-SHORT	X:\CIS_SYM...	P27-LVDS ...	SCHEMAT...
R1651	0_0402_5%	R-SHORT	X:\CIS_SYM...	P27-LVDS ...	SCHEMAT...
R535	0_0603_5%	R-SHORT	X:\CIS_SYM...	P31-LAN ...	SCHEMAT...
R536	0_0603_5%	R-SHORT	X:\CIS_SYM...	P31-LAN ...	SCHEMAT...
R544	0_0402_5%	R-SHORT	X:\CIS_SYM...	P31-LAN ...	SCHEMAT...
R1531	0_0805_5%	R-SHORT	X:\CIS_SYM...	P33-HD A...	SCHEMAT...
R1534	0_0603_5%	R-SHORT	X:\CIS_SYM...	P33-HD A...	SCHEMAT...
R1537	0_0603_5%	R-SHORT	X:\CIS_SYM...	P33-HD A...	SCHEMAT...
R1560	0_0603_5%	R-SHORT	X:\CIS_SYM...	P34-RTS5...	SCHEMAT...

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6	7	8	9
10	11	12	13
14	15	16	17
18	19	20	21
22	23	24	25
26	27		

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Title: HW-PIR3

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Date: Friday, April 29, 2011 | Sheet 53 of 53