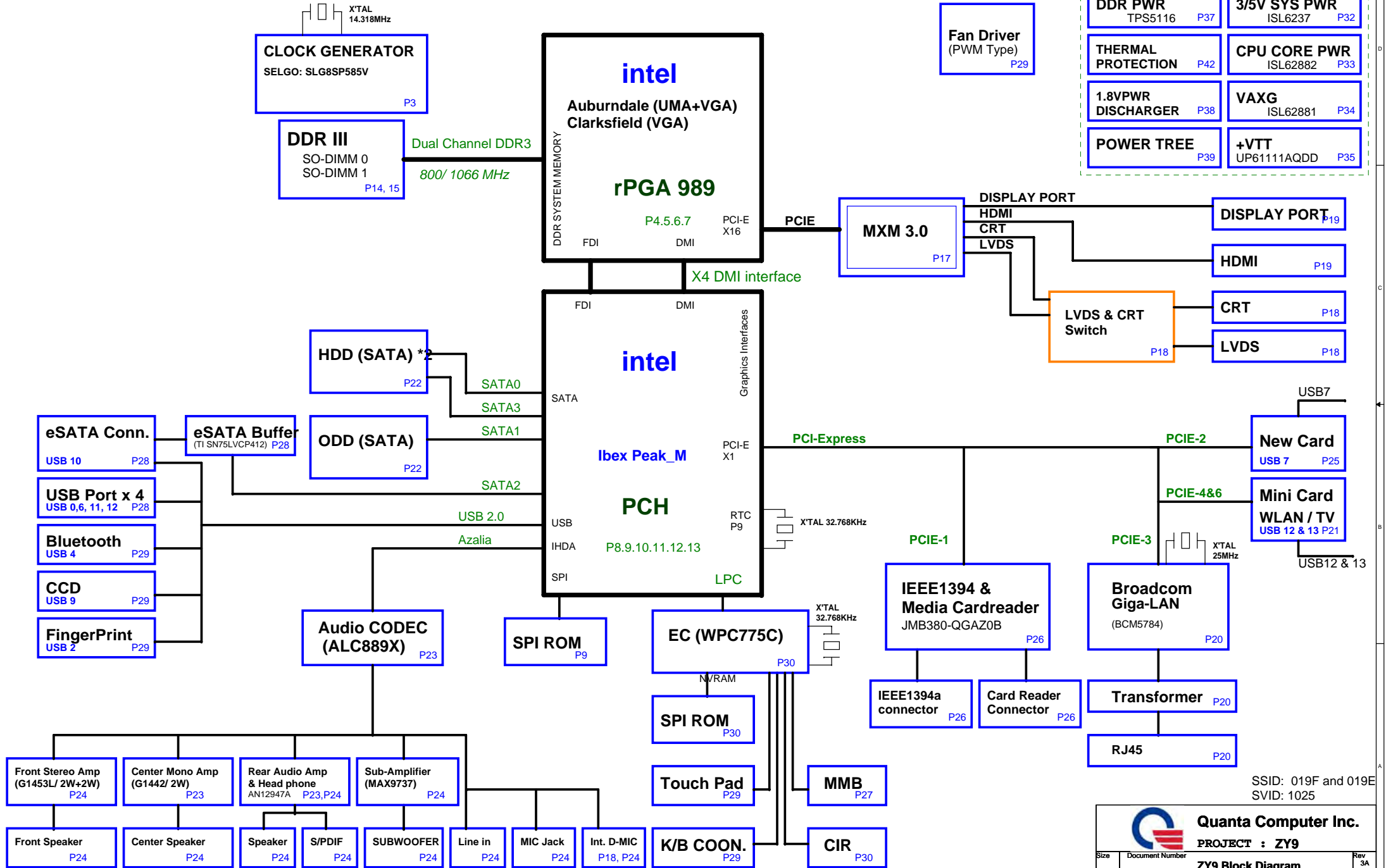


31ZY9MB0000
 ZY9 MB ASSY(DC/GM/MXM)ASSY W/O CPU
 31ZY9MB0010
 ZY9 MB ASSY(QC/GM/MXM)ASSY W/O CPU

ZY9 SYSTEM BLOCK DIAGRAM



SSID: 019F and 019E
 SVID: 1025

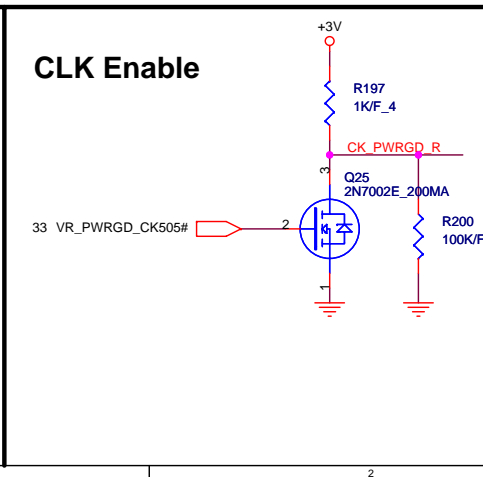
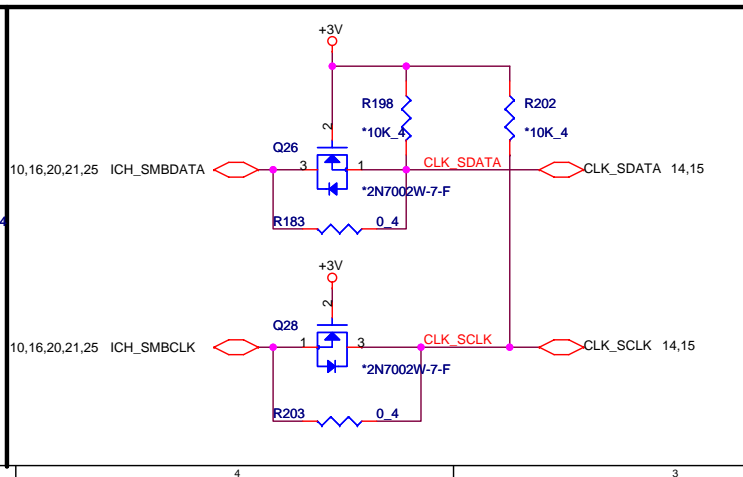
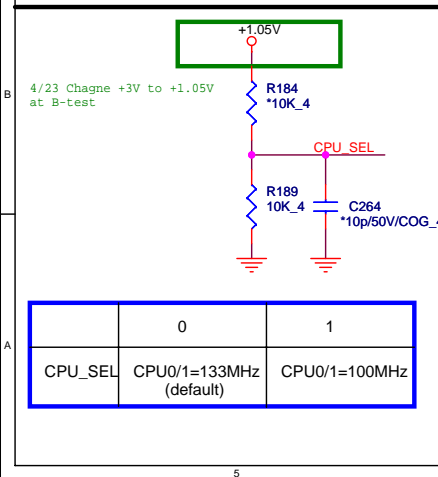
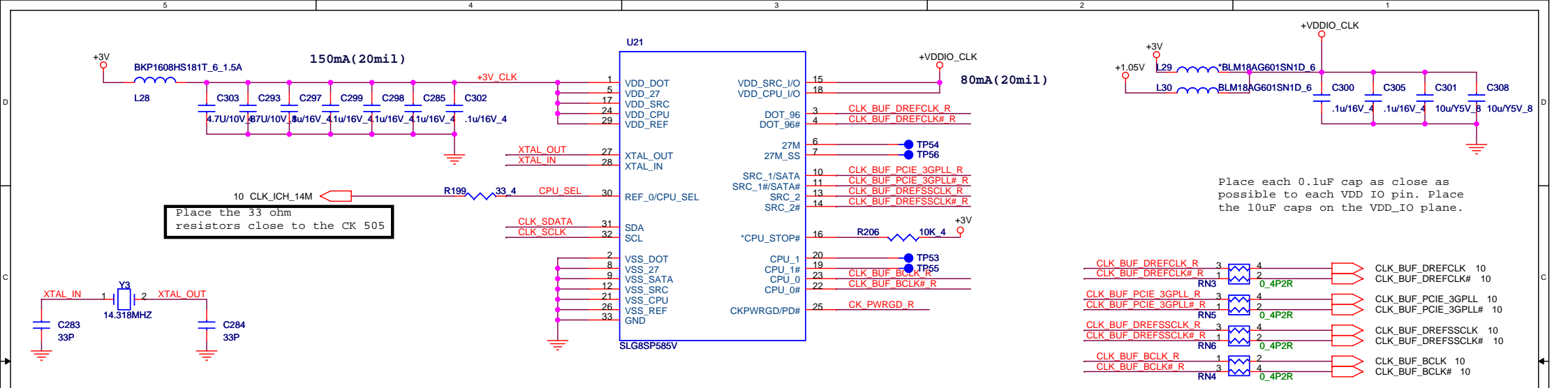
Table of Contents

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1	Schematic Block Diagram
2	Front Page
3	Clock Generator (SLG8SP585V)
4-7	CPU (Clarksfield)
8-13	PCH (Ibex Peak-M)
14-15	DDRIII SO-DIMM
16	BRAIDWOOD
17	MXM3.0
18	CRT/LVDS Conn
19	HDMI / Display port
20	LAN (BCM5784M)
21	MINI PCIE
22	SATA HDD/ODD
23-24	Audio CODEC(ALC889X) /Phone Jack
25	NEW CARD
26	Card Reader (JMB380) / 1394
27	MMB /LED
28	USB / E-SATA
29	KB / FAN /TP /CCD /BT
30	EC /FLASH /CIR
31	Charger (ISL88731)
32	5V /3V (ISL6237)
33	CPU Core (ISL62882)
34	+VTT (UP6111AQDD)
35	+1.05V (UP6111AQDD)
36	DDR 1.5V (TPS51116)
37	Discharge /1.8V
38	POWER TREE TABLE
39	PCH POWER PLANE
40	POWER Management
41	Thermal protection
42	change list

Power States

POWER PLANE	VOLTAGE	DESCRIPTION	CONTROL SIGNAL	ACTIVE IN
VIN	+10V~+19V	MAIN POWER		S0~S5
+RTC_CELL	+3V~+3.3V	RTC		S0~S5
+3VPCU	+3.3V	8051 POWER	ALWON	S0~S5
+5VPCU	+5V	CHARGE POWER	ALWON	S0~S5
+15V	+15V	LARGE POWER	+15V_ALWP	S0~S5
3V_LAN_S5	+3.3V	LAN POWER	AUX_ON	
+5VSUS	+5V		SUSD	
+3VSUS	+3.3V		SUSD	
+1.5VSUS	+1.5V	SODIMM POWER	SUSON	
+0.75V_DDR_VTT	+0.9V	SODIMM POWER	MAINON	
+5V	+5V		MAIND	
+3V	+3.3V		MAIND	
+1.8V	+1.8V		MAINON	
+1.5V	+1.5V	PCH POWER	MAIND	
+1.1V_VTT	+1.05V~+1.1V	CPU POWER	MAINON	
+1.05V	+1.05V	PCH POWER	MAINON	
+VCC_CORE	0V~+1.5V	CPU CORE POWER	VRON	
LCDVCC	+3.3V	LCD Power	LVDS_VDDEN	
MBAT+	+10V~+17V	MAIN BATTERY		
+5V_S5	+5V		S5_ON	
+3V_S5	+3.3V		S5D	

GND PLANE	PAGE	DESCRIPTION
▽ LANGND	20	
▽ E775AGND	30	
▽ ADOGND	23.24	
≡ GND	ALL	

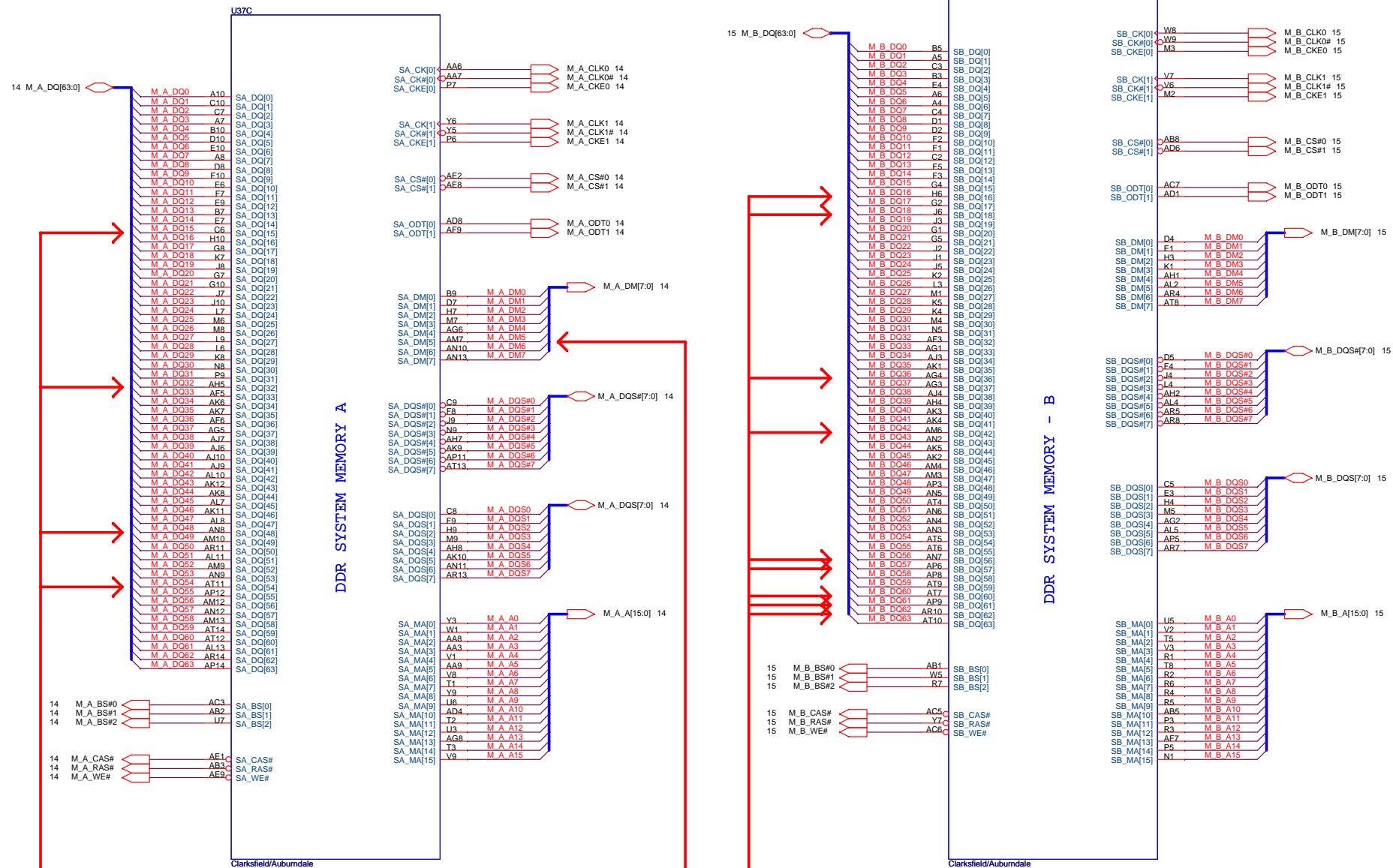


Quanta Computer Inc.

PROJECT : ZY9

Size	Document Number	Rev
	Clock Generator	3A
Date:	Thursday, August 20, 2009	Sheet 3 of 42

AUBURNDALE/CLARKSFIELD PROCESSOR (DDR3)

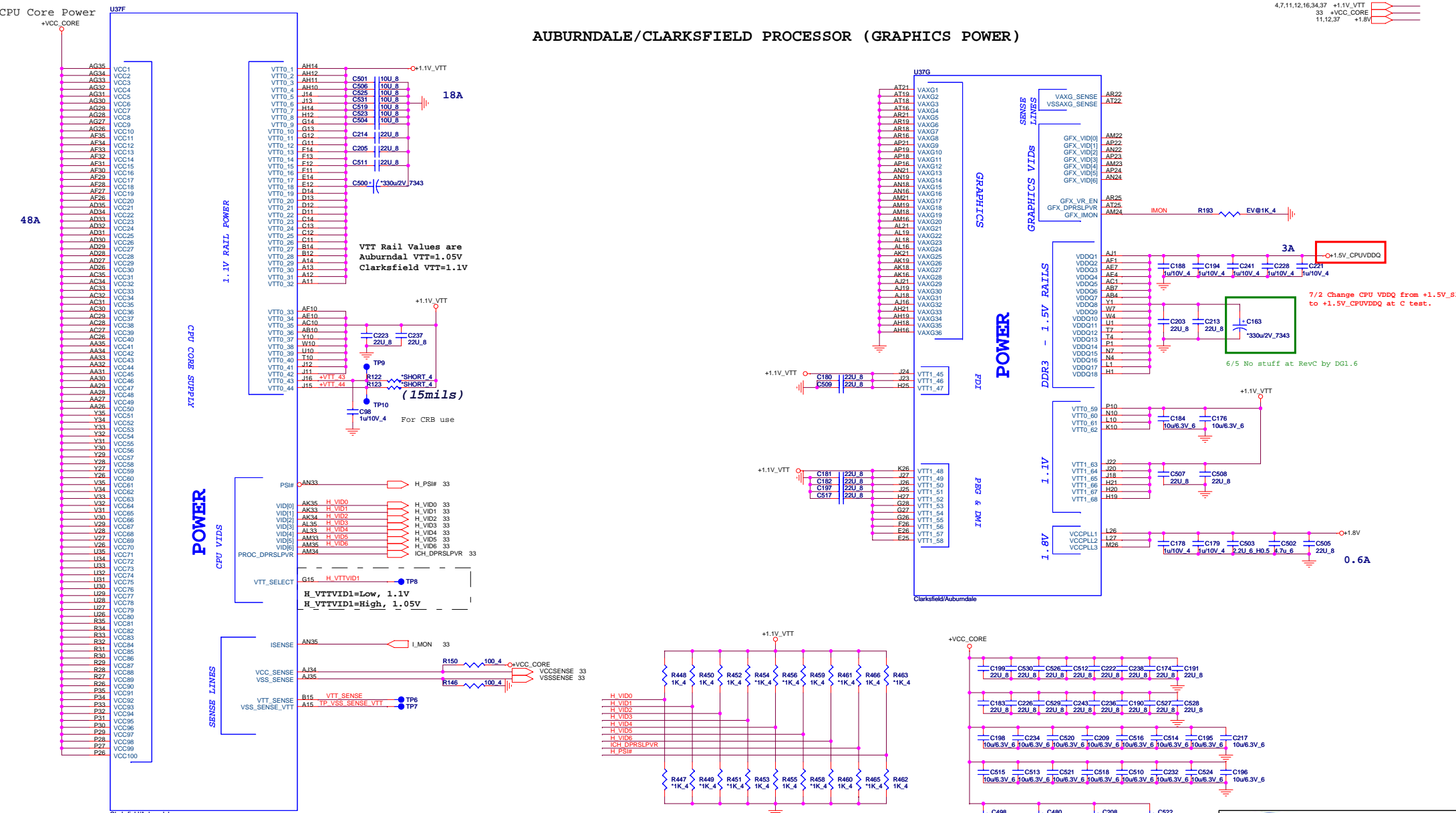


Channel A DQ[15,32,48,54], DM[5]
Requires minimum 12mils spacing
with all other signals, including data signals.

Channel B DQ[16,18,36,42,56,57,60,61,62]
Requires minimum 12mils spacing
with all other signals, including data signals.

DM signals are not present on Clarkfield processor. All DM signal can be left as NC on Clarkfield and connect directly to GND on So-DIMM side for Clarkfield design only

AUBURNDALE/CLARKSFIELD PROCESSOR (GRAPHICS POWER)



AUBURNDALE/CLARKSFIELD PROCESSOR (POWER)

Note:
For Validating IMVP VR R6451 should be STUFF
and R641 NO_STUFF

HFM_VID : Max 1.4V
LFM_VID : Min 0.65V

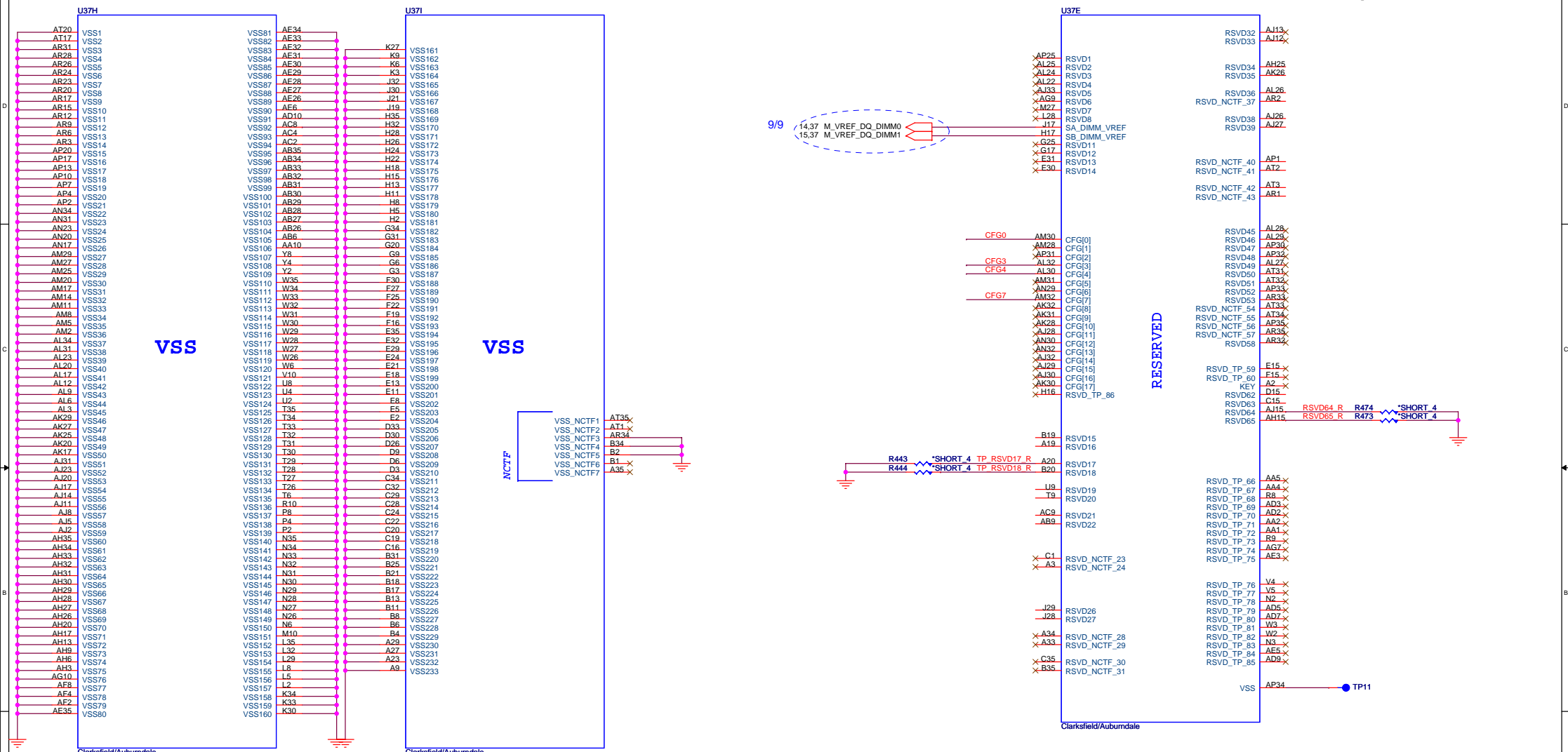
Quanta Computer Inc.
PROJECT : ZY9

Size: Document Number
AUBURND A/34
Date: Tuesday, August 18, 2009 Sheet: 6 of 42

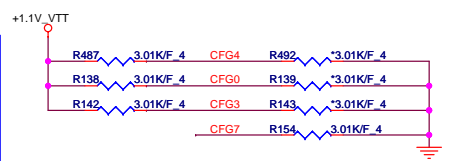
Rev: 3A

AUBURNDALE/CLARKSFIELD PROCESSOR (GND)

AUBURNDALE/CLARKSFIELD PROCESSOR (RESERVED, CFG)



The Clarkfield processor's PCI Express interface may not meet PCI Express 2.0 jitter specifications. Intel recommends placing a 3.01K +/- 5% pull down resistor to VSS on CFG[7] pin for both rPGA and BGA components. This pull down resistor should be removed when this issue is fixed.



Processor Strapping

	1	0
CFG4 (Display Port Presence)	Disabled; No Physical Display Port attached to Embedded Display Port	Enabled; An external Display port device is connected to the Embedded Display port
CFG0 (PCI-Epress Configuration Select)	Single PEG	Bifurcation enabled
CFG3 (PCI-Epress Static Lane Reversal)	Normal Operation	Lane Numbers Reversed

CFG[1:0] - PCI_Epress Configuration Select
 * 11= 1 x 16 PEG
 * 10= 2 x 8 PEG

Quanta Computer Inc.
PROJECT : ZY9

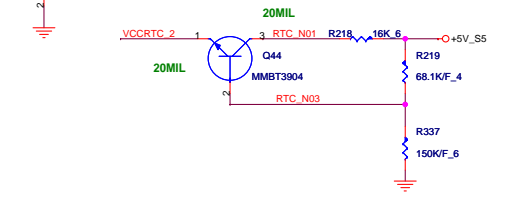
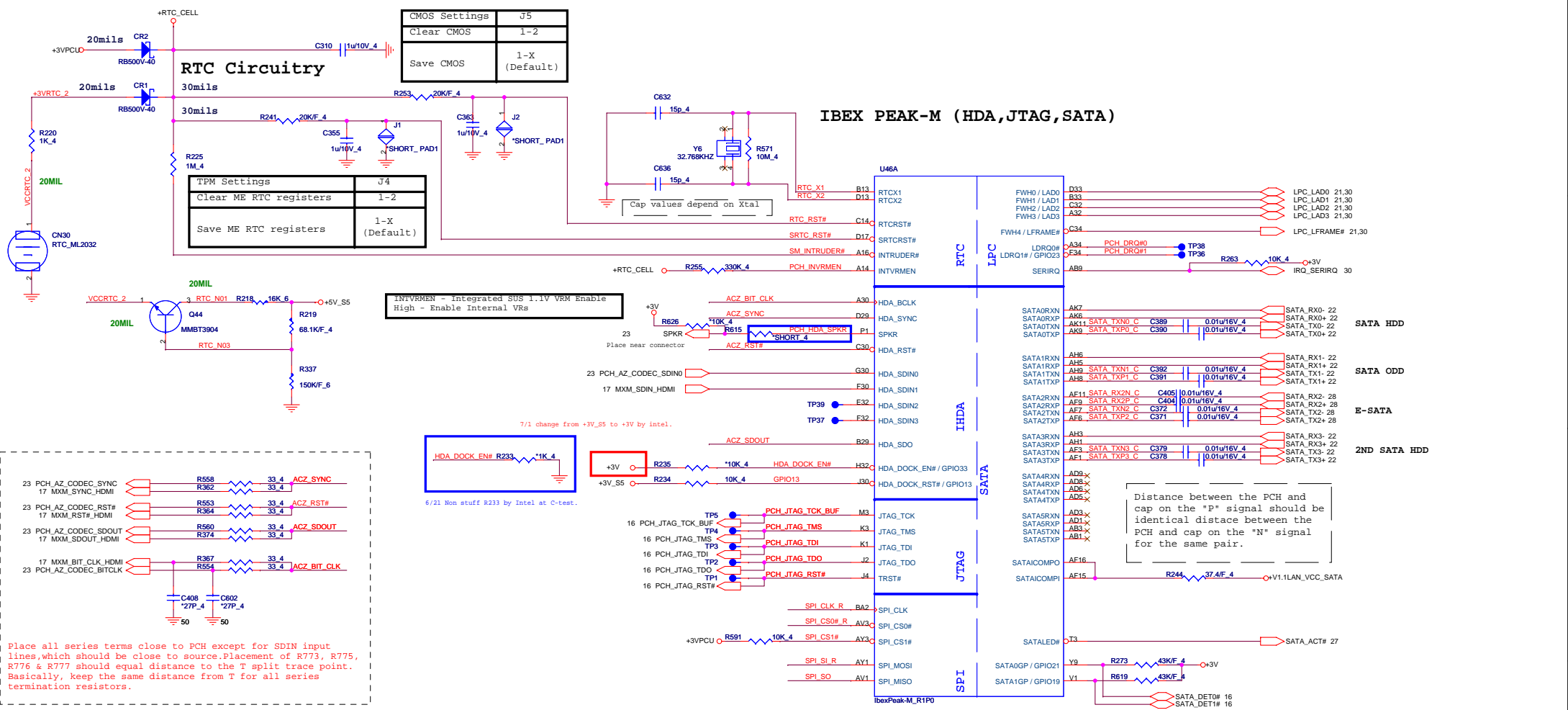
Size	Document Number	Rev
	AUBURND4/4	3A
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RTC Circuitry

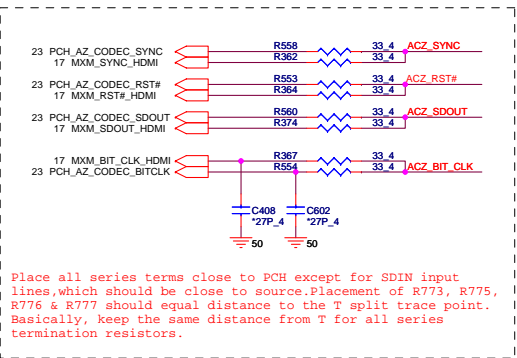
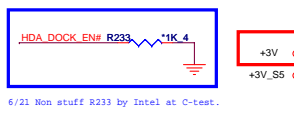
CMOS Settings	J5
Clear CMOS	1-2
Save CMOS	1-X (Default)

TPM Settings	J4
Clear ME RTC registers	1-2
Save ME RTC registers	1-X (Default)

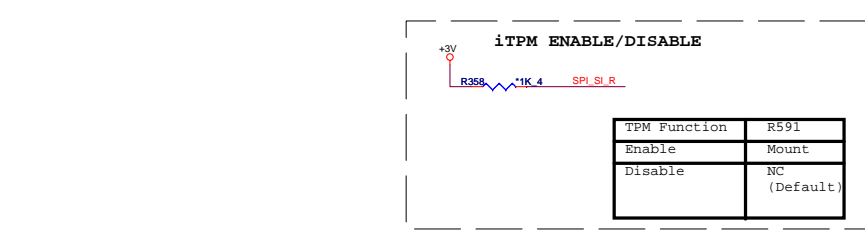
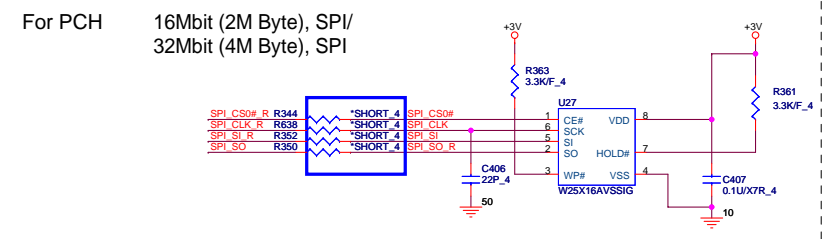
IBEX PEAK-M (HDA, JTAG, SATA)



INVRMEN - Integrated SUS 1.1V VRM Enable
High = Enable Internal VRs



Place all series terms close to PCH except for SDIN input lines, which should be close to source. Placement of R773, R775, R776 & R777 should equal distance to the T split trace point. Basically, keep the same distance from T for all series termination resistors.



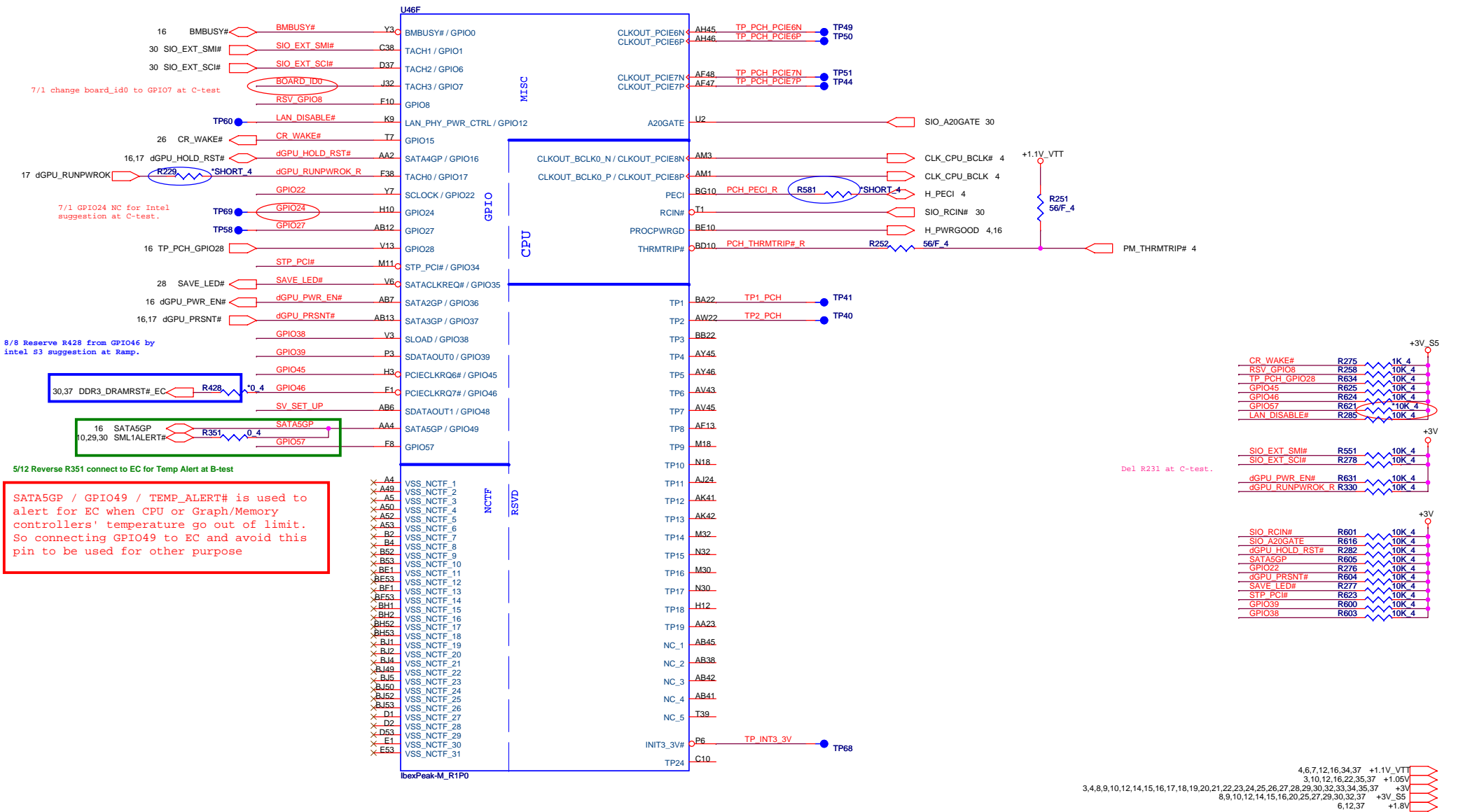
Distance between the PCH and cap on the "P" signal should be identical distance between the PCH and cap on the "N" signal for the same pair.

Quanta Computer Inc.
PROJECT : ZY9

Size	Document Number	Rev
	IBEX PEAK-M 2/6	3A

Date: Tuesday, August 18, 2009 Sheet 9 of 42

IBEX PEAK-M (GPIO,VSS_NCTF,RSVD)



4/9 Reserve GPIO8 by wv14 MoW
7/1 Add R671 for GPIO57 PD and not PU for Intel suggestion at C-test.

Integrated Clock Chip Enable	
RSV_GPIO8	High = Disable Low = Enable
BOARD_ID0	High = Touch Screen Low = Discrete

Danbury Technology Enabled

NV_ALE	High = Enable Low = Disable
--------	--------------------------------

DMI Termination Voltage

NV_CLE	Set to Vcc when LOW Set to Vcc/2 when HIGH
--------	---

5/12 Reverse Q12,Q11 connect to t SYS_SHDN# at B-test

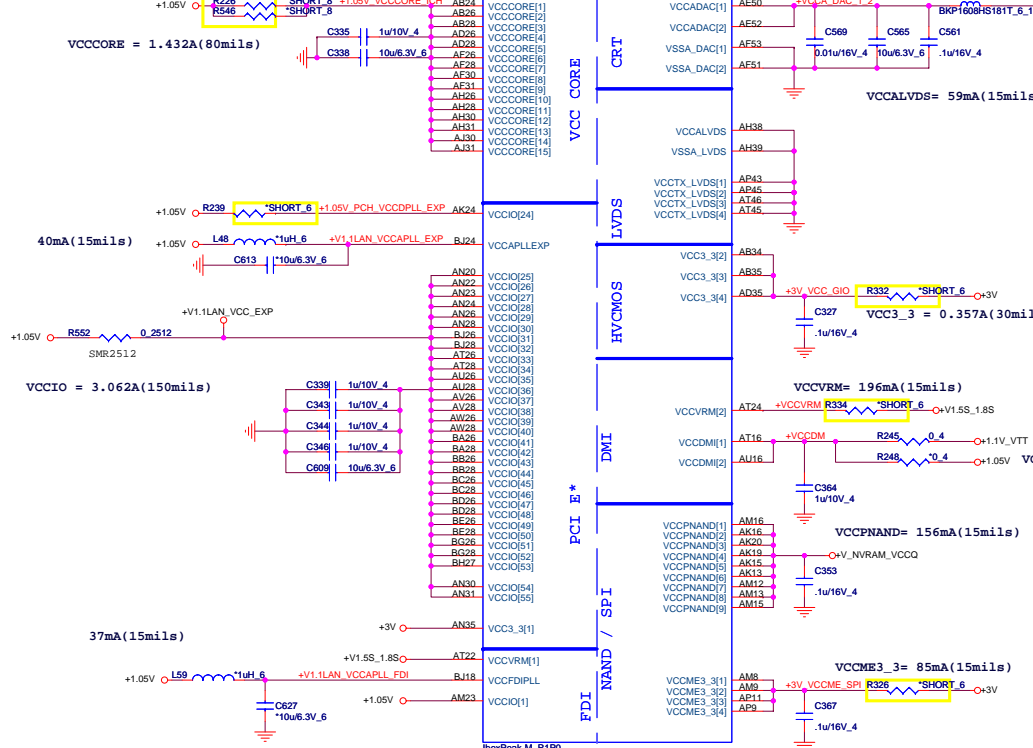
SV_SET_UP	1-X High = Strong (Default)
-----------	-----------------------------

Quanta Computer Inc.
PROJECT : ZY9

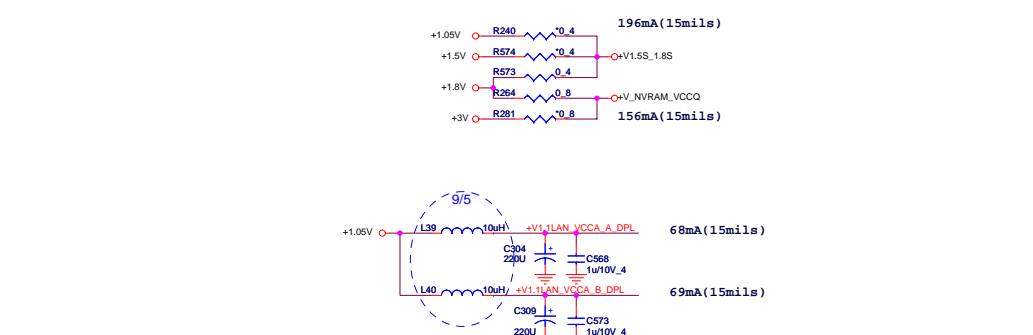
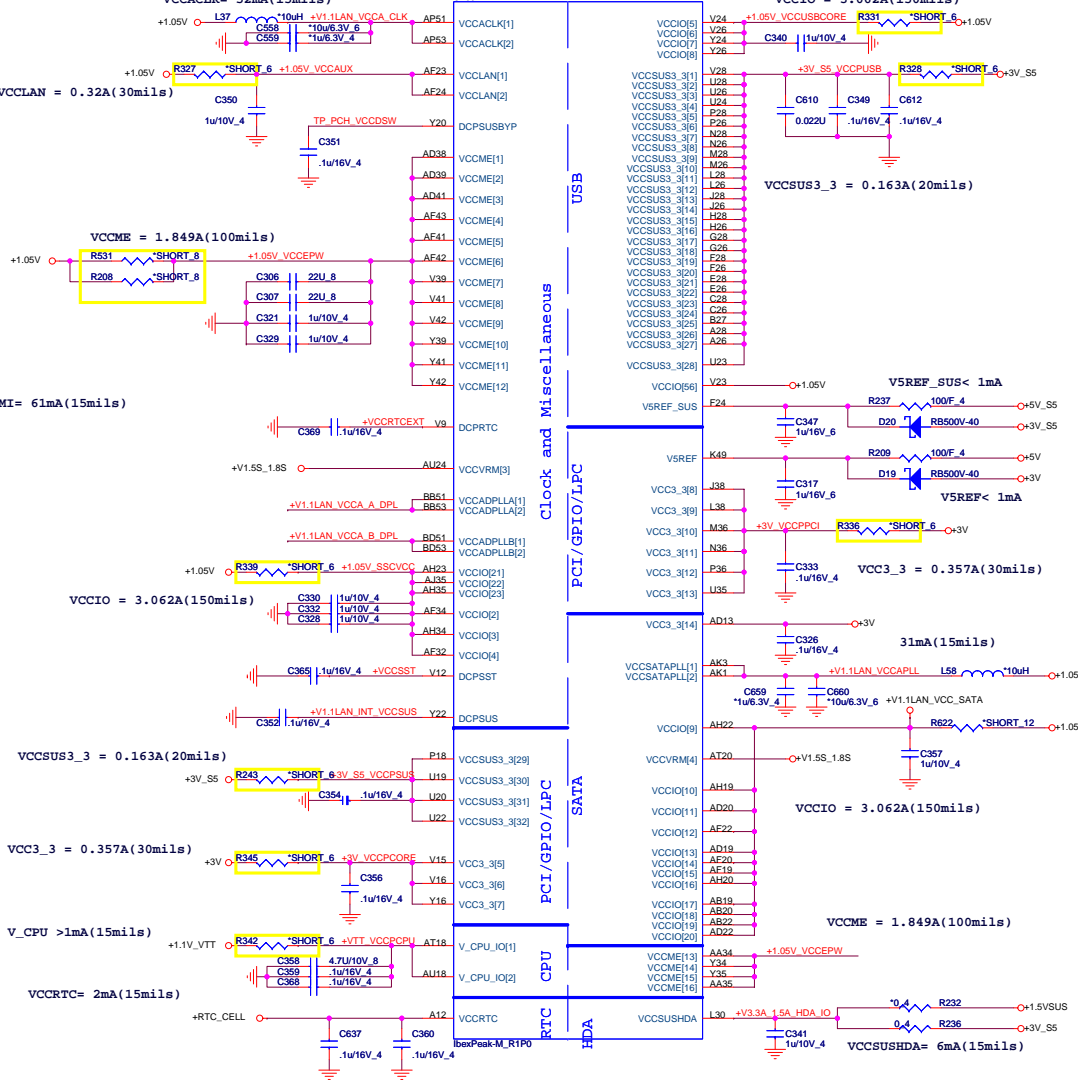
Size: Document Number
IBEX PEAK-M 4/6

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POWER



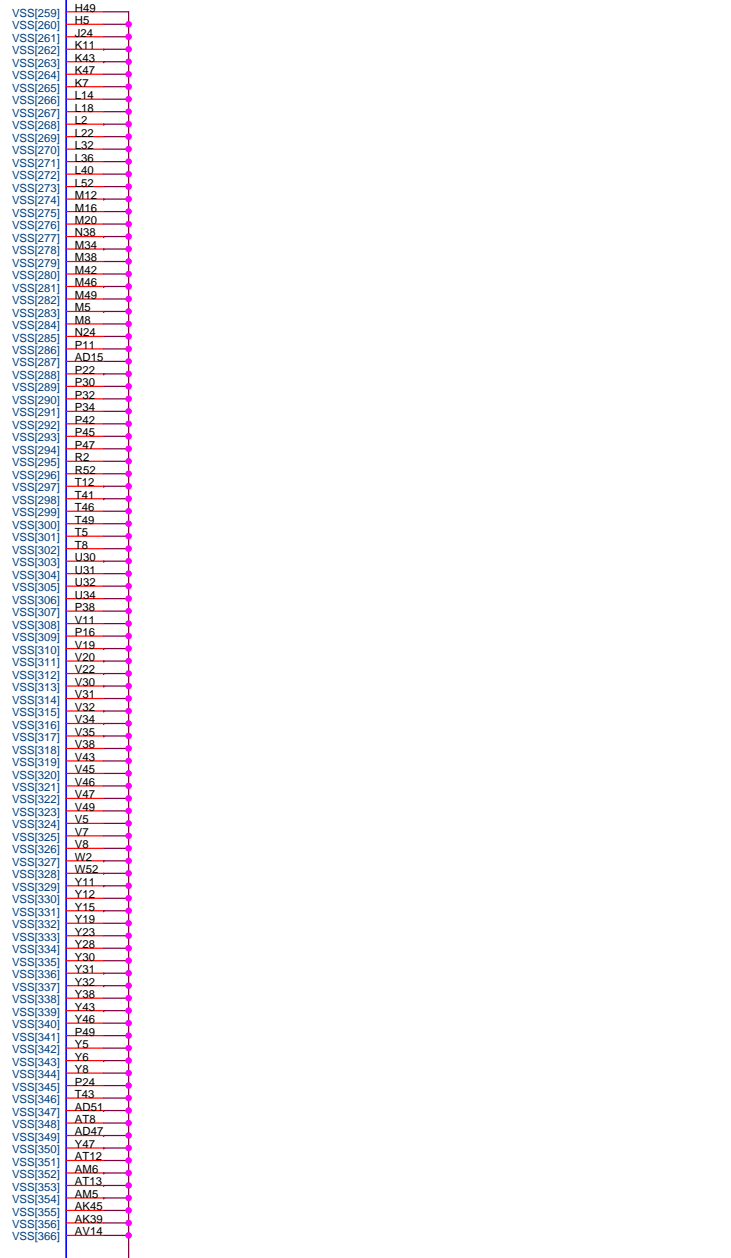
POWER




4,6,7,11,16,34,37	+1.1V_VTT
4,14,15,22,36,37	+1.5VSUS
9,22,28,32,33,34,35,36	+5V_S5
3,10,16,22,35,37	+1.05V
3,4,8,9,10,11,14,15,16,17,18,19,20,21,22,23,24,25,26,27,28,29,30,32,33,34,35,37	+3V
8,9,10,11,14,15,16,20,25,27,29,30,32,37	+3V_S5
6,11,37	+1.8V

Quanta Computer Inc.
PROJECT : ZY9
IBEX PEAK-M 5/6
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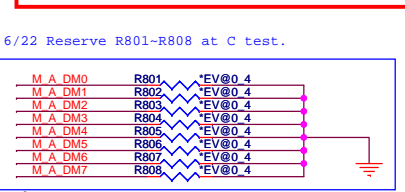
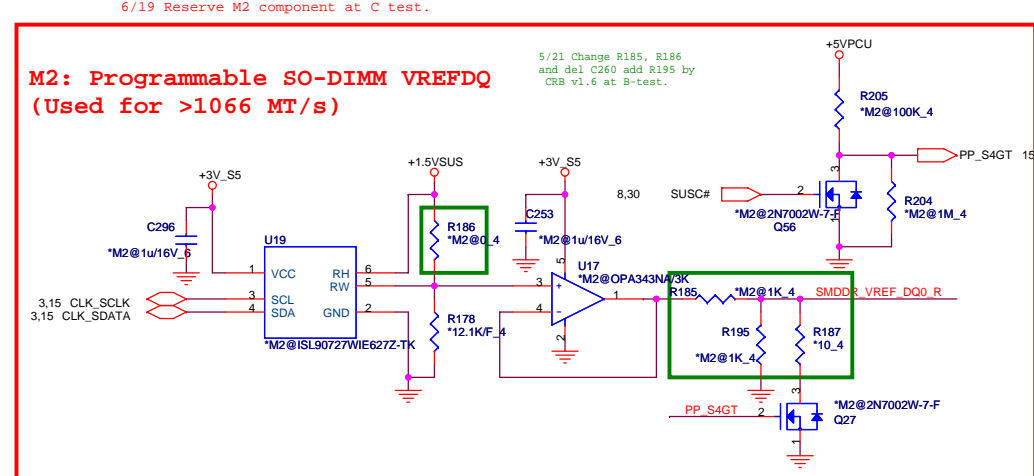
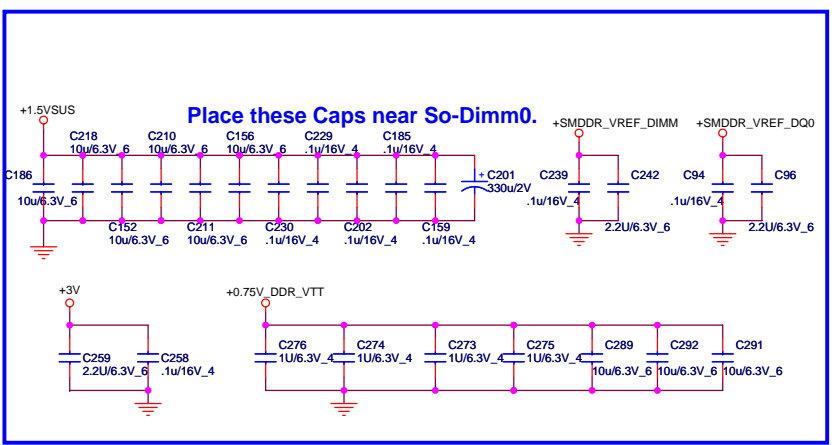
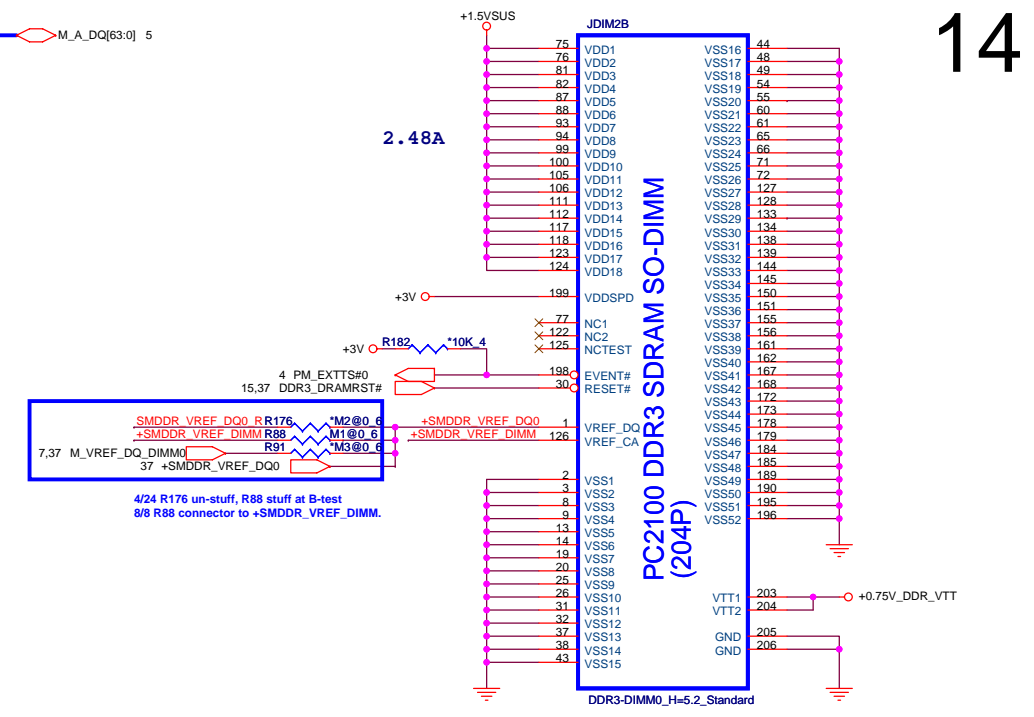
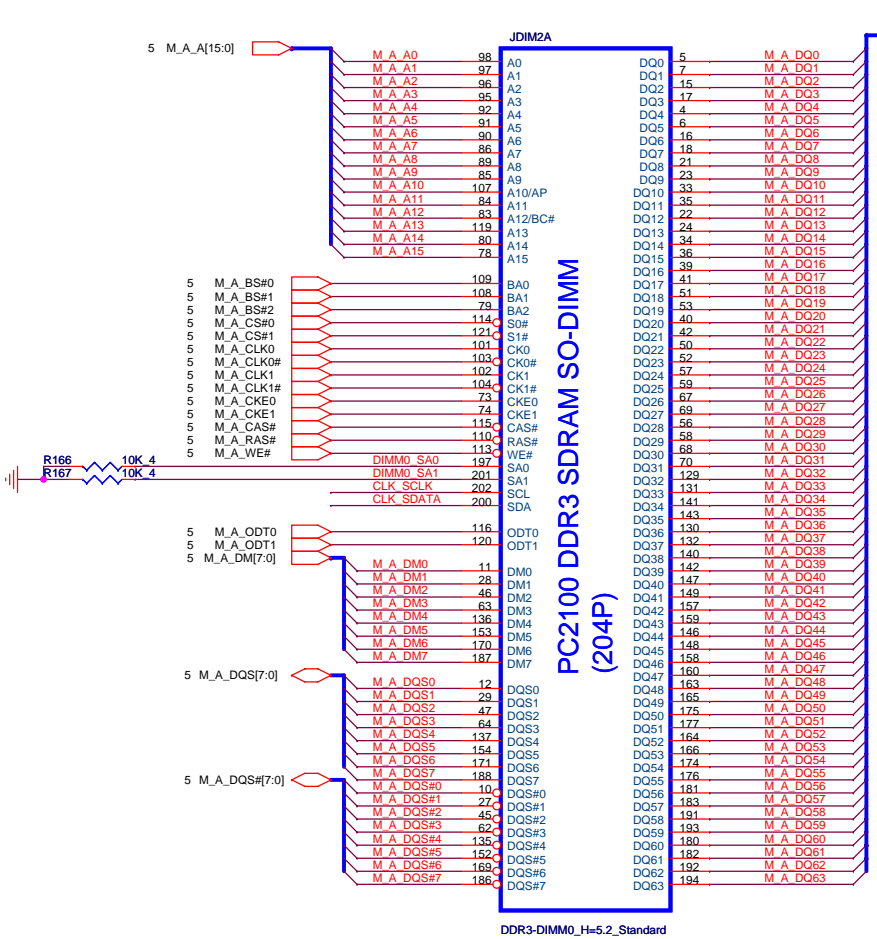
IBEX PEAK-M (GND)

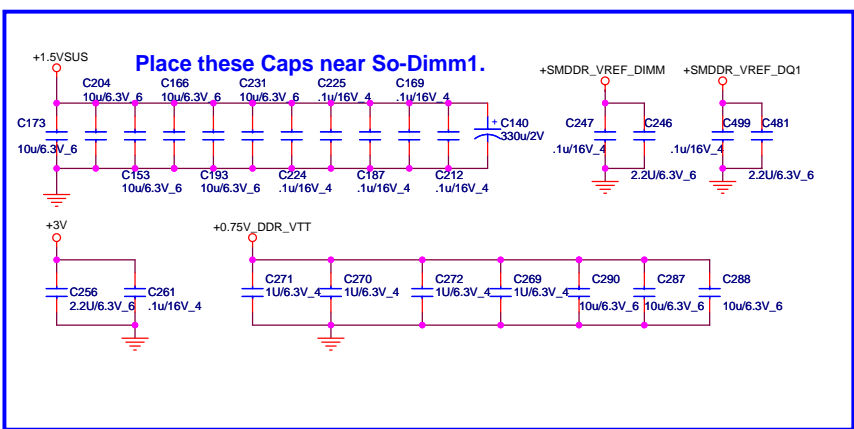
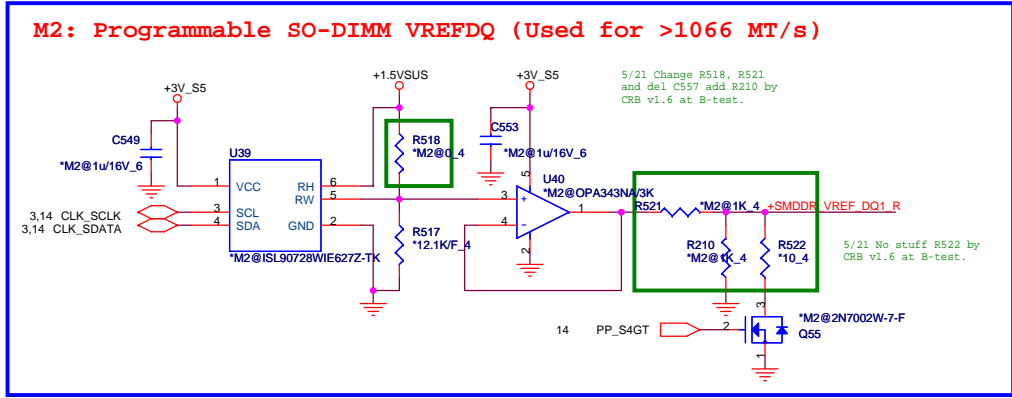
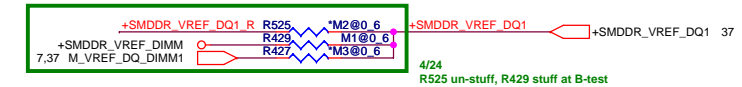
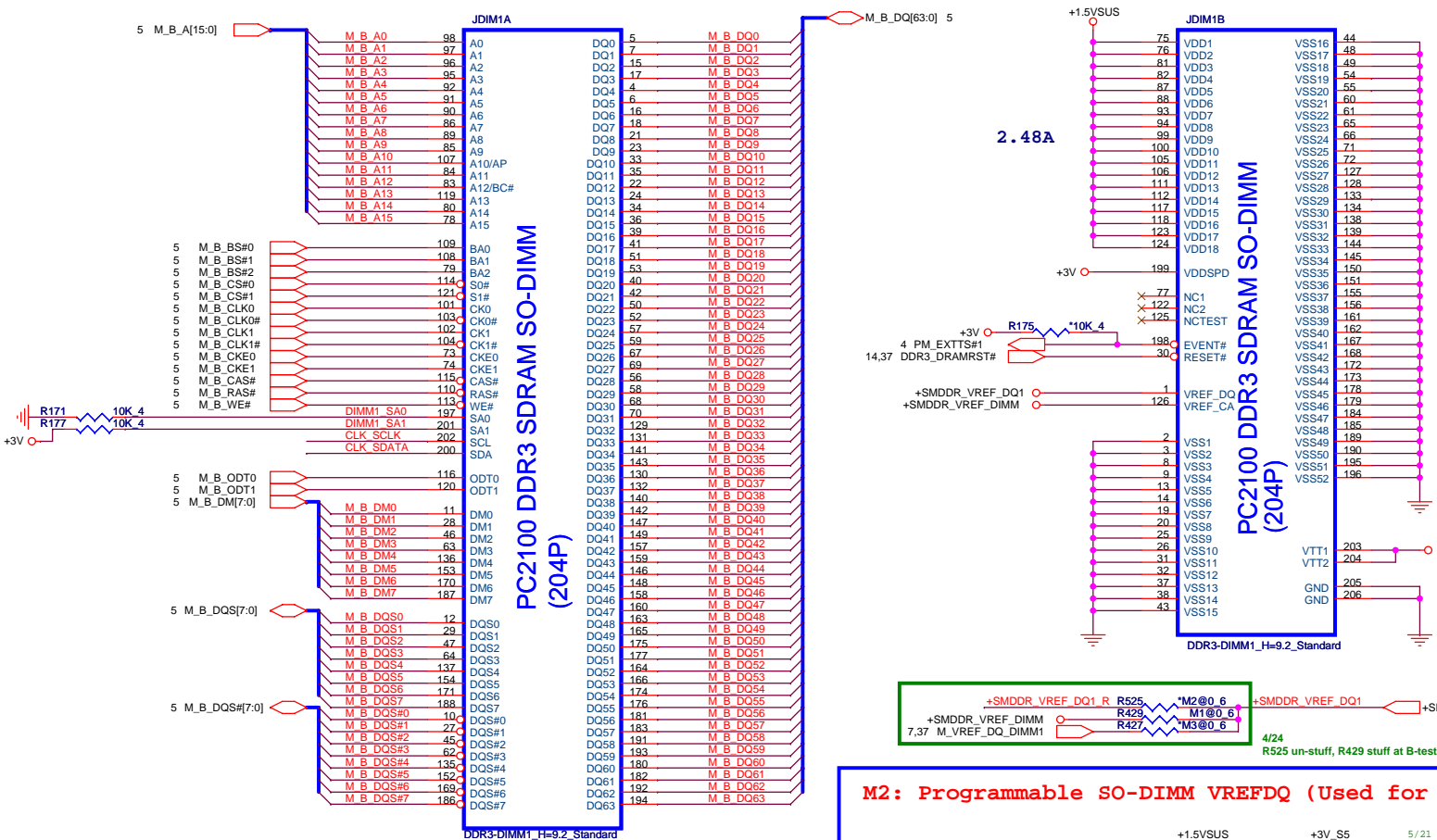




Quanta Computer Inc.
PROJECT : ZY9

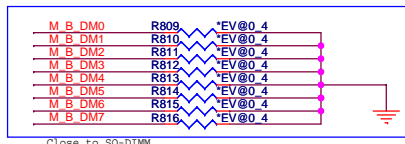
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	IBEX PEAK-M 6/6	3A
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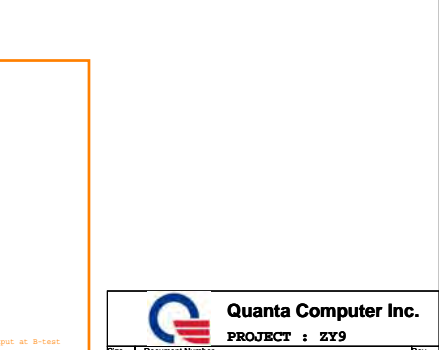
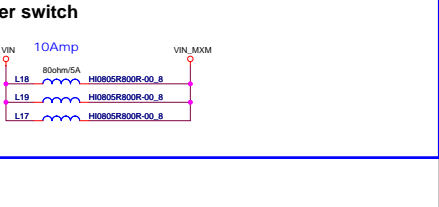
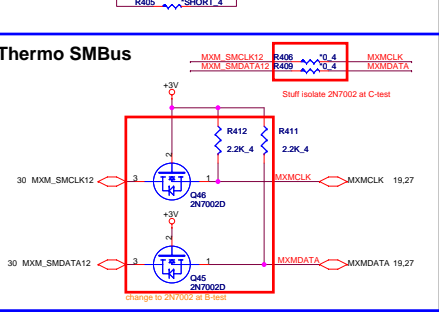
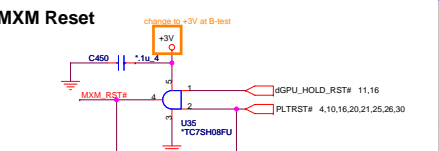
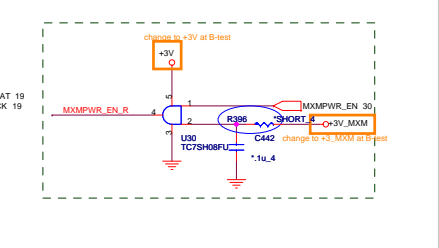
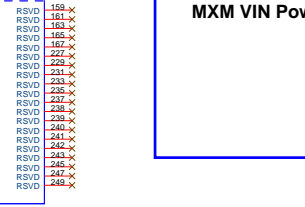
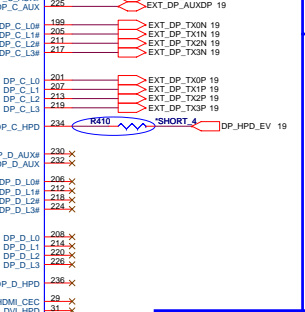
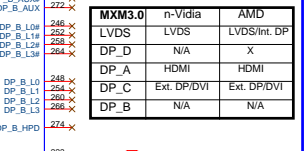
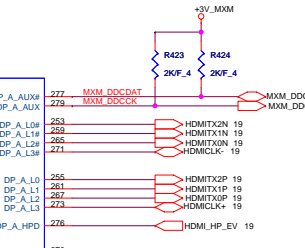
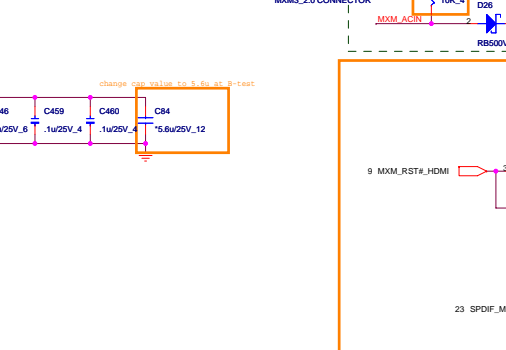
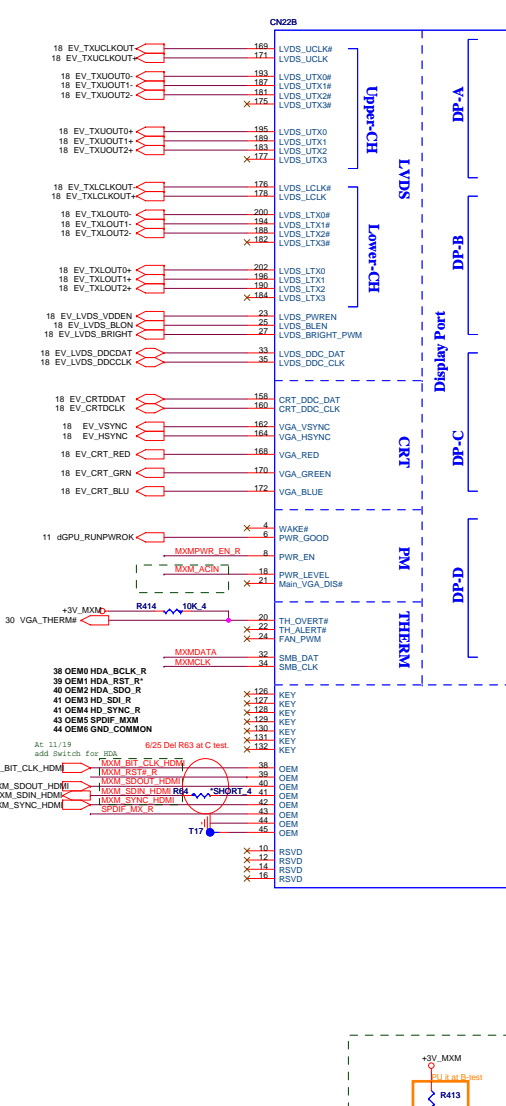
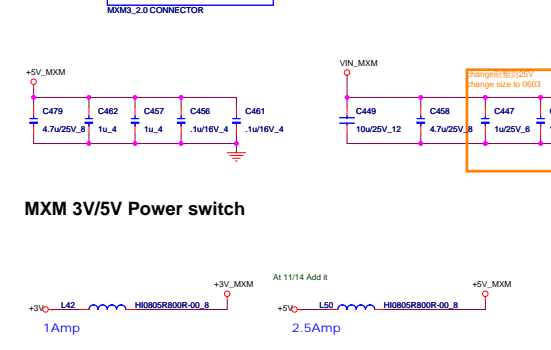
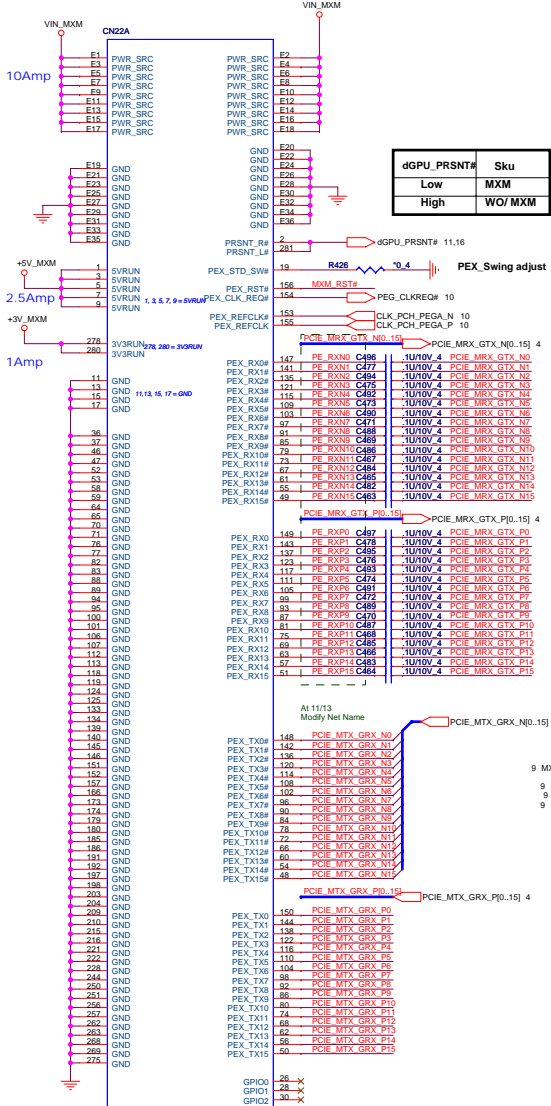
6/19 Reserve M2 component at C test.

6/22 Reserve R809~R816 at C test.



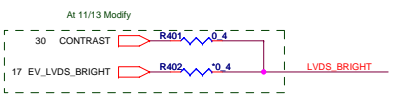
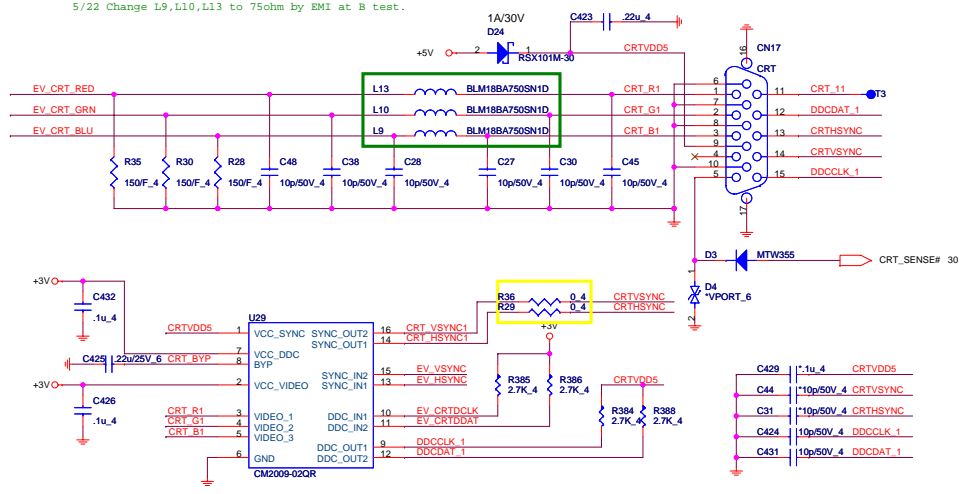
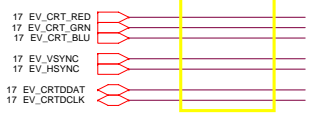
Quanta Computer Inc.
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	DDRIII SO-DIMM-1	3A
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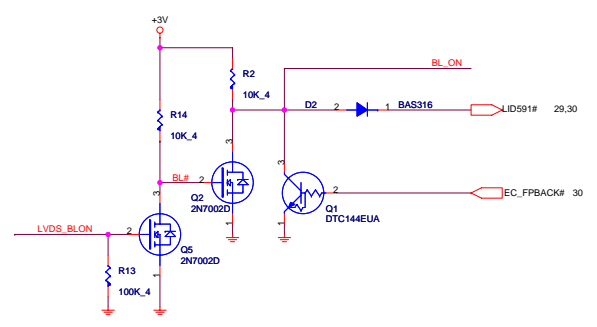
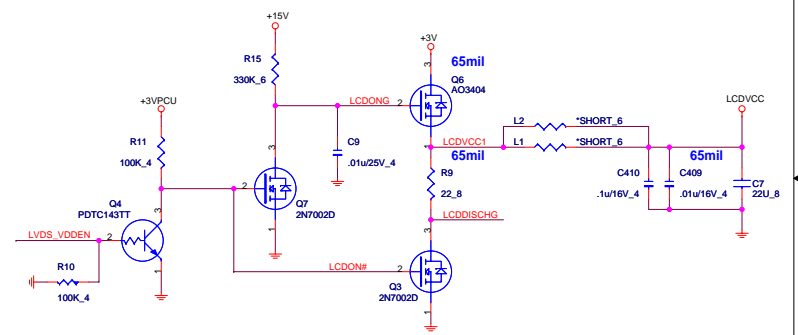
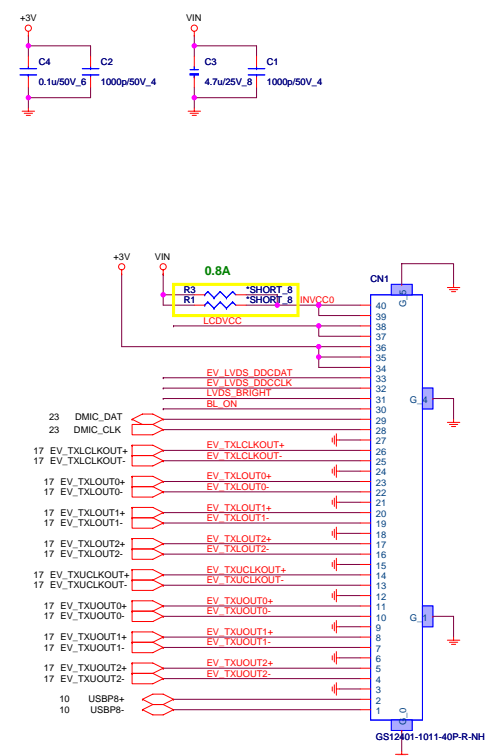
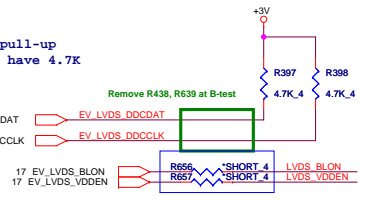


5/22 Change L9, L10, L13 to 75ohm by BMI at B test.

8/12 del R431-R437 at Ramp-test



3/11 NV request I2C pull-up 4.7K, and MXM module have 4.7K pull-up.

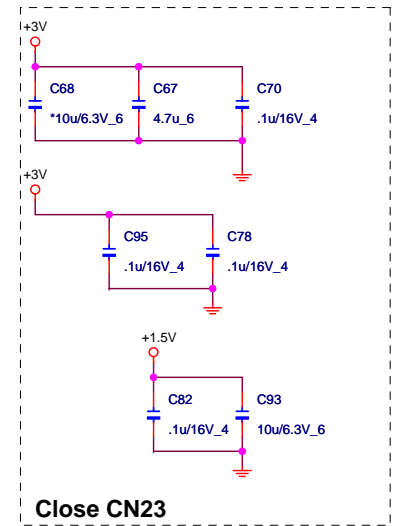
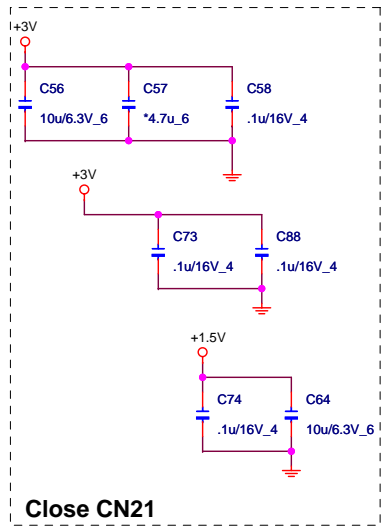
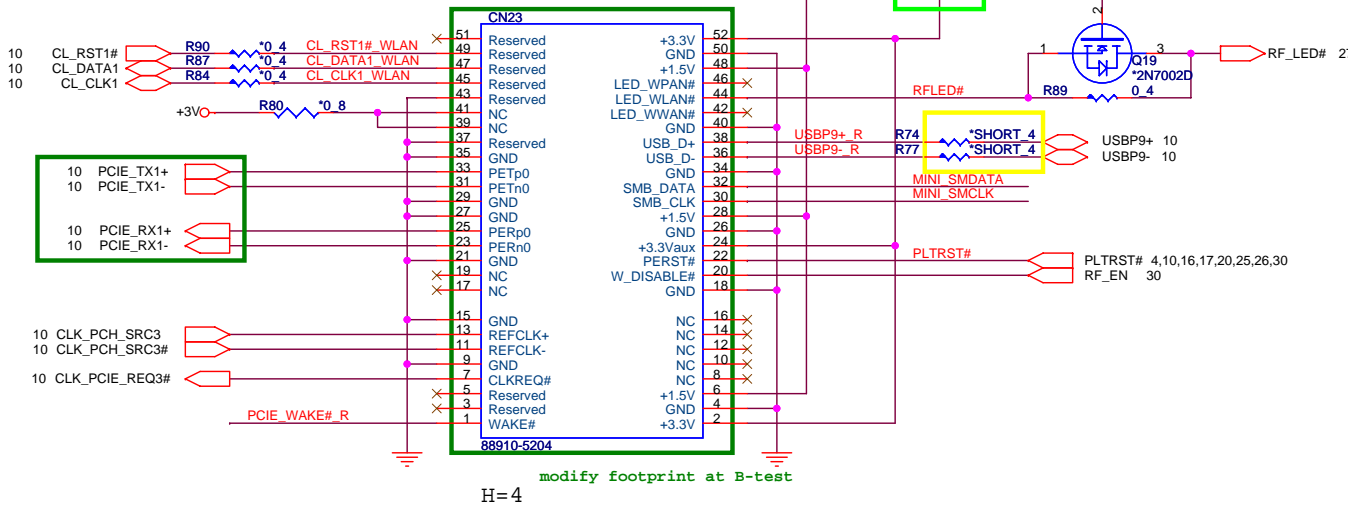


Wireless

Modify to 2Conn. at B-test

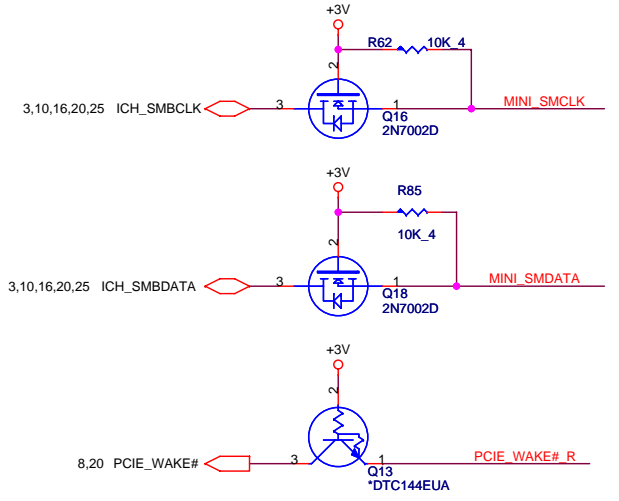
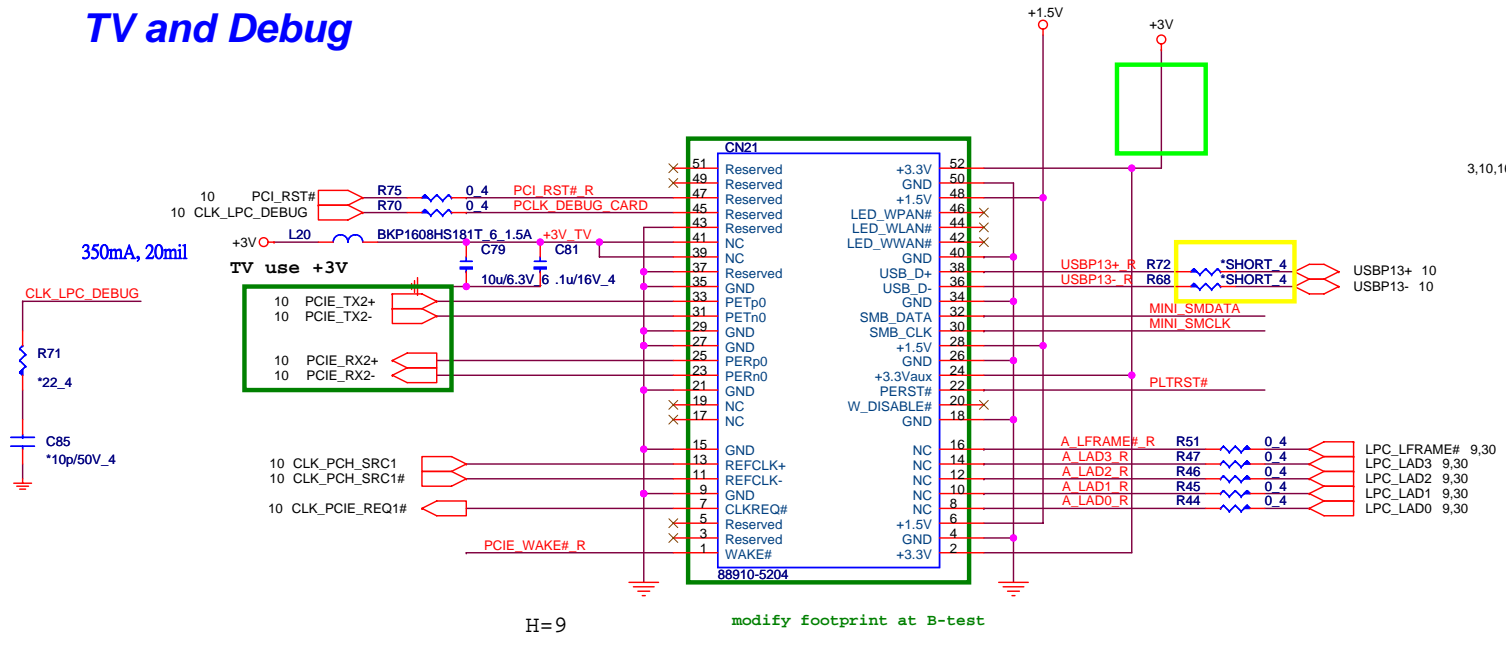
+3.3V: 1000mA
 +3.3Vaux: 330mA
 +1.5V: 500mA

Fotprint : MIPCI-800055FB052GX-52P-LDV-NB4



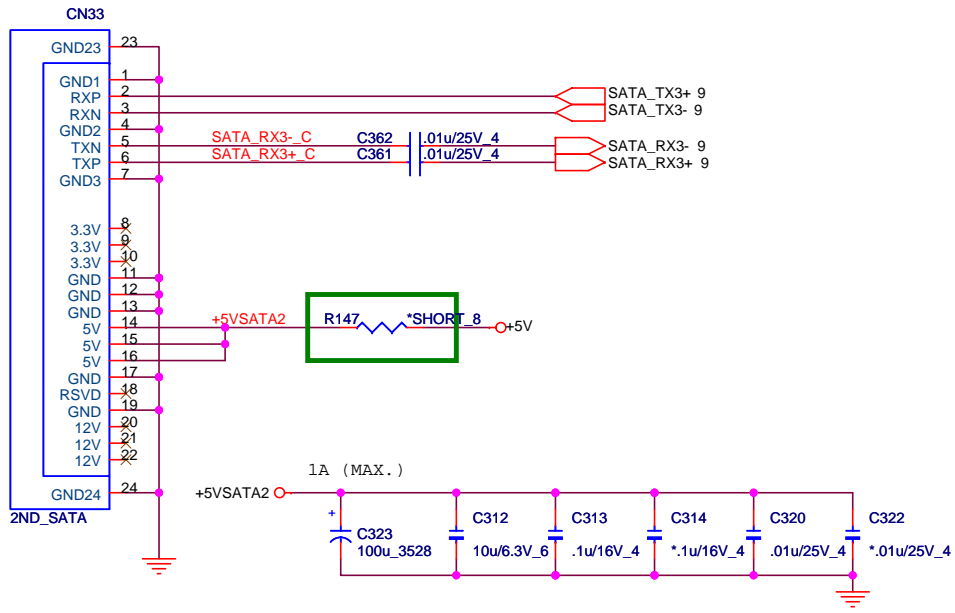
5/14 Change PCIE sequence between CN21 and CN23 by BIOS at B-test.

TV and Debug



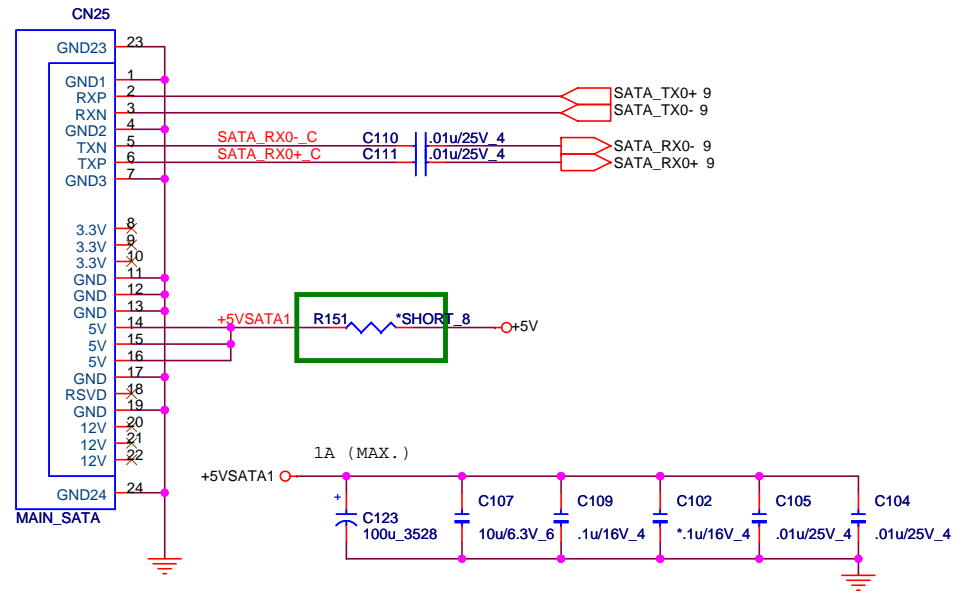
		Quanta Computer Inc.	
		PROJECT : ZY9	
Size	Document Number	MINI PCI-E card/TV	
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			Rev 3A

2nd SATA HDD (edge of board)

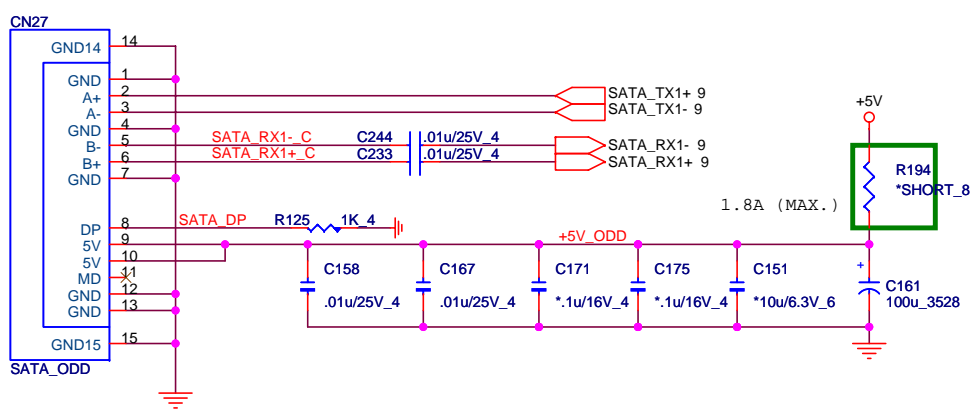


5/13 Add R147,R151,R197 for power consumption measure at B-test.

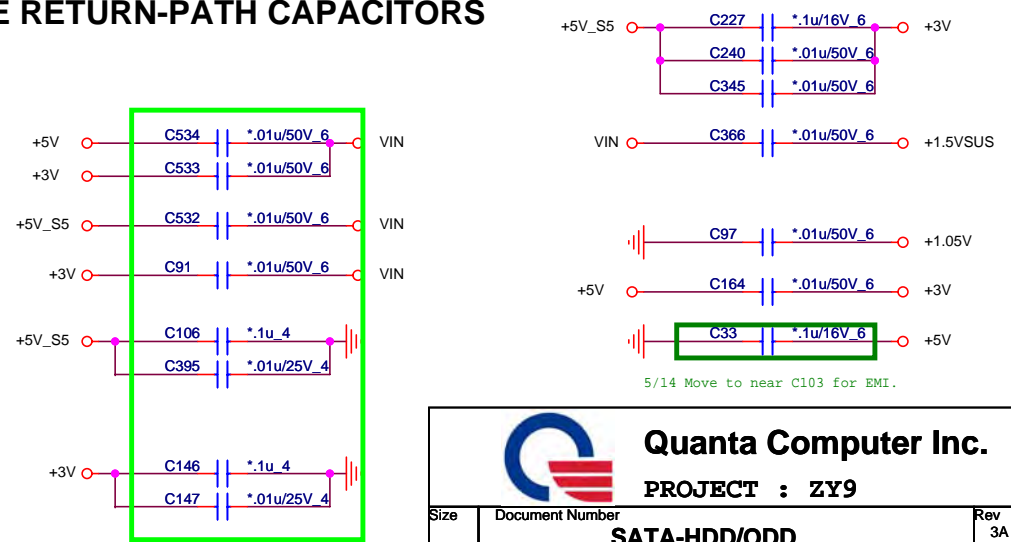
MAIN SATA HDD



ODD (SATA)



EE RETURN-PATH CAPACITORS



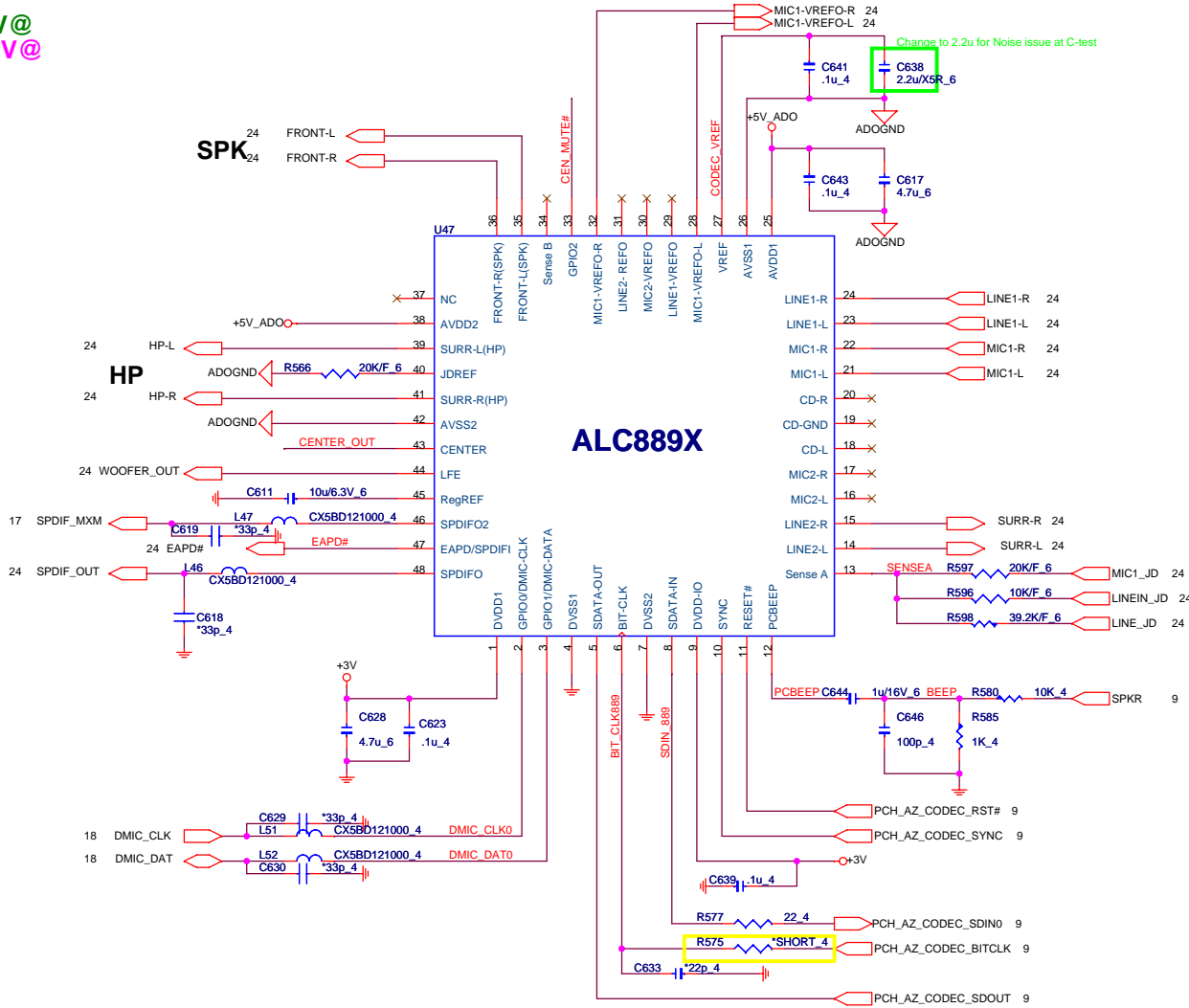
5/14 Move to near C103 for EMI.

Quanta Computer Inc.
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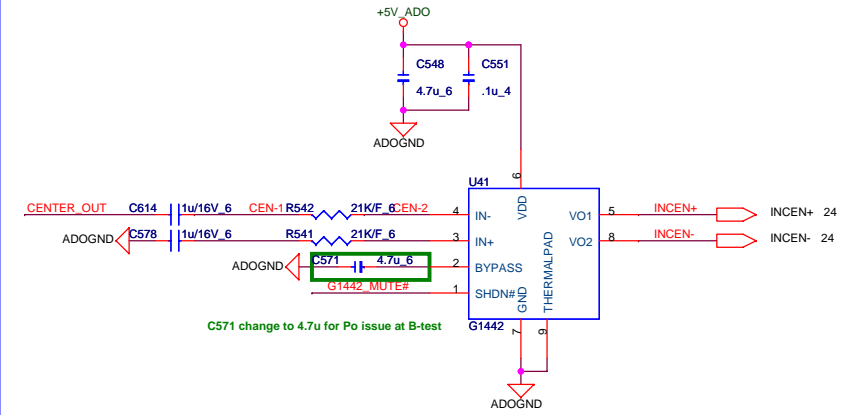
Size	Document Number	Rev
	SATA-HDD/ODD	3A
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CODEC(ALC889X)

IV@
EV@

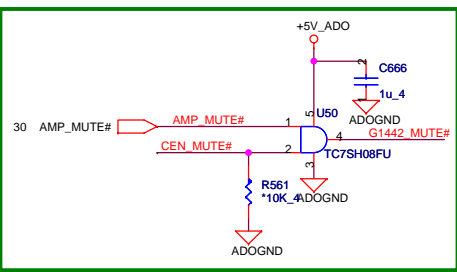


CENTER MONO

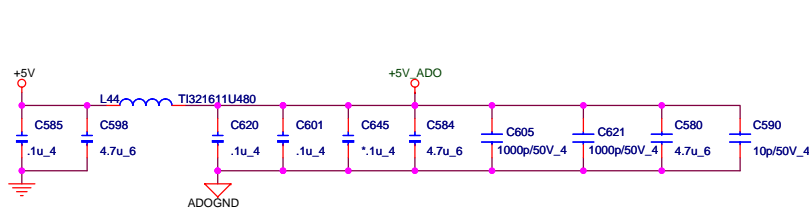


EAPD pin

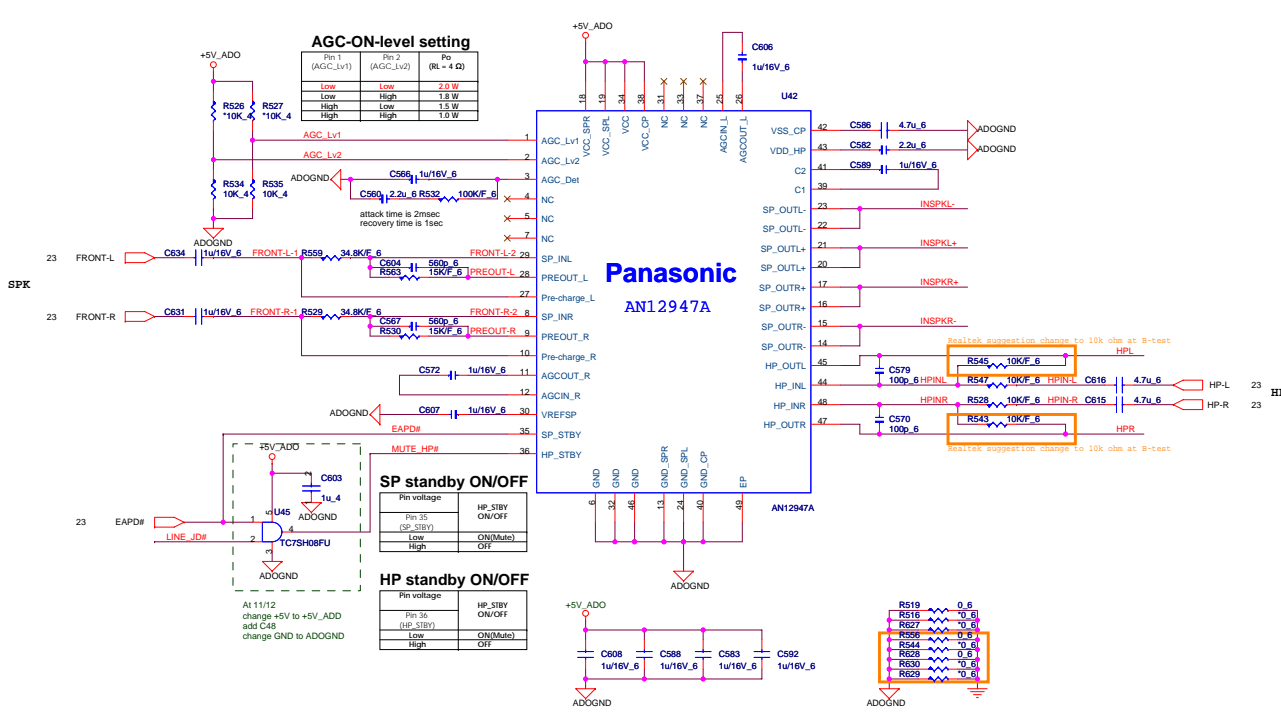
5/11: Add U50, C666 and R561 for Po issue at B-test



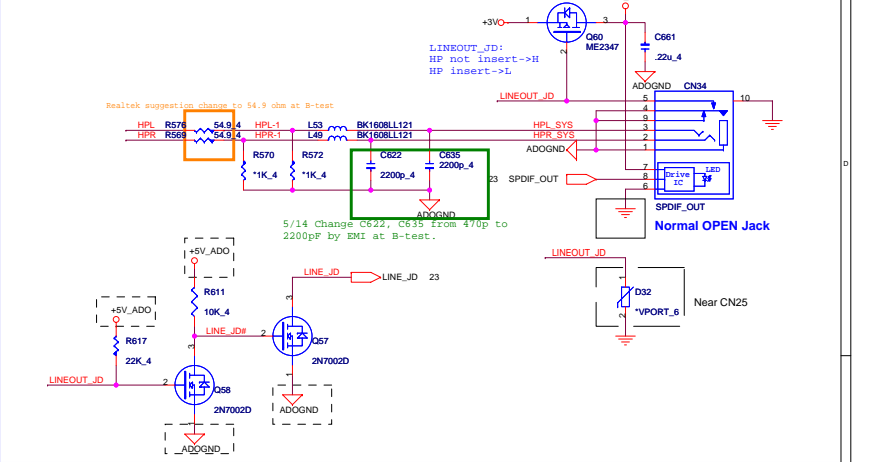
CODEC/AMP Power



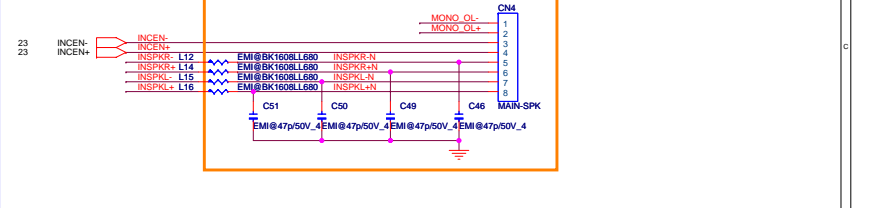
SPEAKER/HP AMP.



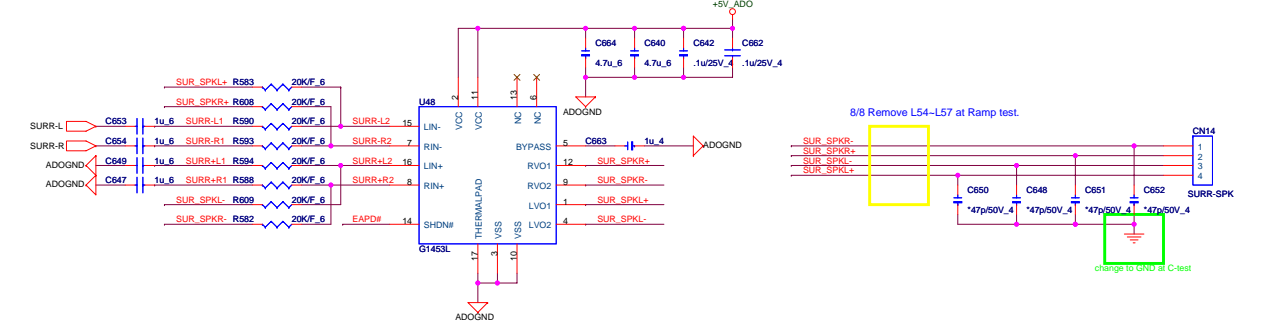
LINE-OUT/SPDIF0



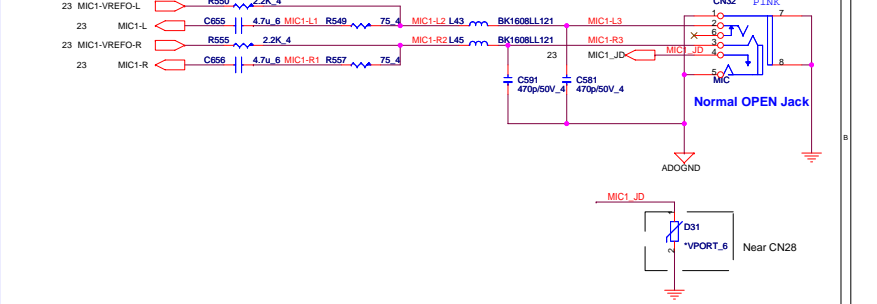
Main SPK/Center/Subwoofer EMI



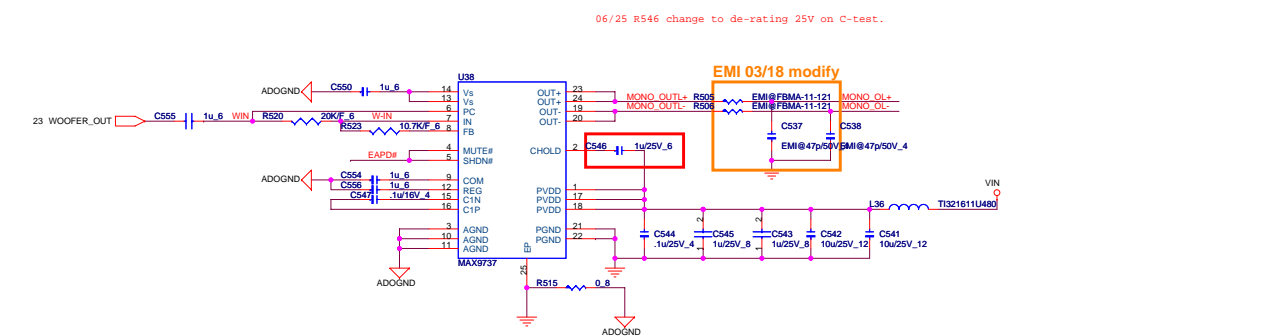
SURR-SPK



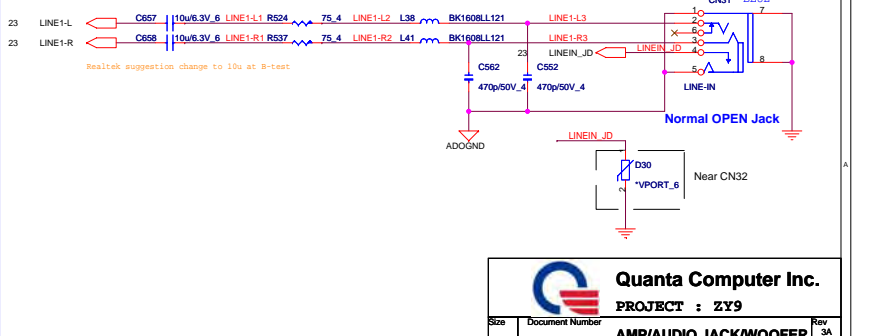
MIC



SUBWOOFER

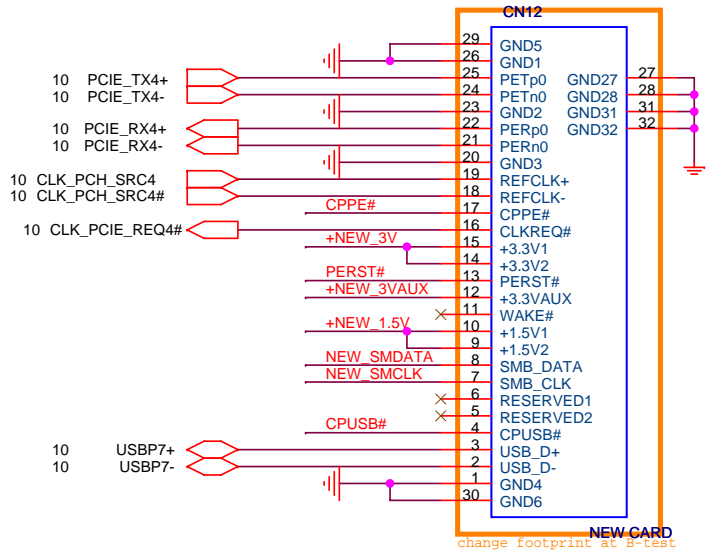


LINE IN



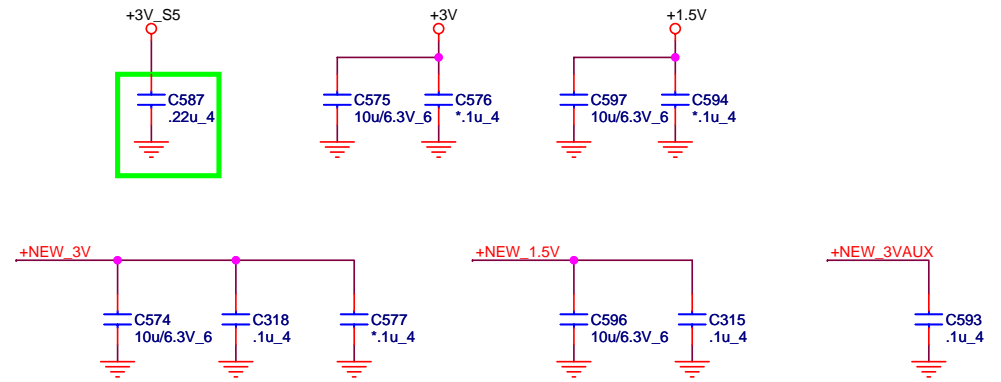
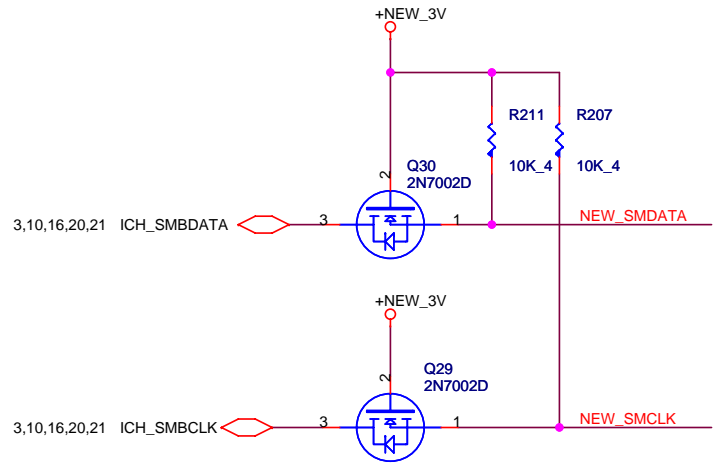
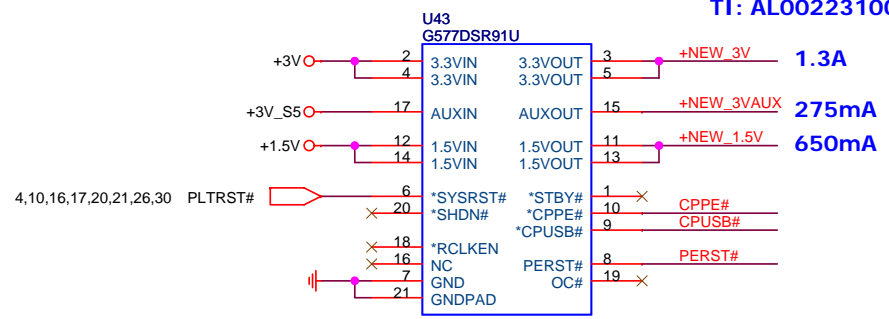
NEW CARD

At 11/18
Change GMT cost down version.



NEW CARD'S POWER SWITCH

GMT: AL000577002
TI: AL002231000

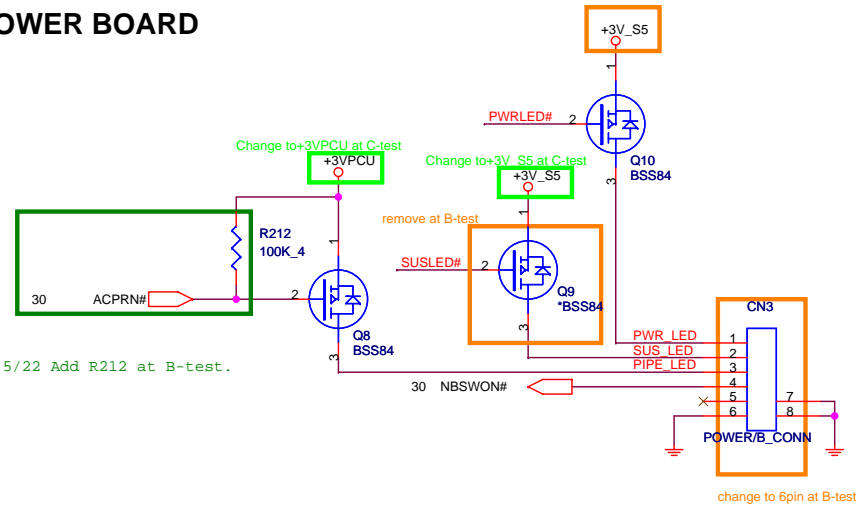


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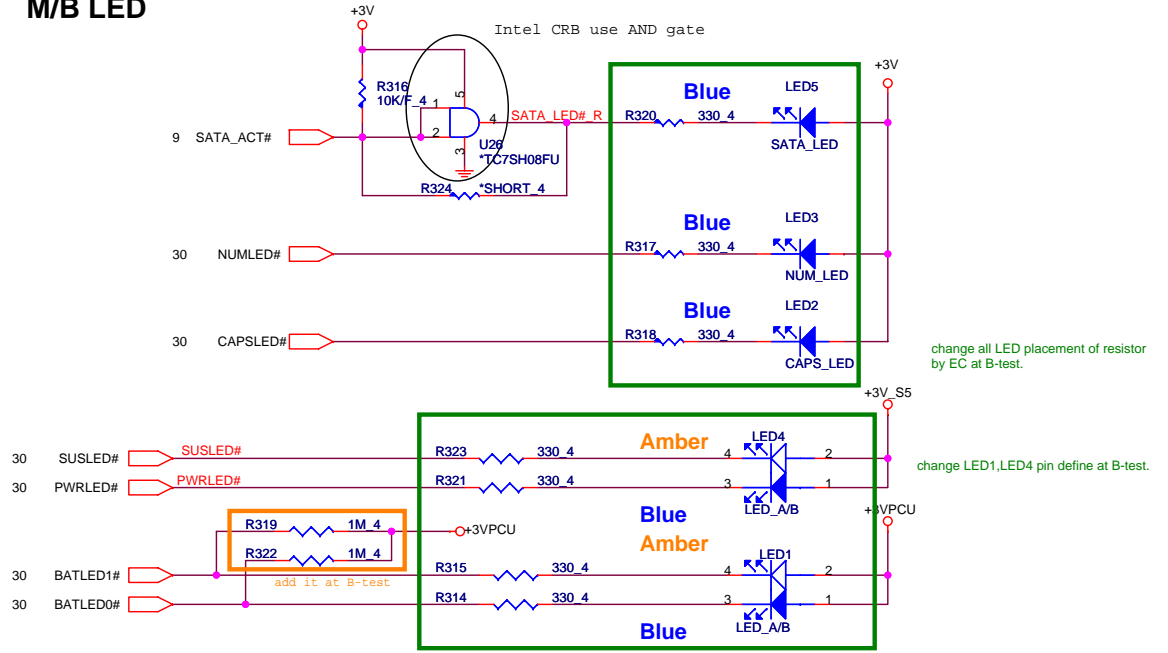
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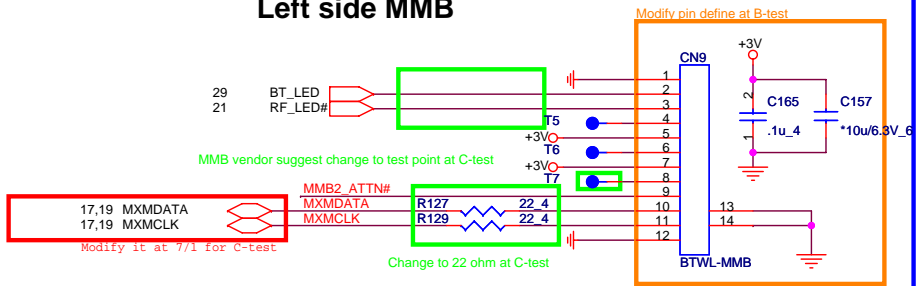
POWER BOARD



M/B LED

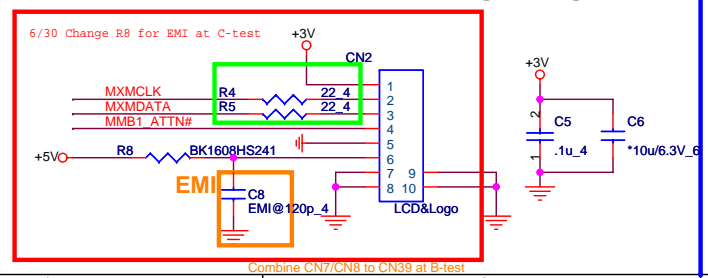


Left side MMB

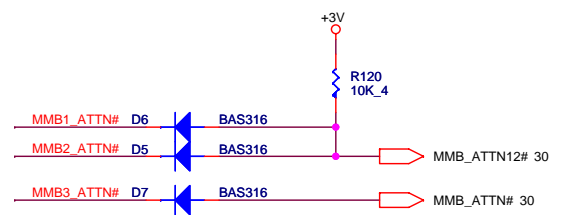


MXMCLK=MXM_SMCLK; MXMDATA=MXM_SMDATA12
 MMB1 and MMB2 need add ISOLATE circuit where are on MXM page.

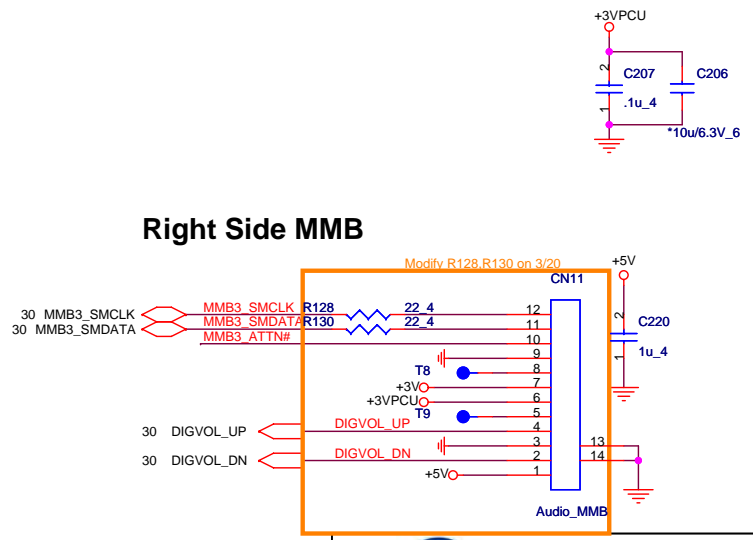
LCD BL_ON/OFF MMB & Backlight Logo LED



MMB Status



Right Side MMB

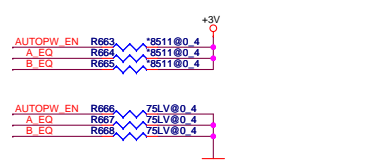
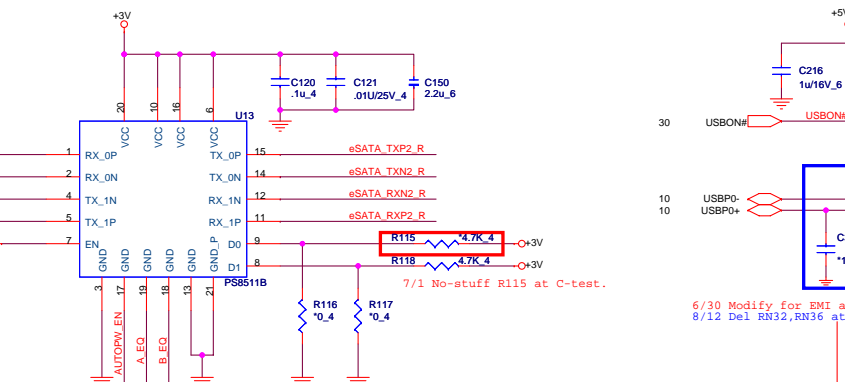


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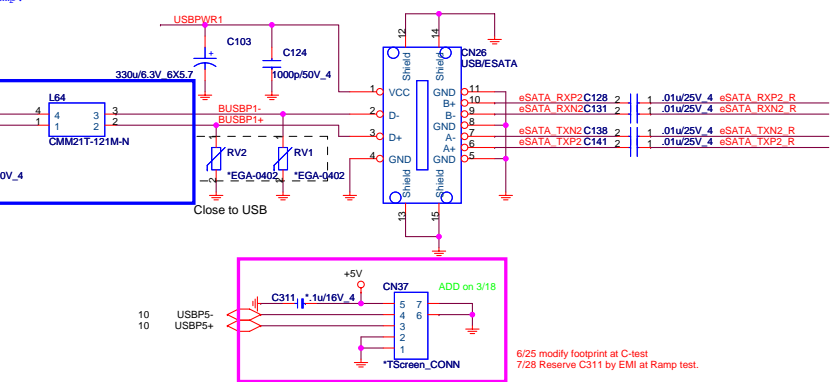
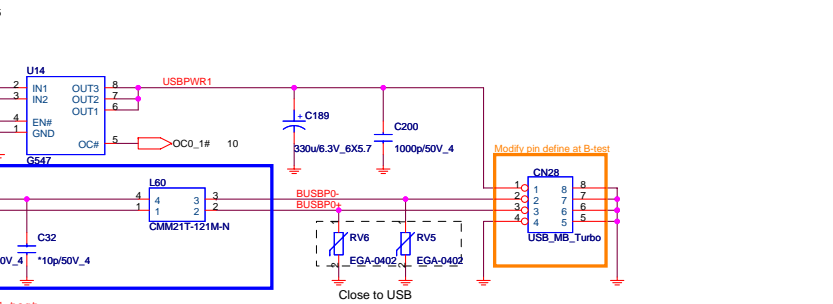
PROJECT : ZY9

Size	Document Number	Rev
	POWER/MMB/LAUNCH/LED	3A
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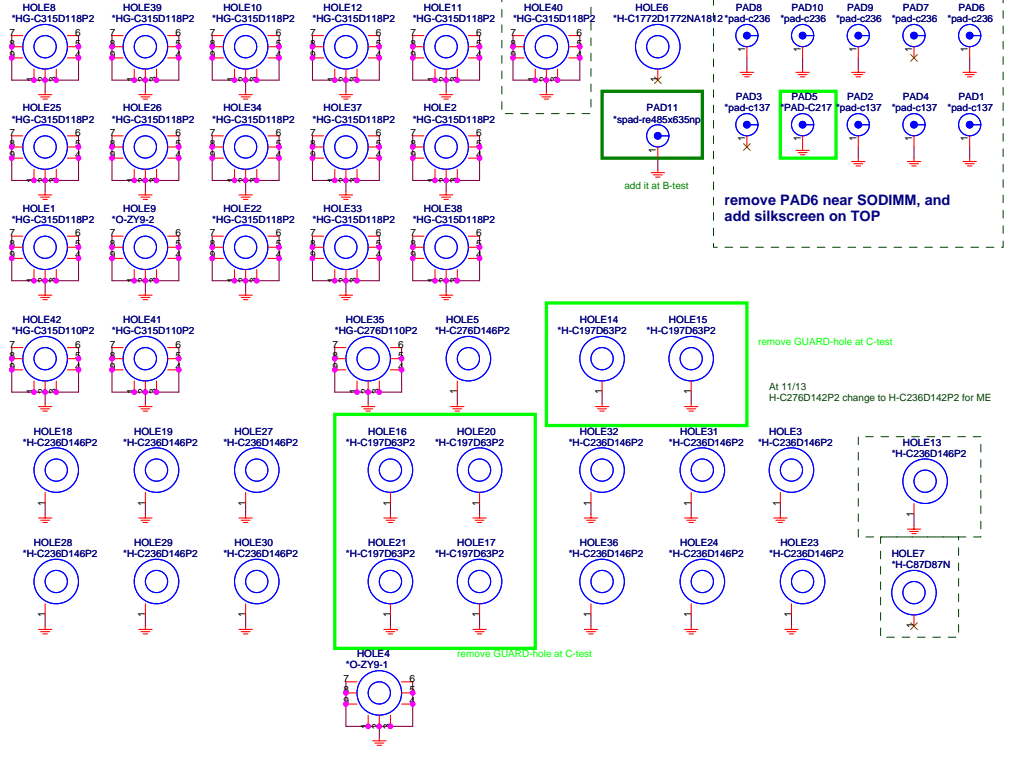
USB & eSATA



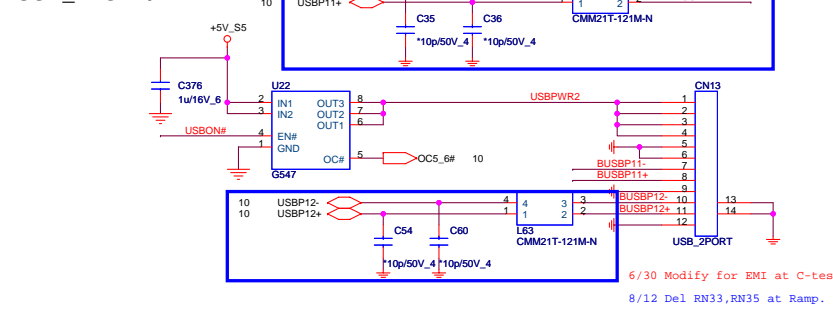
EN	D0	D1	CH-0	CH-1
0	X	X	Standby	Standby
1	0	0	0dB	0dB
1	1	0	Pre-emphasis (5dB)	0dB
1	0	1	0dB	Pre-emphasis (2.5dB)
1	1	1	Pre-emphasis (5dB)	Pre-emphasis (2.5dB)



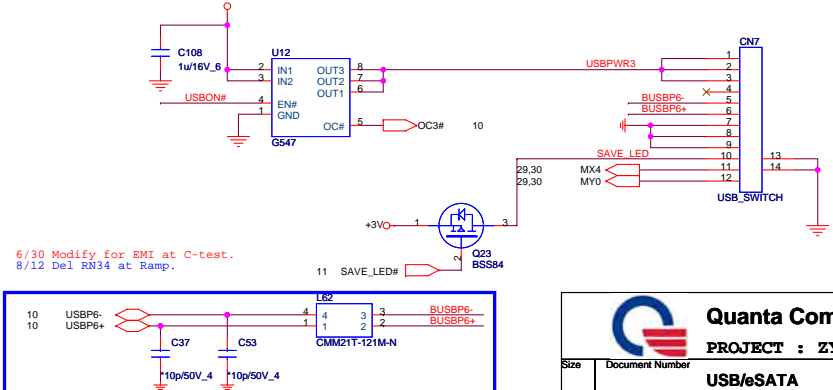
HOLES

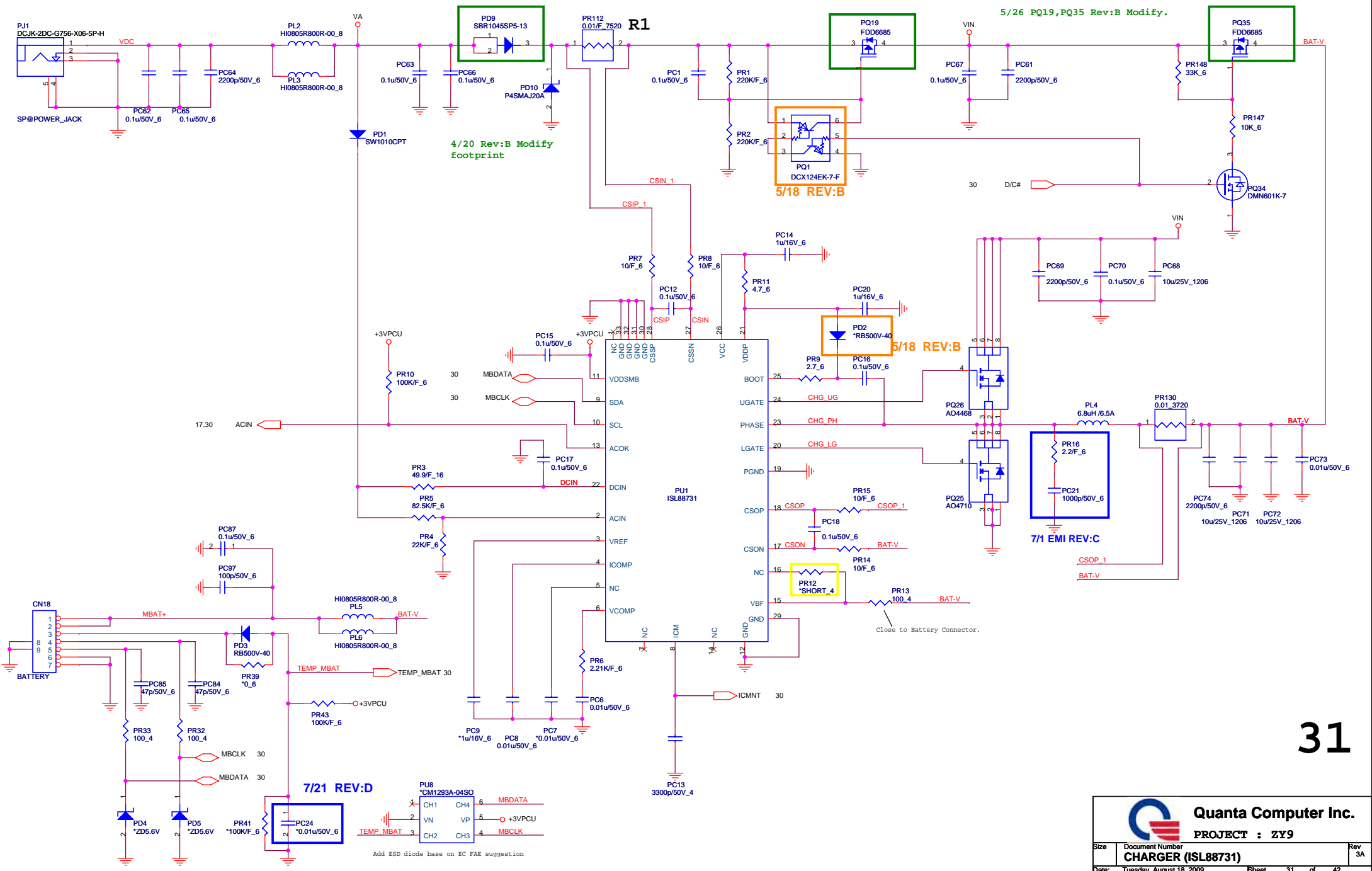


USB_2PORT/B



USB_SWITCH/B



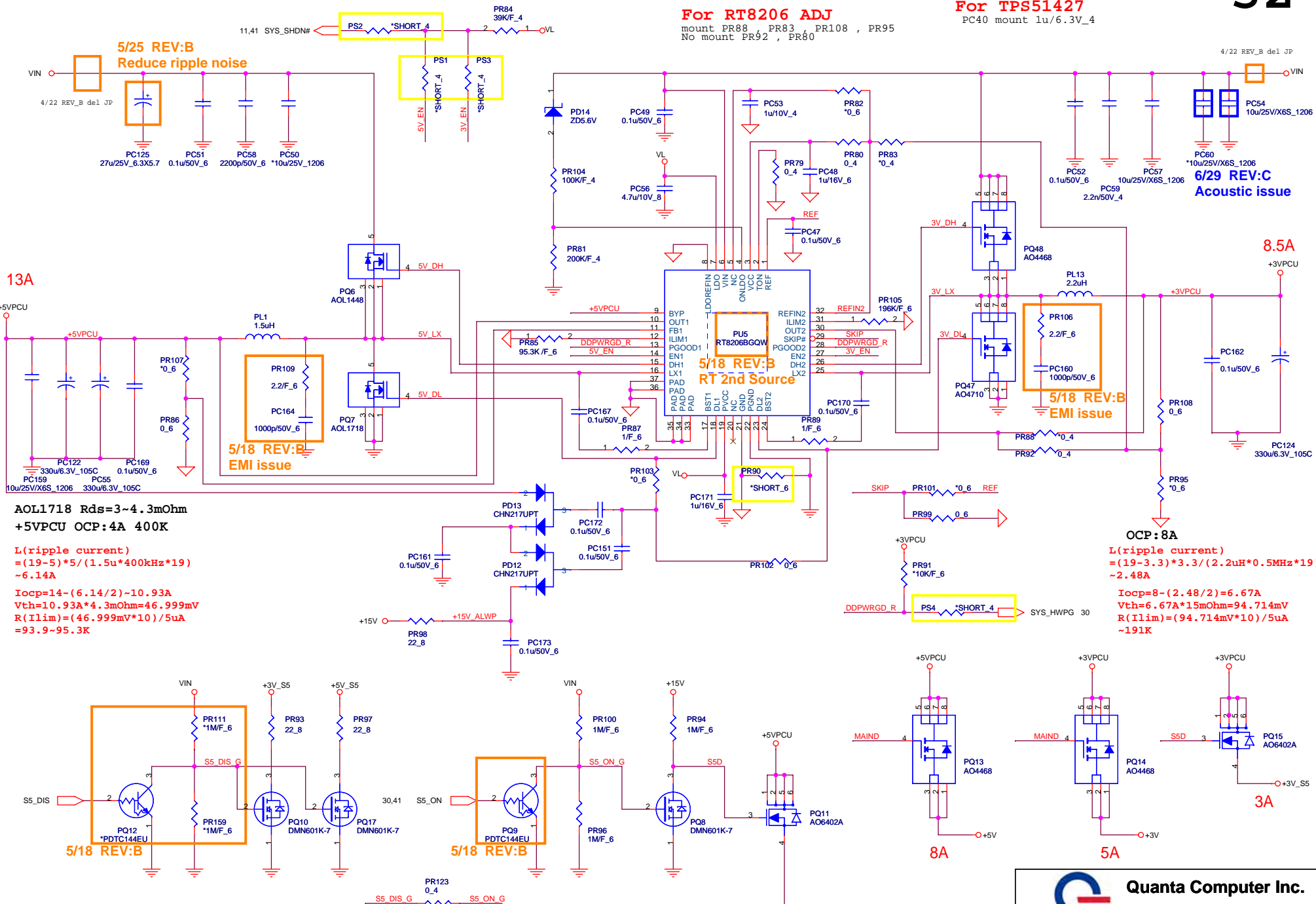


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Size	Document Number	Rev
	CHARGER (ISL88731)	3A
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COMPLEX MARGIN TEST:
For ISL6237 ADJ
 mount PR92, PR80, PR108, PR95
 No mount PR88, PR83
For RT8206 ADJ
 mount PR88, PR83, PR108, PR95
 No mount PR92, PR80

For ISL6237 & RT8206 Fix
 mount PR92, PR108, PR80
 No mount PR88, PR83
For TPS51427
 PC40 mount 1u/6.3V_4



13A

5/18 REV:B EMI issue

5/18 REV:B EMI issue

5/18 REV:B

AOL1718 $R_{ds}=3\sim 4.3\text{m}\Omega$
+5VPCU OCP: 4A 400K

L(ripple current)
 $= (19-5) * 5 / (1.5\mu * 400\text{kHz} * 19)$
 $\sim 6.14\text{A}$

Iocp $= 14 - (6.14 / 2) \sim 10.93\text{A}$
 $V_{th} = 10.93\text{A} * 4.3\text{m}\Omega = 46.999\text{mV}$
 $R(I_{lim}) = (46.999\text{mV} * 10) / 5\mu\text{A}$
 $= 93.9 \sim 95.3\text{K}$

OCP: 8A

L(ripple current)
 $= (19-3.3) * 3.3 / (2.2\mu\text{H} * 0.5\text{MHz} * 19)$
 $\sim 2.48\text{A}$

Iocp $= 8 - (2.48 / 2) = 6.67\text{A}$
 $V_{th} = 6.67\text{A} * 15\text{m}\Omega = 94.714\text{mV}$
 $R(I_{lim}) = (94.714\text{mV} * 10) / 5\mu\text{A}$
 $\sim 191\text{K}$

5/25 stuff PR123, no stuff PQ12, PR111, PR159 at B test.

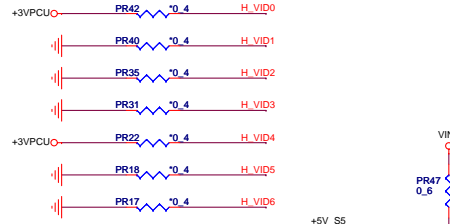
3.75A

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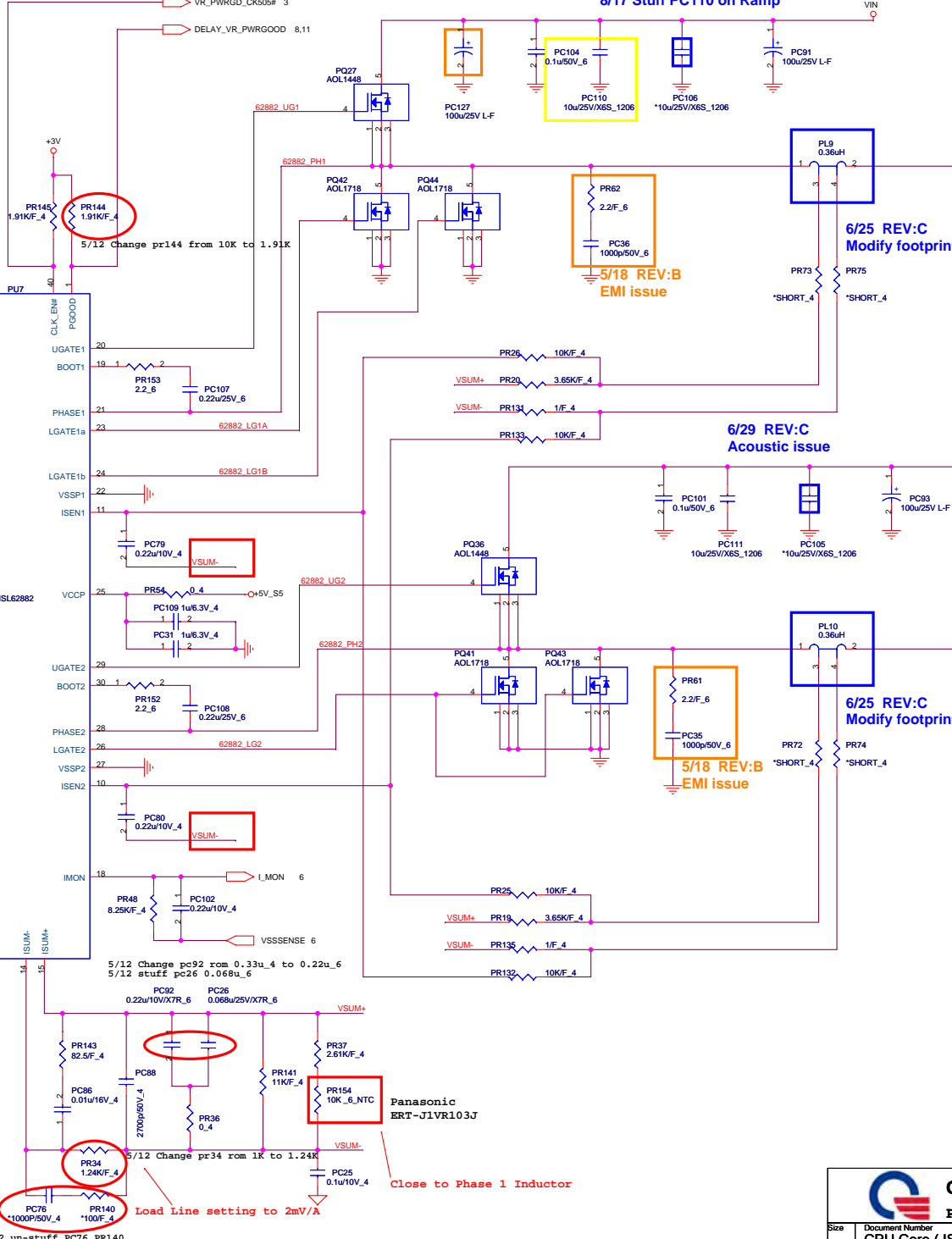
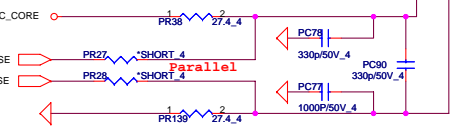
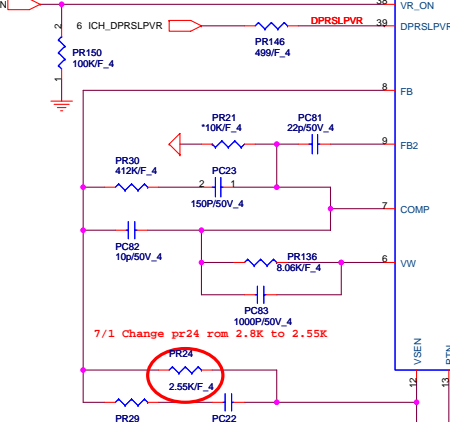
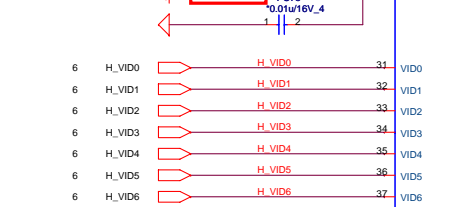
Size	Document Number	Rev
	SYSTEM 5V/3V (ISL6237)	3A
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5/25 REV:B Reduce ripple noise
6/29 REV:C Acoustic issue.
8/17 Stuff PC110 on Ramp

VID 1.2875V



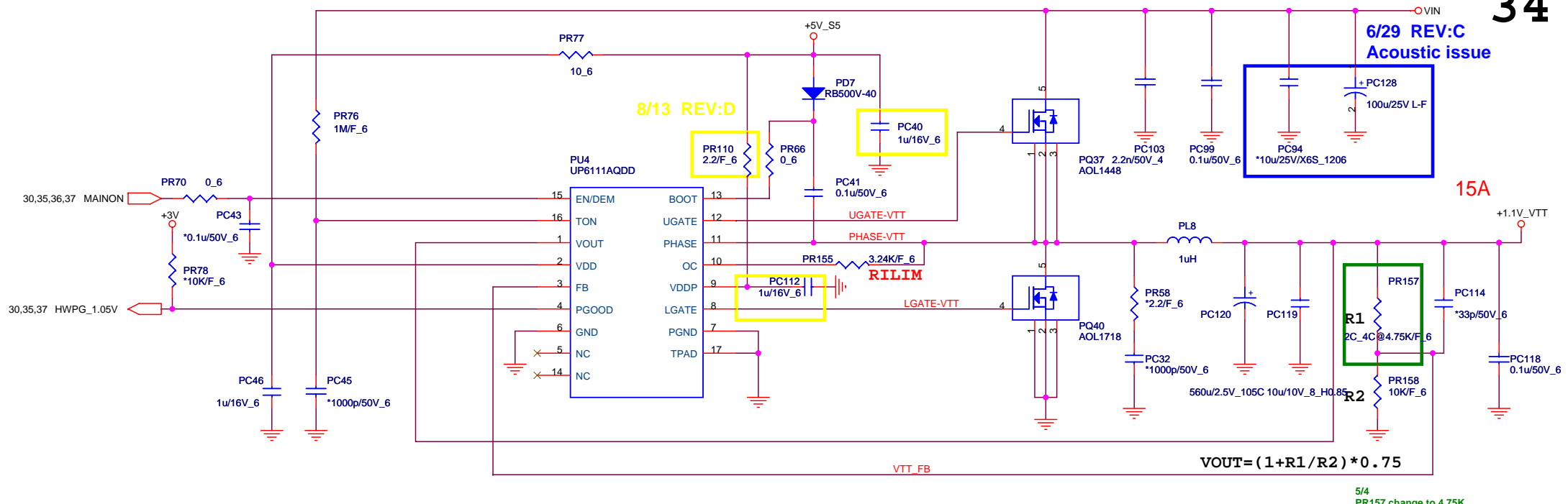
Close to Phase 1 Inductor



36A

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Size	Document Number	Rev
	CPU Core (ISL62882)	3A
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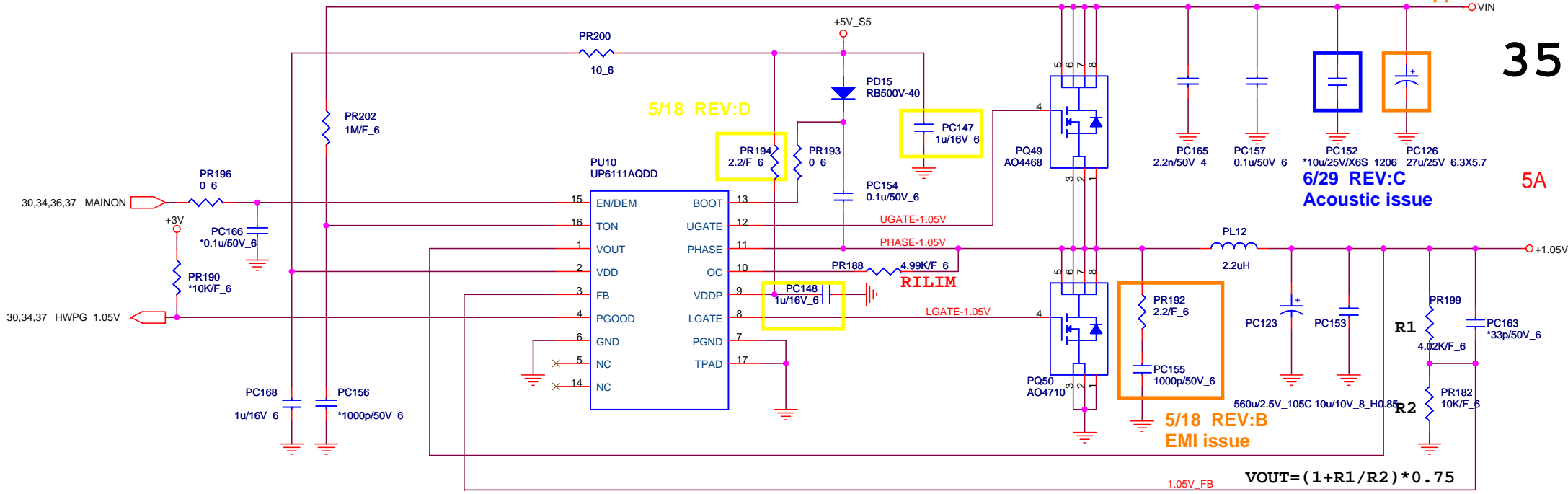
AO1718 Rdson=3~4.3mOhm

Aurbundale (1.05V) R1 = 4.02K (CS24023F928)
 Clarksfield(1.1V) R1 = 4.75K (CS24753F919)

L(ripple current)
 = (19-1.05)*1.05/(1u*272k*19)
 ~3.64A
 4.3m*15=RILIM*20uA
 RILIM=3.24K (3.22K)

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		3A
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	+VTT (UP6111A)	Tuesday, August 18, 2009
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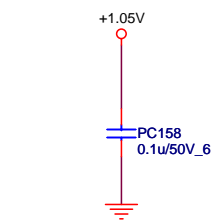
[PWM]



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5A

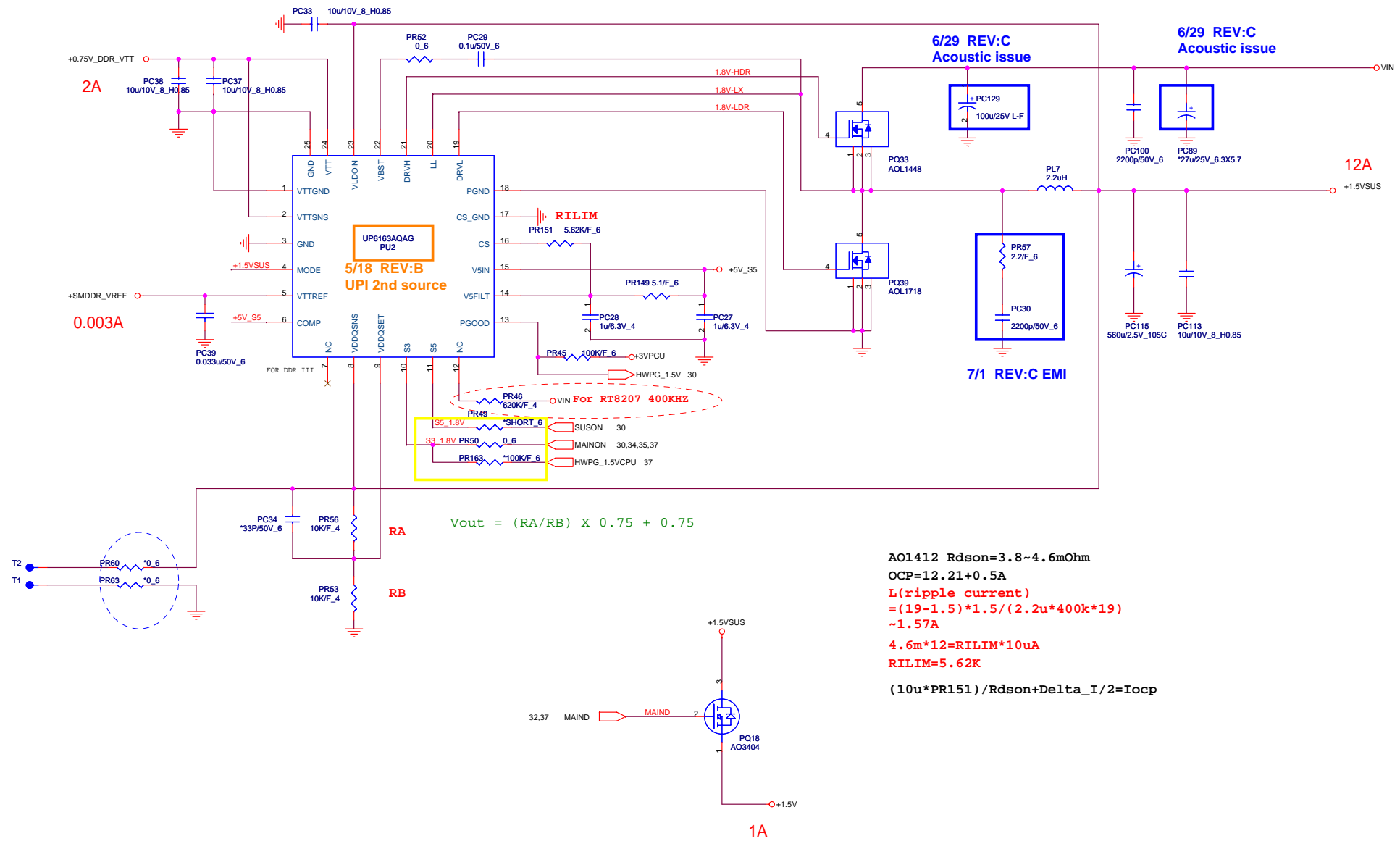
AO4710 $R_{dson}=11.8\sim 14.2m\Omega$
 OCP=7.2-0.8A
 $L(\text{ripple current})$
 $= (19-1.05) * 1.05 / (2.2\mu * 272k * 19)$
 $\sim 1.6577A$
 $14.2m * 7 = RILIM * 20\mu A$
 $RILIM = 4.99K (4.97K)$



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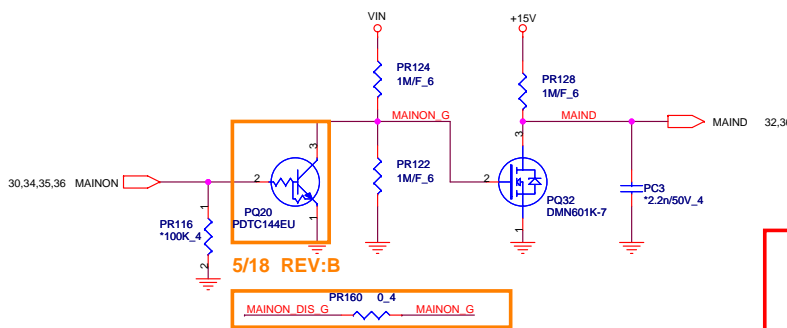
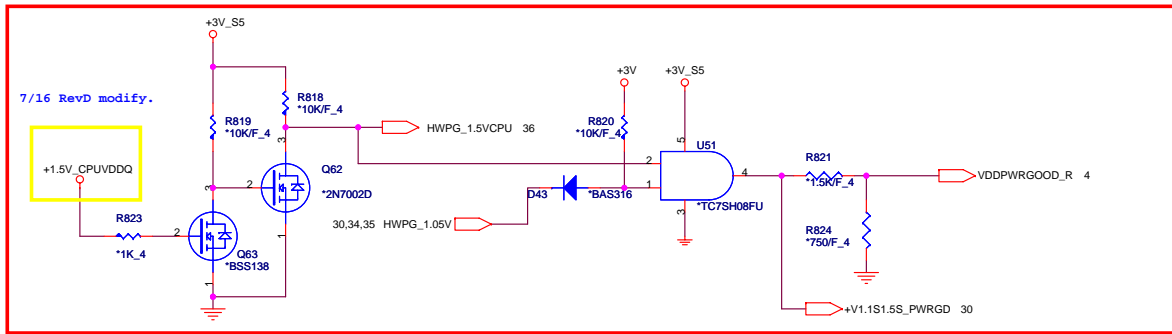
Size	Document Number	Rev
	+1.05V(UP6111AQDD)	3A
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[PWM]

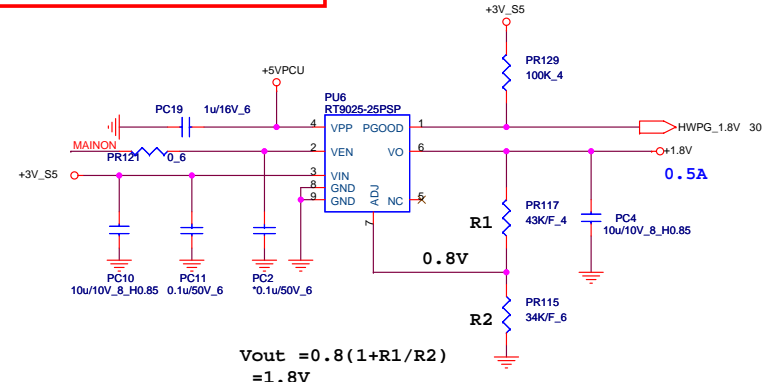
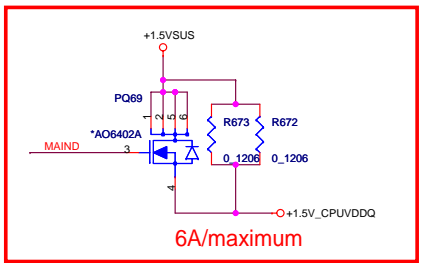


$$V_{out} = (RA/RB) \times 0.75 + 0.75$$

AO1412 $R_{dson} = 3.8 \sim 4.6 m\Omega$
 $OCP = 12.21 + 0.5A$
 $L(\text{ripple current}) = (19 - 1.5) \times 1.5 / (2.2u \times 400k \times 19) \sim 1.57A$
 $4.6m \times 12 = RILIM \times 10uA$
 $RILIM = 5.62K$
 $(10u \times PR151) / R_{dson} + \Delta I / 2 = I_{ocp}$

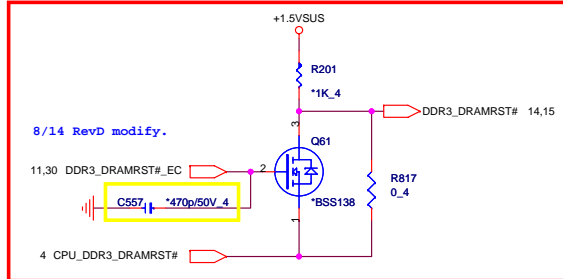
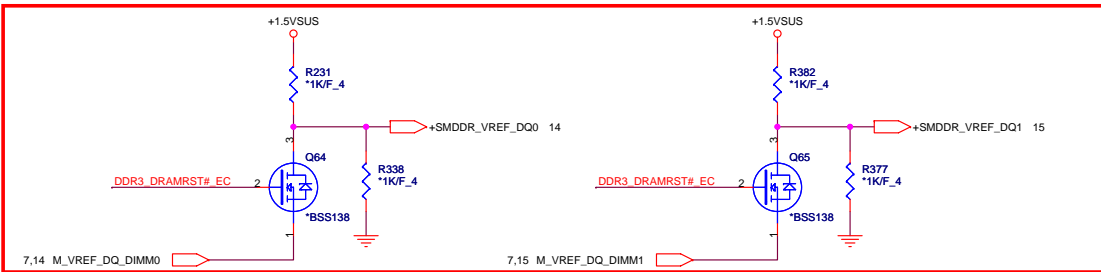
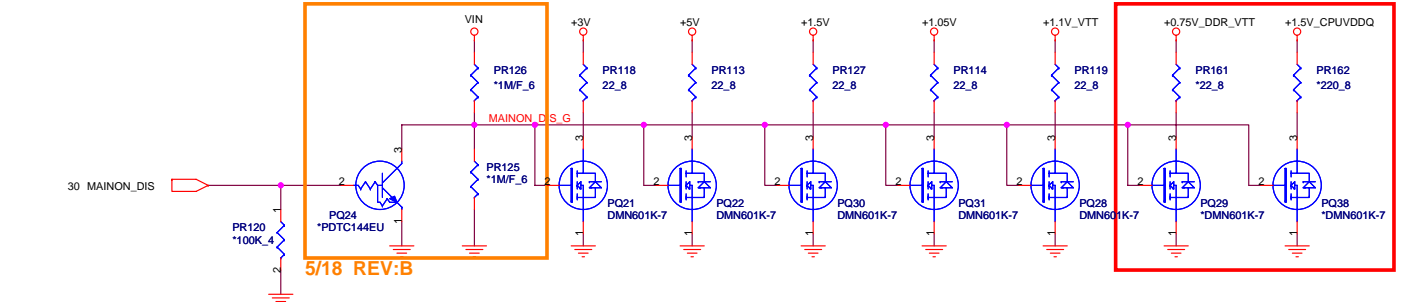
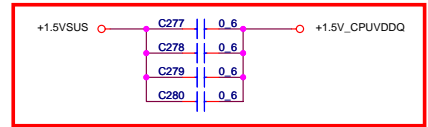


5/18 REV:B
 5/25 stuff PR160, no stuff PQ24, PR126, PR125 at B test.

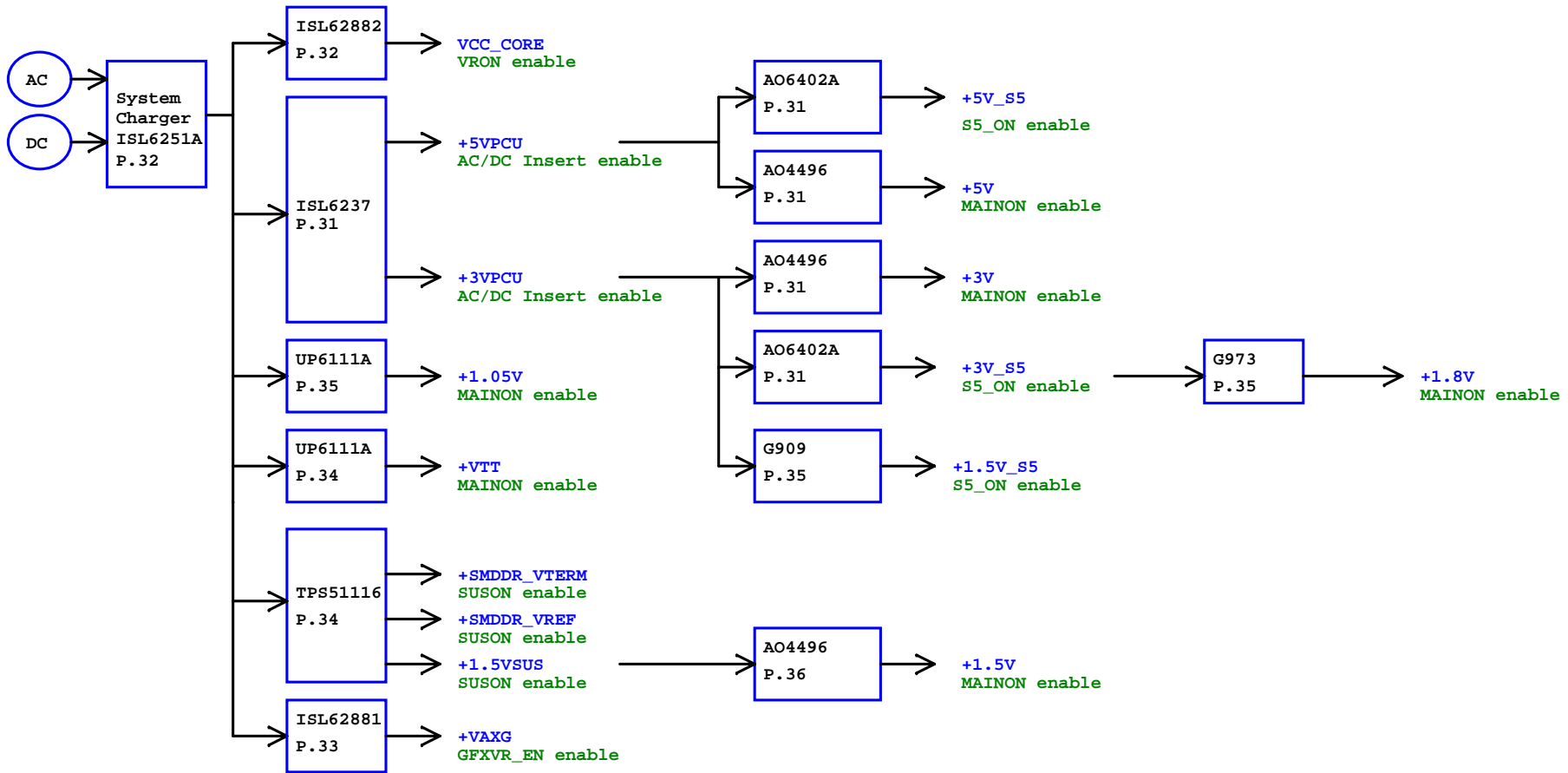


$$V_{out} = 0.8(1 + R1/R2) = 1.8V$$

S3 power solution: C277-C280 stuff 0.1uF cap; Normal : Stuff 0ohm to short.



- 12,21,25,36 +1.5V
- 6 +1.5V_CPUVDDQ



Power Distribution List

Power	Distribution
VCC_CORE	CPU
+5VPCU	ICH8M, RJ45/USB /B, USB/eSATA, Satellite LED, CIR
+3VPCU	RTC, HALL SENSOR, KB, TP/FP/LED /B, Power /B, Kill SW, EC, ID, SPI Flash, CIR
+1.5V	CPU, GMCH, ICH9M, Mini Card, New Card
+1.5VSUS	GMCH, DDR
+SMDDR_VREF	GMCH, DDR
+SMDDR_VTERM	DDR
+1.05V	CPU, CLK, Thermal Trip, GMCH, ICH8M
+5V_S5	ICH8M, G-SENSOR, Felica, USB/eSATA
+5V	CPU, ICH8M, VGA, Camera, CRT, HDMI, SATA HDD, PATA ODD, PCMCIA, TP/FP/LED /B, EC, Speaker, Headphone
+3V	CLK, CPU Thermal Monitor, FAN, GMCH, DDR, ICH8M, VGA, LCD/LED Panel, HALL SENSOR, CRT, HDMI, SATA HDD, PATA ODD, PCMCIA, Mini Card, KB, TP/FP/LED /B, RJ45/USB /B, Bluetooth, MMB, New Card, PC BEEP, EC, Codec (CX20561), VR, Headphone, MDC, Cardreader (OZ129T)
+3V_S5	ICH8M, Mini Card, RJ45/USB /B, New Card
+3VSUS	ICH8M, FP
+1.8V	HDMI, Cardreader (OZ129T)
+1.25V	CLK, GMCH, ICH8M

PCH POWER PLANE

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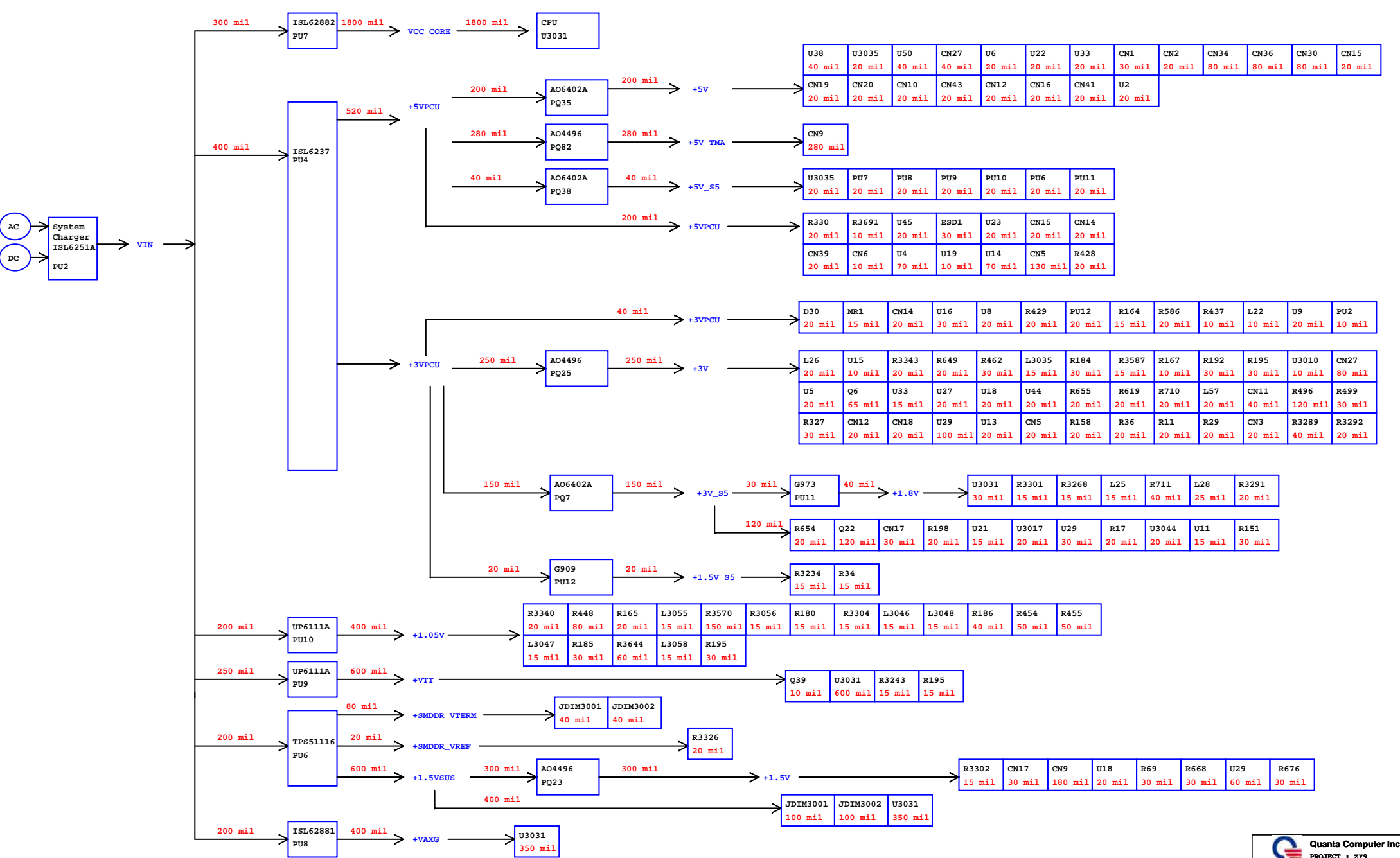
LOGIC	SUPPLY	LEVEL	S0	S3	S4	S5
Fast Flash	VccpNAND	+1.8V/+3.3V	ON	OFF	OFF	OFF
Core	DcpSusByp	+1.05V	ON	OFF	OFF	OFF
CPU	V_CPU_IO	+VTT	ON	OFF	OFF	OFF
PCI	V5REF	+5V/+3V	ON	OFF	OFF	OFF
USB	V5REF_Sus	+5V_S5/+3V_S5	ON	ON	ON	ON
DisplayPort, SATA, PCI	VCC3_3	+3V	ON	OFF	OFF	OFF
Core	VccCore	+1.05V	ON	OFF	OFF	OFF
PCIE/DMI	VccDMI	+VTT/+1.05V	ON	OFF	OFF	OFF
Fast Flash	VccME3_3	+3V	ON	OFF	OFF	OFF
PCIE/DMI,SATA,USB	VccIO	+1.05V	ON	OFF	OFF	OFF
Core	VccLAN	+1.05V	ON	OFF	OFF	OFF
Core	VccME	+1.05V	ON	OFF	OFF	OFF
RTC	VccRTC	+VCCRTC	ON	ON	ON	ON
USB&PCI	VccSus3_3	+3V_S5	ON	ON	ON	ON
IntelR HD Audio	VccSusHDA	+1.5V_S5	ON	ON	ON	ON
Core	VccVRM	+V1.5S_1.8S	ON	OFF	OFF	OFF
CLK	VccAClk	+1.05V	ON	OFF	OFF	OFF
CRT	VccADAC	+3V	ON	OFF	OFF	OFF
DPLL	VccADPLLA	+1.05V	ON	OFF	OFF	OFF
DPLL	VccADPLLB	+1.05V	ON	OFF	OFF	OFF
PCie/DMI	VccapIEXP	+1.05V	ON	OFF	OFF	OFF
IntelR FDI	VccFDIPLL	+1.05V	ON	OFF	OFF	OFF
SATA	VccSATAPLL	+1.05V	ON	OFF	OFF	OFF
Display	VccTX_LVDS	+1.8V	ON	OFF	OFF	OFF

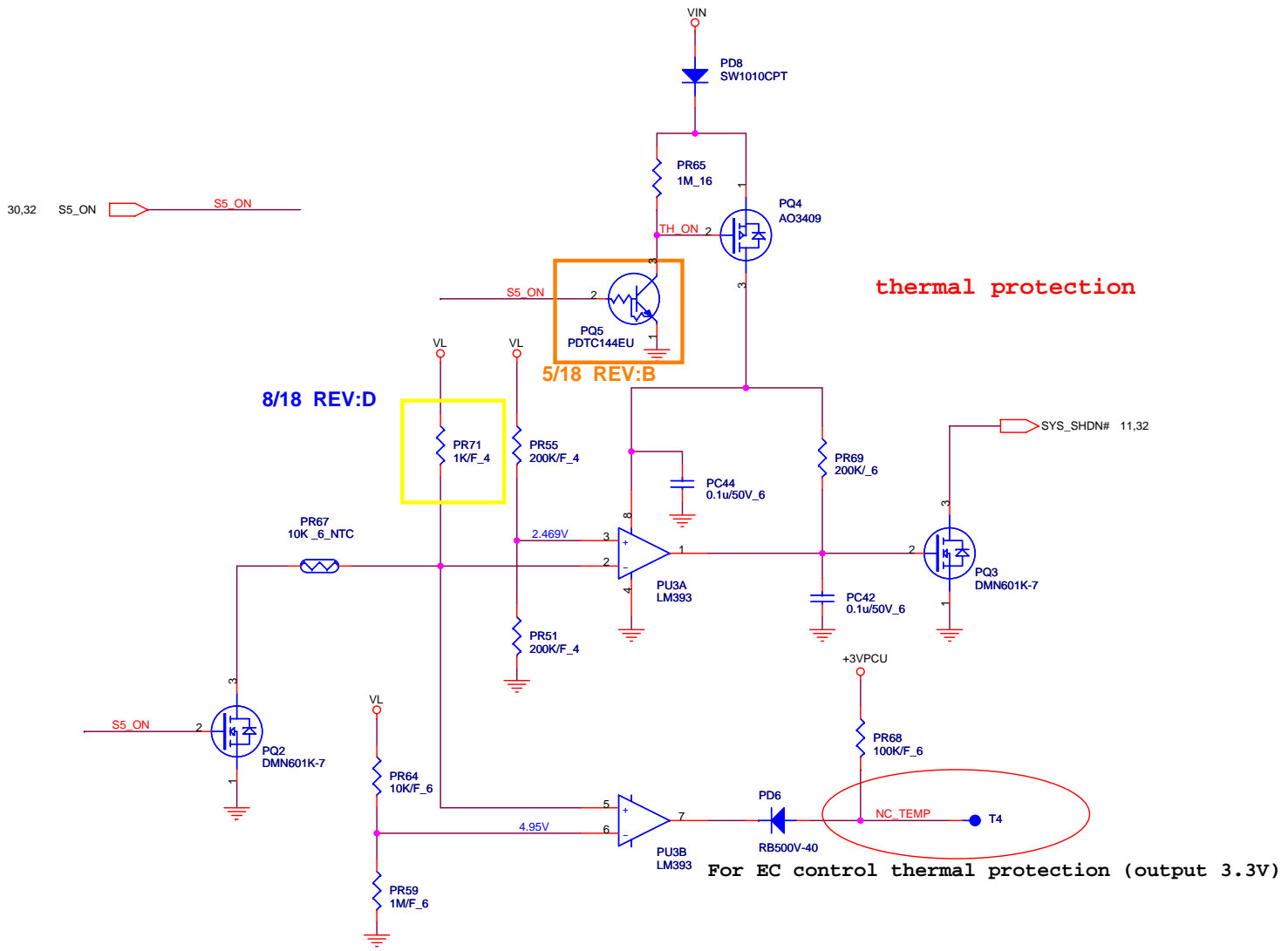


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thermal protection

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Thermal Protection		
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