

# Compal Confidential

## ICW50 Schematics Document

AMD Turion/Sempron + Nvidia MCP67-MV

2007 / 04 / 20

Rev:1.0

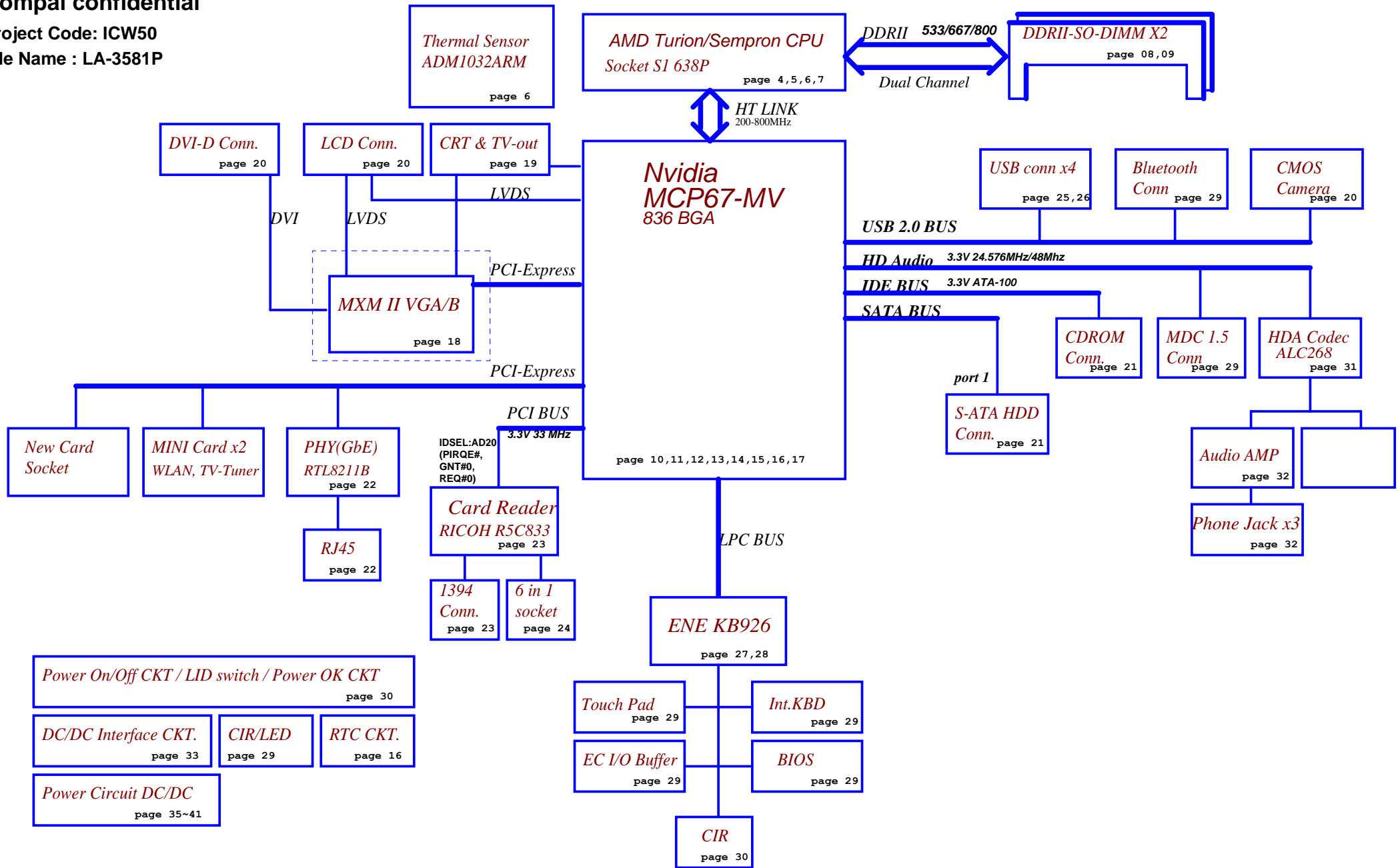
FOR Pre-MP

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Issued Date	2006/08/18	Deciphered Date	2007/8/18	Title	Cover Sheet
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**Compal confidential**

Project Code: ICW50

File Name : LA-3581P



Security Classification		Compal Secret Data		Title	
Issued Date	2006/08/18	Deciphered Date	2007/8/18	BLOCK DIAGRAM	
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## Voltage Rails

Power Plane	Description	S1	S3	S5
VIN	Adapter power supply (19V)	N/A	N/A	N/A
B+	AC or battery power rail for power circuit.	N/A	N/A	N/A
+CPU_CORE	Core voltage for CPU	ON	OFF	OFF
+0.9V	0.9V switched power rail for DDR terminator	ON	ON	OFF
+1.5VS	1.5V switched power rail	ON	OFF	OFF
+1.2VALW	1.2V always on power rail	ON	ON	ON*
+1.2VS	1.2V switched power rail	ON	OFF	OFF
+1.2V_HT	1.2V switched power rail	ON	OFF	OFF
+1.8V	1.8V power rail for DDR	ON	ON	OFF
+1.8VS	1.8V switched power rail	ON	OFF	OFF
+2.5VS	2.5V switched power rail	ON	OFF	OFF
+3VALW/+3V/+3VAUX	3.3V always on power rail	ON	ON	ON*
+3VS	3.3V switched power rail	ON	OFF	OFF
+5VALW	5V always on power rail	ON	ON	ON*
+5VS	5V switched power rail	ON	OFF	OFF
+VSB	VSB always on power rail	ON	ON	ON*
+RTCVC	RTC power	ON	ON	ON

Note : ON\* means that this power plane is ON only with AC power available, otherwise it is OFF.

## External PCI Devices

Device	IDSEL#	REQ#/GNT#	Interrupts
1394	AD20	0	PIRQE

## EC SM Bus1 address

Device	Address	Device	Address
Smart Battery	0001 011X b	ADM1032	1001 100X b

## EC SM Bus2 address

## MCP67 SM Bus address

Device	Address
DDR DIMM0	1001 000Xb
DDR DIMM2	1001 001Xb

STATE	SIGNAL	SLP_S1#	SLP_S3#	SLP_S5#	+VALW	+V	+VS	Clock
Full ON		HIGH	HIGH	HIGH	ON	ON	ON	ON
S1 (Power On Suspend)		LOW	HIGH	HIGH	ON	ON	ON	LOW
S3 (Suspend to RAM)		LOW	LOW	HIGH	ON	ON	OFF	OFF
S4 (Suspend to Disk)		LOW	LOW	HIGH	ON	OFF	OFF	OFF
S5 (Soft OFF)		LOW	LOW	LOW	ON	OFF	OFF	OFF

## Board ID / SKU ID Table for AD channel

Board ID	Rb / Rd / Rf	V <sub>AD_BID min</sub>	V <sub>AD_BID typ</sub>	V <sub>AD_BID max</sub>
0	0	0 V	0 V	0 V
1	8.2K +/- 5%	0.216 V	0.250 V	0.289 V
2	18K +/- 5%	0.436 V	0.503 V	0.538 V
3	33K +/- 5%	0.712 V	0.819 V	0.875 V
4	56K +/- 5%	1.036 V	1.185 V	1.264 V
5	100K +/- 5%	1.453 V	1.650 V	1.759 V
6	200K +/- 5%	1.935 V	2.200 V	2.341 V
7	NC	2.500 V	3.300 V	3.300 V

## BOARD ID Table

Board ID	PCB Revision
0	UMA (0V)
1	DISCRETE (3.3V)
2	
3	
4	
5	
6	
7	

## BTO Option Table

BTO Item	BOM Structure
DIP CAP & RTC	45@
UMA	UMA@
VGA	VGA@
UMA & TV-OUT	UMA&TV@
2 SATA HDD	SATA2@
CAMERA	CMOS@
BLUETOOTH	BT@
MINI CARD 1 (TV)	MINI1@
MINI CARD 2 (WLAN)	MINI2@
NEW CARD	EXPRESS@
TV-OUT	TV@
DVI	DVI@
1394	1394@
CARD READER	5IN1@
HT Debug Port	HT@

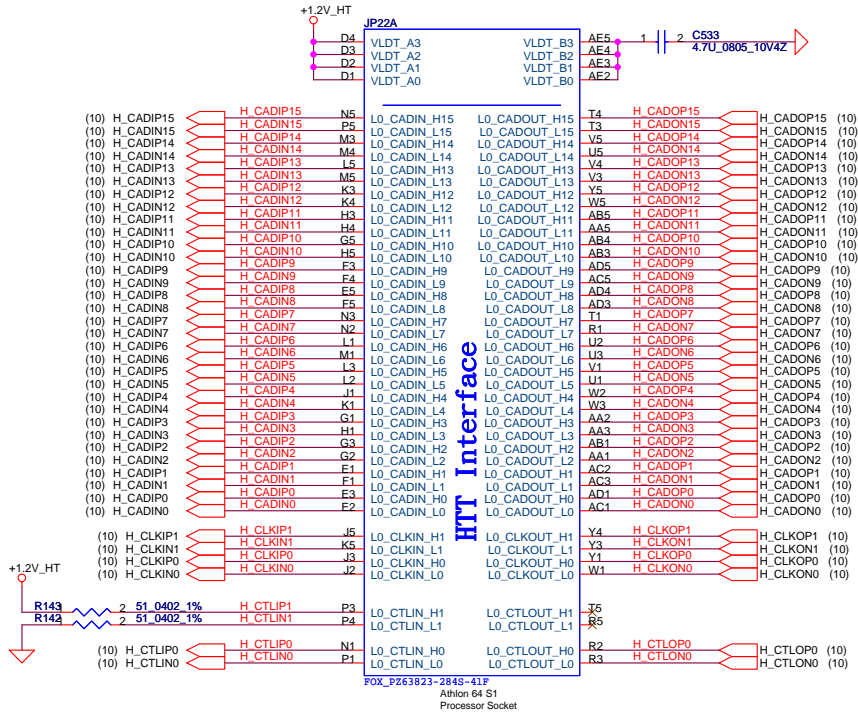
## SKU ID Table

SKU ID	SKU
0	B - PHASE
1	C - PHASE
2	
3	
4	
5	
6	
7	

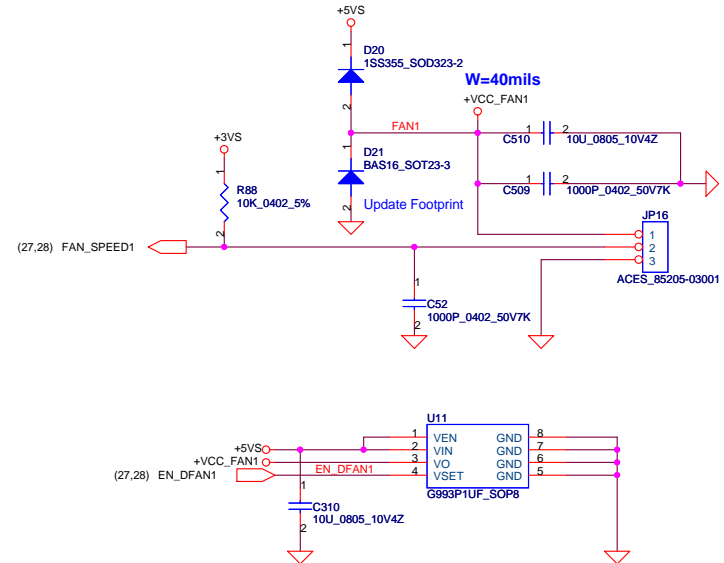
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## PROCESSOR HYPERTRANSPORT INTERFACE

VLDT\_Ax AND VLDT\_Bx ARE CONNECTED TO THE LDT\_RUN POWER SUPPLY THROUGH THE PACKAGE OR ON THE DIE. IT IS ONLY CONNECTED ON THE BOARD TO DECOUPLING NEAR THE CPU PACKAGE



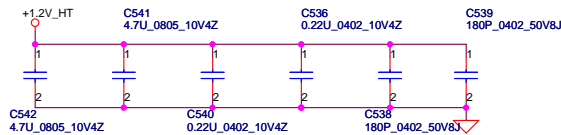
## FAN Conn



## FAN1 Conn

## LAYOUT: Place bypass cap on topside of board

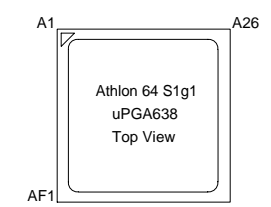
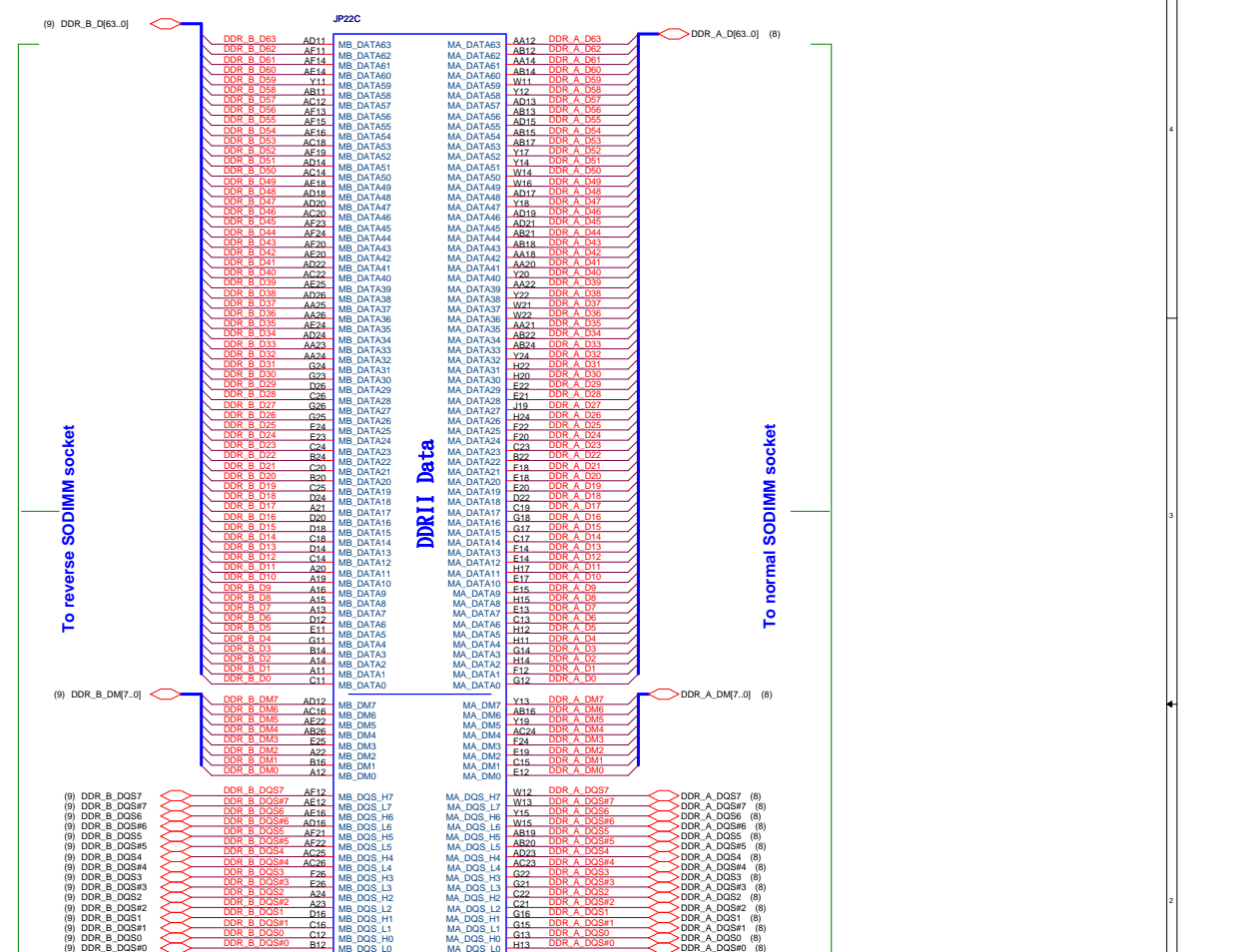
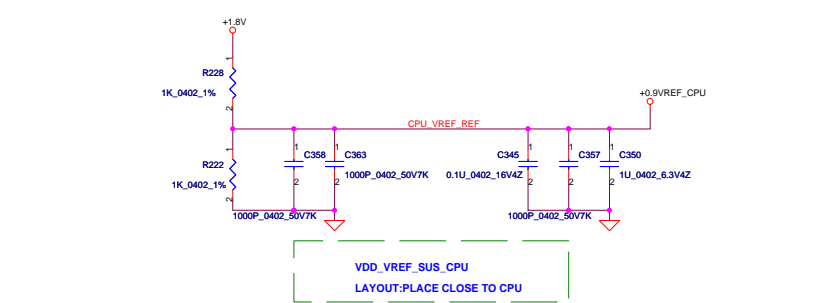
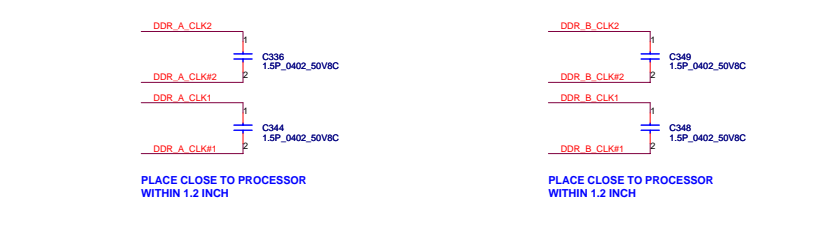
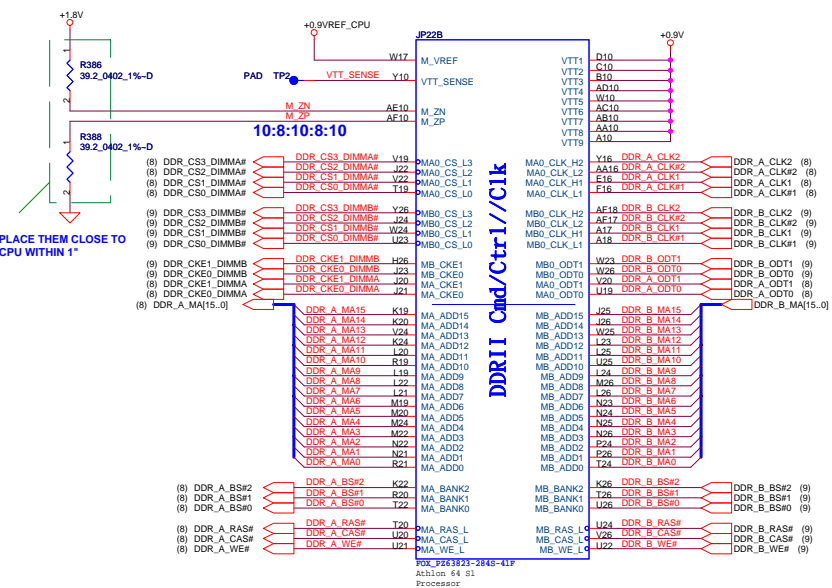
NEAR HT POWER PINS THAT ARE NOT CONNECTED DIRECTLY TO DOWNSTREAM HT DEVICE, BUT CONNECTED INTERNALLY TO OTHER HT POWER PINS PLACE CLOSE TO VLDTO POWER PINS



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Issued Date	2006/08/18	Deciphered Date	2007/8/18	Size	AMD CPU HT I/F
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# Processor DDR2 Memory Interface

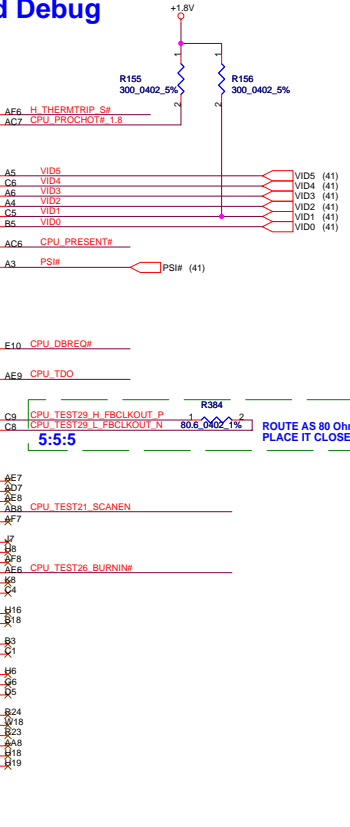
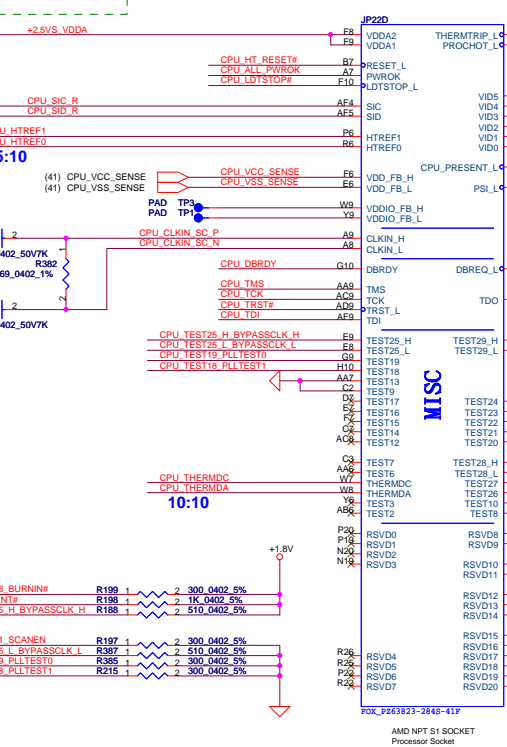
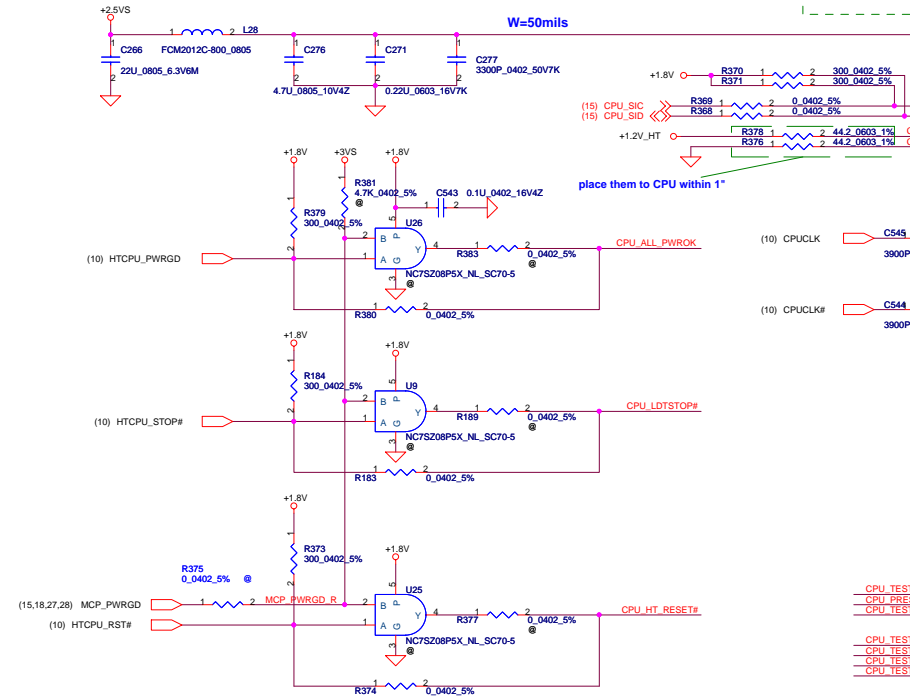
VDD VTT SUS\_CPU IS CONNECTED TO THE VDD VTT SUS POWER SUPPLY THROUGH THE PACKAGE OR ON THE DIE. IT IS ONLY CONNECTED ON THE BOARD TO DECOUPLING NEAR THE CPU PACKAGE.



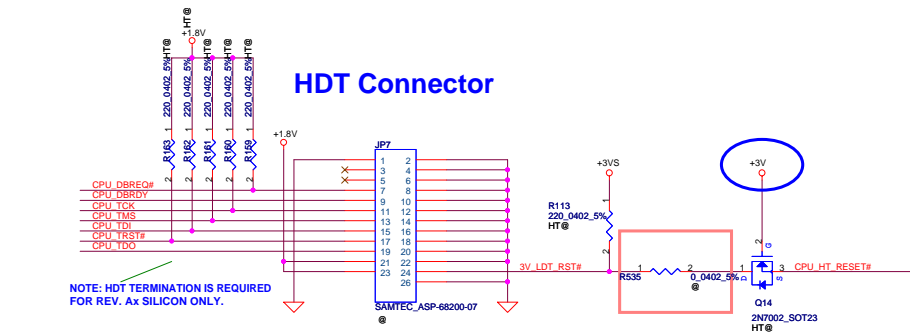
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# ATHLON Control and Debug

LAYOUT: ROUTE VDDA TRACE APPROX. 50 mils WIDE (USE 2x25 mil TRACES TO EXIT BALL FIELD) AND 500 mils LONG.

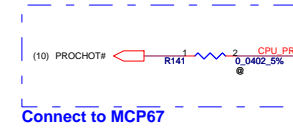


## HDT Connector



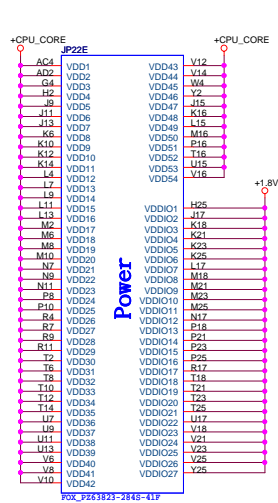
PVT Modify 2007/03/22

U2 CLOSE CPU, CPU\_THERMDA&CPU\_THERMDC PLACE CLOSE TO PROCESSOR WITHIN 1" INCH

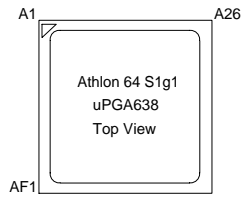


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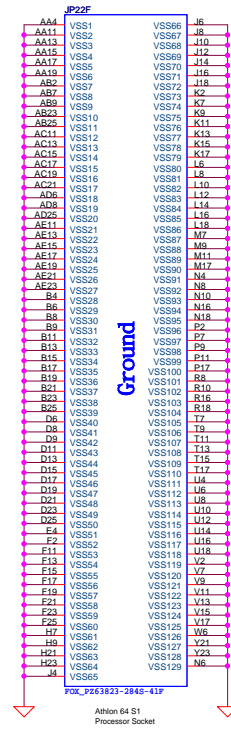
# PROCESSOR POWER AND GROUND



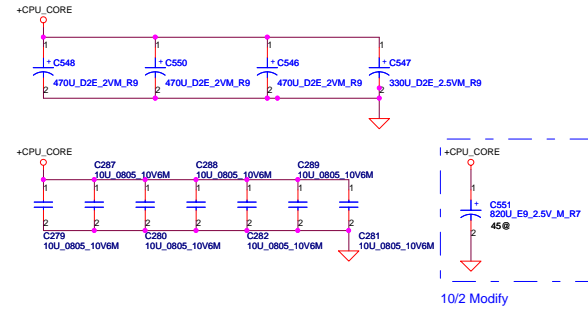
Athlon 64 S1 Processor Socket



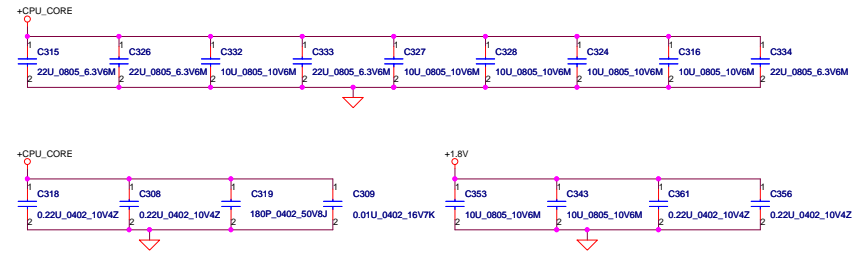
Athlon 64 S1g1 uPGA638 Top View



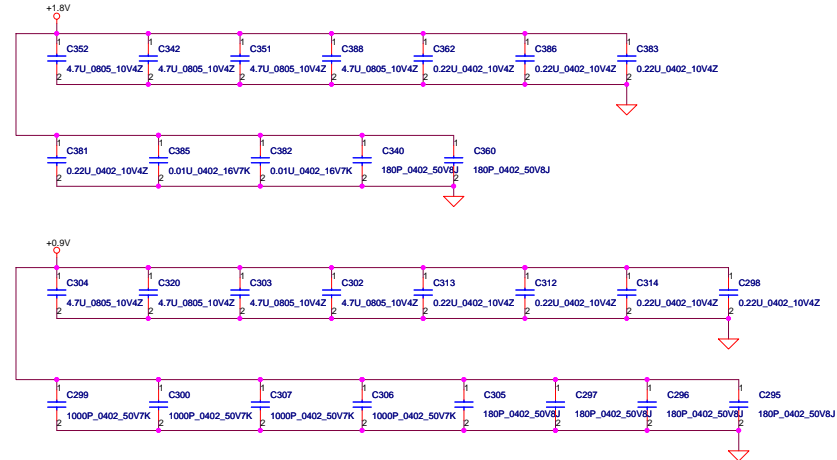
Athlon 64 S1 Processor Socket



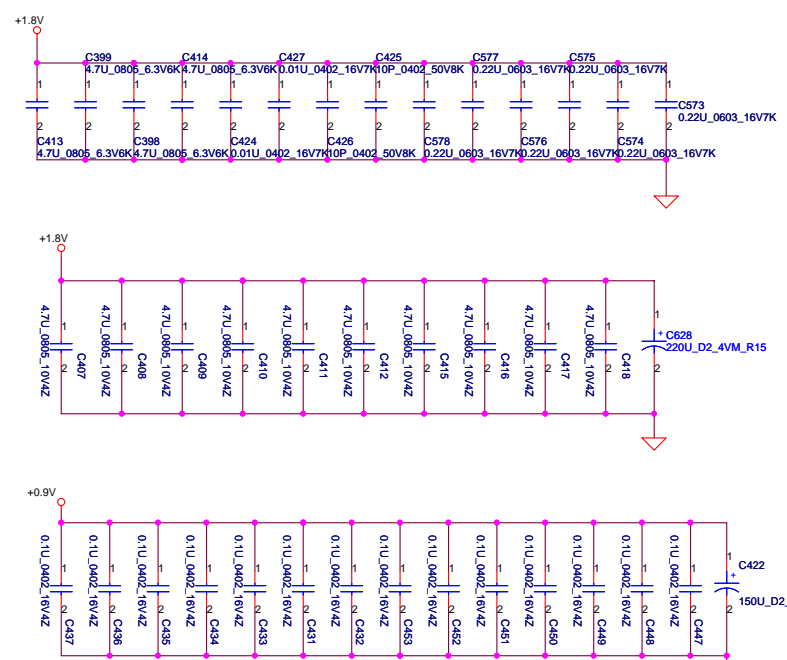
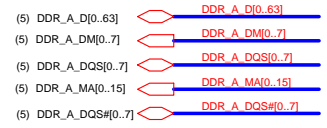
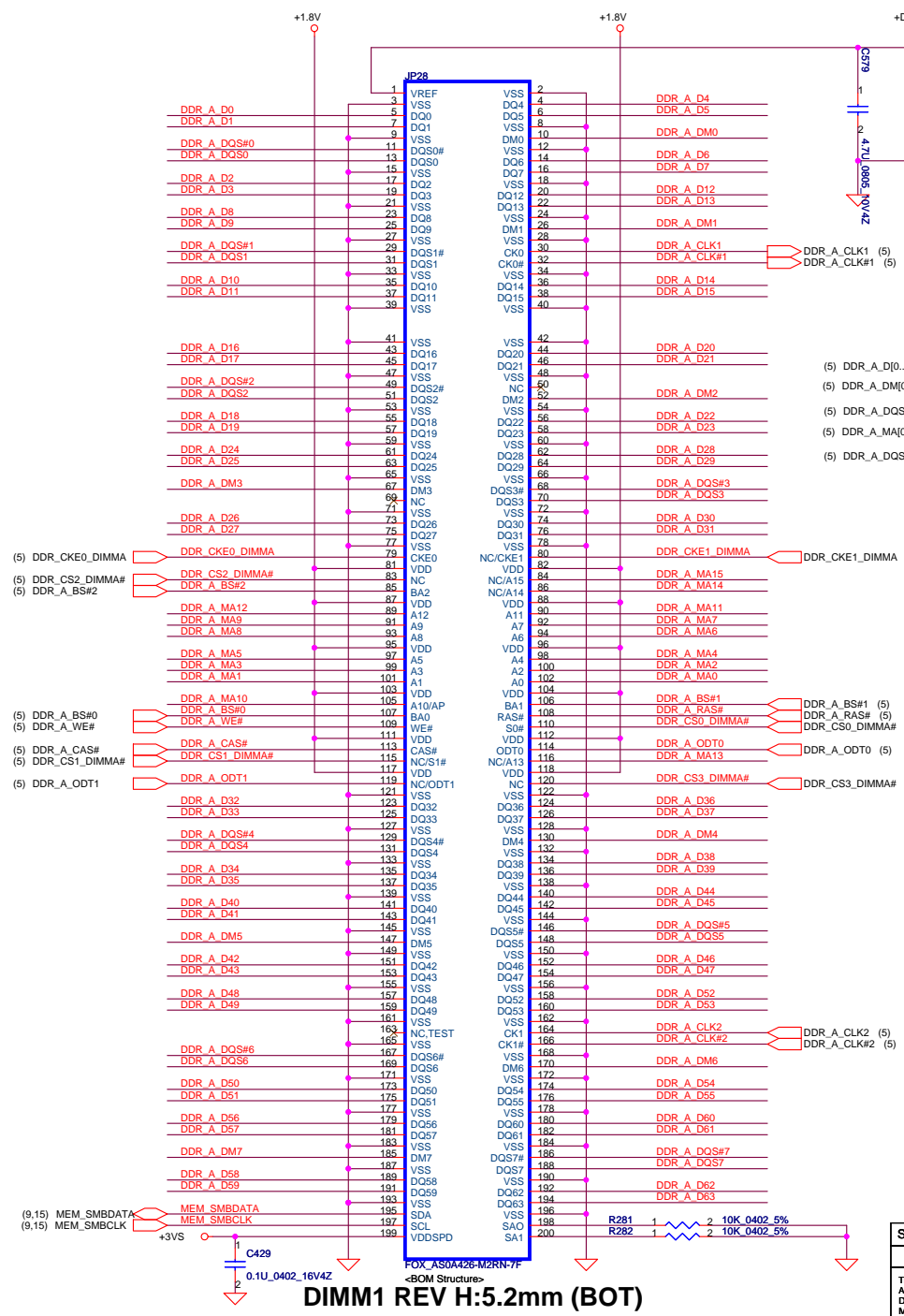
## CPU SOCKET S1 DECOUPLING



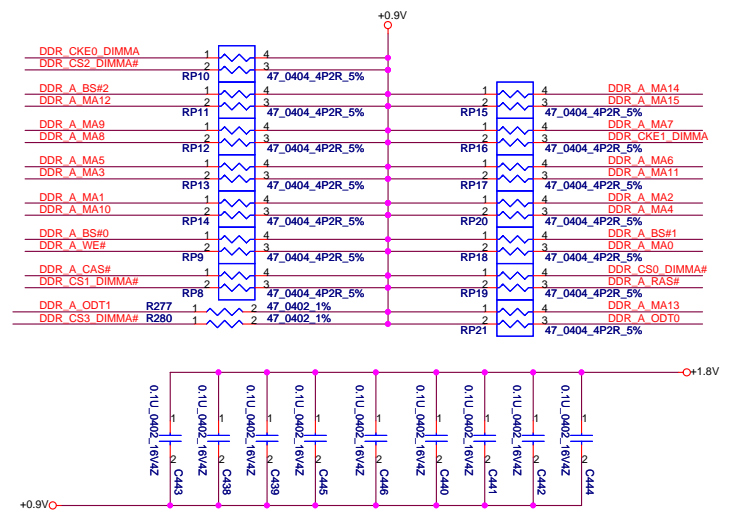
## DECOUPLING BETWEEN PROCESSOR AND DIMMS PLACE CLOSE TO PROCESSOR AS POSSIBLE



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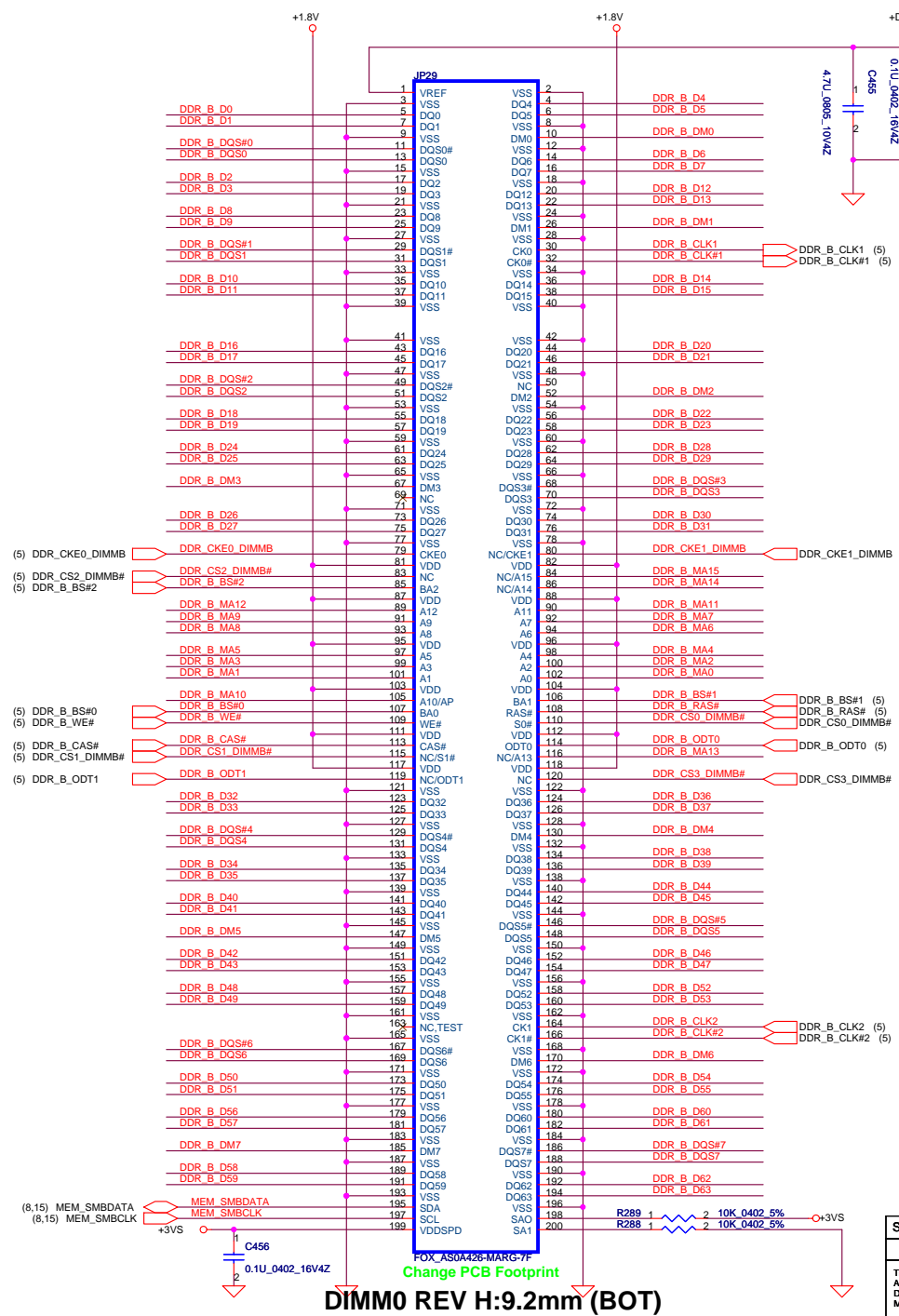
**Layout Note:**  
Place one cap close to every 2 pullup resistors terminated to +0.9V



**Layout Note:**  
Place one 0.1uF cap close to every 2 pullup resistors terminated to +0.9V

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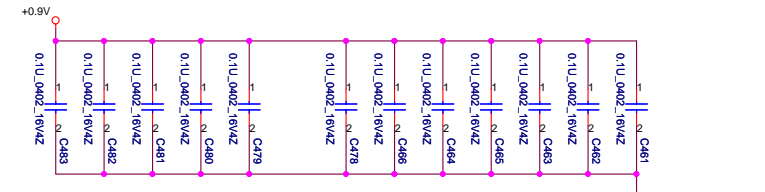
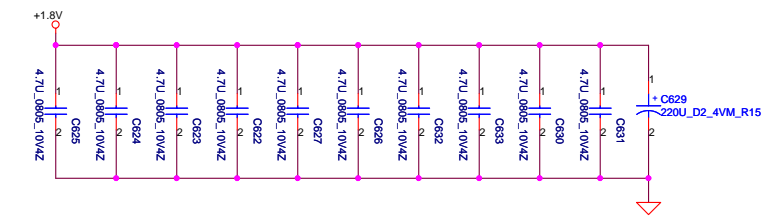
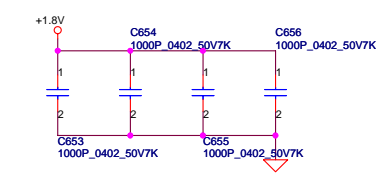




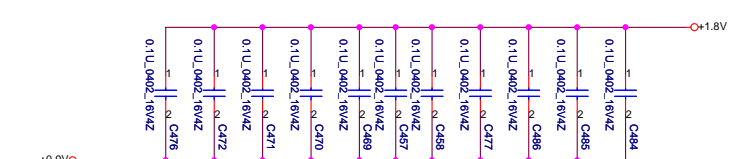
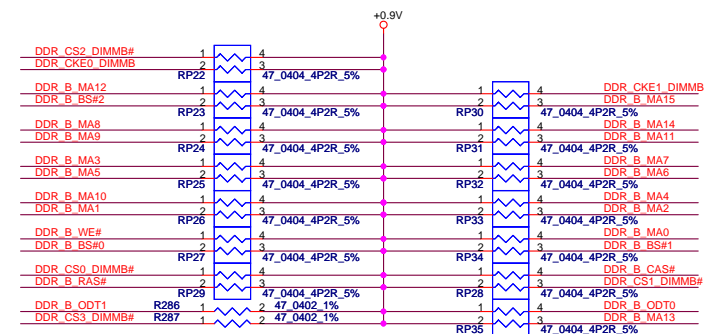
**DIMM0 REV H:9.2mm (BOT)**

Change PCB Footprint

- (5) DDR\_B\_D0[0..63] **DDR\_B\_D0[0..63]**
- (5) DDR\_B\_DM[0..7] **DDR\_B\_DM[0..7]**
- (5) DDR\_B\_DQS[0..7] **DDR\_B\_DQS[0..7]**
- (5) DDR\_B\_MA[0..15] **DDR\_B\_MA[0..15]**
- (5) DDR\_B\_DQS#[0..7] **DDR\_B\_DQS#[0..7]**

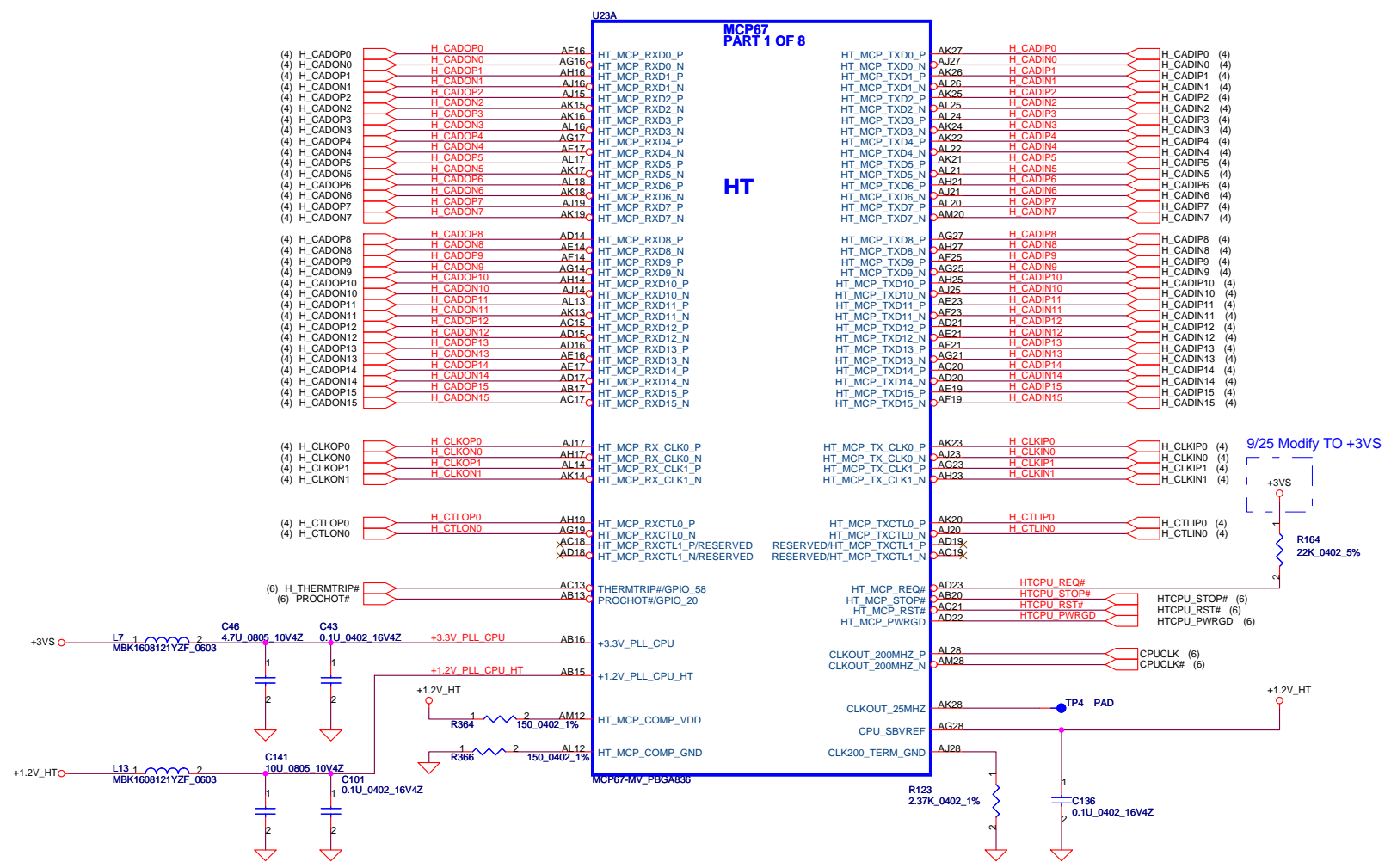


**Layout Note:**  
Place one cap close to every 2 pullup resistors terminated to +0.9V



**Layout Note:**  
Place one 0.1uF cap close to every 2 pullup resistors terminated to +0.9V

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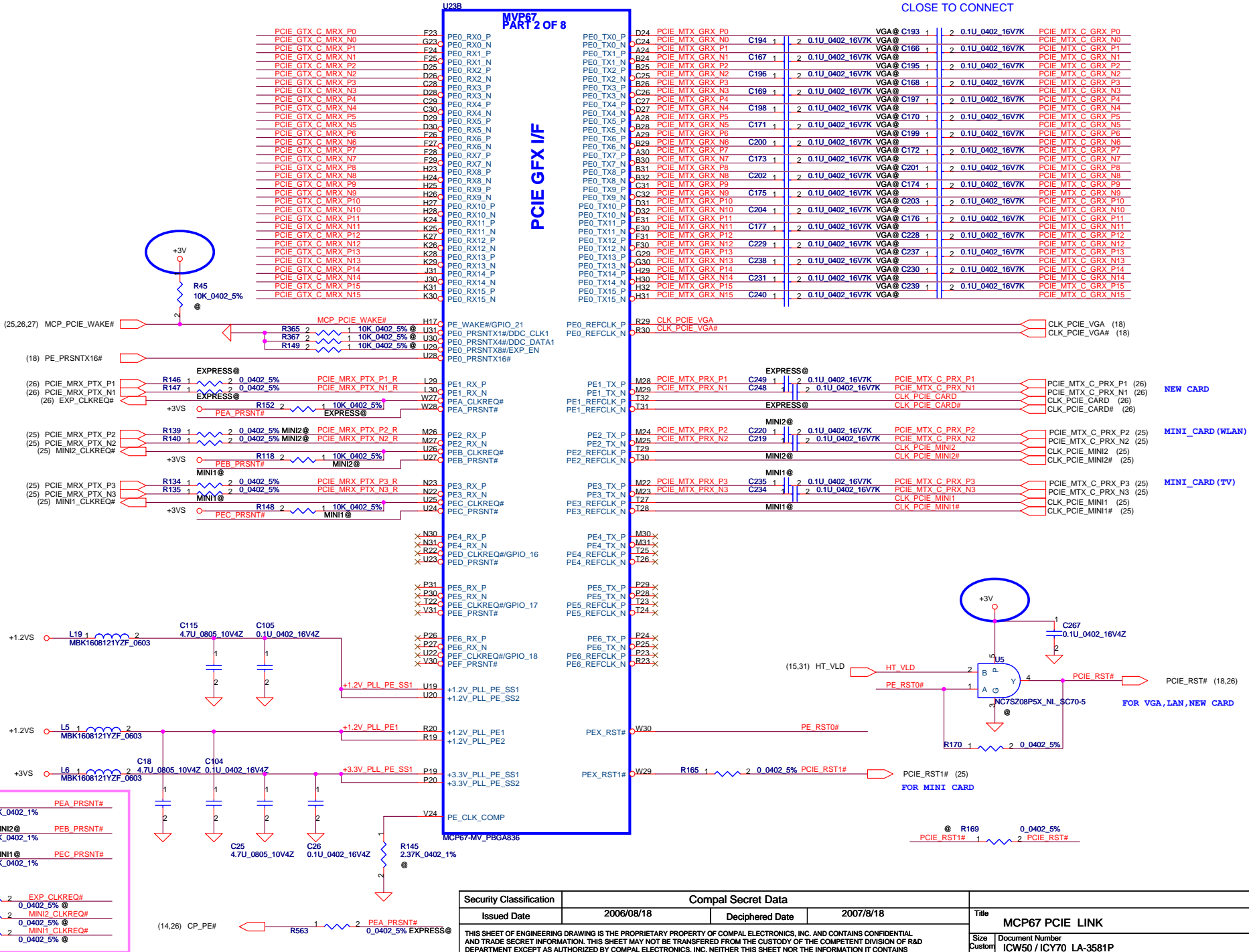
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Issued Date	2006/08/18	Deciphered Date	2007/8/18	MCP67 HT LINK	
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(18) PCIE\_GTX\_C\_MRX\_P[0..15] PCIE GTX C\_MRX\_P[0..15]

(18) PCIE\_GTX\_C\_MRX\_N[0..15] PCIE GTX C\_MRX\_N[0..15]

(18) PCIE\_MTX\_C\_GRX\_P[0..15] PCIE MTX C GRX\_P[0..15]

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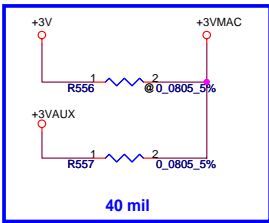


**MP 2007/4/12 Added**

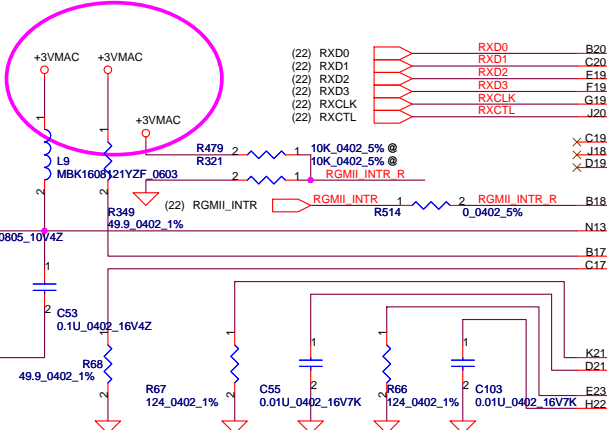
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 R551 2 1K\_0402\_1% MINI2# PEB\_PRSNT#  
 R552 2 1K\_0402\_1% MINI1# PEC\_PRSNT#

R553 1 0.0402\_5% @ EXP\_CLKREQ#  
 R554 1 0.0402\_5% @ MINI2\_CLKREQ#  
 R555 1 0.0402\_5% @ MINI1\_CLKREQ#

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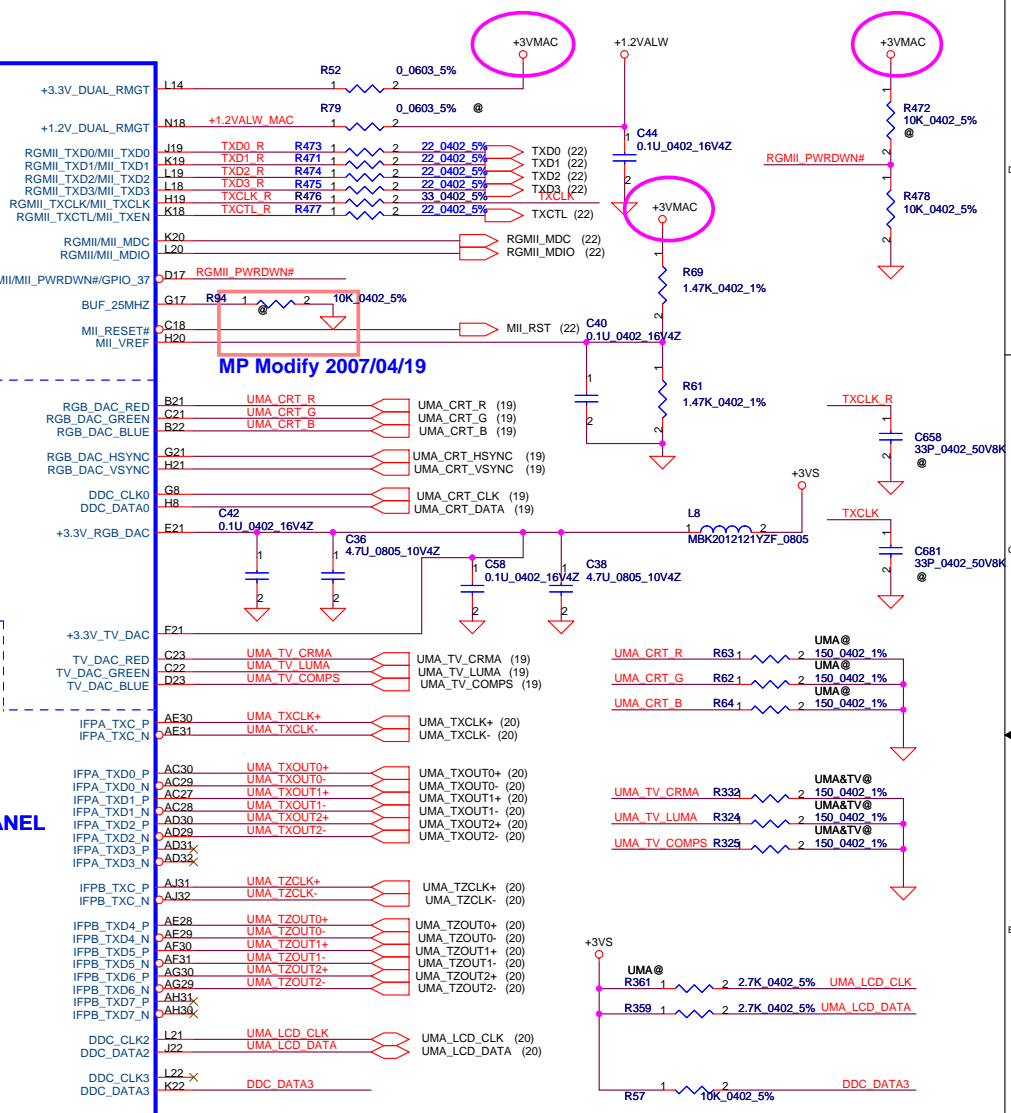
MP Modify 2007/04/13



LAN

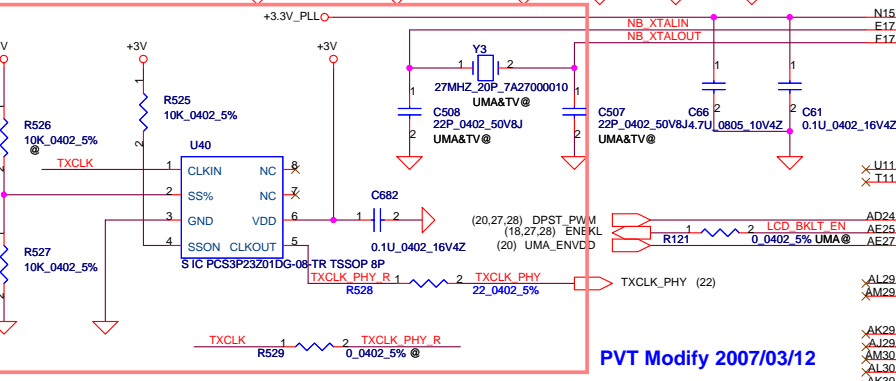
DACS

FLAT PANEL

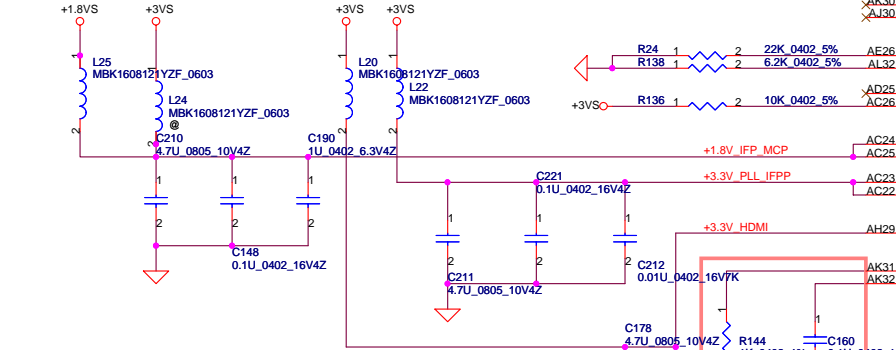


MP Modify 2007/04/19

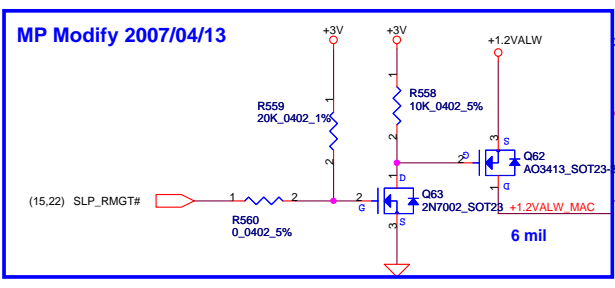
PVT Modify 2007/03/12



PVT Modify 2007/03/12

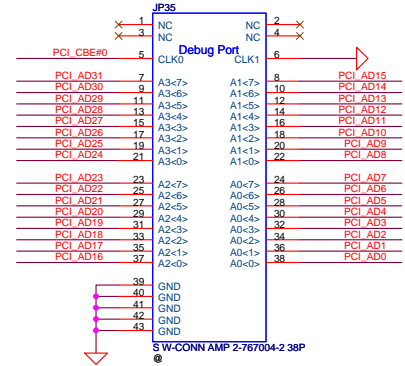
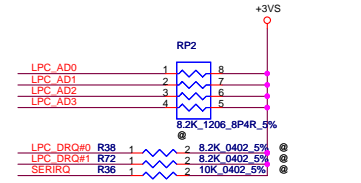
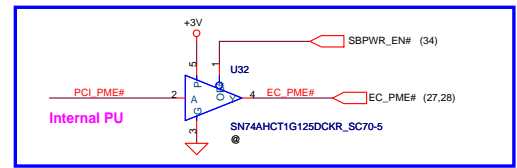
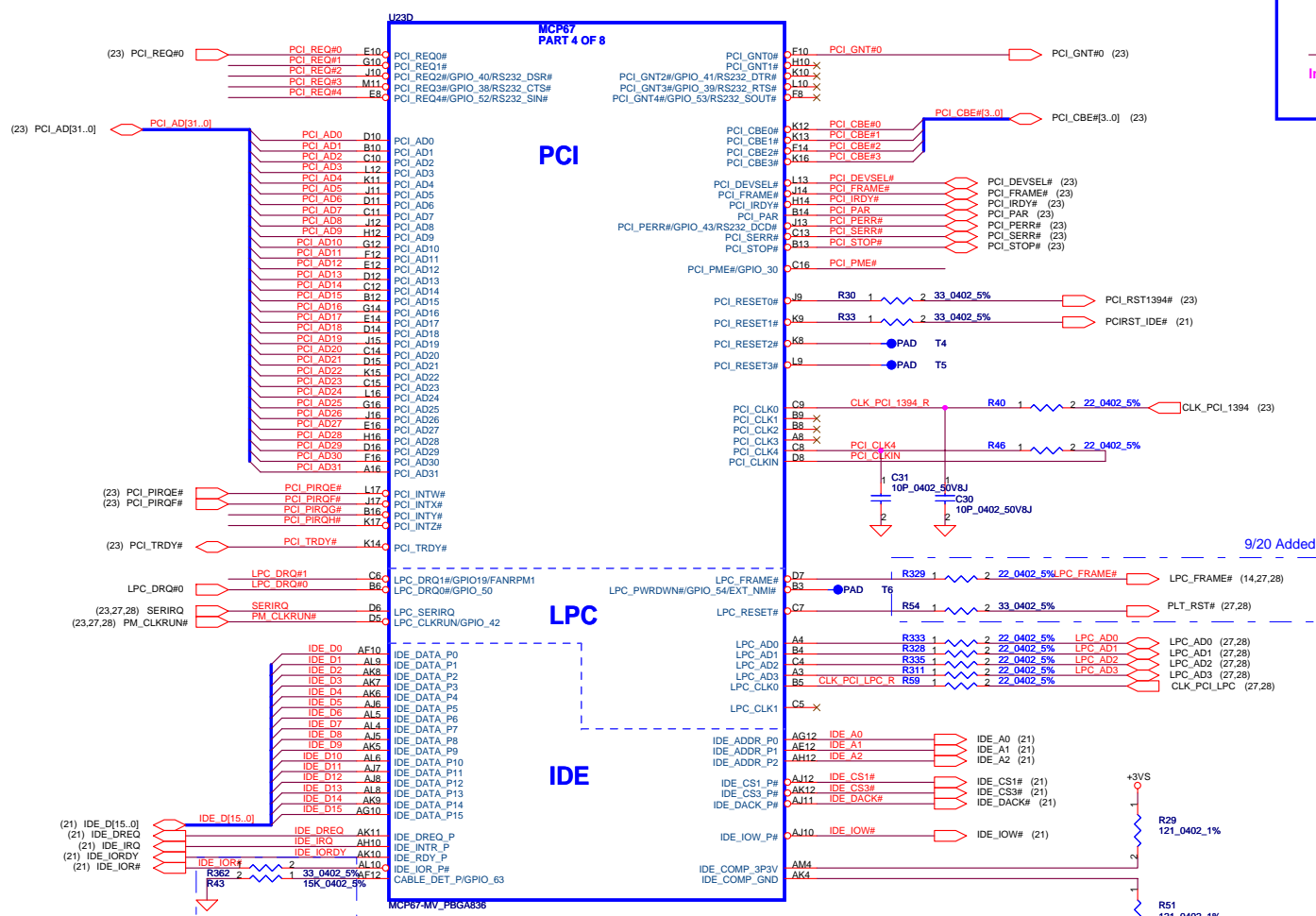
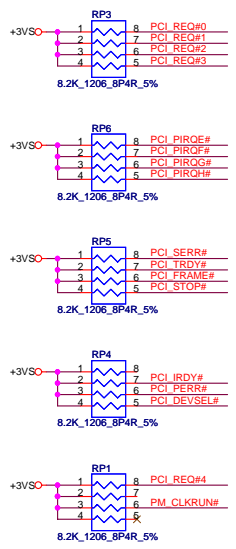


PVT Modify 2007/03/12



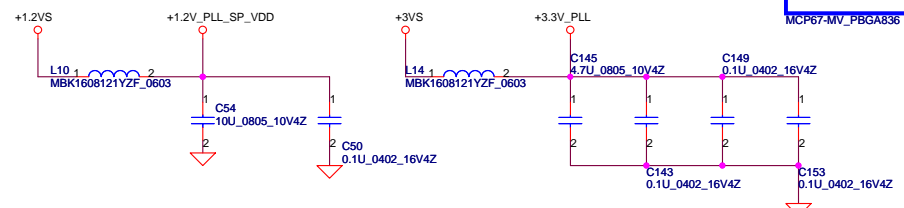
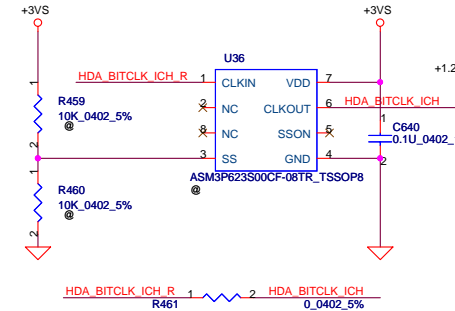
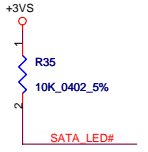
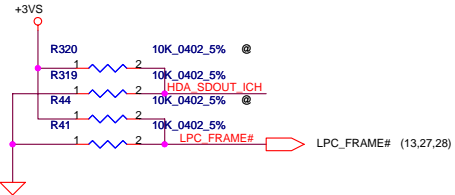
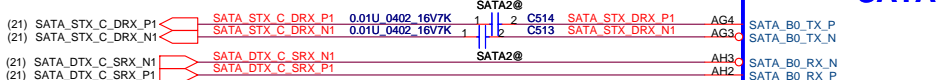
MP Modify 2007/04/13

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				Custom	ICW50 / ICY70 LA-3581P
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Date:	Friday, April 20, 2007	Sheet	12	of	42
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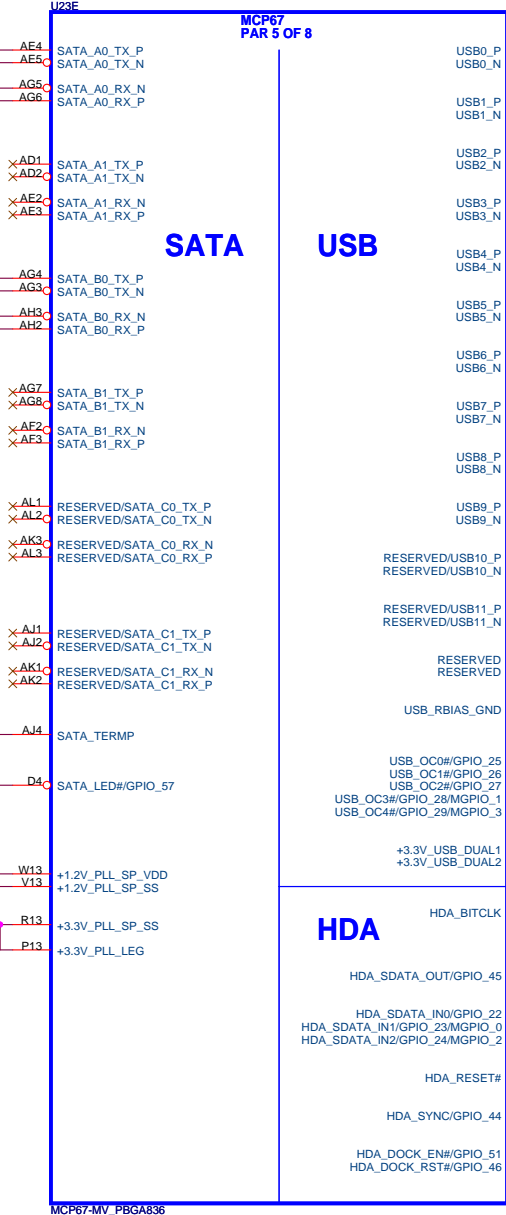
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Issued Date	2006/08/18	Deciphered Date	2007/8/18
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PLACE SATA AC COUPLING  
CAPS CLOSE TO MCP67

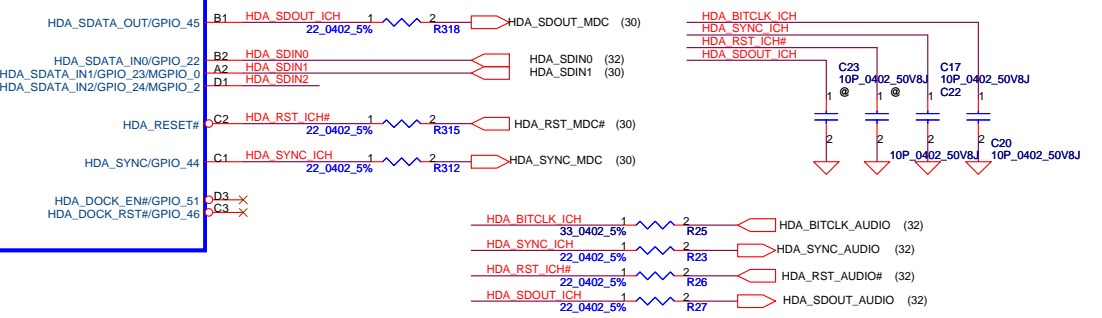


HDA_SDOUT	LPC_FRAME	FUNCTION
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"0"	"1"	PCI BIOS
"1"	"0"	SPI BIOS
"1"	"1"	RESERVED

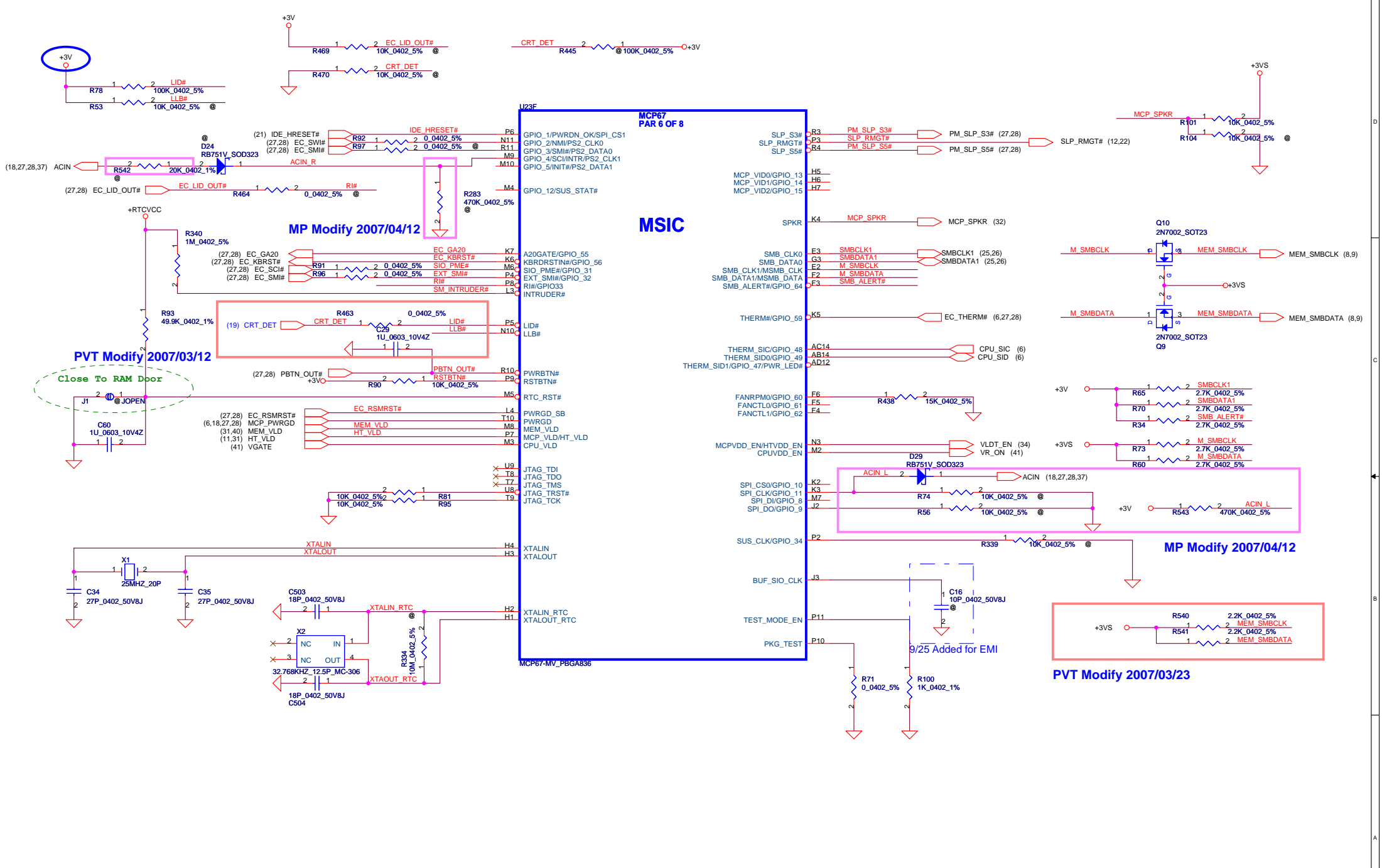
\*DEFAULT



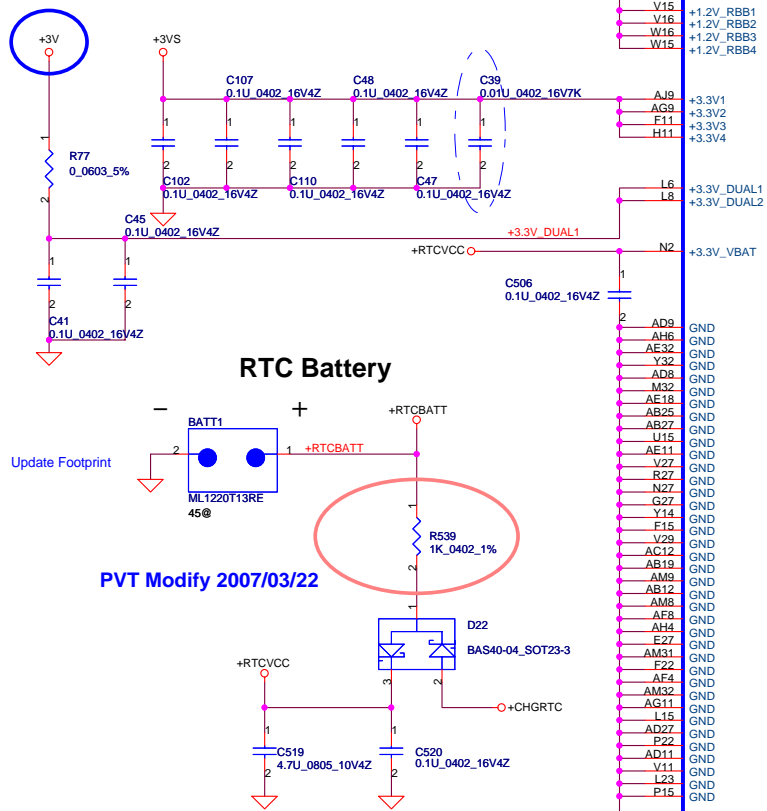
**HDA**



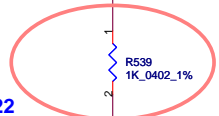
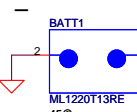
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Issued Date	2006/08/18	Deciphered Date	2007/8/18	MCP67 SATA/ USB/ HDAUDIO		
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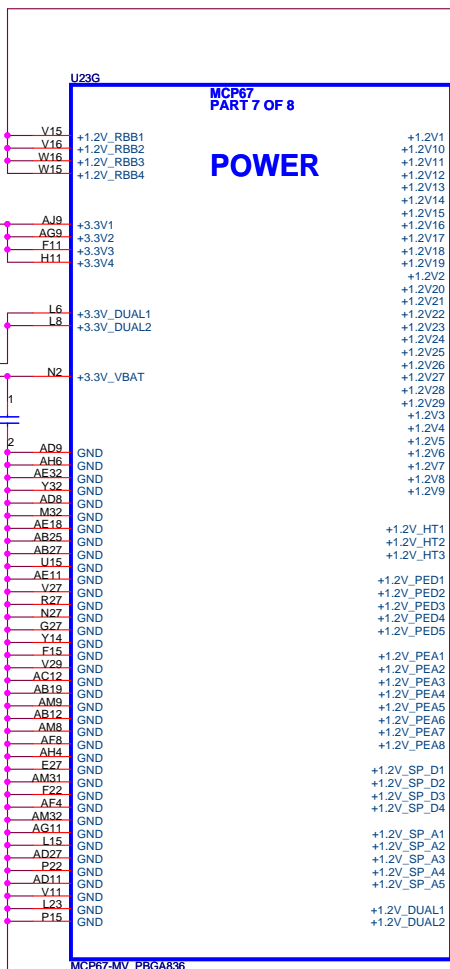


### RTC Battery

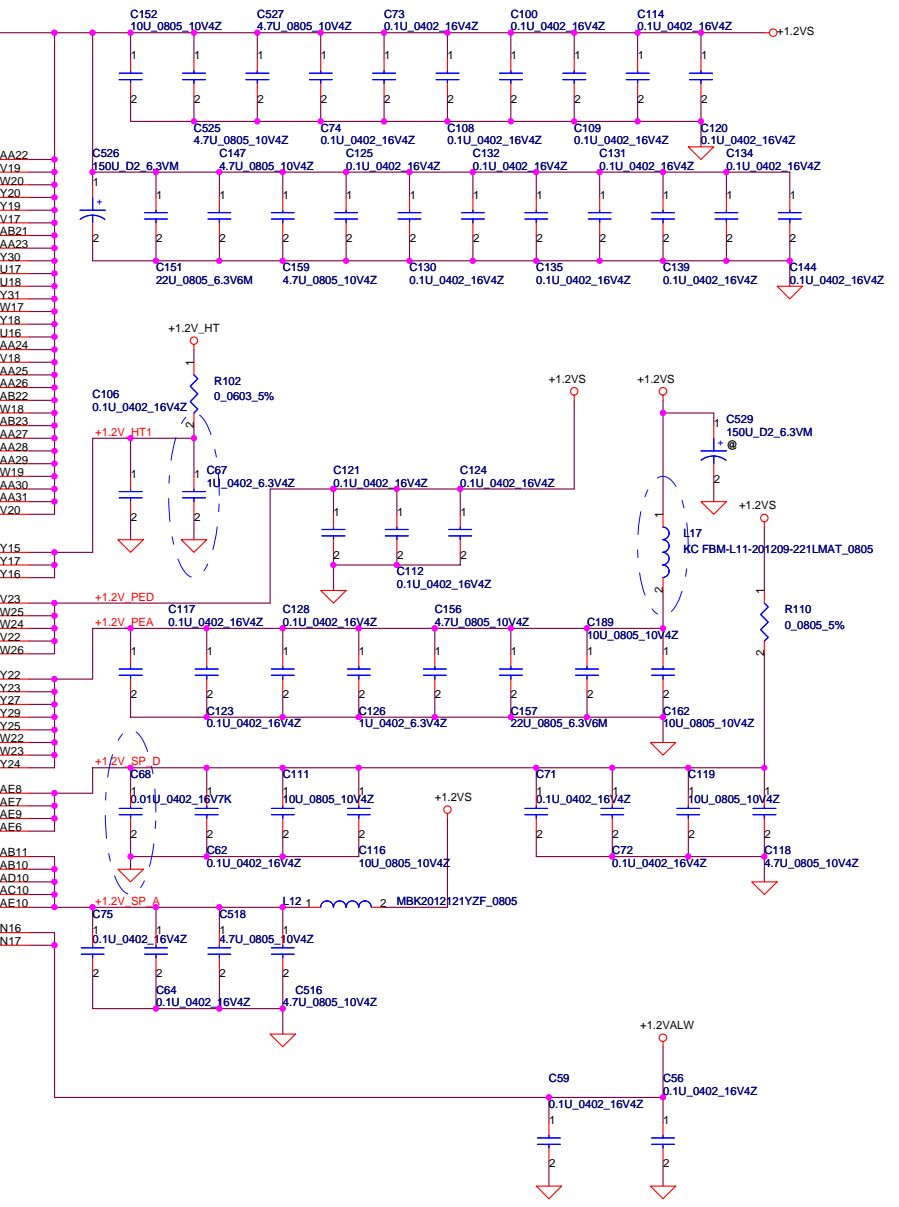


### MCP67-MV POWER STATES

Power Signal	S0	S1	S3	S4/S5	G3
	ON	ON	OFF	OFF	OFF
	ON	ON	OFF	OFF	OFF
	ON	ON	OFF	OFF	OFF
	ON	ON	OFF	OFF	OFF
	ON	ON	OFF	OFF	OFF
	ON	ON	OFF	OFF	OFF
	ON	ON	OFF	OFF	OFF
	ON	ON	OFF	OFF	OFF
	ON	ON	OFF	OFF	OFF
	ON	ON	OFF	OFF	OFF
	ON	ON	OFF	OFF	OFF
	ON	ON	OFF	OFF	OFF
	ON	ON	OFF	OFF	OFF
	ON	ON	OFF	OFF	OFF
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	ON	ON	OFF	OFF	OFF
	ON	ON	OFF	OFF	OFF
	ON	ON	OFF	OFF	OFF

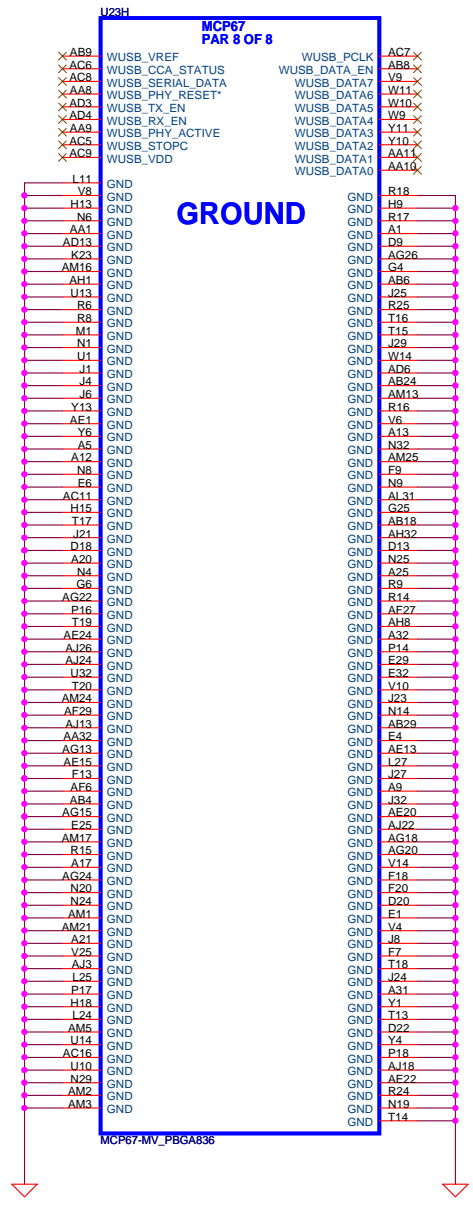


### POWER



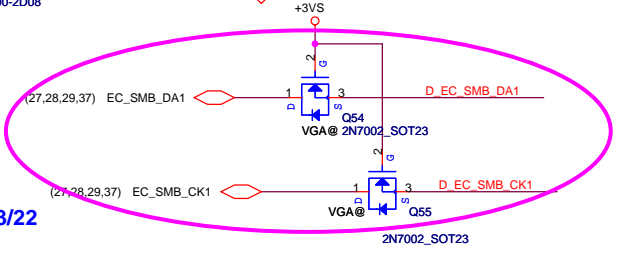
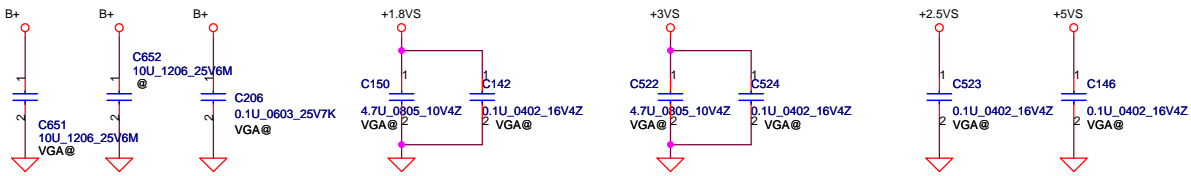
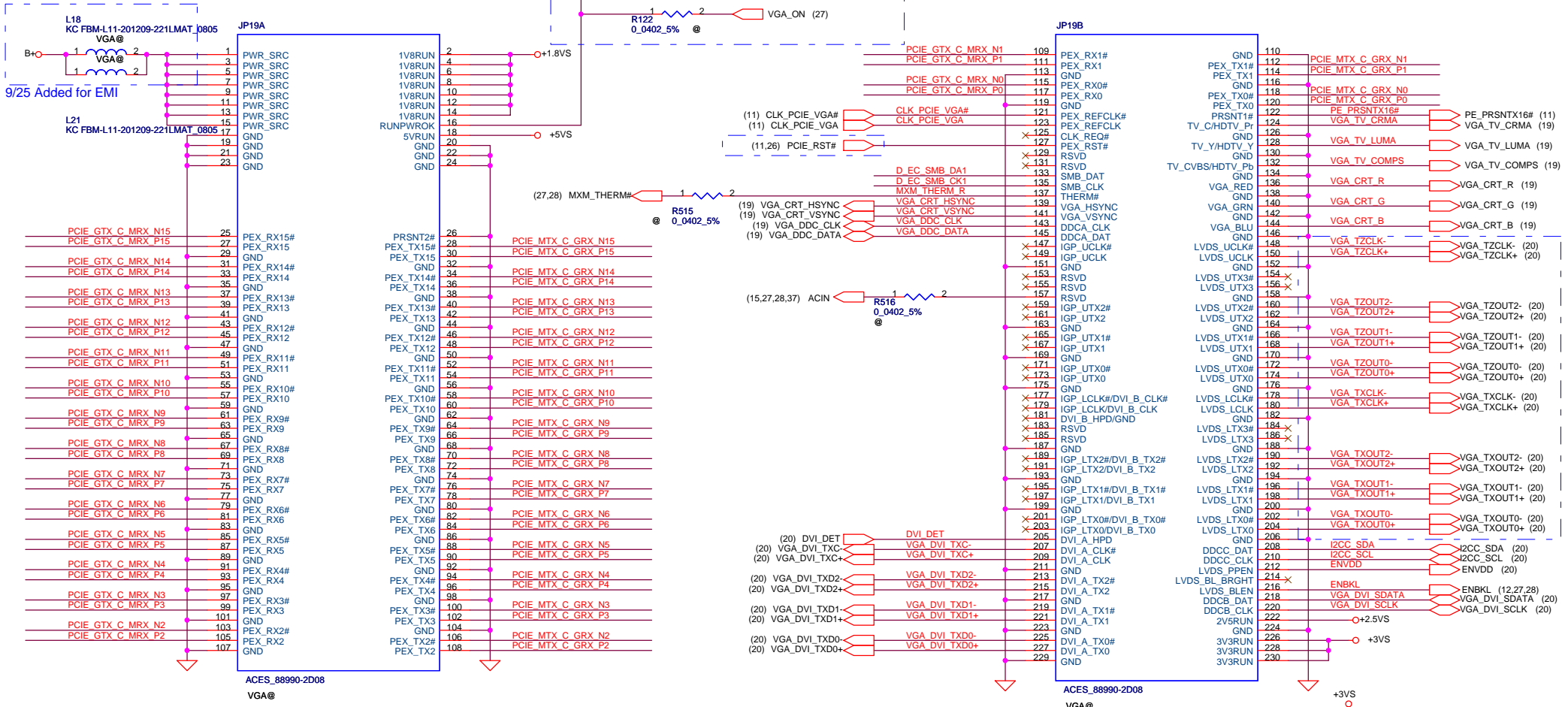
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Issued Date	2006/08/18	Deciphered Date	2007/8/18			
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				MCP67 GROUND	
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				Date:	Friday, April 20, 2007
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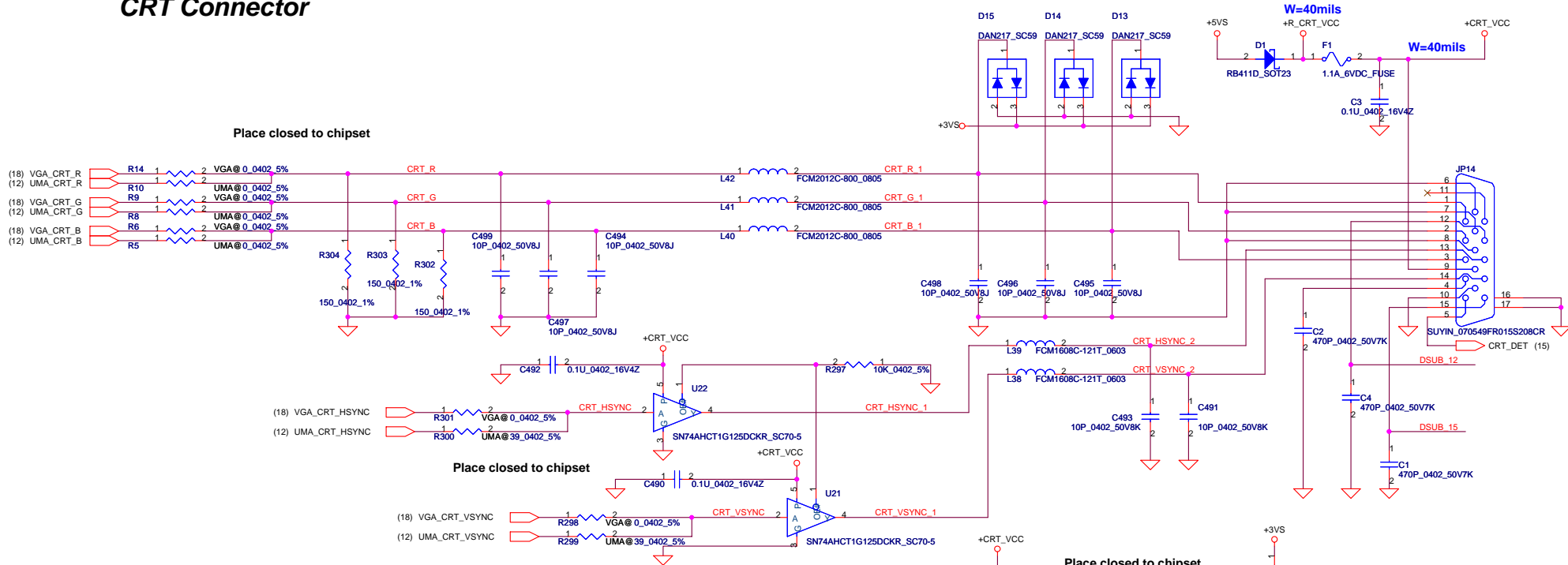
- (11) PCIE\_MTX\_C\_GRX\_N[0..15] PCIE\_MTX\_C\_GRX\_N[0..15]
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- (11) PCIE\_GTX\_C\_MRX\_N[0..15] PCIE\_GTX\_C\_MRX\_N[0..15]
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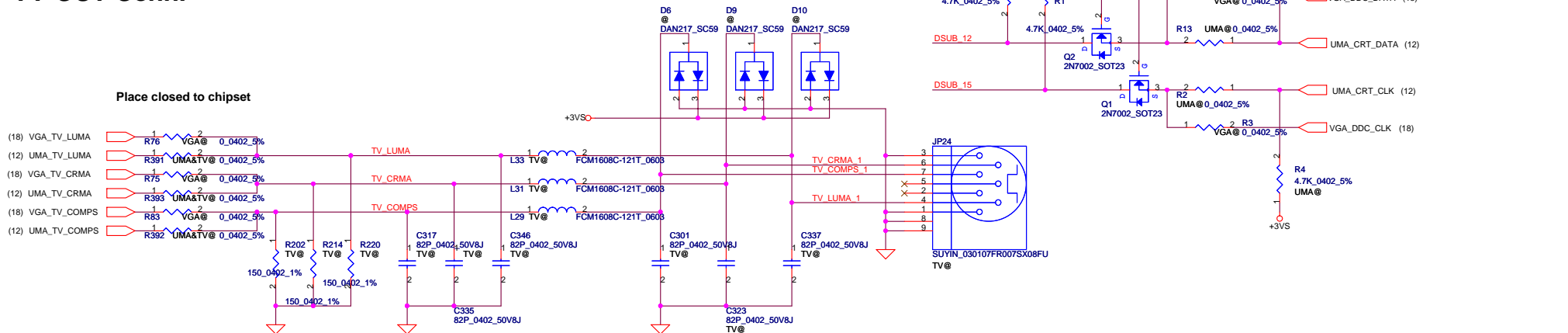
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# CRT Connector

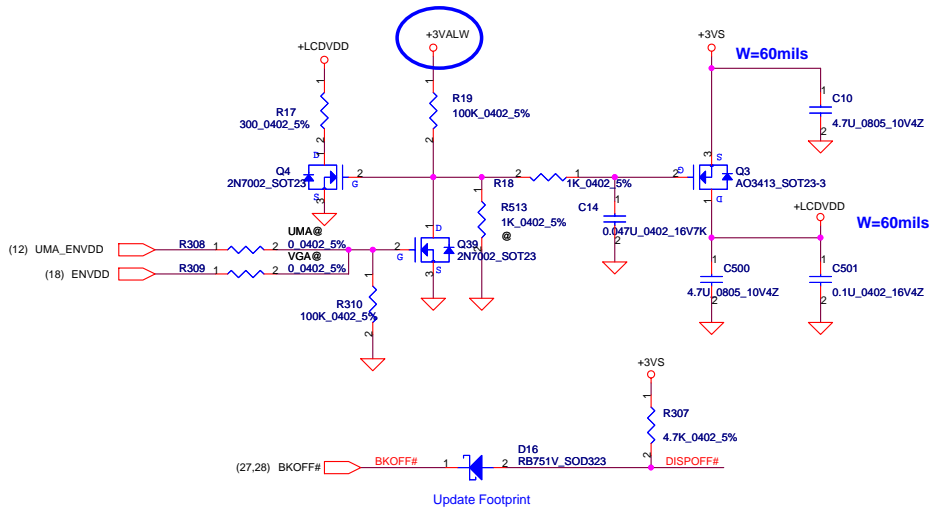


# TV-OUT Conn.

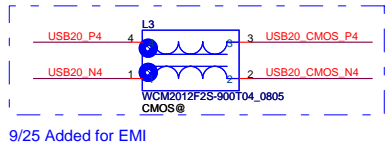
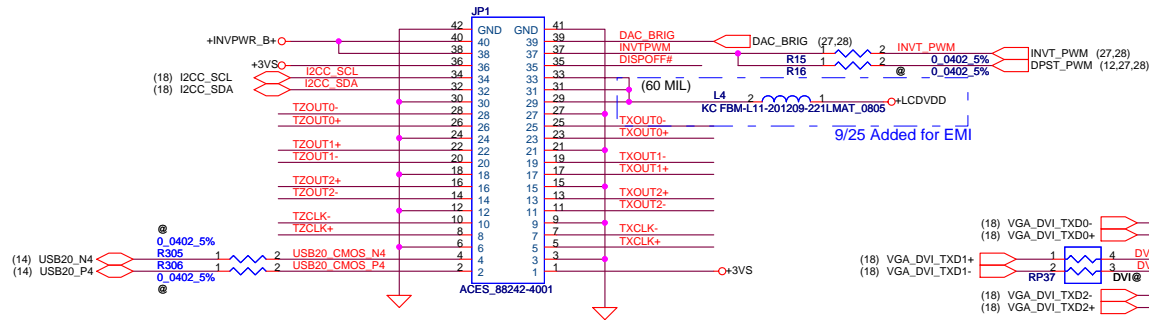


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Size	B	Document Number	ICW50 / ICY70 LA-3581P	Rev	1.0
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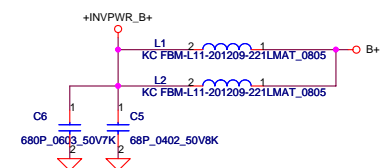
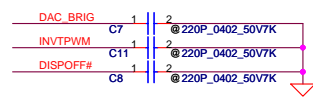
# LCD POWER CIRCUIT



# LCD/PANEL BD. Conn.

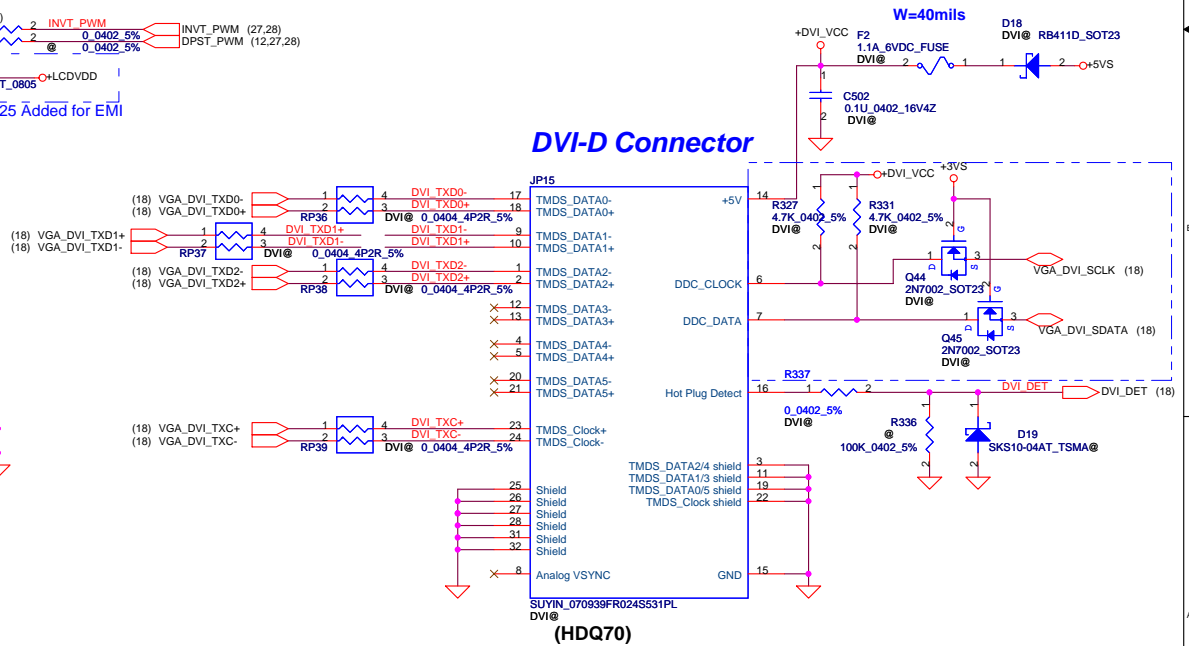


# Fro CMOS Camera



10/2 SWAP PIN

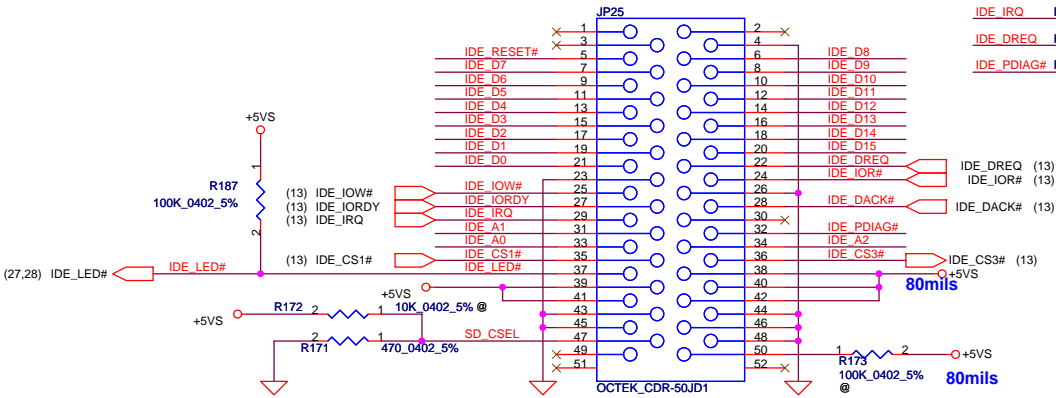
# DVI-D Connector



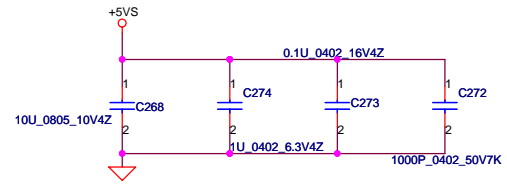
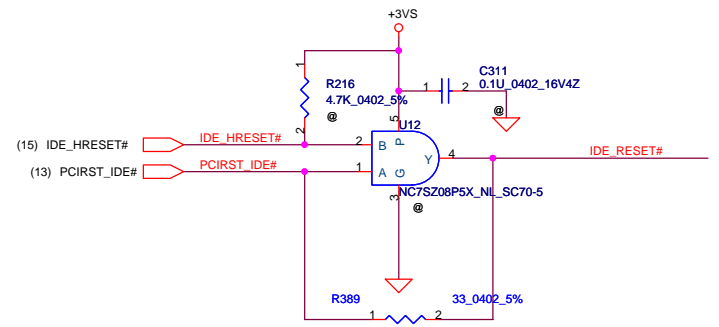
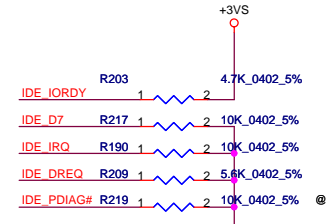
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(13) IDE\_D[0..15]  IDE\_D[0..15]  
 (13) IDE\_A[0..2]  IDE\_A[0..2]

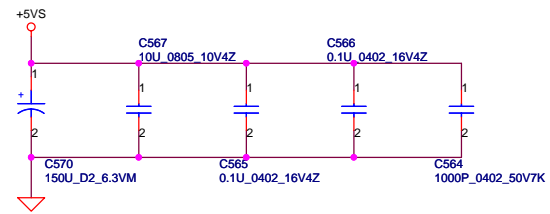
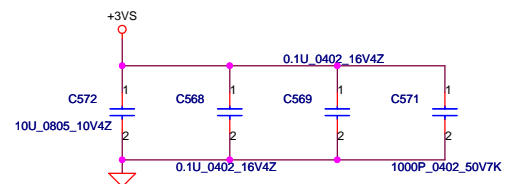
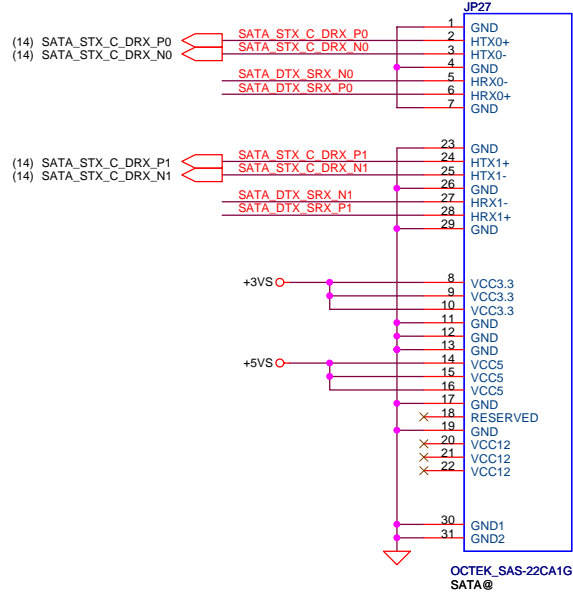
### CDROM CONN



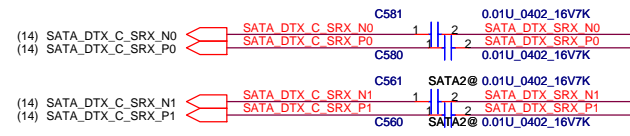
If CDROM is Slave  
 then SD\_CSEL= Floating  
 else SD\_CSEL= Low



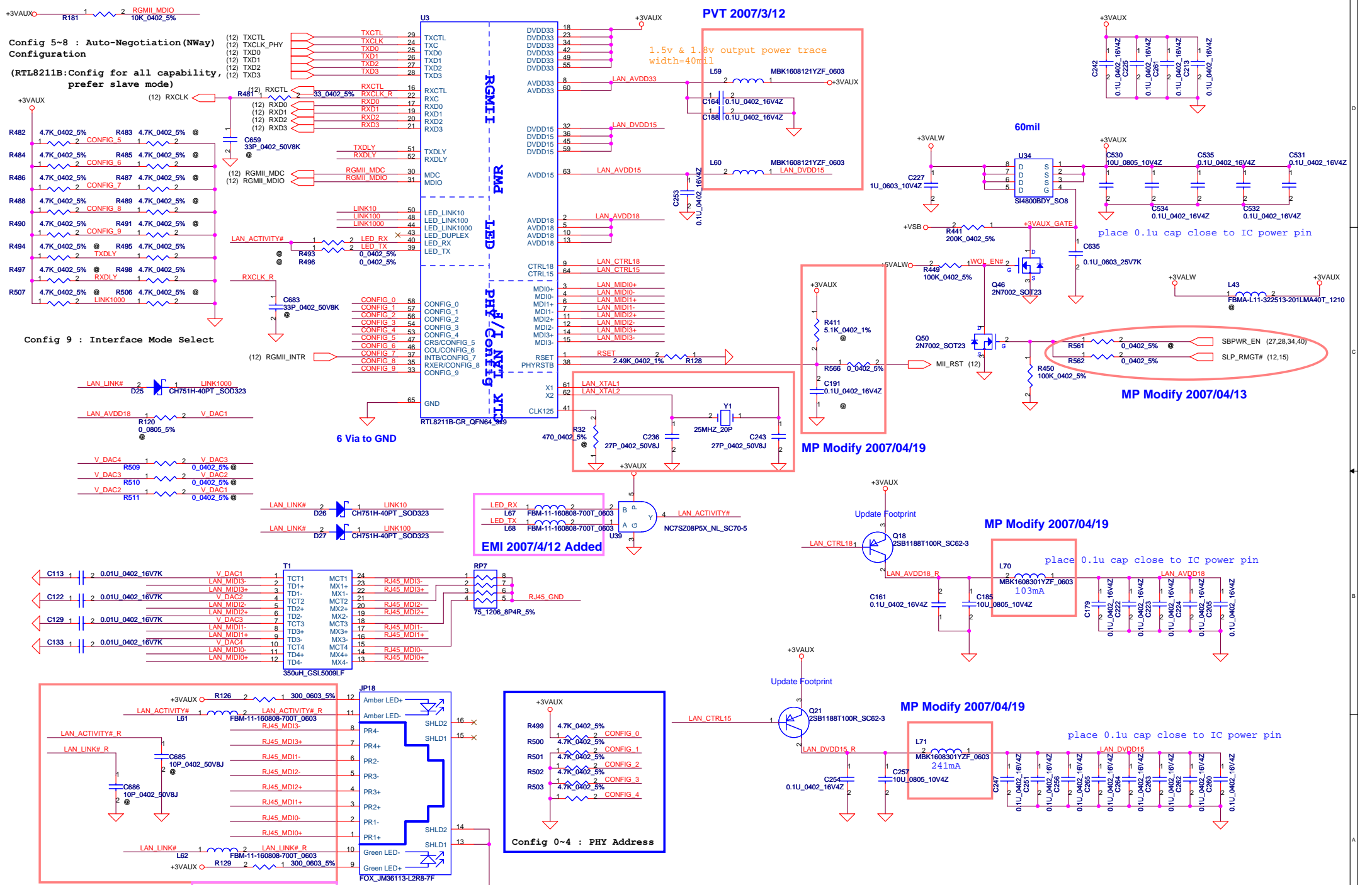
### SATA HDD Conn.(SAS Connector)



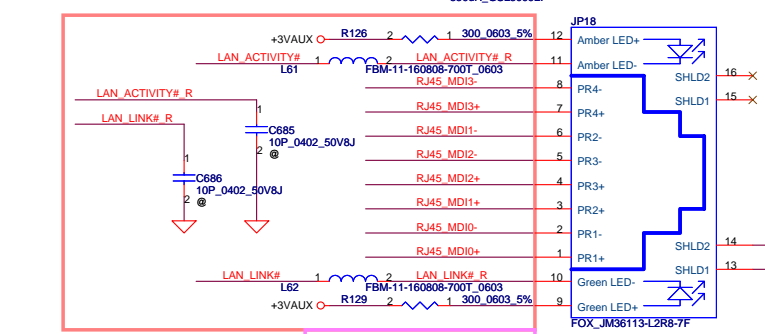
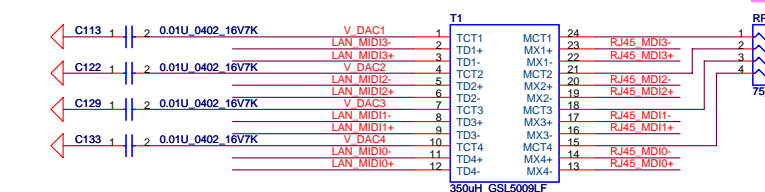
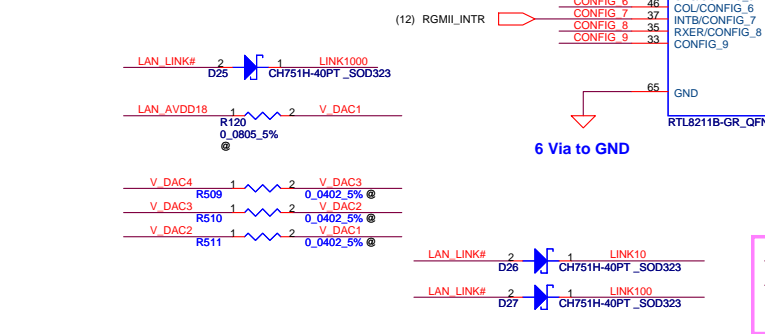
Close to SATA HDD



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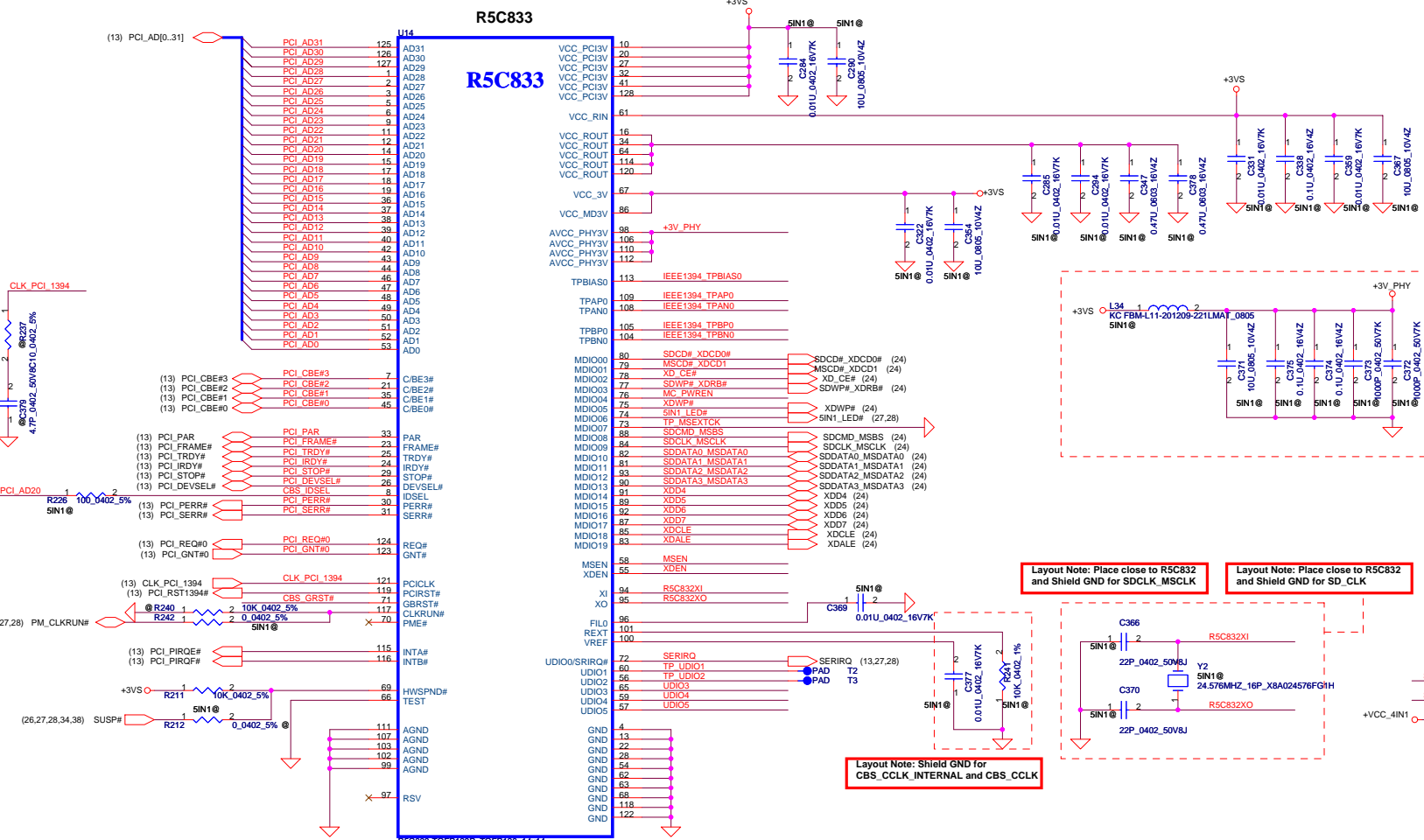
**Config 5-8 : Auto-Negotiation (NWay) Configuration**  
(RTL8211B: Config for all capability prefer slave mode)



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		2007/8/18

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Title	PHY RTL8211B	
Size	Document Number	Rev
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**SD,MMC,MS,XD multi-function pin define**

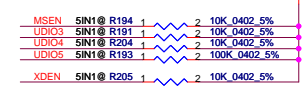
MDIO PIN Name	SD Card PIN Name	MMC Card PIN Name	MS Card PIN Name	XD Card PIN Name
MDIO00	SDCD#	MMCCD#		XDCD0#
MDIO01			MSCD#	XDCD1#
MDIO02				XDCE#
MDIO03	SDWP#			XDR/B#
MDIO04	SDPWR0	MMCPCR	MSWR	XDPWR
MDIO05	SDPWR1			XDWP#
MDIO06	SDLED#	MMCLED#	MSLED#	XDLED#
MDIO07				MSEXTCK
MDIO08	SDCCMD	MMCCMD	MSBS	XDWE#
MDIO09	SDCLK	MMCCLK	MSCLK	XDRE#
MDIO10	SDCDAT0	MMCDAT	MSDAT0	XDCDAT0
MDIO11	SDCDAT1			XDCDAT1
MDIO12	SDCDAT2			XDCDAT2
MDIO13	SDCDAT3			XDCDAT3
MDIO14				XDCDAT4
MDIO15				XDCDAT5
MDIO16				XDCDAT6
MDIO17				XDCDAT7
MDIO18				XDCLE
MDIO19				XDAL

**Function set pin define**

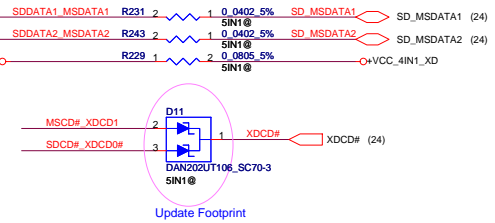
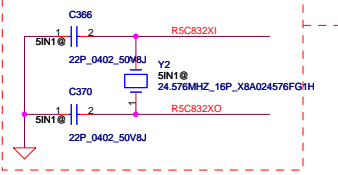
UDIO3	UDIO4	MSEN	XDEN	Function
Pull-up	Pull-up	Pull-up	Pull-up	Enable
				SD, XD, MS, MMC Card

**Layout Note: Place close to R5C832 and Shield GND for SDCLK, MSCLK**

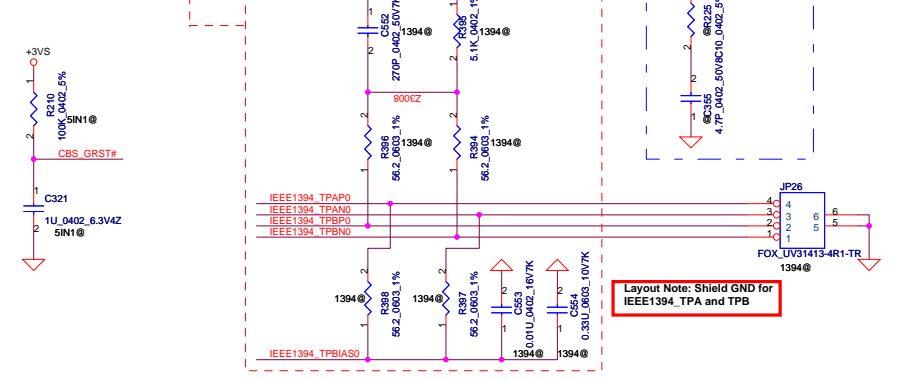
**Layout Note: Place close to R5C832 and Shield GND for SD\_CLK**



**Layout Note: Shield GND for CBS\_CCLK\_INTERNAL and CBS\_CCLK**

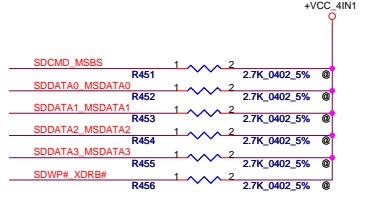
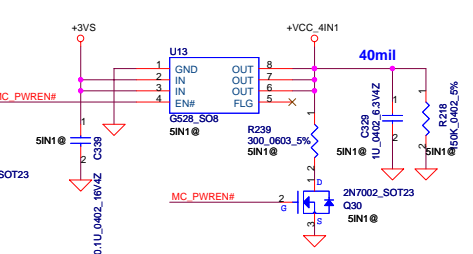


**Layout Note: Place close to R5C832**

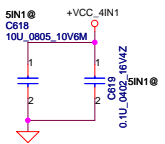
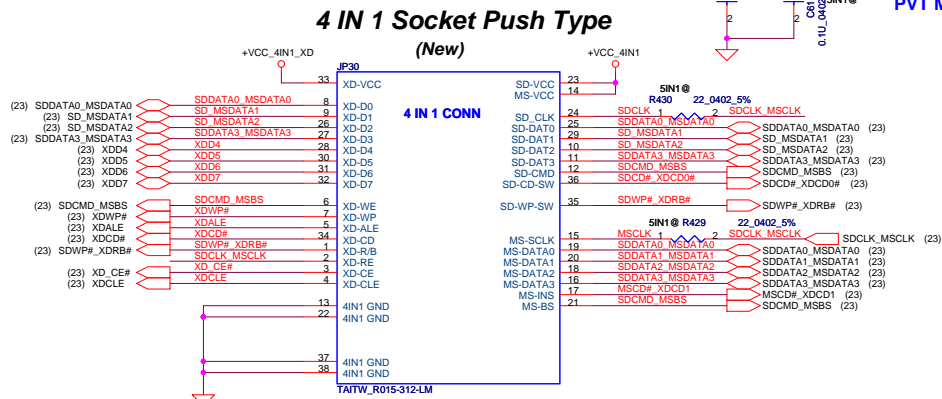


**Layout Note: Shield GND for IEEE1394\_TPA and TPB**

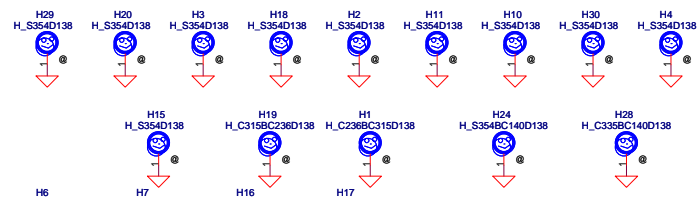
**Memory Card Power Switch**



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Issued Date	2005/10/06	Deciphered Date	2006/10/06	R5C833_1394+Card reader	
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Size	Document Number	Rev	ICW50 / ICY70 LA-3581P		
Customer	Date: Friday, April 20, 2007	Sheet	23	of	42



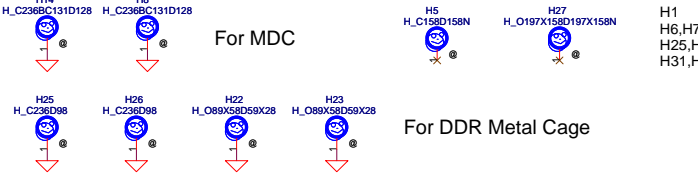
PVT Modify 2007/3/12



For CPU Support Bracket



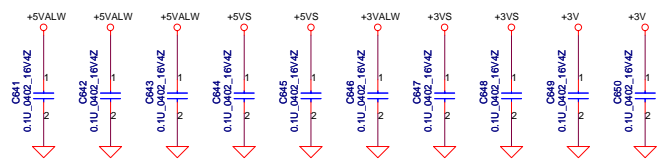
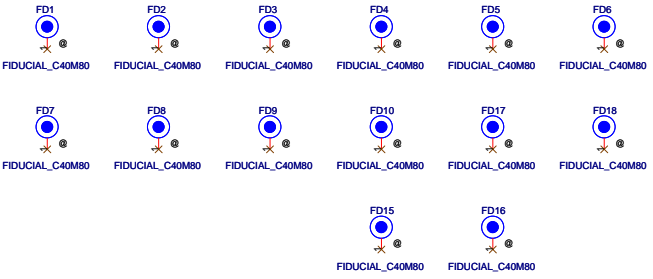
For FAN and MXM



For MDC

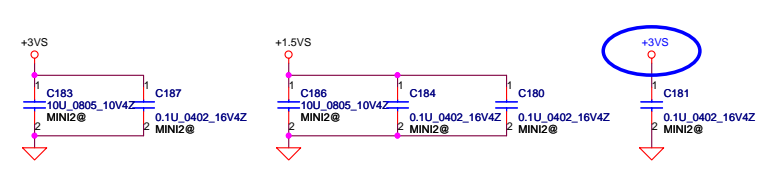
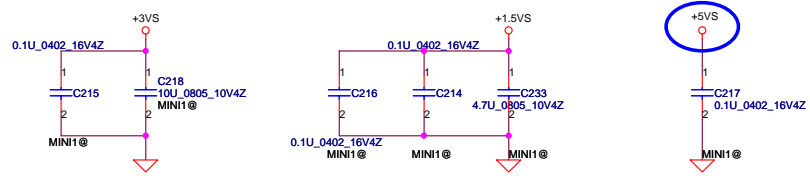
For DDR Metal Cage

H1 : H\_C236BC315D138  
H6,H7,H16,H17 : H\_C315BC168D165  
H25,H26 : H\_C236D98  
H31,H32,H33 : H\_C236BC131D128

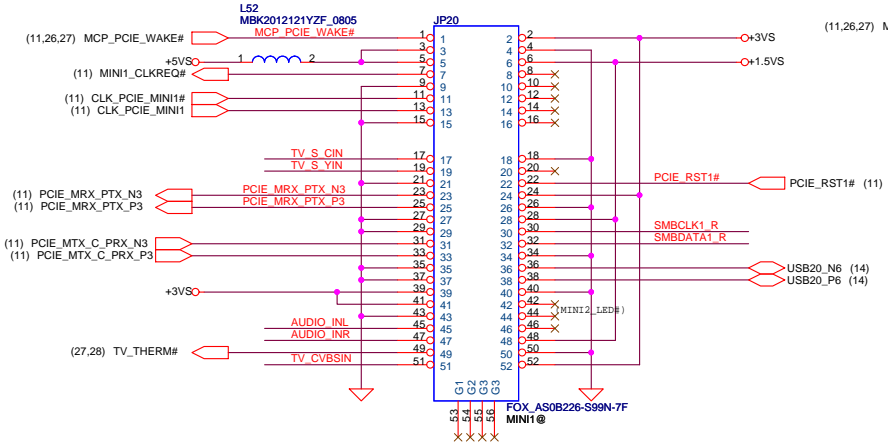


Security Classification	Compal Secret Data		Title <b>Compal Electronics, Inc.</b> Card Reader Conn / Screw
Issued Date	2005/10/06	Deciphered Date	
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			Document Number <b>ICW50 / ICY70 LA-3581P</b>
			Rev 1.0
			Date: Friday, April 20, 2007
			Sheet 24 of 42

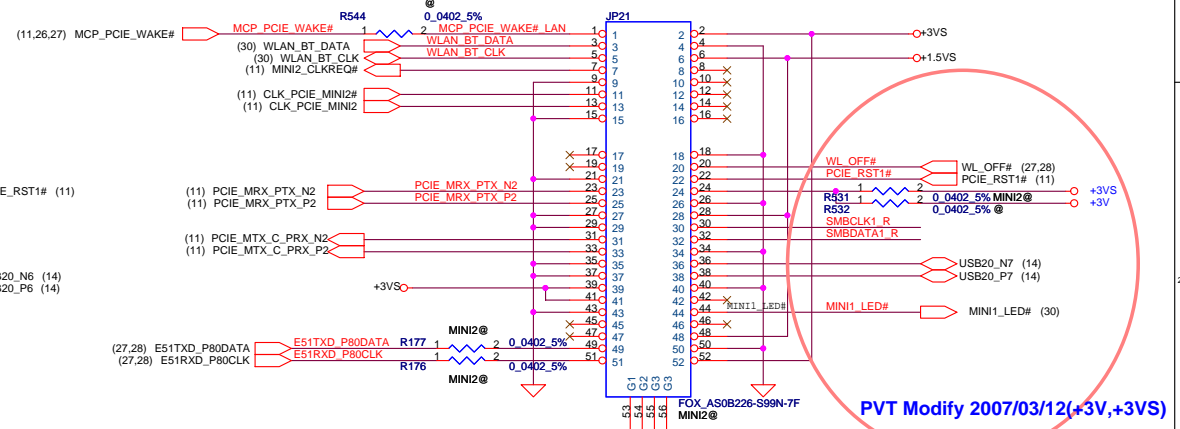




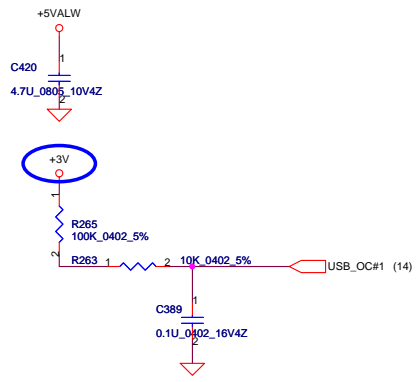
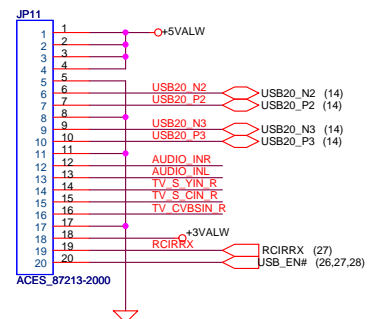
**TV TUNNER**



**PVT2 Modify 2007/04/12**

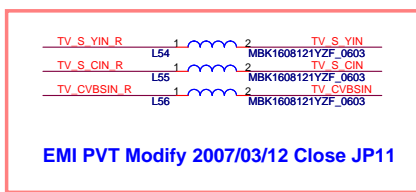


**USB/B Connector**

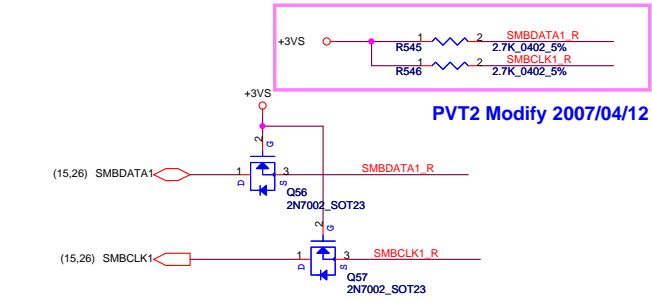


Power	Mini Card Power Rating	
	Primary Power (mA)	Auxiliary Power (mA)
	Peak	Normal
+3VS	1000	750
+3VALW	330	250 (wake enable)
+1.5VS	500	375
		5 (Not wake enable)

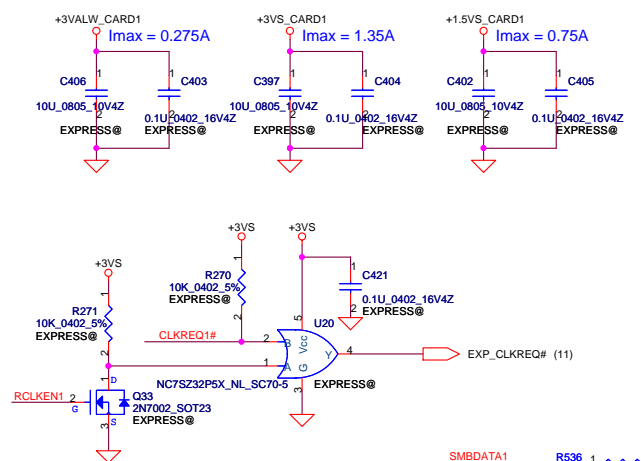
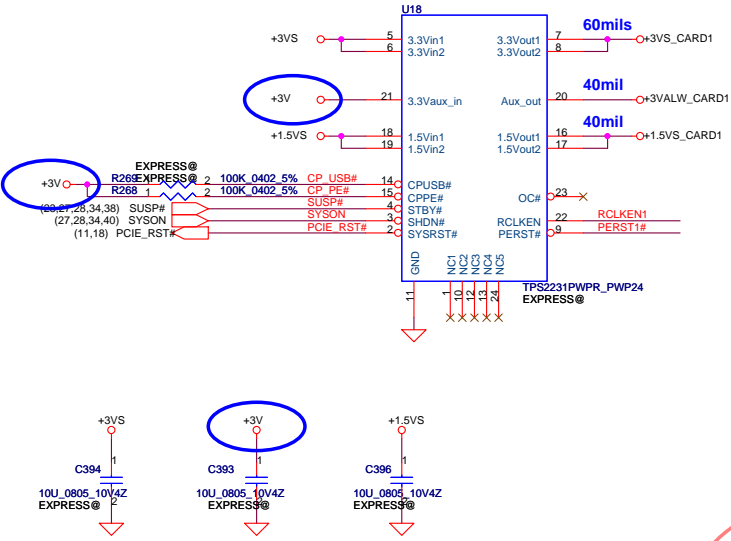
**AV-IN Connector CIR**



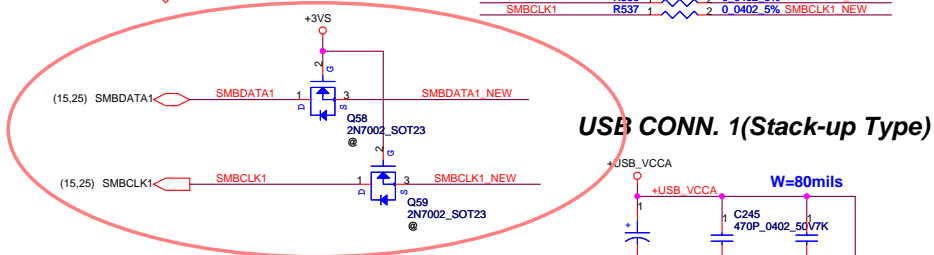
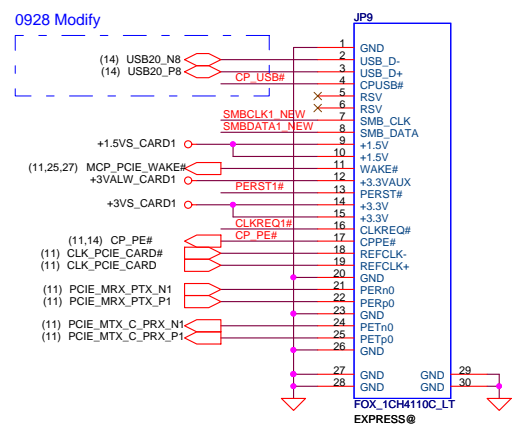
EMI PVT Modify 2007/03/12 Close JP11



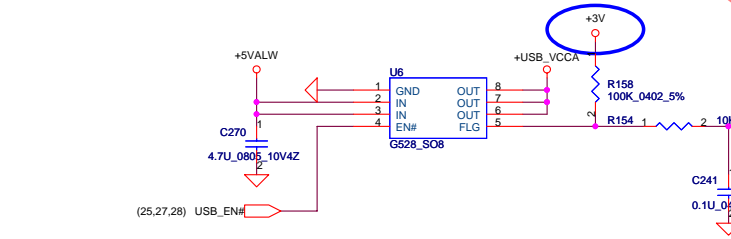
# New Card Power Switch



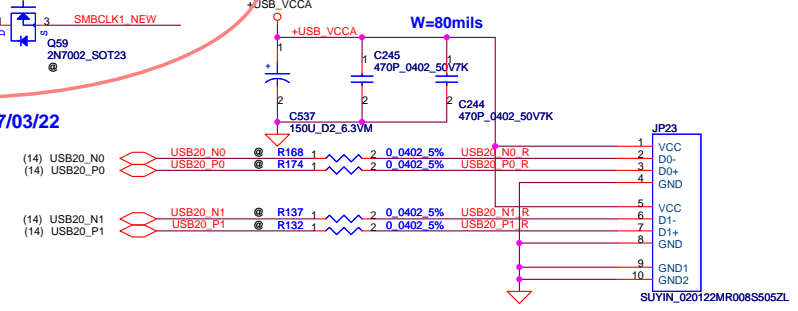
# New Card Socket (Left/TOP)



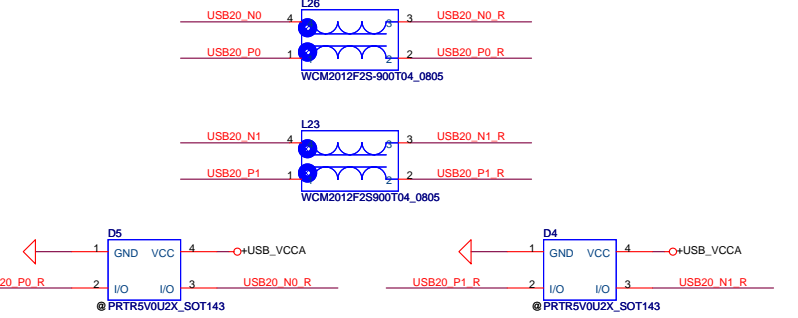
# USB CONN. 1 (Stack-up Type)



# PVT Modify 2007/03/22



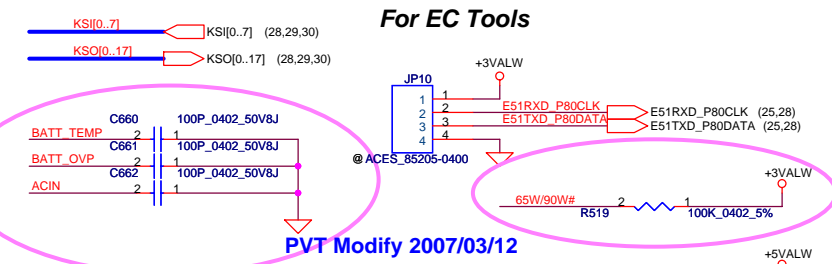
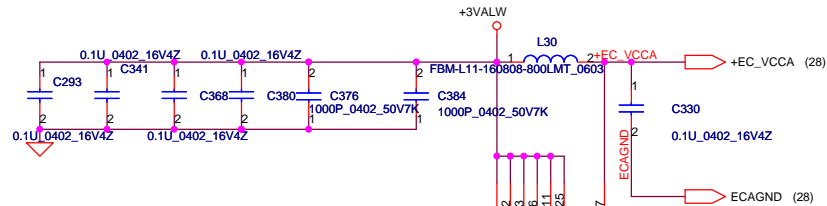
# PVT2 Modify 2007/04/11



SUYIN\_020173MR004G533ZR\_4P

SUYIN\_020173MR004G533ZR\_4P

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Title	NEW CARD & USB Connector			
Size B	Document Number	Rev	1.0	
Date:	Friday, April 20, 2007	Sheet	26	of 42



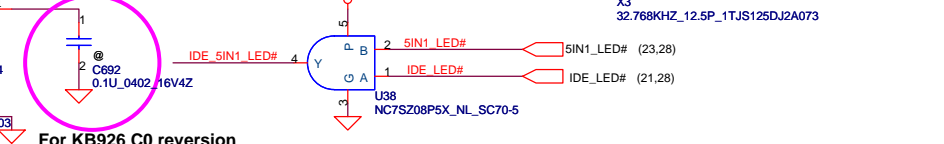
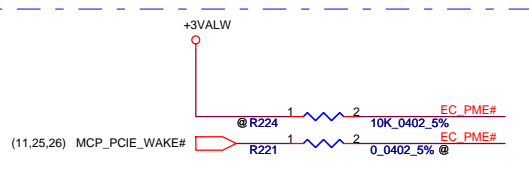
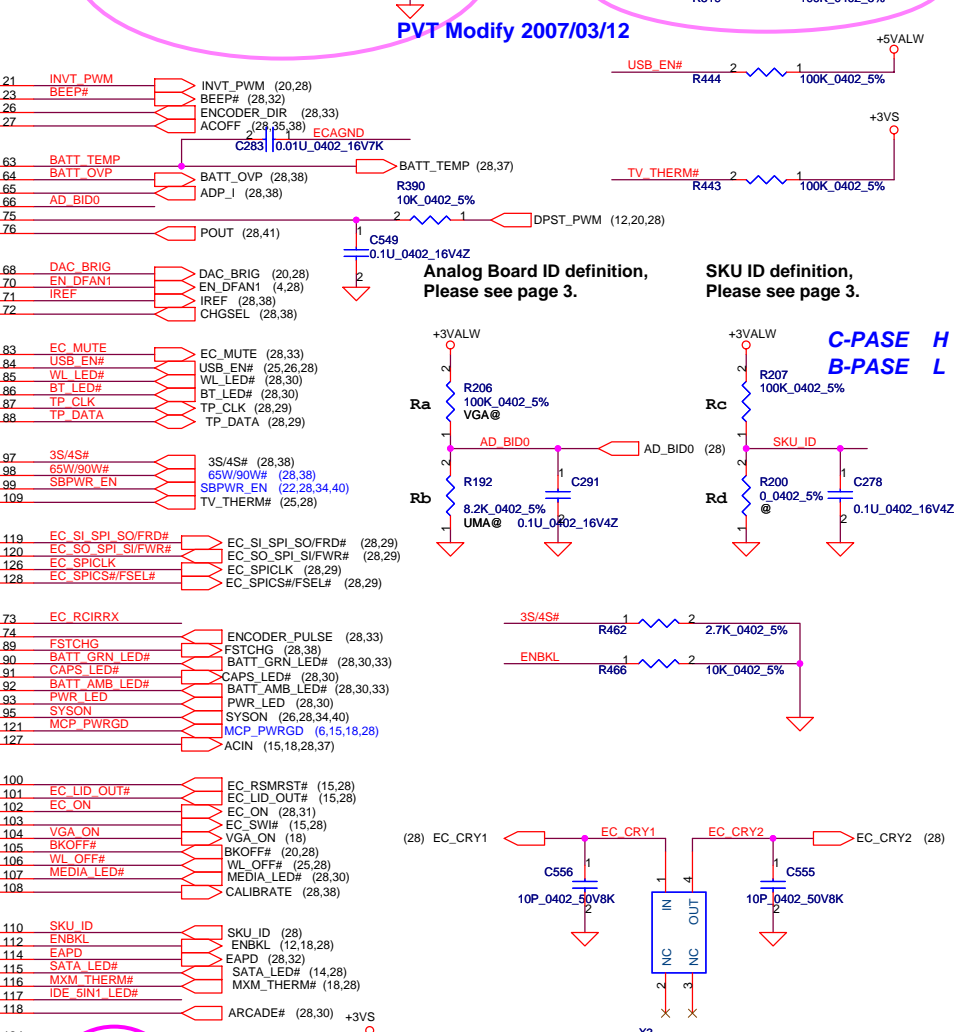
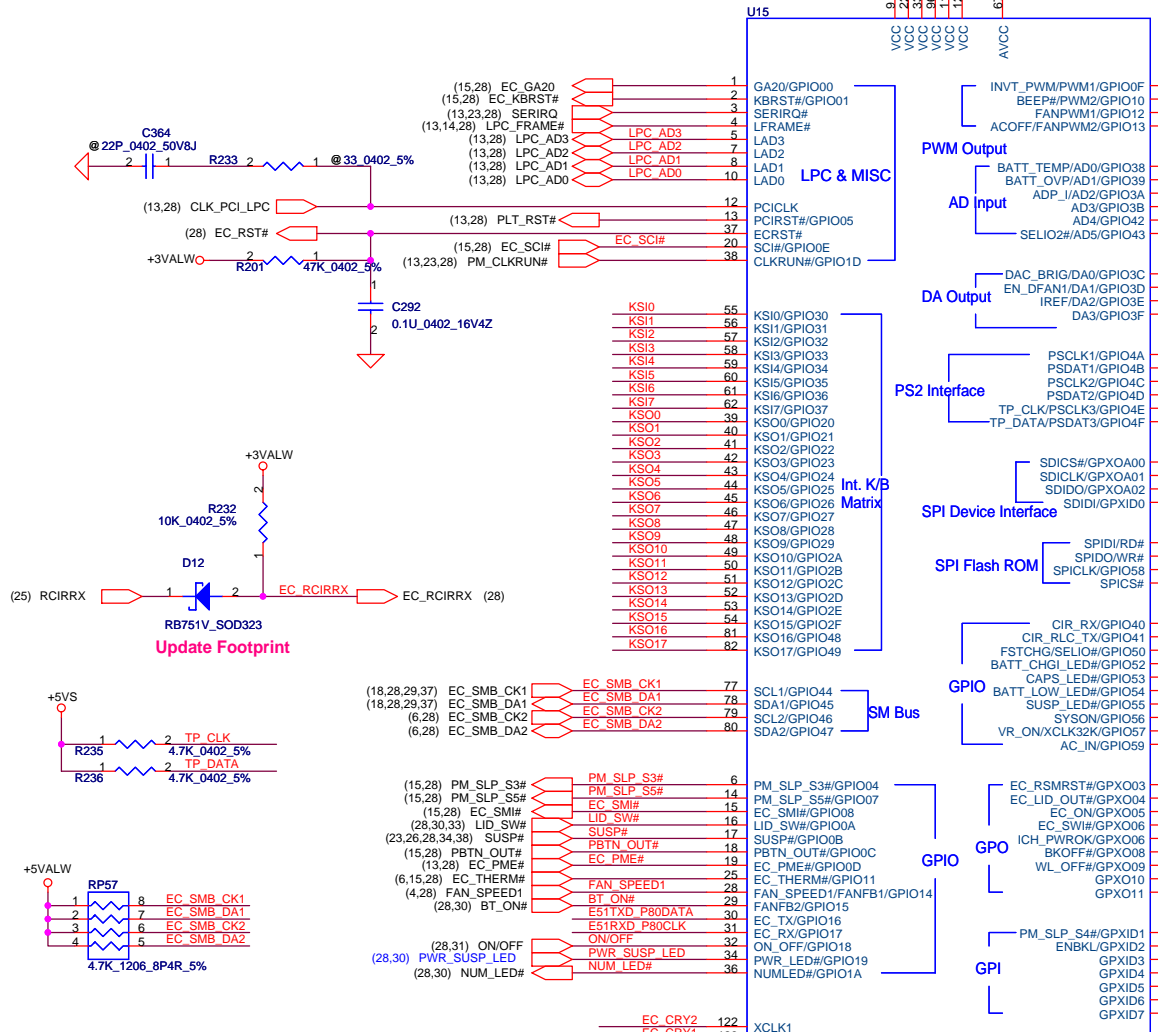
For EC Tools

PVT Modify 2007/03/12

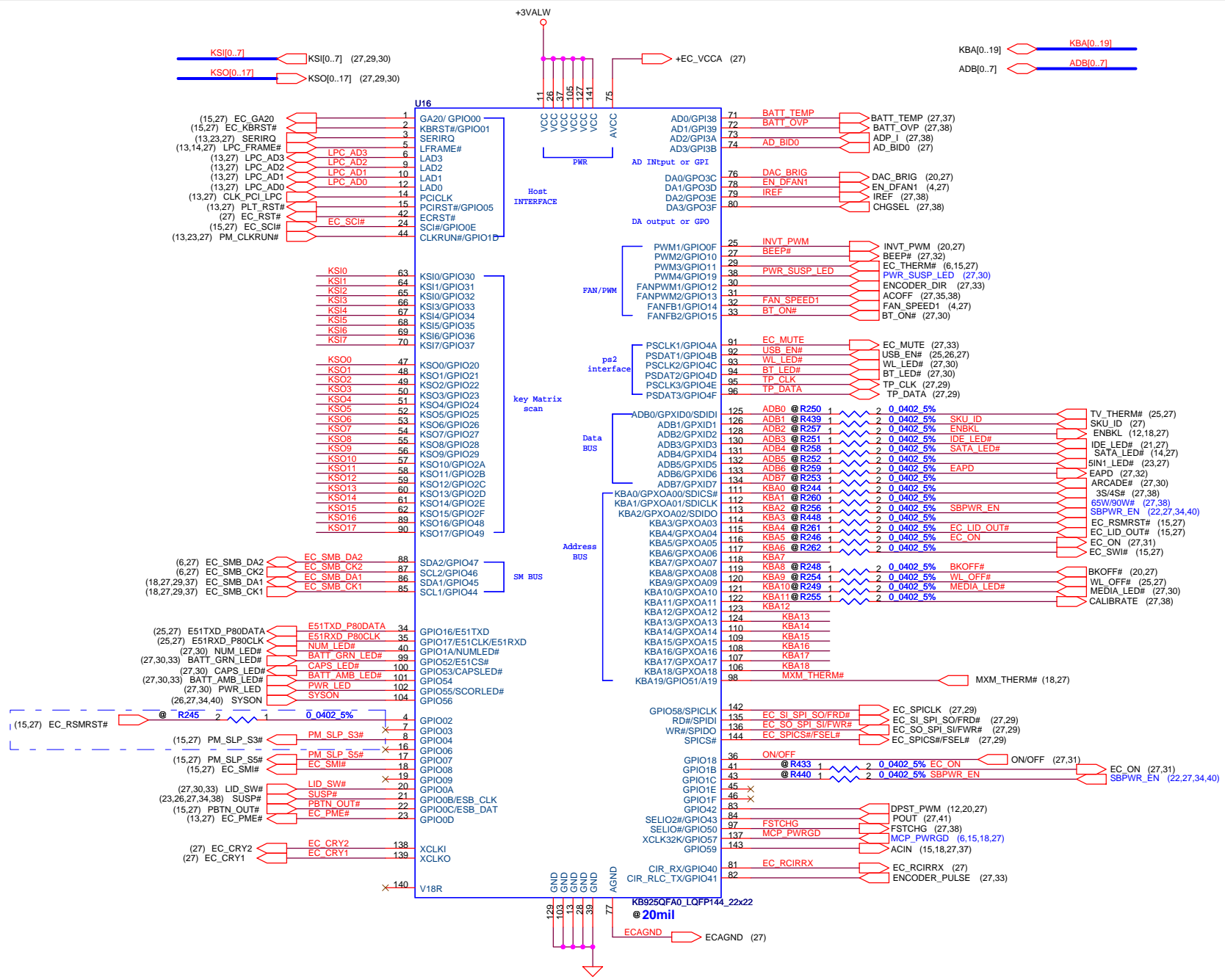
Analog Board ID definition, Please see page 3.

SKU ID definition, Please see page 3.

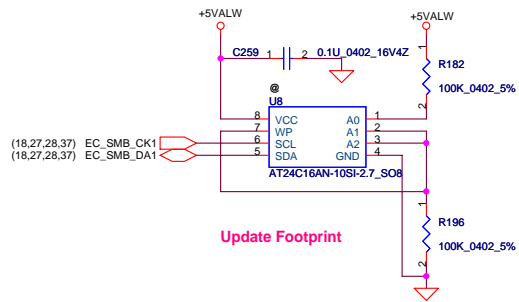
C-PASE H B-PASE L



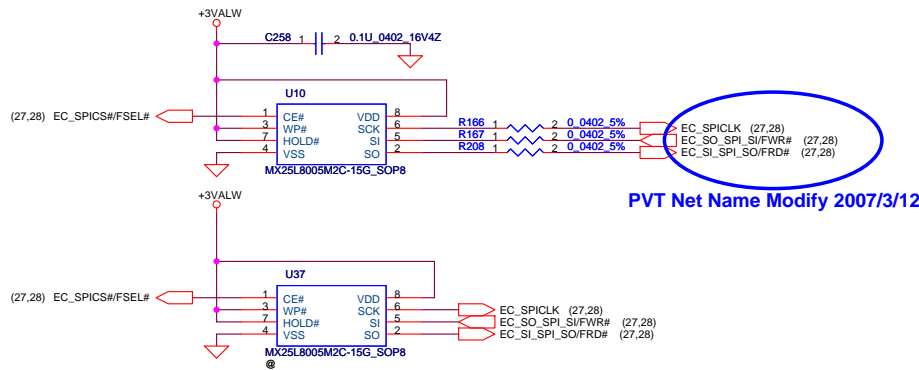
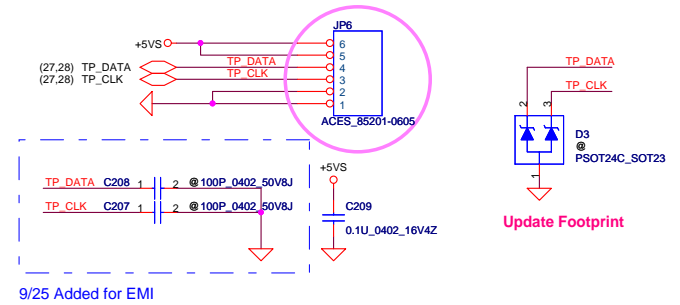
Security Classification		Compal Secret Data		Compal Electronics, Inc.	
Issued Date	2006/08/18	Deciphered Date	2007/8/18	Title	EC ENE KB926
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Size	Document Number		Rev		1.0
Date:	Friday, April 20, 2007	Sheet	27	of	42



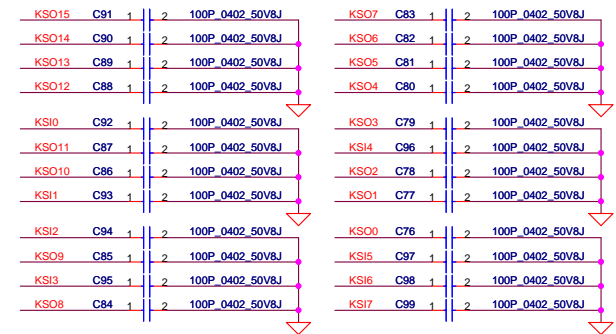
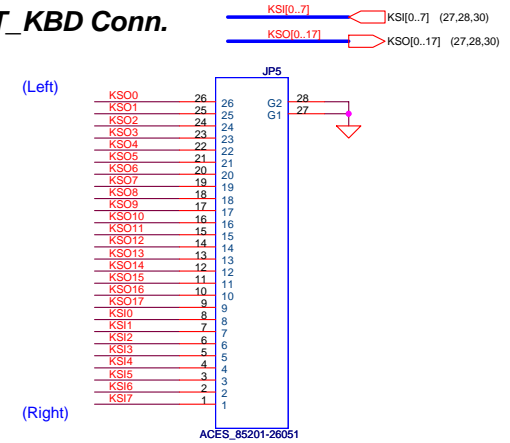
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Issued Date	2006/08/18	Deciphered Date	2007/8/18	Title	
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Size	Document Number			Rev	1.0
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To TP/B Conn.



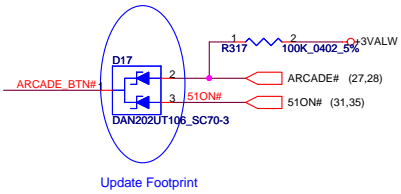
INT\_KBD Conn.



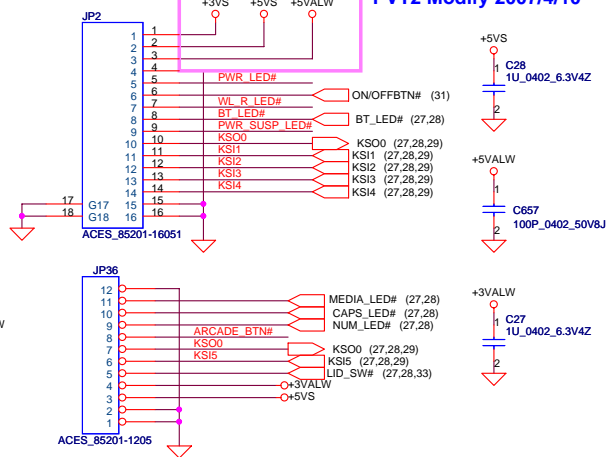
Security Classification		Compal Secret Data		Compal Electronics, Inc.	
Issued Date	2006/08/18	Deciphered Date	2007/8/18	Title	BIOS, I/O Port & K/B Connector
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	<b>KSO0</b>
KSI1	WL_BTN#
KSI2	BT_BTN#
KSI3	EMAIL_BTN#
KSI4	IE_BTN#
KSI5	E-KEY_BTN#

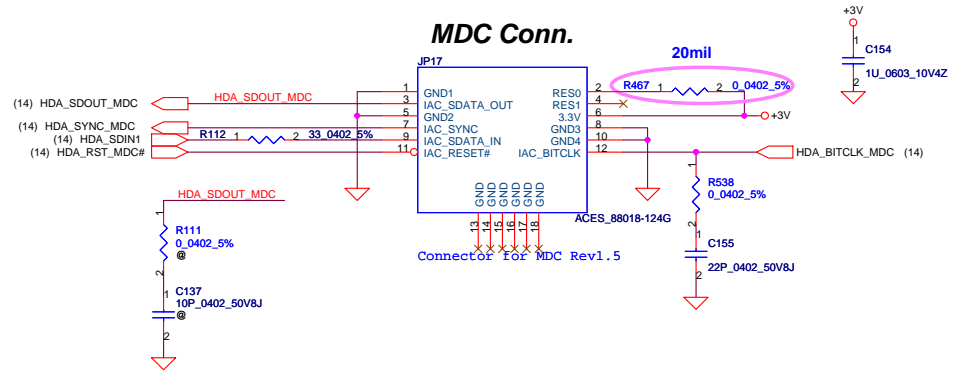
Check 15.4" K/B Matrix



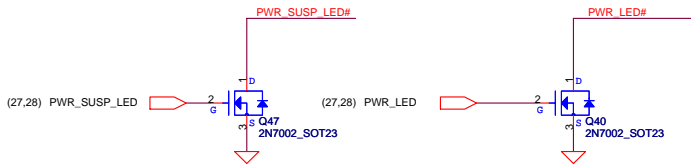
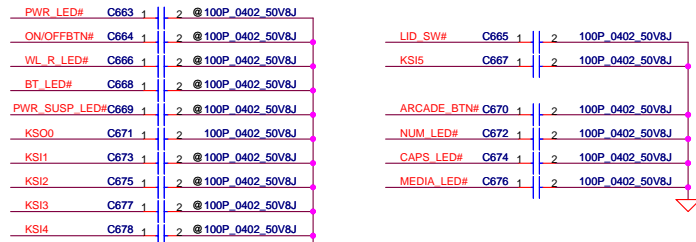
**PVT2 Modify 2007/4/10**



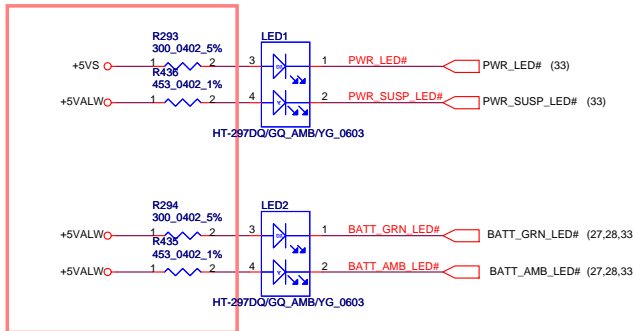
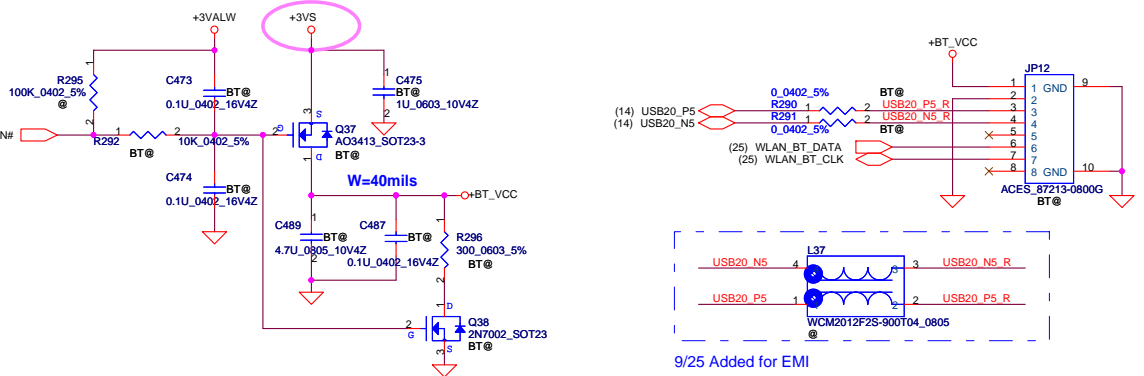
**MDC Conn.**



**EMI PVT Modify 2007/3/12**

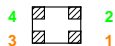


**Bluetooth Conn.**



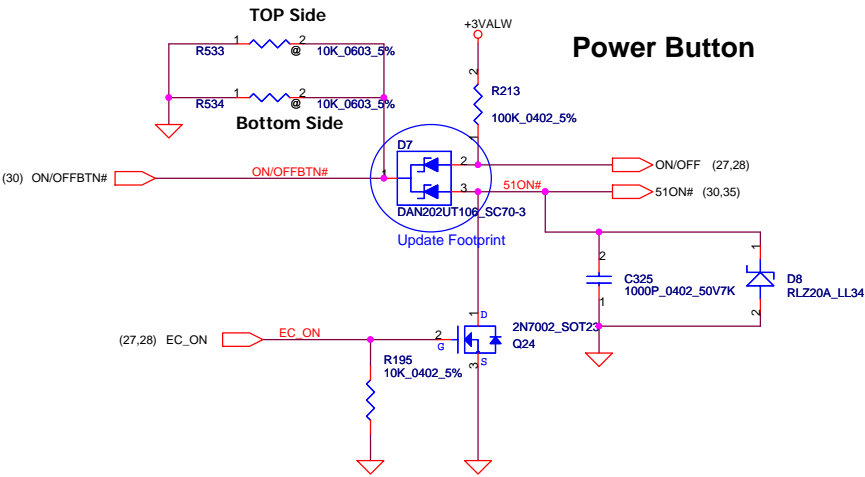
PVT Value Modify to 453E 2007/3/12

Compal Footprint

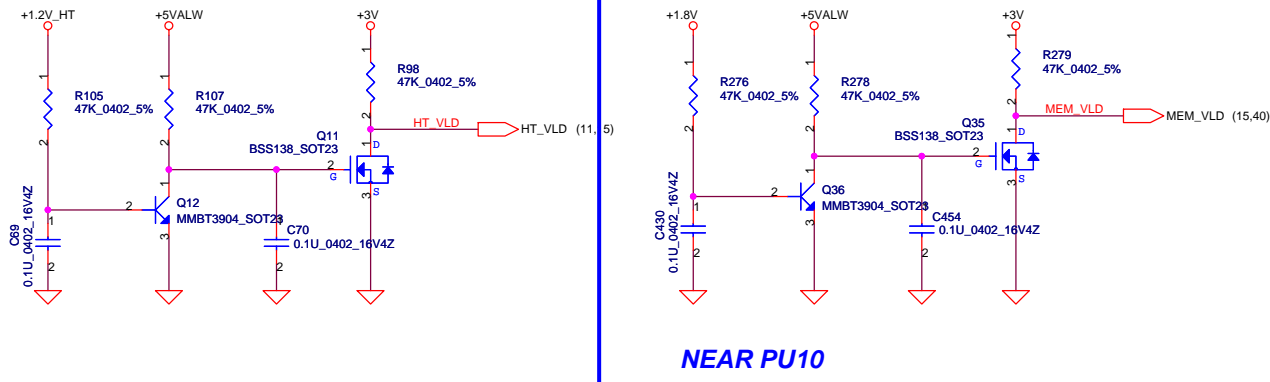


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Title	MDC / BT / CIR / LED			
Size	Document Number	Rev		1.0
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Date:	Friday, April 20, 2007	Sheet	30	of 42

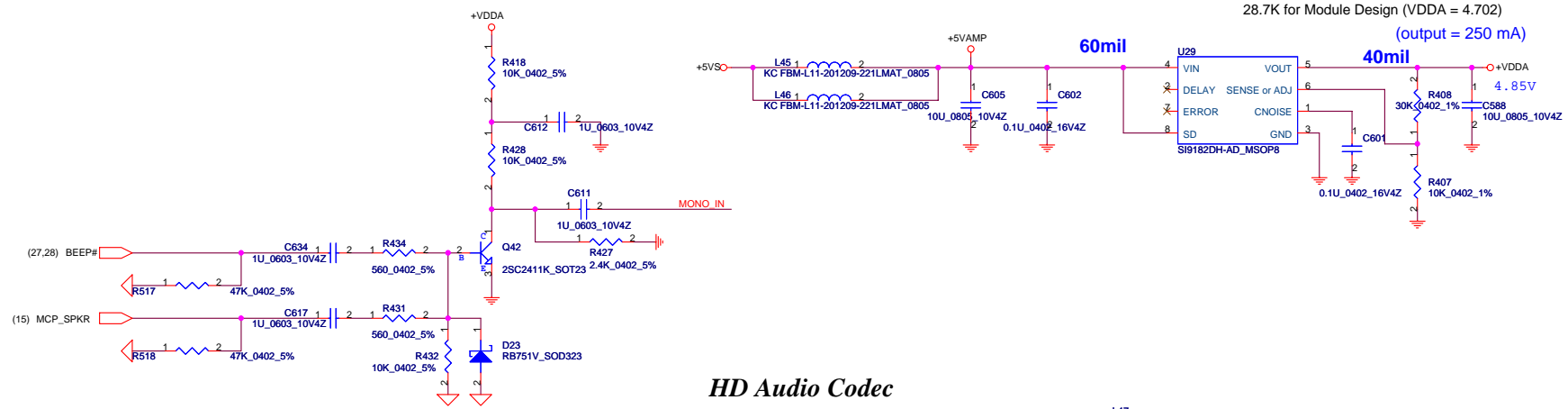


### Power ON Circuit

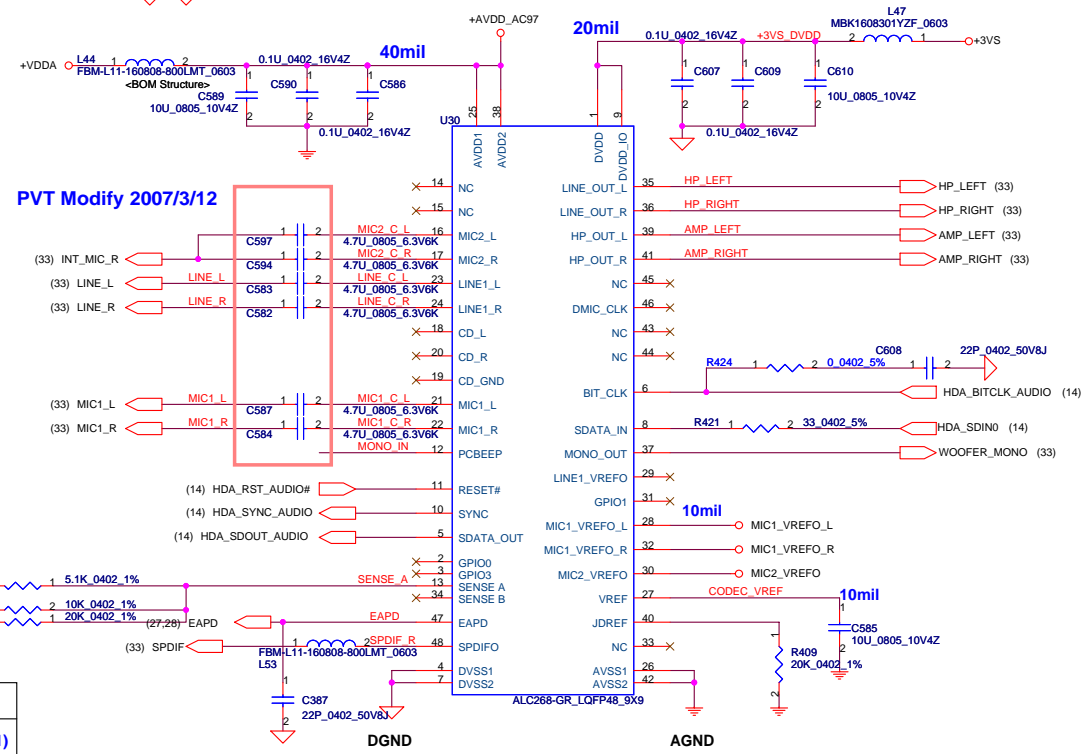


**NEAR PU10**

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				Document Number
				ICW50 / ICY70 LA-3581P
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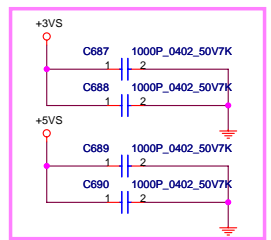
### HD Audio Codec



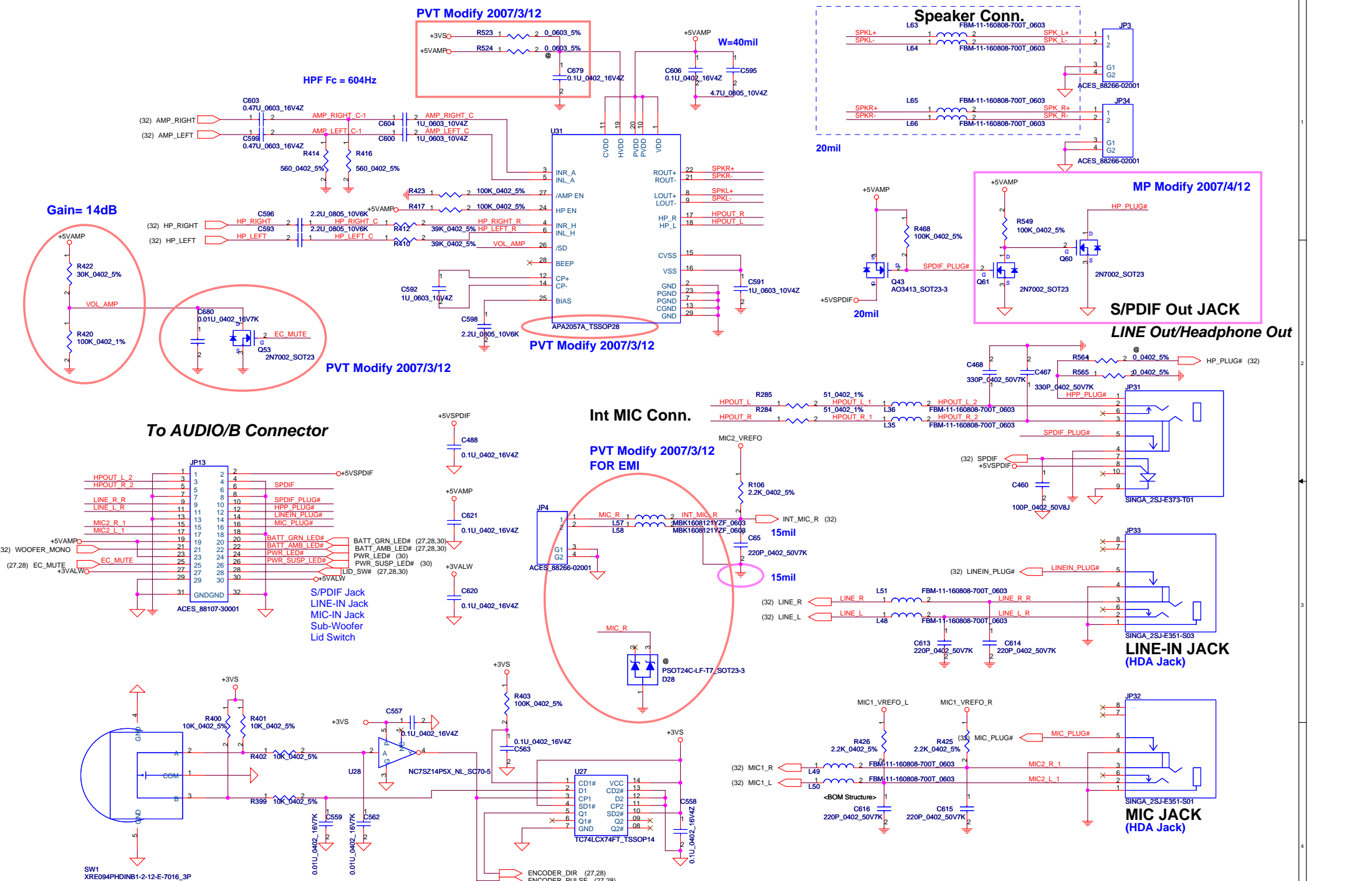
PVT Modify 2007/3/12

EMI Added 2007/4/12

Sense Pin	Impedance	Codec Signals
SENSE A	39.2K	PORT-A (PIN 39, 41)
	20K	PORT-B (PIN 21, 22)
	10K	PORT-C (PIN 23, 24)
	5.1K	PORT-D (PIN 35, 36)
SENSE B	39.2K	PORT-E (PIN 14, 15)
	20K	PORT-F (PIN 16, 17)
	10K	PORT-G (PIN 43, 44)
	5.1K	PORT-H (PIN 45, 46)



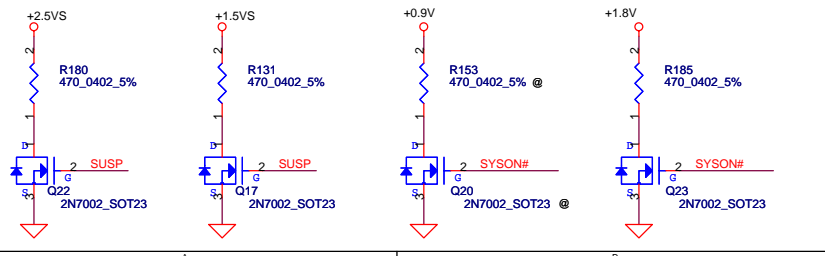
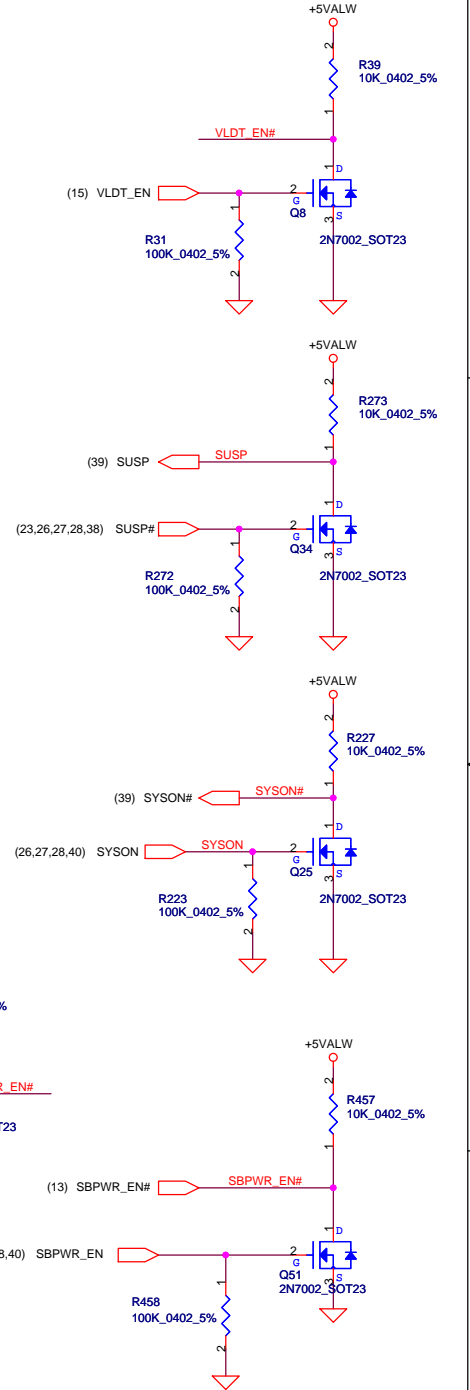
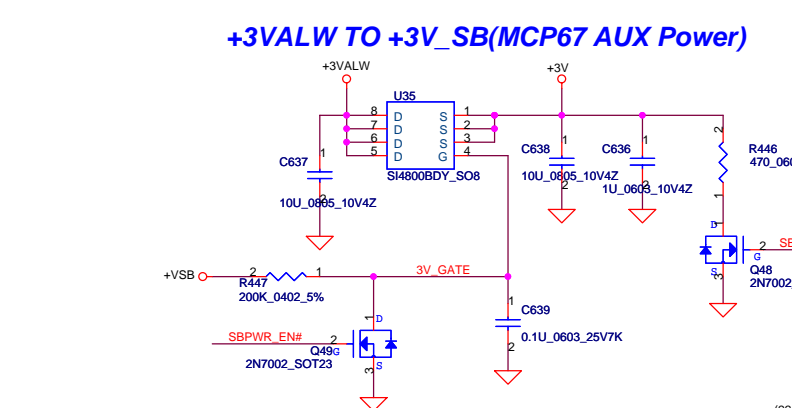
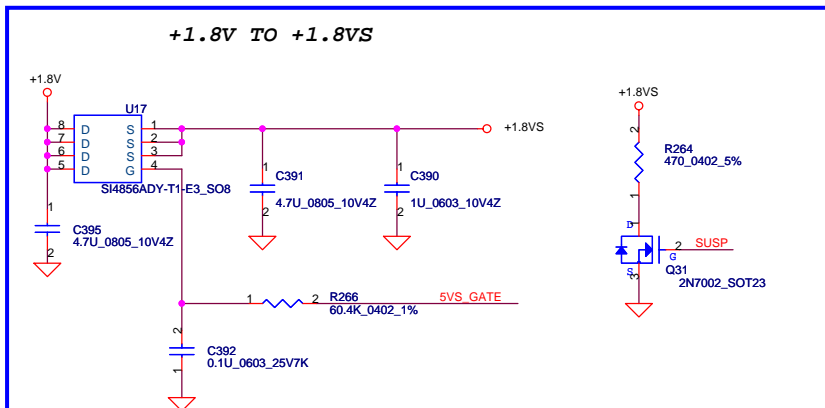
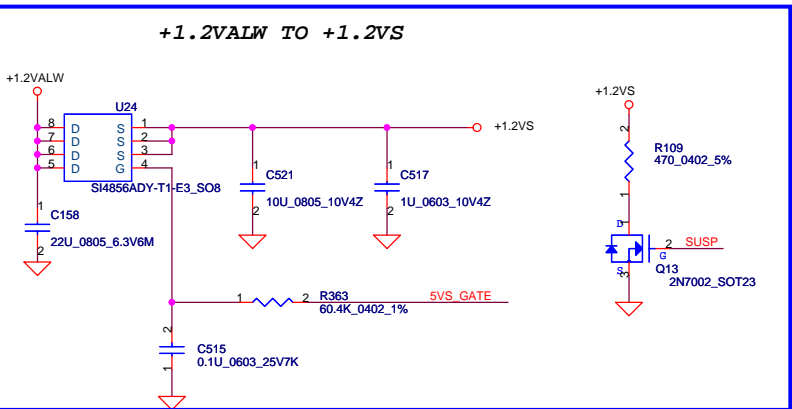
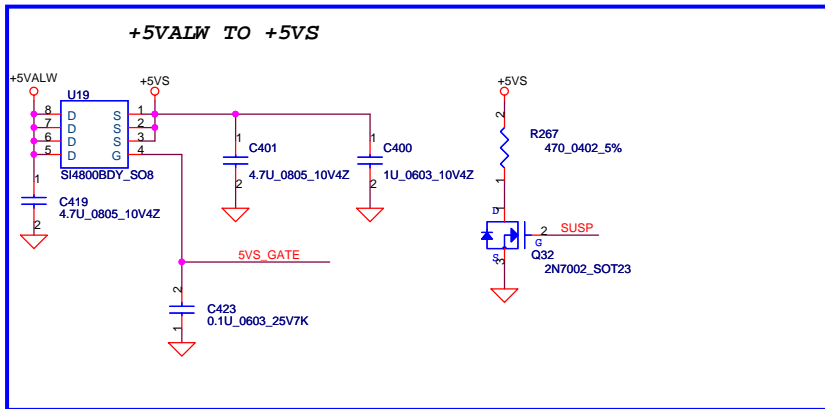
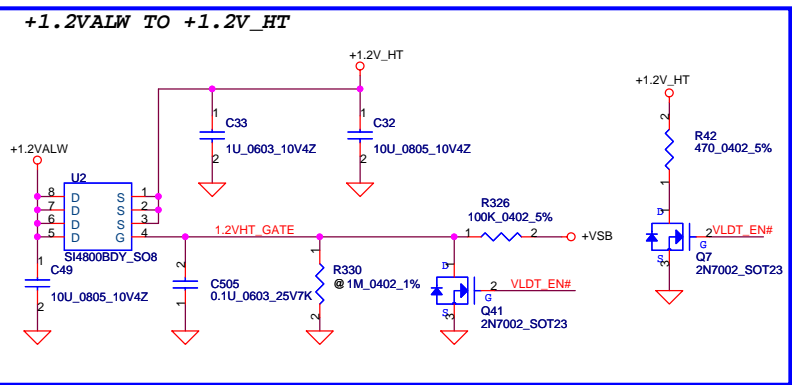
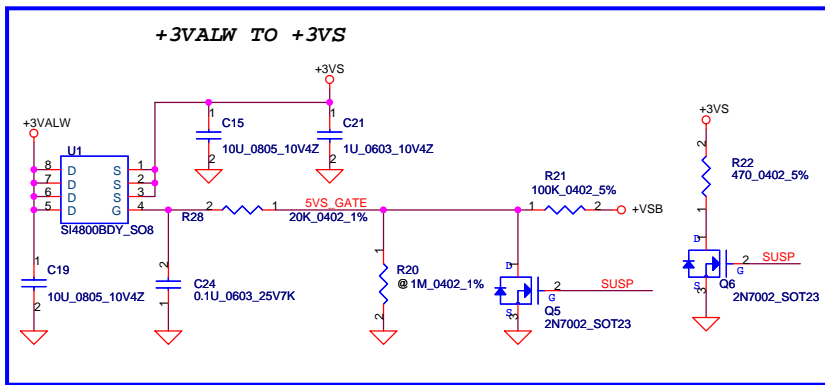




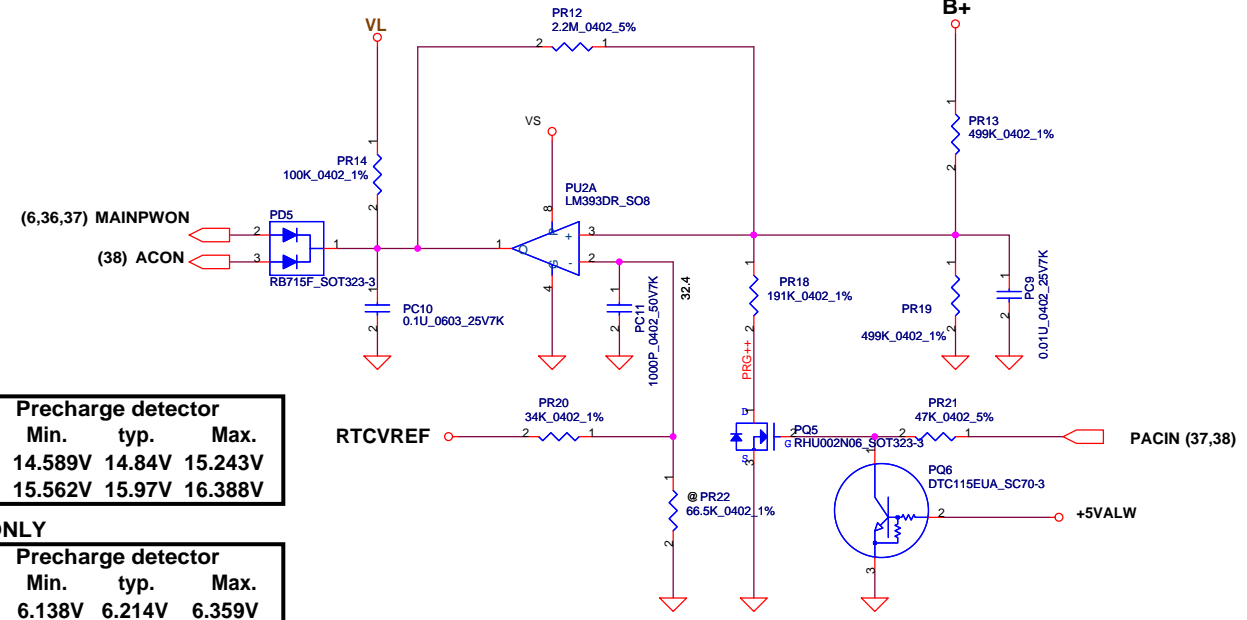
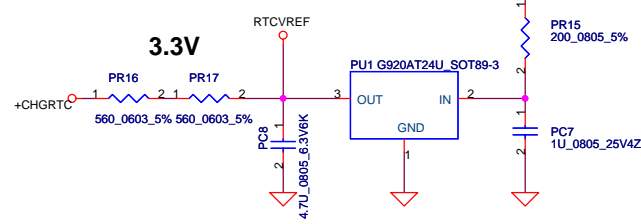
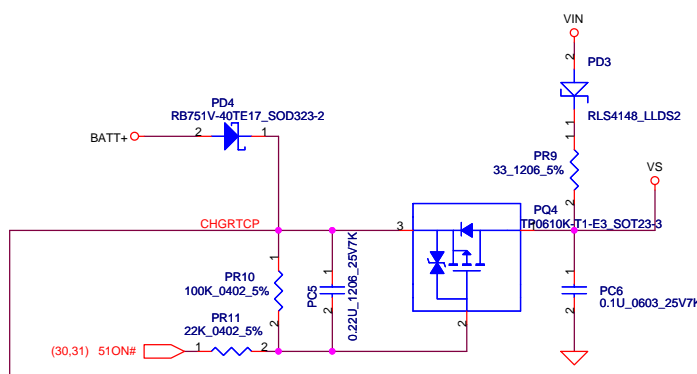
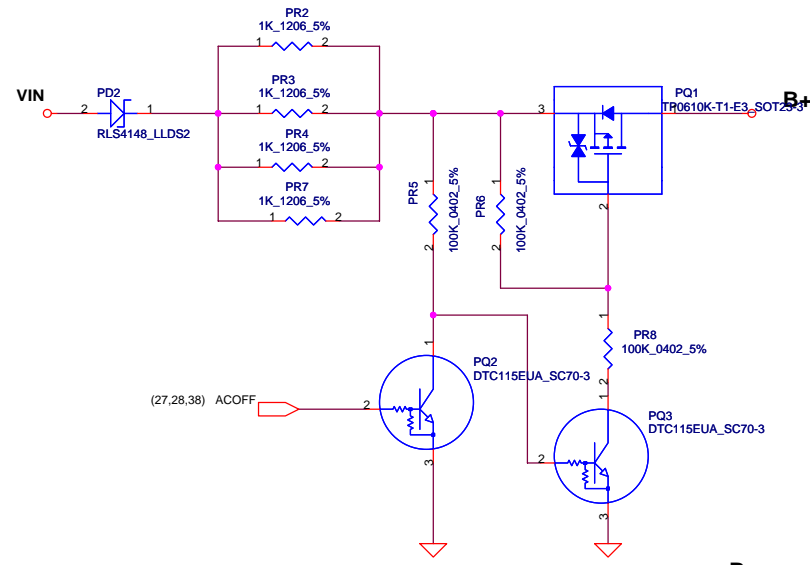
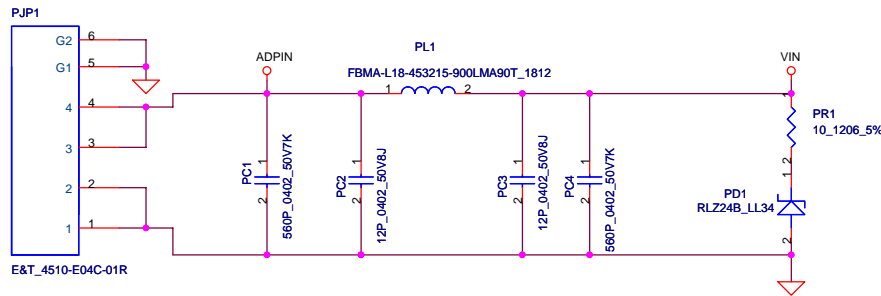
Security Classification	Compal Secret Data	
Issued Date	2006/08/18	Deciphered Date
		2007/8/18

Compal Electronics, Inc.		
Title <b>Amplifier &amp; Audio Jack</b>		
Size B	Document Number <b>ICW50 / ICY70 LA-3581P</b>	Rev 1.0
Date:	Friday, April 20, 2007	Sheet 33 of 42

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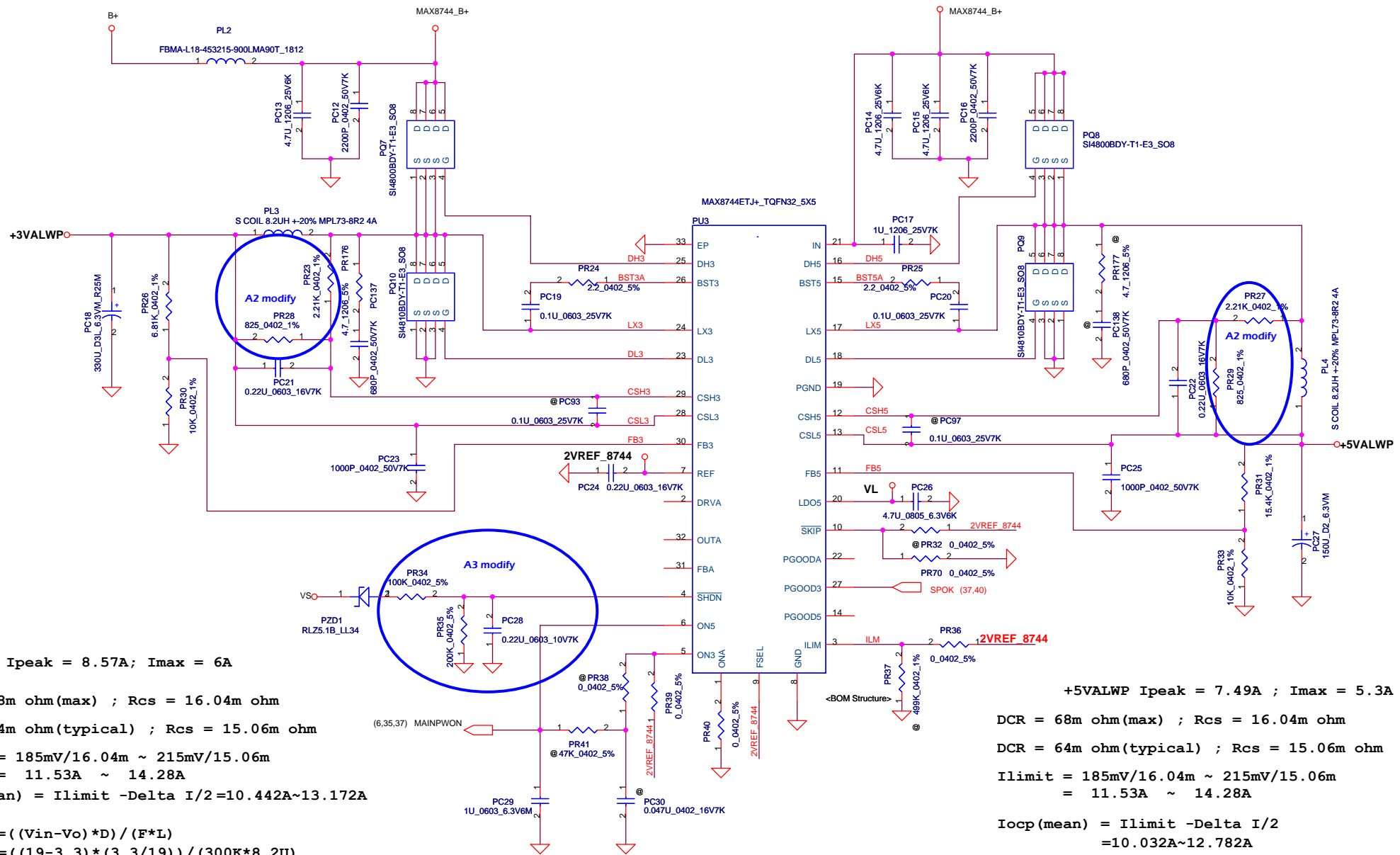
**ACIN**

	Precharge detector		
	Min.	typ.	Max.
H-->L	14.589V	14.84V	15.243V
L-->H	15.562V	15.97V	16.388V

**BATT ONLY**

	Precharge detector		
	Min.	typ.	Max.
H-->L	6.138V	6.214V	6.359V
L-->H	7.196V	7.349V	7.505V

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+3VALWP Ipeak = 8.57A; Imax = 6A

DCR = 68m ohm(max) ; Rcs = 16.04m ohm

DCR = 64m ohm(typical) ; Rcs = 15.06m ohm

Ilimit = 185mV/16.04m ~ 215mV/15.06m  
= 11.53A ~ 14.28A

Iocp(mean) = Ilimit -Delta I/2 = 10.442A~13.172A

$$\Delta I = ((V_{in} - V_o) * D) / (F * L)$$

$$= ((19 - 3.3) * (3.3/19)) / (300K * 8.2U)$$

$$= 1.108A$$

Notes :

$$f_{ESR} \leq f_{OSC} / \pi ; f_{ESR} = 1 / (2 * \pi * RESR * COUT)$$

ON3 = REF ---> 3.3V starts up delay 2ms after 5V starts up

+5VALWP Ipeak = 7.49A ; Imax = 5.3A

DCR = 68m ohm(max) ; Rcs = 16.04m ohm

DCR = 64m ohm(typical) ; Rcs = 15.06m ohm

Ilimit = 185mV/16.04m ~ 215mV/15.06m  
= 11.53A ~ 14.28A

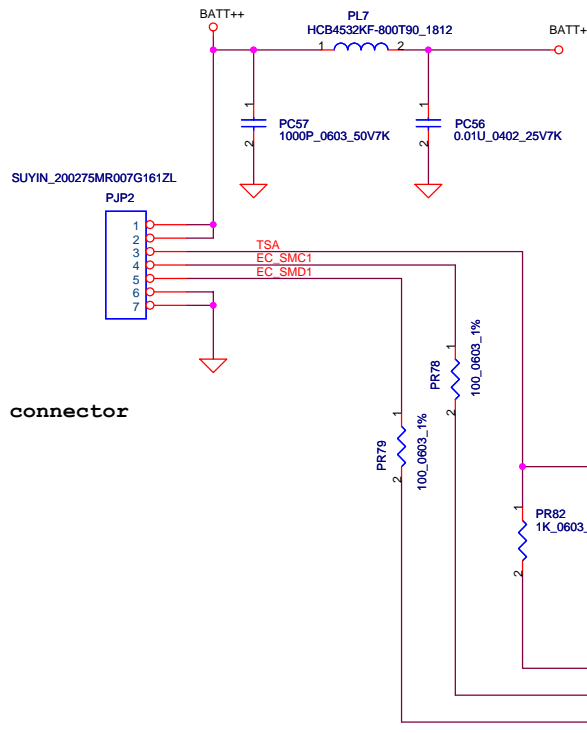
Iocp(mean) = Ilimit -Delta I/2  
= 10.032A~12.782A

$$\Delta I = ((V_{in} - V_o) * D) / (F * L)$$

$$= ((19 - 5) * (5/19)) / (300K * 8.2U)$$

$$= 1.498A$$

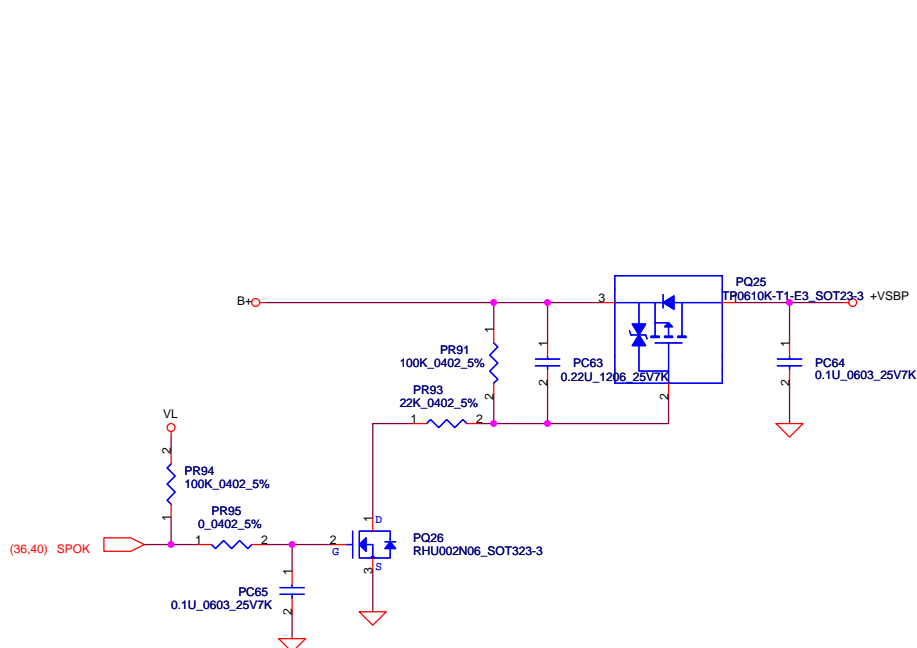
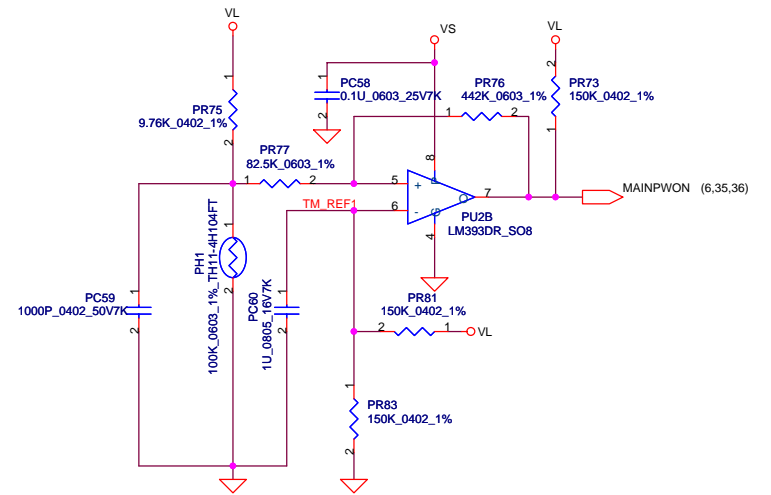
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**PJP2 battery connector**

- SMART Battery:**
1. BATT+
  2. BATT+
  3. TS
  4. SMC
  5. SMD
  6. GND
  7. GND

PH1 under CPU bottom side :  
 CPU thermal protection at 90 degree C  
 Recovery at 70 degree C



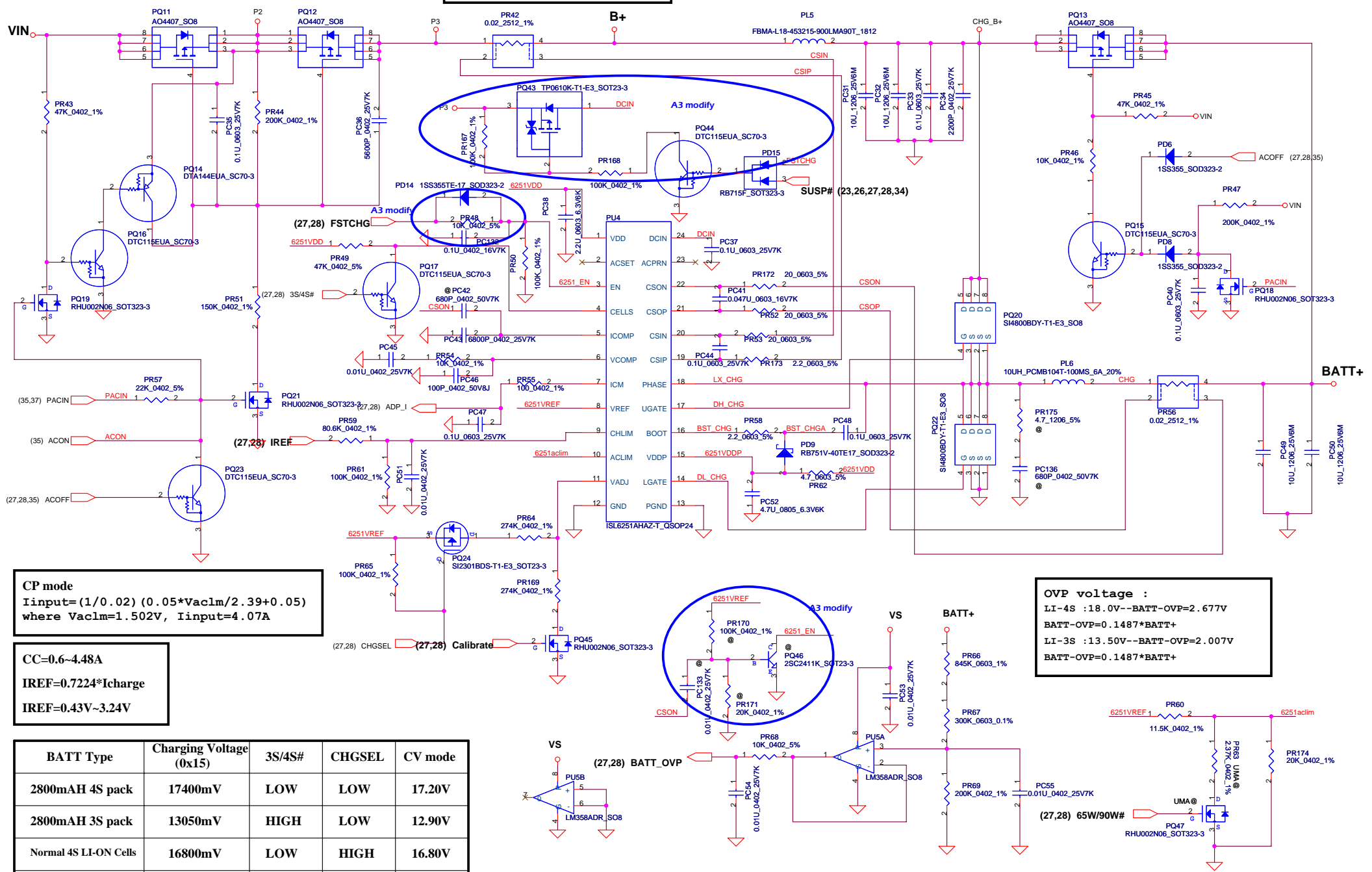
	Min.	typ.	Max.
H-->L	16.976V	17.257V	17.728V
L-->H	17.430V	17.901V	18.384V

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Iada=0~4.74A (90W)

$ADP\_I = 19.9 * I_{adapter} * R_{sense}$

$CP = 85\% * I_{ada} ; CP = 4.07A$



**CP mode**  
 $I_{input} = (1/0.02) (0.05 * V_{aclm} / 2.39 + 0.05)$   
 where  $V_{aclm} = 1.502V$ ,  $I_{input} = 4.07A$

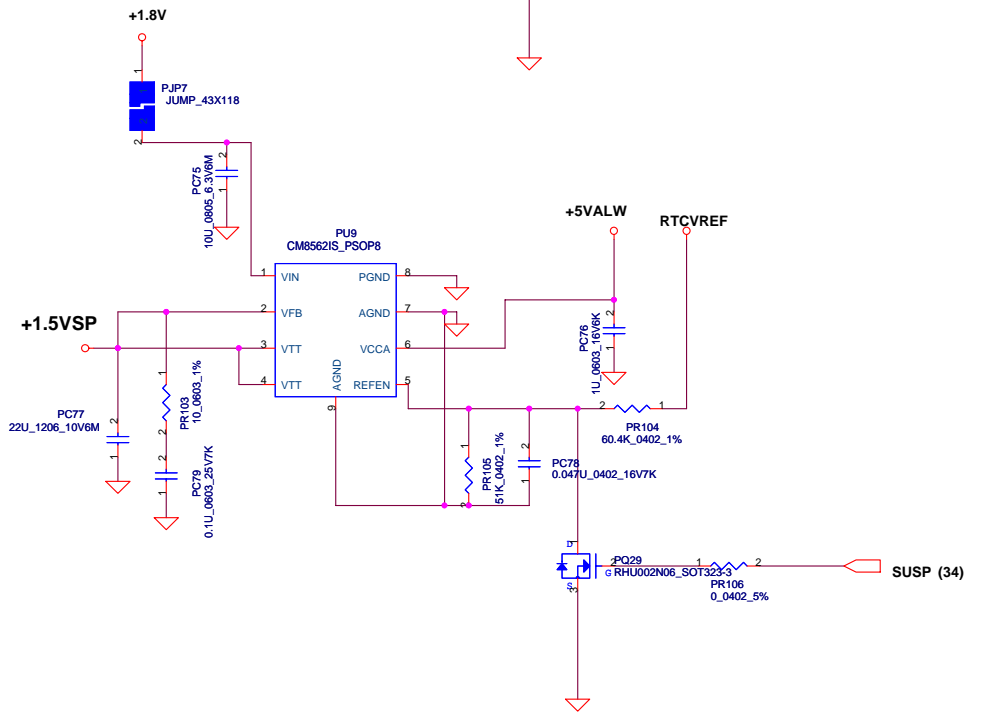
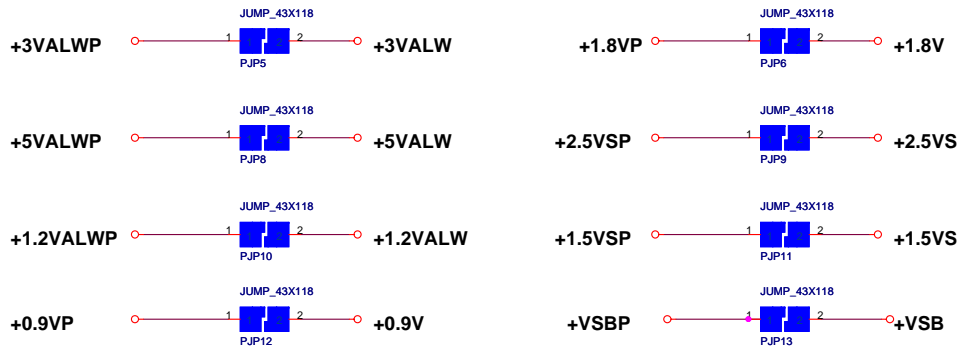
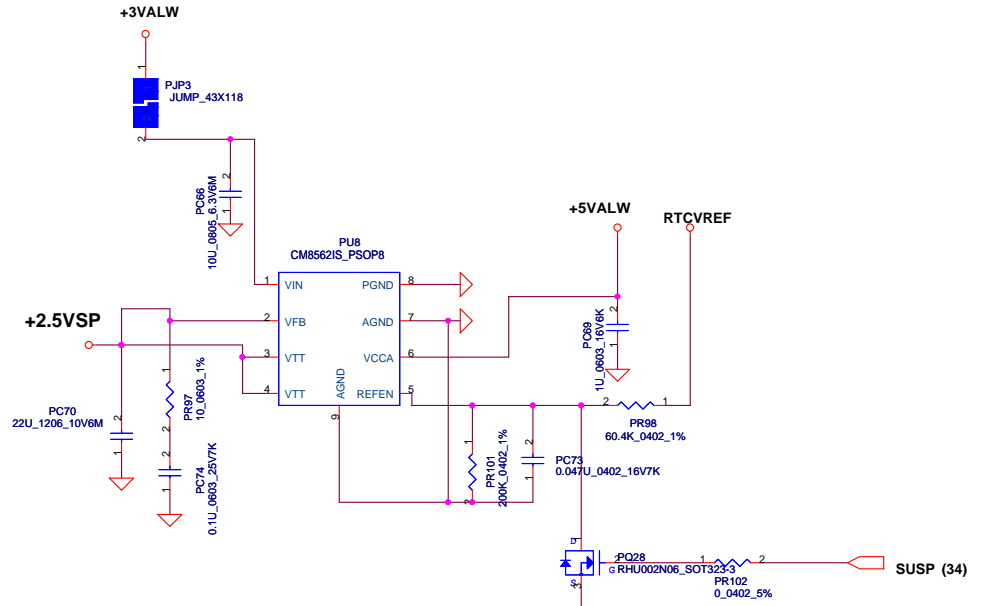
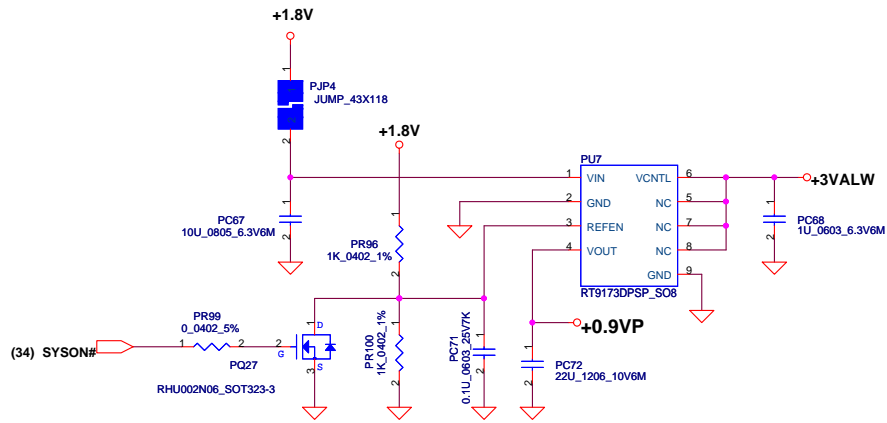
**CC=0.6~4.48A**  
 $I_{REF} = 0.7224 * I_{charge}$   
 $I_{REF} = 0.43V \sim 3.24V$

**OVP voltage :**  
 LI-4S : 18.0V -- BATT-OVP = 2.677V  
 $BATT-OVP = 0.1487 * BATT+$   
 LI-3S : 13.50V -- BATT-OVP = 2.007V  
 $BATT-OVP = 0.1487 * BATT+$

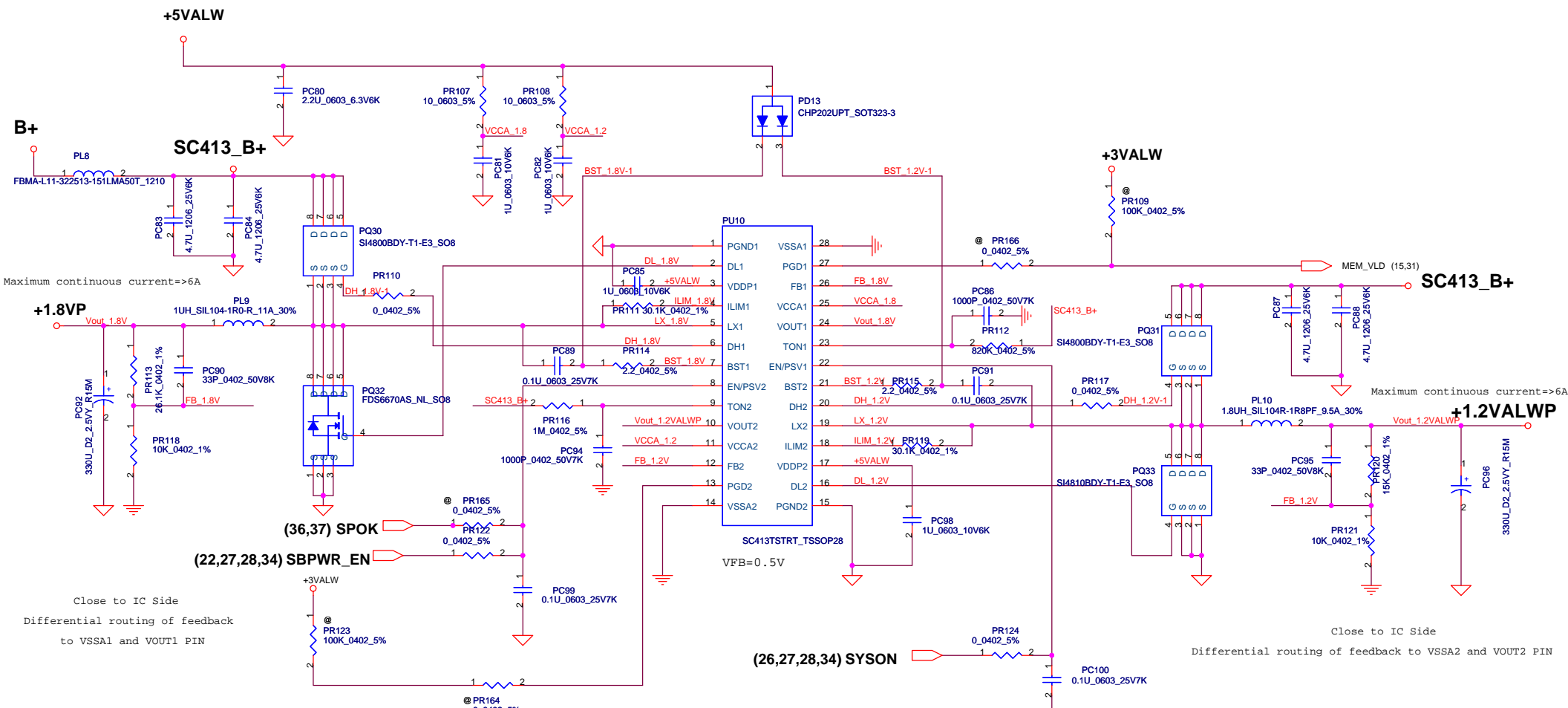
BATT Type	Charging Voltage (0x15)	3S/4S#	CHGSEL	CV mode
2800mAH 4S pack	17400mV	LOW	LOW	17.20V
2800mAH 3S pack	13050mV	HIGH	LOW	12.90V
Normal 4S LI-ON Cells	16800mV	LOW	HIGH	16.80V
Normal 3S LI-ON Cells	12600mV	HIGH	HIGH	12.60V
Wake up charge while no communication	-	HIGH	HIGH	12.60V

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<b>CHARGER</b>			
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Maximum continuous current=>6A

Maximum continuous current=>6A

Close to IC Side  
Differential routing of feedback  
to VSSA1 and VOUT1 PIN

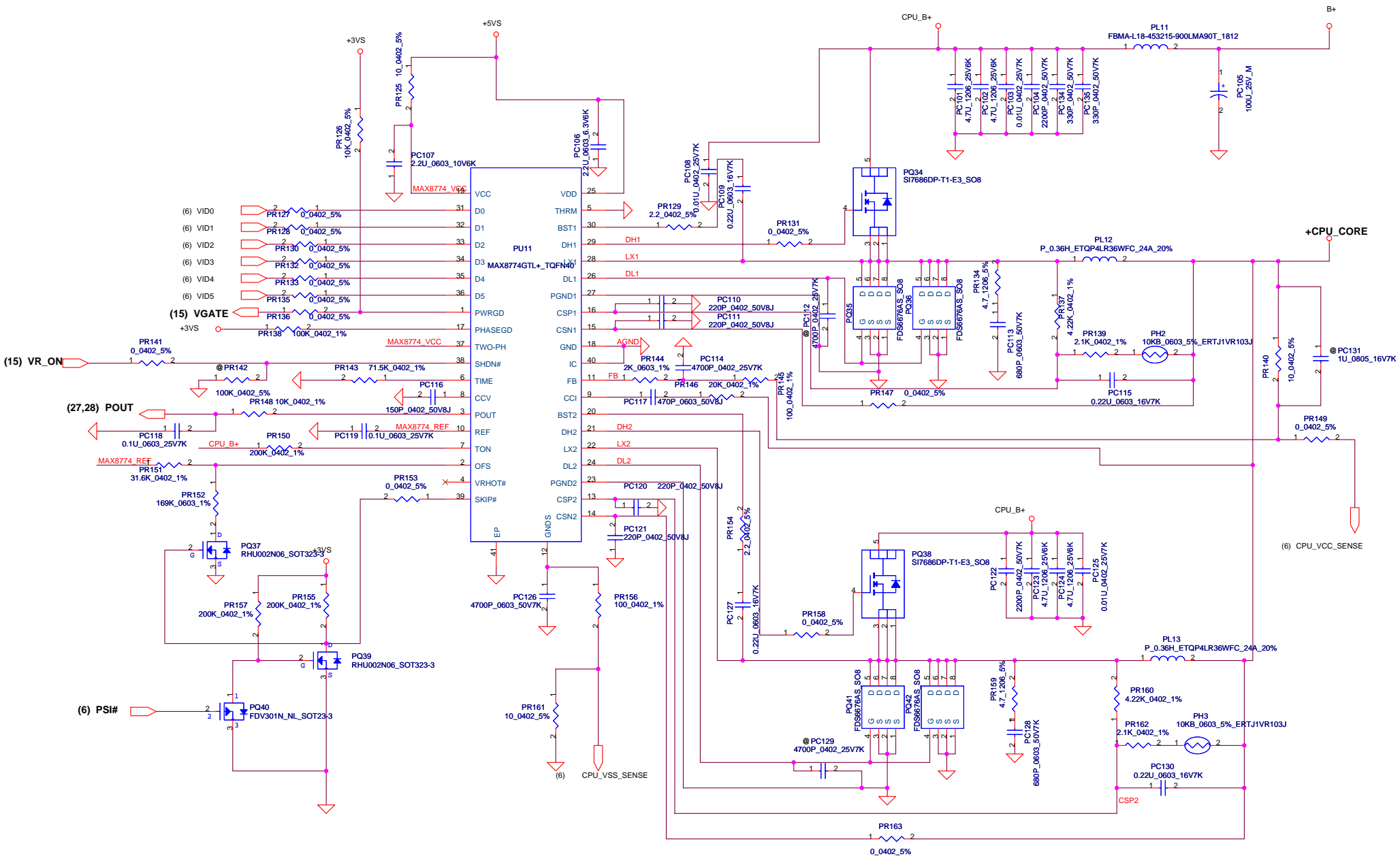
Close to IC Side  
Differential routing of feedback to VSSA2 and VOUT2 PIN

VFB=0.5V  
 $V_o = VFB * (1 + PR122 / PR127) = 1.805V$   
 $I_{peak} = 13.82A$ ,  $I_{max} = 9.68A$   
 $Ton = (3.3E-12 * (PR112 + 37K) * (Vout / VBat)) + 50ns$   
 $= 3.3E-12 * (820K + 37K) * (1.805 / 19) + 50ns = 0.319us$   
 $FDS6670AS: Rds(on) => Typ: 9 mOhm$   
 $Max: 11.5 mOhm$   
 $I_{ocp} = I_{valley} + I_{ripple} / 2$   
 $I_{ripple} = (vin - vout) * (Ton / L) = 5.485A$   
 $I_{valleymin} = 9E-6 * (PR106 / Rds(ON) * max * 1.4) = 16.826A$   
 $I_{valleymax} = 11E-6 * (PR106 / Rds(ON) * typ * 1.2) = 30.657A$   
 $OCP => 19.5685A \sim 33.3995A$

VFB=0.5V  
 $V_o = VFB * (1 + PR120 / PR121) = 1.25V$   
 $I_{peak} = 8.54A$ ,  $I_{max} = 6A$   
 $Ton = (3.3E-12 * (PR116 + 37K) * (Vout / VBat)) + 50ns$   
 $= 0.2661us$   
 $SI4810BDY: Rds(on) => Typ: 16 mOhm$   
 $Max: 20 mOhm$   
 $I_{valleymin} = 9E-6 * (PR119 / Rds(ON) * max * 1.3) = 10.419A$   
 $I_{valleymax} = 11E-6 * (PR119 / Rds(ON) * typ * 1.1) = 18.8125A$   
 $I_{ripple} = (vin - vout) * (Ton / L) = 2.631A$   
 $I_{ocp} = I_{valley} + I_{ripple} / 2$   
 $OCP => 11.7345A \sim 20.128A$

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Version change list (P.I.R. List)

Item	Fixed Issue	Rev.	PG#	Modify List	Date	Phase
1	BOM Change.	0.4	12	Remove R144, R372, C160, C528.		PVT
2	Added SSC for Lan TXCLK. (EMI Request)	0.4	12	Added U40, R525, R526, R527, R528, C682.		PVT
3	Improve Samsung Memory Module compatibility.	0.4	15	Added R540,R541 2.2K pull up +3VS.		PVT
4	Design Modify. (SCH Change)	0.4	15	Change CRT_DET form GPIO_5 to LID#, Add R78 10K. (Bios Request)		PVT
5	BCIC0172 : When Reset or Cold Boot MCP67 ACIN 會漏電到EC.	0.4	15	D24 反向, 47K Pull High 移除. Added R283 200K Pull Down.		PVT
6	RTC Battery 電壓過低.	0.4	16	Added R539 1K.		PVT
7	Design Modify. (SCH Change)	0.4	22	Change Q50.G Pin Net Name to SBPWR_EN.		PVT
8	Added R-C for BUF_25Mhz (EMI Request).	0.4	22	Added R530,C684.		PVT
9	Design Modify for EMI.	0.4	22	Added L59, L60, L61, L62, C685, C686.		PVT
10	解決+3VS 漏電 when enter S3 Mode.	0.4	25,26	Added Q56, Q57, Q58, Q59, R536, R537.		PVT
11	Design Modify for Acer WLAN LED.	0.4	25	JP21.44 Pin Added MINI1_LED# Net, Added R520, R521.		PVT
12	防止 BATT_TEMP, BATT_OVP, ACIN 被干擾.	0.4	27	Added C660, C661, C662.		PVT
13	Design Modify for Power. (65W/95W Detect Function)	0.4	27	U15.98 Pin Added 65W/95W# Net, Added R519 100K to +3VALW.		PVT
14	Design Modify for EMI.	0.4	30	Added C663~C678.		PVT
15	For AUDIO EA Test.	0.4	32	Change C582, C583, C584, C587,C594, C597 to 4.7uF.		PVT
16	解決關機 bo bo 聲問題.	0.4	33	Added Q53,C680.		PVT
17	Design Modify for EMI.	0.4	33	Added L57, L58 for Mic. L63, L64, L65, L66 for SPK. D28 for ESD.		PVT
18	Change Codec Amp to APA2057RI-TRL_TSSOP28.	0.4	33	Change U31 to SA00001QD00, added R523,R524.		PVT
19	Remove PJP14.	0.4	34	Remove PJP14.		PVT
20	Change MCP67-MV form A01 to A02.	0.4	10~17	Change MCP67-MV form A01 to A02.		PVT
21	解決系統時間延遲問題.	0.4	15	Change C503, C504 form 18pF to 6.8pF.		PVT
22	Improve WLAN Module compatibility.	0.3	11,25	Change WLAN Port form PCIE4 to PCIE2.		DVT2
23	Fixed LAN LED work abnormal.	0.3	22	Added D25,D27,D27, U39.		DVT2
24	Change LAN to RTL8211B.	0.2	22	Change Page 22 all compnent. DVT1		

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Title			
PIR (HW)			
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