Compal Confidential

JALB0 Schematics Document

AMD Griffin Processor with RS780M+SB700

(With ATI MXM/B)

2008-4-16

REV:1.0

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Issued Date	2008/04/16	Deciphered Date	2009/04/16	Title: Cover Page
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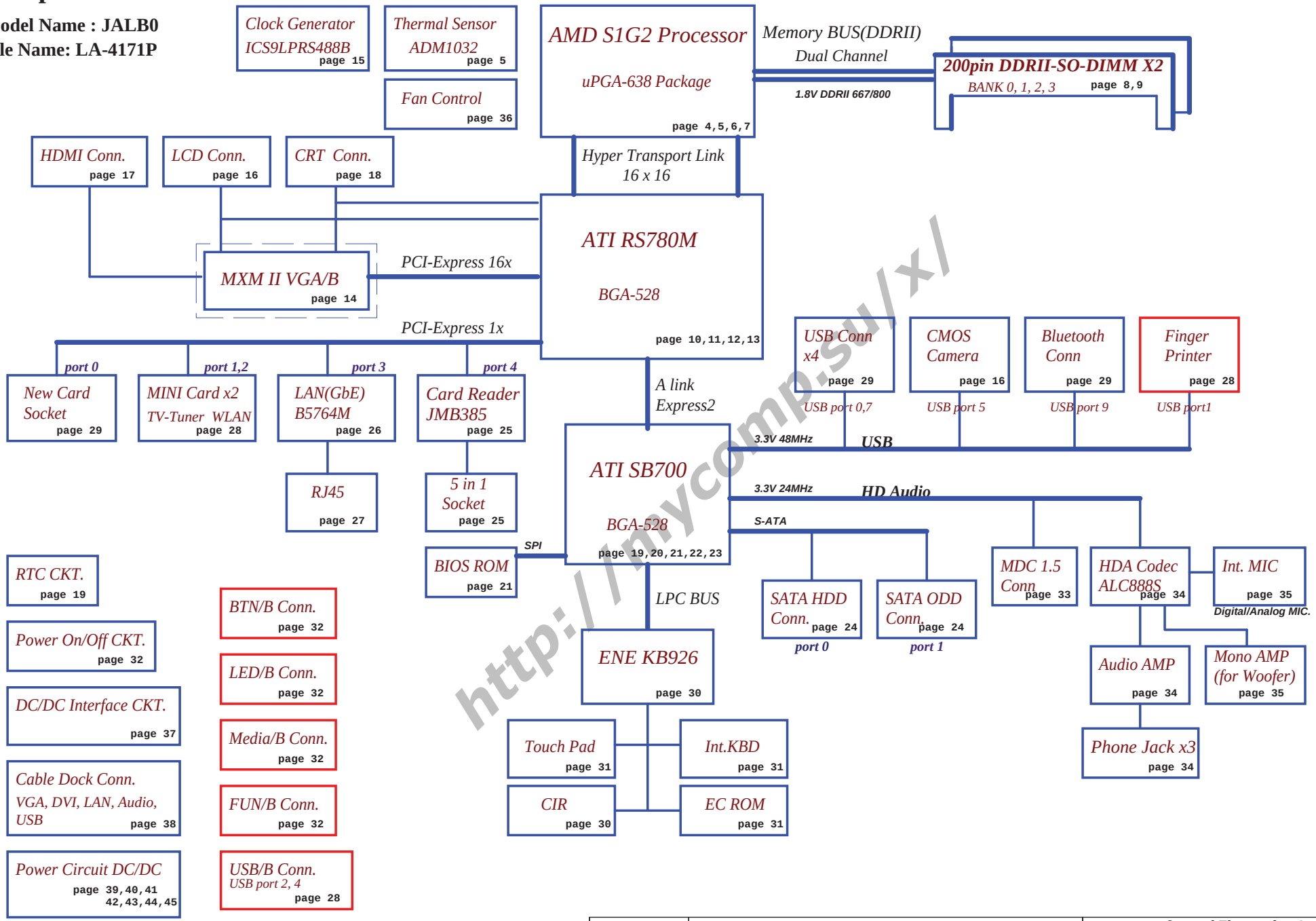
Model Name : JALB0
File Name: LA-4171P



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Compal Electronics, Inc.			
Title: Block Diagrams			
Size: B	Document Number: JALB0 LA-4181P		Rev: 1.0
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Voltage Rails

Power Plane	Description	S1	S3	S5
VIN	Adapter power supply (19V)	N/A	N/A	N/A
B+	AC or battery power rail for power circuit.	N/A	N/A	N/A
+CPU_CORE_0	Core voltage for CPU	ON	OFF	OFF
+CPU_CORE_1	Core voltage for CPU	ON	OFF	OFF
+CPU_CORE_NB	Core voltage for CPU	ON	OFF	OFF
+0.9V	0.9V switched power rail for DDR terminator	ON	ON	OFF
+1.1VS	1.05V switched power rail	ON	OFF	OFF
+1.2V_HT	1.25V switched power rail	ON	OFF	OFF
+NB_CORE	1.0V~1.1V switched power rail for NB VDDC	ON	OFF	OFF
+1.5VS	1.5V power rail for PCIE Card	ON	OFF	OFF
+1.8V	1.8V power rail for CPU VDDIO and DDR	ON	ON	OFF
+1.8VS	1.8V switched power rail	ON	OFF	OFF
+2.5VS	2.5V for CPU_VDDA and MXM/B	ON	OFF	OFF
+3VALW	3.3V always on power rail	ON	ON	ON*
+3V_LAN	3.3V power rail for LAN	ON	ON	ON
+3VS	3.3V switched power rail	ON	OFF	OFF
+5VALW	5V always on power rail	ON	ON	ON*
+5VS	5V switched power rail	ON	OFF	OFF
+VSB	VSB always on power rail	ON	ON	ON*
+RTCVCC	RTC power	ON	ON	ON

Note : ON* means that this power plane is ON only with AC power available, otherwise it is OFF.

External PCI Devices

Device	IDSEL#	REQ#/GNT#	Interrupts

No PCI device

EC SM Bus1 address

Device	Address
Smart Battery	0001 011X b
EEPROM(24C16/02)	1010 000X b
MXM GMT G781-1	1001 101X b

EC SM Bus2 address

Device	Address
ADI ADM1032	1001 100X b
CPU SB	1001 101X b

SB700 SM Bus 0 address

Device	Address
Clock Generator (ICS9LPRS365)	1101 001Xb
DDR DIMM0	1001 000Xb
DDR DIMM2	1001 010Xb
Minicard	
Minicard	

SB700 SM Bus 1 address

Device	Address
New card	
Lan	

STATE \ SIGNAL	SLP_S1#	SLP_S3#	SLP_S4#	SLP_S5#	+VALW	+V	+VS	Clock
Full ON	HIGH	HIGH	HIGH	HIGH	ON	ON	ON	ON
S1(Power On Suspend)	LOW	HIGH	HIGH	HIGH	ON	ON	ON	LOW
S3 (Suspend to RAM)	LOW	LOW	HIGH	HIGH	ON	ON	OFF	OFF
S4 (Suspend to Disk)	LOW	LOW	LOW	HIGH	ON	OFF	OFF	OFF
S5 (Soft OFF)	LOW	LOW	LOW	LOW	ON	OFF	OFF	OFF

Board ID / SKU ID Table for AD channel

Vcc	3.3V +/- 5%
Ra/Rc/Re	100K +/- 5%

Board ID	Rb / Rd / Rf	V_{AD_BID} min	V_{AD_BID} typ	V_{AD_BID} max
0	0	0 V	0 V	0 V
1	8.2K +/- 5%	0.216 V	0.250 V	0.289 V
2	18K +/- 5%	0.436 V	0.503 V	0.538 V
3	33K +/- 5%	0.712 V	0.819 V	0.875 V
4	56K +/- 5%	1.036 V	1.185 V	1.264 V
5	100K +/- 5%	1.453 V	1.650 V	1.759 V
6	200K +/- 5%	1.935 V	2.200 V	2.341 V
7	NC	2.500 V	3.300 V	3.300 V

BOARD ID Table

Board ID	PCB Revision
0	0.1
1	0.2
* 2	0.3 0.4 1.0
3	
4	
5	
6	
7	

BTO Option Table

BTO Item	BOM Structure
Discrete	VGA@
UMA	UMA@

PROJECT ID Table

Board ID	PROJECT
0	JALB0
1	JALC0
2	
3	
4	
5	
6	
7	

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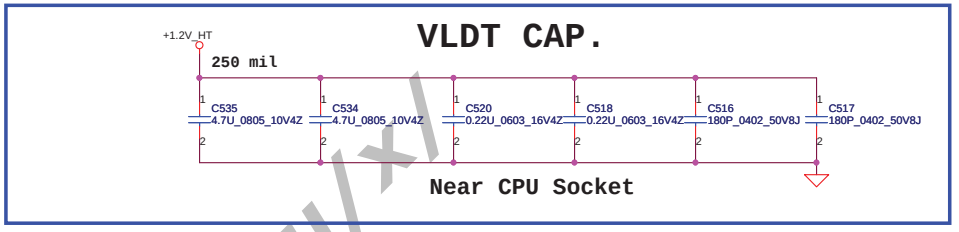

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Title: **AMD CPU S1G2 HT I/F**

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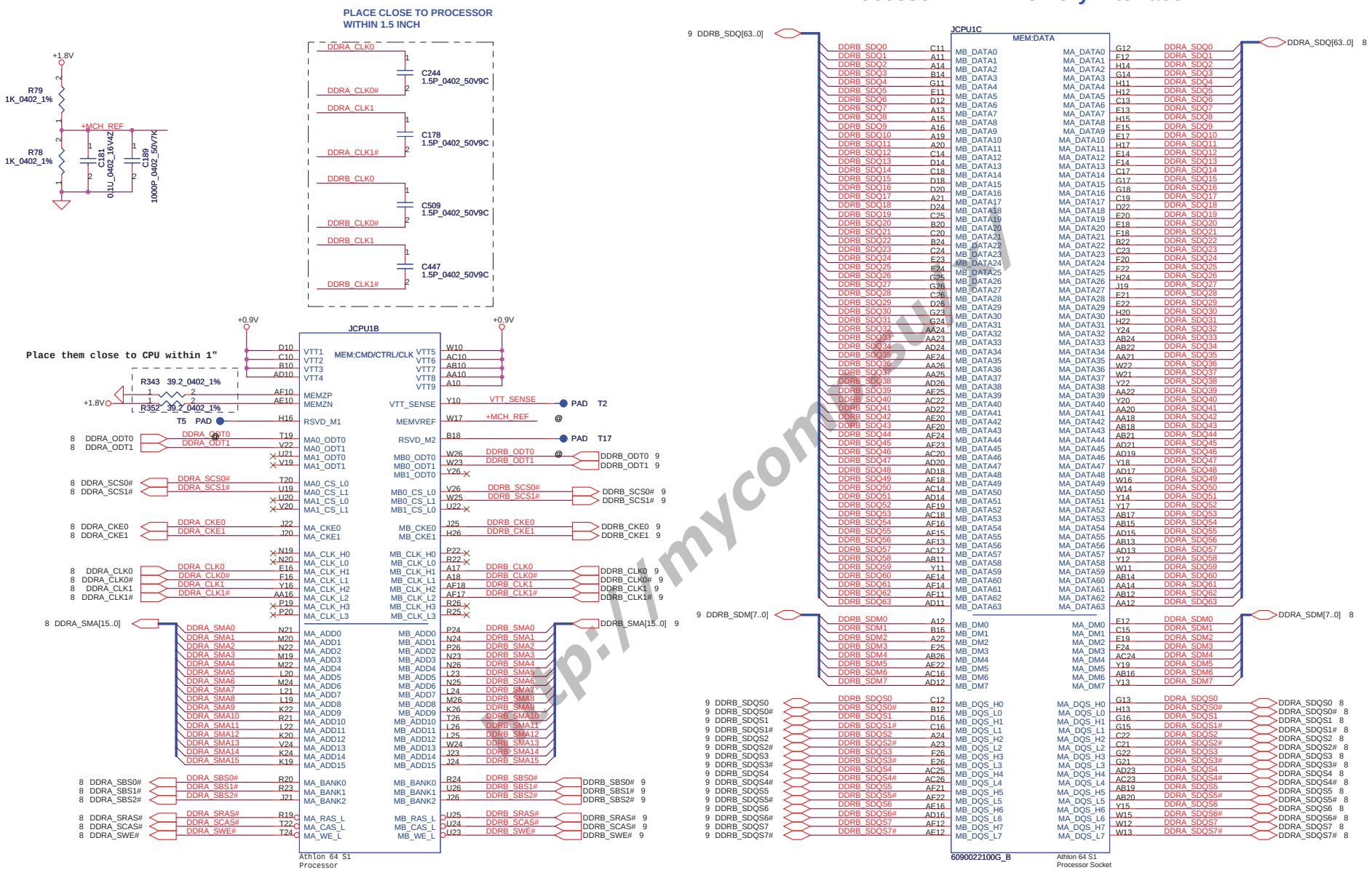
Processor DDR2 Memory Interface



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Compal Electronics, Inc.

Title: **AMD CPU S1G2 DDRII I/F**

Size	Document Number	Rev
Custom	JALB0 LA-4171P	1.0

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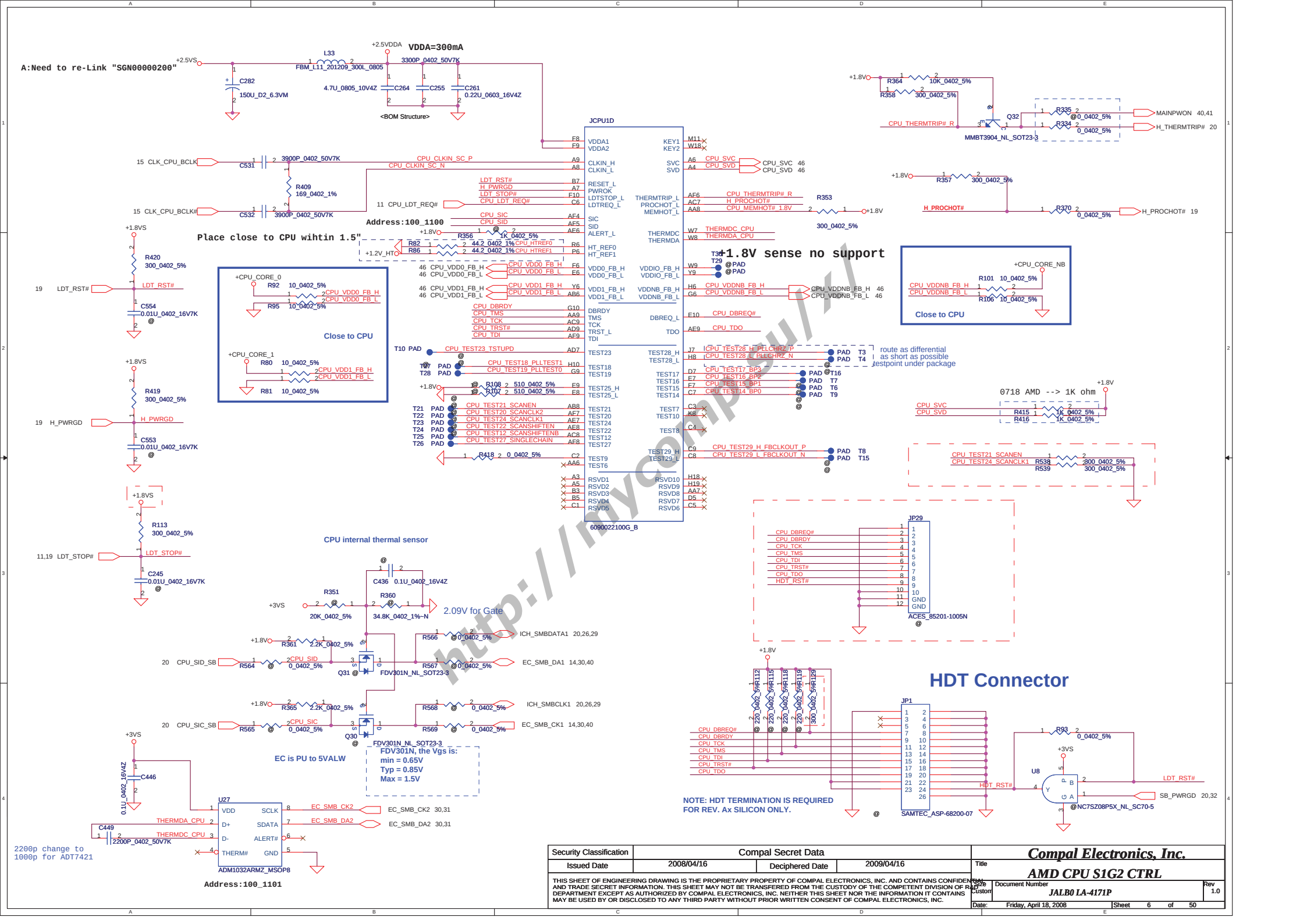

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Compal Electronics, Inc.			
Title: AMD CPU S1G2 CTRL			
Size: Custom	Document Number: JALB0 LA-4171P		Rev: 1.0
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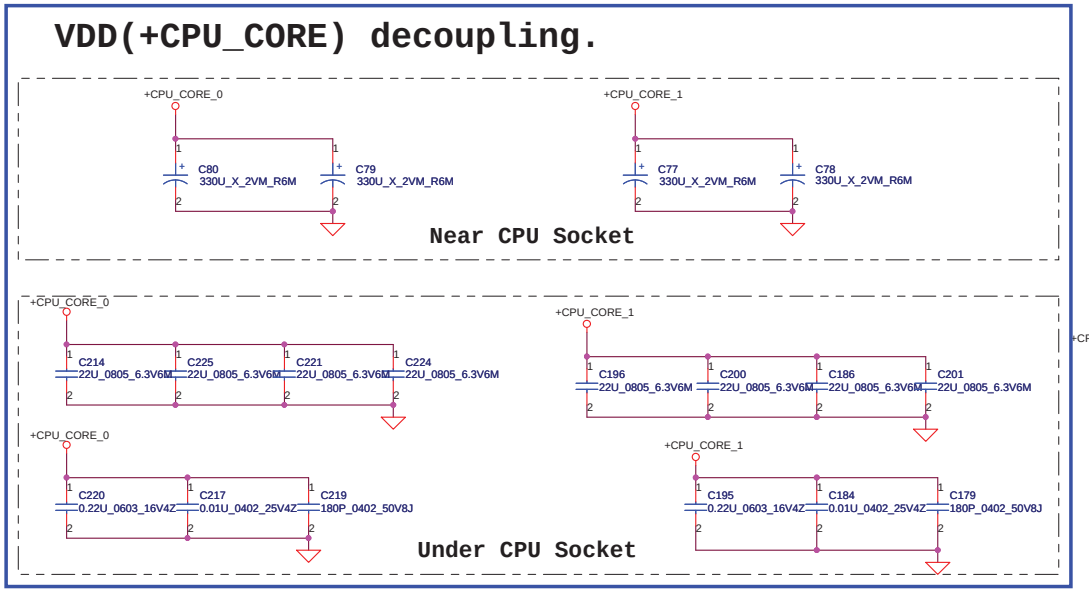
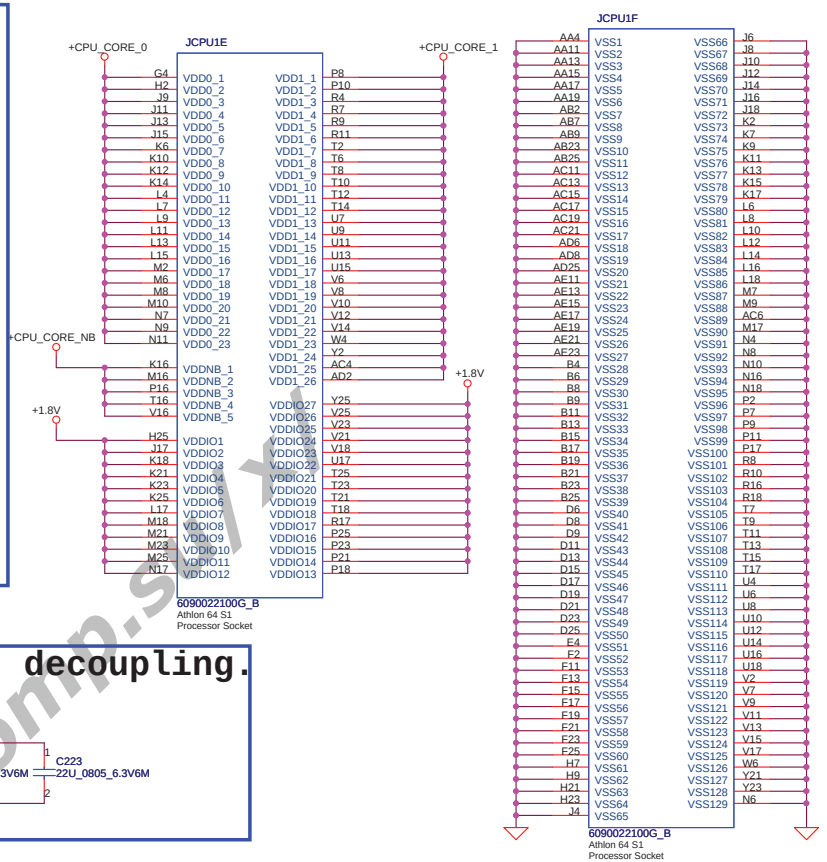
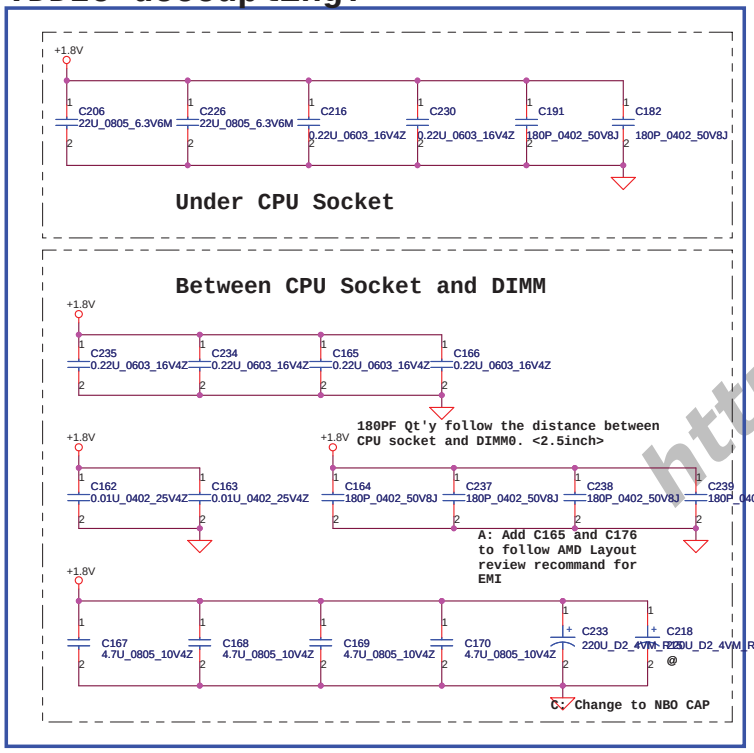
VDD(+CPU_CORE) decoupling.

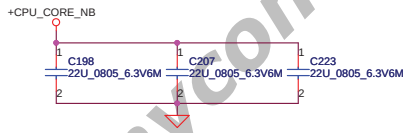




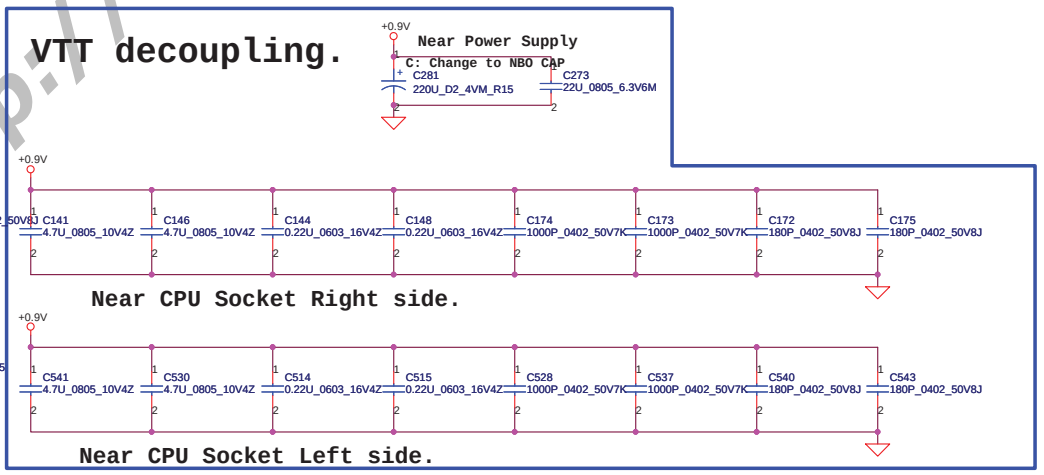
VDDIO decoupling.



+CPU_CORE_NB decoupling.



VTT decoupling.



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Title	AMD CPU S1G2 PWR & GND
Size: Custom	Document Number: JALB0 LA-4171P
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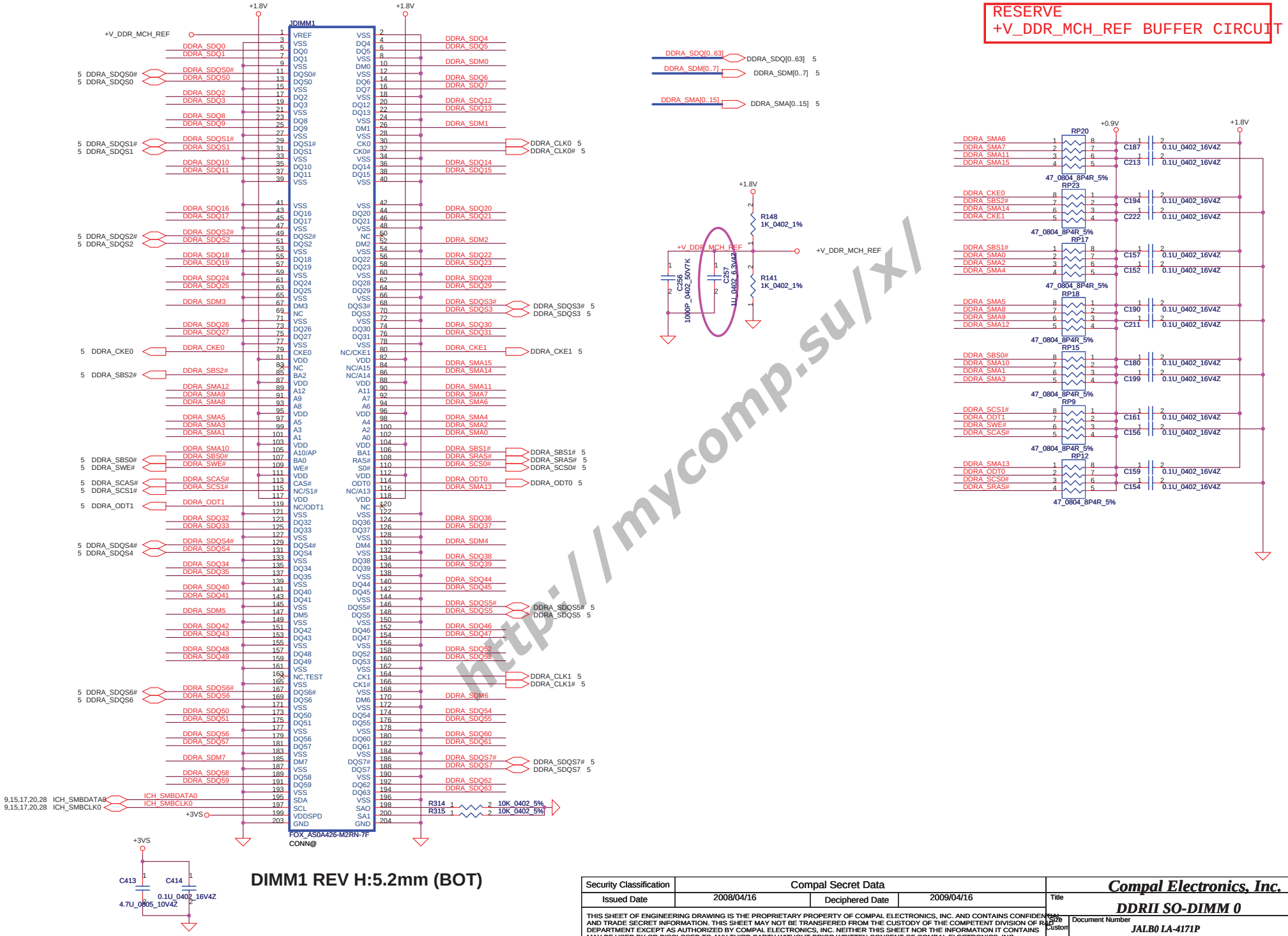

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Title: DDRII SO-DIMM 0

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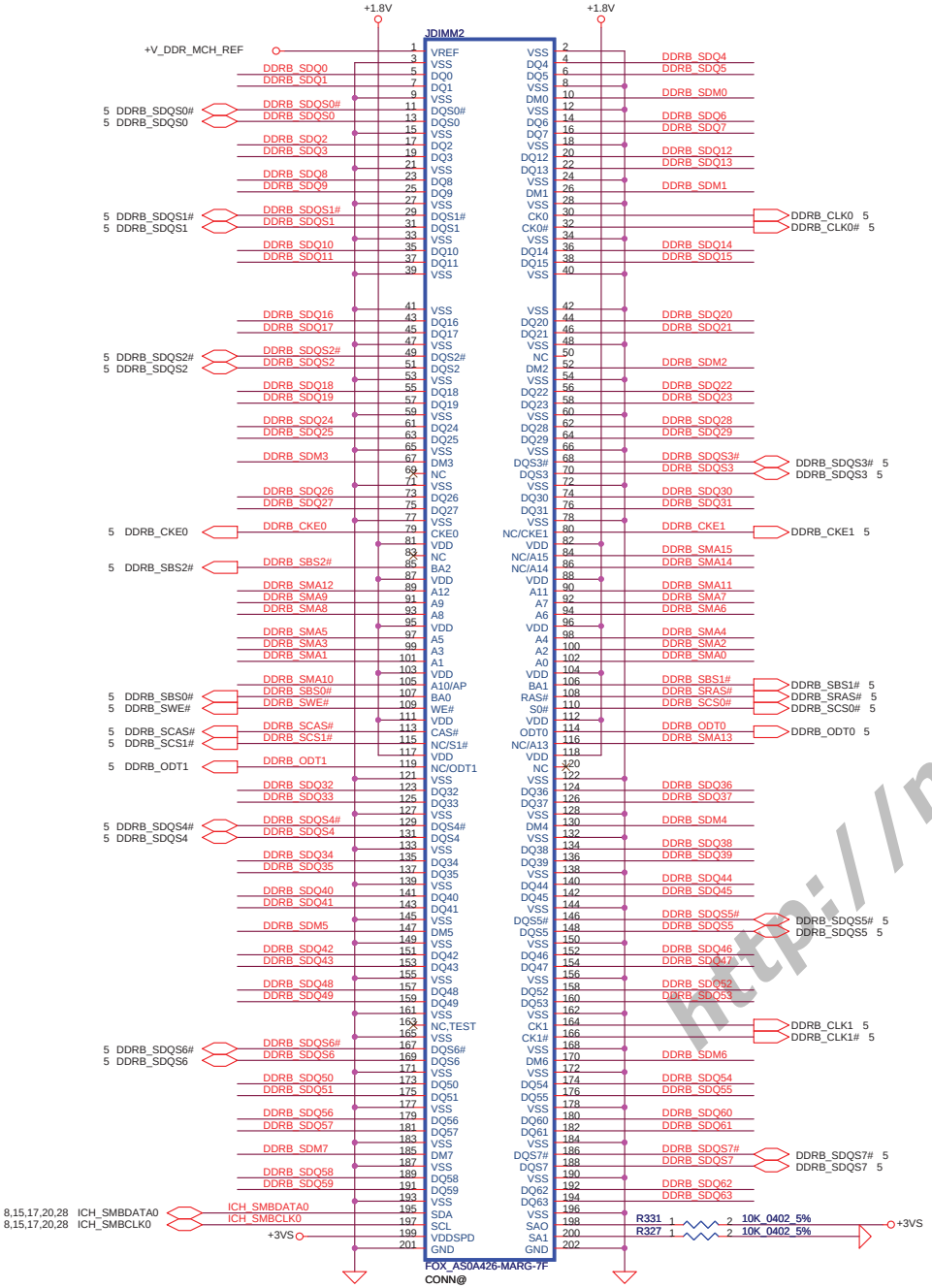
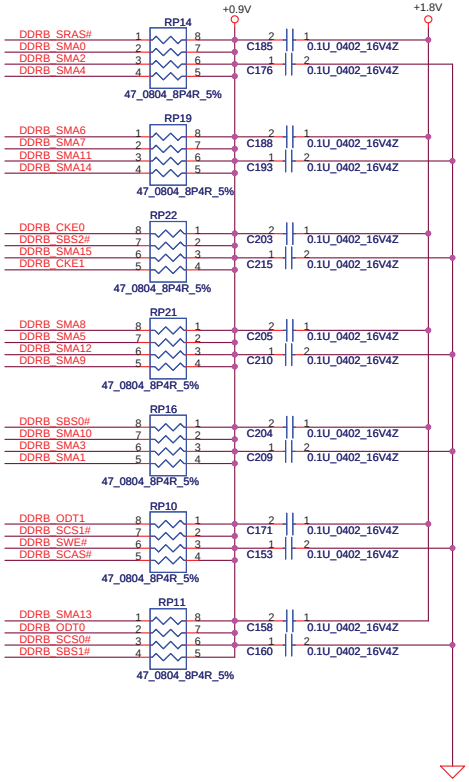


DIMM1 REV H:9.2mm (BOT)

DDRB_SDQ[0..63] DDRB_SDQ[0..63] 5
DDRB_SDM[0..7] DDRB_SDM[0..7] 5
DDRB_SMA[0..15] DDRB_SMA[0..15] 5



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Title: DDRII SO-DIMM 1

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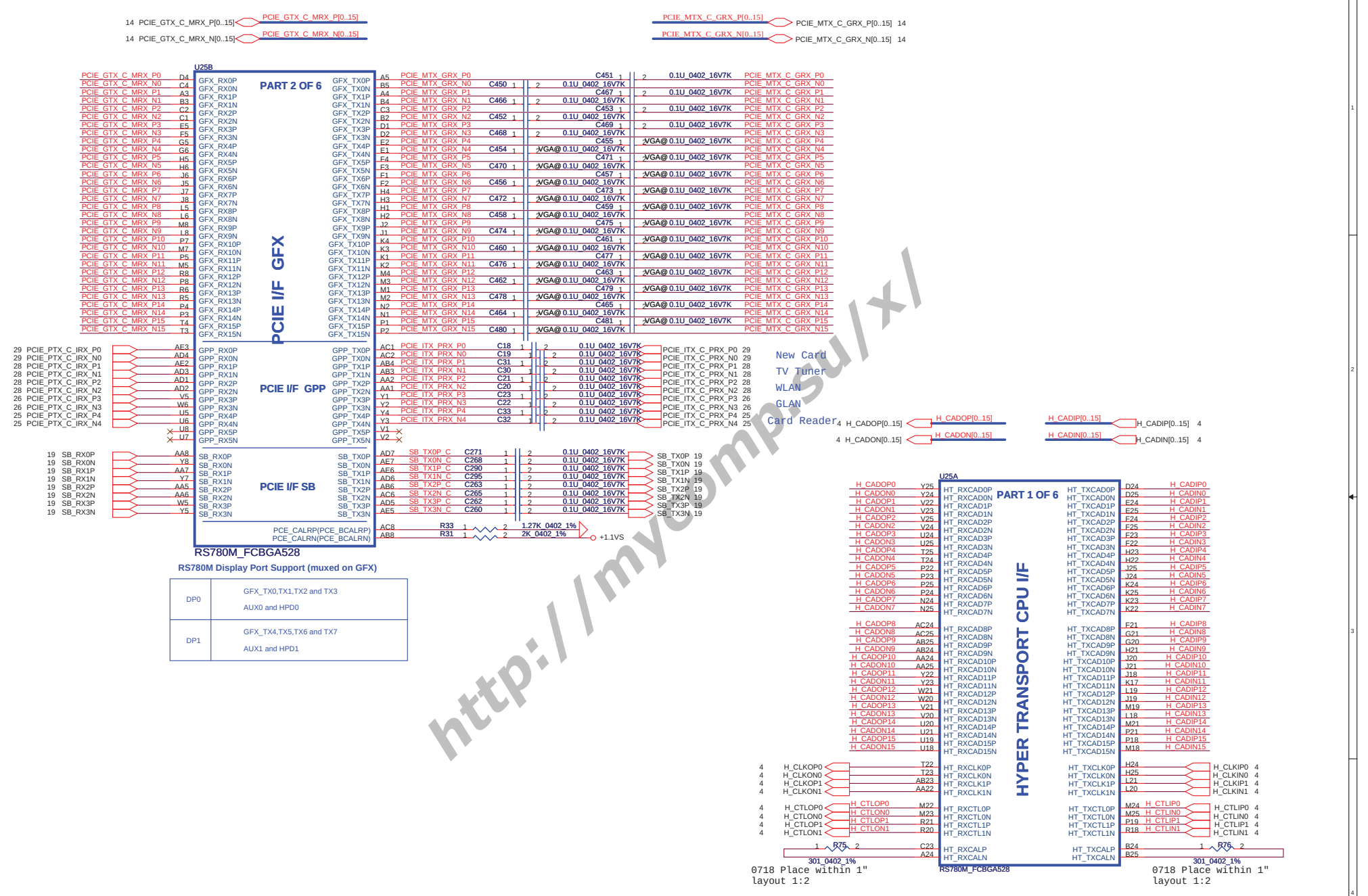

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Compal Electronics, Inc.	
Title	RS780-HT/PCIE
Size: Custom	Document Number: JALB0 LA-4171P
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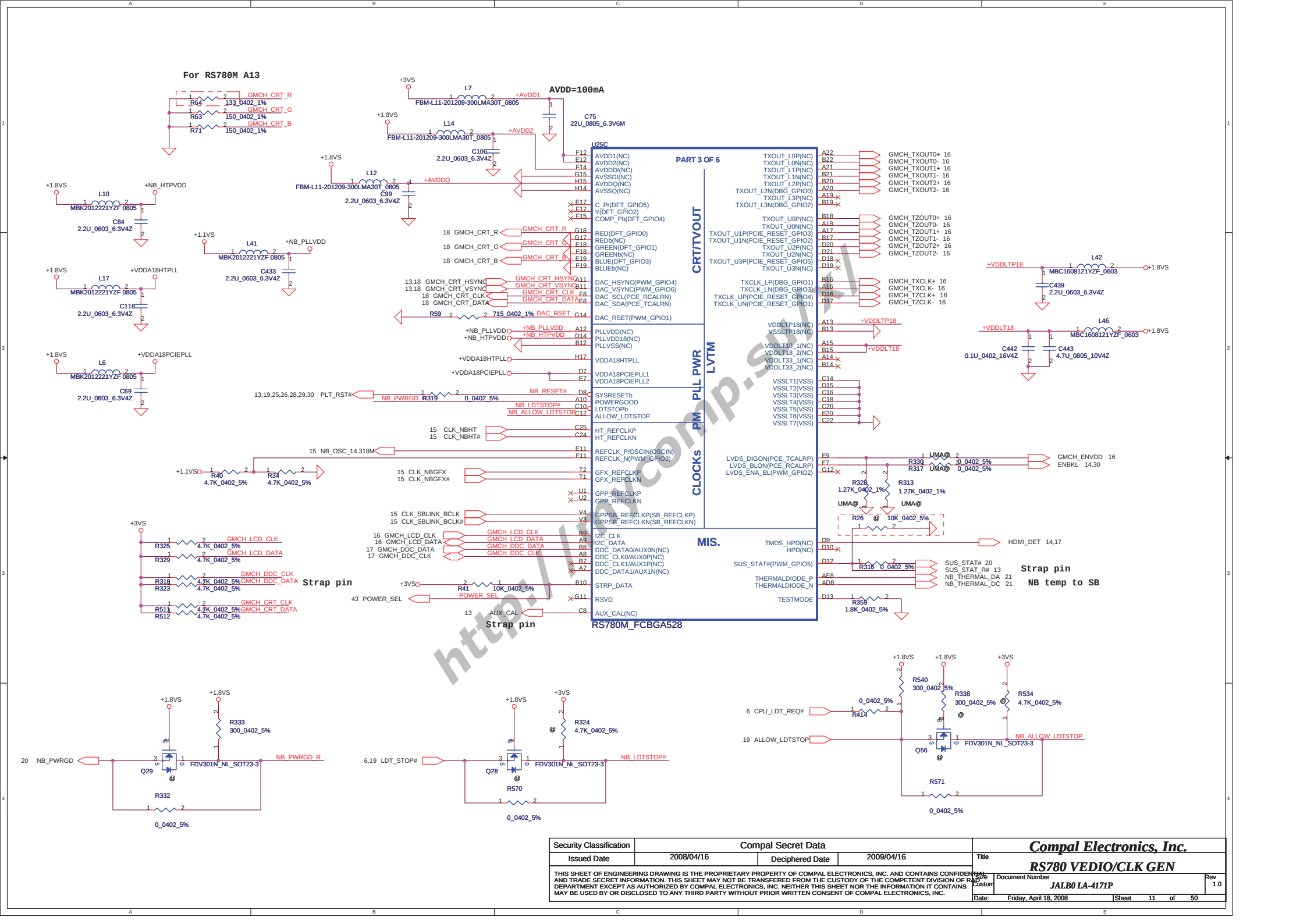
Date: Friday, April 18, 2008	Sheet 10 of 50



Security Classification	Compal Secret Data		
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Compal Electronics, Inc.

Title: **RS780 VEDIO/CLK GEN**

Size	Document Number	Rev
Custom	JALB0 LA-4171P	1.0

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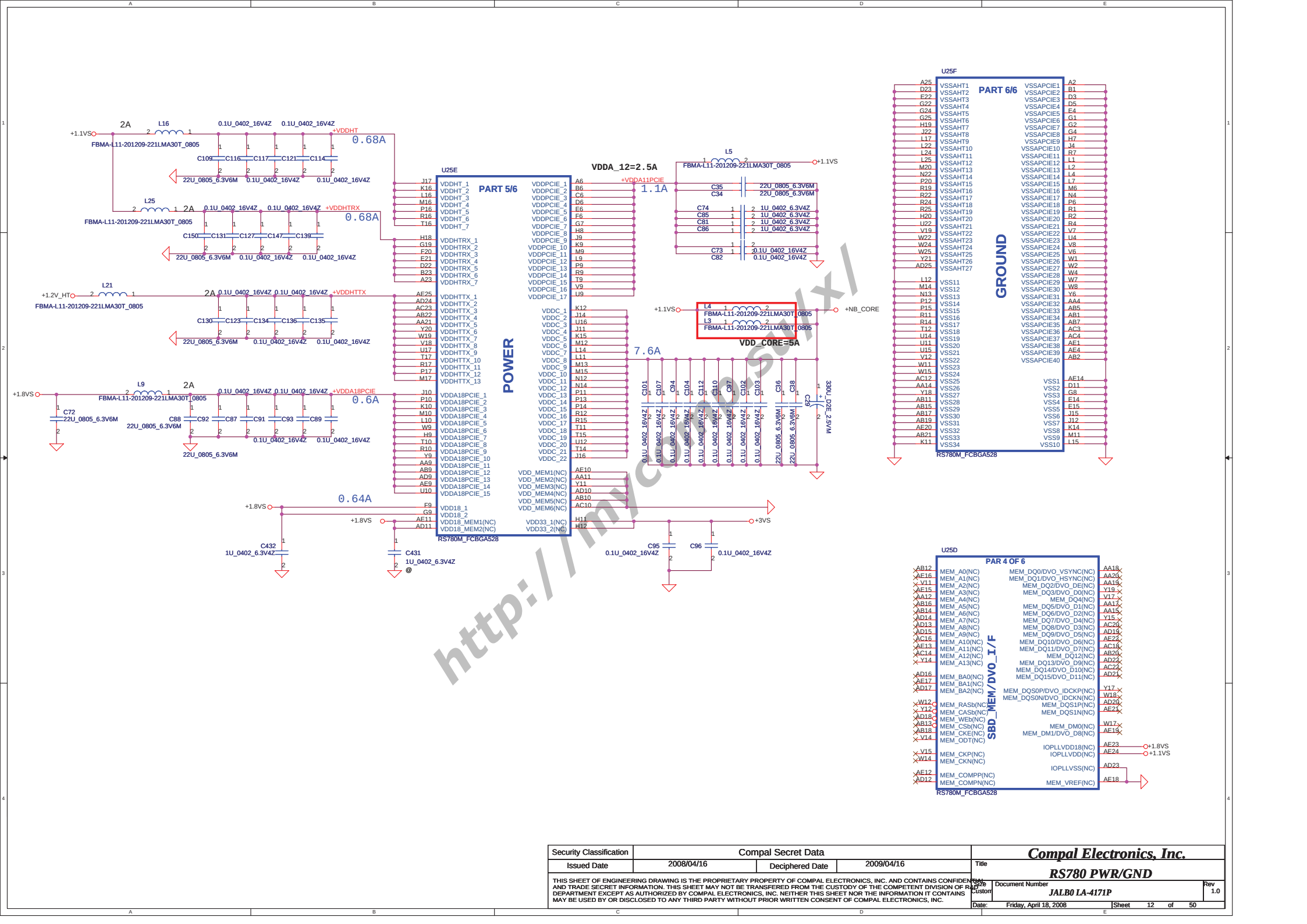

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Title: **RS780 PWR/GND**

Size	Document Number	Rev
Custom	JALB0 LA-4171P	1.0

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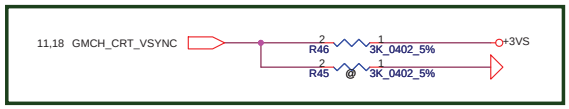
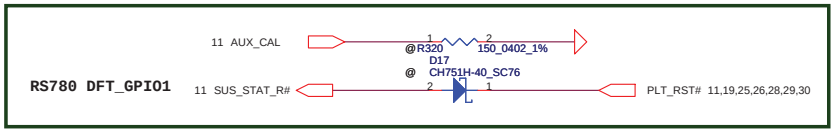


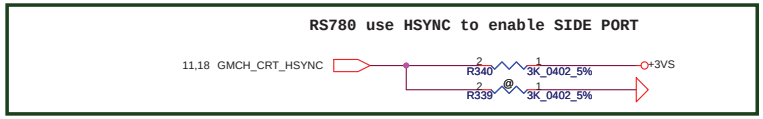
DFT_GPIO5:STRAP_DEBUG_BUS_GPIO_ENABLEb

```
Enables the Test Debug Bus using GPIO. (VSYNC)
1 : Disable (RS780)
0 : Enable (Rs780)
```



DFT_GPIO1: LOAD_EEPROM_STRAPS

```
Selects Loading of STRAPS from EPROM
1 : Bypass the loading of EEPROM straps and use Hardware Default Values
0 : I2C Master can load strap values from EEPROM if connected, or use
default values if not connected
RS740/RX780: DFT_GPIO1  RS780:SUS_STAT
```



RS780 use HSYNC to enable SIDE PORT

```
RS740/RS780: Enables Side port memory ( RS780 use HSYNC#)
0.    Enable (RS780)
1 :   Disable(RS780)
```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Compal Electronics, Inc.			
Title: RS780 STRAPS			
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10 PCIE_MTX_C_GRX_N[0..15] PCIE_MTX_C_GRX_N[0..15]
10 PCIE_MTX_C_GRX_P[0..15] PCIE_MTX_C_GRX_P[0..15]
10 PCIE_GTX_C_MRX_N[0..15] PCIE_GTX_C_MRX_N[0..15]
10 PCIE_GTX_C_MRX_P[0..15] PCIE_GTX_C_MRX_P[0..15]

JMXM1A

+MXM_B+ 1,3,5,7,9,11,13,15 PWR_SRC; 17,19,21,23 GND

2,4,6,8,10,12,14 1V8RUN → +1.8VS

140mil(3.5A)

16 RUNPWROK → VGA_ON 32

18 5VRUN → +5VS

20,22,24 GND

PCIE_GTX_C_MRX_N0	25	PEX_RX15#
PCIE_GTX_C_MRX_P0	27	PEX_RX15
	29	GND
PCIE_GTX_C_MRX_N1	31	PEX_RX14#
PCIE_GTX_C_MRX_P1	33	PEX_RX14
	35	GND
PCIE_GTX_C_MRX_N2	37	PEX_RX13#
PCIE_GTX_C_MRX_P2	39	PEX_RX13
	41	GND
PCIE_GTX_C_MRX_N3	43	PEX_RX12#
PCIE_GTX_C_MRX_P3	45	PEX_RX12
	47	GND
PCIE_GTX_C_MRX_N4	49	PEX_RX11#
PCIE_GTX_C_MRX_P4	51	PEX_RX11
	53	GND
PCIE_GTX_C_MRX_N5	55	PEX_RX10#
PCIE_GTX_C_MRX_P5	57	PEX_RX10
	59	GND
PCIE_GTX_C_MRX_N6	61	PEX_RX9#
PCIE_GTX_C_MRX_P6	63	PEX_RX9
	65	GND
PCIE_GTX_C_MRX_N7	67	PEX_RX8#
PCIE_GTX_C_MRX_P7	69	PEX_RX8
	71	GND
PCIE_GTX_C_MRX_N8	73	PEX_RX7#
PCIE_GTX_C_MRX_P8	75	PEX_RX7
	77	GND
PCIE_GTX_C_MRX_N9	79	PEX_RX6#
PCIE_GTX_C_MRX_P9	81	PEX_RX6
	83	GND
PCIE_GTX_C_MRX_N10	85	PEX_RX5#
PCIE_GTX_C_MRX_P10	87	PEX_RX5
	89	GND
PCIE_GTX_C_MRX_N11	91	PEX_RX4#
PCIE_GTX_C_MRX_P11	93	PEX_RX4
	95	GND
PCIE_GTX_C_MRX_N12	97	PEX_RX3#
PCIE_GTX_C_MRX_P12	99	PEX_RX3
	101	GND
PCIE_GTX_C_MRX_N13	103	PEX_RX2#
PCIE_GTX_C_MRX_P13	105	PEX_RX2
	107	GND

	26	PRSNT2#
	28	PEX_TX15#
	30	PEX_TX15
	32	GND
	34	PEX_TX14#
	36	PEX_TX14
	38	GND
	40	PEX_TX13#
	42	PEX_TX13
	44	GND
	46	PEX_TX12#
	48	PEX_TX12
	50	GND
	52	PEX_TX11#
	54	PEX_TX11
	56	GND
	58	PEX_TX10#
	60	PEX_TX10
	62	GND
	64	PEX_TX9#
	66	PEX_TX9
	68	GND
	70	PEX_TX8#
	72	PEX_TX8
	74	GND
	76	PEX_TX7#
	78	PEX_TX7
	80	GND
	82	PEX_TX6#
	84	PEX_TX6
	86	GND
	88	PEX_TX5#
	90	PEX_TX5
	92	GND
	94	PEX_TX4#
	96	PEX_TX4
	98	GND
	100	PEX_TX3#
	102	PEX_TX3
	104	GND
	106	PEX_TX2#
	108	PEX_TX2

PCIE_MTX_C_GRX_N0 … PCIE_MTX_C_GRX_N15 / PCIE_MTX_C_GRX_P0 … PCIE_MTX_C_GRX_P15

ACES_88990-2D08
CONN@

Lane Reversal on PCIEX16

JMXM1B

PCIE_GTX_C_MRX_N14	109	PEX_RX1#
PCIE_GTX_C_MRX_P14	111	PEX_RX1
	113	GND
PCIE_GTX_C_MRX_N15	115	PEX_RX0#
PCIE_GTX_C_MRX_P15	117	PEX_RX0
	119	GND
15 CLK_PCIE_VGA#	121	CLK_PCIE_VGA#
15 CLK_PCIE_VGA	123	CLK_PCIE_VGA
	125	PEX_REFCLK#
	127	PEX_REFCLK
19 VGA_RST#	129	CLK_REQ#
20 HDA_SYNC_MXM	131	PEX_RST#
20 HDA_BCLK_MXM	133	RSVD
	135	RSVD
	137	SMB_DAT
18 VGA_CRT_HSYNC	139	SMB_CLK
18 VGA_CRT_VSYNC	141	THERM#
18 VGA_DDC_CLK	143	VGA_HSYNC
18 VGA_DDC_DATA	145	VGA_VSYNC
20 HDA_SDI_MXM	147	DDCA_CLK
20 HDA_SDO_MXM	149	DDCA_DAT
	151	IGP_UCLK#
	153	IGP_UCLK
	155	GND
	157	RSVD
	159	RSVD
	161	RSVD
	163	IGP_UTX2#
	165	IGP_UTX2
	167	GND
	169	IGP_UTX1#
	171	IGP_UTX1
	173	GND
	175	IGP_UTX0#
	177	IGP_UTX0
	179	GND
	181	IGP_LCLK#/DVI_B_CLK#
	183	IGP_LCLK/DVI_B_CLK
	185	DVI_B_HPD/GND
	187	RSVD
	189	RSVD
	191	GND
	193	IGP_LTX2#/DVI_B_TX2#
	195	IGP_LTX2/DVI_B_TX2
	197	GND
	199	IGP_LTX1#/DVI_B_TX1#
	201	IGP_LTX1/DVI_B_TX1
	203	GND
	205	IGP_LTX0#/DVI_B_TX0#
	207	IGP_LTX0/DVI_B_TX0
	209	DVI_A_HPD
	211	DVI_A_CLK#
	213	DVI_A_CLK
	215	GND
	217	DVI_A_TX2#
	219	DVI_A_TX2
	221	GND
	223	DVI_A_TX1#
	225	DVI_A_TX1
	227	GND
	229	DVI_A_TX0#
	231	DVI_A_TX0
		GND

	110	GND
	112	PEX_TX1#
	114	PEX_TX1
	116	GND
	118	PEX_TX0#
	120	PEX_TX0
	122	PRSNT1#
	124	TV_C/HDTV_Pr
	126	GND
	128	TV_Y/HDTV_Y
	130	GND
	132	TV_CVBS/HDTV_Pb
	134	GND
	136	VGA_RED
	138	GND
	140	VGA_GRN
	142	GND
	144	VGA_BLU
	146	GND
	148	LVDS_UCLK#
	150	LVDS_UCLK
	152	GND
	154	LVDS_UTX3#
	156	LVDS_UTX3
	158	GND
	160	LVDS_UTX2#
	162	LVDS_UTX2
	164	GND
	166	LVDS_UTX1#
	168	LVDS_UTX1
	170	GND
	172	LVDS_UTX0#
	174	LVDS_UTX0
	176	GND
	178	LVDS_LCLK#
	180	LVDS_LCLK
	182	GND
	184	LVDS_LTX3#
	186	LVDS_LTX3
	188	GND
	190	LVDS_LTX2#
	192	LVDS_LTX2
	194	GND
	196	LVDS_LTX1#
	198	LVDS_LTX1
	200	GND
	202	LVDS_LTX0#
	204	LVDS_LTX0
	206	GND
	208	DDCC_DAT
	210	DDCC_CLK
	212	LVDS_PPEN
	214	LVDS_BL_BRGHT
	216	LVDS_BLEN
	218	DDCB_DAT
	220	DDCB_CLK
	222	2V5RUN
	224	GND
	226	3V3RUN
	228	3V3RUN
	230	3V3RUN
	232	GND

ACES_88990-2D08
CONN@

PCIE_MTX_C_GRX_N14 … PCIE_MTX_C_GRX_N15 / PCIE_MTX_C_GRX_P14 … PCIE_MTX_C_GRX_P15

R502 1 @ 2 1K_0402_5%
VGA_CRT_R → HDA_RST#_MXM 20 / VGA_CRT_R 18
VGA_CRT_G → VGA_CRT_G 18
VGA_CRT_B → VGA_CRT_B 18
VGA_TZCLK- → VGA_TZCLK- 16
VGA_TZCLK+ → VGA_TZCLK+ 16

R377 1 @ 2 0_0402_5%
SPDIF_HDMI 33
VGA_TZOUT2- → VGA_TZOUT2- 16
VGA_TZOUT2+ → VGA_TZOUT2+ 16
VGA_TZOUT1- → VGA_TZOUT1- 16
VGA_TZOUT1+ → VGA_TZOUT1+ 16
VGA_TZOUT0- → VGA_TZOUT0- 16
VGA_TZOUT0+ → VGA_TZOUT0+ 16
VGA_TXCLK- → VGA_TXCLK- 16
VGA_TXCLK+ → VGA_TXCLK+ 16

VGA_TXOUT2- → VGA_TXOUT2- 16
VGA_TXOUT2+ → VGA_TXOUT2+ 16
VGA_TXOUT1- → VGA_TXOUT1- 16
VGA_TXOUT1+ → VGA_TXOUT1+ 16
VGA_TXOUT0- → VGA_TXOUT0- 16
VGA_TXOUT0+ → VGA_TXOUT0+ 16

I2CC_SDA → I2CC_SDA 16
I2CC_SCL → I2CC_SCL 16
ENVDD → ENVDD 16
ENBKL → ENBKL 11,30
VGA_DVI_SDATA → VGA_DVI_SDATA 17
VGA_DVI_SCLK → VGA_DVI_SCLK 17
+2.5VS
+3VS

C668 @ 2 1 0.1U_0402_16V4Z
+3VS
21,30,31,37,39,42 ACIN
U43 NC7SZ08P5X_NL_SC70-5 @

11,17 HDMI_DET
17 VGA_DVI_TXC- → VGA_DVI_TXC-
17 VGA_DVI_TXC+ → VGA_DVI_TXC+
17 VGA_DVI_TXD2- → VGA_DVI_TXD2-
17 VGA_DVI_TXD2+ → VGA_DVI_TXD2+
17 VGA_DVI_TXD1- → VGA_DVI_TXD1-
17 VGA_DVI_TXD1+ → VGA_DVI_TXD1+
17 VGA_DVI_TXD0- → VGA_DVI_TXD0-
17 VGA_DVI_TXD0+ → VGA_DVI_TXD0+

+MXM_B+
160mil(4A)
L26 2 1 KC FBM-L11-201209-221LMAT_0805 VGA@
L27 2 1 KC FBM-L11-201209-221LMAT_0805 VGA@
C202 2 B+ 160mil(4A) 0.1U_0603_25V7K
C183 1 2 VGA@ 680P_0402_50V7K
C197 1 2 68P_0402_50V8J
VGA@

+1.2V_HT C567 1 2 0.1U_0402_16V4Z
+2.5VS C483 1 2 0.1U_0402_16V4Z VGA@
+5VS C482 1 2 0.1U_0402_16V4Z VGA@

6,30,40 EC_SMB_DA1 → Q34A 2N7002DW-T/R7_SOT363-6 VGA@ → D_EC_SMB_DA1
6,30,40 EC_SMB_CK1 → Q34B 2N7002DW-T/R7_SOT363-6 VGA@ → D_EC_SMB_CK1

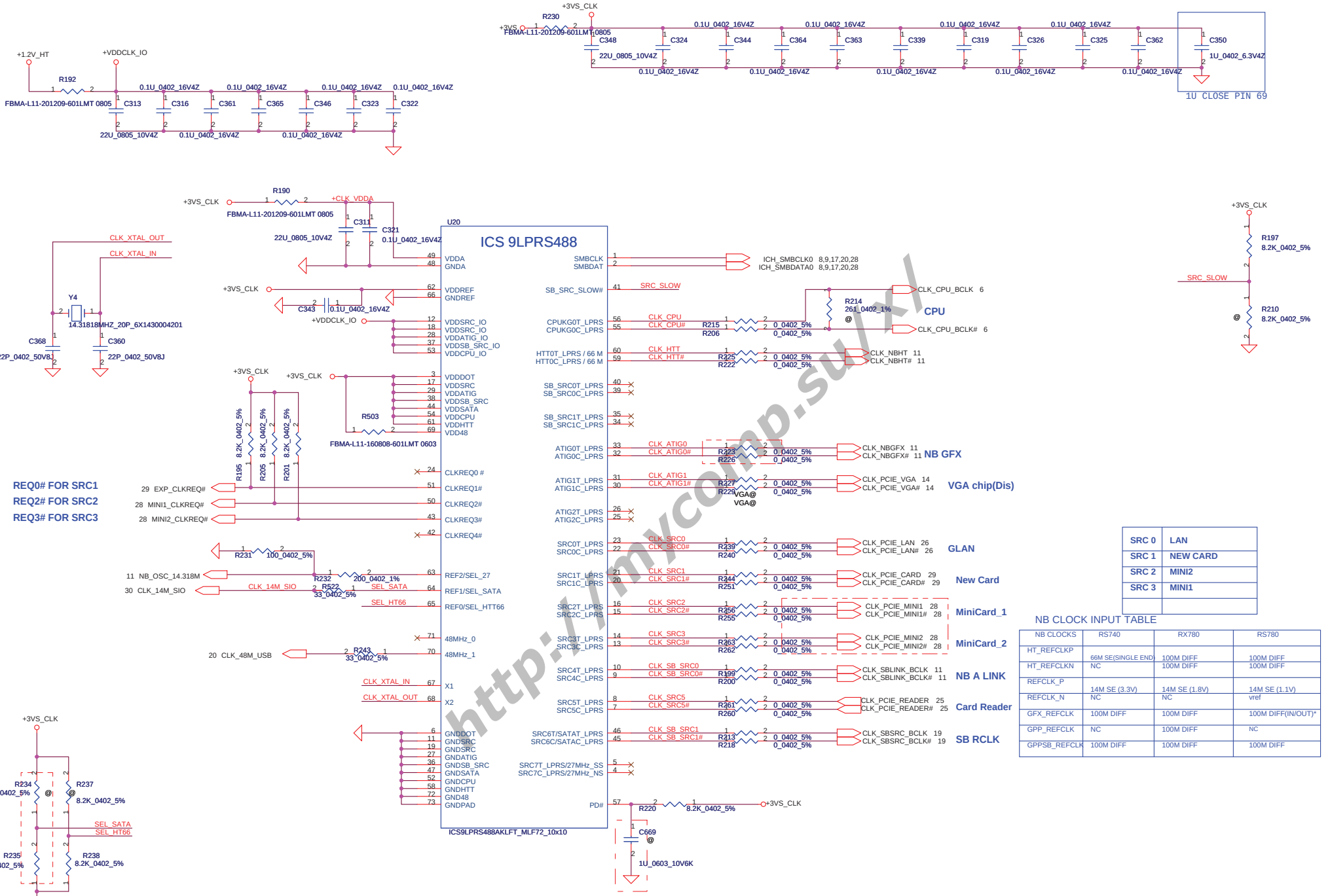
Security Classification	Compal Secret Data		
Issued Date	2008/04/16	Deciphered Date	2009/04/16

Compal Electronics, Inc.

Title: MXM Connector

Size: B | Document Number: JALB0 LA-4171P | Rev: 1.0

Date: Friday, April 18, 2008 | Sheet 14 of 50



SRC 0	LAN
SRC 1	NEW CARD
SRC 2	MINI2
SRC 3	MINI1

NB CLOCK INPUT TABLE

NB CLOCKS	RS740	RX780	RS780
HT_REFCLKP	66M SE(SINGLE END)	100M DIFF	100M DIFF
HT_REFCLKN	NC	100M DIFF	100M DIFF
REFCLK_P	14M SE (3.3V)	14M SE (1.8V)	14M SE (1.1V)
REFCLK_N	NC	NC	vref
GFX_REFCLK	100M DIFF	100M DIFF	100M DIFF(IN/OUT)*
GPP_REFCLK	NC	100M DIFF	NC
GPPSB_REFCLK	100M DIFF	100M DIFF	100M DIFF

SEL_HTT66	1	configure as single-ended 66MHz output
	0*	configure as differential 100MHz output
SEL_SATA	1*	100M_SATA SRC6 output
	0	SPREAD 100M_SATA SRC6 output

* default

NB_OSC_14.318M	1	configure as 27M and 27M_SS output
	0*	configure as SRC_7 output

Security Classification	Compal Secret Data		
Issued Date	2008/04/16	Deciphered Date	2009/04/16

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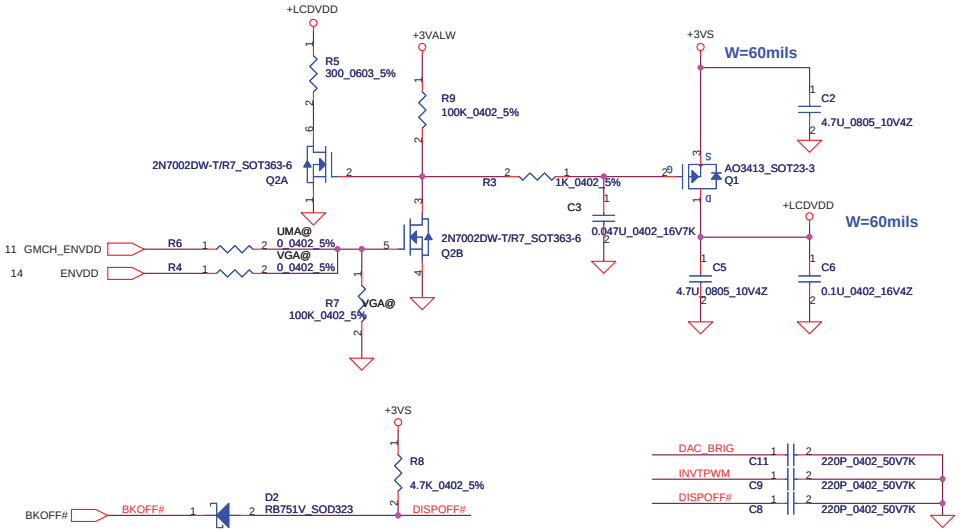
Compal Electronics, Inc.

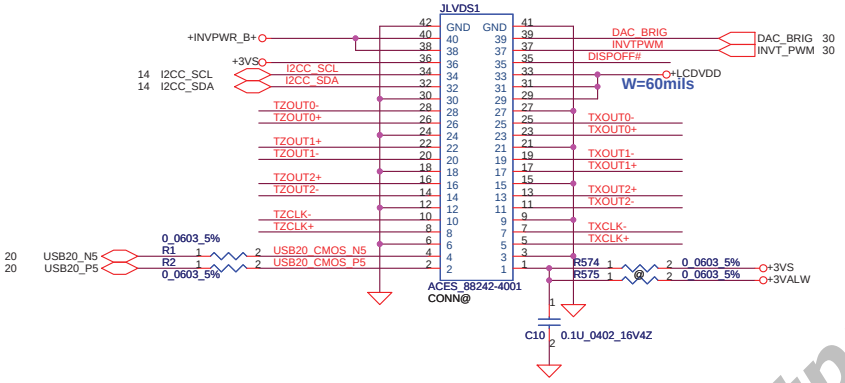
Title: **Clock generator**

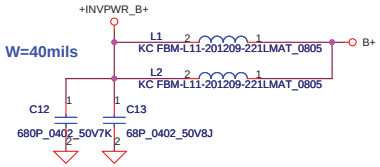
Size: Custom	Document Number: JALB0 LA-4171P	Rev: 1.0
Date: Friday, April 18, 2008	Sheet 15 of 50	

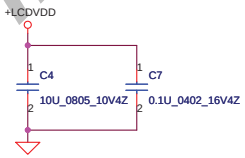
LCD POWER CIRCUIT

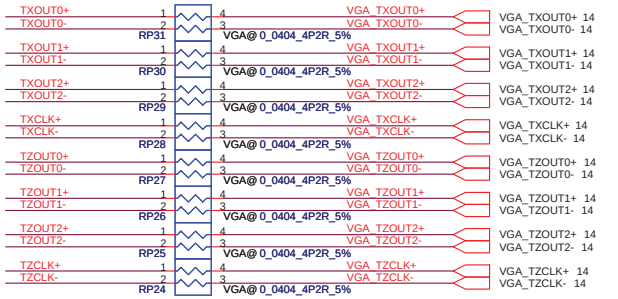


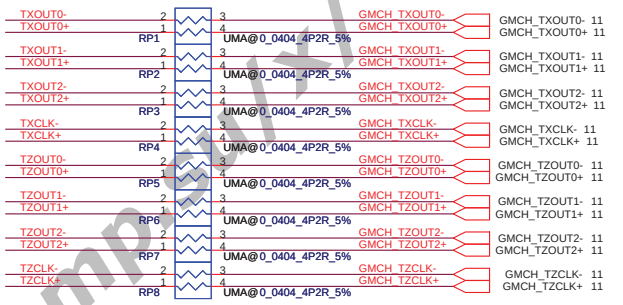
LCD/PANEL BD. Conn.











Security Classification	Compal Secret Data		
Issued Date	2008/04/16	Deciphered Date	2009/04/16

Compal Electronics, Inc.

Title: LVDS & DVI Connector

Size	Document Number	Rev
B	JALB0 LA-4171P	1.0

Date: Friday, April 18, 2008 Sheet 16 of 50

reserve HDMI I2C ESD diode

DDC to Docking

38 EC_DOCKIN
11 GMCH_DDC_CLK
14 VGA_DVI_SCLK
14 VGA_DVI_SDATA
11 GMCH_DDC_DATA
R89 UMA@ 0_0402_5%
R88 VGA@ 0_0402_5%
R98 VGA@ 0_0402_5%
R94 UMA@ 0_0402_5%
VGA_DVI_SCLK_R
VGA_DVI_SDATA_R
+HDMI_5V_OUT
R90 2K_0402_5%
R91 2K_0402_5%
Q48 BSH111 1N_SOT23-3
Q47 BSH111 1N_SOT23-3
D_DVI_SCLK 38
D_DVI_SDATA 38

DDC to HDMI CONN

18,33,38 EC_DOCKIN#_S0
R84 6.8K_0402_5%
R87 6.8K_0402_5%
Q50 BSH111 1N_SOT23-3
Q49 BSH111 1N_SOT23-3
HDMI_SCLK
HDMI_SDATA
Place closed to JHDMI1

JHDMI1
HDMI_HPD
HDMI_SDATA
HDMI_SCLK
HDMI_R_CK-
HDMI_R_CK+
HDMI_R_D0-
HDMI_R_D0+
HDMI_R_D1-
HDMI_R_D1+
HDMI_R_D2-
HDMI_R_D2+
HP_DET
+5V
DDC/CEC_GND
SDA
SCL
Reserved
CEC
CK-
CK_shield
CK+
D0-
D0_shield
D0+
D1-
D1_shield
D1+
D2-
D2_shield
D2+
GND
TYCO_1939864-1
CONN@

U41 SN74CBTD3306CPWR_TSSOP8 @
U42 SN74CBTD3306CPWR_TSSOP8 @
1A 2A 1OE# 2OE# VCC 1B 2B GND
D_DVI_SCLK D_DVI_SDATA
HDMI_SCLK HDMI_SDATA
EC_DOCKIN#_S0
EC_DOCKIN

D6 RB491D_SC59-3
F1 1.1A_6VDC_FUSE
W=40mils
+5VS
C177 0.1U_0402_16V4Z

R524 0_0402_5% D_DVI_DET 38
R123 2.2K_0402_5%
+3VS
C243 0.1U_0402_16V7K
U9 SN74AHCT1G125GW_SOT353-5
HDMI_DET 11,14
R105 100K_0402_5%
C242 0.1U_0402_16V7K

R393 4.7K_0402_5% MS
R392 @ 0_0402_5%
D22 RB751V_SOD323 OE
R400 4.7K_0402_5%

D21 SS1040_SOD123
+3VS_D80
C486 0.1U_0402_16V4Z
C485 0.1U_0402_16V4Z

NOTE: L : D-->A
H: D-->B

U28 PI3HDMI412ADZBE_TQFN56_8X8
VDD1 VDD2 VDD3 VDD4 VDD5 VDD6 VDD7 AVDD
D0+ D0- D1+ D1- D2+ D2- D3+ D3-
D3-_B D3+_B D2-_B D2+_B D1-_B D1+_B D0-_B D0+_B
D3-_A D3+_A D2-_A D2+_A D1-_A D1+_A D0-_A D0+_A
SEL_OUT SEL_IN
SCL/S3 SDA/S2
MS TEST_OUT TEST_IN OE
A0/S4 A1/S5 A2/S6 A3/S7
NC T-pad
VSS1 VSS2 VSS3 VSS4 VSS5 VSS6 VSS7 VSS8 VSS9 VSS10 AVSS

14 VGA_DVI_TXC+
14 VGA_DVI_TXC-
14 VGA_DVI_TXD0+
14 VGA_DVI_TXD0-
14 VGA_DVI_TXD1+
14 VGA_DVI_TXD1-
14 VGA_DVI_TXD2+
14 VGA_DVI_TXD2-
HDMI_TX2- HDMI_TX2+ HDMI_TX1- HDMI_TX1+ HDMI_TX0- HDMI_TX0+ HDMI_CLK- HDMI_CLK+
D_DVI_TXD2- 38
D_DVI_TXD2+ 38
D_DVI_TXD1- 38
D_DVI_TXD1+ 38
D_DVI_TXD0- 38
D_DVI_TXD0+ 38
D_DVI_TXC- 38
D_DVI_TXC+ 38
T12 PAD @
T13 PAD @
T11 PAD @
8,9,15,20,28 ICH_SMBCLK0
8,9,15,20,28 ICH_SMBDATA0
R395 @4.7K_0402_5%
R401 0_0402_5%
R396 @4.7K_0402_5%
R402 0_0402_5%
R397 @4.7K_0402_5%
R403 0_0402_5%
R398 @4.7K_0402_5%
R404 0_0402_5%
A0 A1 A2 A3

SMBus Address: 1100 000X (b)

R382 HDMI_CLK- HDMI_R_CK- L50 @WCM-2012-900T_0805
R383 HDMI_CLK+ HDMI_R_CK+
R384 HDMI_TX0- HDMI_R_D0- L51 @WCM-2012-900T_0805
R385 HDMI_TX0+ HDMI_R_D0+
R386 HDMI_TX1- HDMI_R_D1- L52 @WCM-2012-900T_0805
R387 HDMI_TX1+ HDMI_R_D1+
R388 HDMI_TX2- HDMI_R_D2- L53 @WCM-2012-900T_0805
R390 HDMI_TX2+ HDMI_R_D2+
0_0402_5%

Security Classification	Compal Secret Data		
Issued Date	2008/04/16	Deciphered Date	2009/04/16

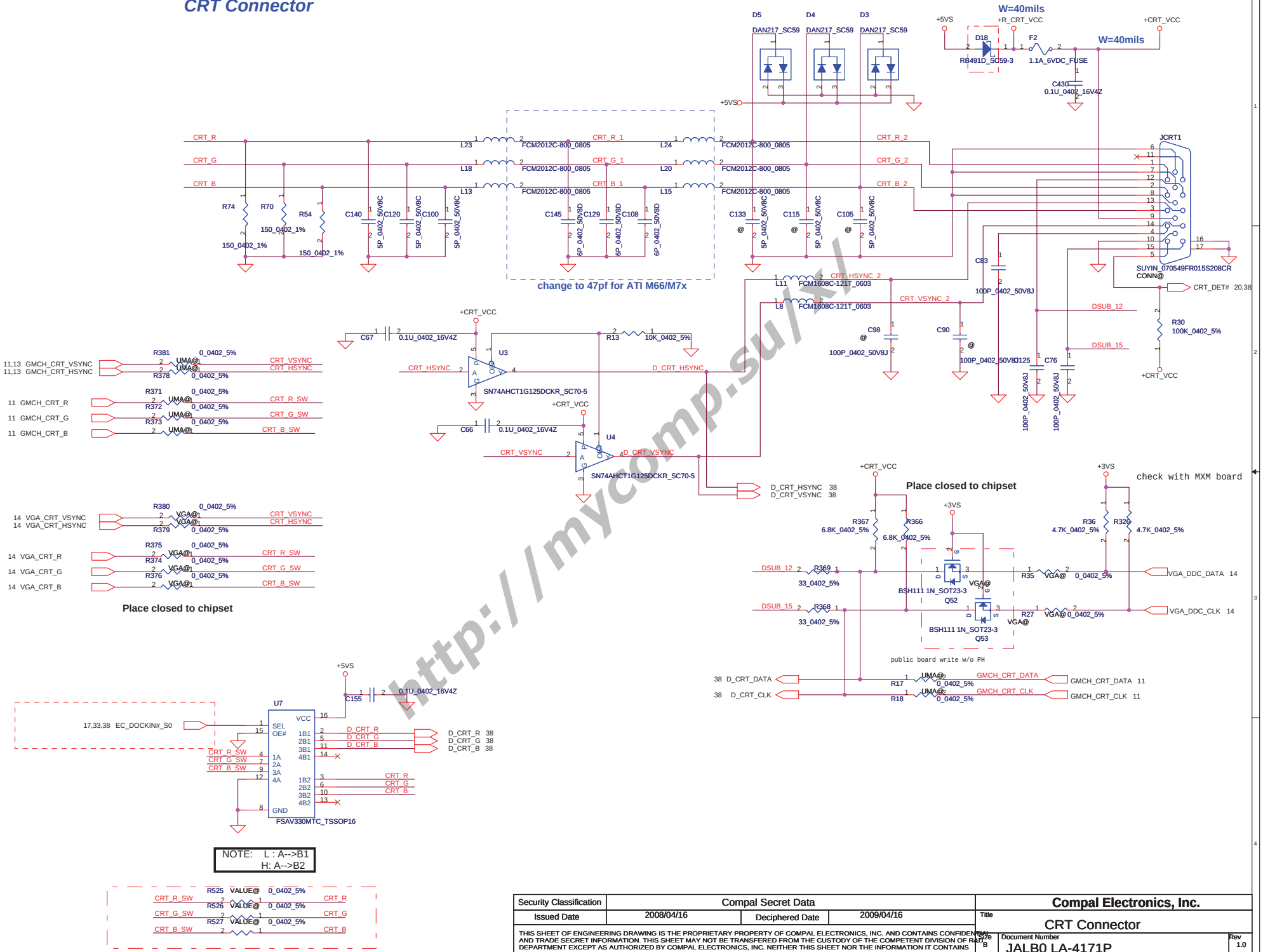
Compal Electronics, Inc.

Title: DVI/HDMI Connector

Size: Custom | Document Number: JALB0 LA-4171P | Rev: 1.0

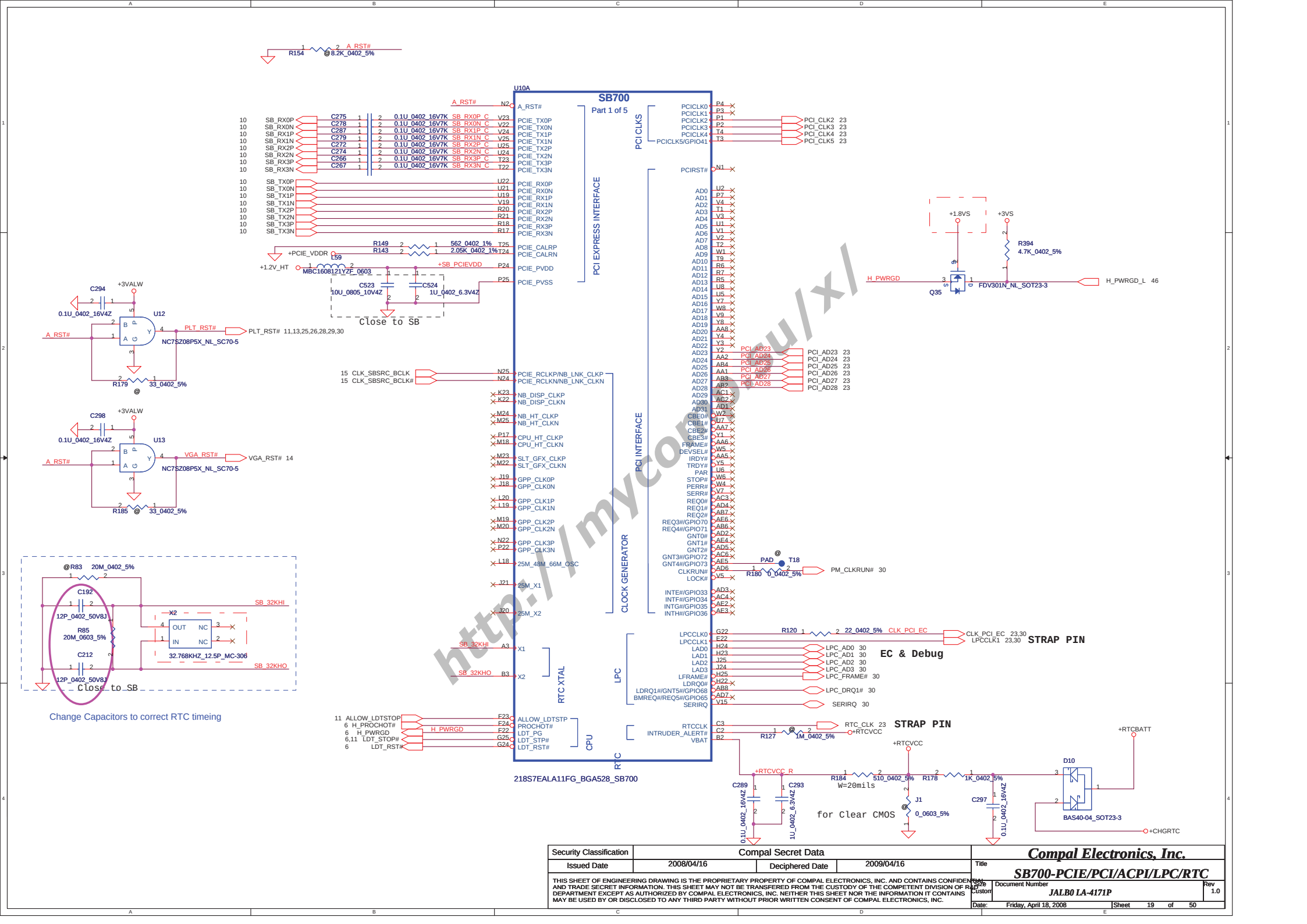
Date: Friday, April 18, 2008 | Sheet 17 of 50

CRT Connector



Security Classification	Compal Secret Data		
Issued Date	2008/04/16	Deciphered Date	2009/04/16

Compal Electronics, Inc.	
Title	CRT Connector
Size	B
Document Number	JALB0 LA-4171P
Rev	1.0
Date:	Friday, April 18, 2008
Sheet	18 of 50



Security Classification	Compal Secret Data		
Issued Date	2008/04/16	Deciphered Date	2009/04/16

Title	Compal Electronics, Inc.
	SB700-PCIE/PCI/ACPI/LPC/RTC
Size: Custom	Document Number: JALB0 LA-4171P
Rev	1.0
Date:	Friday, April 18, 2008
Sheet	19 of 50

SKU-ID	R509	R510
UMA		POP
DIS	POP	

demo circuit LID use RI#

SB700 has internal PD

U10D

SB700 Part 4 of 5

218S7EALA11FG_BGA528_SB700

USB-11 New Card
USB-10 MiniCard(TV tuner)
USB-9 Bluetooth
USB-8 WLAN
USB-7 M/B
USB-5 USB Camera
USB-4 TV/B
USB-3 DOCK
USB-2 USB/B
USB-1 Fingerprint
USB-0 M/B

STRAP PIN

FOR Nvidia VGA/B

SB Power Domain :S5

High: CRT Plugged

Security Classification	Compal Secret Data		
Issued Date	2008/04/16	Deciphered Date	2009/04/16

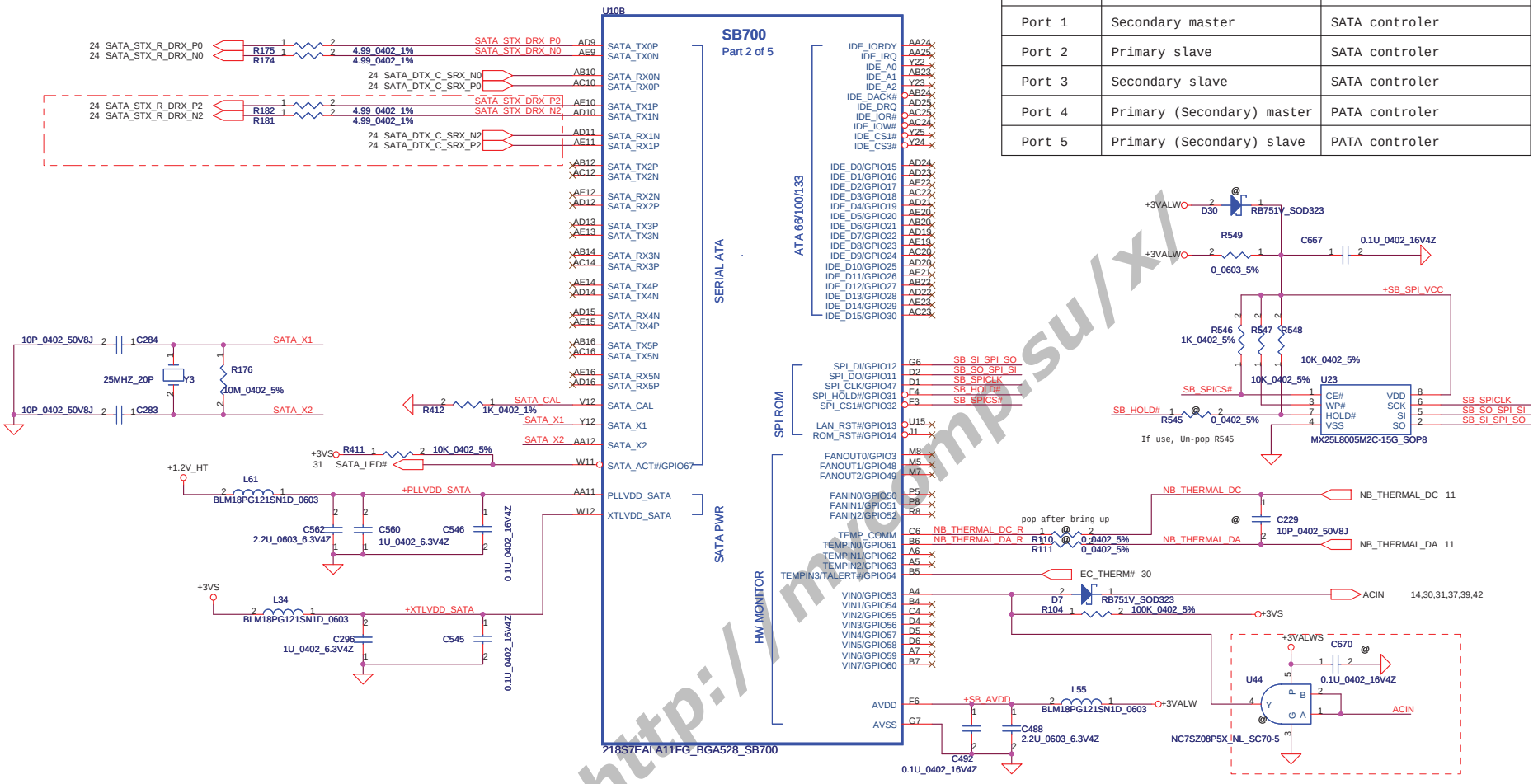
Compal Electronics, Inc.

Title: SB700 USB/HD audio

Size: Custom | Document Number: JALB0 LA-4171P | Rev: 1.0

Date: Friday, April 18, 2008 | Sheet 20 of 50

Port Number	Pri/SEC,Mas/Slave assignment	SATA drive controlled by
Port 0	Primary master	SATA controler
Port 1	Secondary master	SATA controler
Port 2	Primary slave	SATA controler
Port 3	Secondary slave	SATA controler
Port 4	Primary (Secondary) master	PATA controler
Port 5	Primary (Secondary) slave	PATA controler



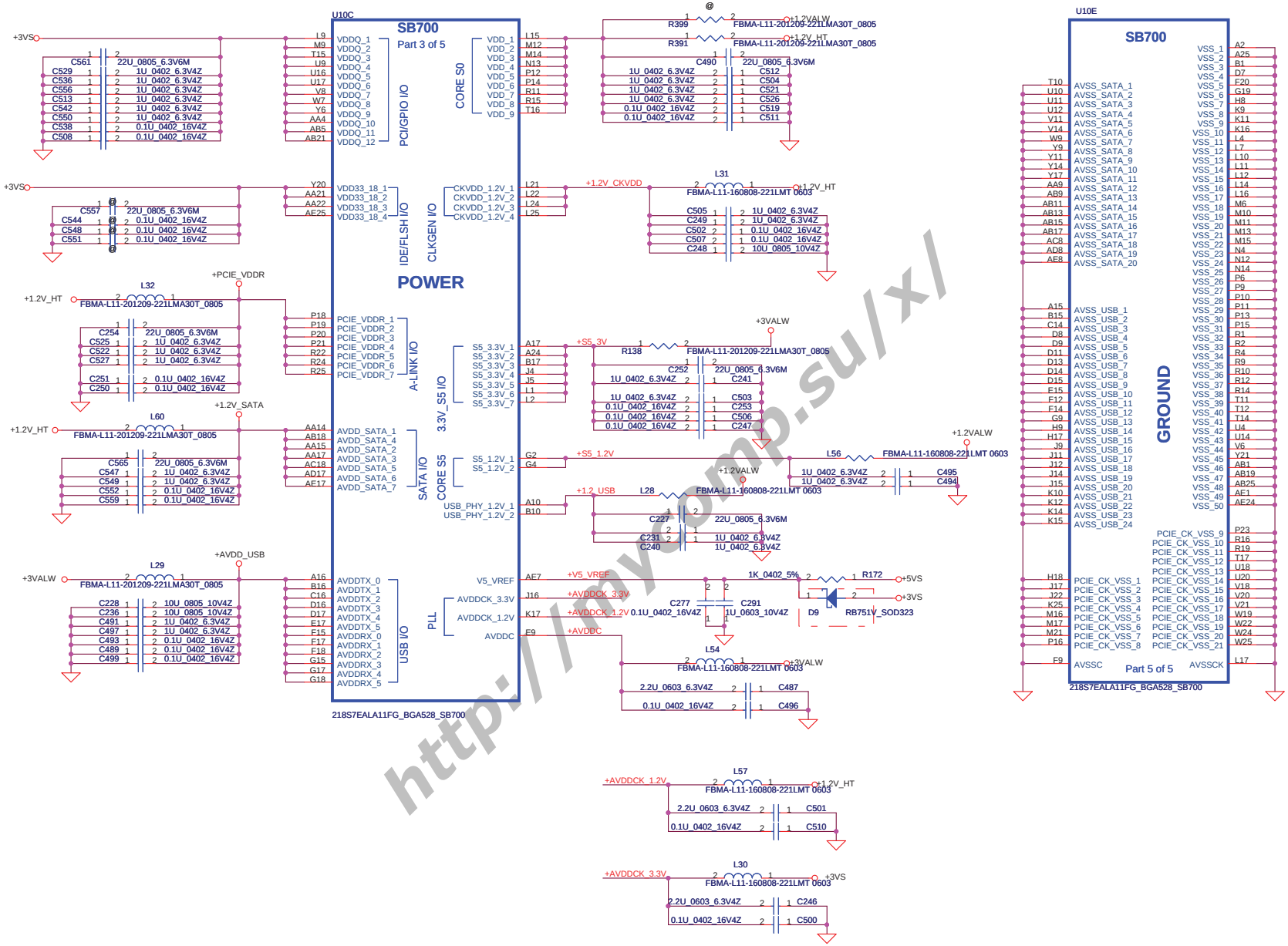
Security Classification	Compal Secret Data		
Issued Date	2008/04/16	Deciphered Date	2009/04/16

Compal Electronics, Inc.

Title: SB700 SATA/IDE/SPI

Size: Custom	Document Number: JALB0 LA-4171P	Rev: 1.0
Date: Friday, April 18, 2008	Sheet 21 of 50	

FOR SB700 ALL issue
A12 Will change to +1.2V_HT



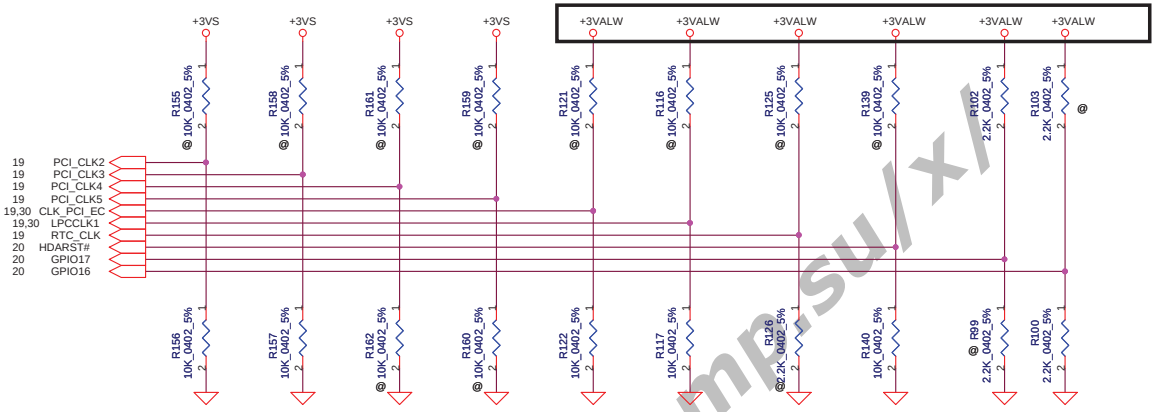
Security Classification	Compal Secret Data		
Issued Date	2008/04/16	Deciphered Date	2009/04/16

Compal Electronics, Inc.			
Title: SB700 power/GND			
Size: Custom	Document Number: JALB0 LA-4171P		Rev: 1.0
Date: Friday, April 18, 2008	Sheet 22 of 50		

REQUIRED STRAPS

NOTE: SB700 HAS INTERNAL 15K PULL UP RESISTOR FOR RTC_CLK

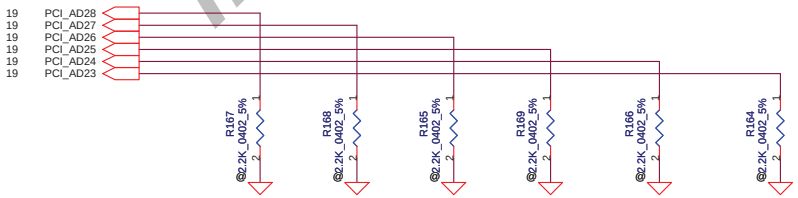
	PCI_CLK2 CLK_PCI_PCM	PCI_CLK3 CLK_PCI_DBG	PCI_CLK4	PCI_CLK5	LPC_CLK0 CLK_PCI_EC	LPC_CLK1	RTC_CLK	AZ_RST_CD#	GP17 GP16
PULL HIGH	BOOTFAIL TIMER ENABLED	USE DEBUG STRAPS	RESERVED	RESERVED	ENABLE PCI MEM BOOT	CLKGEN ENABLED	**INTERNAL RTC** DEFAULT	EC ENABLED	Internal pull up H,H = Reserved H,L = SPI ROM **L,H = LPC ROM (Default L,NC)** L,L = FWH ROM
PULL LOW	**BOOTFAIL TIMER DISABLED** DEFAULT	**IGNORE DEBUG STRAPS** DEFAULT			**DISABLE PCI MEM BOOT** DEFAULT	**CLKGEN DISABLED** DEFAULT	**EXT. RTC** (PD on X1, apply 32KHz to RTC_CLK)	**EC DISABLED** DEFAULT	



DEBUG STRAPS

SB700 HAS 15K INTERNAL PU FOR PCI_AD[28:23]

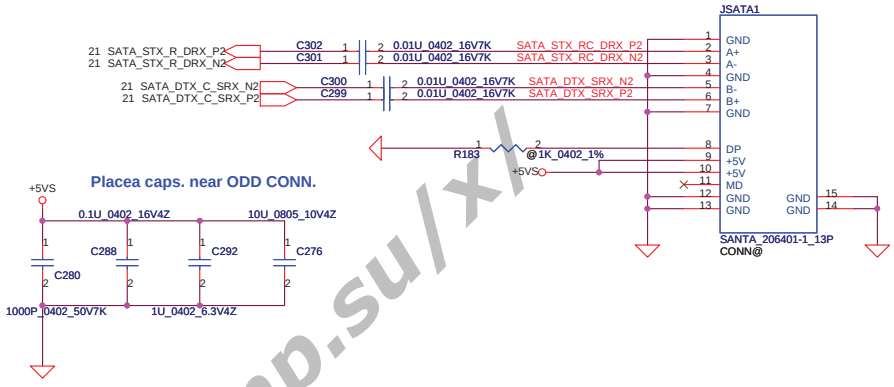
	PCI_AD28	PCI_AD27	PCI_AD26	PCI_AD25	PCI_AD24	PCI_AD23
PULL HIGH	**USE LONG RESET** DEFAULT	**USE PCI PLL** DEFAULT	**USE ACPI BCLK** DEFAULT	**USE IDE PLL** DEFAULT	**USE DEFAULT PCIE STRAPS** DEFAULT	**RESERVED**
PULL LOW	USE SHORT RESET	BYPASS PCI PLL	BYPASS ACPI BCLK	BYPASS IDE PLL	USE EEPROM PCIE STRAPS	



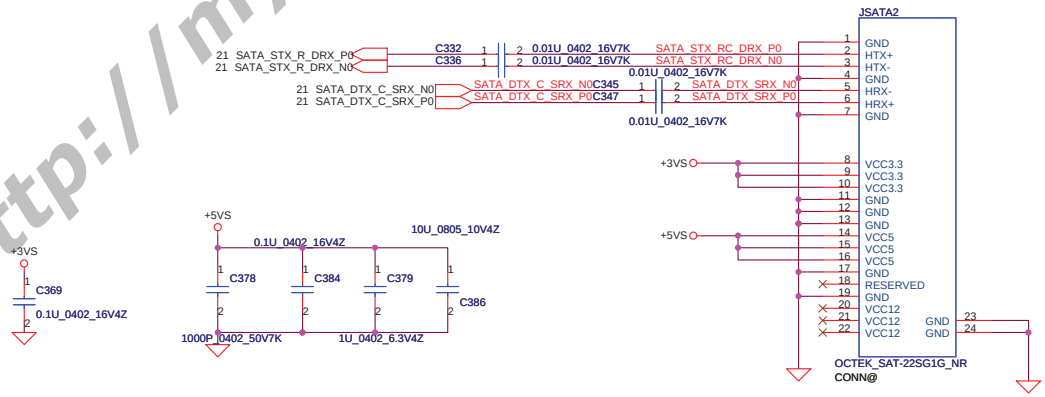
Security Classification	Compal Secret Data		
Issued Date	2008/04/16	Deciphered Date	2009/04/16

Compal Electronics, Inc.			
Title: SB700 STRAPS			
Size: Custom	Document Number: JALB0 LA-4171P		Rev: 1.0
Date: Friday, April 18, 2008	Sheet 23 of 50		

SATA ODD Conn.

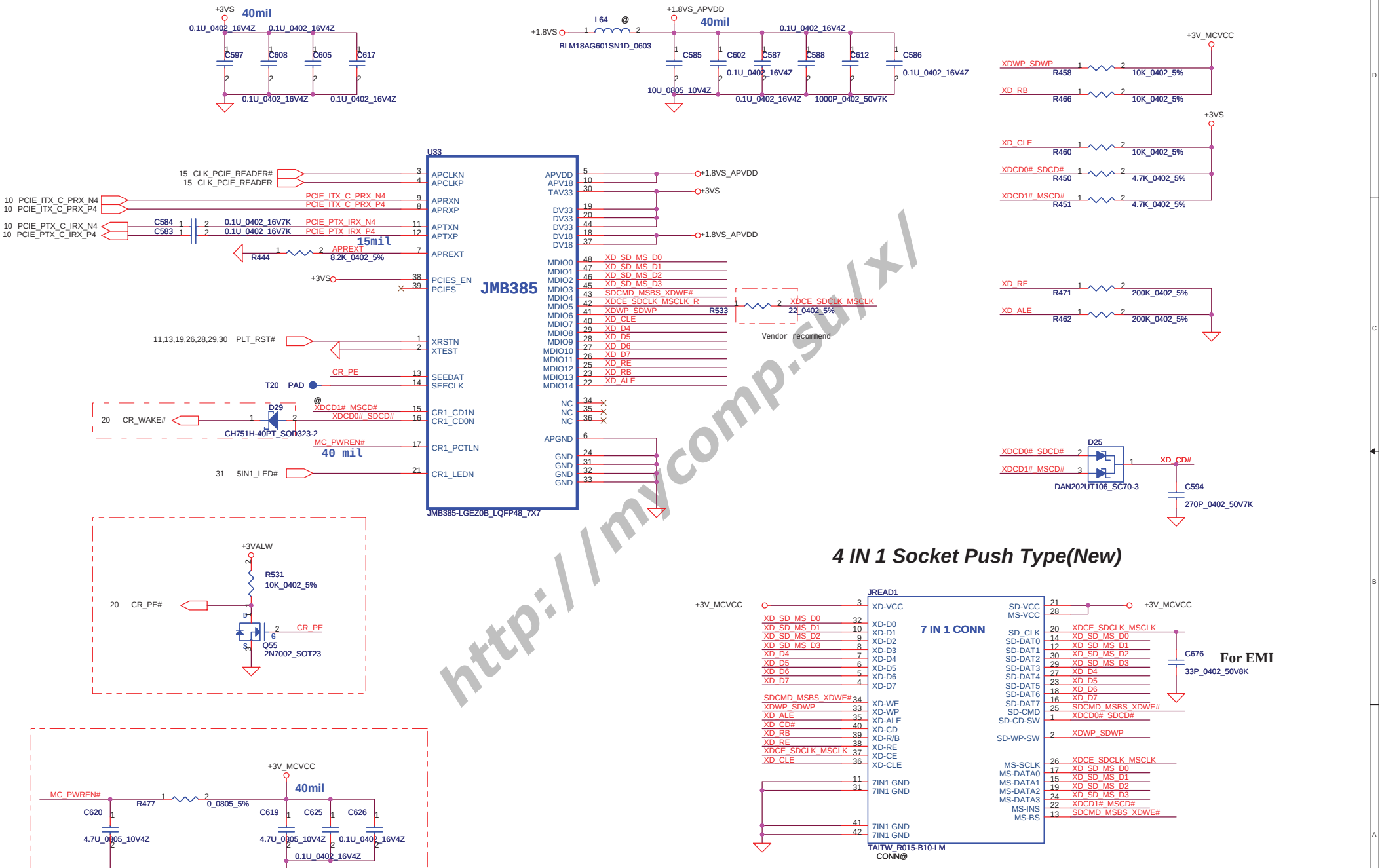


SATA HDD Conn.



Security Classification	Compal Secret Data		Compal Electronics, Inc.
Issued Date	2008/04/16	Deciphered Date 2009/04/16	Title: HDD & ODD Connector

Size: B	Document Number: JALB0 LA-4171P		Rev: 1.0
Date: Friday, April 18, 2008	Sheet 24 of 50		



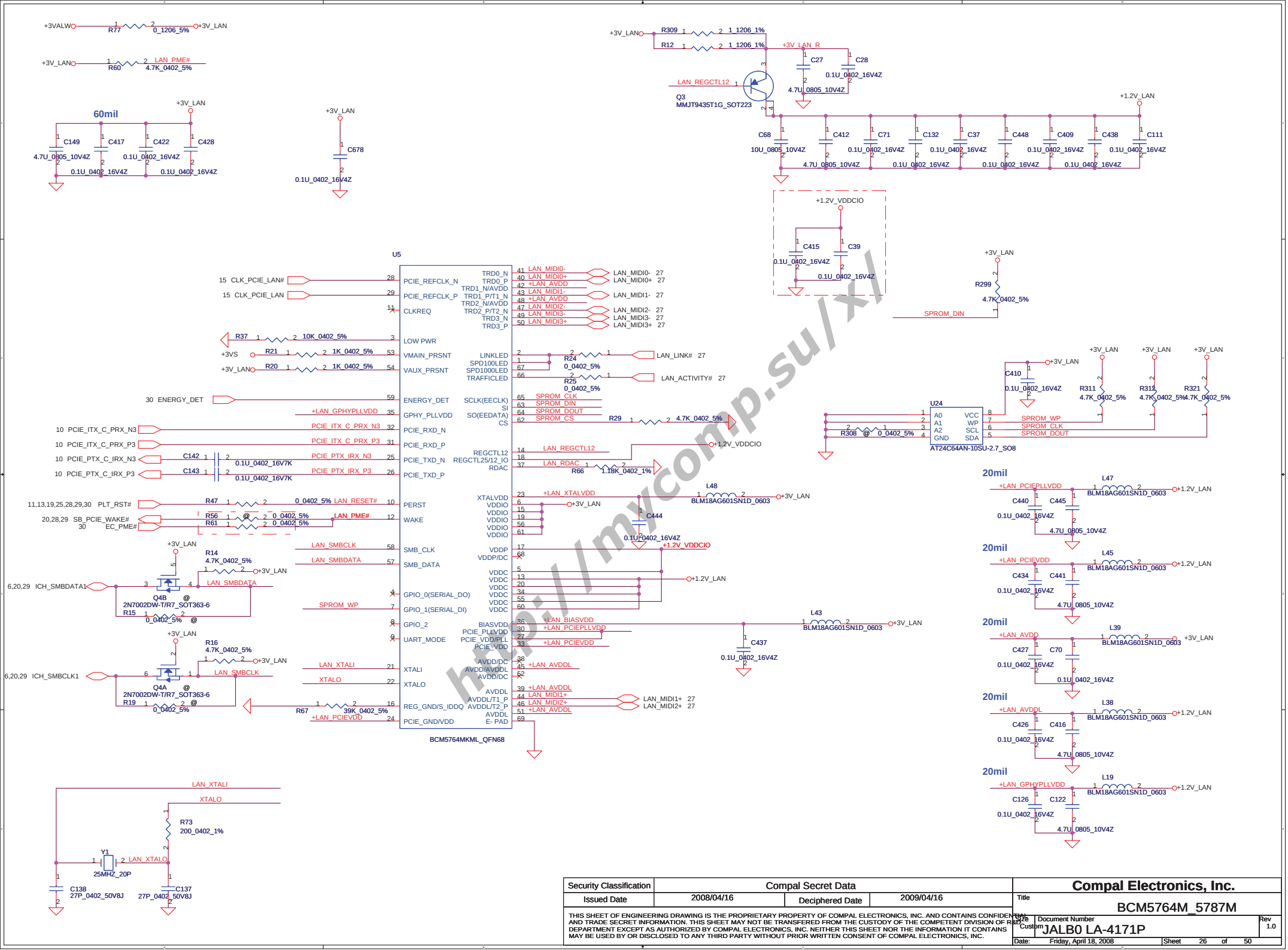
Security Classification	Compal Secret Data		
Issued Date	2008/04/16	Deciphered Date	2009/04/16

Compal Electronics, Inc.

Title: Card Reader JMB385

Size: Custom | Document Number: JALB0 LA-4171P | Rev: 1.0

Date: Friday, April 18, 2008 | Sheet 25 of 50



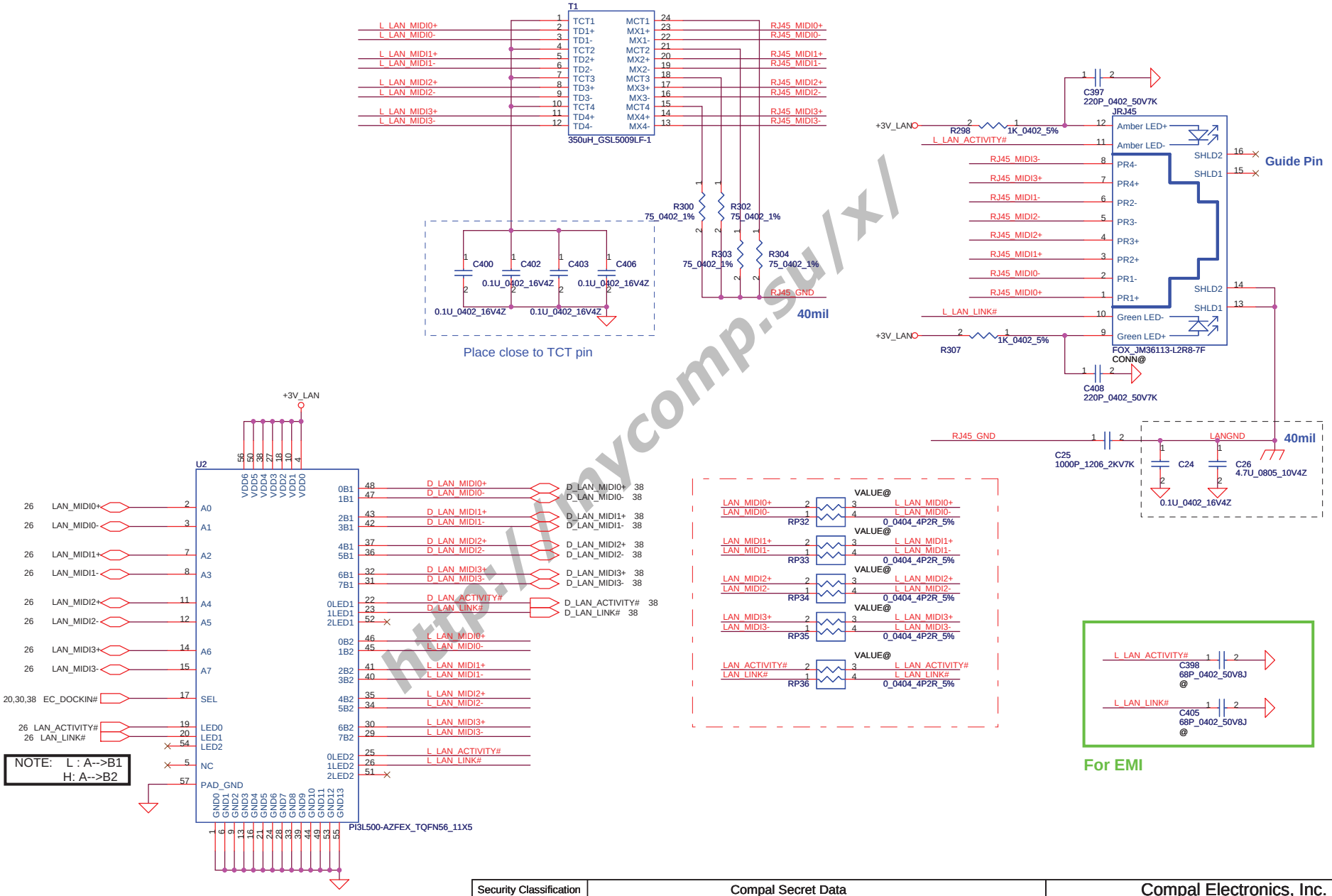
Security Classification	Compal Secret Data		
Issued Date	2008/04/16	Deciphered Date	2009/04/16

Compal Electronics, Inc.

Title: BCM5764M_5787M

Size: Custom | Document Number: JALB0 LA-4171P | Rev: 1.0

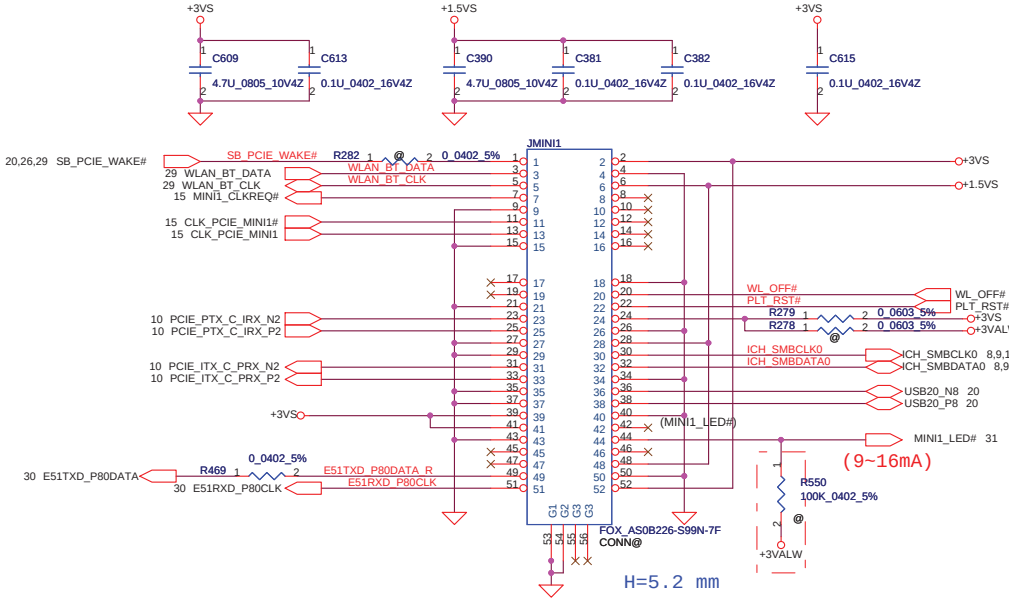
Date: Friday, April 18, 2008 | Sheet 26 of 50



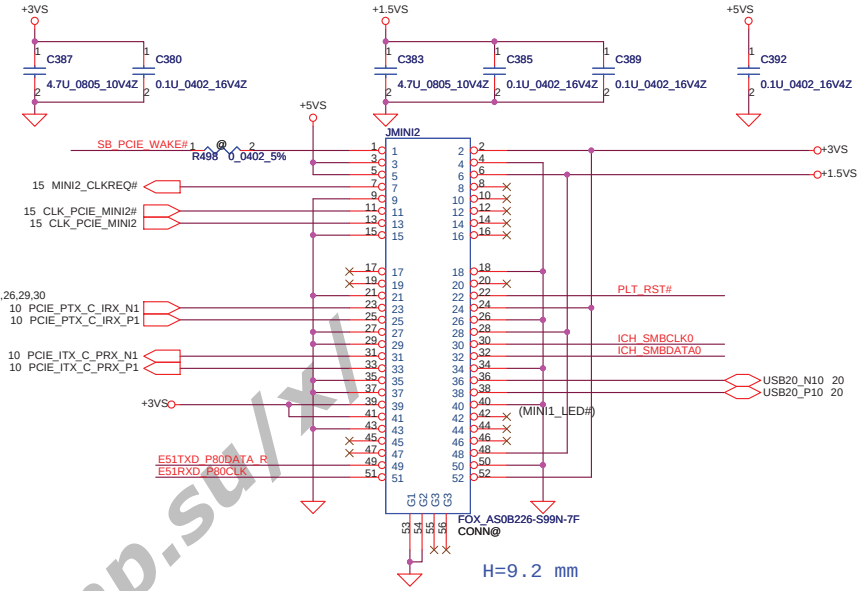
Security Classification	Compal Secret Data		
Issued Date	2008/04/16	Deciphered Date	2009/04/16

Compal Electronics, Inc.			
Title	LAN Magnetic & RJ45/RJ11		
Size B	Document Number JALB0 LA-4171P		Rev 1.0
Date: Friday, April 18, 2008	Sheet 27 of 50		

For Wireless LAN

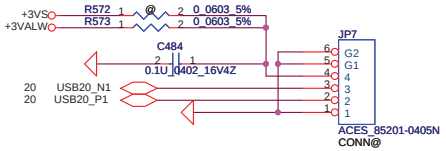


For TV-Tuner/HW MPEG

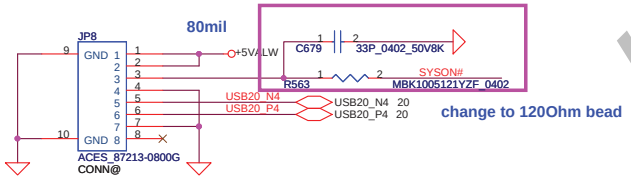


Mini Card Power Rating			
Power	Primary Power (mA)		Auxiliary Power (mA)
	Peak	Normal	Normal
+3VS	1000	750	
+3V	330	250	250 (wake enable)
+1.5VS	500	375	5 (Not wake enable)

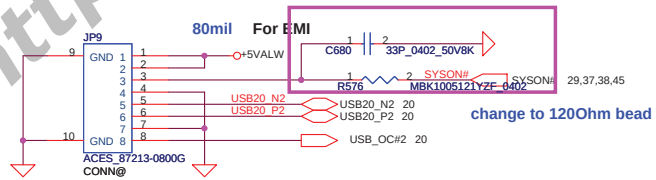
Fingerprint Conn

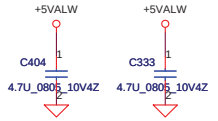


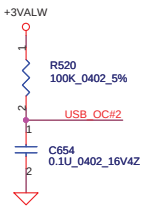
To USB/B Connector



To USB/B Connector







Security Classification	Compal Secret Data		
Issued Date	2008/04/16	Deciphered Date	2009/04/16

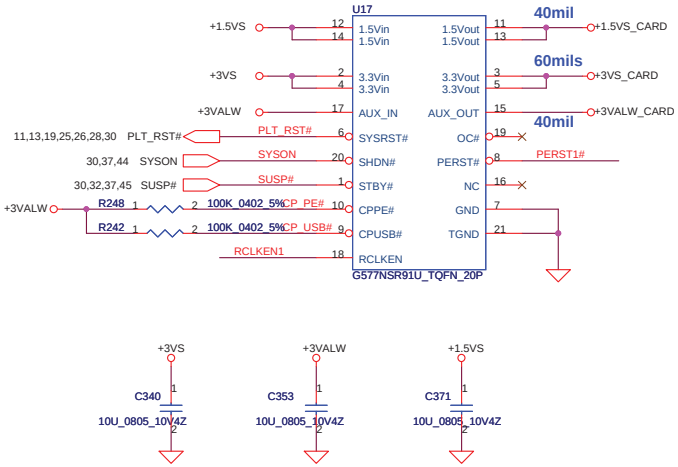
Compal Electronics, Inc.

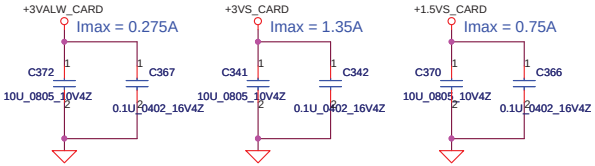
Title: MINI CARD (WLAN & TV-Tuner)

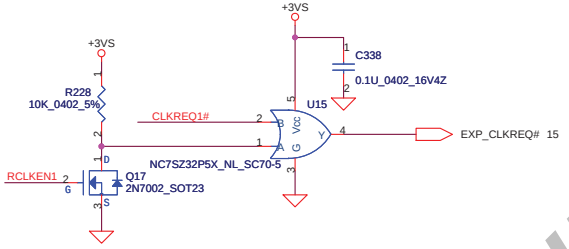
Size: B | Document Number: JALB0 LA-4171P | Rev: 1.0

Date: Friday, April 18, 2008 | Sheet 28 of 50

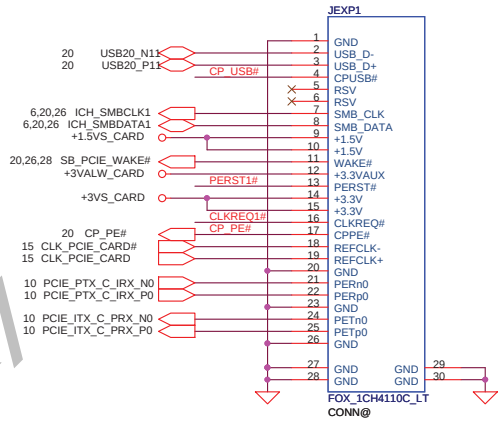
New Card Power Switch



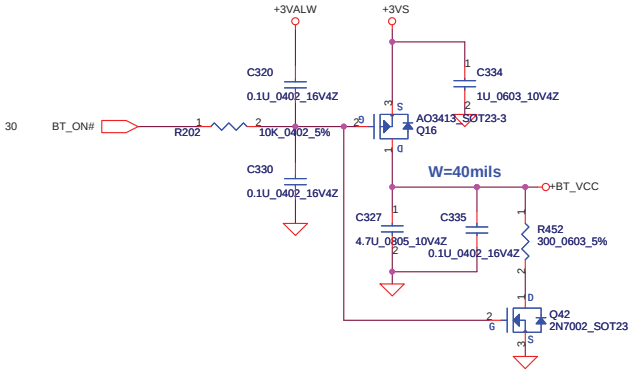


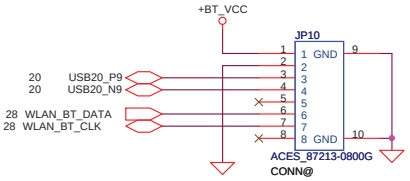


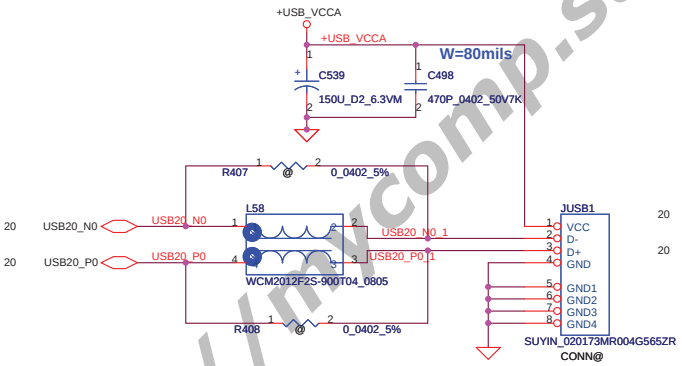
New Card Socket (Left/TOP)

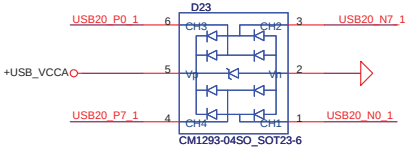


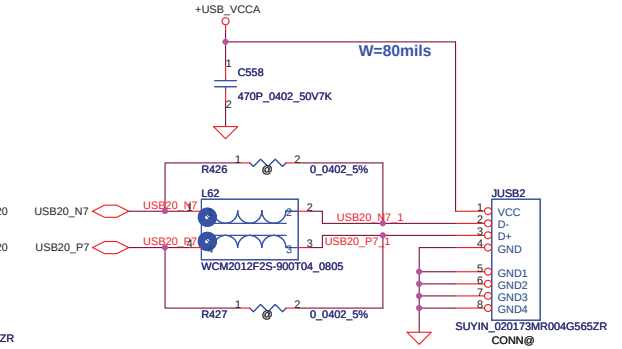
Bluetooth Conn.

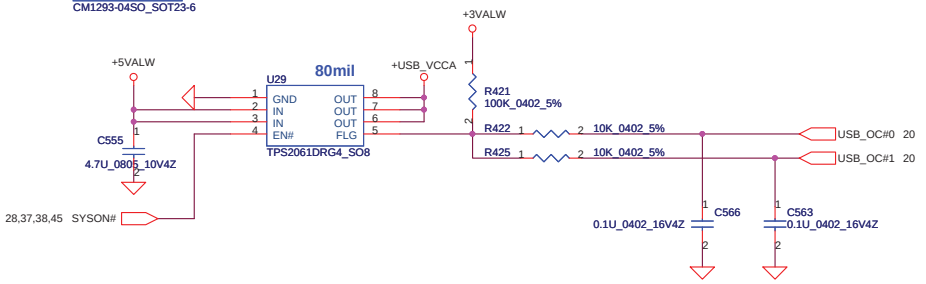






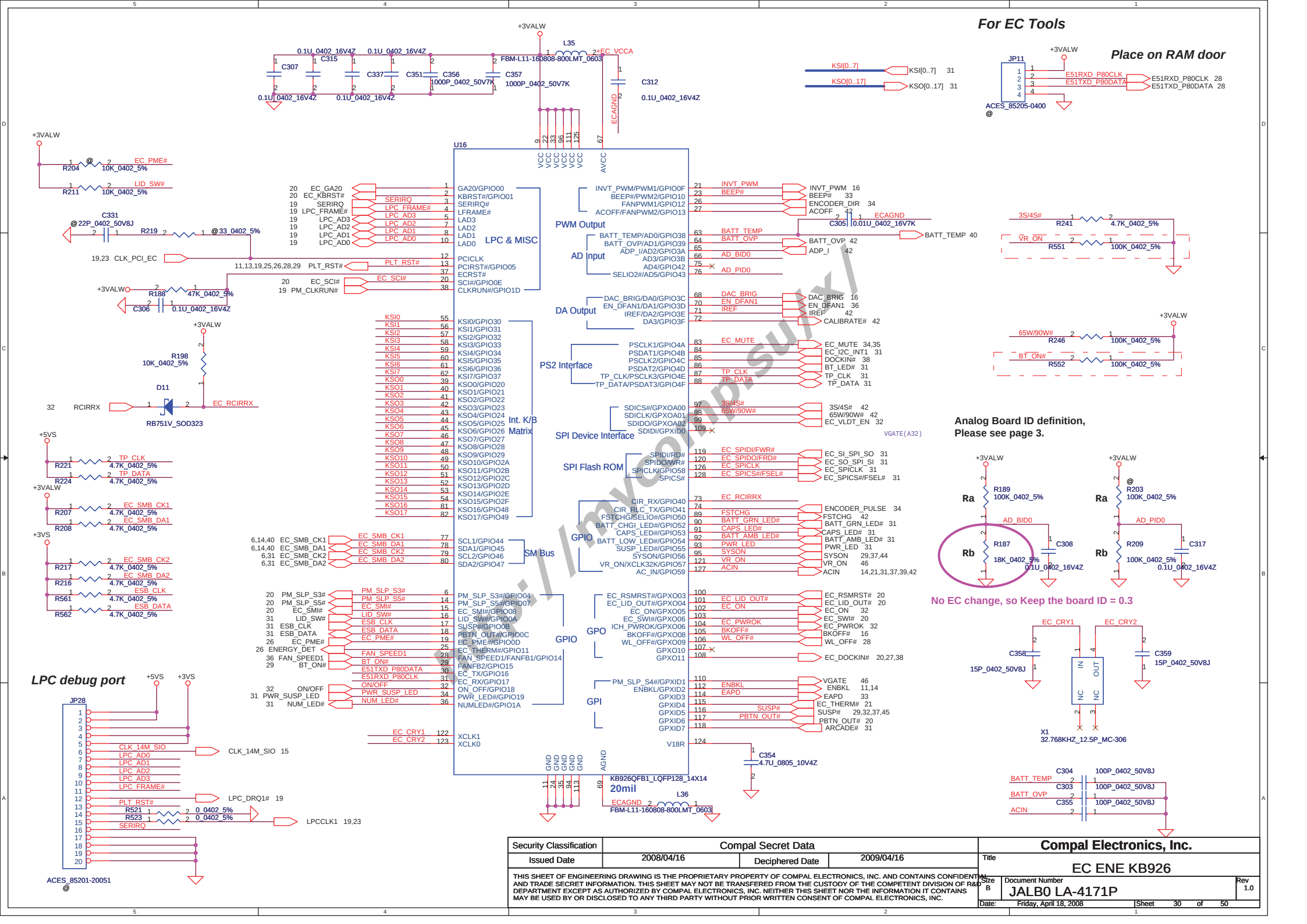


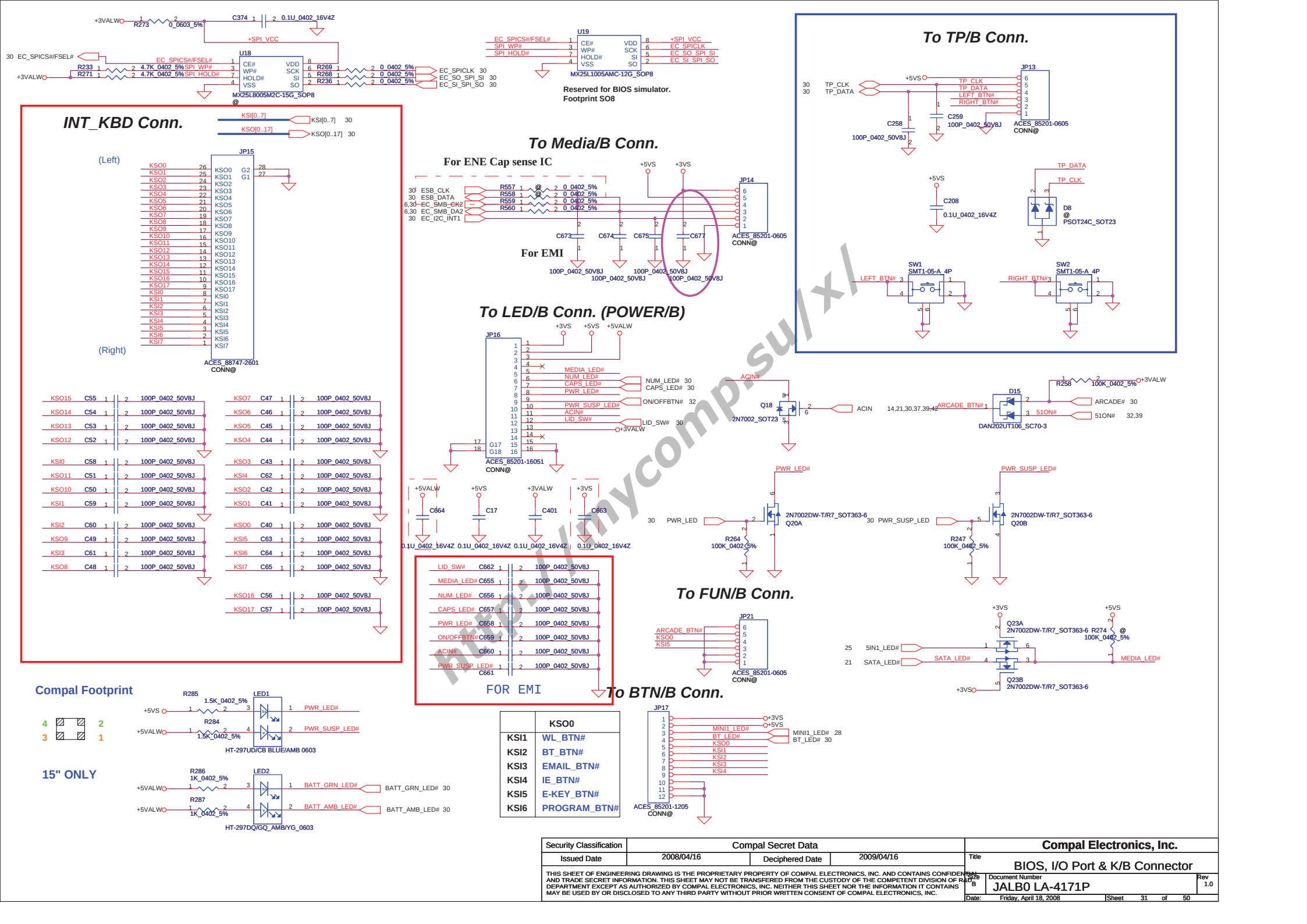




Security Classification	Compal Secret Data		
Issued Date	2008/04/16	Deciphered Date	2009/04/16

Compal Electronics, Inc.	
Title	NEW CARD & USB Connector
Size B	Document Number JALB0 LA-4171P
Rev	1.0
Date: Friday, April 18, 2008	Sheet 29 of 50


For EC Tools
Place on RAM door
LPC debug port
U16
KB926QFB1_LQFP128_14X14
20mil
Analog Board ID definition,
Please see page 3.
No EC change, so Keep the board ID = 0.3
LPC & MISC
PWM Output
AD Input
DA Output
PS2 Interface
Int. K/B Matrix
SPI Device Interface
SPI Flash ROM
GPIO
SM Bus
GPO
GPI
Compal Secret Data
Compal Electronics, Inc.
EC ENE KB926
JALB0 LA-4171P
2008/04/16
2009/04/16
Friday, April 18, 2008
Sheet 30 of 50

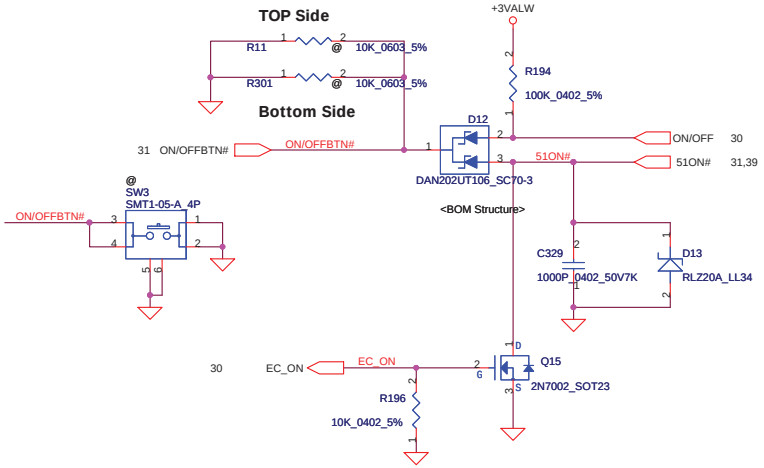


	KSO0
KSI1	WL_BTN#
KSI2	BT_BTN#
KSI3	EMAIL_BTN#
KSI4	IE_BTN#
KSI5	E-KEY_BTN#
KSI6	PROGRAM_BTN#

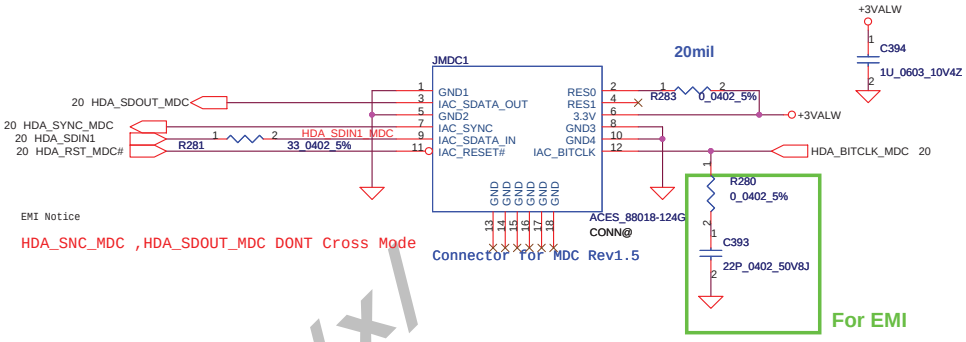
Security Classification	Compal Secret Data		Compal Electronics, Inc.
Issued Date	2008/04/16	Deciphered Date	2009/04/16
Title	BIOS, I/O Port & K/B Connector		
Size B	Document Number JALB0 LA-4171P		Rev 1.0
Date: Friday, April 18, 2008	Sheet 31 of 50		

Power Button

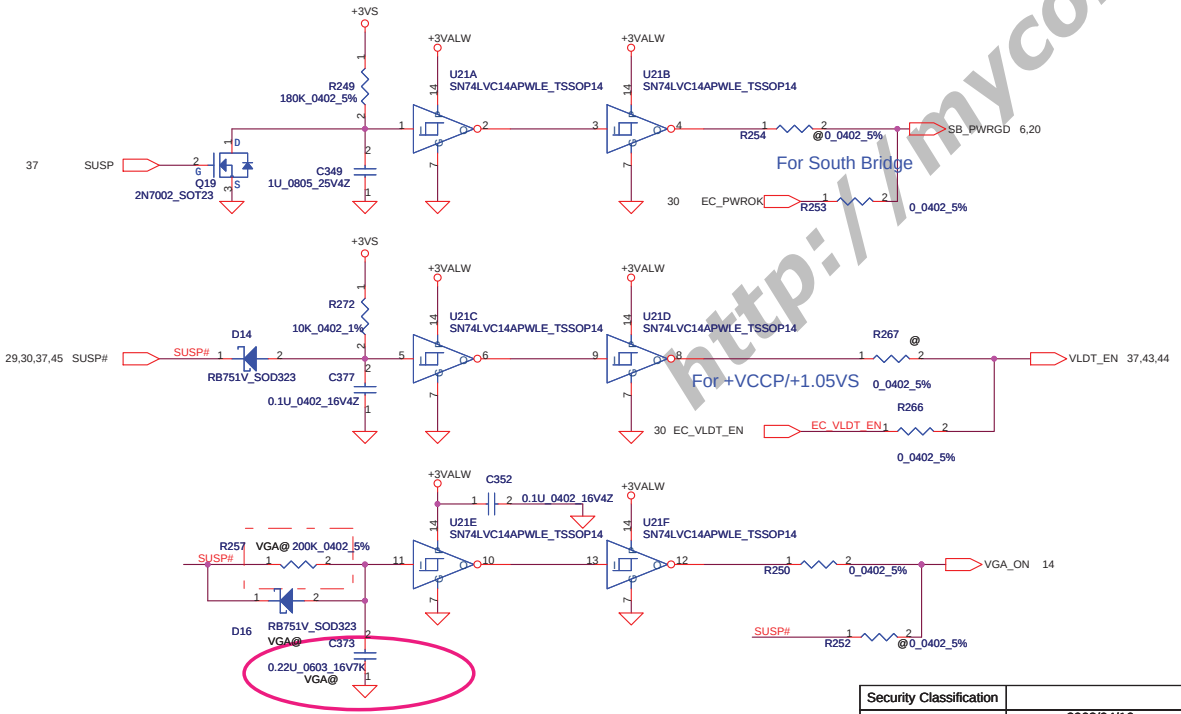
ON/OFF switch



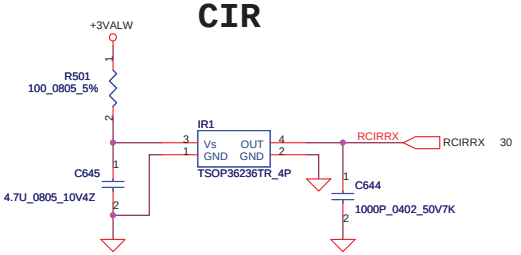
HDA MDC Conn.



Power ON Circuit



CIR



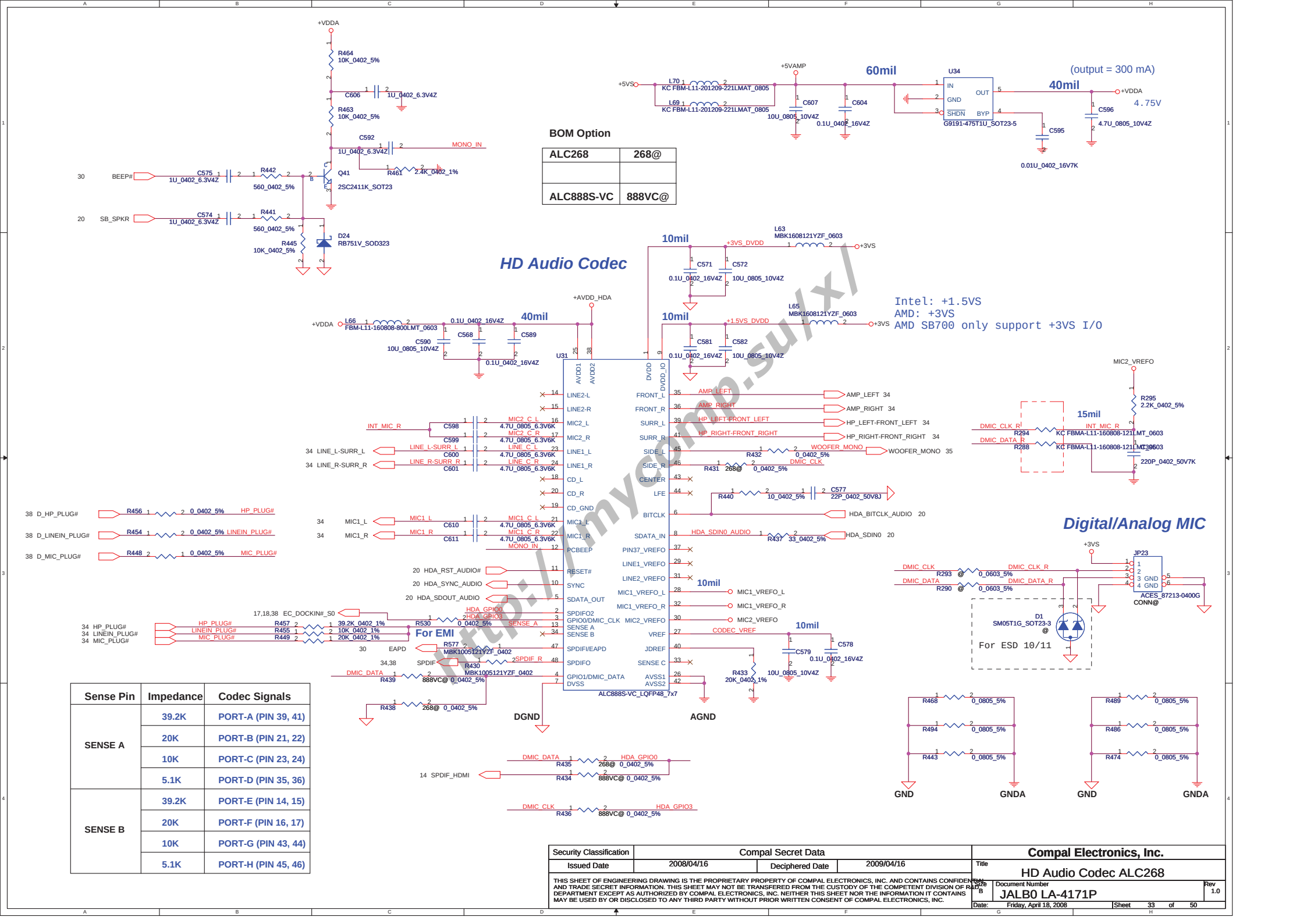
Security Classification	Compal Secret Data		
Issued Date	2008/04/16	Deciphered Date	2009/04/16

Compal Electronics, Inc.

Title: Power OK, Reset and RTC Circuit, TP

Size: B | Document Number: JALB0 LA-4171P | Rev: 1.0

Date: Friday, April 18, 2008 | Sheet 32 of 50



Sense Pin	Impedance	Codec Signals
SENSE A	39.2K	PORT-A (PIN 39, 41)
	20K	PORT-B (PIN 21, 22)
	10K	PORT-C (PIN 23, 24)
	5.1K	PORT-D (PIN 35, 36)
SENSE B	39.2K	PORT-E (PIN 14, 15)
	20K	PORT-F (PIN 16, 17)
	10K	PORT-G (PIN 43, 44)
	5.1K	PORT-H (PIN 45, 46)

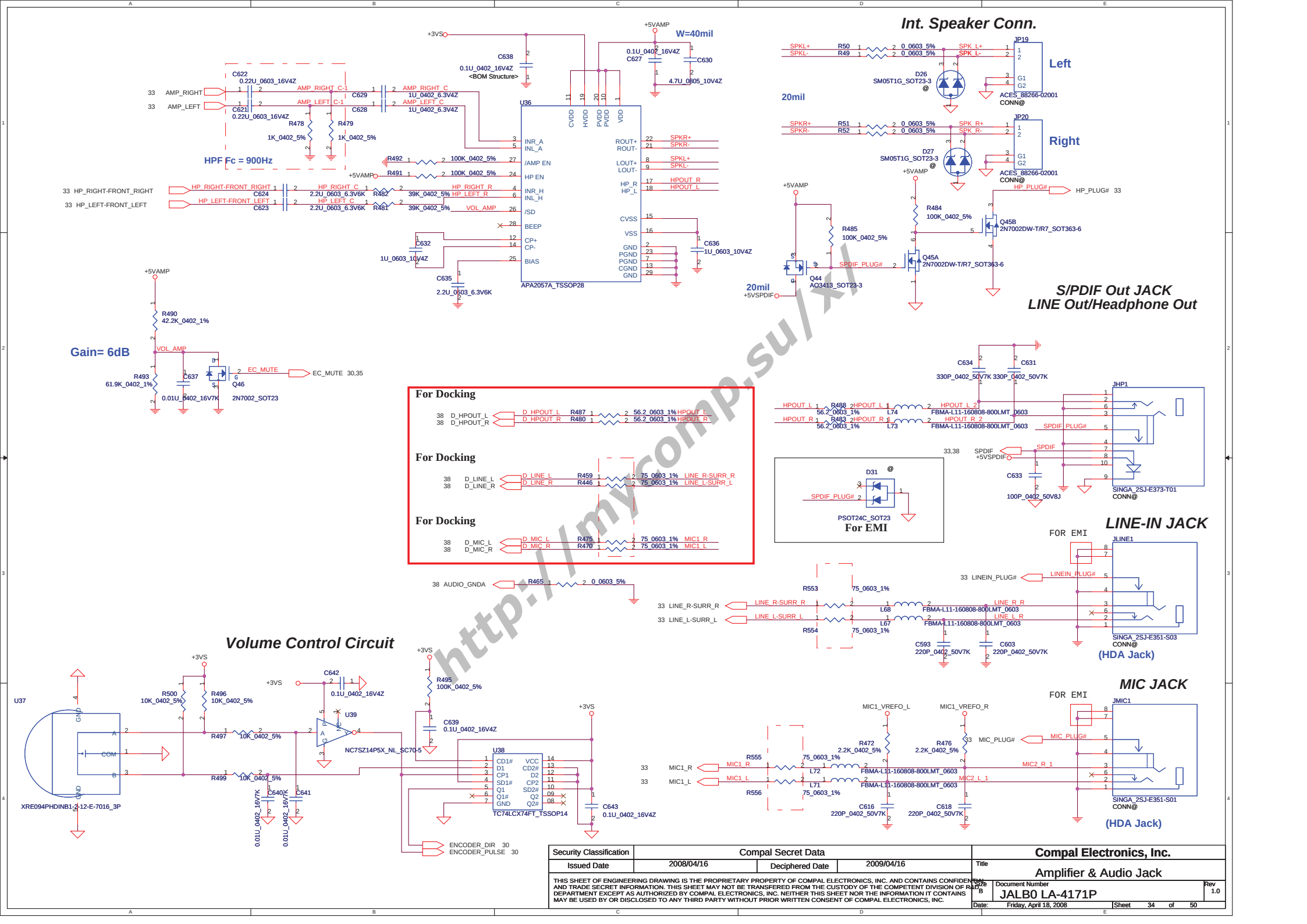
Security Classification	Compal Secret Data		
Issued Date	2008/04/16	Deciphered Date	2009/04/16

Compal Electronics, Inc.

Title: HD Audio Codec ALC268

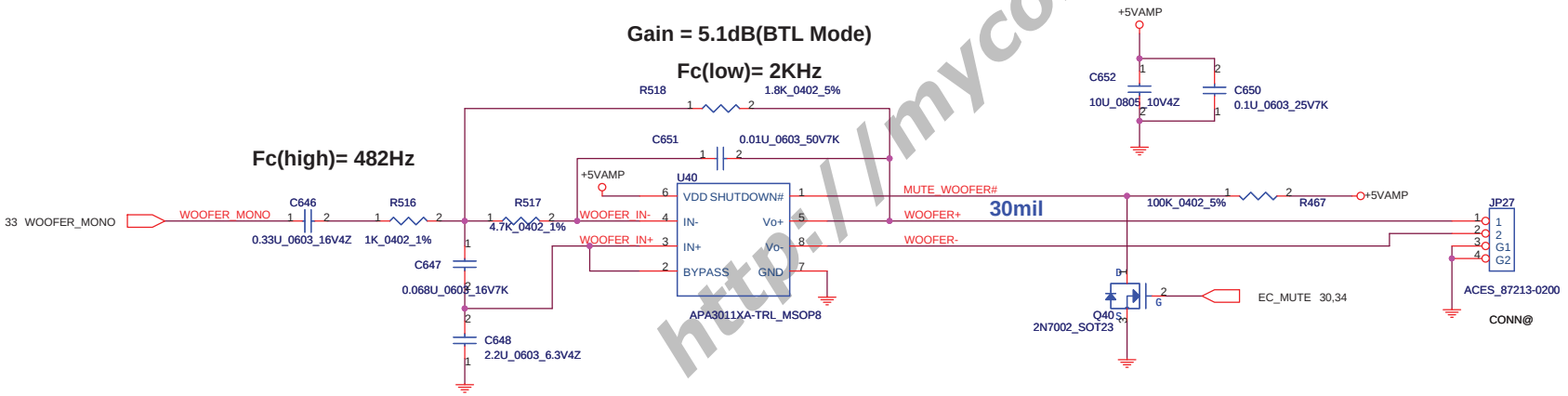
Size: B | Document Number: JALB0 LA-4171P | Rev: 1.0

Date: Friday, April 18, 2008 | Sheet 33 of 50



Security Classification	Compal Secret Data		
Issued Date	2008/04/16	Deciphered Date	2009/04/16

Compal Electronics, Inc.	
Title	Amplifier & Audio Jack
Size: B	Document Number: JALB0 LA-4171P
Rev	1.0
Date: Friday, April 18, 2008	Sheet 34 of 50



Security Classification	Compal Secret Data		
Issued Date	2008/04/16	Deciphered Date	2009/04/16

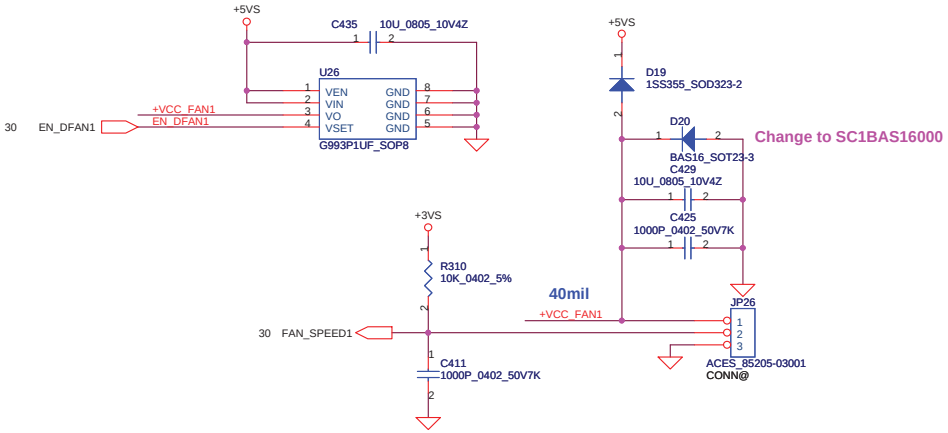
Compal Electronics, Inc.

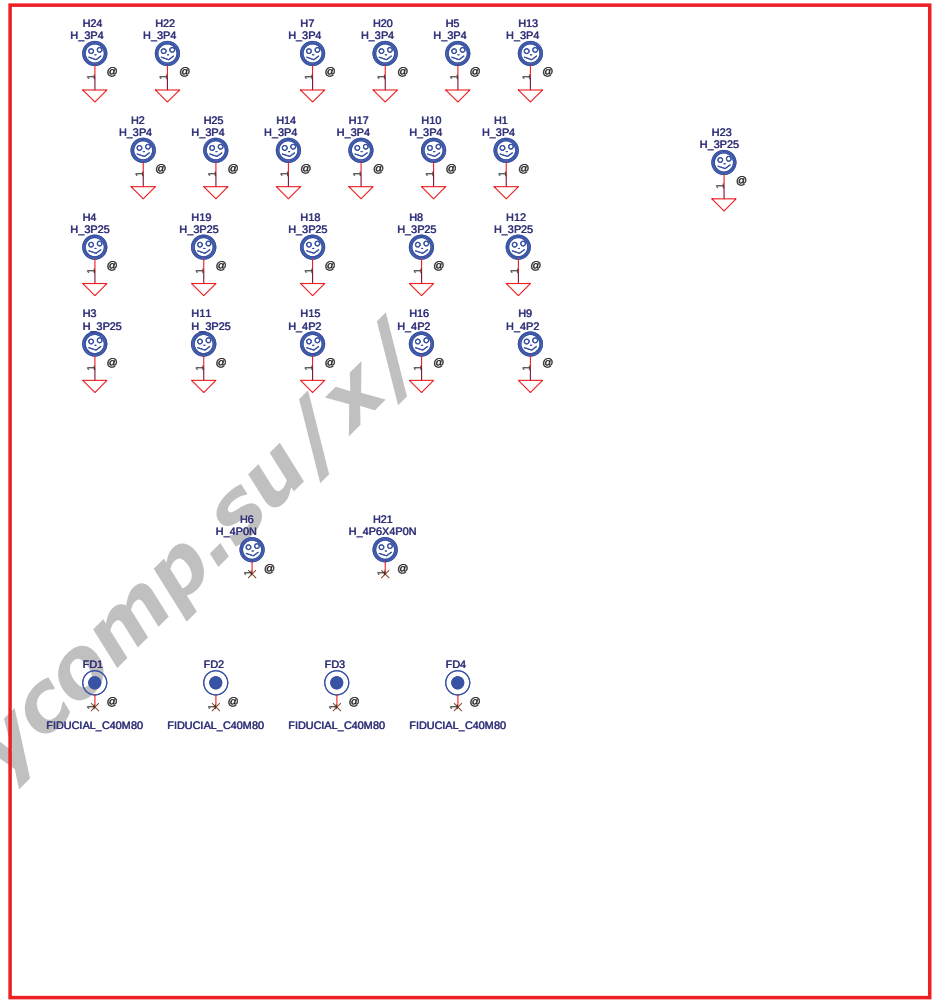
Title: **SUB WOOFER**

Size: Custom | Document Number: **JALB0 LA-4171P** | Rev: 1.0

Date: Friday, April 18, 2008 | Sheet 35 of 50

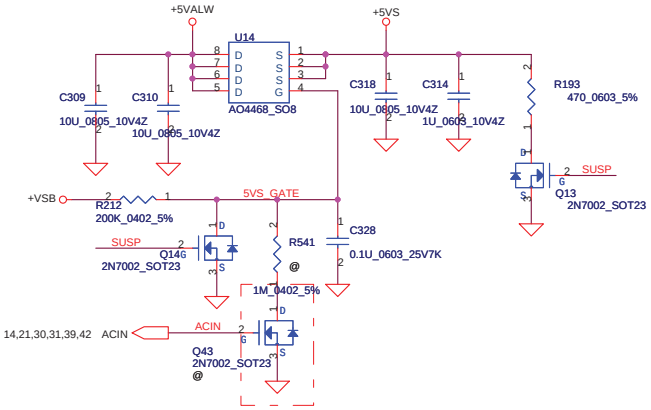
FAN1 Conn



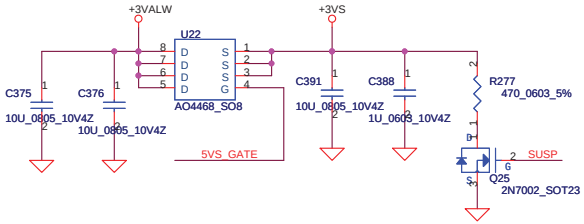


Security Classification	Compal Secret Data		Compal Electronics, Inc.
Issued Date	2008/04/16	Deciphered Date	2009/04/16
Title	FAN & Screw Hole		
Size B	Document Number JALB0 LA-4171P		Rev 1.0
Date: Friday, April 18, 2008	Sheet 36 of 50		

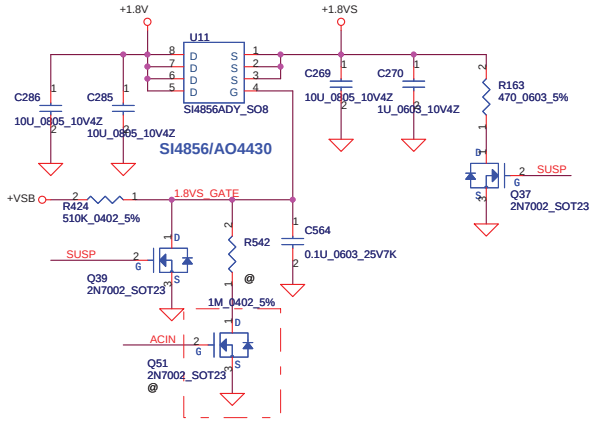
+5VALW TO +5VS

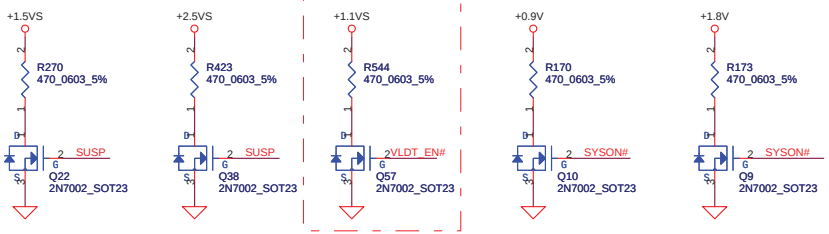


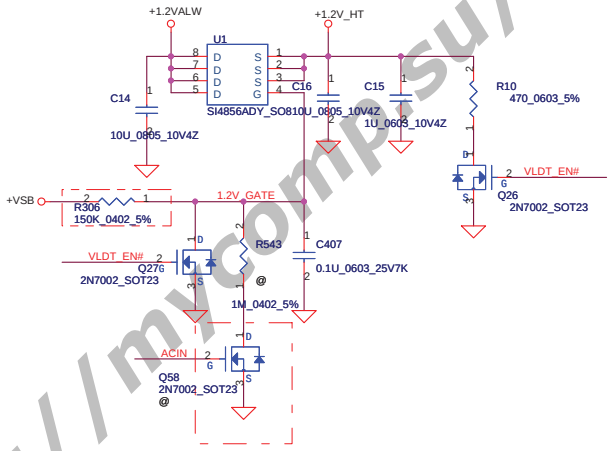
+3VALW TO +3VS

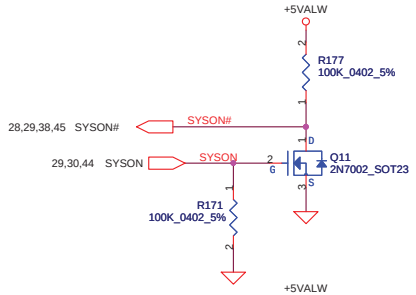


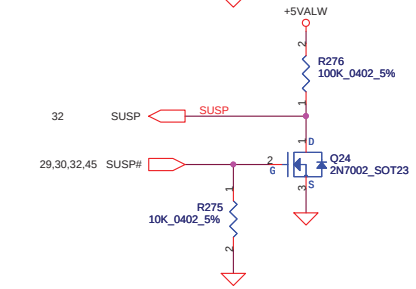
+1.8V to +1.8VS

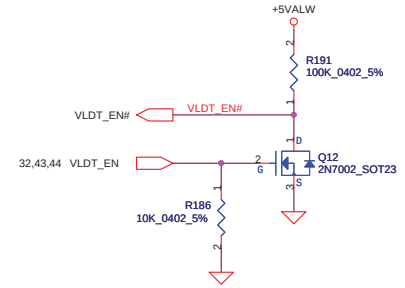












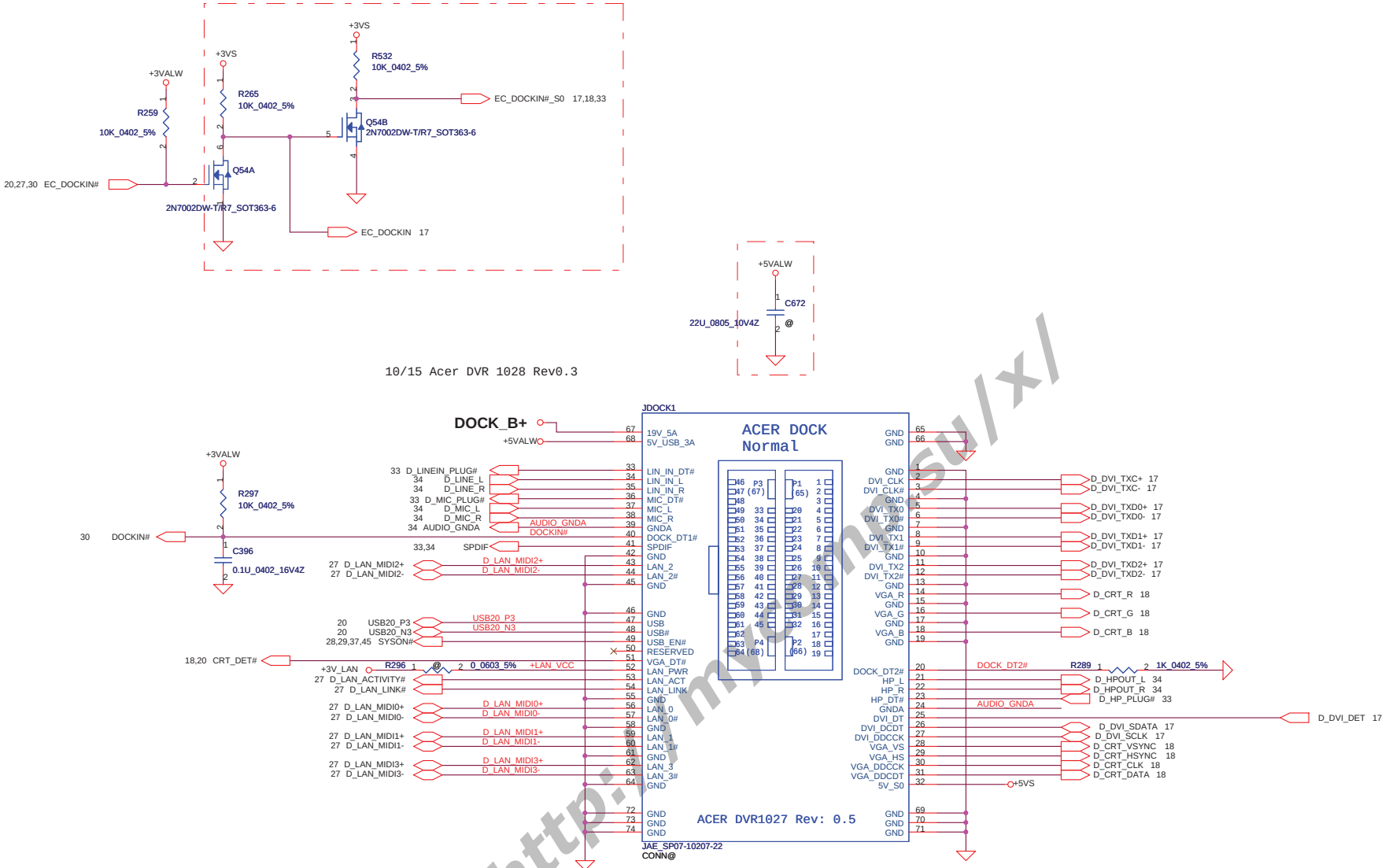
Security Classification	Compal Secret Data		
Issued Date	2008/04/16	Deciphered Date	2009/04/16

Compal Electronics, Inc.

Title: DC Interface

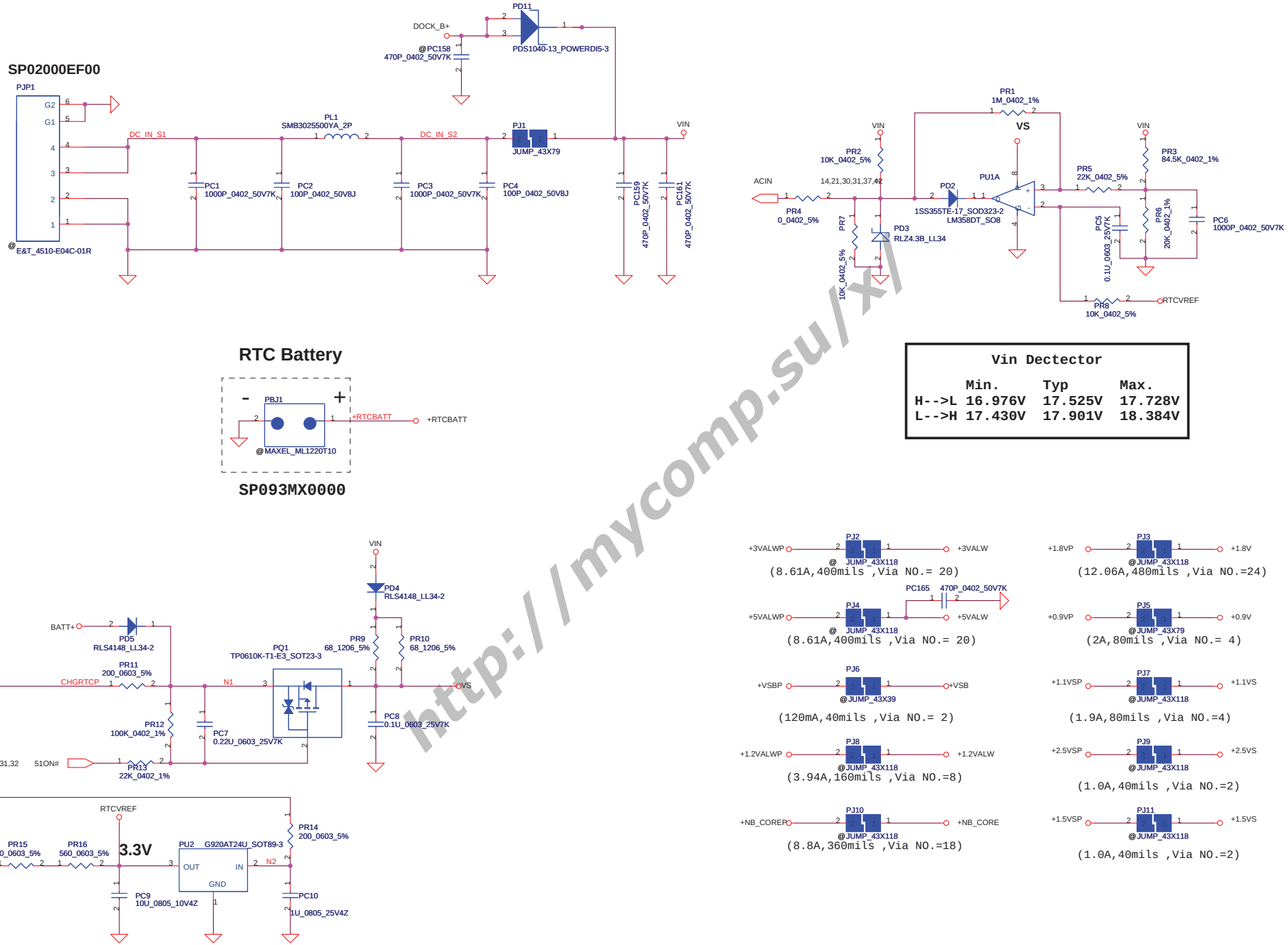
Size: B | Document Number: JALB0 LA-4181P | Rev: 1.0

Date: Friday, April 18, 2008 | Sheet 37 of 50



Security Classification	Compal Secret Data		
Issued Date	2008/04/16	Deciphered Date	2009/04/16

Compal Electronics, Inc.			
Title: CABLE DOCK			
Size: Custom	Document Number: JALB0 LA-4171P		Rev: 1.0
Date: Friday, April 18, 2008	Sheet 38 of 50		



Security Classification	Compal Secret Data		
Issued Date	2008/04/16	Deciphered Date	2009/04/16

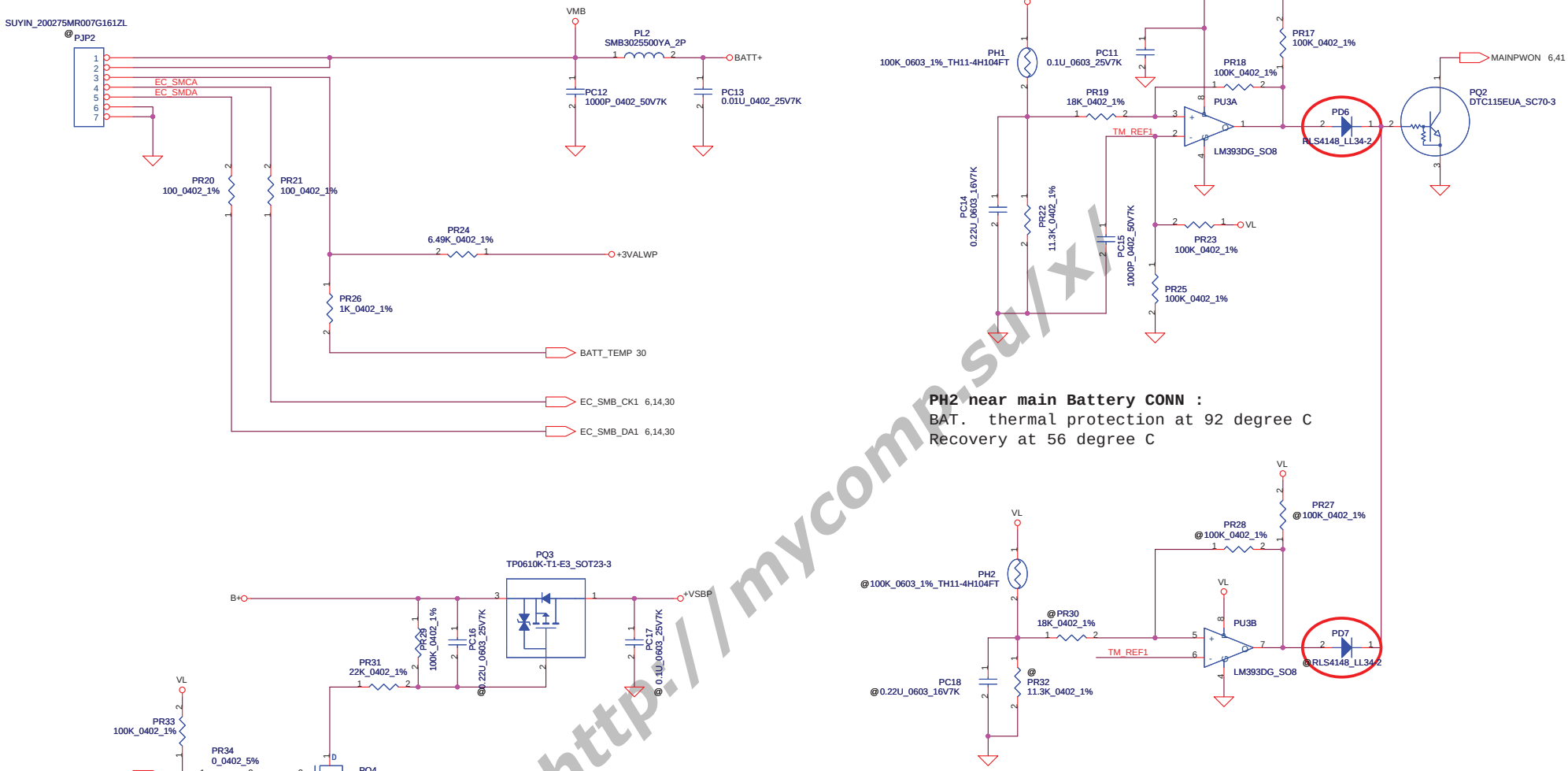
Compal Electronics, Inc.

Title: DCIN & DETECTOR

Size: C | Document Number: JALB0 | Rev: 1.0

Date: Friday, April 18, 2008 | Sheet 39 of 50

PH1 under CPU botten side :
CPU thermal protection at 92 degree C
Recovery at 56 degree C



PH2 near main Battery CONN :
BAT. thermal protection at 92 degree C
Recovery at 56 degree C

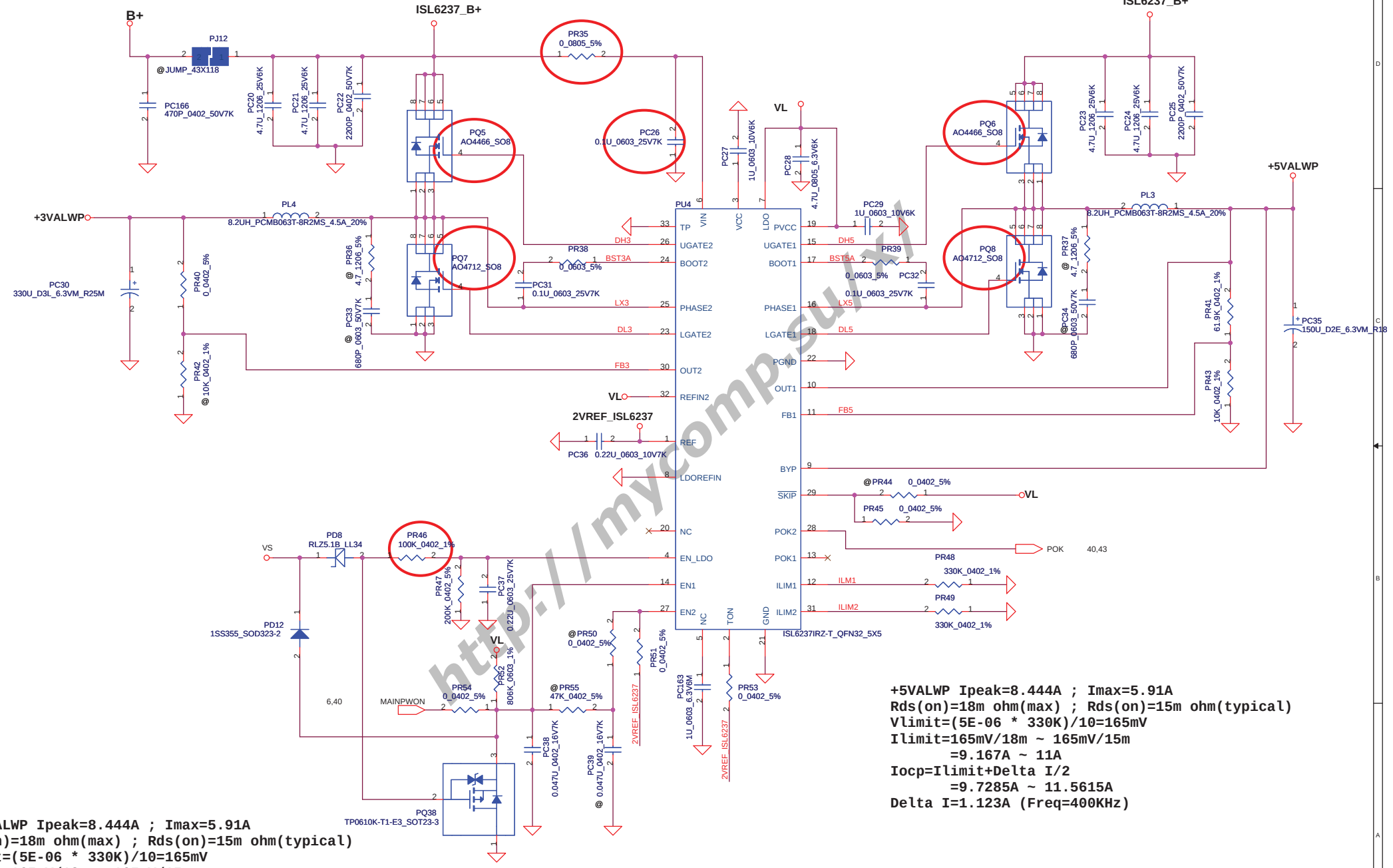
Security Classification	Compal Secret Data		
Issued Date	2008/04/16	Deciphered Date	2009/04/16

Compal Electronics, Inc.

Title: BATTERY CONN / OTP

Size	Document Number	Rev
	JALB0	1.0

Date: Friday, April 18, 2008 | Sheet 40 of 50



+5VALWP Ipeak=8.444A ; Imax=5.91A
Rds(on)=18m ohm(max) ; Rds(on)=15m ohm(typical)
Vlimit=(5E-06 * 330K)/10=165mV
Ilimit=165mV/18m ~ 165mV/15m
=9.167A ~ 11A
Iocp=Ilimit+Delta I/2
=9.7285A ~ 11.5615A
Delta I=1.123A (Freq=400KHz)

+3.3VALWP Ipeak=8.444A ; Imax=5.91A
Rds(on)=18m ohm(max) ; Rds(on)=15m ohm(typical)
Vlimit=(5E-06 * 330K)/10=165mV
Ilimit=165mV/18m ~ 165mV/15m
=9.167A ~ 11A
Iocp=Ilimit+Delta I/2
=9.721A ~ 11.554A
Delta I=1.108A (Freq=300KHz)

Security Classification	Compal Secret Data		
Issued Date	2008/04/16	Deciphered Date	2009/04/16

Compal Electronics, Inc.

Title: +5V/+3V

Size: Custom | Document Number: JALB0 | Rev: 1.0

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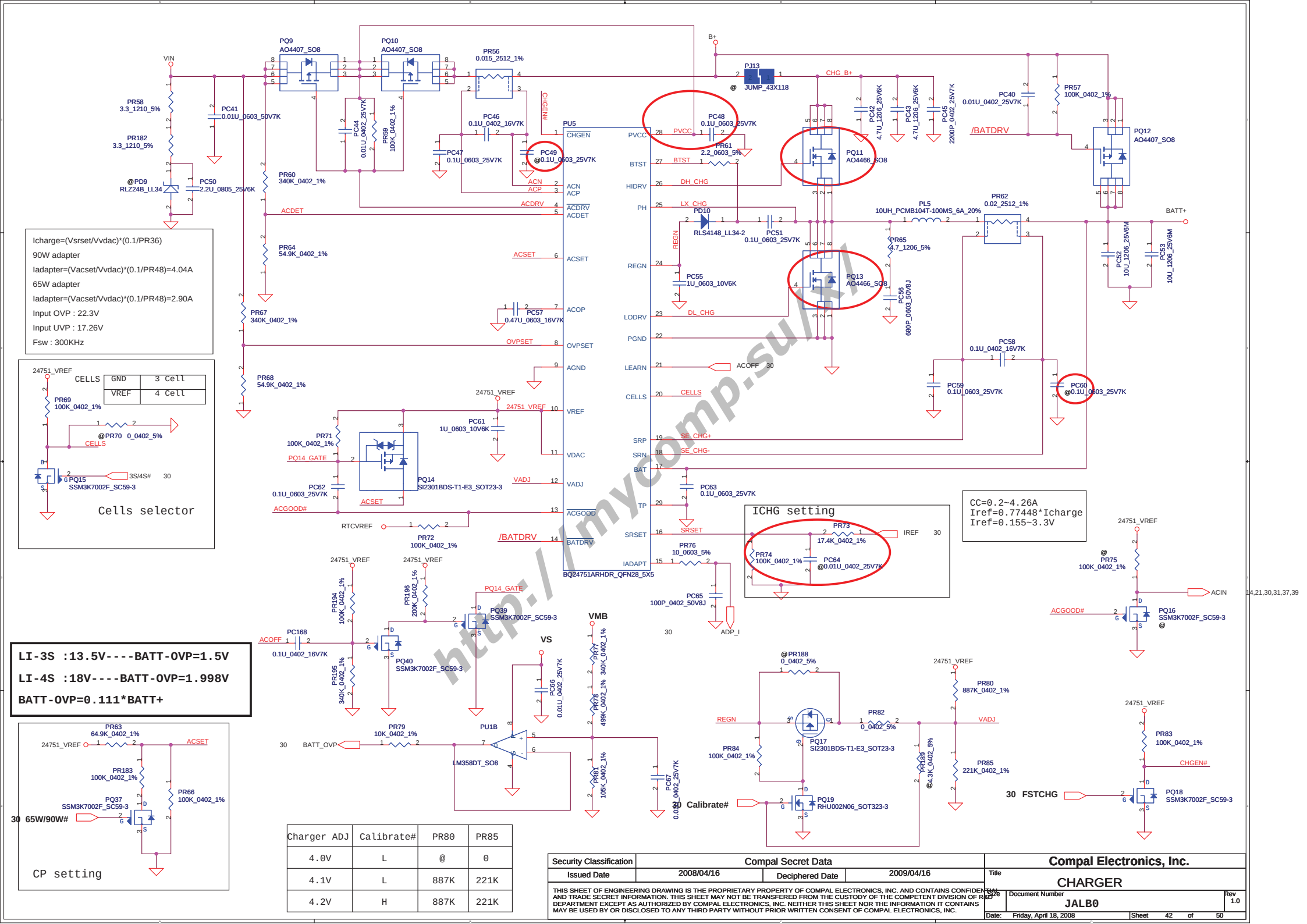
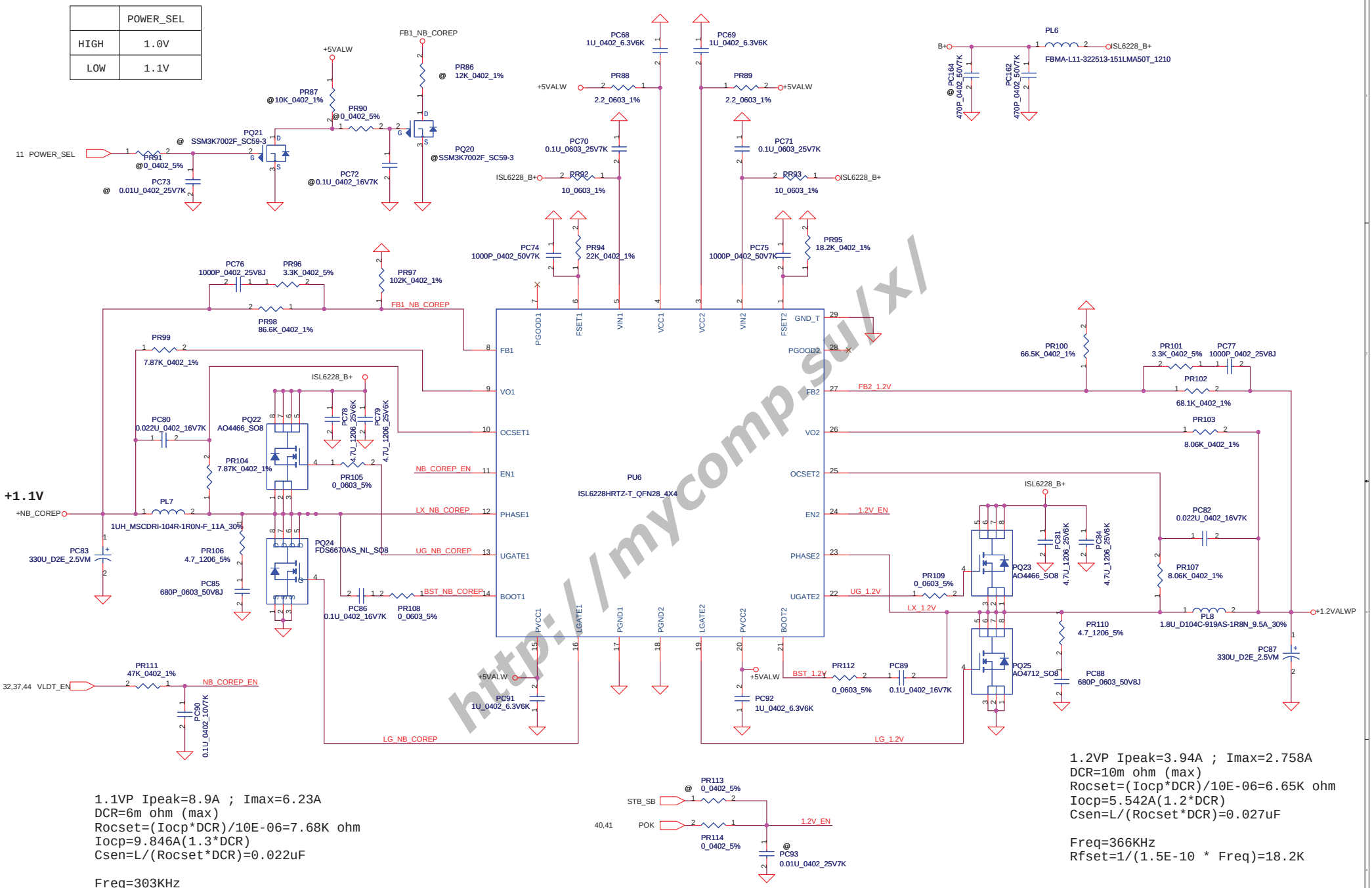

Icharge=(Vsrset/Vvdac)*(0.1/PR36)
90W adapter
Iadapter=(Vacset/Vvdac)*(0.1/PR48)=4.04A
65W adapter
Iadapter=(Vacset/Vvdac)*(0.1/PR48)=2.90A
Input OVP : 22.3V
Input UVP : 17.26V
Fsw : 300KHz
Cells selector
CELLS | GND | 3 Cell
VREF | 4 Cell
LI-3S :13.5V----BATT-OVP=1.5V
LI-4S :18V----BATT-OVP=0.111*BATT+
CP setting
ICHG setting
CC=0.2~4.26A
Iref=0.77448*Icharge
Iref=0.155~3.3V
BQ24751ARHDR_QFN28_5X5
Charger ADJ | Calibrate# | PR80 | PR85
4.0V | L | @ | 0
4.1V | L | 887K | 221K
4.2V | H | 887K | 221K
Security Classification | Compal Secret Data
Issued Date | 2008/04/16 | Deciphered Date | 2009/04/16
Compal Electronics, Inc.
CHARGER
Document Number JALB0
Rev 1.0
Date: Friday, April 18, 2008 Sheet 42 of 50

	POWER_SEL
HIGH	1.0V
LOW	1.1V



1.1VP Ipeak=8.9A ; Imax=6.23A
DCR=6m ohm (max)
Rocset=(Iocp*DCR)/10E-06=7.68K ohm
Iocp=9.846A(1.3*DCR)
Csen=L/(Rocset*DCR)=0.022uF

Freq=303KHz
Rfset=1/(1.5E-10 * Freq)=22K

1.2VP Ipeak=3.94A ; Imax=2.758A
DCR=10m ohm (max)
Rocset=(Iocp*DCR)/10E-06=6.65K ohm
Iocp=5.542A(1.2*DCR)
Csen=L/(Rocset*DCR)=0.027uF

Freq=366KHz
Rfset=1/(1.5E-10 * Freq)=18.2K

Security Classification	Compal Secret Data		
Issued Date	2008/04/16	Deciphered Date	2009/04/16

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Title: NB_COREP / 1.2VSB

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	JALB0	1.0

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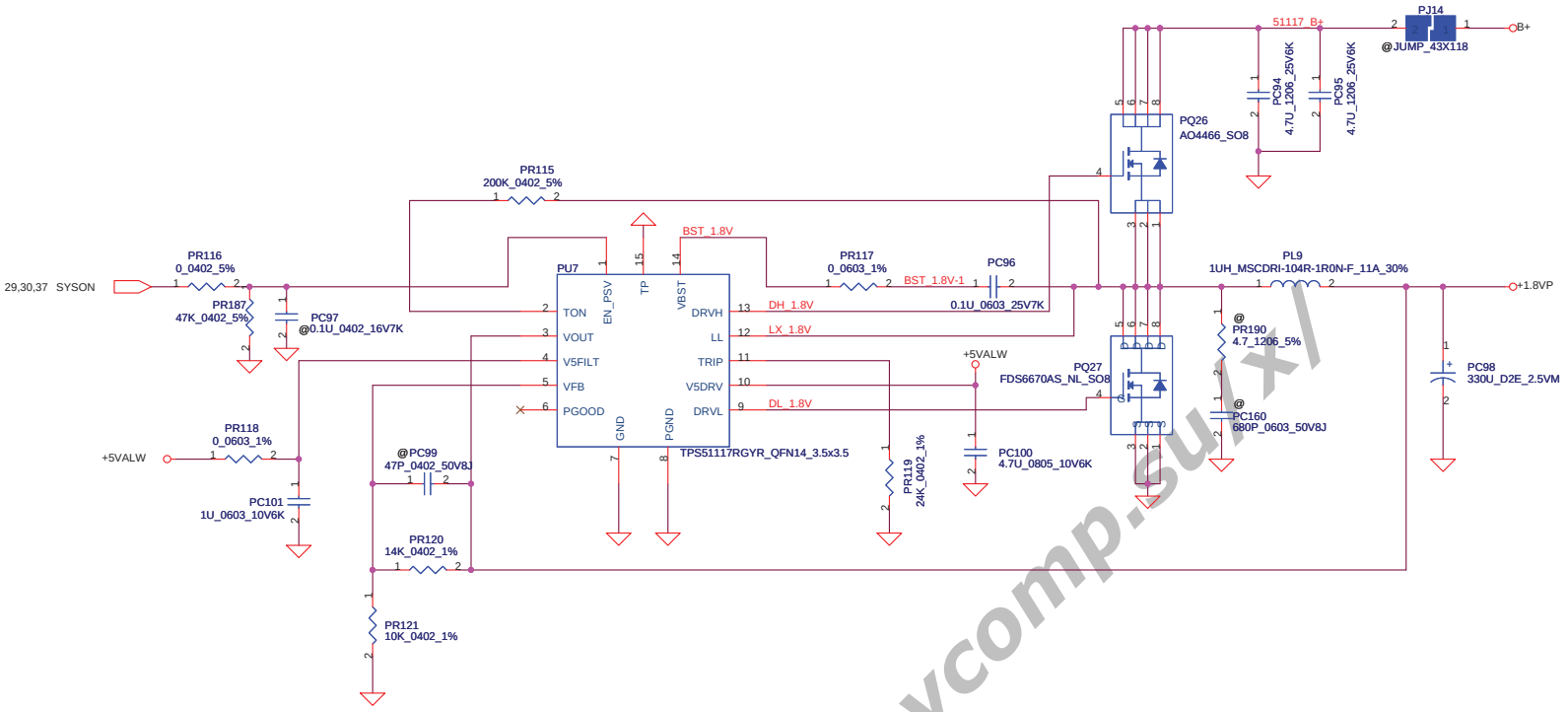
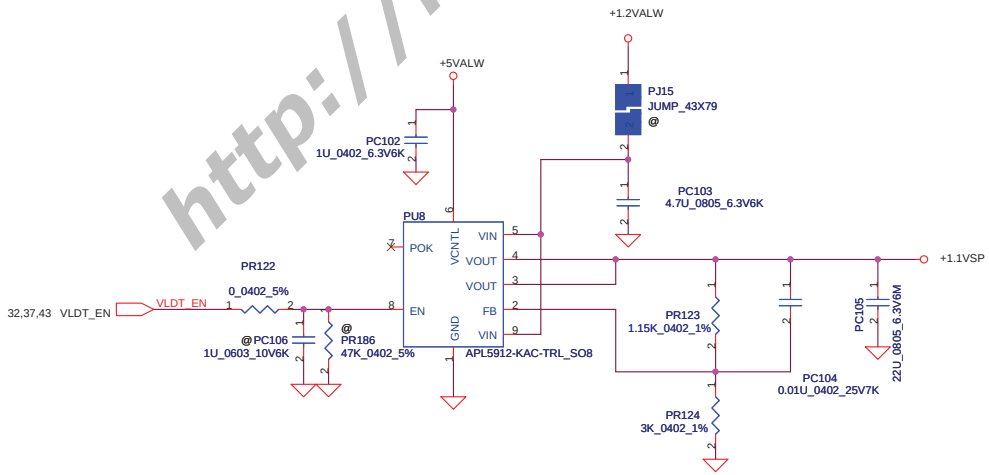


VFB=0.75V
Vo=VFB*(1+PR120/PR121)=1.8V
Ton=19E-12*Ron*(((2/3)*Vo+100mV)/Vin)+50ns=3.1E-07
Freq=305KHz

Cesr=15m ohm
Ipeak=12.6A Imax=8.82A
Delta I=((19-1.8)*(1.8/19))/(L*Freq)=5.332A
Vtrip=Rtrip*10uA=0.24V
Iocp-min=Vtrip/Rdsonmax*1.4+2.666=17.573A
Iocp-max=Vtrip/Rdsontyp*1.2+2.666=26.908A
Iocp=17.573~26.908A



Security Classification	Compal Secret Data		
Issued Date	2008/04/16	Deciphered Date	2009/04/16

Compal Electronics, Inc.

Title: 1.8VSP/+1.1VSP

Size | Document Number | Rev 1.0

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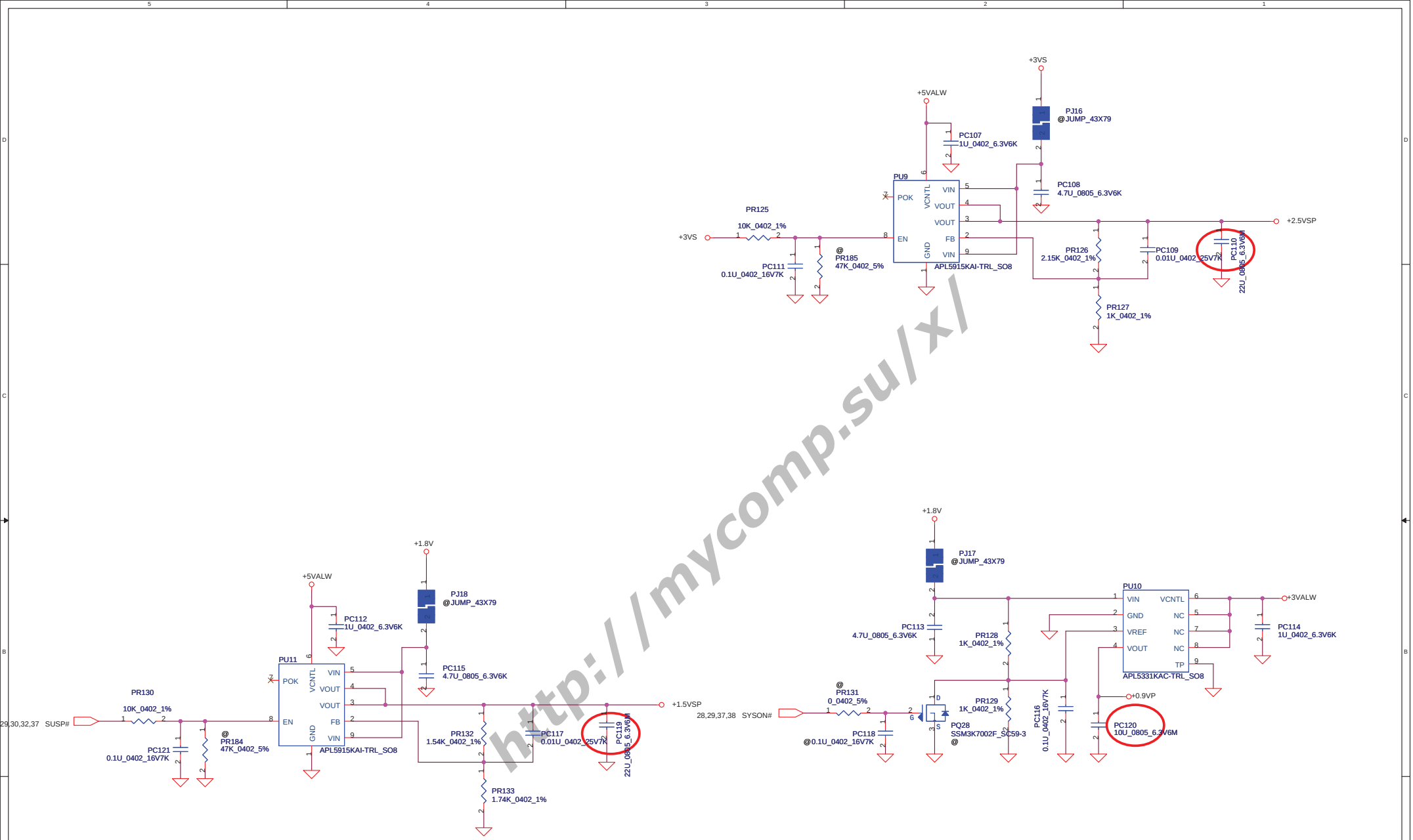

Security Classification	Compal Secret Data		
Issued Date	2008/04/16	Deciphered Date	2009/04/16

Compal Electronics, Inc.

Title: 0.9VP//1.5VSP/2.5VSP

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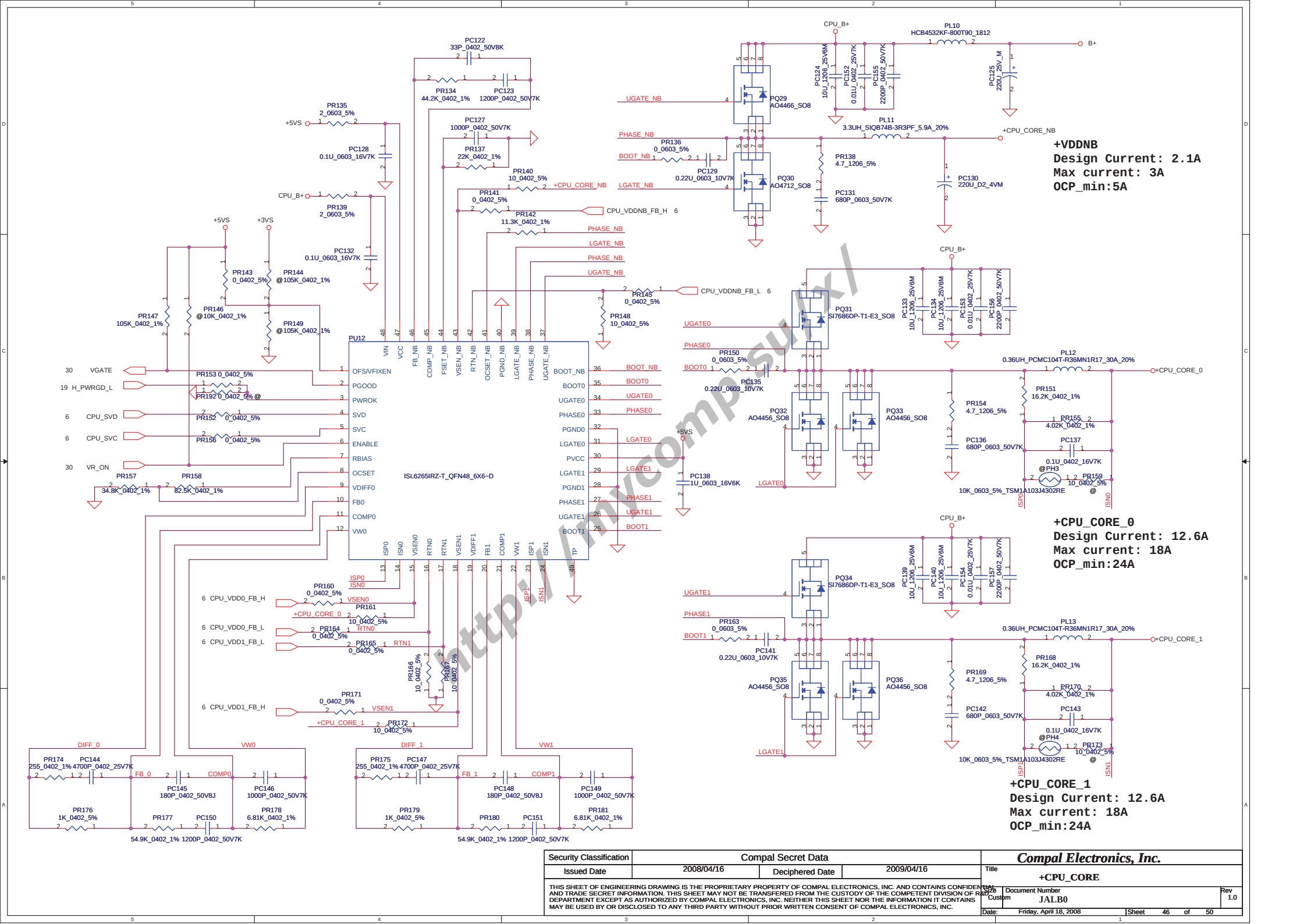

Security Classification	Compal Secret Data		
Issued Date	2008/04/16	Deciphered Date	2009/04/16

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Compal Electronics, Inc.

Title: +CPU_CORE

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NO	DATE	PAGE	MODIFICATION LIST	PURPOSE
7/9		DCIN	Change PL1 to bead coil	link to SM010008E10
7/9		DCIN	Link RTC battery symbol	link to SP093MX0000
7/9		Battery conn	Change PL2 to bead coil	link to SM010008E10
7/9		Battery conn	Change PD3,PD4 to RLS4148	For low cost
7/9		Battery conn	Change PU2 pin8 to VL	Design change
7/9		Charger	Delete PU3 PVCC resistor and change PC26 to 1U	avoid PQ6 false turn-on when AC plug-in
7/9		Charger	Change PQ7,PQ9 to AO4466	For low cost
7/9		Charger	Change PU4 pin8 to +5VALW	Design change
7/9		Charger	Unpop PC28, PC37	avoid interfere by other signal
7/9		3V/5V	Change PR54 and PC51	Add design margine
7/9		3V/5V	Change MOSFET to AO4466+AO4712	For low cost
7/9		1.8V/1.5V	Change MOSFET to AO4466+AO4712	For low cost
7/9		1.8V/1.5V	Change PR75 to 2.2ohm	Design change
7/9		1.05V/1.25V/0.9V	Change MOSFET to AO4466+AO4712	For low cost
7/9		1.05V/1.25V/0.9V	Change PC94 to 330U	Decrease overshoot
7/9		1.05V/1.25V/0.9V	Change PU7 PVCC source to +5VS	Design change
7/9		1.05V/1.25V/0.9V	Change PC105,PC108 size to 0805	For low cost
7/9		CPU CORE	Change input MLCC to 4pcs	Design change
7/9		CPU CORE	Unpop PC111	Reserve for high frequency noise
7/10		Charger	Change PR38, PR39 and unpop PC32	increase resistor to reduce power loss on resistor divider
7/10		Charger	Change PR45, PR47 and unpop PC41	increase resistor to reduce power loss on resistor divider
7/10		Charger	Change PR43 to 100K	increase resistor to reduce power loss
7/10		3V/5V	Change PR65 to 100K_1%	Let BOM clear
7/10		Charger/0.9V	Change PQ4,PQ11,PQ12,PQ13,PQ24 to SB000009080	For low cost
8/1		Charger	Change PR30 to 0.015ohm and PR38 to 80.6K	Change over power protection point

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Title: Power PIR		
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NO	DATE	PAGE	MODIFICATION LIST	PURPOSE
	12/11	p.11	DEL R26	
	12/11	P.15	UN-POP R234,POP R235	
	12/11	P.17	Change R123 to 2.2K	
	12/11	P.18	ADD R525,R526,R527	For non-Dockin sku
	12/11	P.20	Del R128	
	12/11	P.23	Change R103 to 2.2k	
	12/11	P.25	DEL U35,Q43,R473	
	12/11	P.27	ADD RP32,RP33,RP34,RP35,RP36	For non-Dockin sku
	12/11	P.29	Change U17 P/N to SA000029E00	
	12/11	P.31	Change JP14.4 Net to EC_SMB_CK2,JP14.5 Net to EC_SMB_DA2	
	12/11	P.31	Change LED1,LED2 P/N to SC597UDB000	
	12/11	P.35	Change U40.3 to WOOFER_IN+,U40,4 to WOOFER_IN-	
	12/11	P.38	Del R291,R292	
	12/14	P.30	Raise KB926 pin.75	
	12/12	P.14	ADD D28 and pull high R529 to +3VS to AC_IN form JMXM1.157	
	12/12	P.17	Change Q47,Q48,Q49,Q50 P/N to SB501110010	
	12/12	P.18	DEL Q5,ADD Q52,Q53	
	12/12	P.33	Change U31 P/N to SA000026V00	
	12/12	P.30	Change Board ID	
	12/12	P.26	Un-pop R56, POP R61	
	12/13	P.25	DEL U35,R473,Q43	
	12/13	P.7	DEL C762,C763	
	12/14	P.38	update dock footprint and add CRT_Det#	
	12/19	P.18	change CRT_DET to CRT_DET# from CRT to Q36 and output CRT_DET TO U10.J2	
	12/14	P.26	DEL U23,R305,C399,R28	
	12/14	P.6	Change R420, R419, R113 pull-up change to +1.8VS	
	12/14	P.12	Delete U6, R68, R65, Q6, R55, C119, C113, C128, C151,C124	Remove 1.35V LDO circuit
	12/14	P.12	Del L22, POP L21	Change VDDHTTX from 1.35V to 1.2V
	12/14	P.14	Change C183 to 0402 package	
	12/14	P.16	Change C12 to 0402 package	
	12/14	P.17	Change R90,R91 from 1.5K to 2K	
	12/14	P.22	Delete R399, add R391	VDD should connect to S0 power on A12
	12/14	P.34	Change R480, R487 from 0Ohm to 75Ohm	
	12/14	P.37	Change R306 to 10K	
	12/14	P.32	Change D16.1 from +3VS to SUSP#	1.2V_HT should faster than NB_CORE
	12/19	P.25	Connect U33.16 to U10.AD18 (CR_WAKE#) through D29; U33.13 to U10.F2 (CR_PE#) through a MOS(Q55)	VGA_ON should drop before +3VS
	12/17	P.28	DEL TV_THERM#,ADD Port80 Signal to JMINI2.49,JMINI2.51	
	12/17	P.19	Delete R179,R185, add U12, U13	

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NO	DATE	PAGE	MODIFICATION LIST	PURPOSE
	12/17	P.26	Del BCM5787 Co-lay part	
	12/17	P.38	ADD EC_DOCKIN#_S0	
	12/18	P.25	ADD R533	
	12/19	P.11	ADD Q54,R534 Level shift, and CPU_LDT_REQ#,ALLOW_LDTSTOP Pull high 300 to 1.8vs	
	12/19	P.20	Change New Card CP_PE# to SB GPM5#	
			Change CRT_DET to SB GPM7#	
			Change EC_LID_OUT# to SB GPM4#	
			Del USB_OC#4	
	12/19	P.6	ADD R129,R538,R539	
	12/19	P.21	change R104 from 10K to 100K	
	12/19	P.34	Change R488,R483 to 75 ohm	
	12/19	P.37	Change R306 from 10K to 150K	
	12/19	P.6	POP R93	
	12/19	P.18	change D18 from RB411 to RB491	
	12/19	P.19	Change Y2 location to X2 and p/n change to SJ132P7K220	
	12/19	P.30	EC_SMB_CK1,EC_SMB_DA1 Pull high to +3VALW,EC_SMB_CK2,EC_SMB_CK2 pull high to +3VS	
	12/20	P.37	Reserve R541,R542,R543	
	12/20	P.33	Change R294,R288 P/N to SM010016720	
	12/20	P.31	ADD C655,C656,C657,C658,C659,C660,C661,C662 for EMI	
	12/20	P.37	ADD Q57,R544	
	12/20	P.34	JMIC1.7,JMIC1.8,JLINE1.7,JLINE1.8 connect to AGND,	
	12/21	P.21	Change SATA HDD Port to U10 SATA port 1	
	12/24	P.21/P22.	Change D7,D9 P/N to SC1B751V010	
	12/24	P.34	Change L73,L74,L67,L68,L71,L72 P/N to SM010015410	
	12/24	P.21	ADD SPI ROM Schematic for SB700	
	12/24	P.34	JHP1.6,JHP1.10 connect to AGND	
	12/24	P.29	Add U17 .21 to gnd	
	12/24	P.26	Change U5.18,U5.17,U5.5,U5.33 connect to +1.2_VDDCIO	
	12/26	P.34	Change R490 to 42.2K, R478,R479 to 1K,C621,C622 to 0.22u	
	12/26	P.35	Change R516 to 6.8K	
	1/22	P.15	Reversal MiniCard1 & MiniCard2 PCIE CLK Signal	
	1/22	P.37	Change R275 from 100K to 10K	
	1/22	P.37	Change Q57.2 to VLDT_EN#	
	1/31	P.6	POP CPU internal themal sensor schematic	
	1/31	P.11	change R64 to 133 ohm	
	1/31	P.14	Add AND GATE	
	1/31	P.15	Add C669	
	1/31	P.17	Change EC_DOCKIN#_S0 to Q50.2/Q49.2	
	1/31	P.18	Change EC_DOCKIN#_S0 to U7.1	
	1/31	P.20	Change CRT_DET to U10.H7,add EC_DOCKIN# to U10.B9	

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NO	DATE	PAGE	MODIFICATION LIST	PURPOSE
	1/31	P.21	Reserve AND gate form ACIN to U10.A4	
	1/31	P.28	Reserve MINI1_LED# Pull high 100K to +3VS	
	1/31	P.30	ADD R551,R552 (VR_ON pull down 100k,BT_ON# Pull 100k)	
	1/31	P.30	Del JP12	
	1/31	P.33	Change R257 from 200k to 330k	
	1/31	P.33	ADD EC_DOCKIN#_S0 to R530.1	
	1/31	P.34	Change R459,R446,R475,R470 to 75ohm	
	1/31	P.34	Add R553,R554,R555,R556	
	1/31	P.38	Add C672	
	2/4	P.25	For EMI request,add C676	
	2/4	P.31	For EMI request,add C673,C674,C675	
	2/4	P.34	For EMI request,add D31	
	2/12	P.6	Change R361,R365 to 2.2k	
	2/12	P.30/31	ADD ESB_CLK/ESB/DATA (add R557,R558,R559,R560,R561,R562)	
	2/13	P.28	ADD R563	
	2/14	P.6/20	UPDATE cpu internal themal sensor schematic (add R564,R565,R566,R567,R568,R569,ADD CPU_SIC_SB,CPU_SID_SB)	
	3/12		R493=>61.9K (SD034619280) R516=>1K (SD028100180) R517=>4.7K (SD028470180) R518=>1.8K (SD028180180) C647=> 0.068u (SE026683K80)	
	3/12	P.33	For EMI request,Change R440 to SD028100A80	
	3/12	P.12	Change C109,C150,C130,C88,C92,C35,C34,C36,C38 to SE000000I10 (22U)	
	3/12	P.7	Change C77,C78,C79,C80 to SGA00002380	
	3/12	P.37	Change R186 to10K	
	3/17	P.11	ADD R570,R571, Un-pop Q28,Q56,R324,R534	
	3/26	P.6	Un-pop R351,C436,R360,R566,R568,Q31,Q30	
	3/26	P.19	Change C192,C22 to 22p	
	3/26	P.34	Change R487,R480,R488,R483 to 56.2	
	4/16	P.8	Change C257 from 0.1U to 1UF	
	4/16	P.19	Change C192, C212 to 12P for RTC Timer issue	
	4/16	P.28	Add L, C on SYSON# signal close to USB/B connector and TV/B connector	
	4/16	P.30	Change the board ID back to R0.3 for BIOS identify issue	
	4/16	P.31	Add 100pF capacitor on +3VS close to MEDIA/B	
	4/16	P.32	Change C373 to 0.22U_0603_X7R for VGA power sequence	
	4/16	P.32	Remove power on/off button SW3 for MP BOM	
	4/16	P.37	Reserve voltage divider circuit on Power MOS	

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