

Wistron Confidential

MV-3

2008/08/20

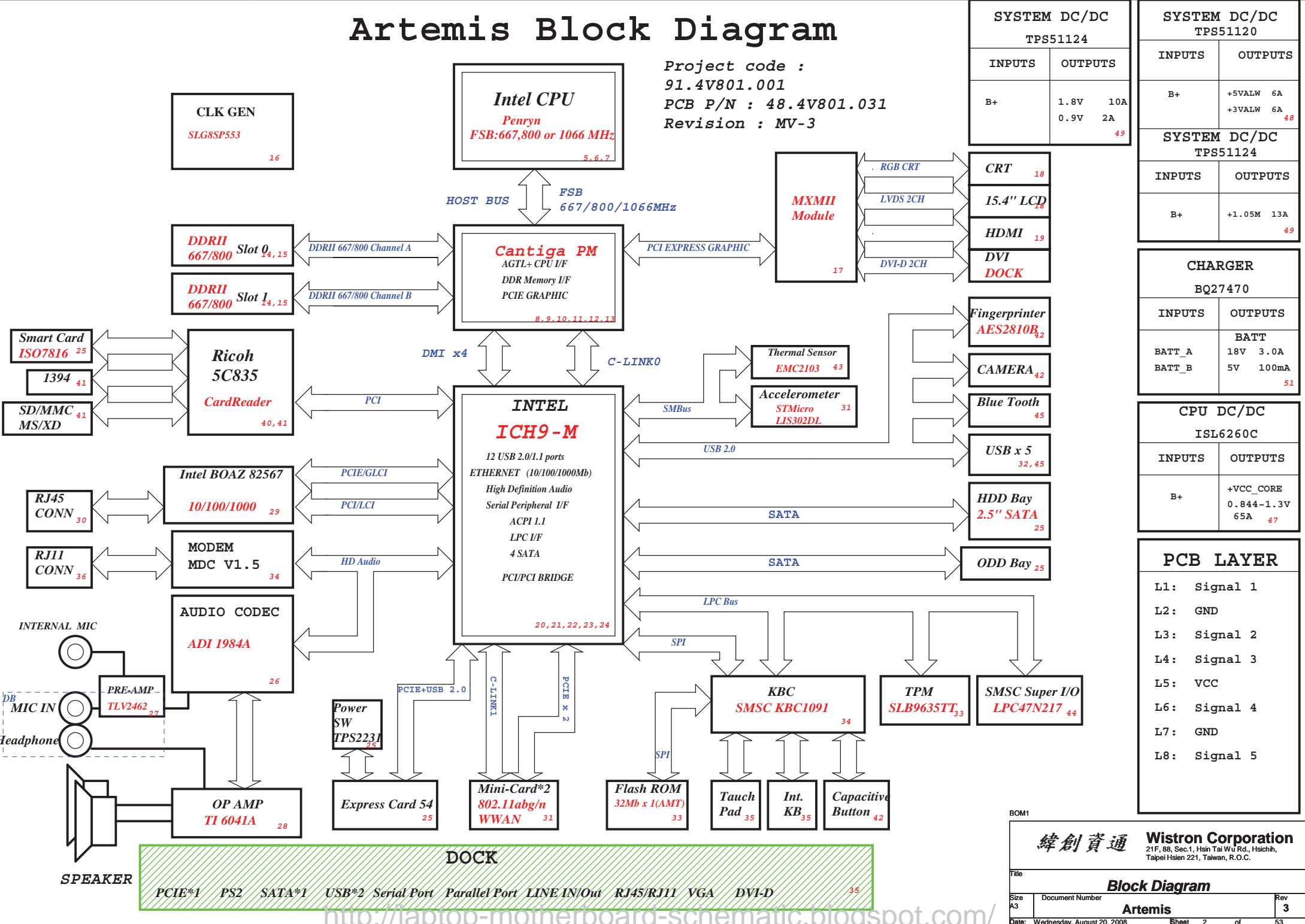
REV :MV-03

BOM1

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Title			
VOX			
Size	Document Number	Rev	
A3	Artemis	3	
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Artemis Block Diagram

Project code :
 91.4V801.001
 PCB P/N : 48.4V801.031
 Revision : MV-3



SYSTEM DC/DC TPS51124	
INPUTS	OUTPUTS
B+	1.8V 10A 0.9V 2A

SYSTEM DC/DC TPS51120	
INPUTS	OUTPUTS
B+	+5VALW 6A +3VALW 6A

SYSTEM DC/DC TPS51124	
INPUTS	OUTPUTS
B+	+1.05M 13A

CHARGER BQ27470	
INPUTS	OUTPUTS
BATT_A BATT_B	BATT 18V 3.0A 5V 100mA

CPU DC/DC ISL6260C	
INPUTS	OUTPUTS
B+	+VCC_CORE 0.844~1.3V 65A

PCB LAYER	
L1:	Signal 1
L2:	GND
L3:	Signal 2
L4:	Signal 3
L5:	VCC
L6:	Signal 4
L7:	GND
L8:	Signal 5

CLK GEN
 SLG8SP553
 16

Intel CPU
 Penryn
 FSB:667,800 or 1066 MHz
 5, 6, 7

DDRII Slot 0
 667/800
 14, 15

DDRII Slot 1
 667/800
 14, 15

Cantiga PM
 AGTL+ CPU I/F
 DDR Memory I/F
 PCIE GRAPHIC
 8, 9, 10, 11, 12, 13

MXMII Module
 17

RGB CRT
 LVDS 2CH
 DVI-D 2CH

CRT 18
15.4" LCD 18
HDMI 19
DVI DOCK

Smart Card ISO7816 25
I394 41
SD/MMC MS/XD 41

Ricoh 5C835 CardReader
 40, 41

INTEL ICH9-M
 12 USB 2.0/1.1 ports
 ETHERNET (10/100/1000Mb)
 High Definition Audio
 Serial Peripheral I/F
 ACPI 1.1
 LPC I/F
 4 SATA
 PCI/PCI BRIDGE
 20, 21, 22, 23, 24

Thermal Sensor EMC2103 43
Accelerometer STMicro LIS302DL 31

Fingerprinter AES2810B 42
CAMERA 42

Blue Tooth 45
USB x 5 32, 45

HDD Bay 2.5" SATA 25

ODD Bay 25

RJ45 CONN 30
RJ11 CONN 36

Intel BOAZ 82567 10/100/1000 29
MODEM MDC V1.5 34

INTERNAL MIC
DB MIC IN
Headphone

PRE-AMP TLV2462 27

AUDIO CODEC ADI 1984A 26

OP AMP TI 6041A 28

Power SW TPS2231 25
Express Card 54 25

Mini-Card*2 802.11ab/g/n WWAN 31

Flash ROM 32Mb x 1(AMT) 33

KBC SMSC KBC1091 34
Tauch Pad 35
Int. KB 35
Capacitive Button 42

TPM SLB9635TT 33

SMSC Super I/O LPC47N217 44

DOCK
 PCIE*1 PS2 SATA*1 USB*2 Serial Port Parallel Port LINE IN/Out RJ45/RJ11 VGA DVI-D 35

BOM1

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5

4

3

2

1

D

D

C

C

B

B

A

A

VOX

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Title		
Change Notes List		
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Voltage Rails ○ MEANS ON × MEANS OFF

power plane State	+B +3VL LD05	+5VALW +3VALW	+1.5V +5V +0.75V	+5VS +3VS +1.5VS +CPU CORE +VCCP	+3VM +1.05VM	CLOCK
S0	○	○	○	○	○	○
S3/M1	○	○	○	×	○	○
S3	○	○	○	×	○	○
S5 S4/AC	○	○	×	×	○	○
S5 S4/Battery only	○	×	×	×	×	×
S5 S4/AC & Battery don't exist	×	×	×	×	×	×

PCI Devices

EETERNAL	IDSEL#	REQ/GNT#	PIRQ
Cardreader & 1394	AD22	2	G,E

DMA Channel	Device
DMA0	Modem/LAN
DMA1	ECP
DMA2	Floppy Disk
DMA3	Audio
DMA4	(Cascade)
DMA5	Unused
DMA6	Unused
DMA7	Unused

USB PORT#	Destination
0	USB1
1	USB4
2	EXPRESS SLOT
3	USB5
4	USB2
5	USB3
6	Bluetooth
7	WWAN
8	Fingerprint
9	Dock 1
10	Camera
11	Dock 2

Symbols	Description
DY/DUMMY	No install
1KR2J	Resistor 1K ohm ,Size 0402 ,5%
1KR3F	Resistor 1K ohm ,Size 0603 ,1%
GP	ROHS parts
NC	Pin no connect to anything

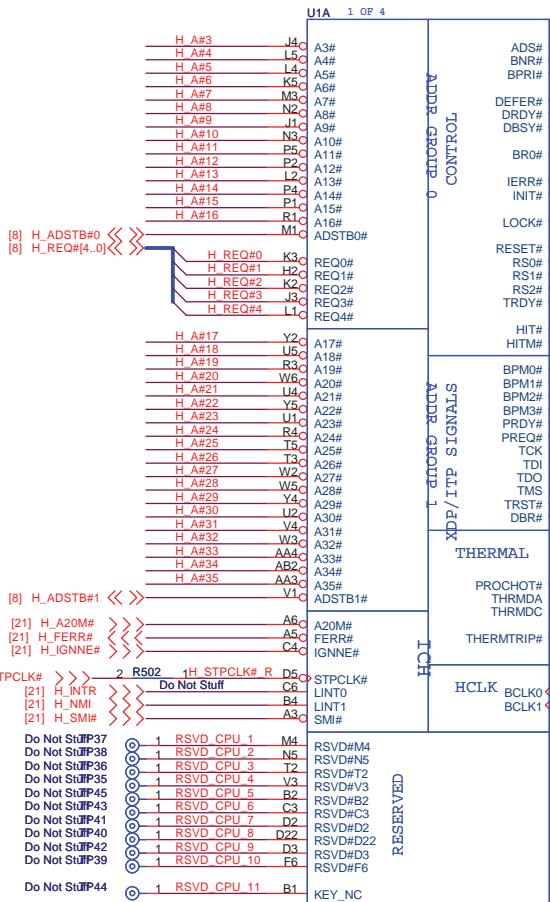
IRQ	Device
0	System Timer
1	Keyboard
2	N/A
3	Serial port (COM2) ,LAN/Modem
4	Serial port (COM1)
5	Audio/VGA
6	Floppy
7	Parallel port
8	System CMOS/Real-time clock
9	Microsoft ACPI
10	N/A,Modem,LAN
11	Mass storage control/PCI simple communication control
12	synactic PS2 port GlidePAD
13	Numeric Data Process
14	Primary IDE interface ,HDD
15	Secondary IDE interface ,CD-ROM
16	Mobile Intel Crestline Express Chipset Family Microsoft UAA Bus Drive for High Definition Audio Intel 82801H (ICH8 Family) PCI Express Root Port -27D0
17	Intel 82801I (ICH9 Family) PCI Express Root Port -27D2 Intel 82801I (ICH9 Family) USB Universal Host Control
18	Intel 82801I (ICH9 Family) USB Universal Host Control Richo R5C835 Integrates FlashMedia Control Richo R5C835 Gemcore based SmartCard Control
19	Intel 82801I (ICH9 Family) PCI Express Root Port -27D6 Intel 82801I (ICH9 Family) USB Universal Host Control
20	Intel 82801I (ICH9 Family) USB Universal Host Control Intel 82801I (ICH9 Family) USB2 Enhanced Host Control
21	Intel 82801I (ICH9 Family) USB Universal Host Control
22	SDA Standard Compliant SD Host Control Accelerometer LIS302DL
23	HP Mobile Data Protection Sensor

VOX

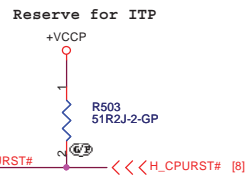
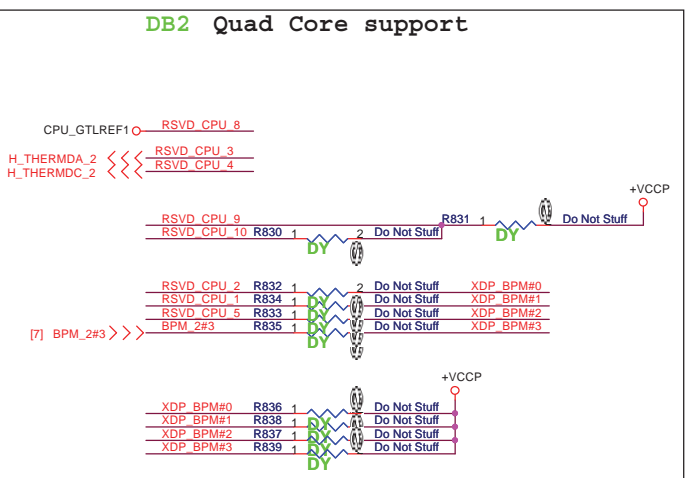
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Artemis List	
Title	
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CPU (1 of 3)

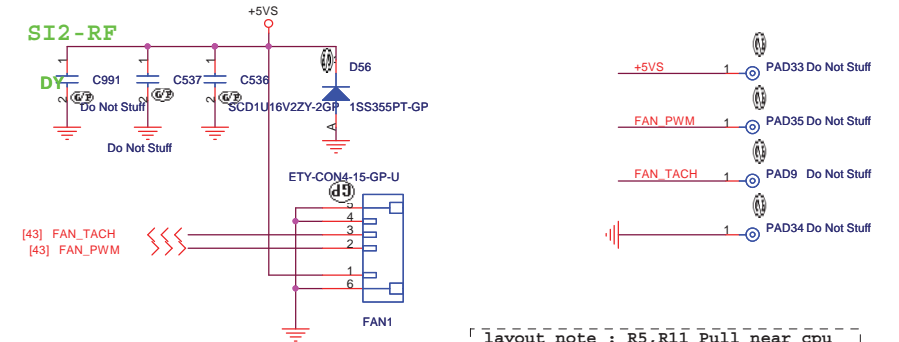
5 H_A#[35..3] <<< H_A#[35..3]



BGA479-SKT-8-GP-U3
62.10053.401

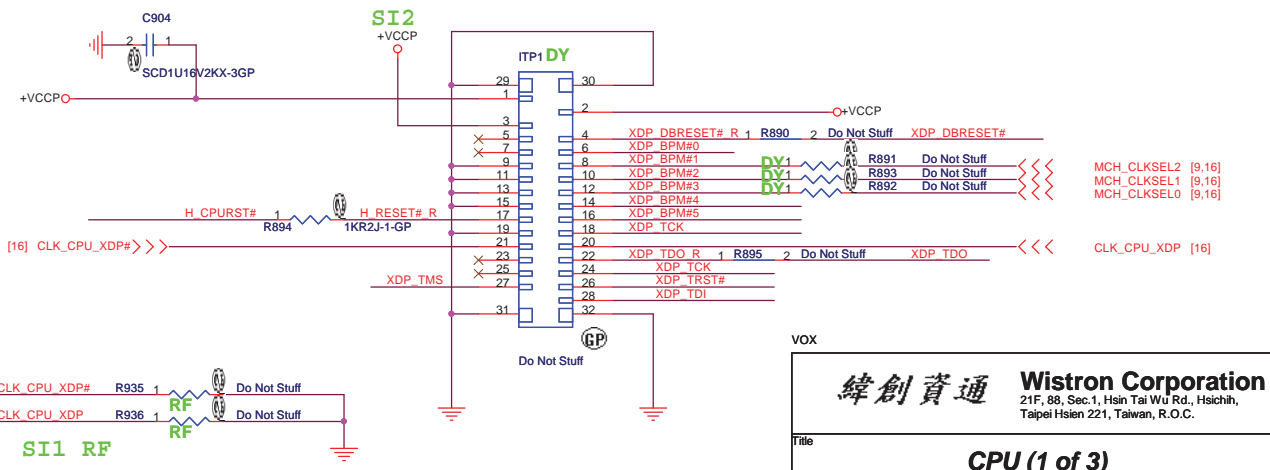
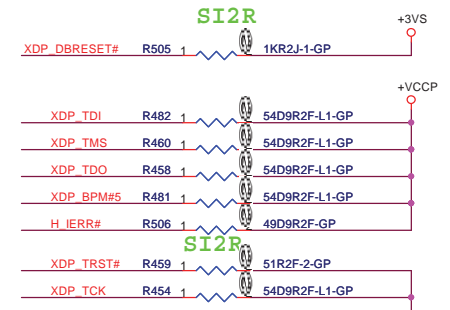
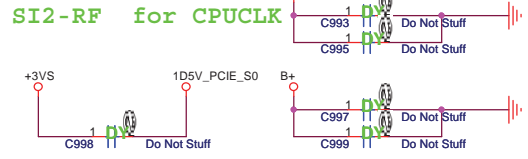


4 WIRE PWM Fan Control circuit



H_THERMDA, H_THERMDC routing together,
Trace width / Spacing = 10 / 10 mil

PM_THERMTRIP# should connect to IC19 and IC8 without T-ing (No stub)



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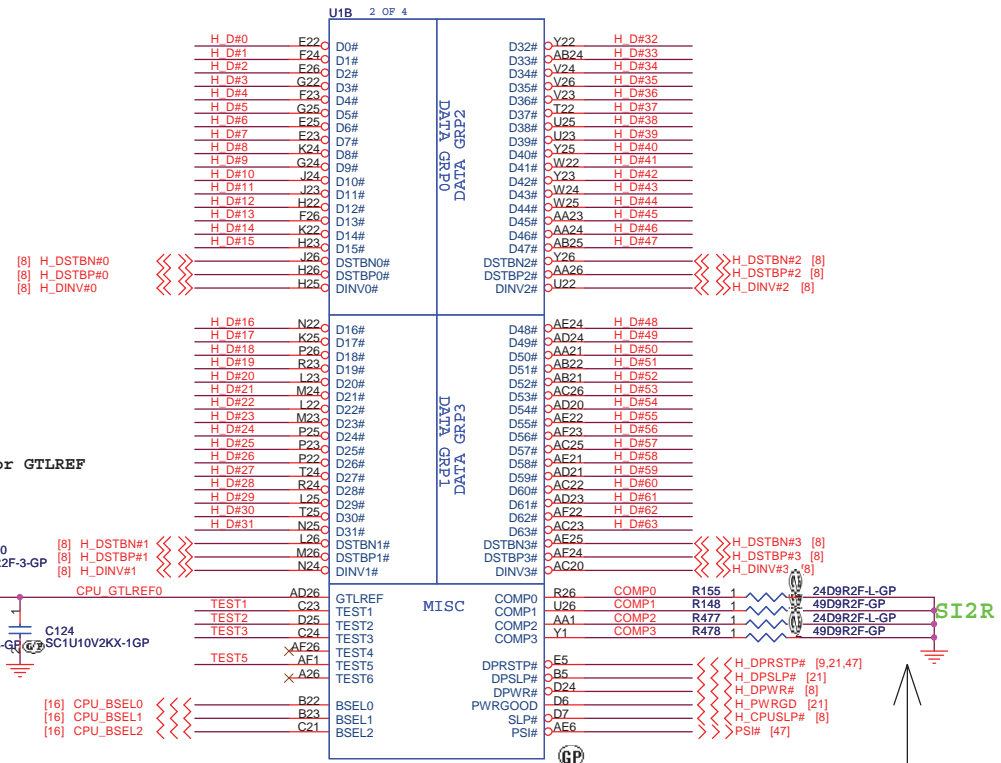
File CPU (1 of 3)

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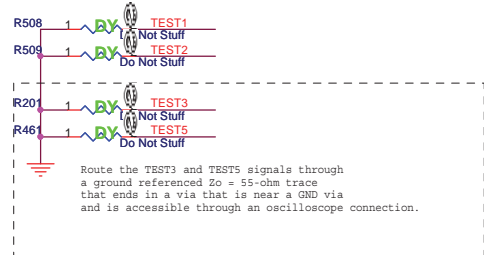
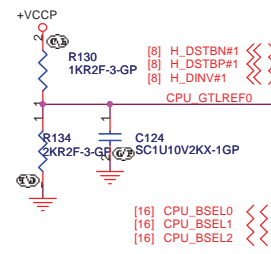
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CPU (2 of 3)

H_DINV#3..0 << >> H_DINV#3..0 [8]
 H_DSTBN#3..0 << >> H_DSTBN#3..0 [8]
 H_DSTBP#3..0 << >> H_DSTBP#3..0 [8]
 H_D#63..0 << >> H_D#63..0 [8]



Layout notes
 Z= 55 Ohm 0.5" MAX for GTLREF



Layout Note:
 Comp0, 2 connect with Zo=27.4 ohm, make trace length shorter than 0.5".
 Comp1, 3 connect with Zo=55 ohm, make trace length shorter than 0.5".

BGA479-SKT-8-GP-U3

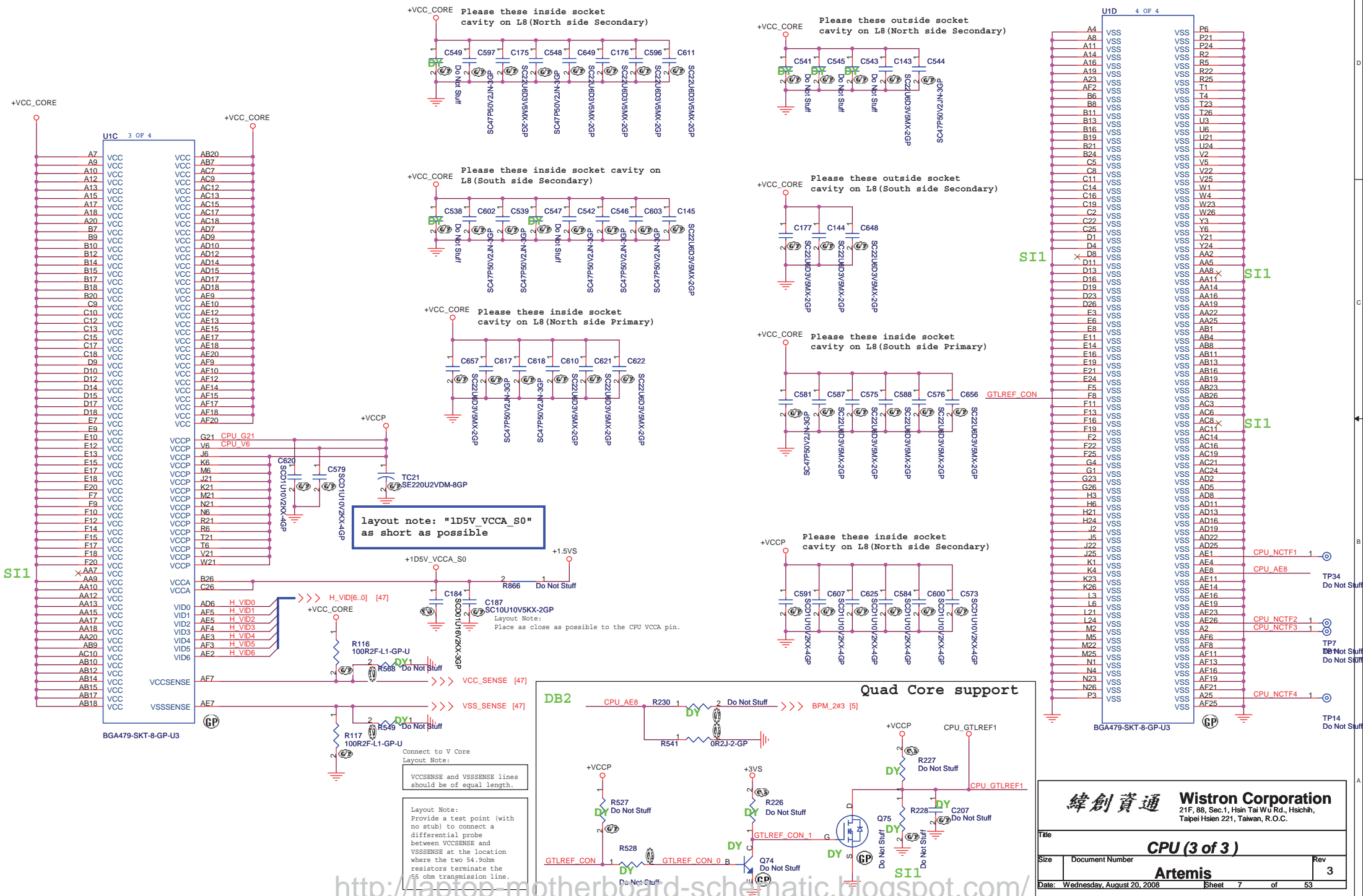
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layout note: "1D5V_VCCA_S0" as short as possible

Connect to V Core
Layout Note:

VCCSENSE and VSSSENSE lines should be of equal length.
Layout Note:
Provide a test point (with no stub) to connect a differential probe between VCCSENSE and VSSSENSE at the location where the two 54.9ohm resistors terminate the 55 ohm transmission line.

UID 4 OF 4	
A4	VSS
A8	VSS
A11	VSS
A14	VSS
A16	VSS
A19	VSS
A23	VSS
AF2	VSS
B6	VSS
B8	VSS
B11	VSS
B13	VSS
B16	VSS
B19	VSS
B21	VSS
B24	VSS
C5	VSS
C8	VSS
C11	VSS
C14	VSS
C16	VSS
C19	VSS
C2	VSS
C22	VSS
C25	VSS
D1	VSS
D4	VSS
D8	VSS
D11	VSS
D13	VSS
D16	VSS
D19	VSS
D23	VSS
D26	VSS
E3	VSS
E6	VSS
E8	VSS
F11	VSS
F14	VSS
F16	VSS
F19	VSS
F2	VSS
F22	VSS
F25	VSS
G4	VSS
G1	VSS
G23	VSS
G26	VSS
H3	VSS
H6	VSS
H21	VSS
H24	VSS
J2	VSS
J22	VSS
J25	VSS
K1	VSS
K23	VSS
K26	VSS
L3	VSS
L6	VSS
L21	VSS
L24	VSS
M2	VSS
M5	VSS
M22	VSS
M25	VSS
N1	VSS
N4	VSS
N23	VSS
N26	VSS
P3	VSS
P6	VSS
P21	VSS
P24	VSS
R2	VSS
R5	VSS
R22	VSS
R25	VSS
T1	VSS
T4	VSS
T23	VSS
T26	VSS
U3	VSS
U6	VSS
U21	VSS
U24	VSS
V2	VSS
V5	VSS
V22	VSS
V25	VSS
W1	VSS
W4	VSS
W23	VSS
W26	VSS
Y3	VSS
Y6	VSS
Y21	VSS
Y24	VSS
AA2	VSS
AA5	VSS
AA8	VSS
AA11	VSS
AA16	VSS
AA19	VSS
AA22	VSS
AA25	VSS
AB1	VSS
AB4	VSS
AB6	VSS
AB11	VSS
AB13	VSS
AB16	VSS
AB19	VSS
AB23	VSS
AB26	VSS
AC3	VSS
AC6	VSS
AC8	VSS
AC11	VSS
AC14	VSS
AC16	VSS
AC19	VSS
AC21	VSS
AC24	VSS
AD2	VSS
AD5	VSS
AD8	VSS
AD11	VSS
AD13	VSS
AD16	VSS
AD19	VSS
AD22	VSS
AD25	VSS
AE1	VSS
AE4	VSS
AE8	VSS
AE11	VSS
AE14	VSS
AE16	VSS
AE19	VSS
AE23	VSS
AE26	VSS
AF2	VSS
AF6	VSS
AF8	VSS
AF11	VSS
AF13	VSS
AF16	VSS
AF19	VSS
AF21	VSS
AF25	VSS

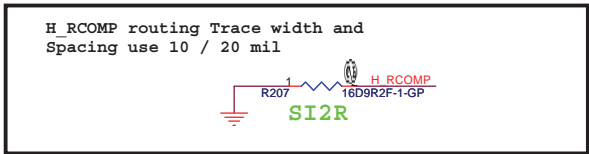
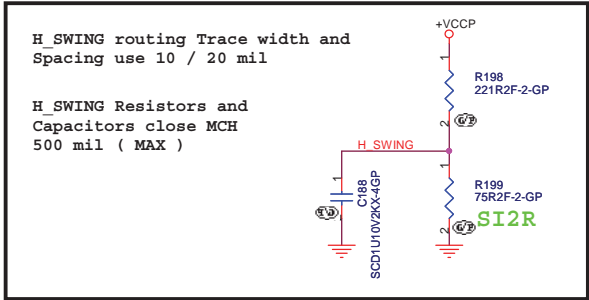
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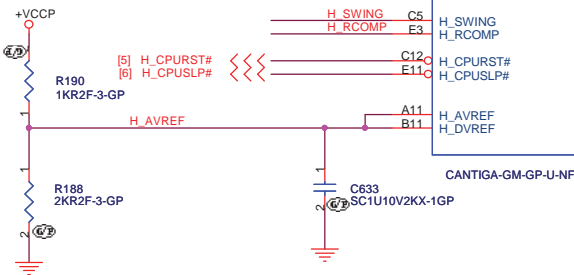
Artemis

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NB (1 of 6) HOST



Place them near to the chip (< 0.5")



U2A		1 OF 10	
H_D#0	F2	H_A#_3	A14
H_D#1	G8	H_A#_4	C15
H_D#2	F8	H_A#_5	F16
H_D#3	E6	H_A#_6	H13
H_D#4	G2	H_A#_7	C18
H_D#5	H6	H_A#_8	M16
H_D#6	H2	H_A#_9	J13
H_D#7	F6	H_A#_10	P16
H_D#8	D4	H_A#_11	R16
H_D#9	H3	H_A#_12	N17
H_D#10	M9	H_A#_13	M13
H_D#11	M11	H_A#_14	E17
H_D#12	J1	H_A#_15	P17
H_D#13	J2	H_A#_16	E17
H_D#14	N12	H_A#_17	G20
H_D#15	J6	H_A#_18	B19
H_D#16	P2	H_A#_19	J16
H_D#17	L2	H_A#_20	E20
H_D#18	R2	H_A#_21	H16
H_D#19	N9	H_A#_22	J20
H_D#20	L6	H_A#_23	L17
H_D#21	M5	H_A#_24	A17
H_D#22	J3	H_A#_25	B17
H_D#23	N2	H_A#_26	L16
H_D#24	R1	H_A#_27	C21
H_D#25	N5	H_A#_28	J17
H_D#26	N6	H_A#_29	H20
H_D#27	P13	H_A#_30	B18
H_D#28	N8	H_A#_31	K17
H_D#29	L7	H_A#_32	B20
H_D#30	N10	H_A#_33	F21
H_D#31	M3	H_A#_34	K21
H_D#32	Y3	H_A#_35	L20
H_D#33	AD14	H_ADS#	H12
H_D#34	Y6	H_ADSTB#_0	B16
H_D#35	Y10	H_ADSTB#_1	G17
H_D#36	Y12	H_BNR#	A9
H_D#37	Y14	H_BPR#	E11
H_D#38	Y7	H_BREQ#	G12
H_D#39	W2	H_DEFER#	B10
H_D#40	AA8	H_DBSY#	AH7
H_D#41	Y9	HPLL_CLK#	AH6
H_D#42	AA13	H_DPWR#	J11
H_D#43	AA9	H_DRDY#	E9
H_D#44	AA11	H_HIT#	E12
H_D#45	AD11	H_HITM#	H11
H_D#46	AD10	H_LOCK#	H11
H_D#47	AD13	H_TRDY#	C9
H_D#48	AE12		
H_D#49	AE9		
H_D#50	AA2		
H_D#51	AD8		
H_D#52	AA3		
H_D#53	AD3		
H_D#54	AD7		
H_D#55	AE14		
H_D#56	AF3		
H_D#57	AC1		
H_D#58	AE3		
H_D#59	AC3		
H_D#60	AE11		
H_D#61	AE8		
H_D#62	AG2		
H_D#63	AD6		

H_A#_35	L20	H_A#35	H_A#[35..3]
H_A#_34	K21	H_A#34	H_A#[35..3]
H_A#_33	F21	H_A#33	H_A#[35..3]
H_A#_32	B20	H_A#32	H_A#[35..3]
H_A#_31	K17	H_A#31	H_A#[35..3]
H_A#_30	B18	H_A#30	H_A#[35..3]
H_A#_29	H20	H_A#29	H_A#[35..3]
H_A#_28	J17	H_A#28	H_A#[35..3]
H_A#_27	C21	H_A#27	H_A#[35..3]
H_A#_26	L16	H_A#26	H_A#[35..3]
H_A#_25	B17	H_A#25	H_A#[35..3]
H_A#_24	A17	H_A#24	H_A#[35..3]
H_A#_23	J20	H_A#23	H_A#[35..3]
H_A#_22	L17	H_A#22	H_A#[35..3]
H_A#_21	H16	H_A#21	H_A#[35..3]
H_A#_20	E20	H_A#20	H_A#[35..3]
H_A#_19	J16	H_A#19	H_A#[35..3]
H_A#_18	B19	H_A#18	H_A#[35..3]
H_A#_17	G20	H_A#17	H_A#[35..3]
H_A#_16	E17	H_A#16	H_A#[35..3]
H_A#_15	P17	H_A#15	H_A#[35..3]
H_A#_14	E17	H_A#14	H_A#[35..3]
H_A#_13	M13	H_A#13	H_A#[35..3]
H_A#_12	N17	H_A#12	H_A#[35..3]
H_A#_11	R16	H_A#11	H_A#[35..3]
H_A#_10	P16	H_A#10	H_A#[35..3]
H_A#_9	J13	H_A#9	H_A#[35..3]
H_A#_8	M16	H_A#8	H_A#[35..3]
H_A#_7	C18	H_A#7	H_A#[35..3]
H_A#_6	H13	H_A#6	H_A#[35..3]
H_A#_5	F16	H_A#5	H_A#[35..3]
H_A#_4	C15	H_A#4	H_A#[35..3]
H_A#_3	A14	H_A#3	H_A#[35..3]

H_DIN#_0	J8	H_DIN#0	H_DINV#[3..0]
H_DIN#_1	L3	H_DIN#1	H_DINV#[3..0]
H_DIN#_2	Y13	H_DIN#2	H_DINV#[3..0]
H_DIN#_3	Y1	H_DIN#3	H_DINV#[3..0]
H_DSTB#_0	L10	H_DSTB#0	H_DSTB#[3..0]
H_DSTB#_1	M7	H_DSTB#1	H_DSTB#[3..0]
H_DSTB#_2	AA5	H_DSTB#2	H_DSTB#[3..0]
H_DSTB#_3	AE6	H_DSTB#3	H_DSTB#[3..0]
H_DSTBP#_0	L9	H_DSTBP#0	H_DSTBP#[3..0]
H_DSTBP#_1	M8	H_DSTBP#1	H_DSTBP#[3..0]
H_DSTBP#_2	AA6	H_DSTBP#2	H_DSTBP#[3..0]
H_DSTBP#_3	AE5	H_DSTBP#3	H_DSTBP#[3..0]
H_REQ#_0	B15	H_REQ#0	H_REQ#[4..0]
H_REQ#_1	K13	H_REQ#1	H_REQ#[4..0]
H_REQ#_2	E13	H_REQ#2	H_REQ#[4..0]
H_REQ#_3	B13	H_REQ#3	H_REQ#[4..0]
H_REQ#_4	B14	H_REQ#4	H_REQ#[4..0]
H_RS#_0	B6	H_RS#0	H_RS#[2..0]
H_RS#_1	F12	H_RS#1	H_RS#[2..0]
H_RS#_2	C8	H_RS#2	H_RS#[2..0]

HOST

VOX

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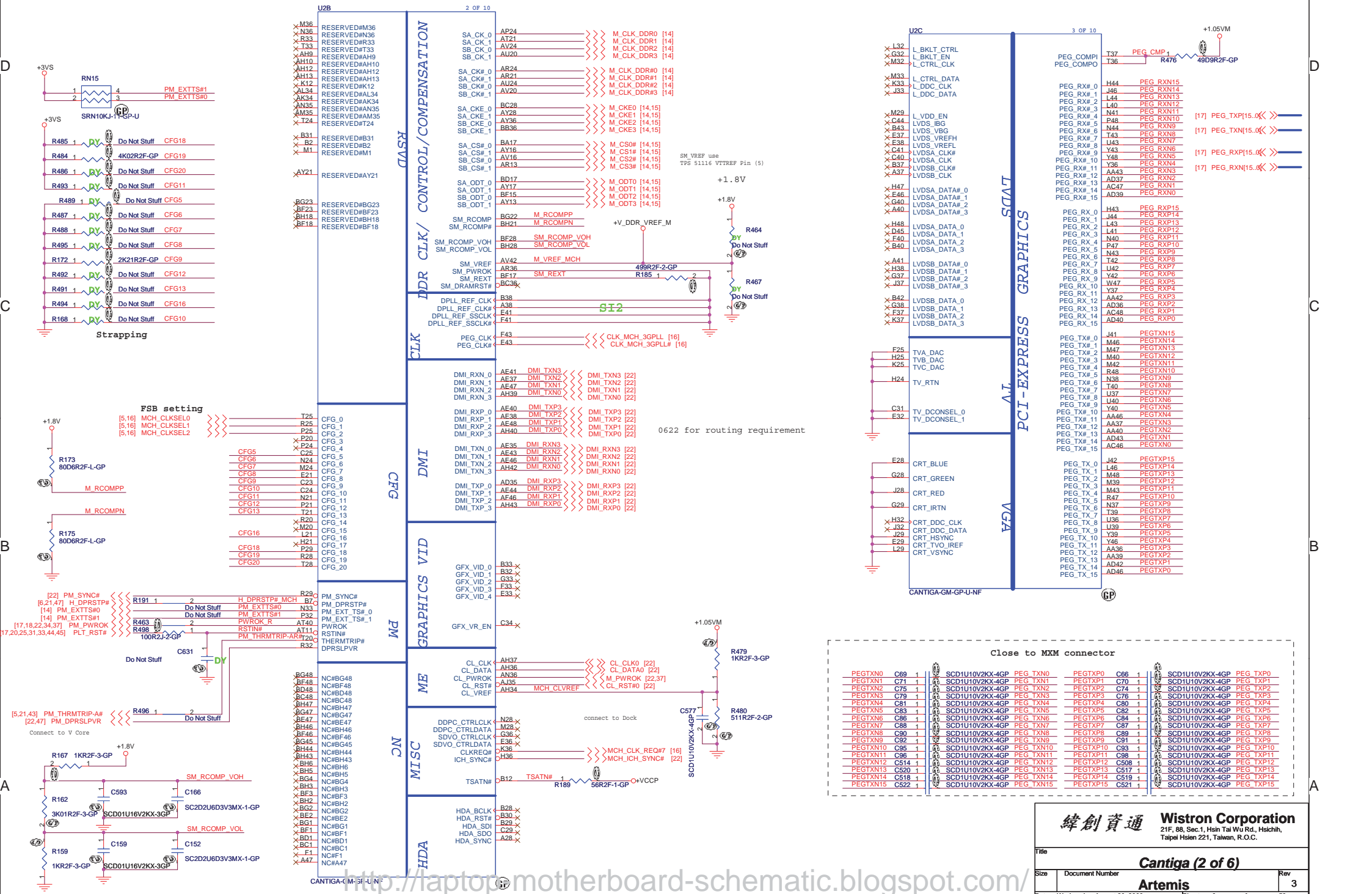
Title: **Cantiga (1 of 6)**

Size: Document Number: **Artemis** Rev: **3**

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NB (2 of 6) 3 PEG/DMI

Place the 49D9 Ohm resistor within 500 mils (1.27 mm) of the (G)MCH.



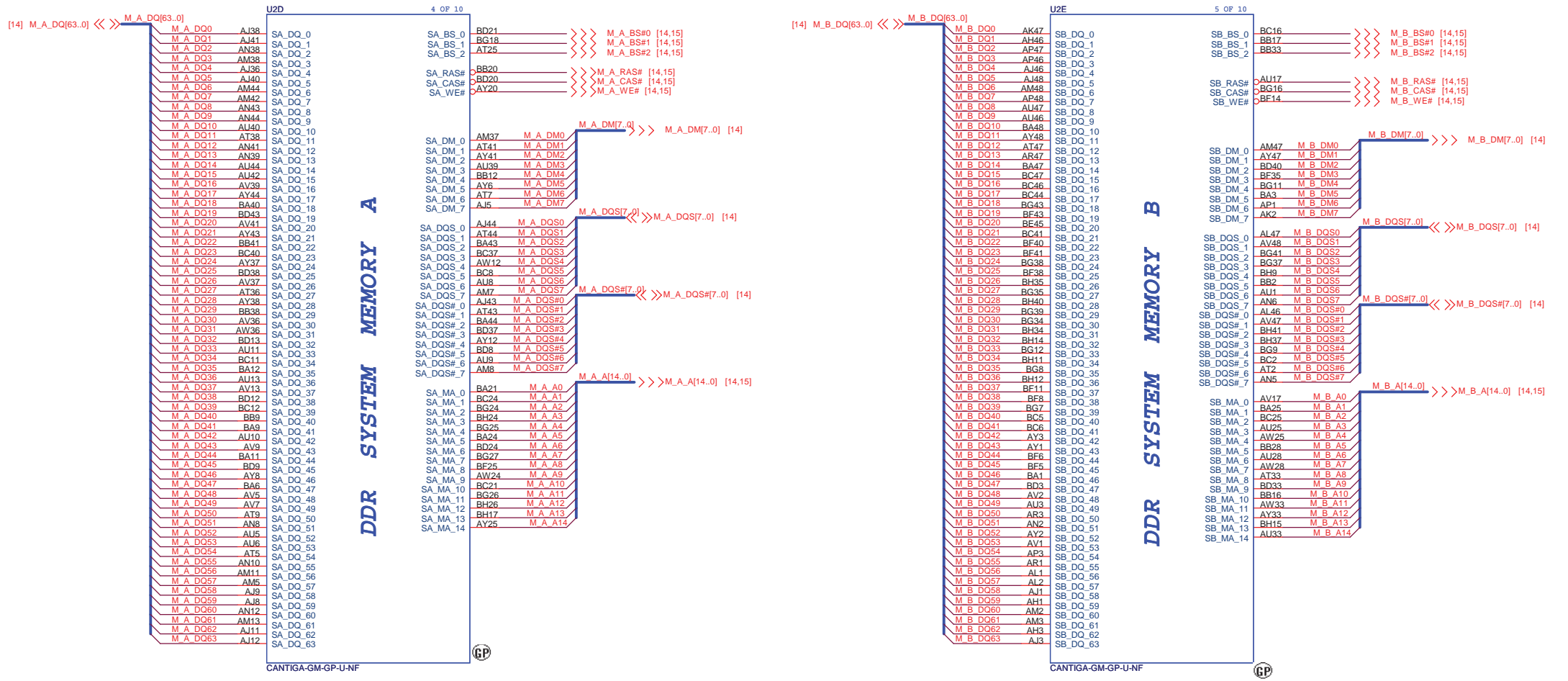
緯創資通 **Wistron Corporation**
 21F, 88, Sec. 1, Hsin Tai Wu Rd., Hsichih,
 Taipei Hsien 221, Taiwan, R.O.C.

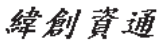
Title: **Cantiga (2 of 6)**

Size: Document Number: **Artemis** Rev: **3**

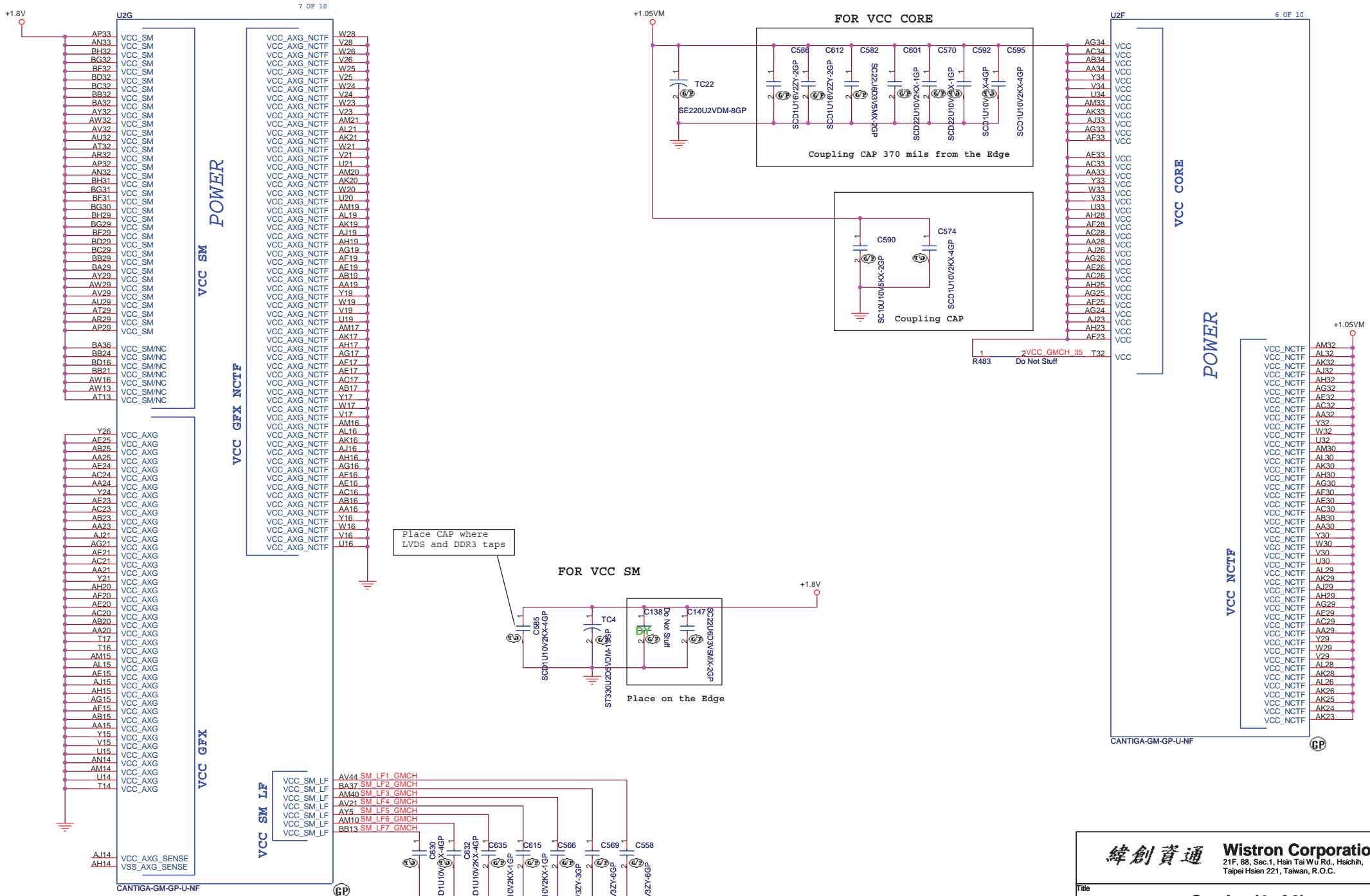
Date: Wednesday, August 20, 2008 Sheet: 9 of 53

NB (3 of 6) DDRIII



 Wistron Corporation 21F, 88, Sec. 1, Hsin Tai Wu Rd., Hstichih, Taipei Hsien 221, Taiwan, R.O.C.		
Cantiga (3 of 6)		
Title		
Size	Document Number	Rev
Artemis		3
Date: Wednesday, August 20, 2008		Sheet 10 of 53

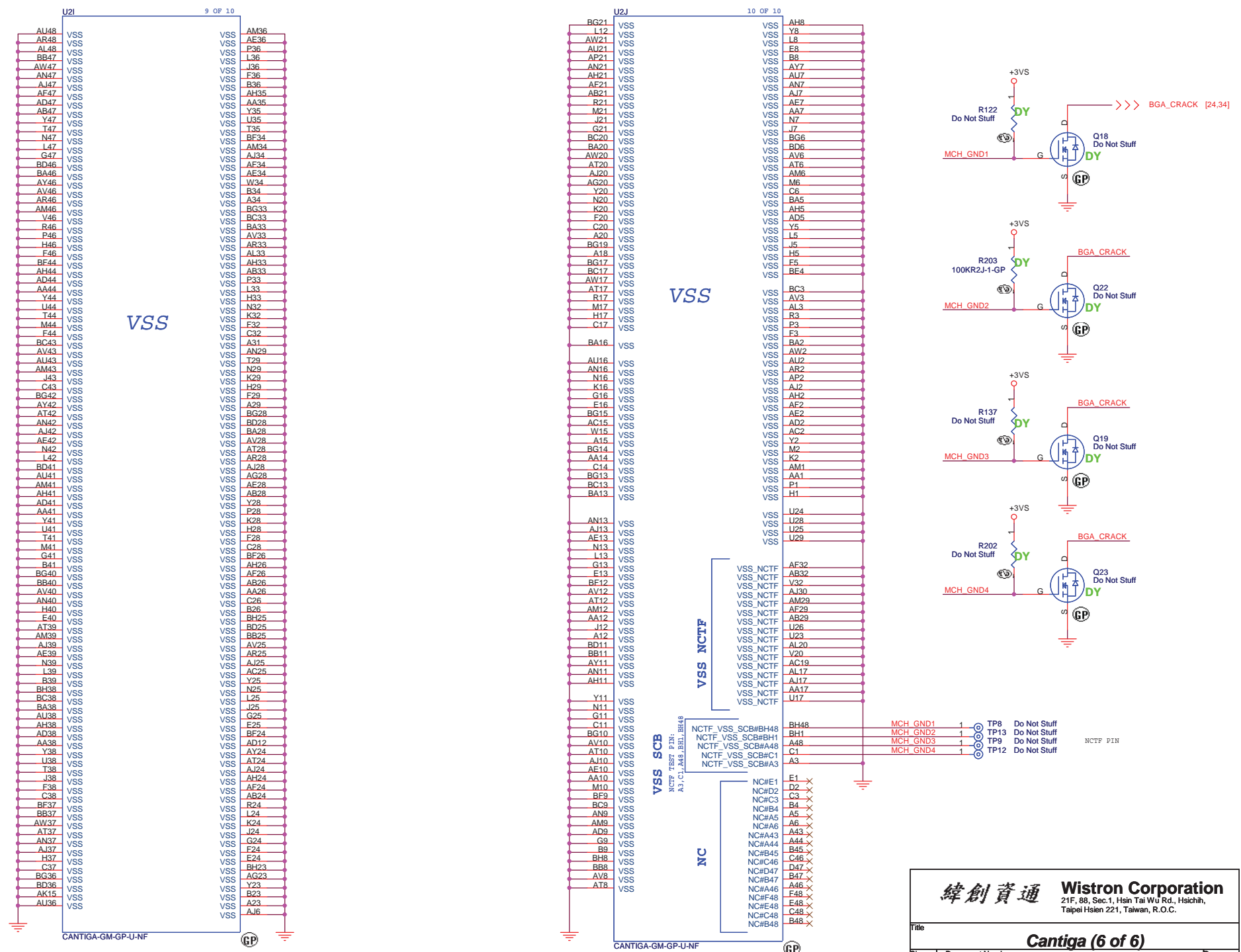
NB (4 of 6) PWR



Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.		
Title: Cantiga (4 of 6)		
Size	Document Number	Rev
		3
Date: Wednesday, August 20, 2008		Sheet 11 of 53

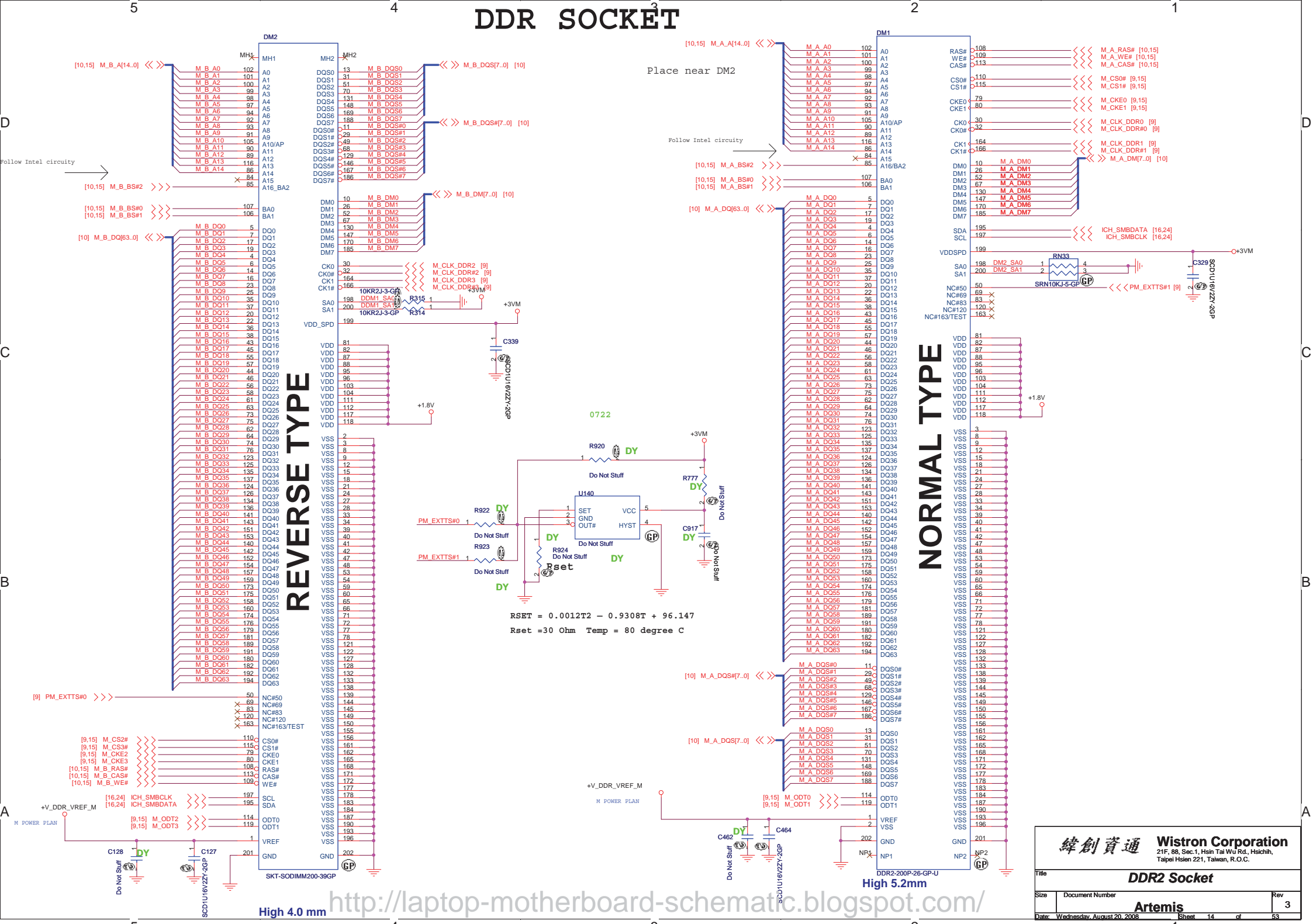
NB (6 of 6) GND

07/20 BGA CRACK CIRCUIT



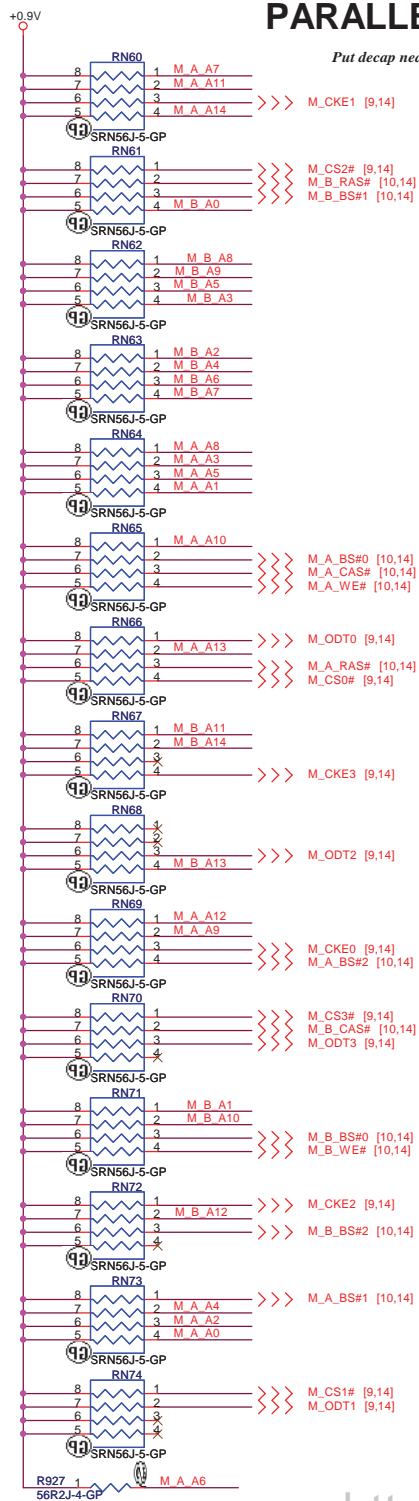
緯創資通 Wistron Corporation	
21F, 88, Sec. 1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title: Cantiga (6 of 6)	
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DDR SOCKET



PARALLEL TERMINATION

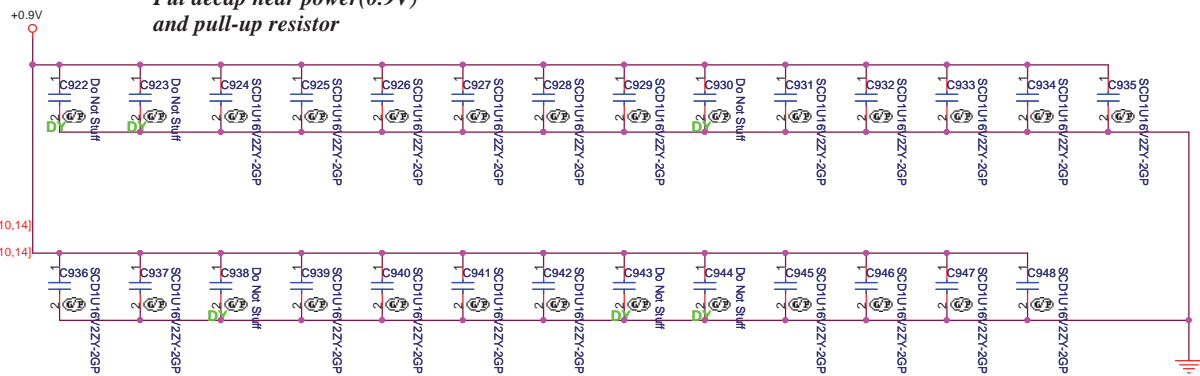
Put decap near power(0.9V) and pull-up resistor



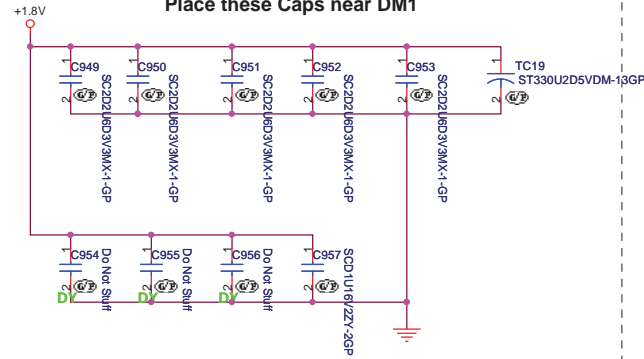
M_A A[14..0] <<< M_A_A[14..0] [10,14]
 M_B A[14..0] <<< M_B_A[14..0] [10,14]

Decoupling Capacitor

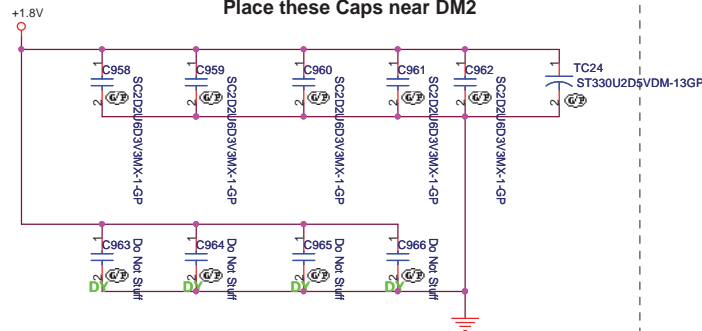
Put decap near power(0.9V) and pull-up resistor



Place these Caps near DM1



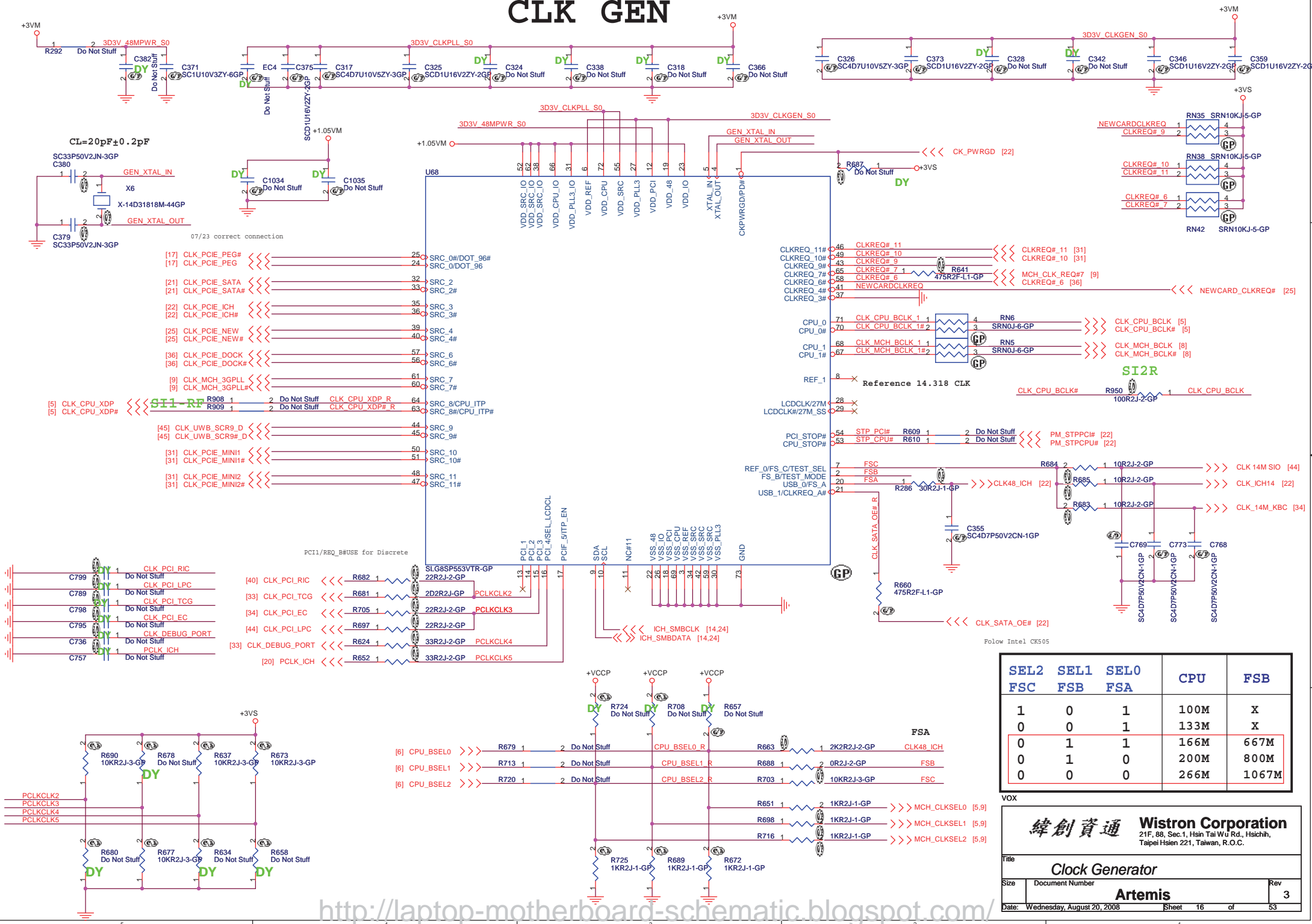
Place these Caps near DM2



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Title DDR2 Termination Resistor		
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CLK GEN



SEL2	SEL1	SEL0	CPU	FSB
FSC	FSB	FSA		
1	0	1	100M	X
0	0	1	133M	X
0	1	1	166M	667M
0	1	0	200M	800M
0	0	0	266M	1067M

VOX

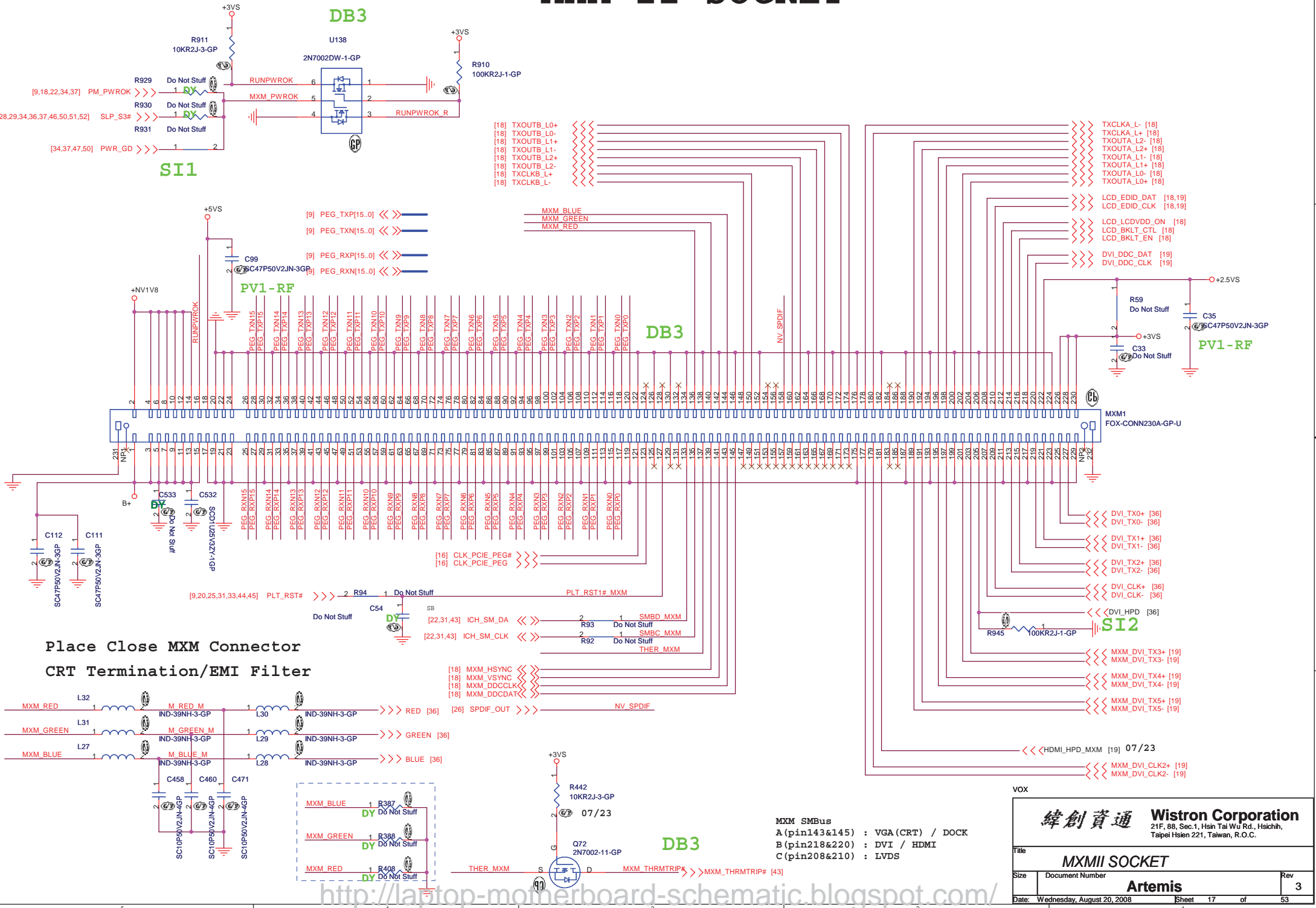
緯創資通 Wistron Corporation
 21F, 88, Sec. 1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.

Title: **Clock Generator**

Size: Document Number **Artemis** Rev **3**

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MXM II SOCKET



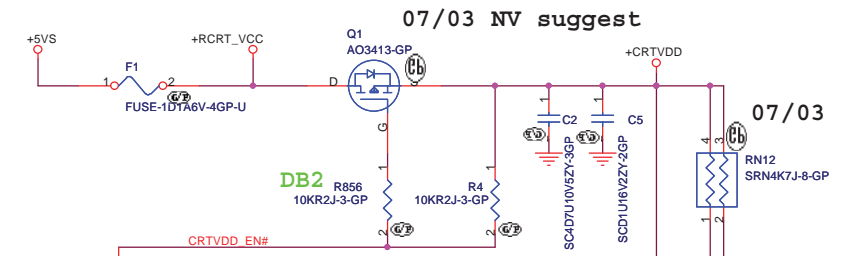
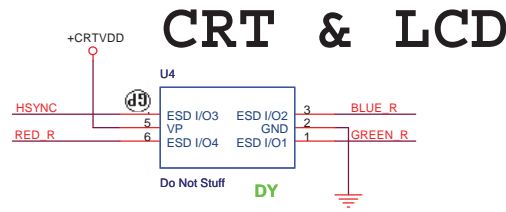
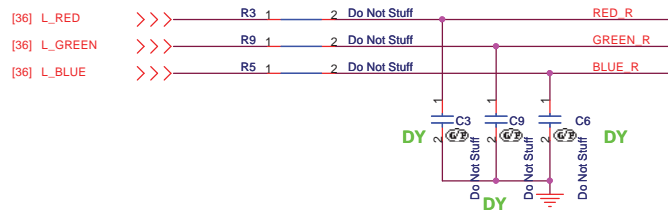
Place Close MXM Connector
CRT Termination/EMI Filter

VOX

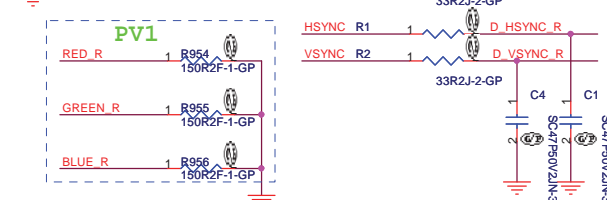
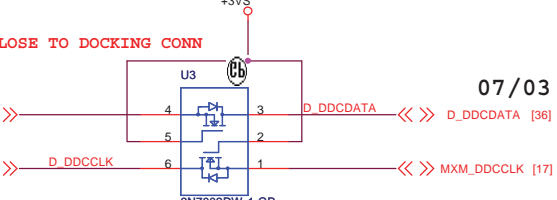
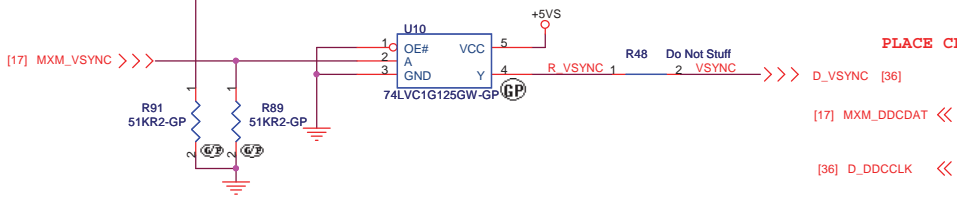
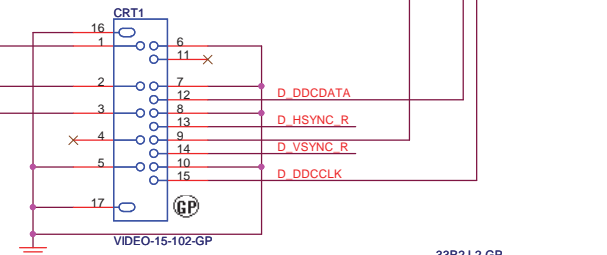
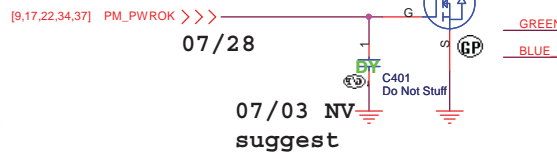
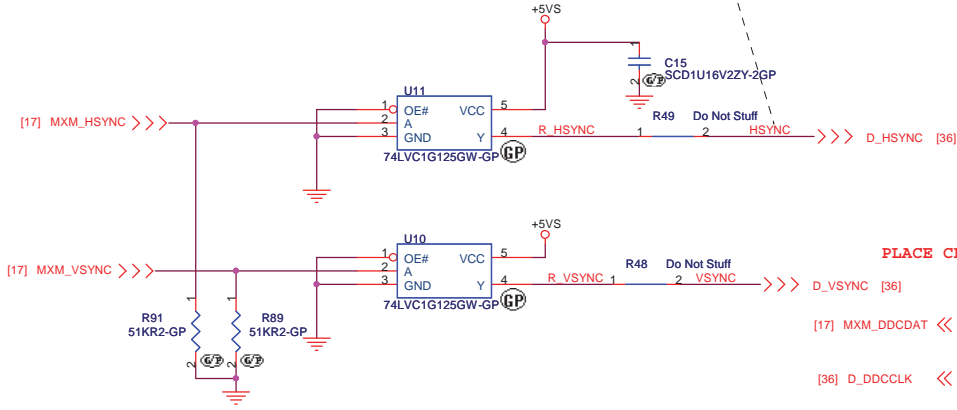
緯創資通 Wistron Corporation
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Title		MXMII SOCKET	
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Date	Wednesday, August 20, 2008	Sheet	17 of 53
			3

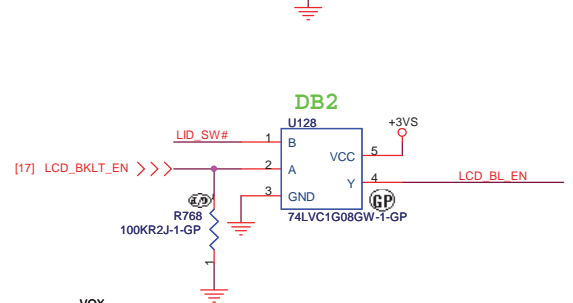
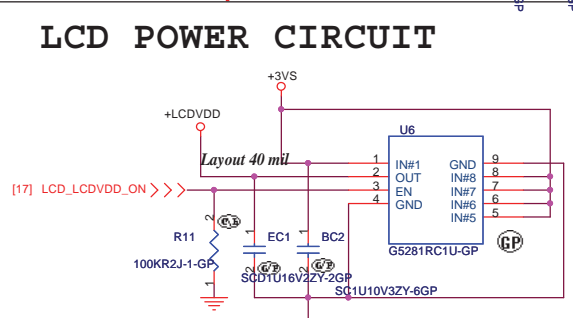
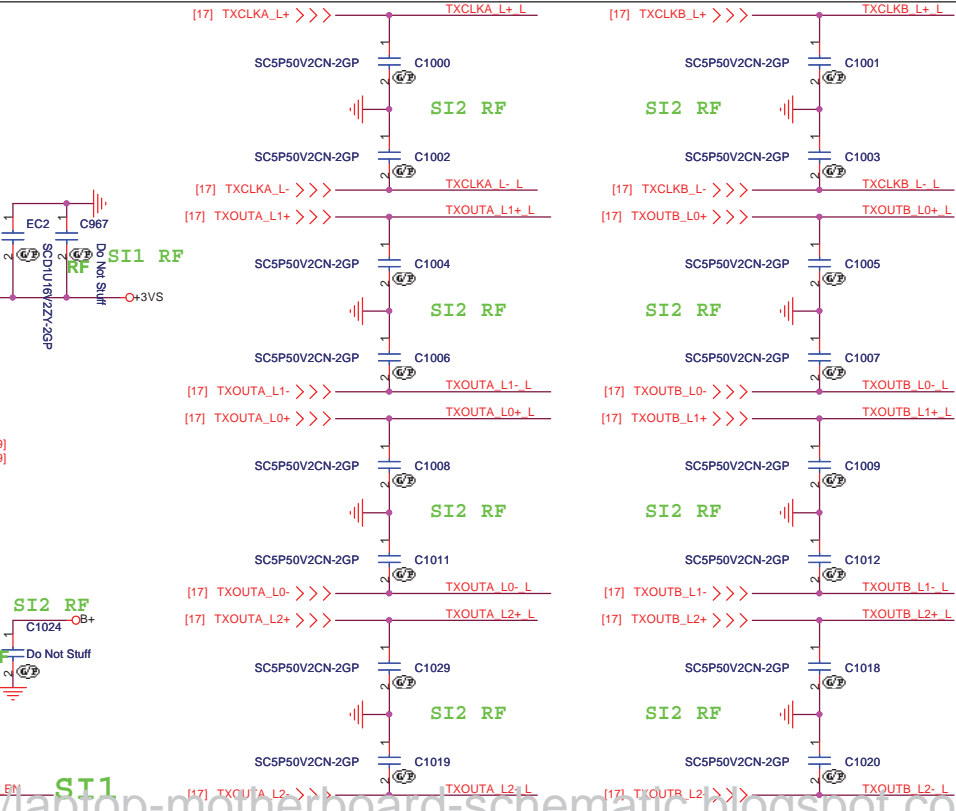
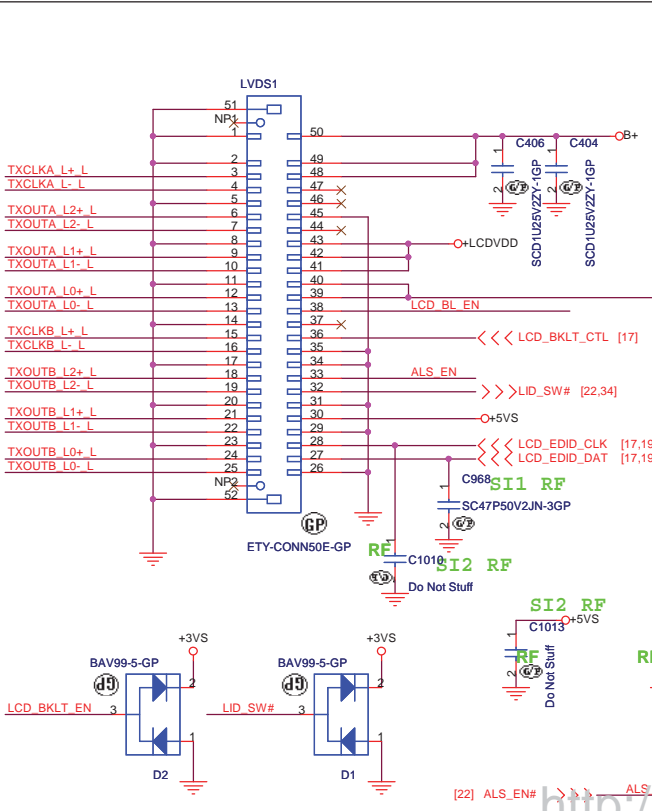
MXM SMBus
A (pin143&145) : VGA(CRT) / DOCK
B (pin218&220) : DVI / HDMI
C (pin208&210) : LVDS



Layout Note : HSYNC & VSYNC SHOULD BE ROUTED TO DOCK CRT CONN. , THEN TO SYSTEM CRT CONN.



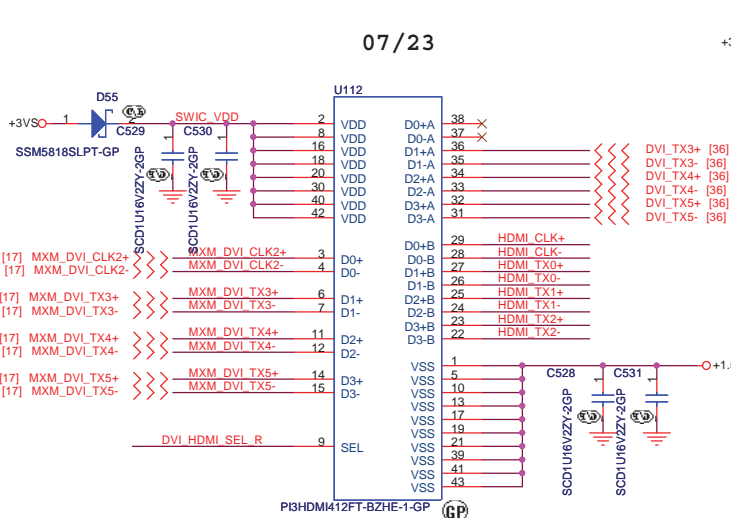
LCD POWER CIRCUIT



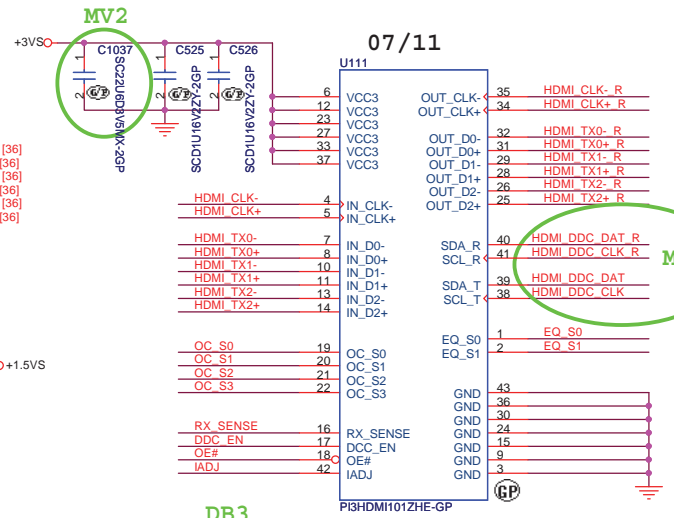
緯創資通 Wistron Corporation
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CRT/LCD CONNECTOR

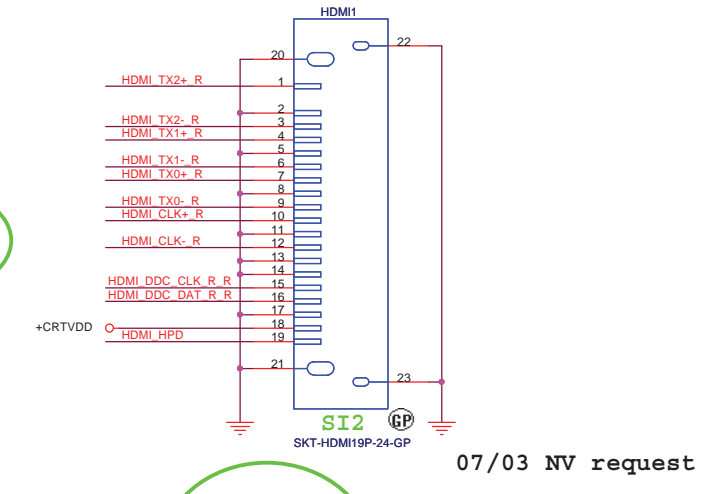
Title	Document Number		
Size	Artemis		
A3	Rev 3		
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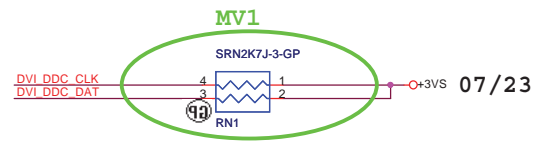
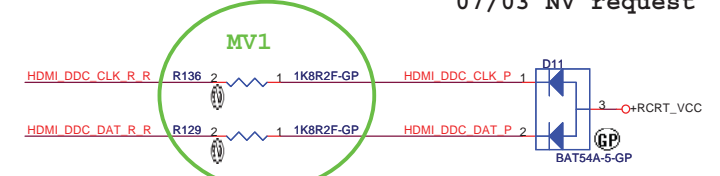
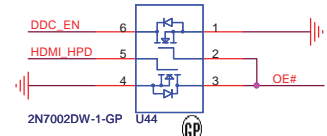
07/23



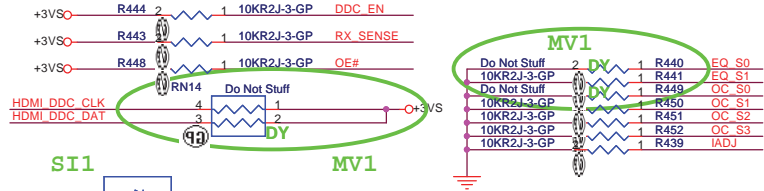
07/11



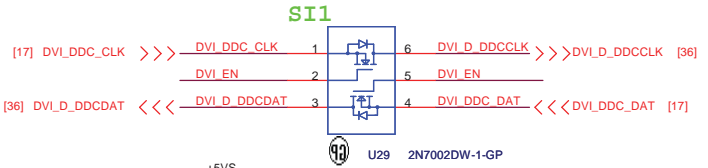
07/03 NV request



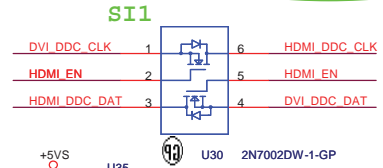
07/23



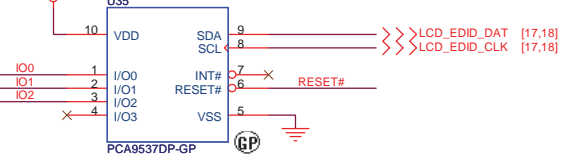
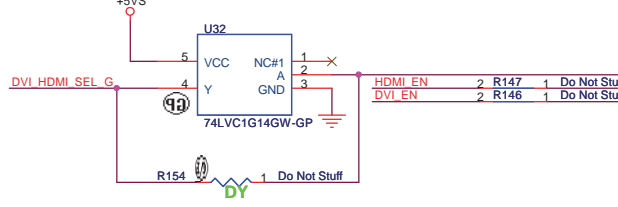
MV1



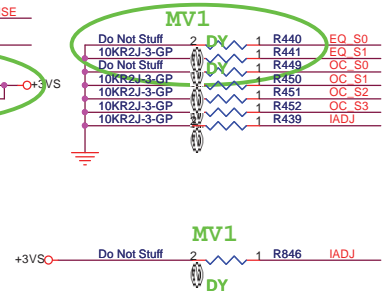
SI1



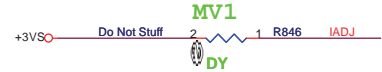
SI1



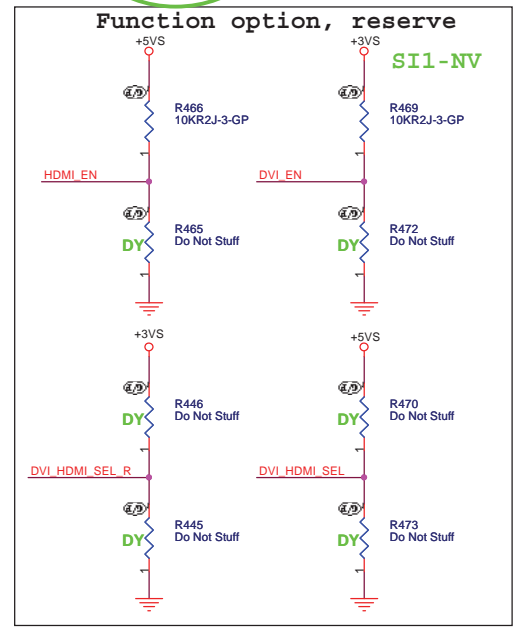
07/04 NV request



MV1

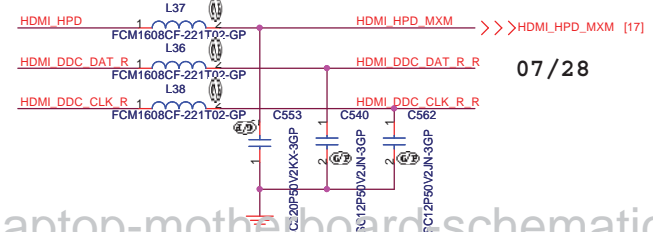


MV1



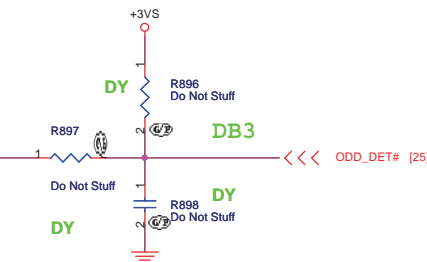
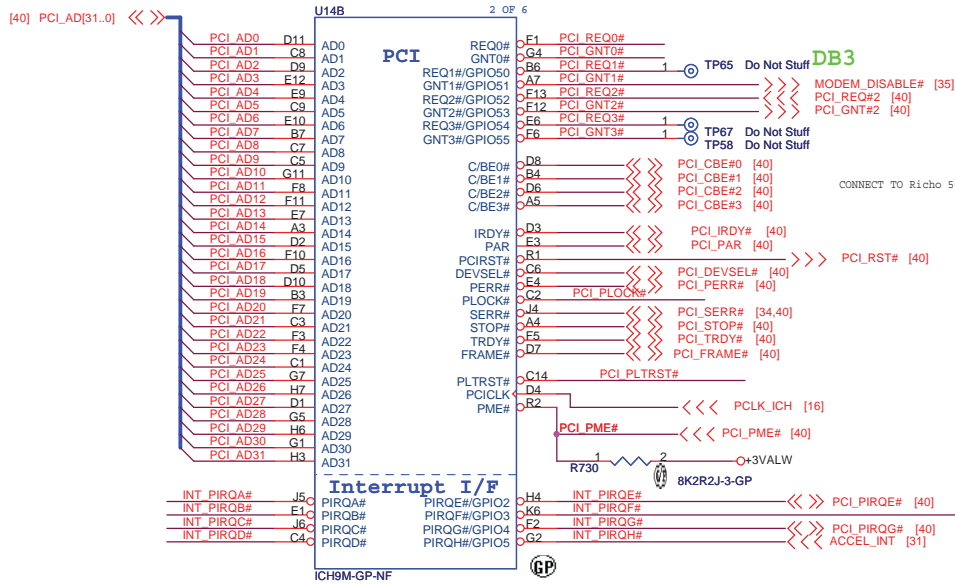
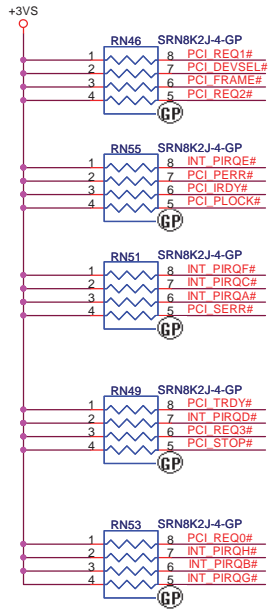
Function option, reserve

SI1-NV

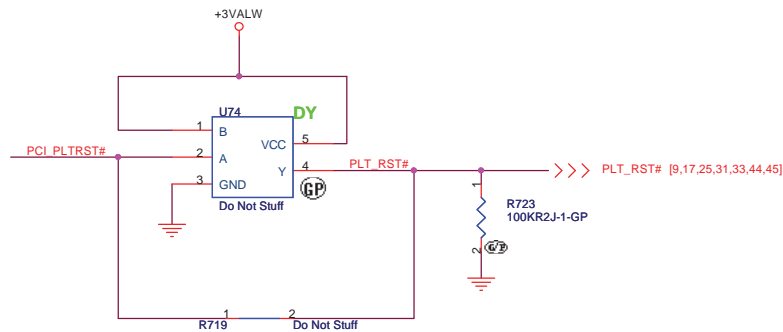


07/28

ICH9-M (1 of 5) PCI



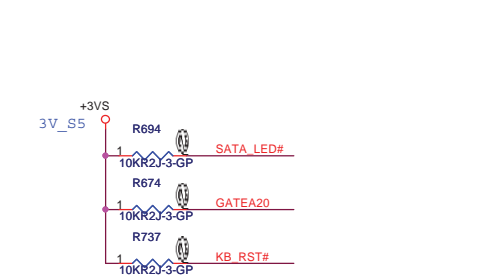
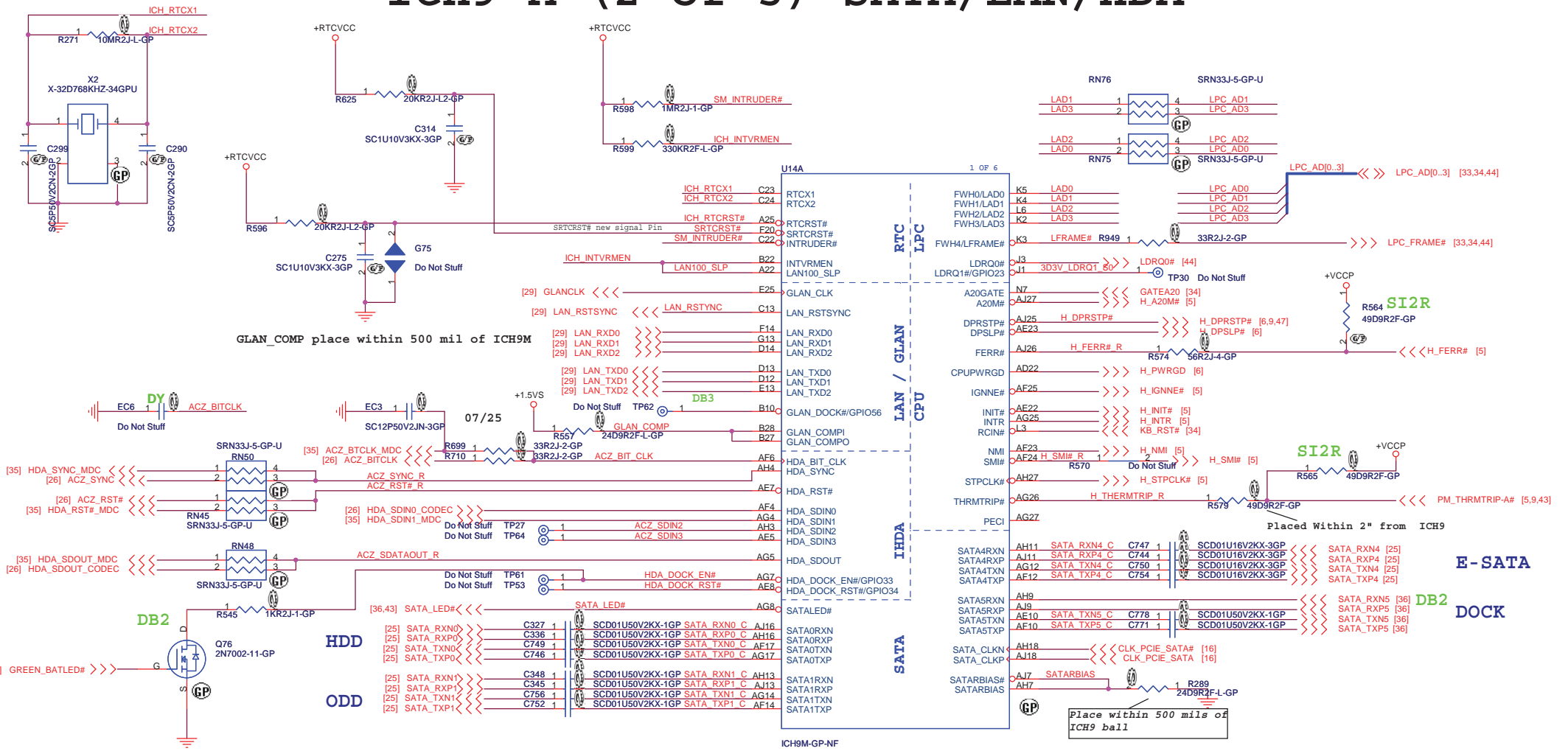
BOOT BIOS Strap		
PCI_GNT#0	SPI_CS#1	BOOT BIOS Location
0	1	SPT
1	0	PCI
1	1	LPC(Default)
A16 swap override strap		
PCI_GNT#3	low = A16 swap override enable	high = default



VOX

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ICH9-M (1 of 5)	
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ICH9-M (2 of 5) SATA/LAN/HDA



integrated VccSus1_05,VccSus1_5,VccCL1_5	
INTVRMEN	High=Enable Low=Disable
integrated VccLan1_05VccCL1_05	
LAN100_SLP	High=Enable Low=Disable

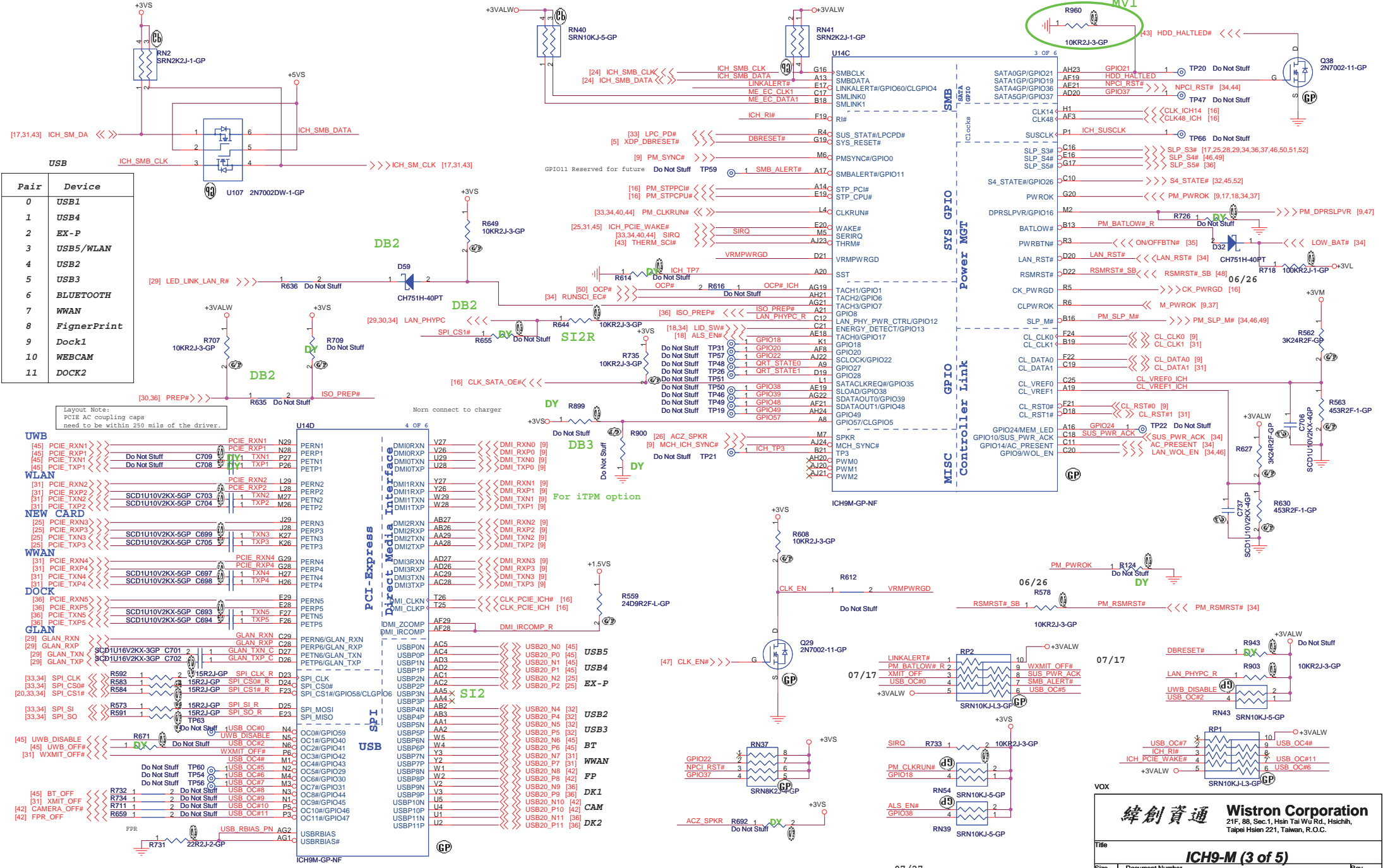
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ICH9-M (2 of 5)

Artemis

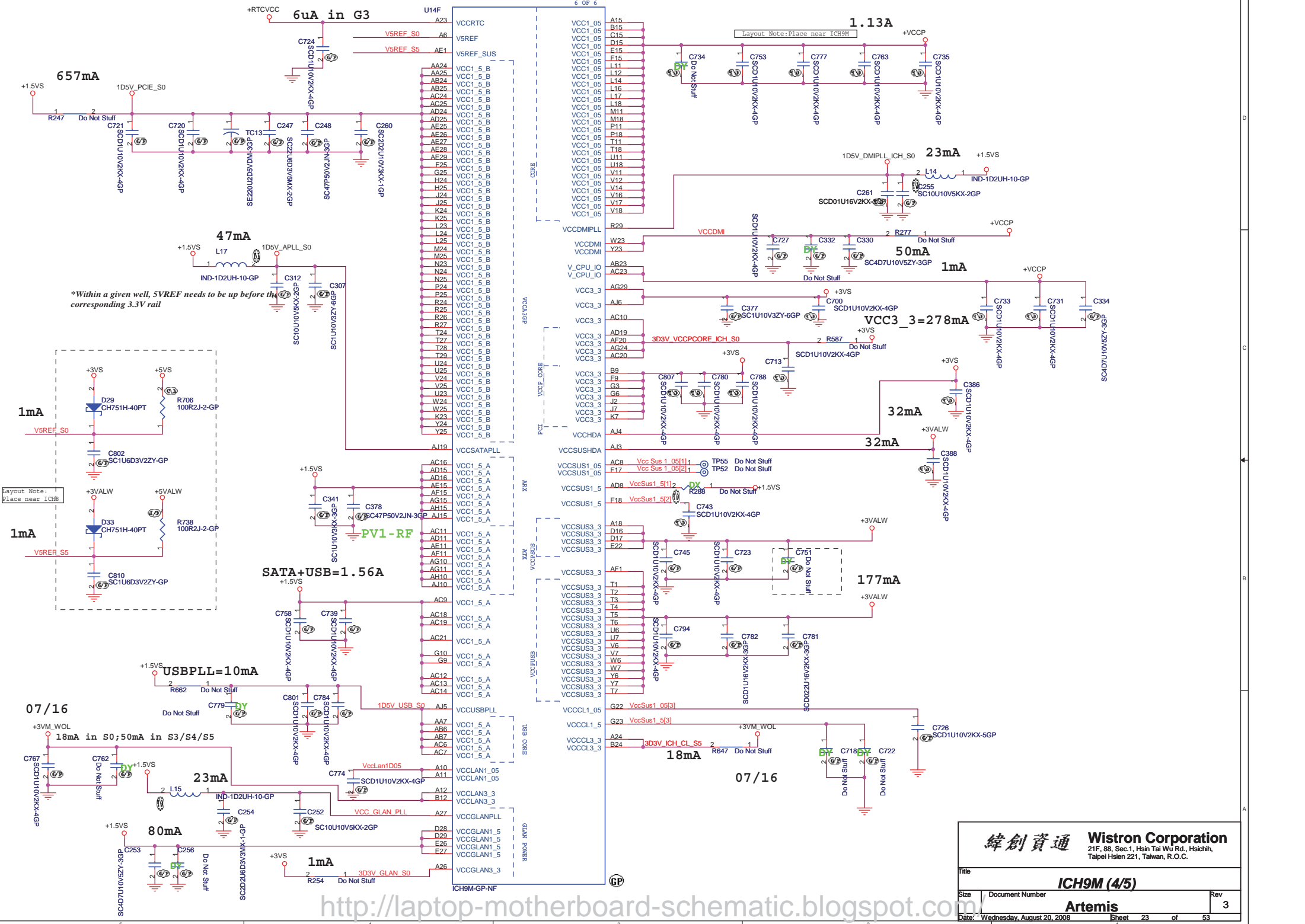
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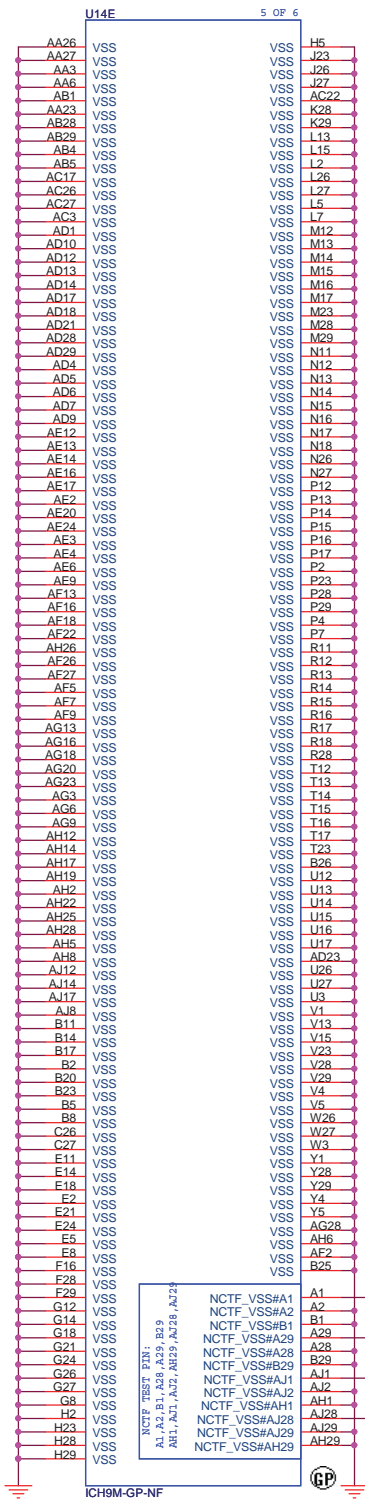
ICH9-M (3 of 5) USB/PCIE/DMI



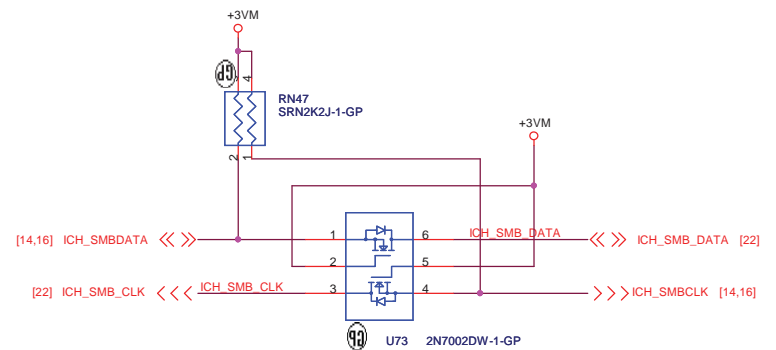
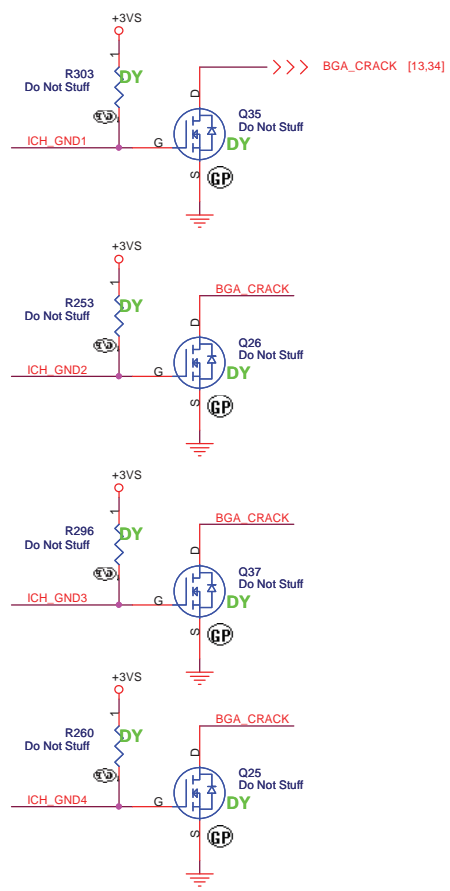
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ICH9-M (3 of 5)		
Artemis		
Title	Document Number	Rev
		3
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07/20 BGA CRACK CIRCUIT



Q13 & Q14 connect SMLINK and SMBUS in S) for SMBus 2.0 compliance

SMBUS

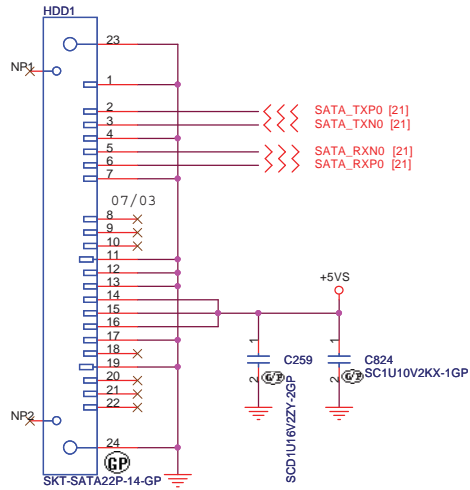
緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.

Title: ICH9-M (5 of 5)

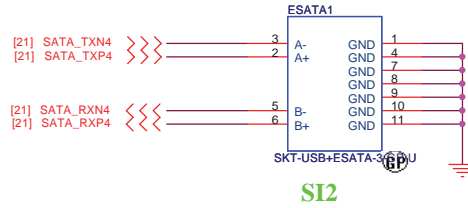
Size	Document Number	Rev
		3

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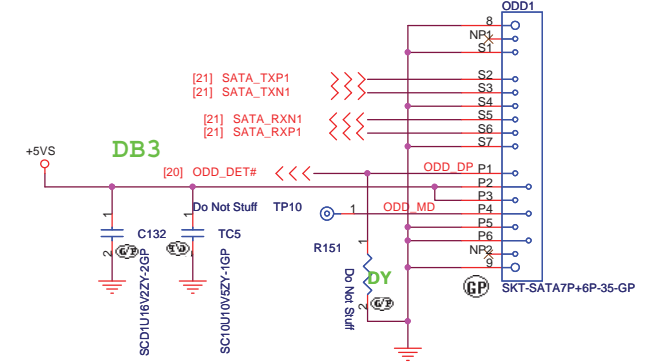
SATA HDD Connector



ESATA Connector

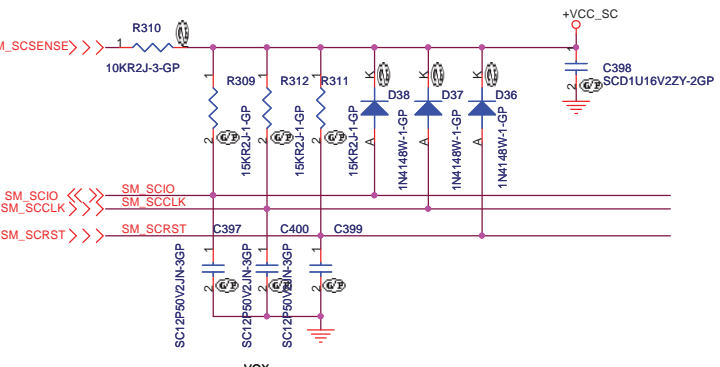
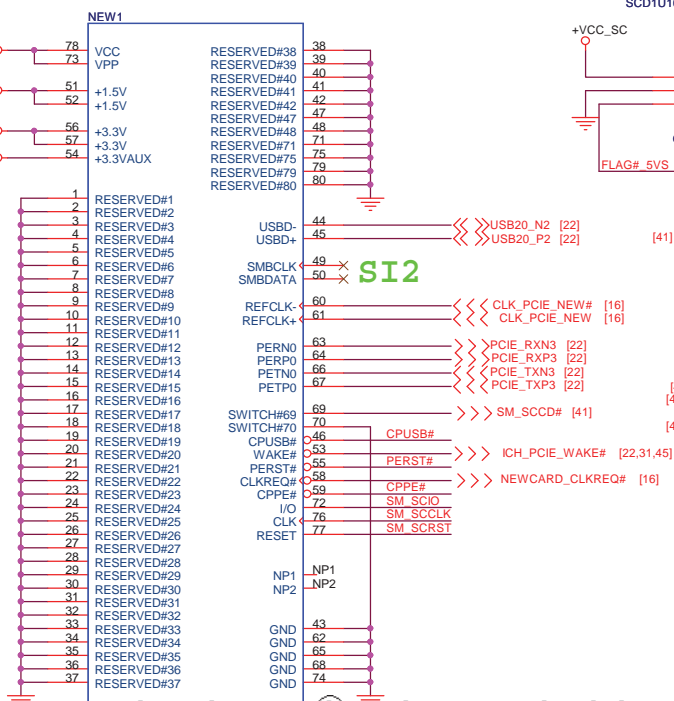
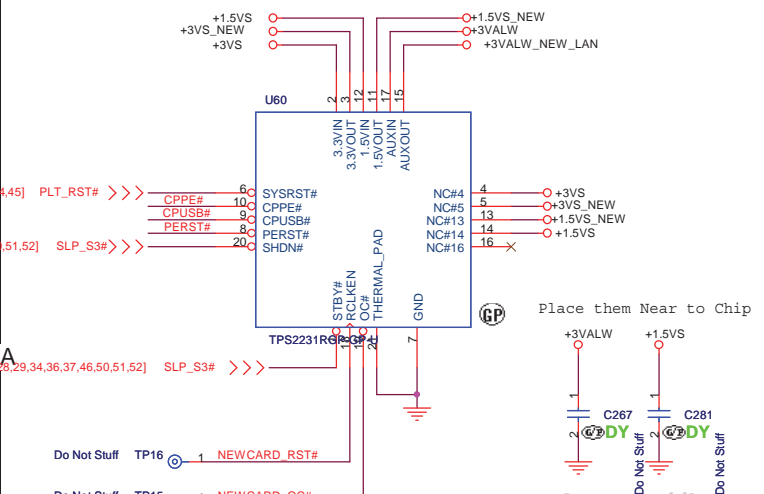
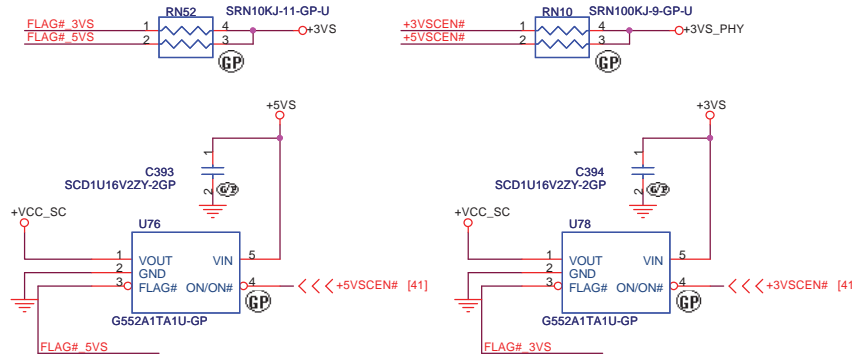
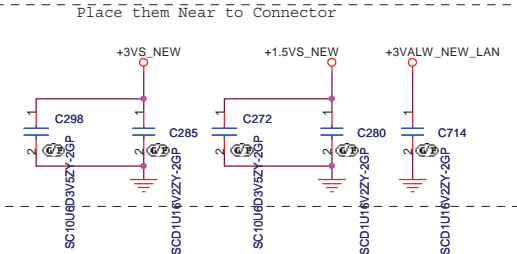
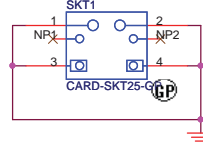


ODD Connector



NEWCARD/SMART CARD Connector

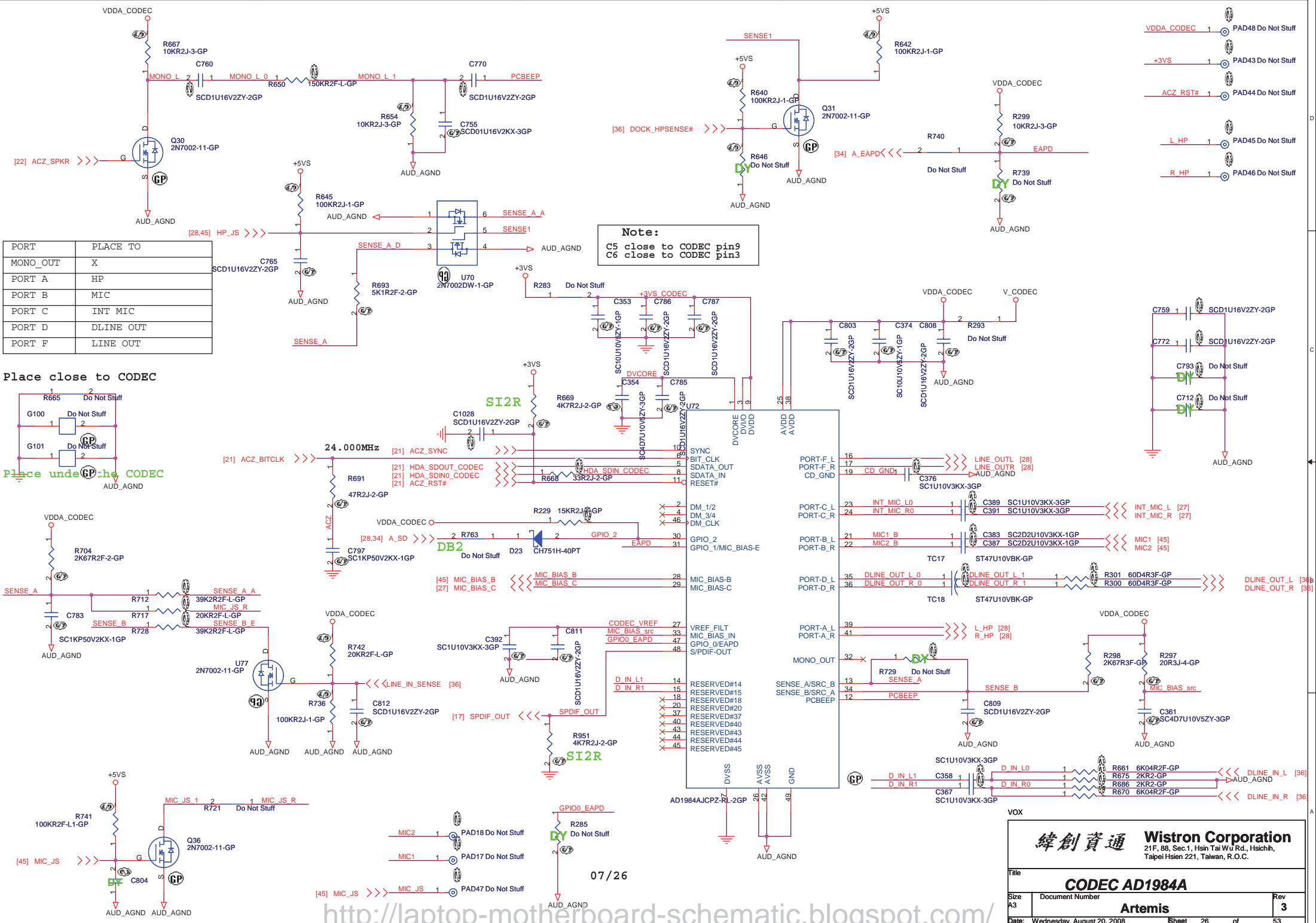
For Newcard socket



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HDD/NEW CARD CONN.

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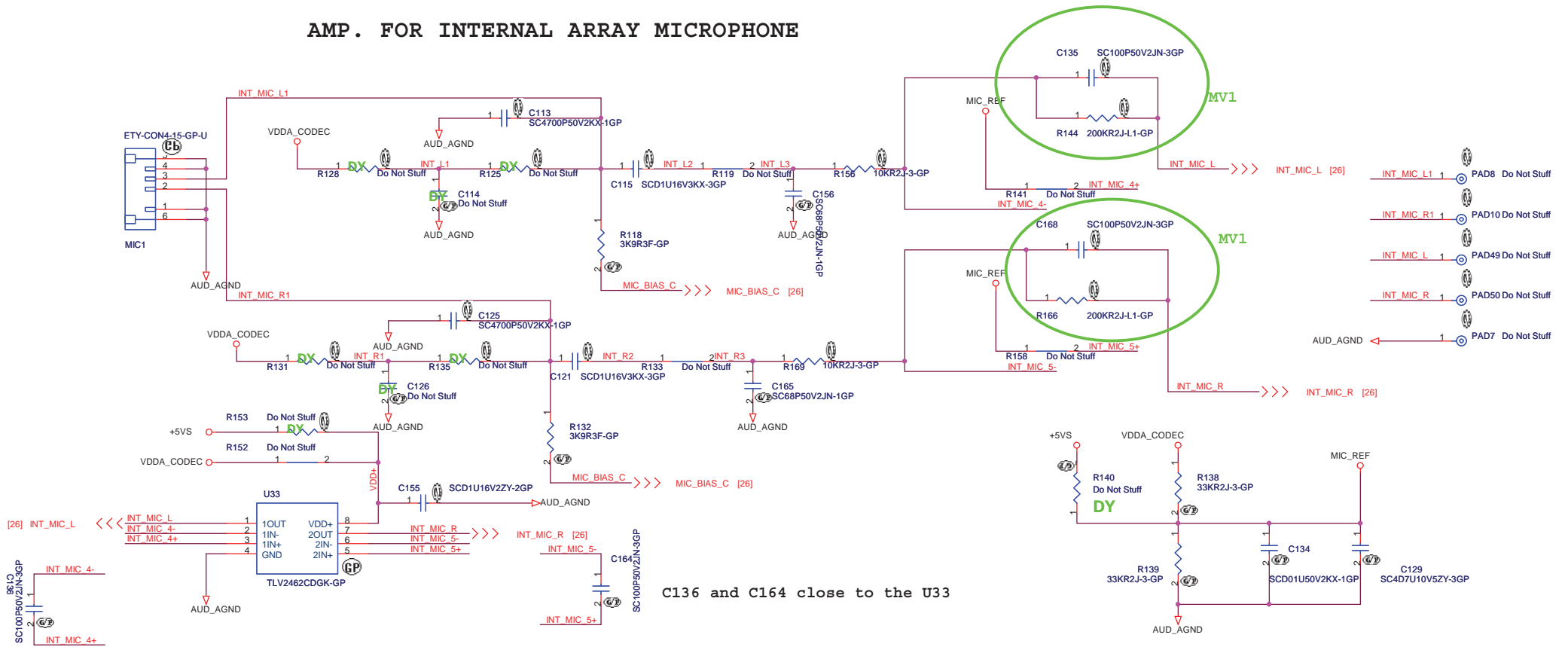
<http://laptop-motherboard-schematic.blogspot.com/>

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File: **CODEC AD1984A**

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AMP. FOR INTERNAL ARRAY MICROPHONE



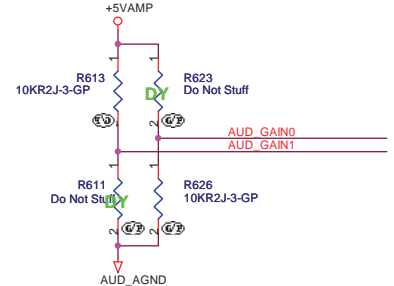
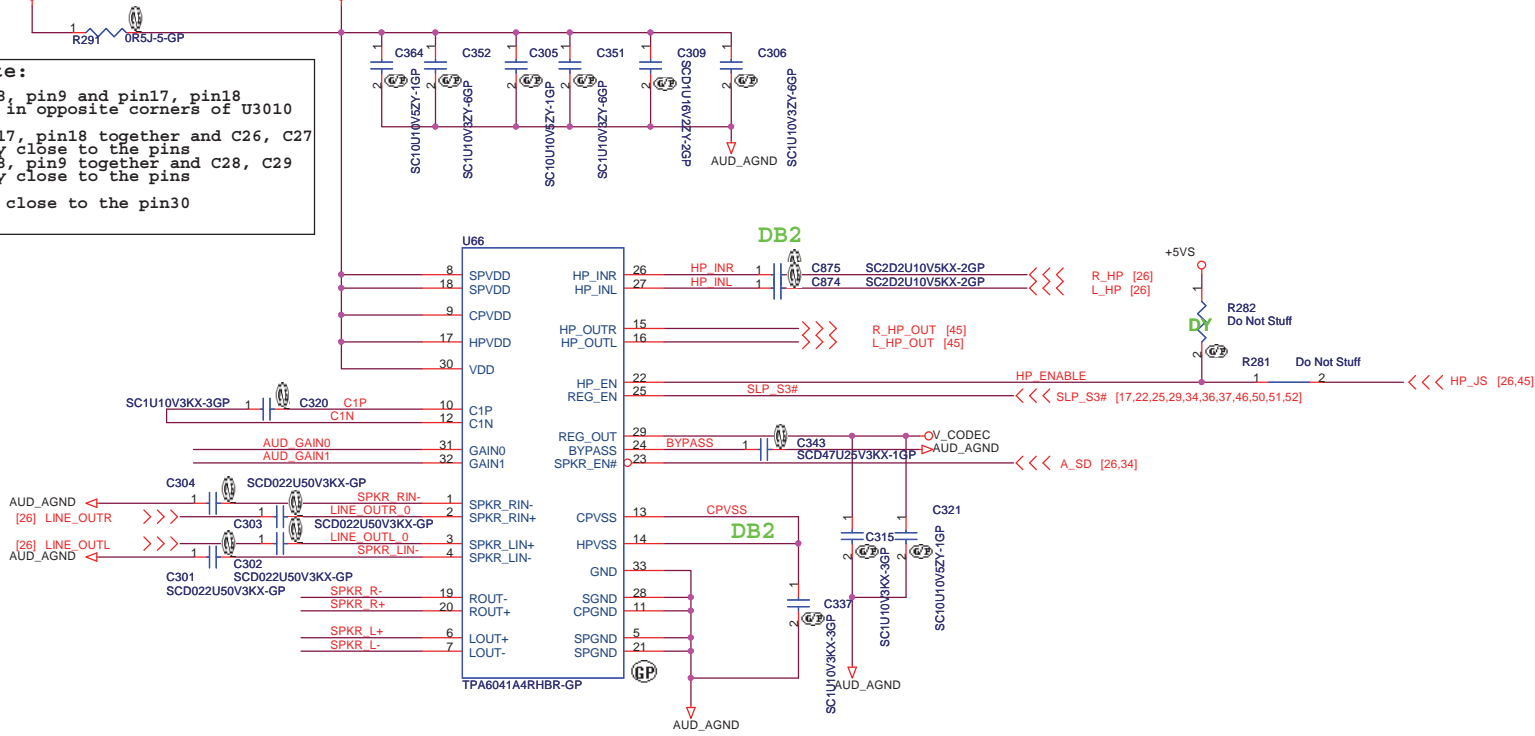
VOX

緯創資通 Wistron Corporation 21F, 88, Sec. 1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
INT MIC	
Size A3	Document Number Artemis
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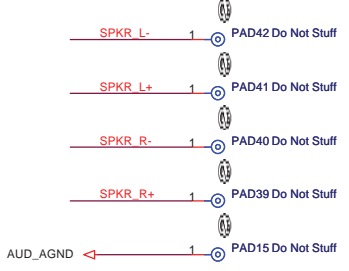
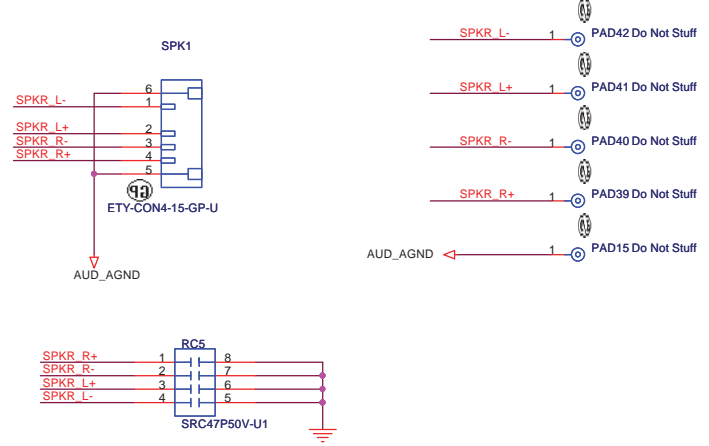
SI2R
+5VS

+5VAMP

Note:
 pin8, pin9 and pin17, pin18
 are in opposite corners of U3010
 pin17, pin18 together and C26, C27
 very close to the pins
 pin8, pin9 together and C28, C29
 very close to the pins
 C32 close to the pin30



Speaker CONN.

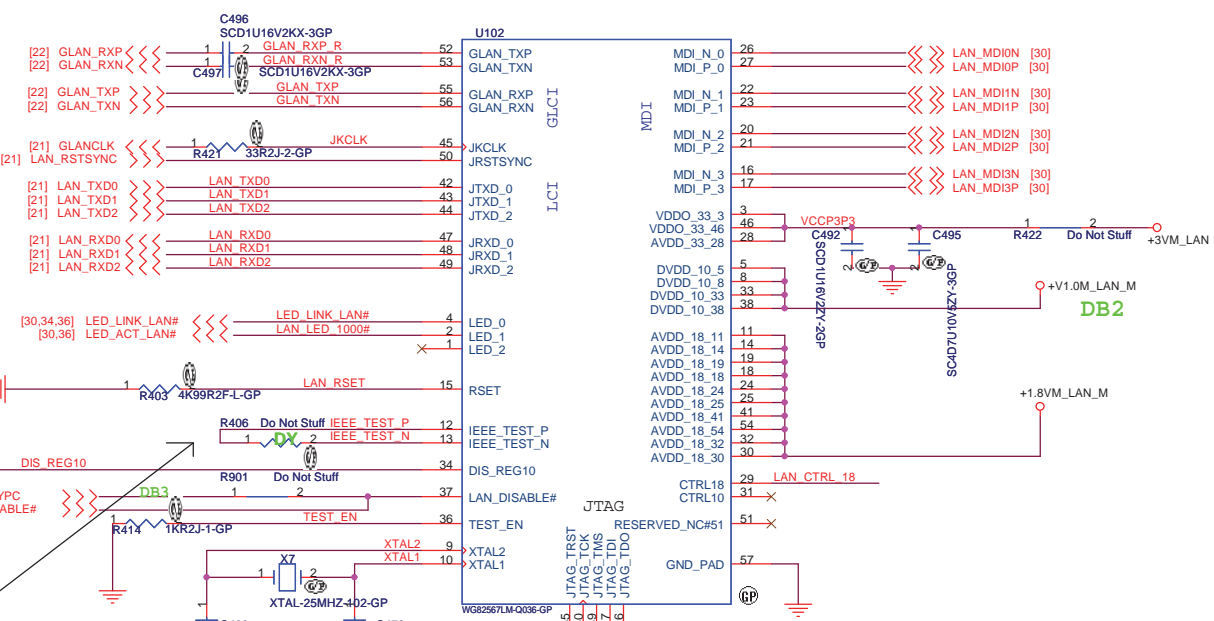
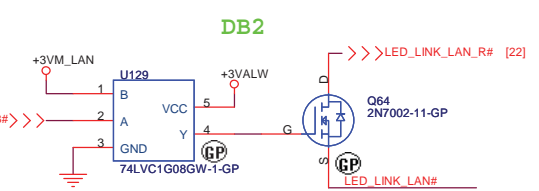
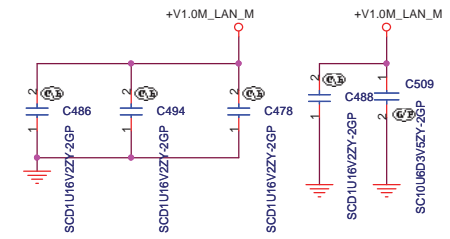
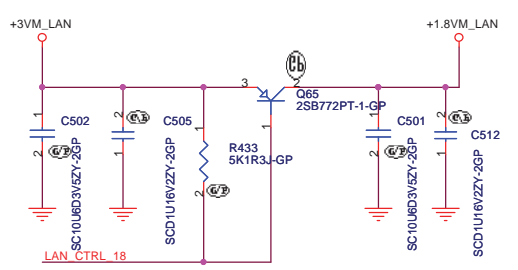
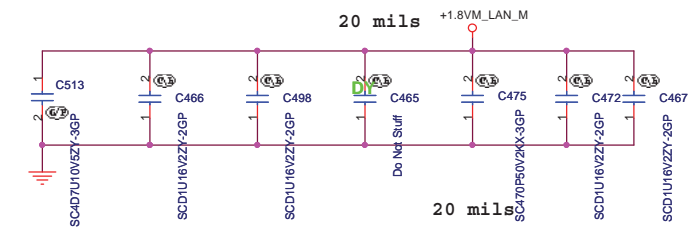
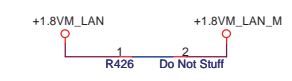
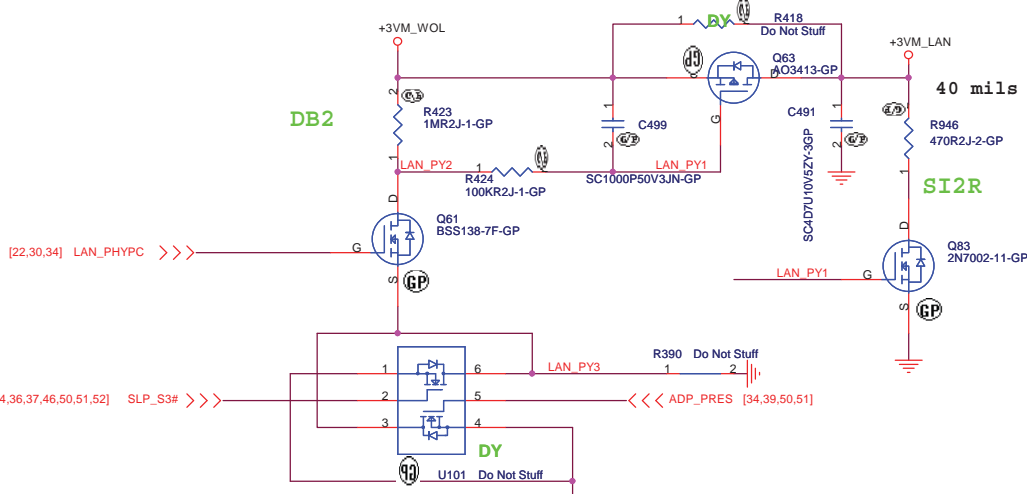


VOX

緯創資通 Wistron Corporation
 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
 Taipei Hsien 221, Taiwan, R.O.C.

Title: **AMP & SPEAKER**

Size A3	Document Number	Rev 3
Date: Wednesday, August 20, 2008	Sheet 28	of 53



Layout Note
Keep this R406 on top side
and route differentially

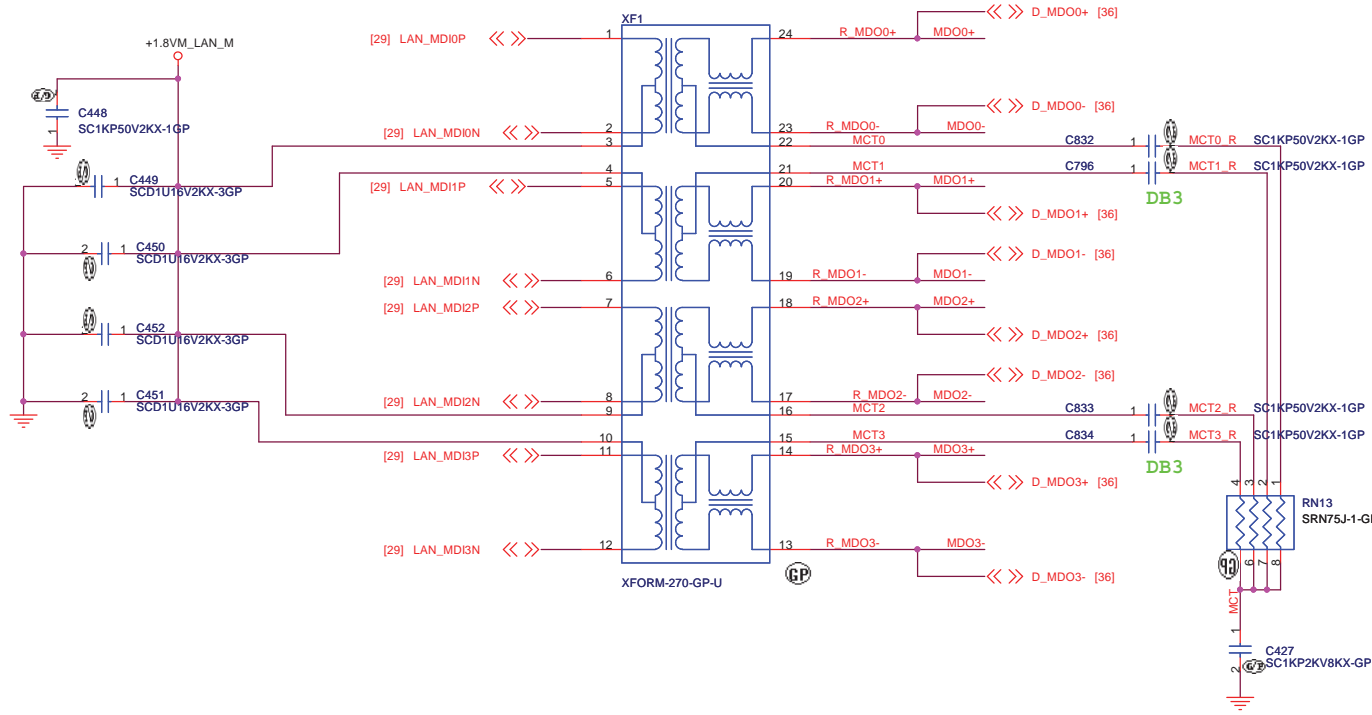
VOX

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

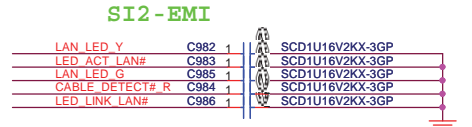
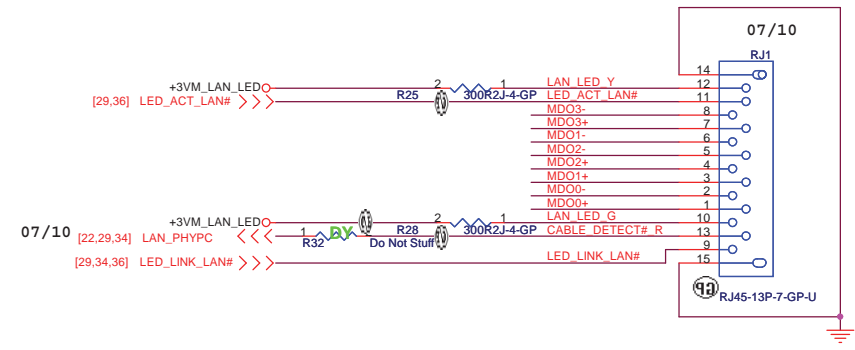
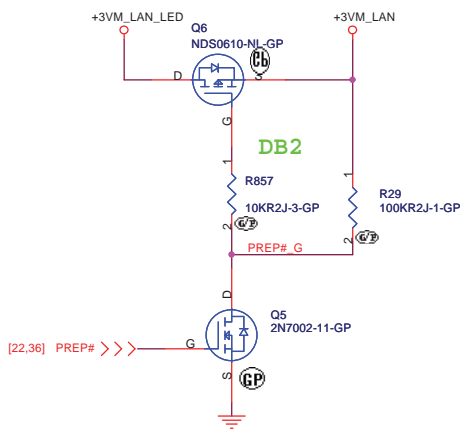
Title: **Intel 82567 Boaz**

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Date: Wednesday, August 20, 2008	Sheet 29	of 53

Note : MDO[3..0]+ signals should route to RJ45 first then to DOCK CONN .



LAN ENERGY DET



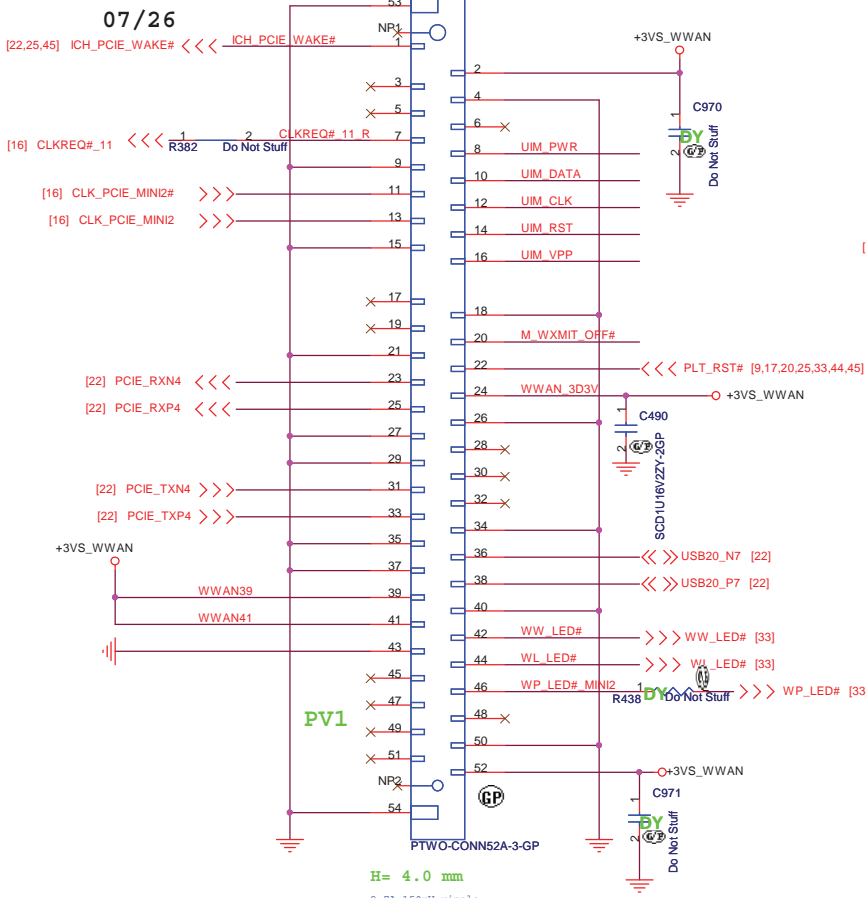
VOX

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.

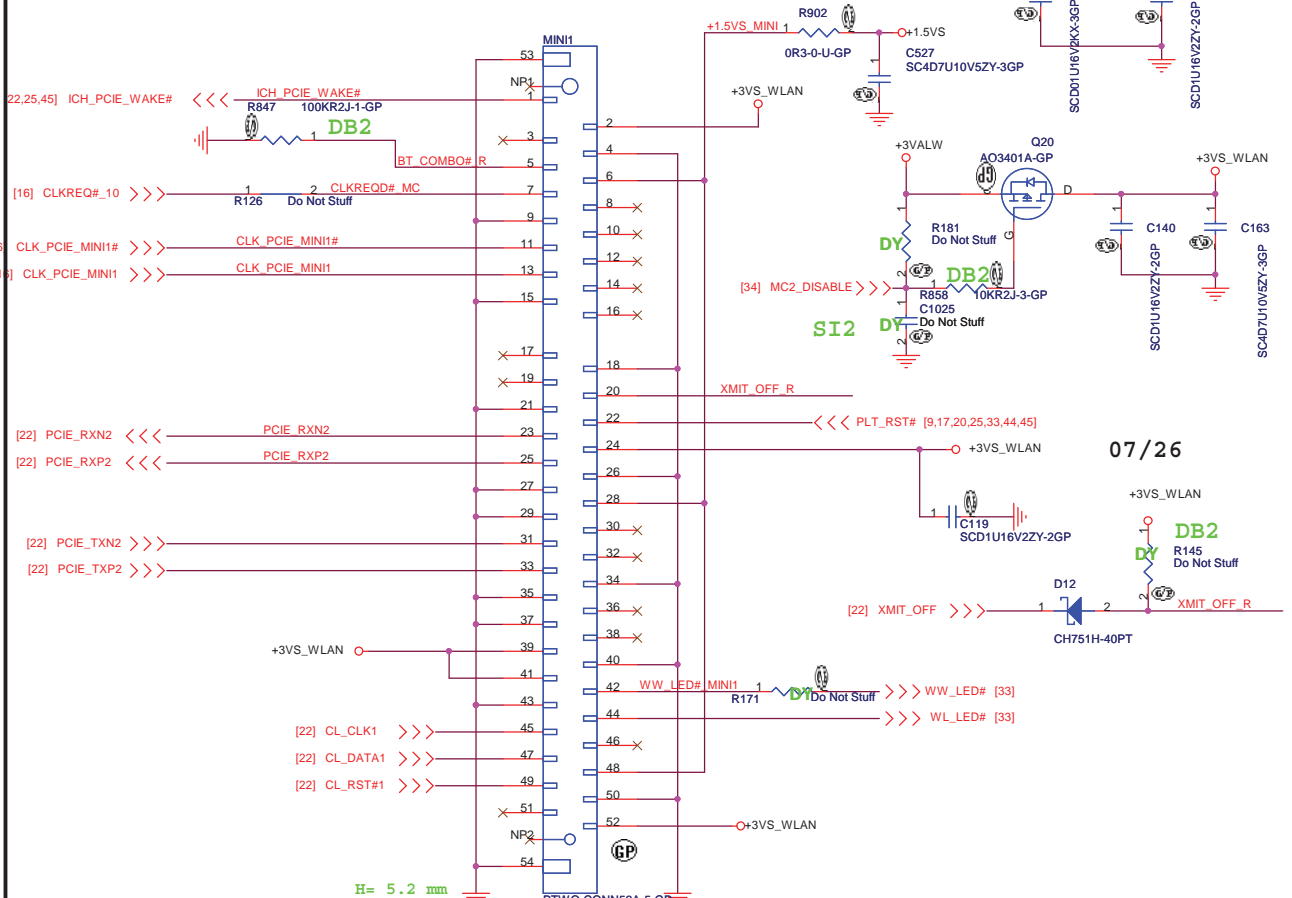
Title: **Magnetic & RJ45**

Size A3	Document Number	Rev 3
Date: Wednesday, August 20, 2008		Sheet 30 of 53

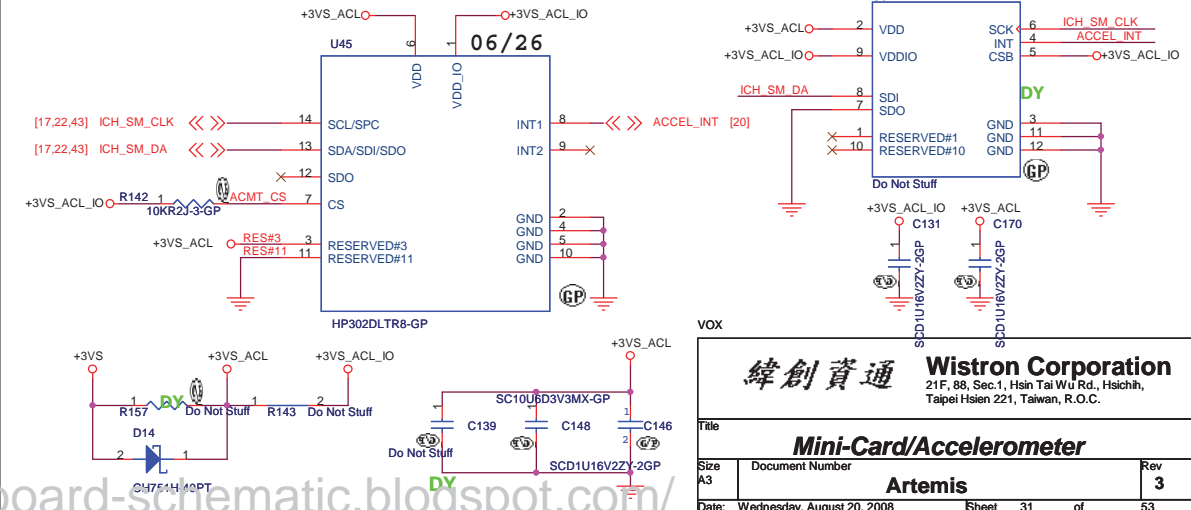
Mini-Card--WWAN BOTTOM



Mini-Card--WLAN TOP



ACCELEROMETER Must be placed in the center of the system



07/12

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.

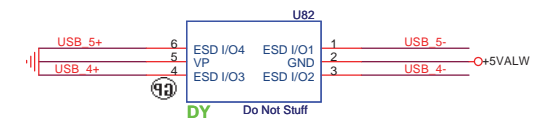
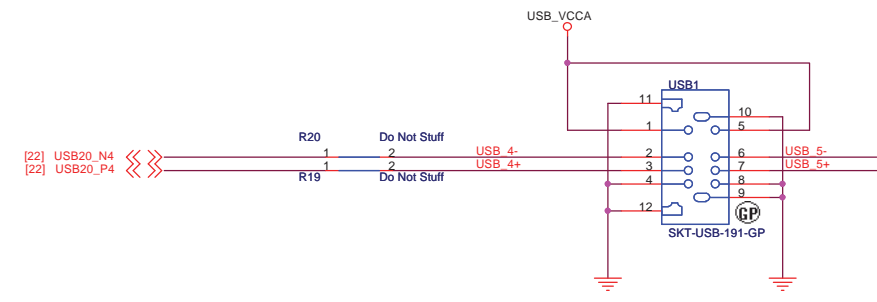
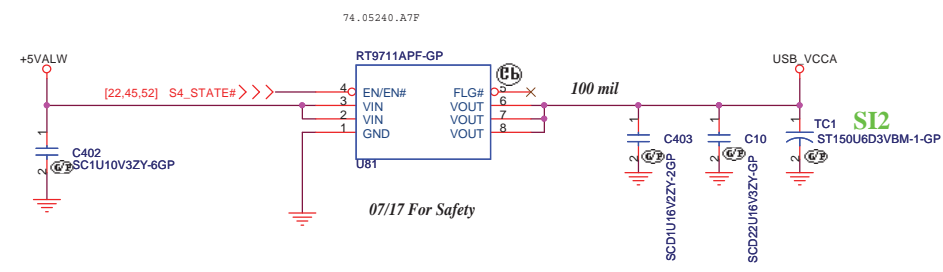
Mini-Card/Accelerometer

Artemis

Rev 3

Date: Wednesday, August 20, 2008 Sheet 31 of 53

74.02231.073-->74.00577.A73,74.05538.073
2462--G1224



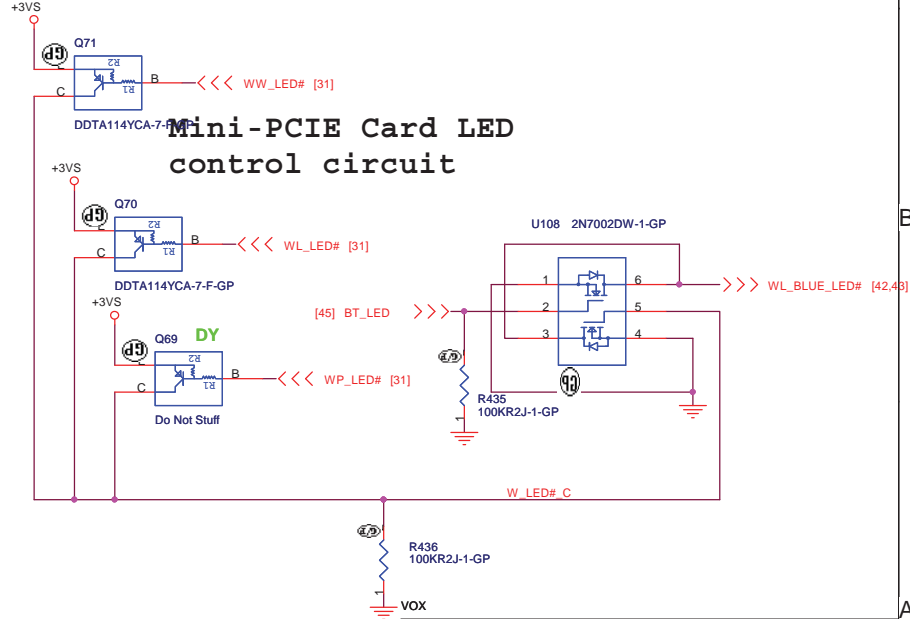
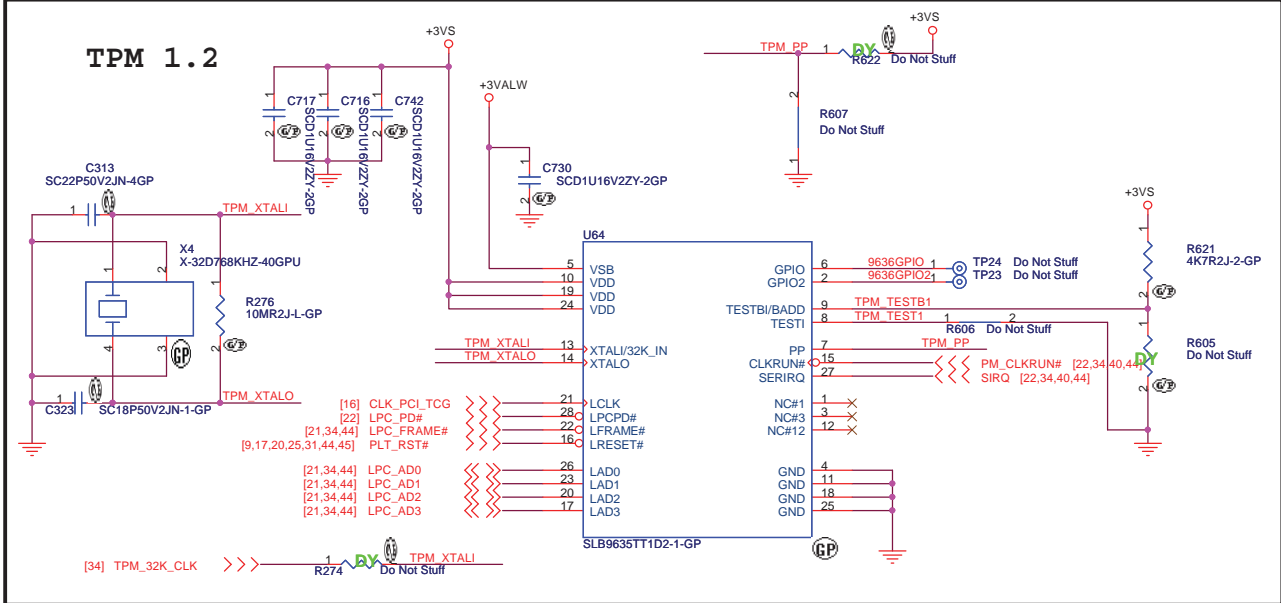
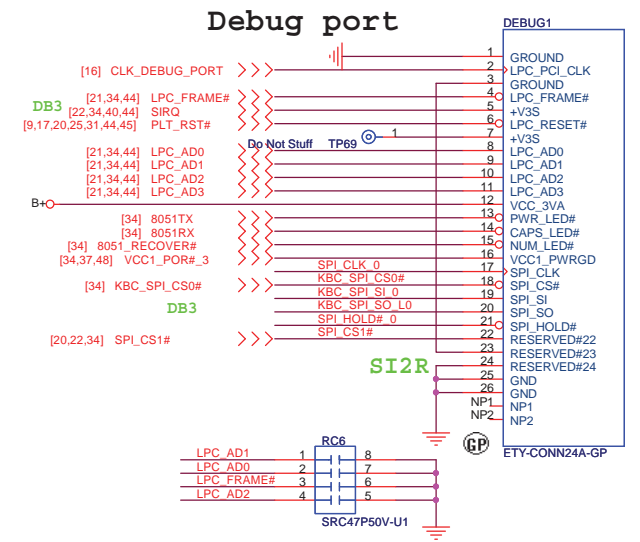
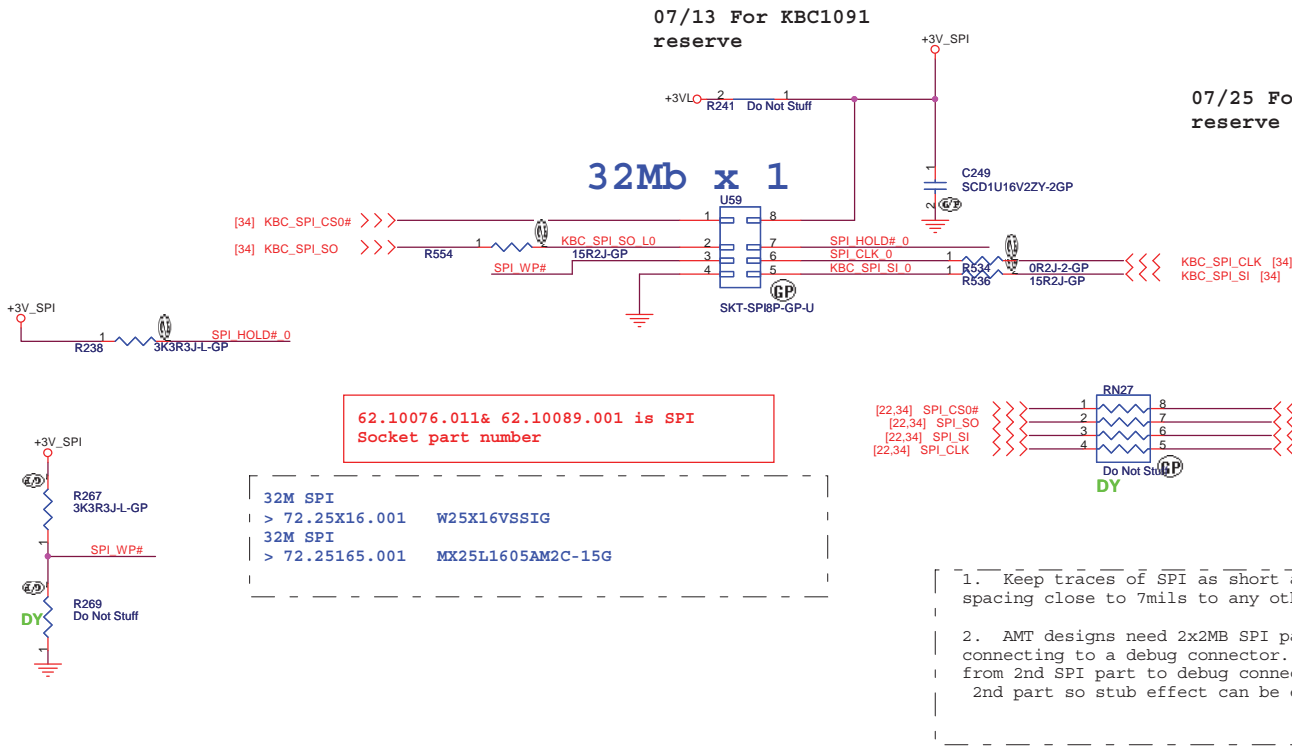
VOX

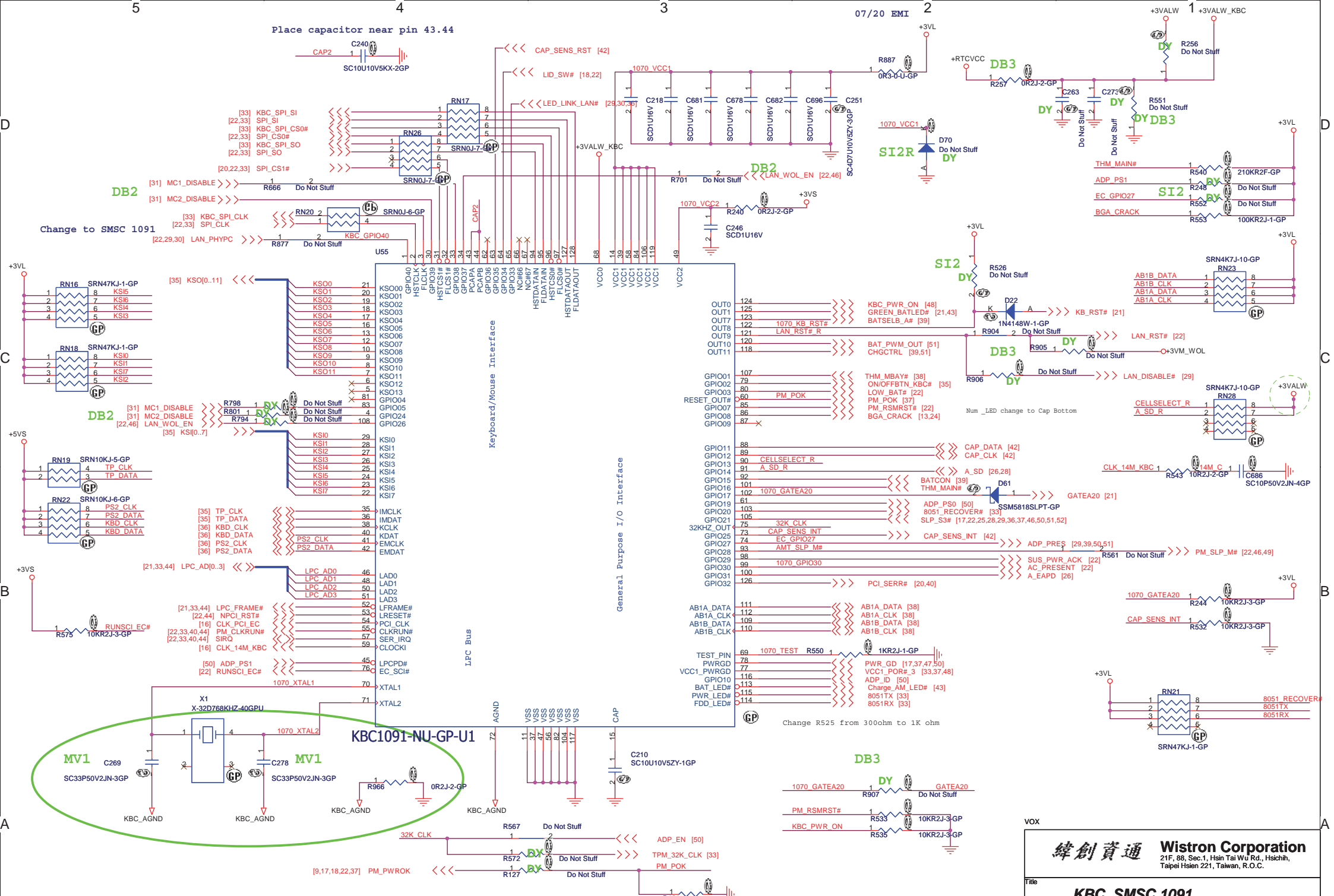
緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: **USB Connector**

Size A3 Document Number **Artemis** Rev **3**

Date: Wednesday, August 20, 2008 Sheet 32 of 53



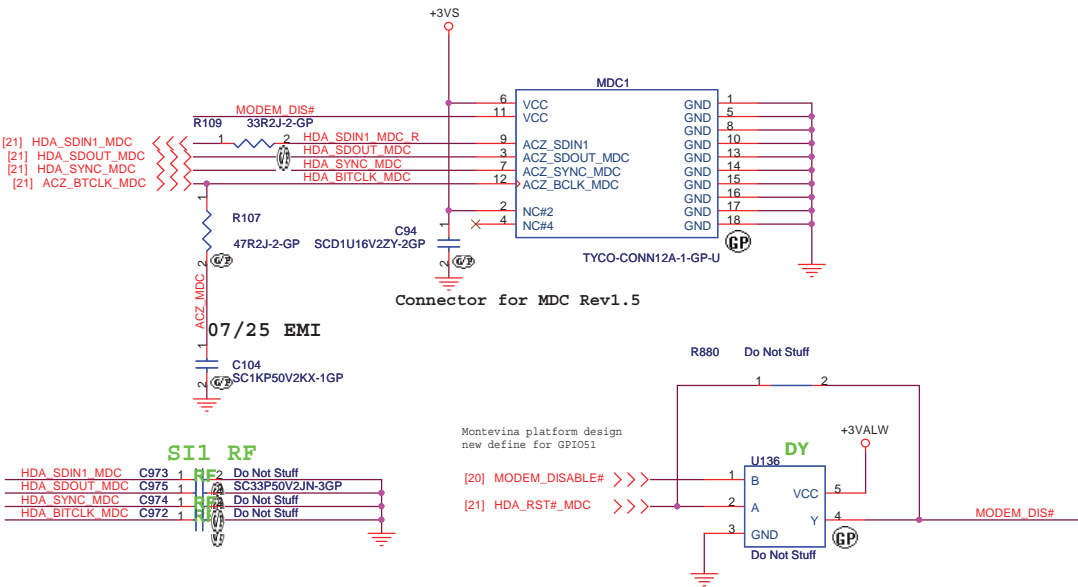


VOX

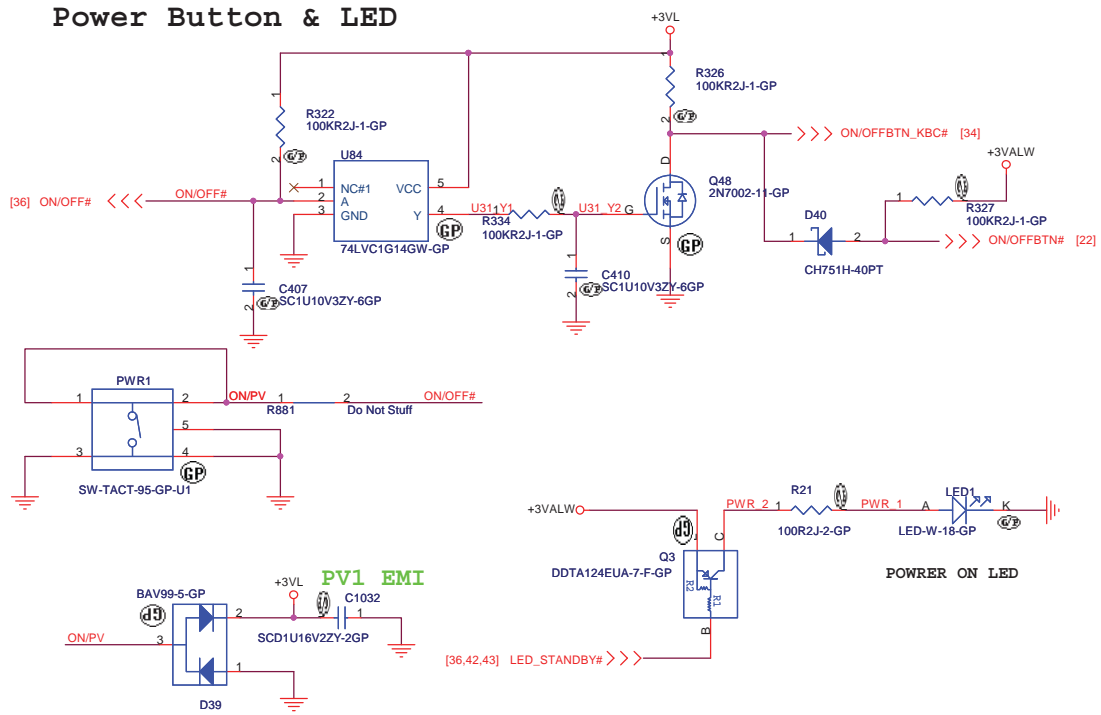
緯創資通 Wistron Corporation
 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.

Title		KBC SMSC 1091	
Size	A3	Document Number	
Date: Wednesday, August 20, 2008		Sheet 34 of 53	
Artemis		Rev 3	

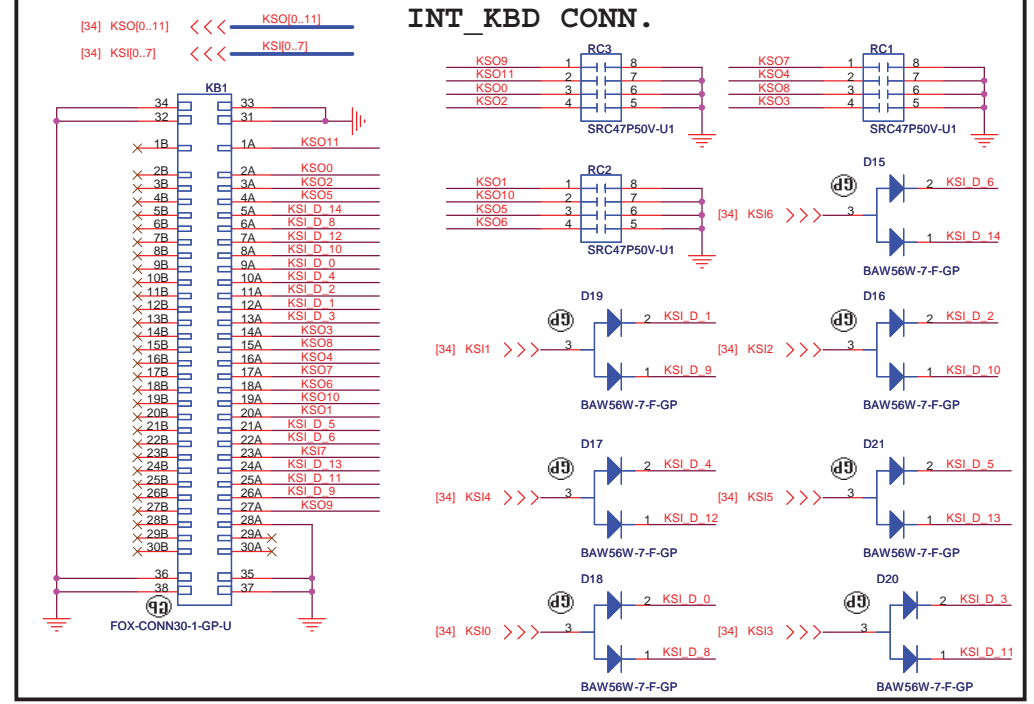
MDC 1.5 Conn.



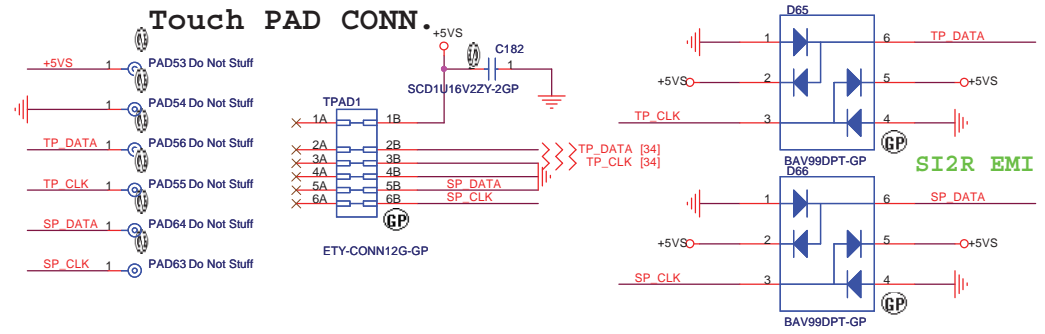
Power Button & LED



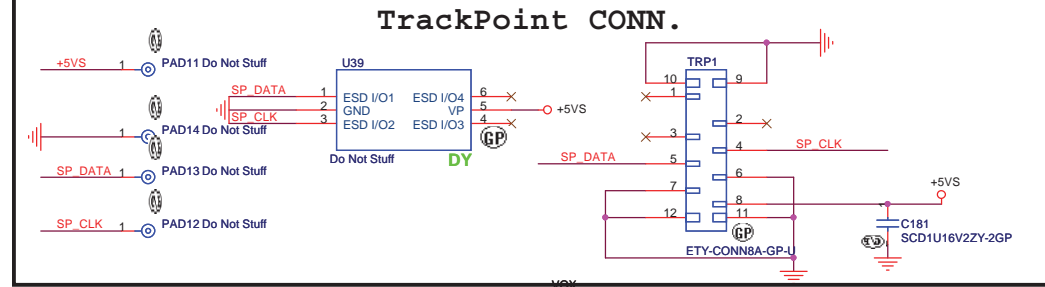
INT_KBD CONN.



Touch PAD CONN.



TrackPoint CONN.



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21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.

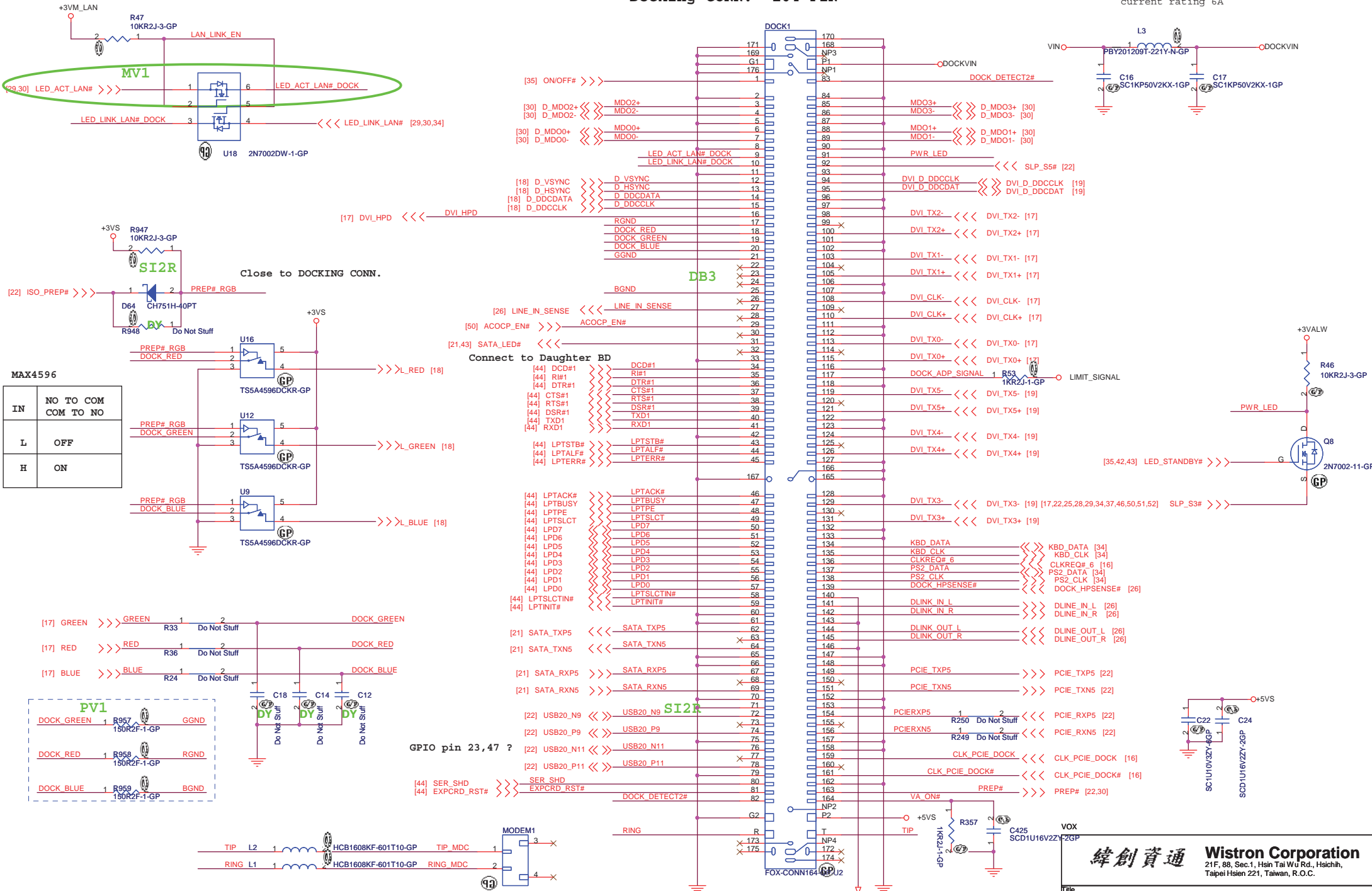
Title: **MDC/KBD/ON OFF/T.P.**

Size A3 Document Number: **Artemis** Rev **3**

Date: Wednesday, August 20, 2008 Sheet 35 of 53

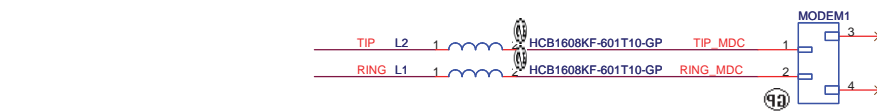
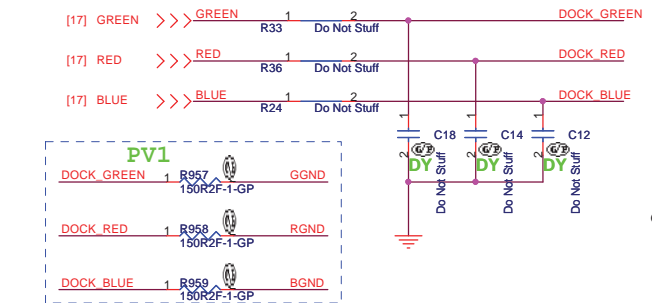
Docking CONN. 164 PIN

current rating 6A



MAX4596

IN	NO TO COM COM TO NO
L	OFF
H	ON

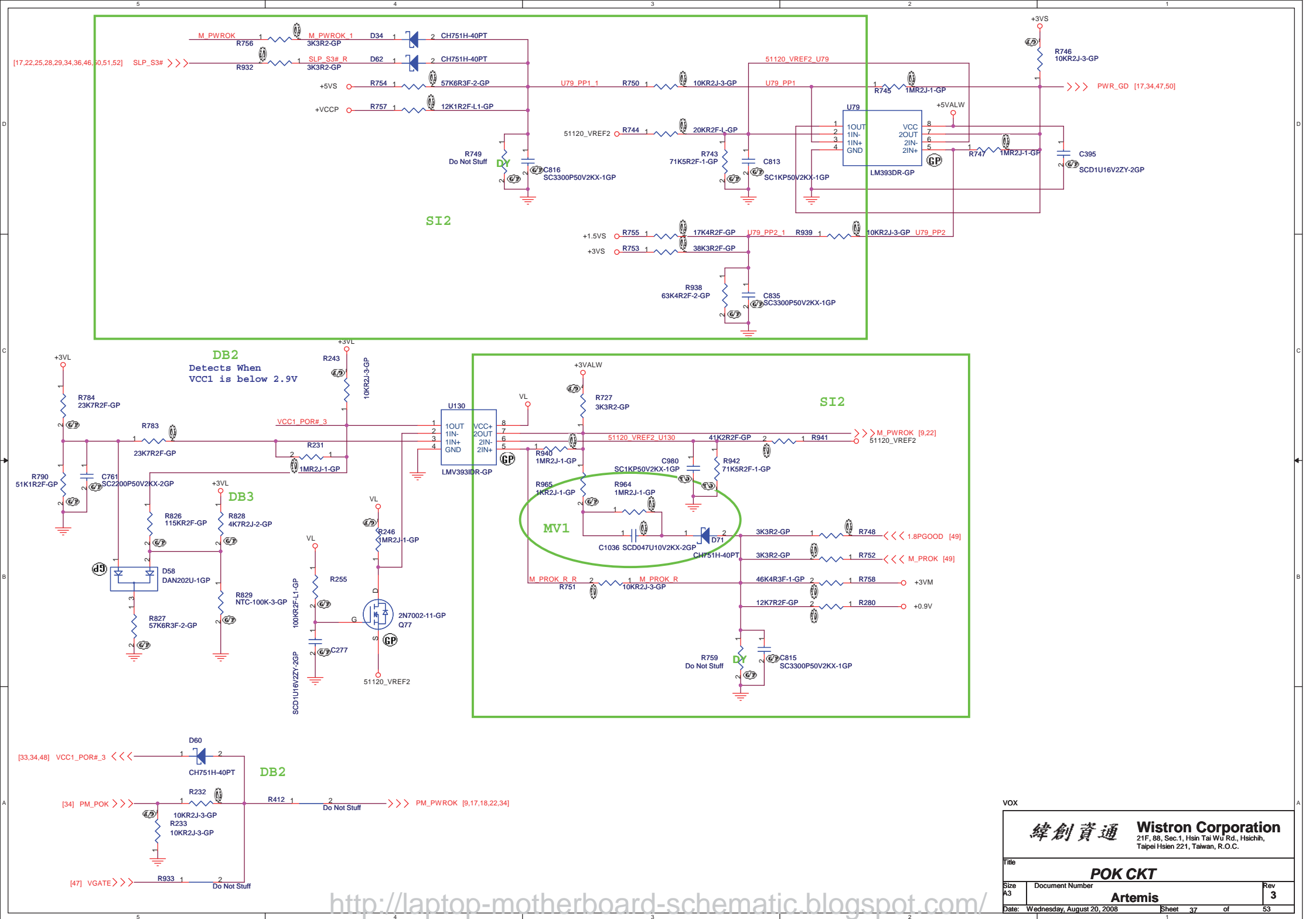


Layout Notes :
Place MODEM1 & BEAD near Docking connector

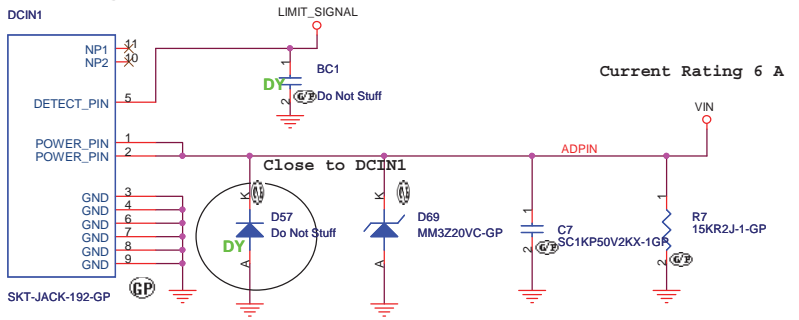
For TIP and Ring cut all layers

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

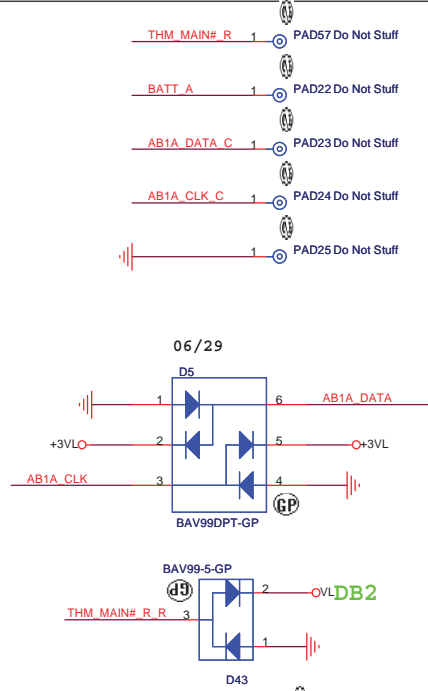
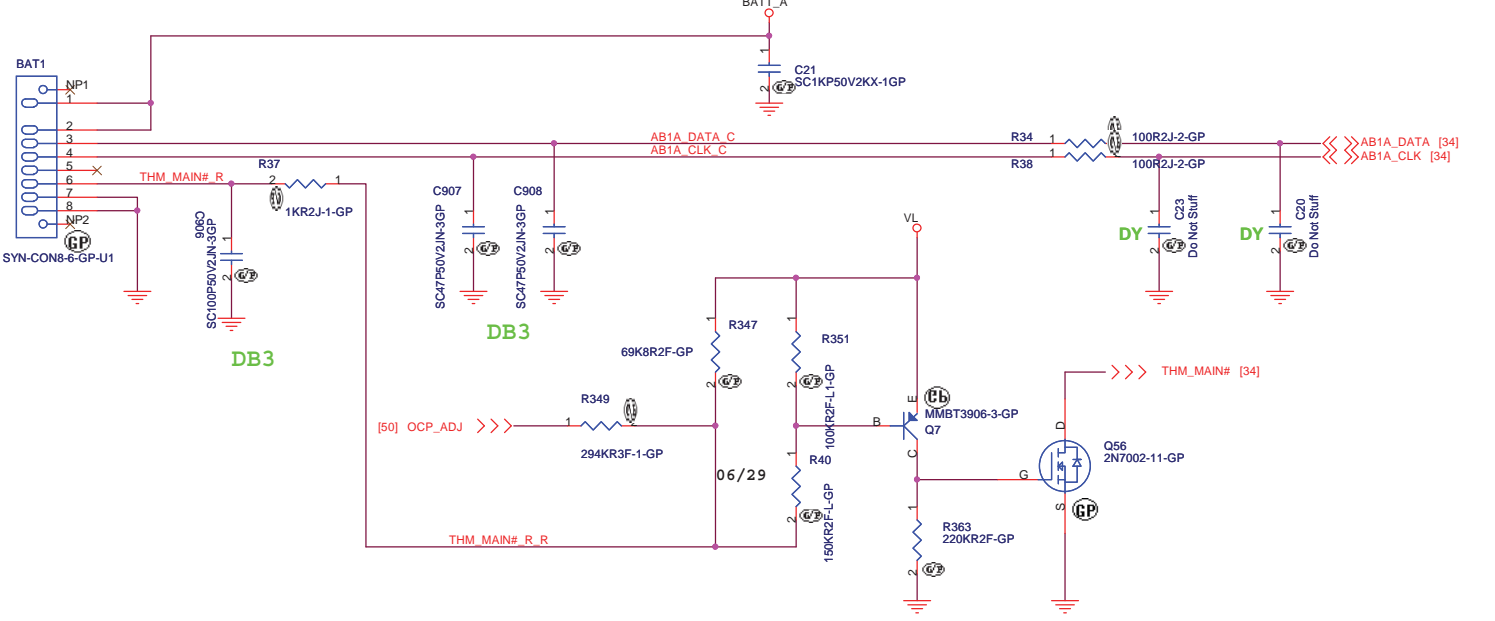
Title Docking CONN		
Size A3	Document Number Artemis	Rev 3
Date: Wednesday, August 20, 2008	Sheet 36	of 53



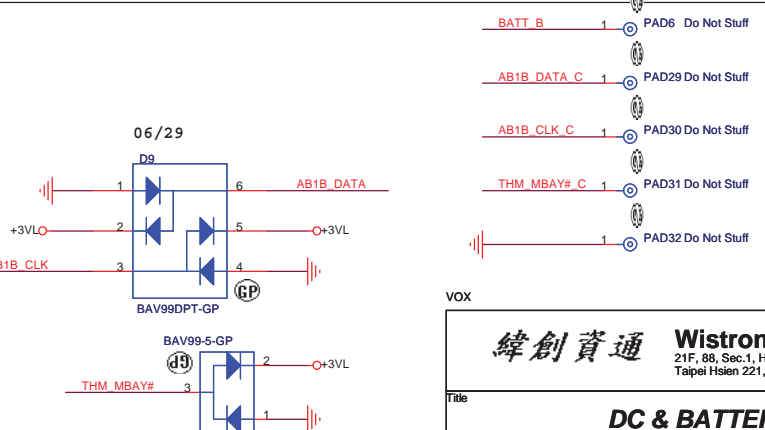
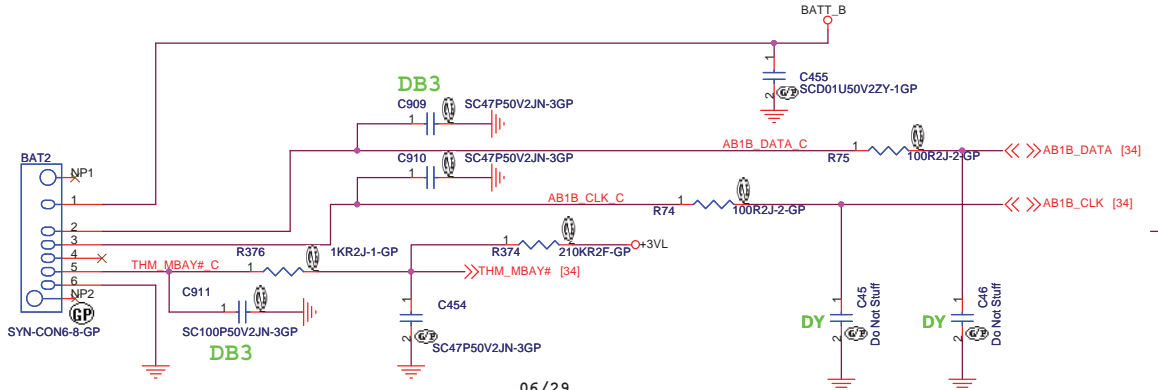
Adaptor in to generate DCBATTOUT



MAIN BATTERY CONNECTOR



BAY BATTERY CONNECTOR



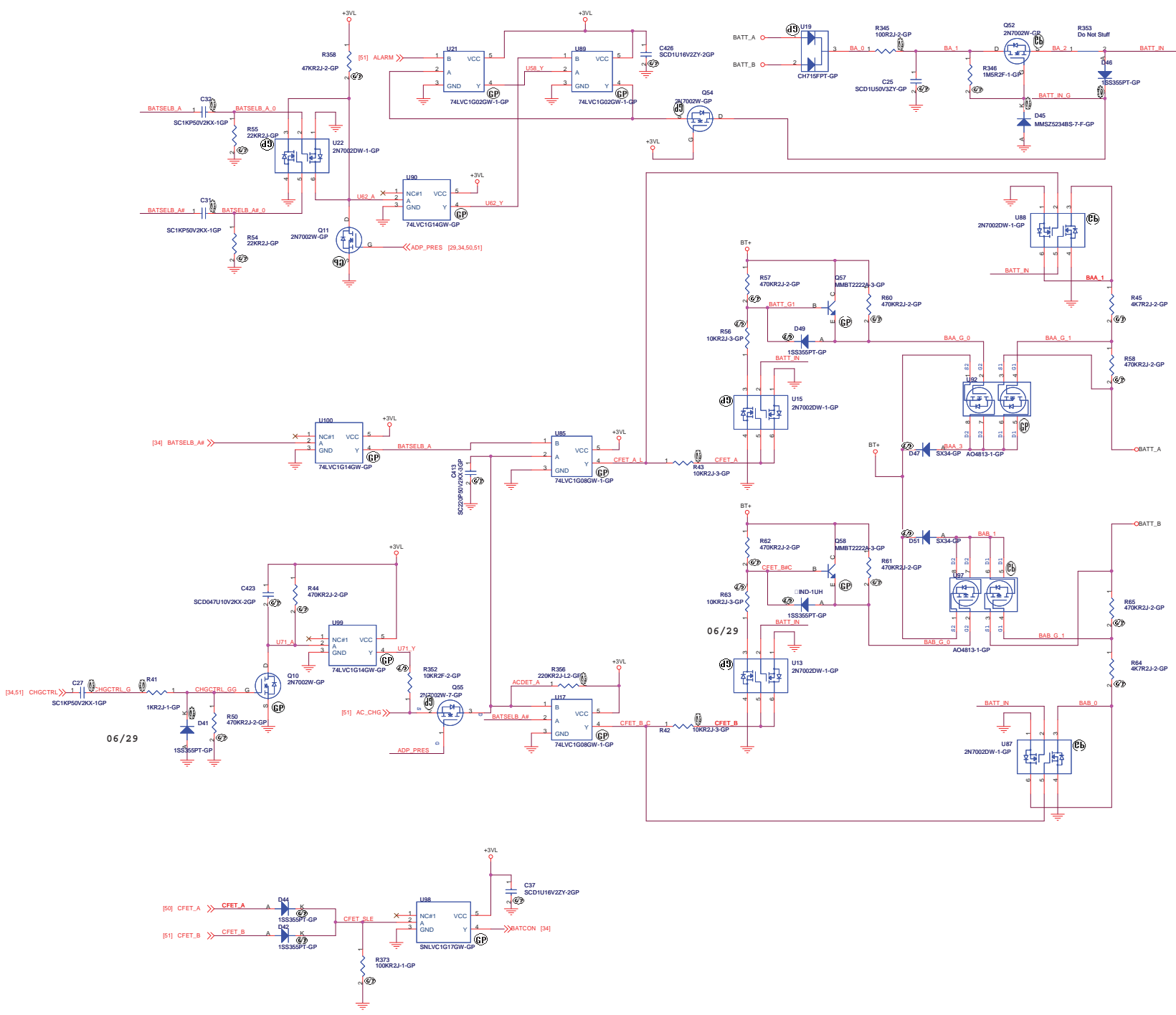
VOX

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.

Title: **DC & BATTERY CONN.**

Size A3 Document Number **Artemis** Rev **3**

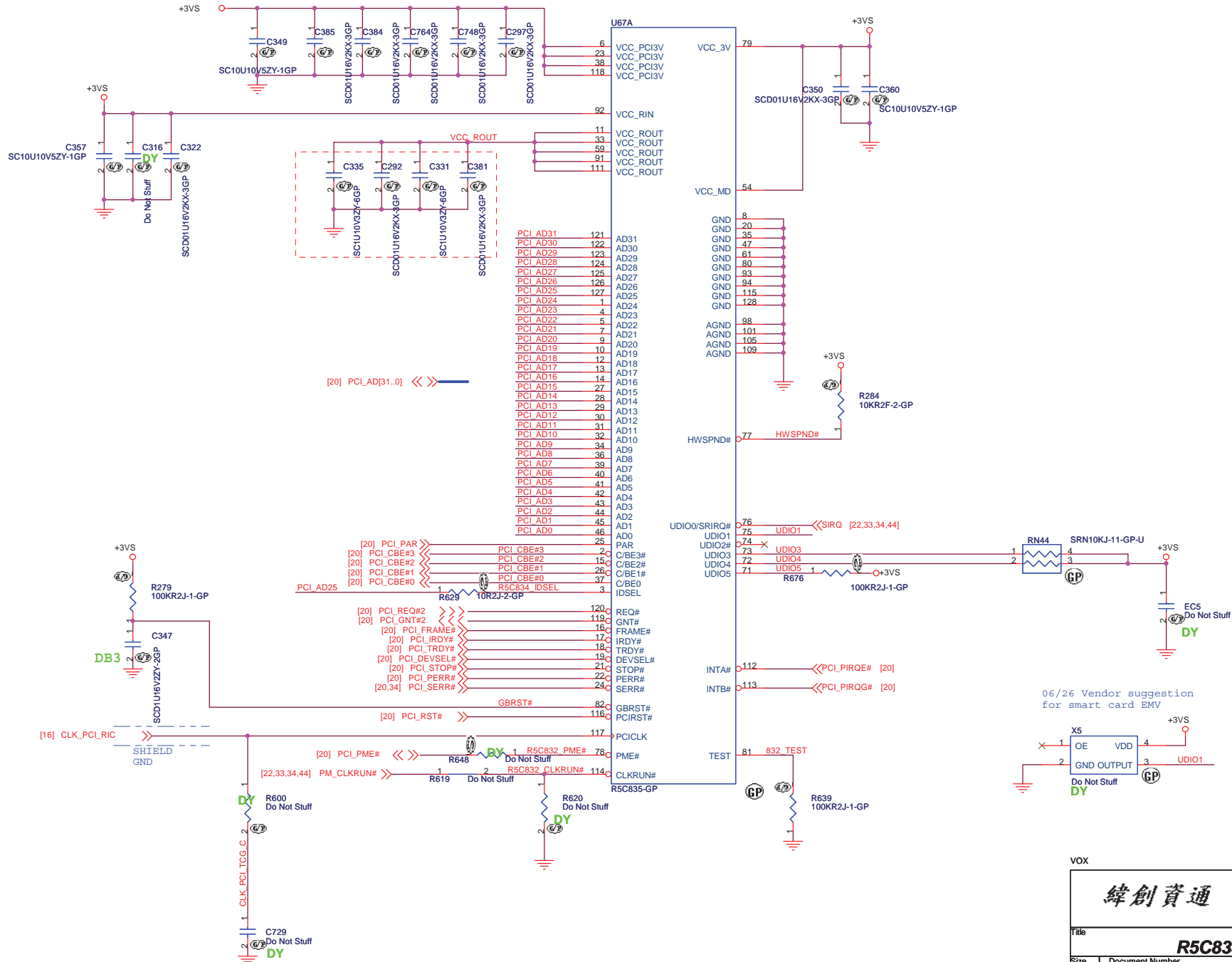
Date: Wednesday, August 20, 2008 Sheet 38 of 53



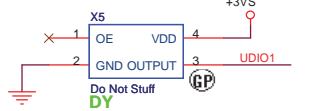
<http://laptop-motherboard-schematic.blogspot.com/>

VOX	
緯創資通 Wistron Corporation	
21F, 88, Sec. 1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
File	Battery Selector
Size A2	Artemis
Document Number	3
Date: Wednesday, August 24, 2006	Sheet 39 of 53

RICOH R5C835 (1 OF 2) PCI



06/26 Vendor suggestion for smart card EMV

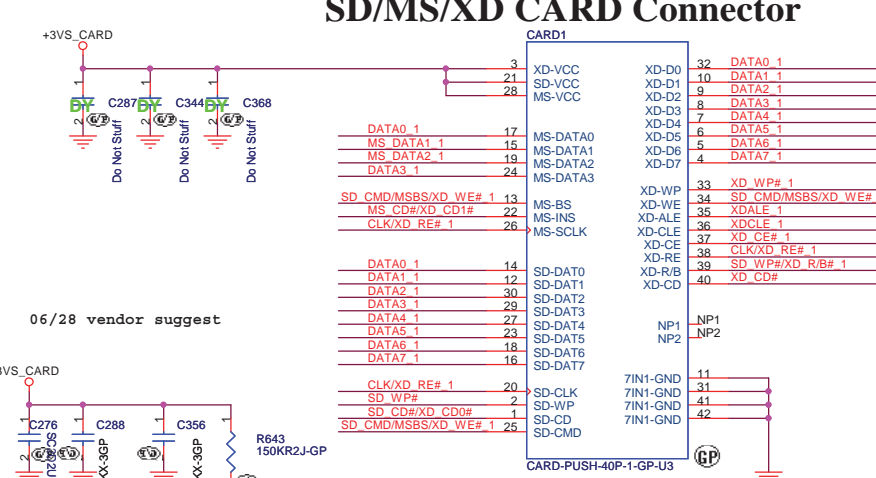
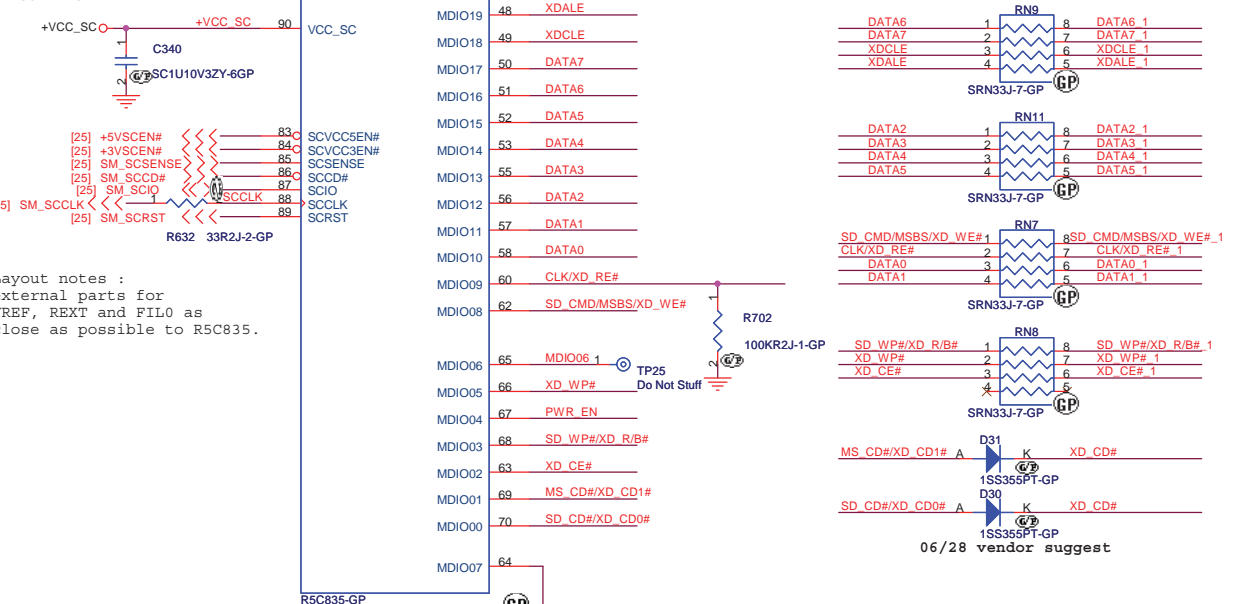
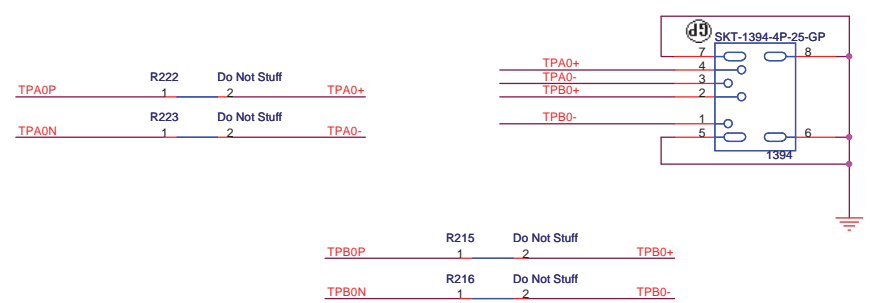
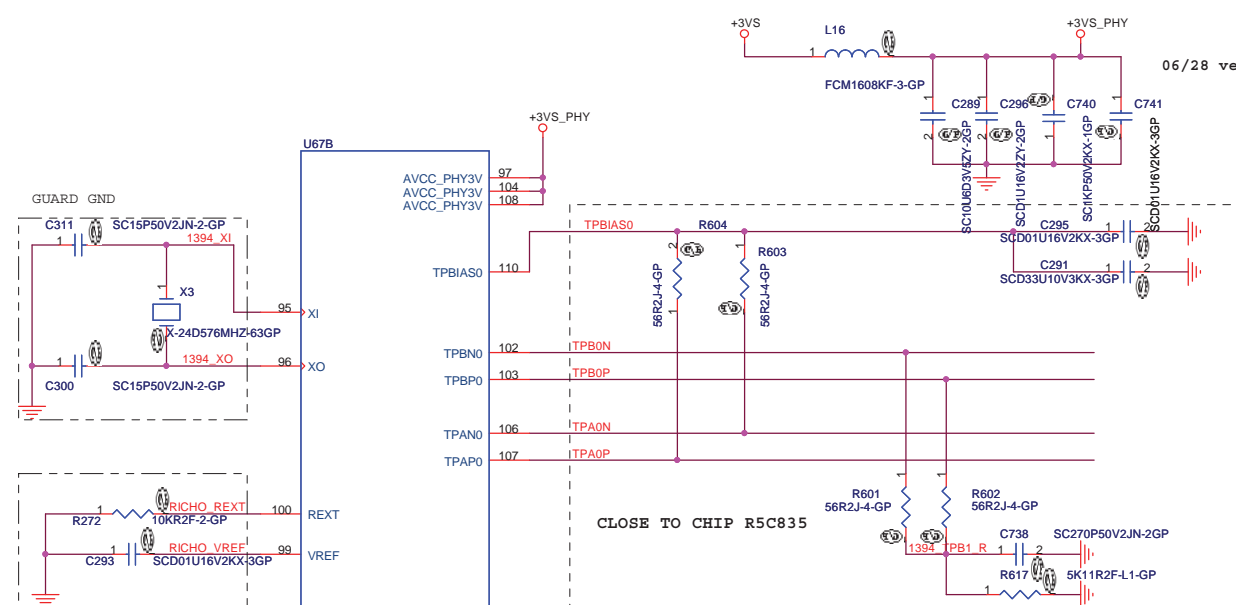


緯創資通 Wistron Corporation	
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title R5C835/PCI	
Size A3	Document Number Artemis
Date: Wednesday, August 20, 2008	Sheet 40 of 53
	Rev 3

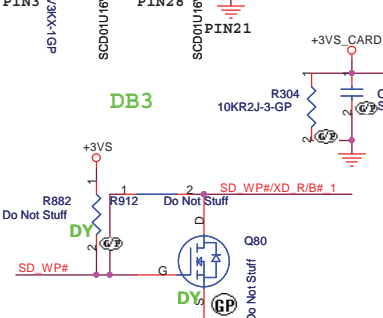
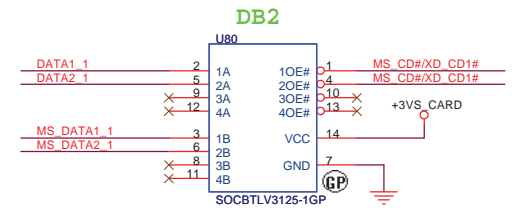
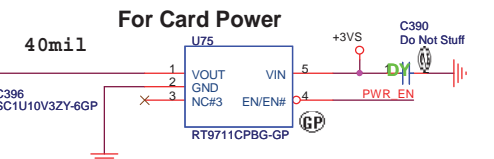
RICOH R5C835 (2 OF 2)

Layout notes :
1394

-----GND
-----TPB0-
-----TPB0+
-----GND
-----TPA0-
-----TPA0+
-----GND



Layout notes :
external parts for
VREF, REXT and FIL0 as
close as possible to R5C835.

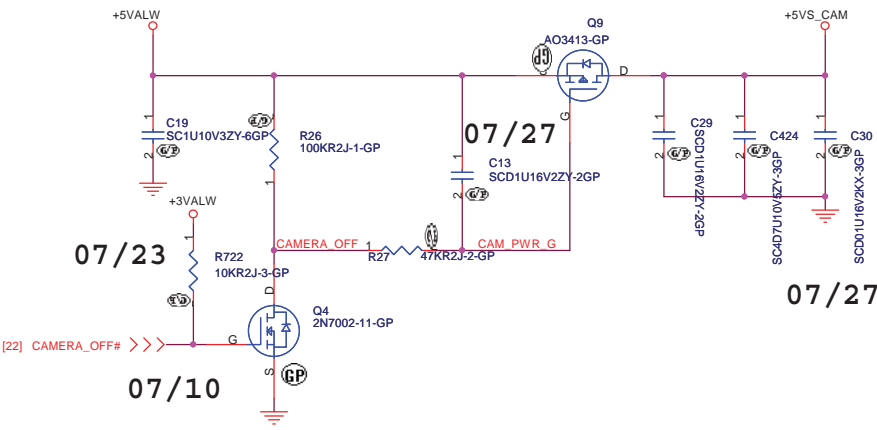


緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

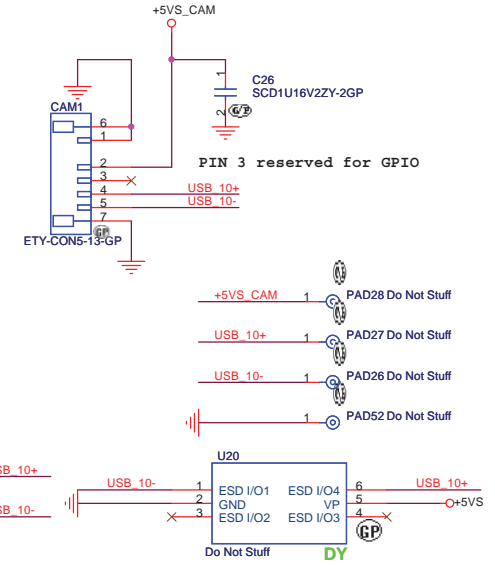
R5C835/1394/SD/Smart

File	Document Number	Rev
		3
Size	Artemis	
A3	Date: Wednesday, August 20, 2008	Sheet 41 of 53

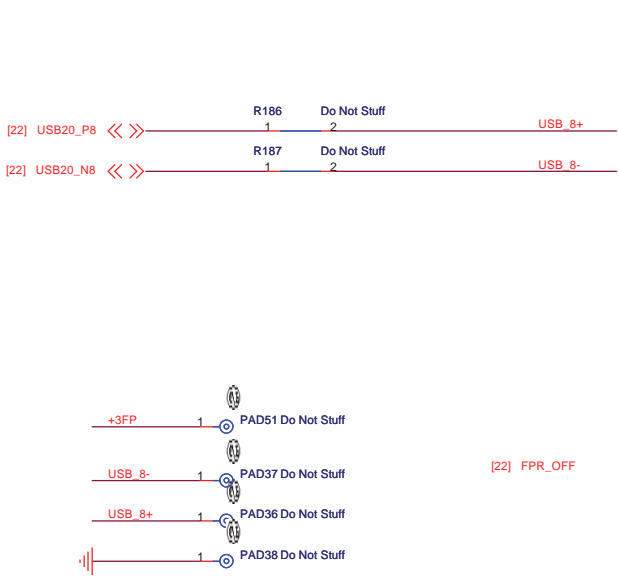
CAMERA



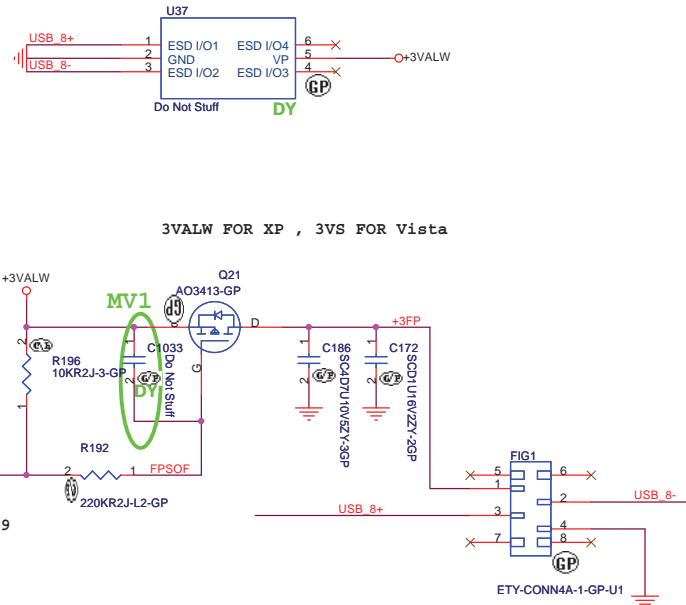
CAMERA Conn.



FingerPrint



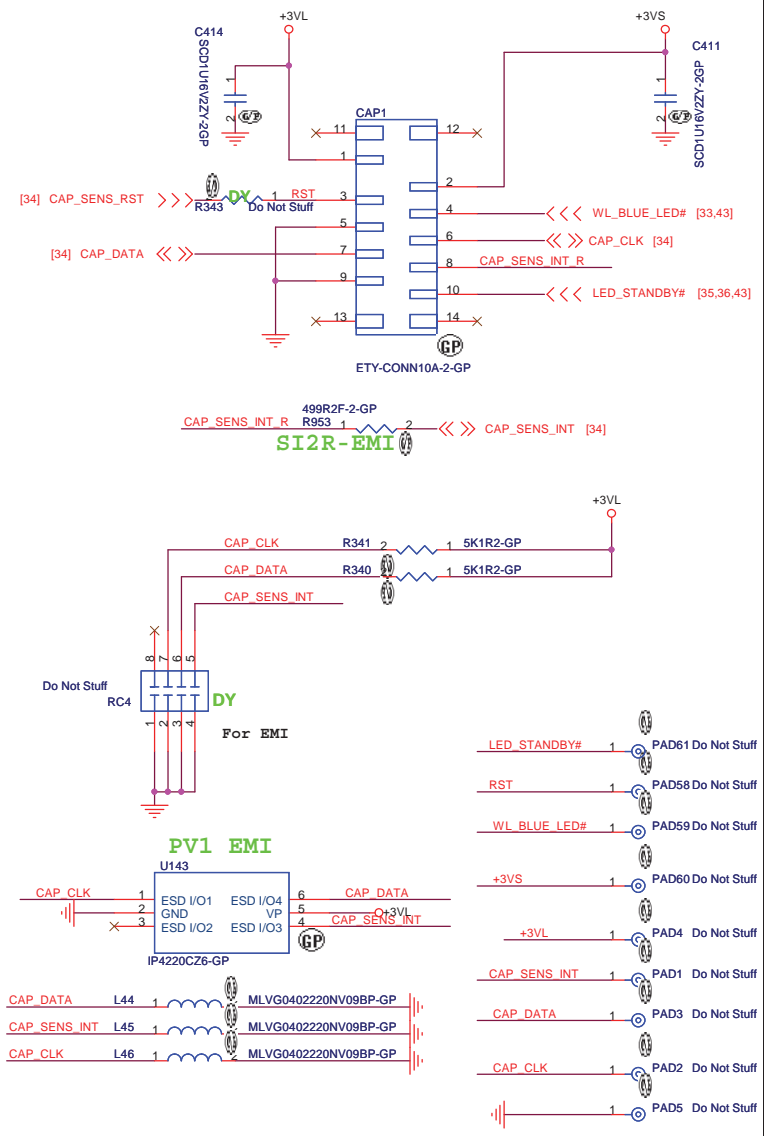
FingerPrint Conn.



SYSTEM CAPACITY BOARD

Vol up , Vol down , Mute , Presentation

PIN 3 reserved for GPIO



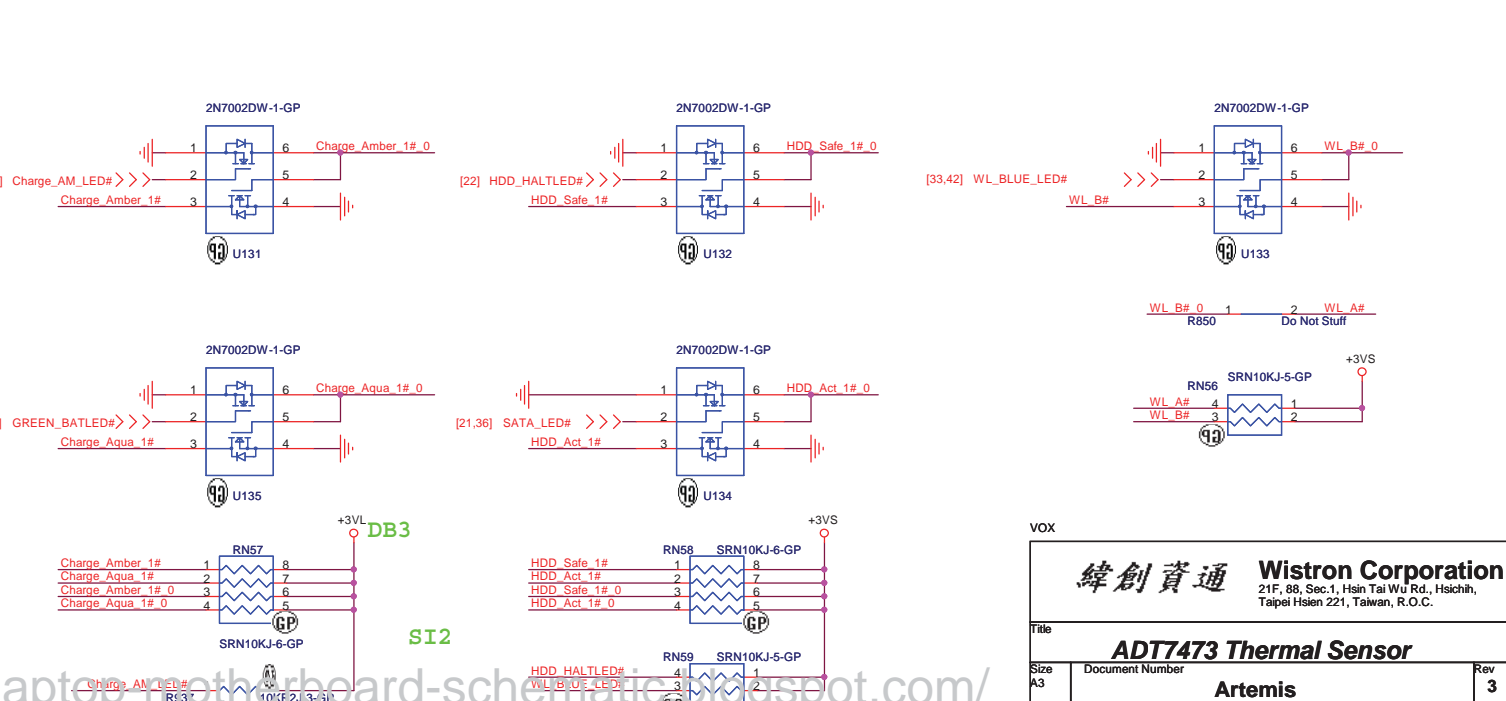
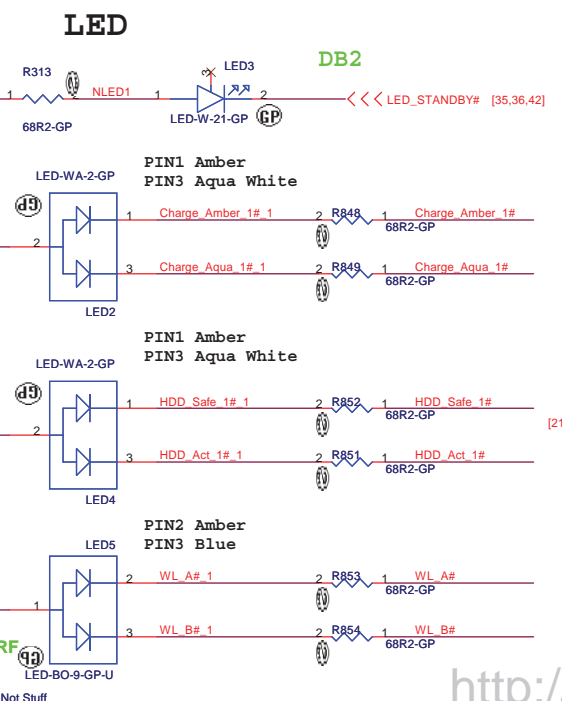
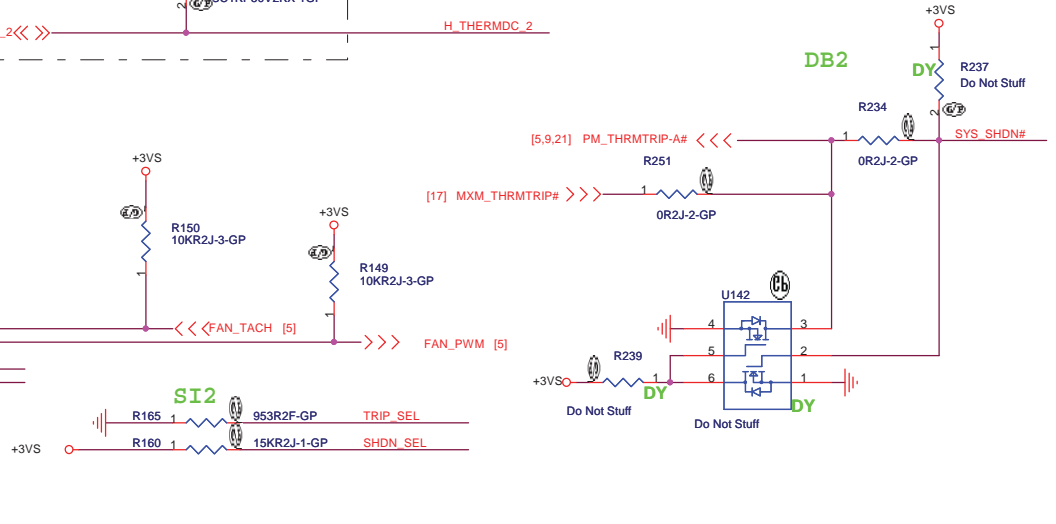
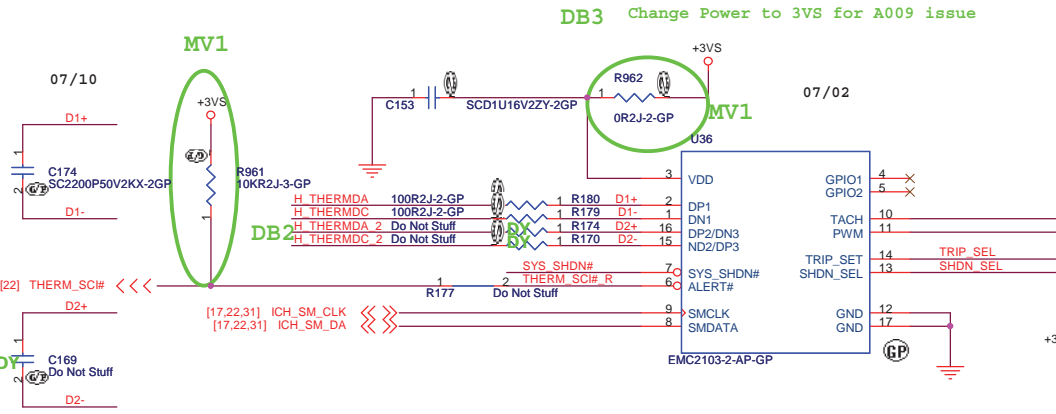
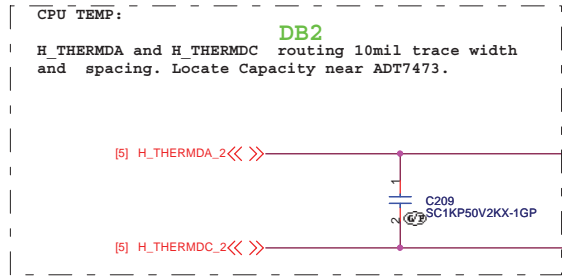
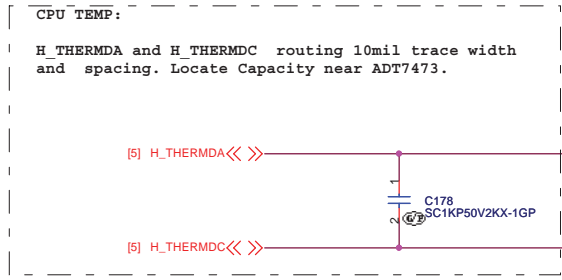
VOX

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.

Title: **Camera/W-COM**

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Thermal Sensor



VOX

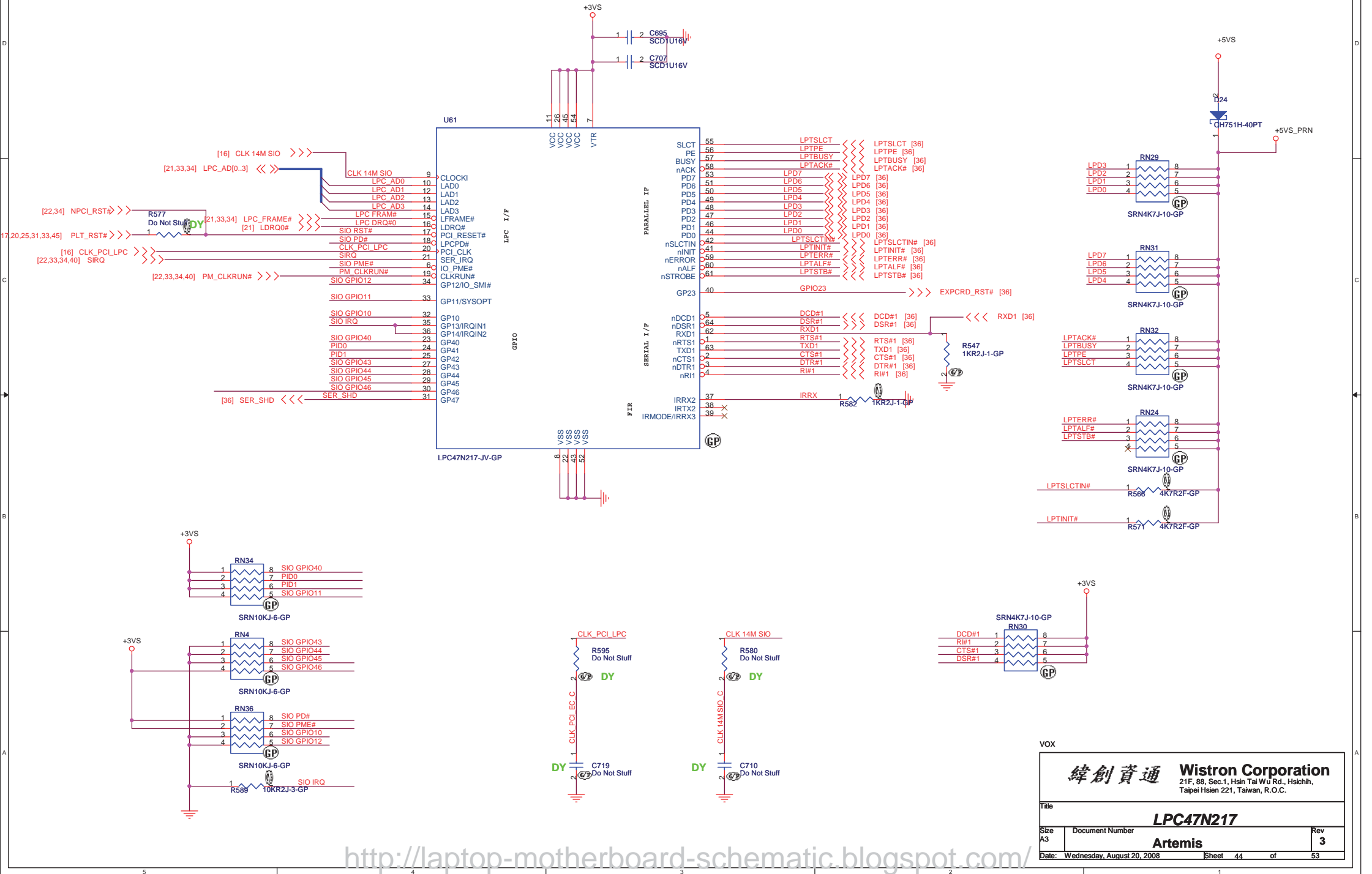
緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.

Title: **ADT7473 Thermal Sensor**

Size A3 Document Number **Artemis** Rev **3**

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SIO



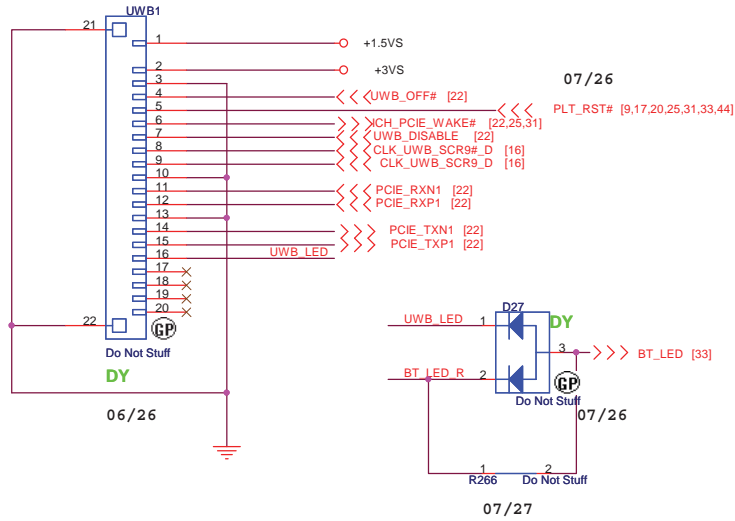
VOX

緯創資通 Wistron Corporation
 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
 Taipei Hsien 221, Taiwan, R.O.C.

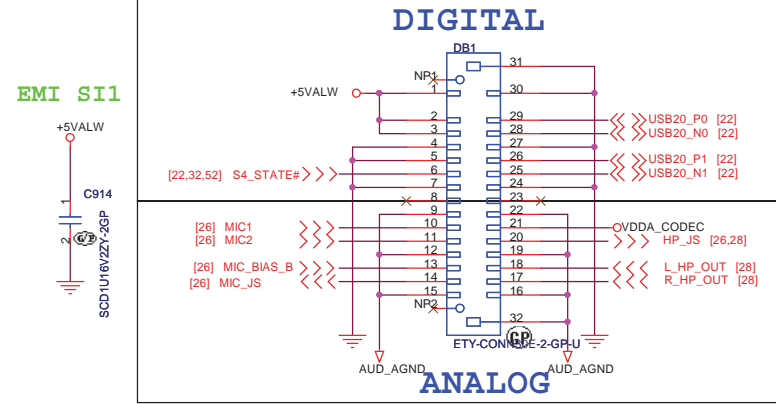
Title: **LPC47N217**

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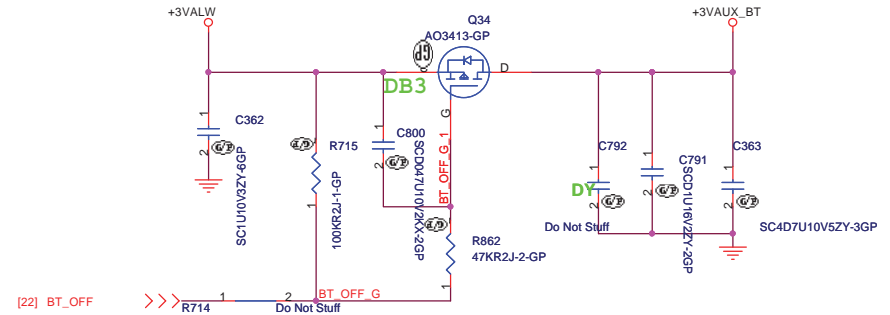
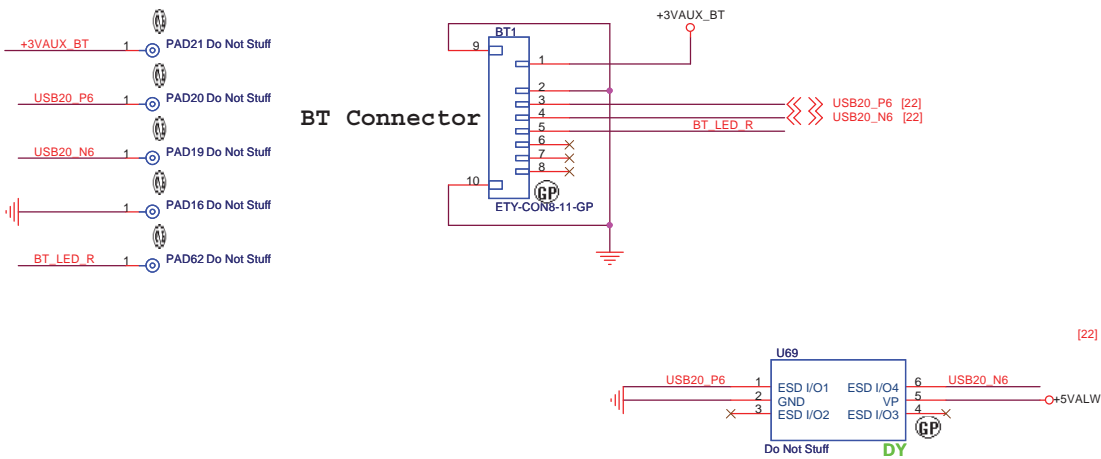
UWB Connector



AUDIO Daughter Board Connector



Bluetooth Connector



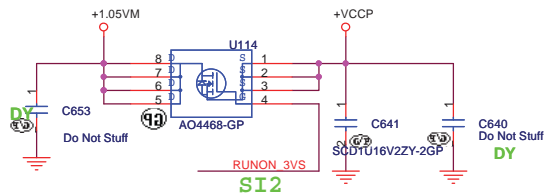
VOX

緯創資通 Wistron Corporation
 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
 Taipei Hsien 221, Taiwan, R.O.C.

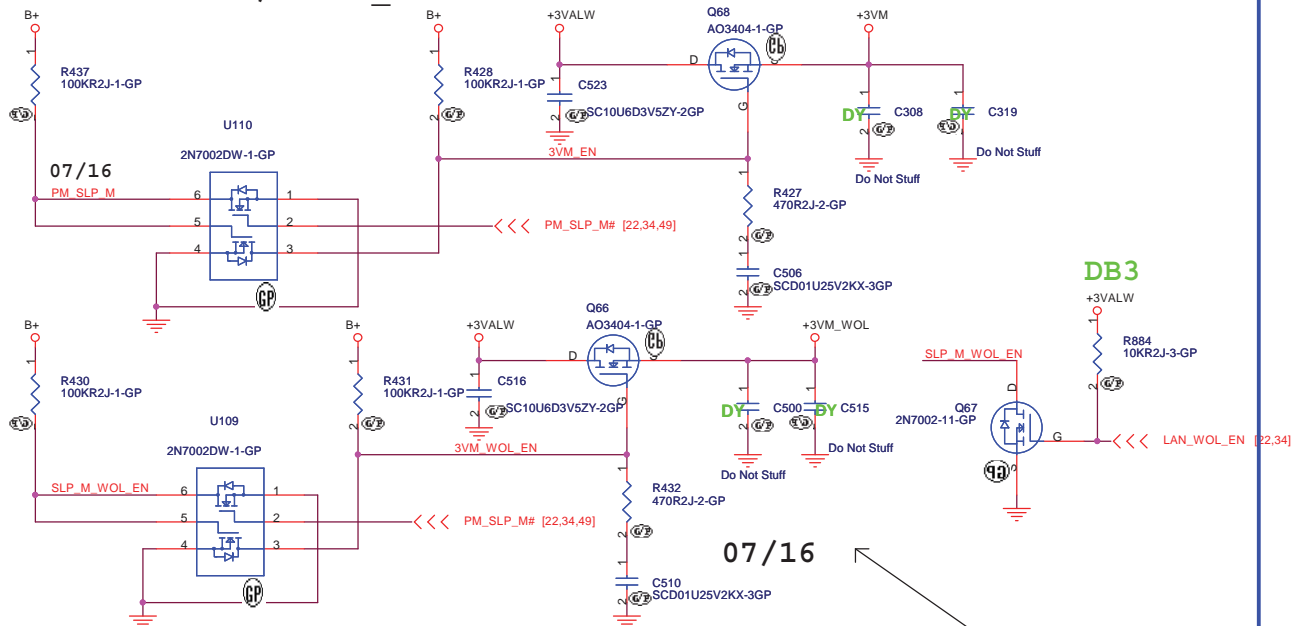
Title: **BT/UWB/Audio board Connector**

Size A3	Document Number	Rev 3
Date: Wednesday, August 20, 2008		Sheet 45 of 53

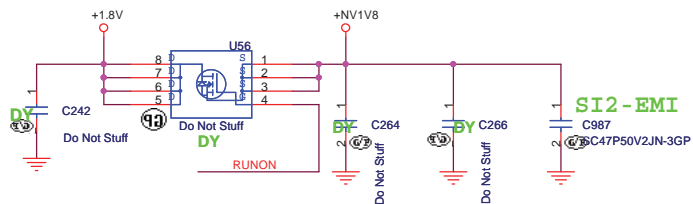
+1.05VM to +VCCP Transfer



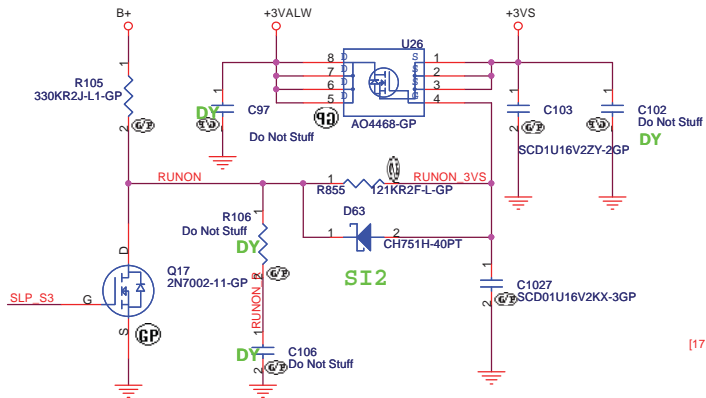
+3VALW to +3VM / +3VM_WOL Transfer



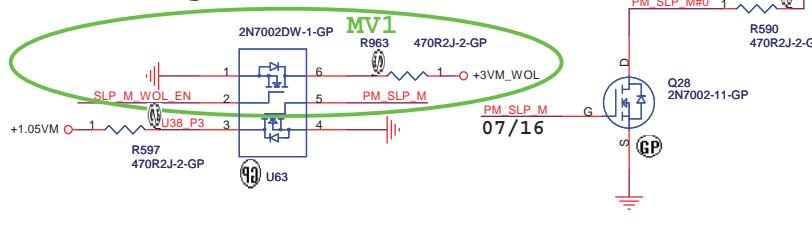
+1.8V to +1.8VS Transfer



+3VALW to +3VS Transfer

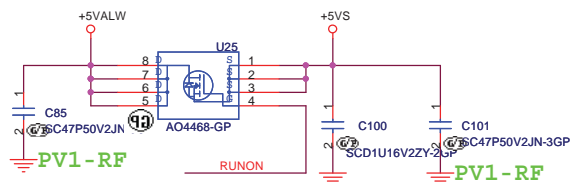


Discharge circuit-2 for V-M

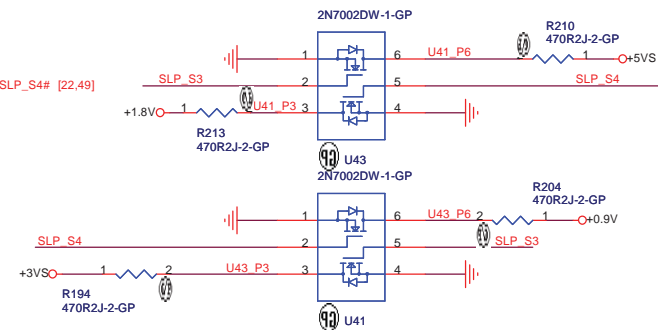
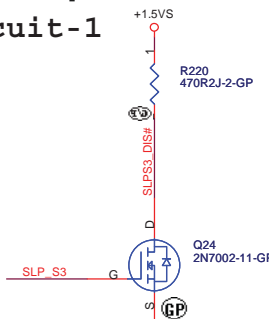


PM_SLP_M#	LAN_WOL_EN	+3VM_WOL	+3VM	SYSTEM STATE
0	0	0V	0V	MoIff / No WOL
0	1	3.3V	0V	Legacy WOL/ MoEff
1	0	3.3V	3.3V	M1
1	1	3.3V	3.3V	M1

+5VALW to +5VS Transfer



Discharge circuit-1

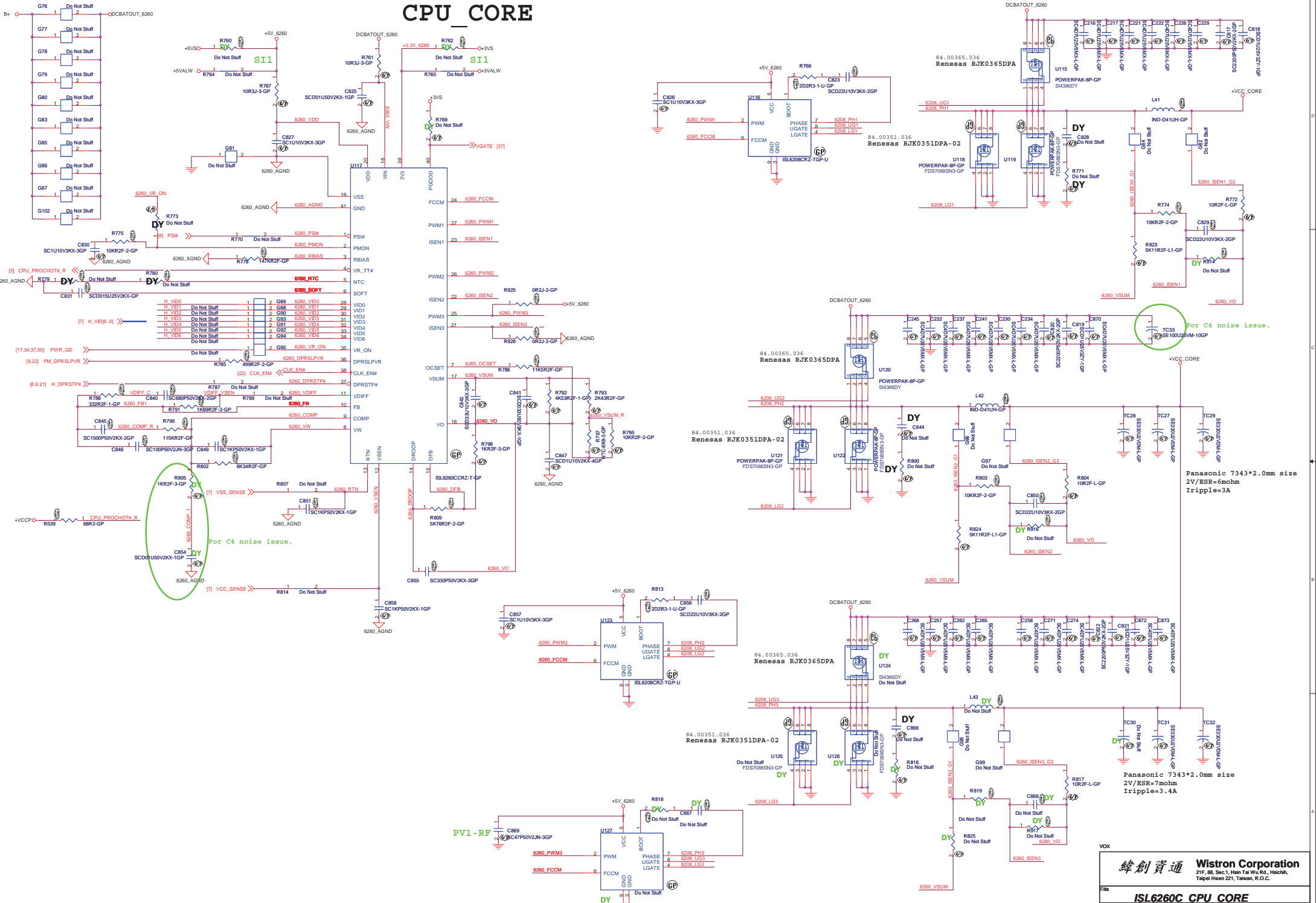


VOX

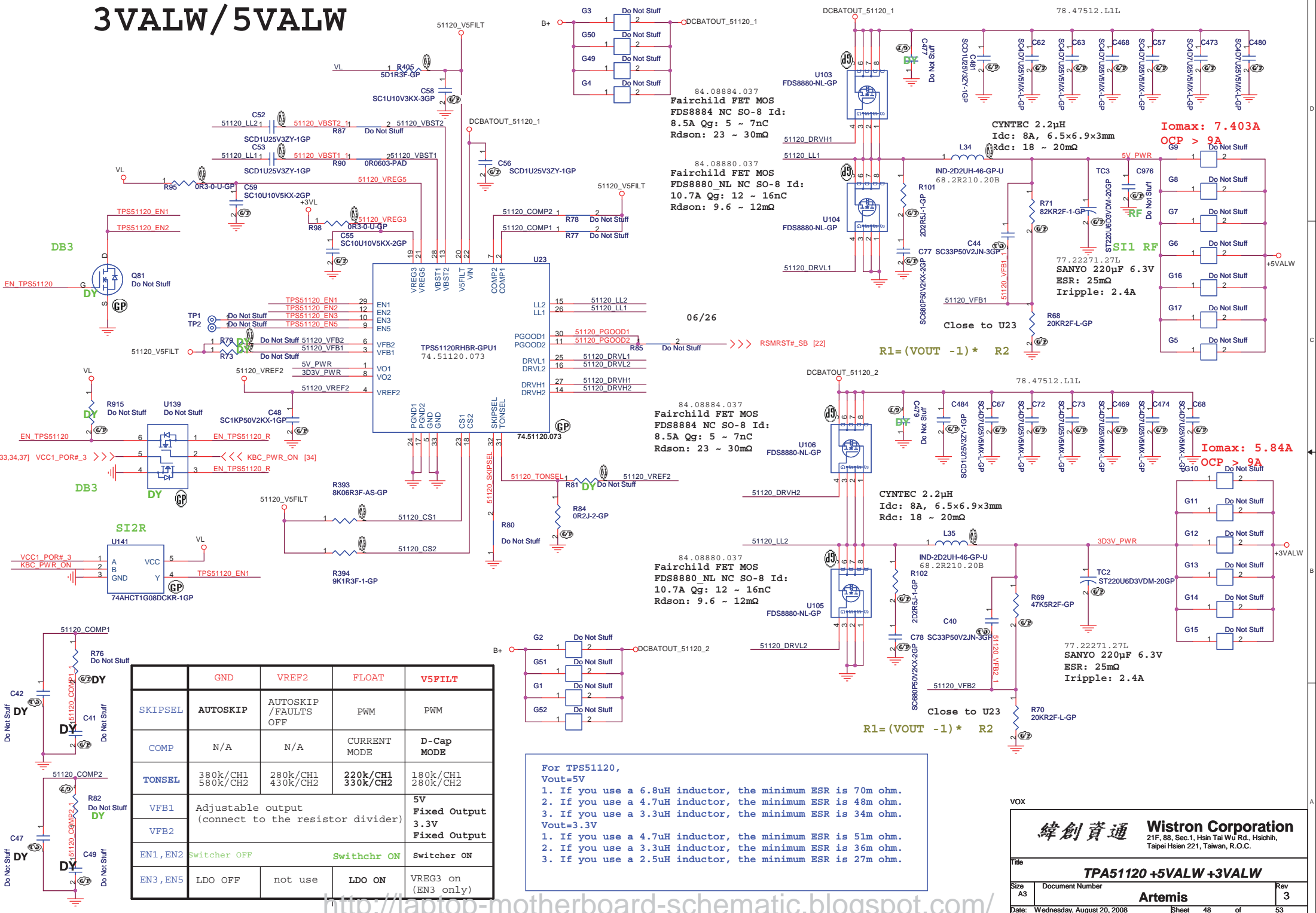
緯創資通 Wistron Corporation
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Title		
DC/DC Circuit		
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CPU_CORE



3VALW/5VALW



84.08884.037
Fairchild FET MOS
FDS8884 NC SO-8 Id:
8.5A Qg: 5 ~ 7nC
Rdson: 23 ~ 30mΩ

84.08880.037
Fairchild FET MOS
FDS8880 NL NC SO-8 Id:
10.7A Qg: 12 ~ 16nC
Rdson: 9.6 ~ 12mΩ

CYNTREC 2.2μH
Idc: 8A, 6.5×6.9×3mm
Rdc: 18 ~ 20mΩ

Iomax: 7.403A
OCP > 9A

77.22271.27L
SANYO 220μF 6.3V
ESR: 25mΩ
Iripple: 2.4A

Close to U23

$R1 = (VOUT - 1) * R2$

CYNTREC 2.2μH
Idc: 8A, 6.5×6.9×3mm
Rdc: 18 ~ 20mΩ

Iomax: 5.84A
OCP > 9A

77.22271.27L
SANYO 220μF 6.3V
ESR: 25mΩ
Iripple: 2.4A

Close to U23

$R1 = (VOUT - 1) * R2$

For TPS51120,
Vout=5V

1. If you use a 6.8uH inductor, the minimum ESR is 70m ohm.
2. If you use a 4.7uH inductor, the minimum ESR is 48m ohm.
3. If you use a 3.3uH inductor, the minimum ESR is 34m ohm.

Vout=3.3V

1. If you use a 4.7uH inductor, the minimum ESR is 51m ohm.
2. If you use a 3.3uH inductor, the minimum ESR is 36m ohm.
3. If you use a 2.5uH inductor, the minimum ESR is 27m ohm.

	GND	VREF2	FLOAT	V5FILT
SKIPSEL	AUTOSKIP	AUTOSKIP / FAULTS OFF	PWM	PWM
COMP	N/A	N/A	CURRENT MODE	D-Cap MODE
TONSEL	380k/CH1 580k/CH2	280k/CH1 430k/CH2	220k/CH1 330k/CH2	180k/CH1 280k/CH2
VFB1	Adjustable output (connect to the resistor divider)			5V Fixed Output 3.3V Fixed Output
VFB2				
EN1, EN2	Switcher OFF		Switchchr ON	Switcher ON
EN3, EN5	LDO OFF	not use	LDO ON	VREG3 on (EN3 only)

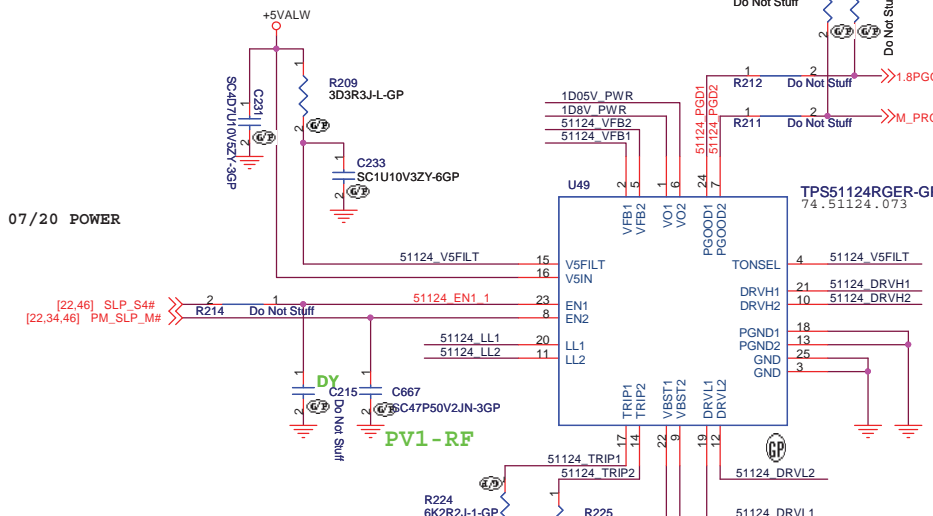
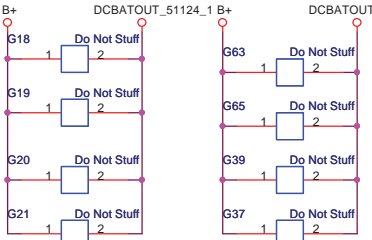
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File: **TPA51120 +5VALW +3VALW**

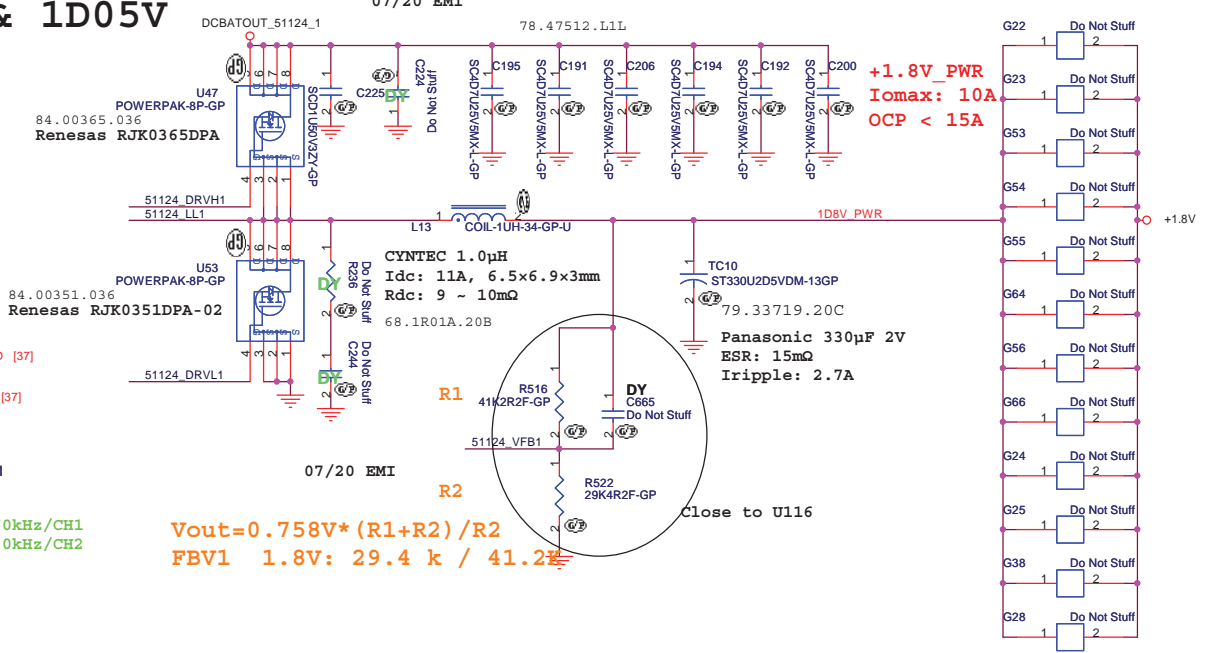
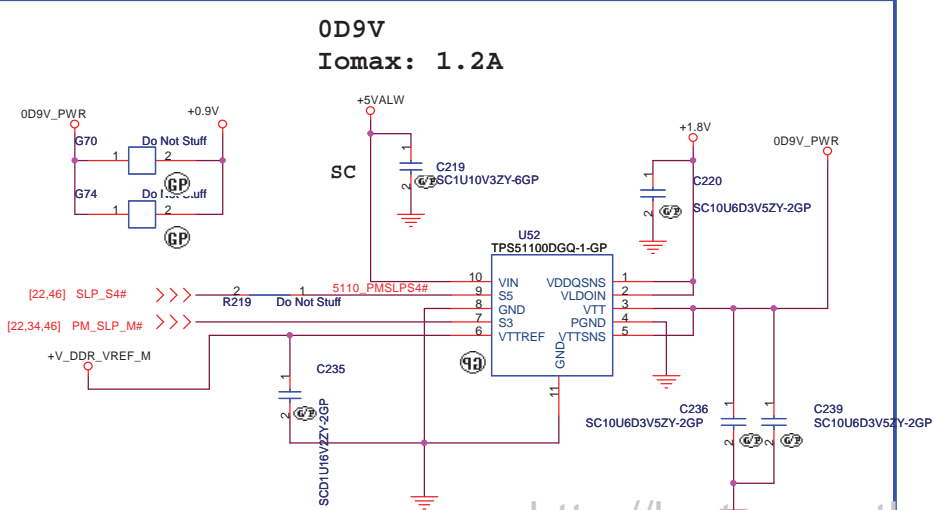
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1D8V & 1D05V

	GND	OPEN	V5FILT
TONSEL	230k/CH1 283k/CH2	283k/CH1 346k/CH2	360kHz/CH1 420kHz/CH2

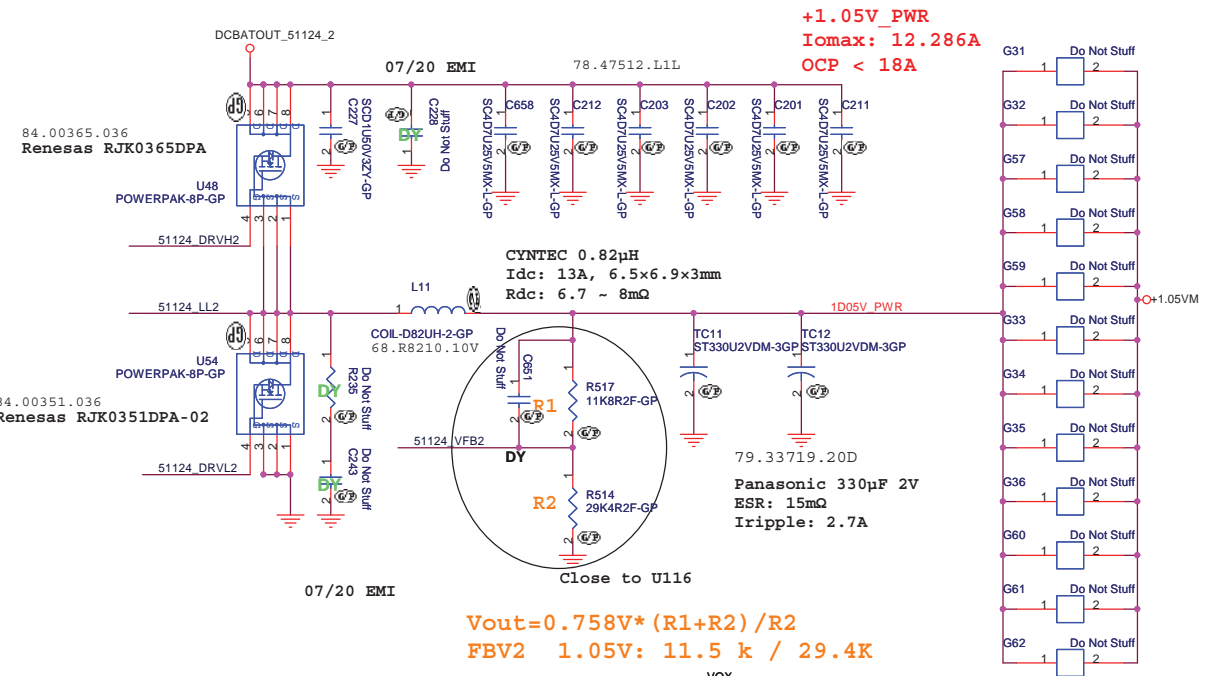


1.5V OCP: 12A, Trip1: 12K7
1.05V OCP: 15A, Trip2: 7k5



$$V_{out} = 0.758V * (R1 + R2) / R2$$

$$FBV1 \ 1.8V: 29.4 \text{ k} / 41.2 \text{ k}$$



$$V_{out} = 0.758V * (R1 + R2) / R2$$

$$FBV2 \ 1.05V: 11.5 \text{ k} / 29.4 \text{ k}$$

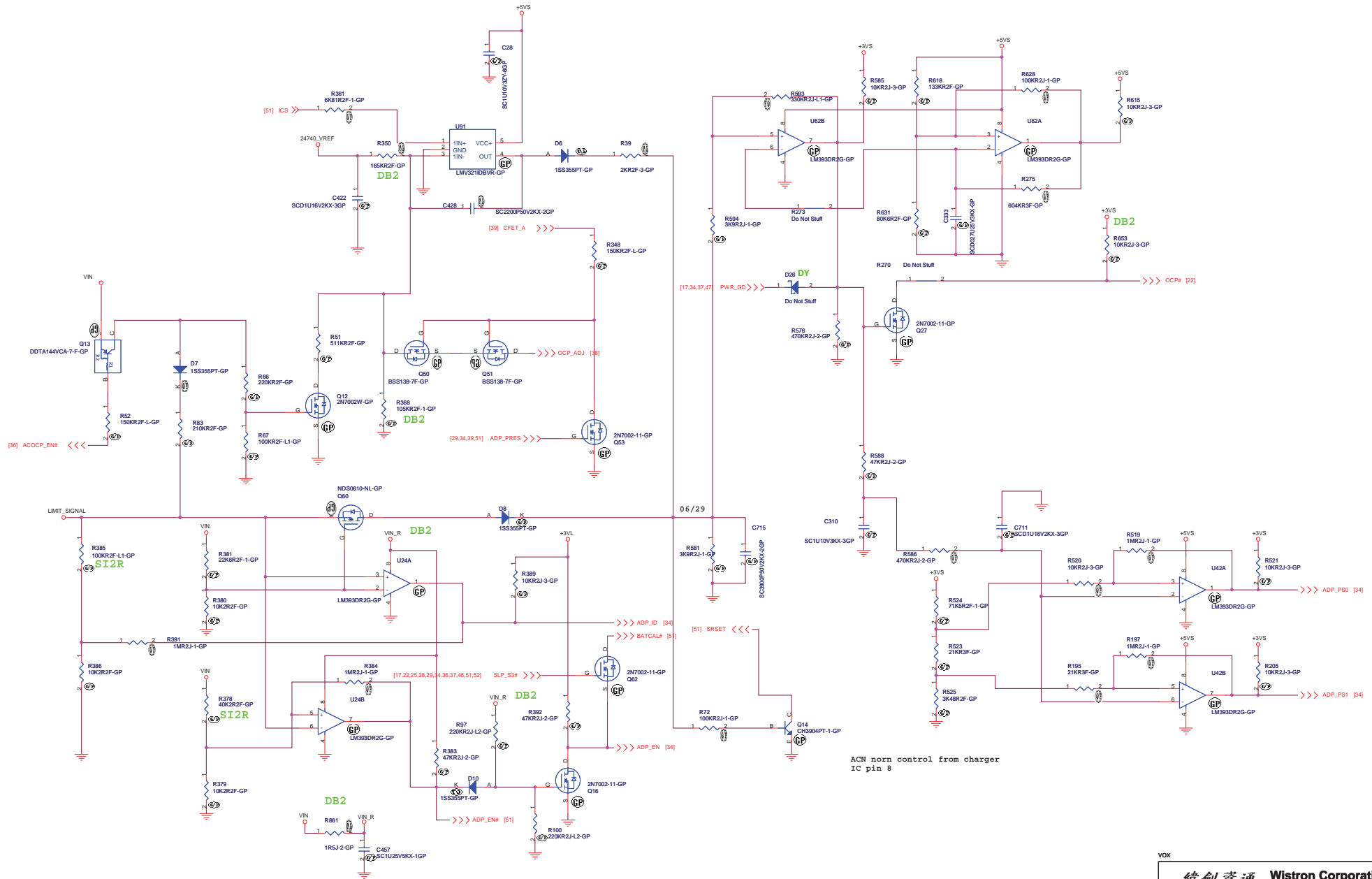
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Title: **TPS51124 1D5V/1D05V**

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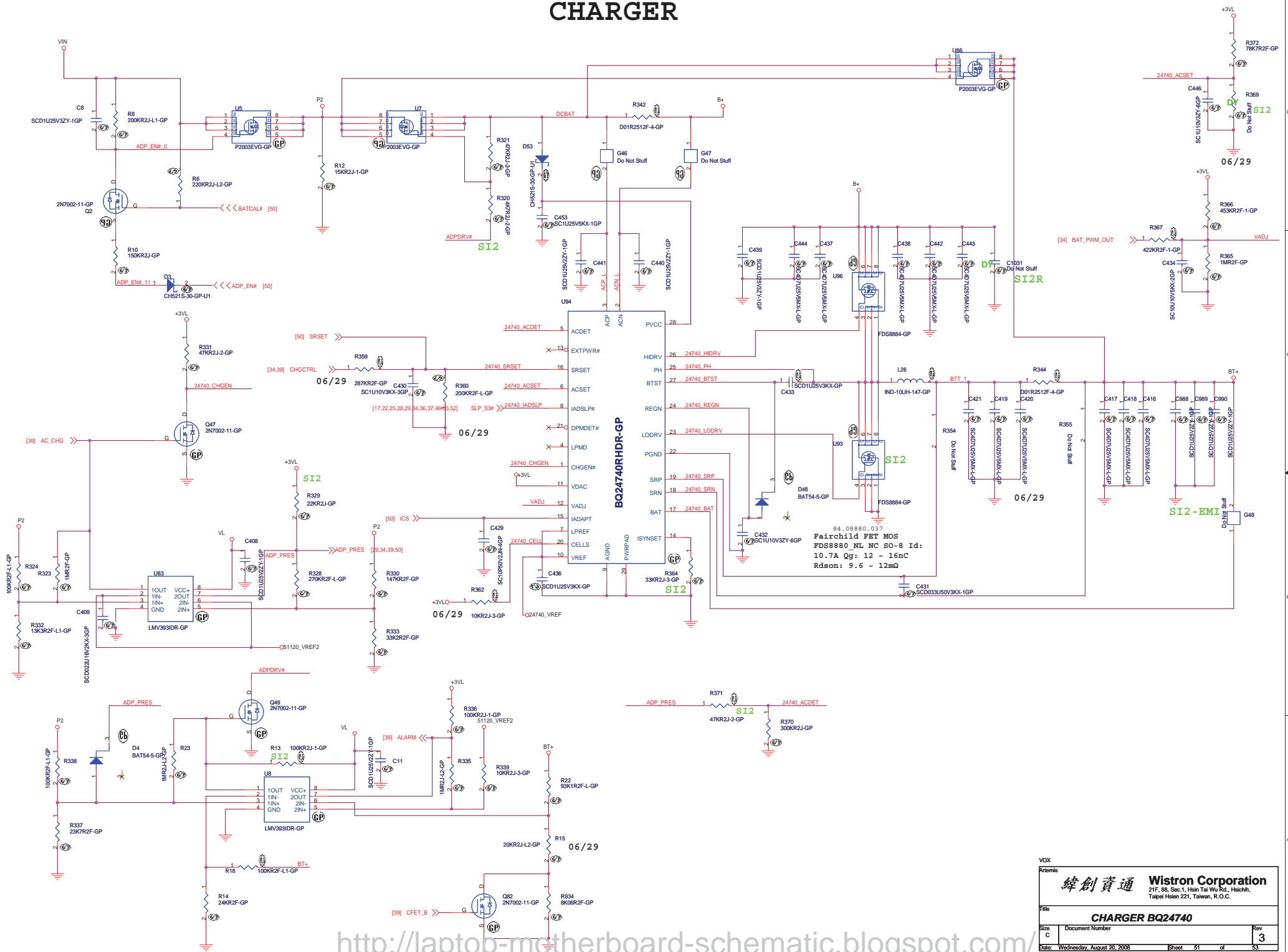
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ADP/OCP

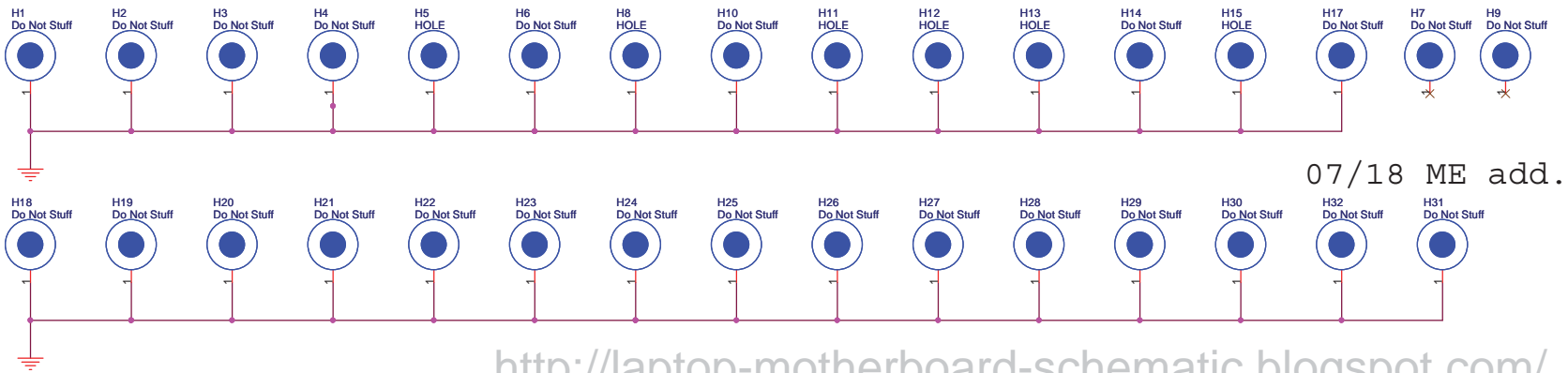
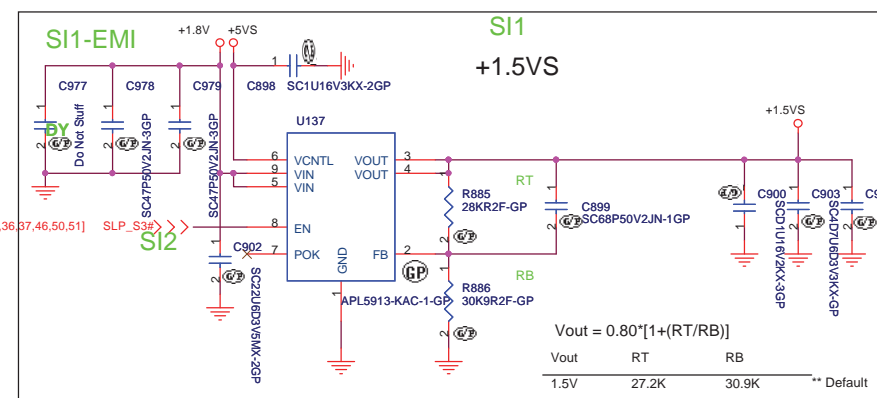
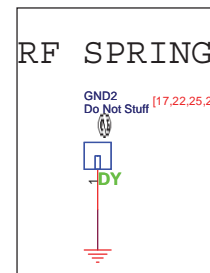
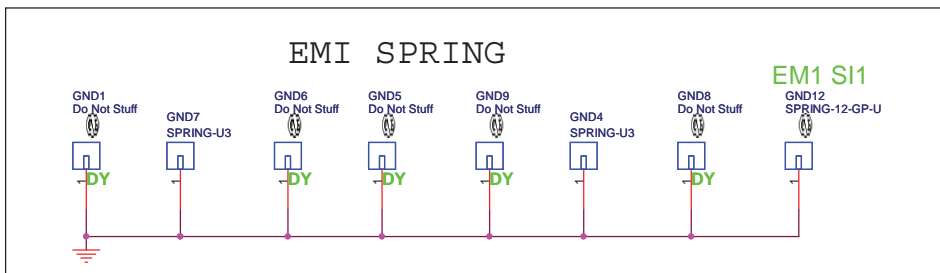
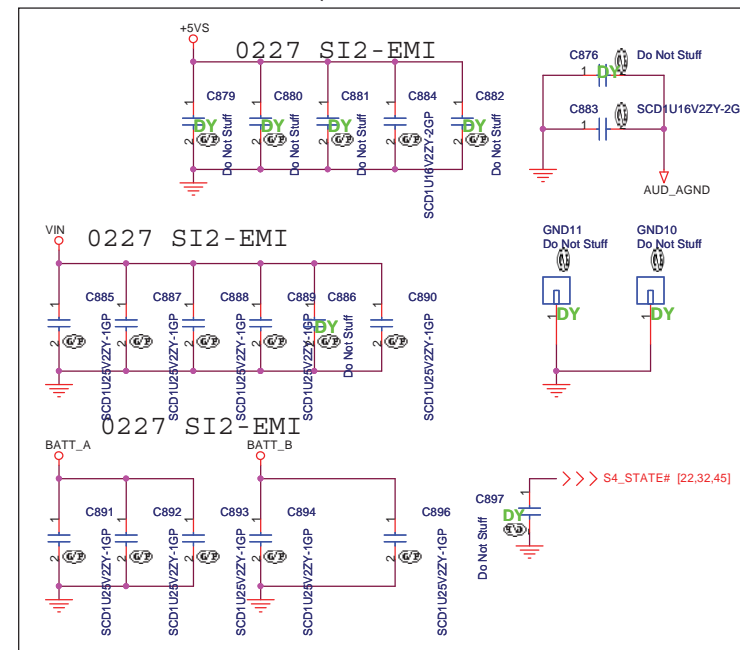
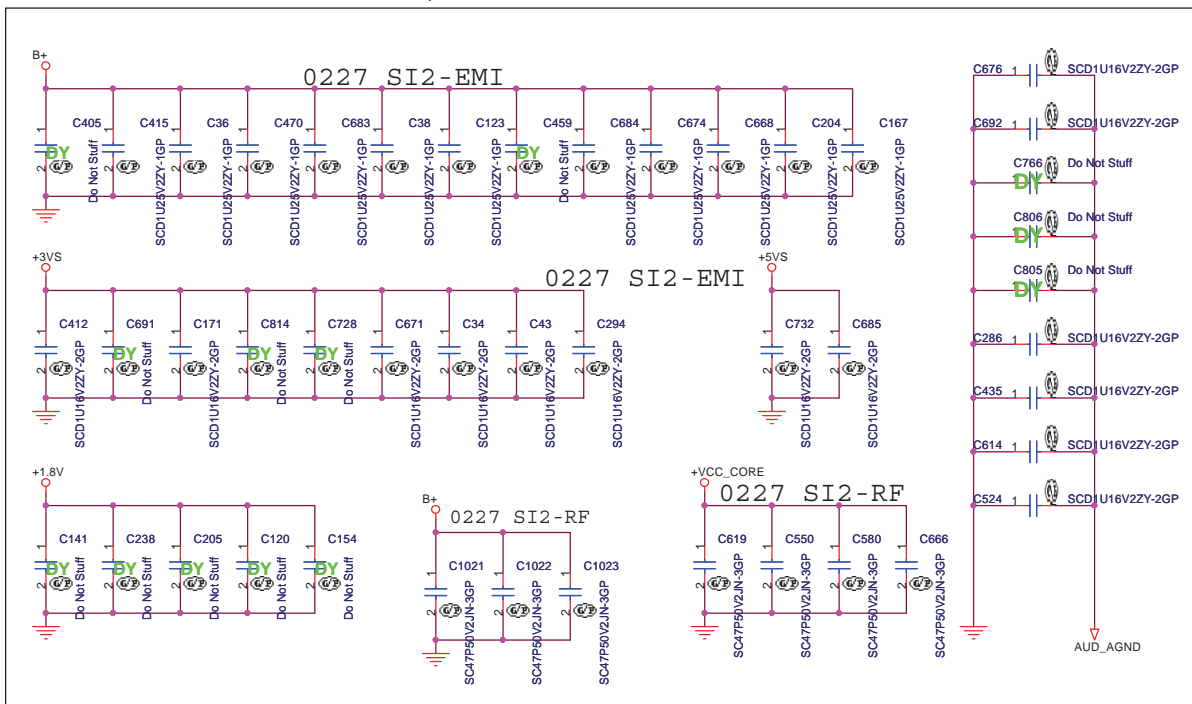


VOX	
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CHARGER



VOX	
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CHARGER BQ24740	
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07/18 ME add.

