

# PWWAA

## LC Marseille

# LA-6842P REV 0.2 Schematic

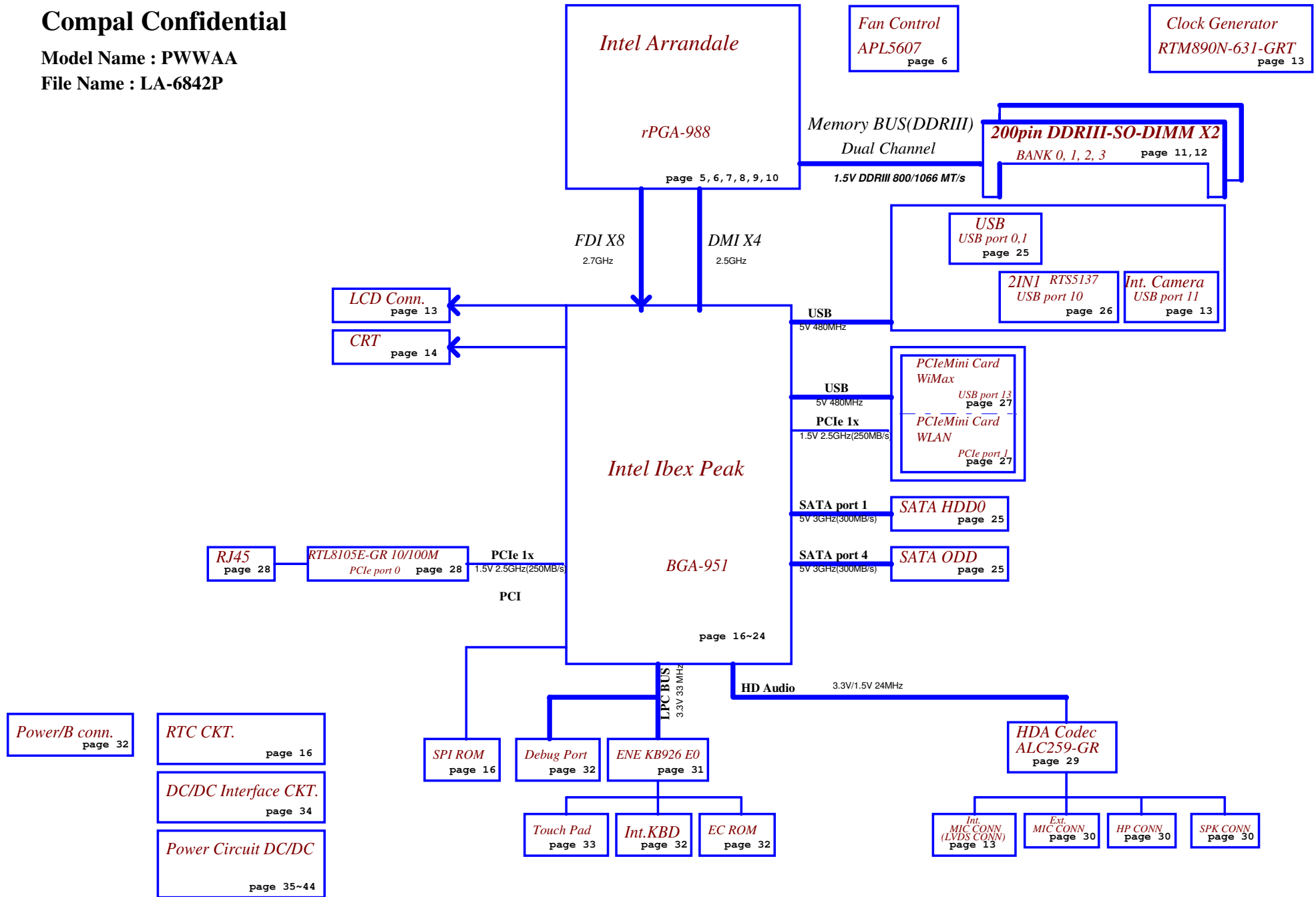
Intel Processor (ARD) /PCH (HM55)  
2010-07-22 Rev 0.2

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Issued Date	2010/06/21	Deciphered Date	2011/06/21	Title <b>Cover Page</b>		
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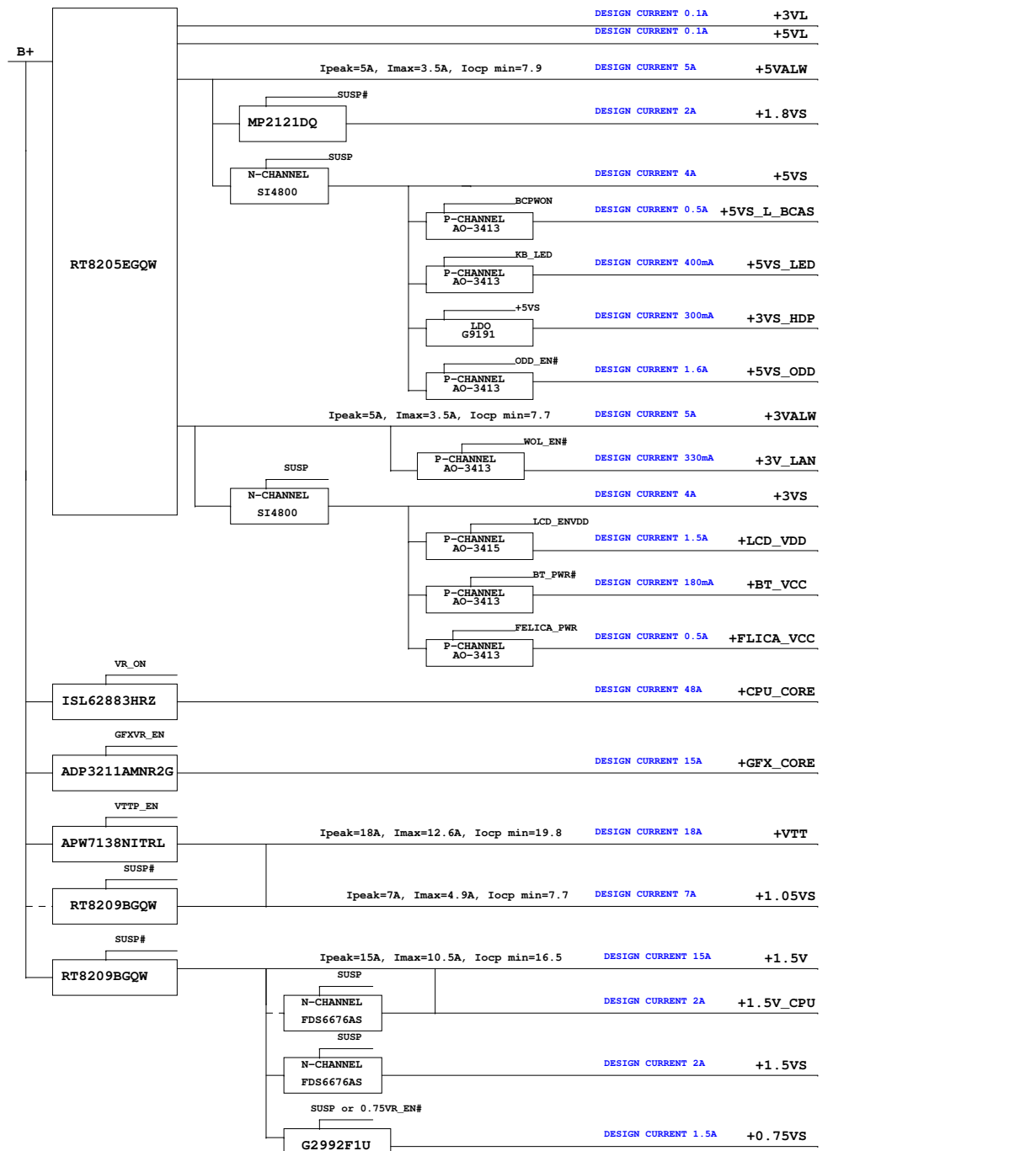
# Compal Confidential

Model Name : PWVAA

File Name : LA-6842P



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				<b>Power Tree</b>
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**Voltage Rails** ( O MEANS ON X MEANS OFF )

power plane	+RTCVCC	+B	+5VL +3VL	+5VALW +3VALW +VSB	+1.5V	+5VS +3VS +1.5VS +VGA_CORE +CPU_CORE +VTT +1.05VS +1.8VS +1.1VS +0.75VS	
							State
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**BTO Option Table**

Function	MINI PCI-E SLOT		LAN					
description		SLOT1	LAN					
explain		WLAN/BT	10/100M					
BTO								

Function			Camera & Mic					
description			Camera & Mic					
explain			Camera & Mic					
BTO			CAM@					

Function	S3 Power Saving		
description	S3 Power Saving		
explain		Power Saving	
BTO			

**PCH SM Bus Address**

Power	Device	HEX	Address
+3VS	DDR SO-DIMM 0	A0 H	1010 0000 b
+3VS	DDR SO-DIMM 1	A4 H	1010 0100 b
+3VS	Clock Generator	D2 H	1101 0010 b
+3VS	New Card		
+3VS	WLAN/WIMAX		
+3VS	Clock Generator		

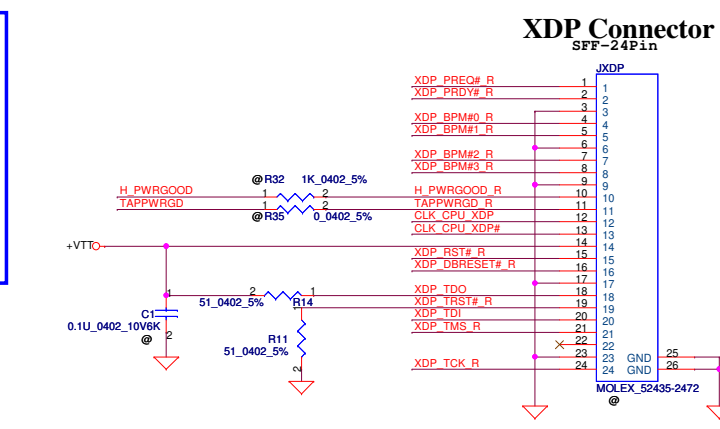
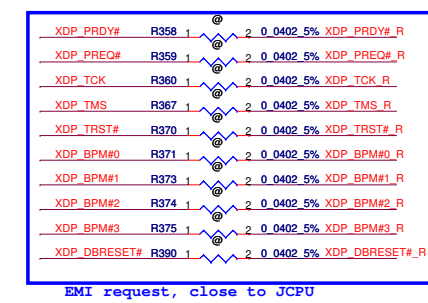
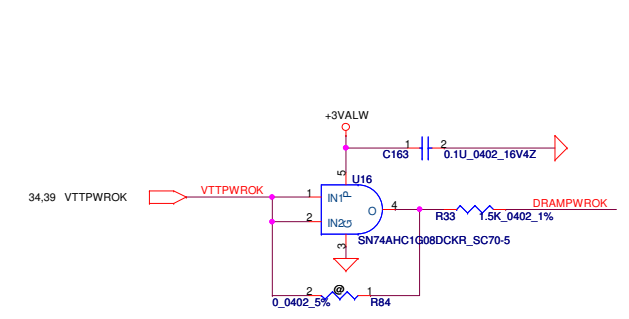
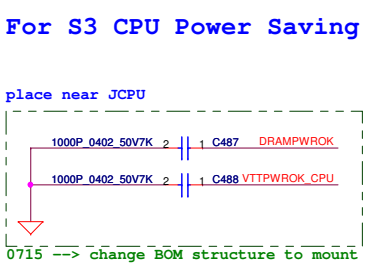
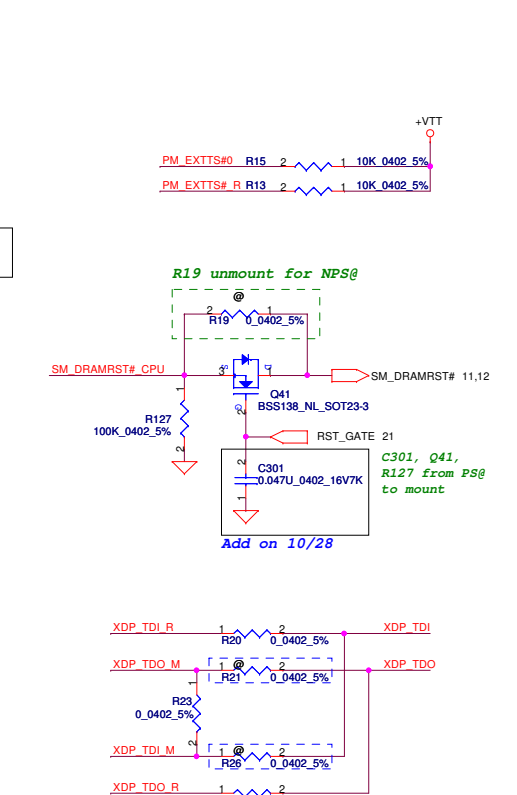
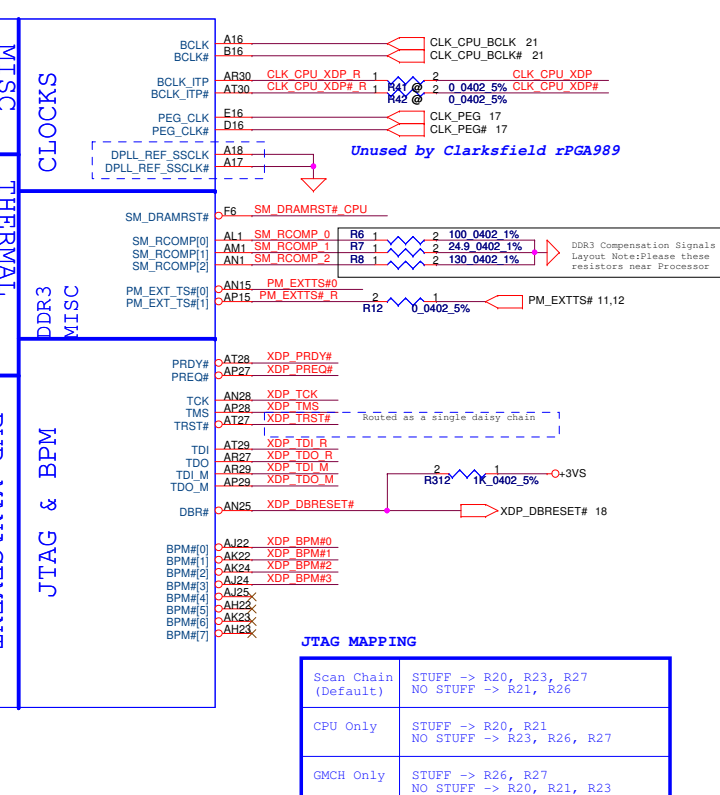
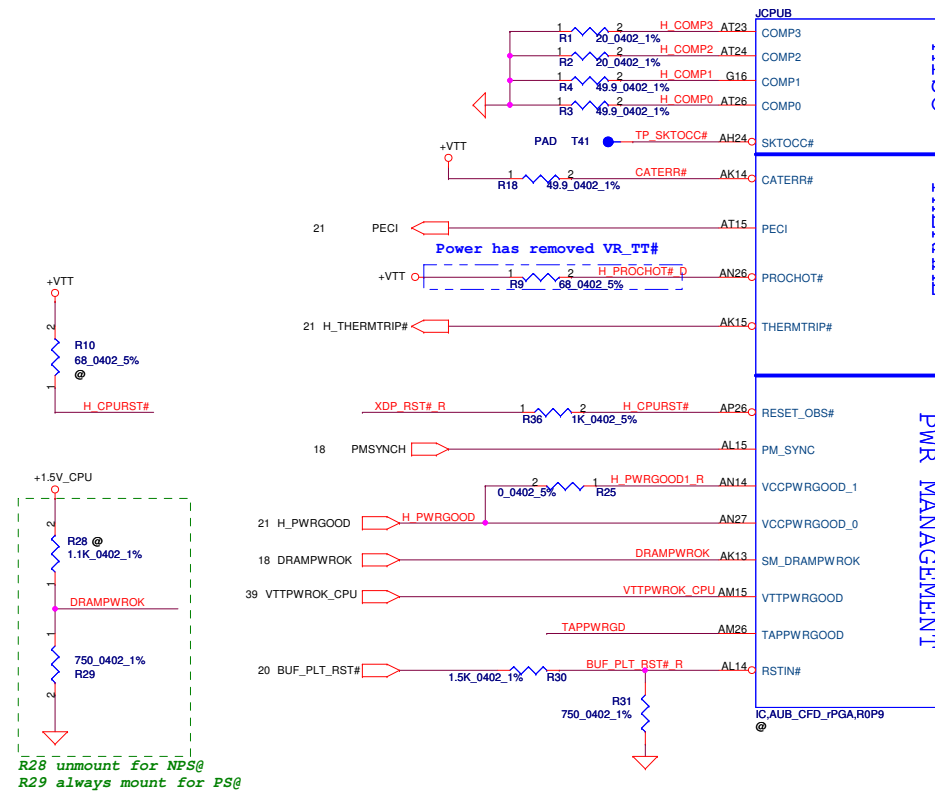
**EC SM Bus1 Address**

Power	Device	HEX	Address
+3VL	Smart Battery	16 H	0001 0110 b

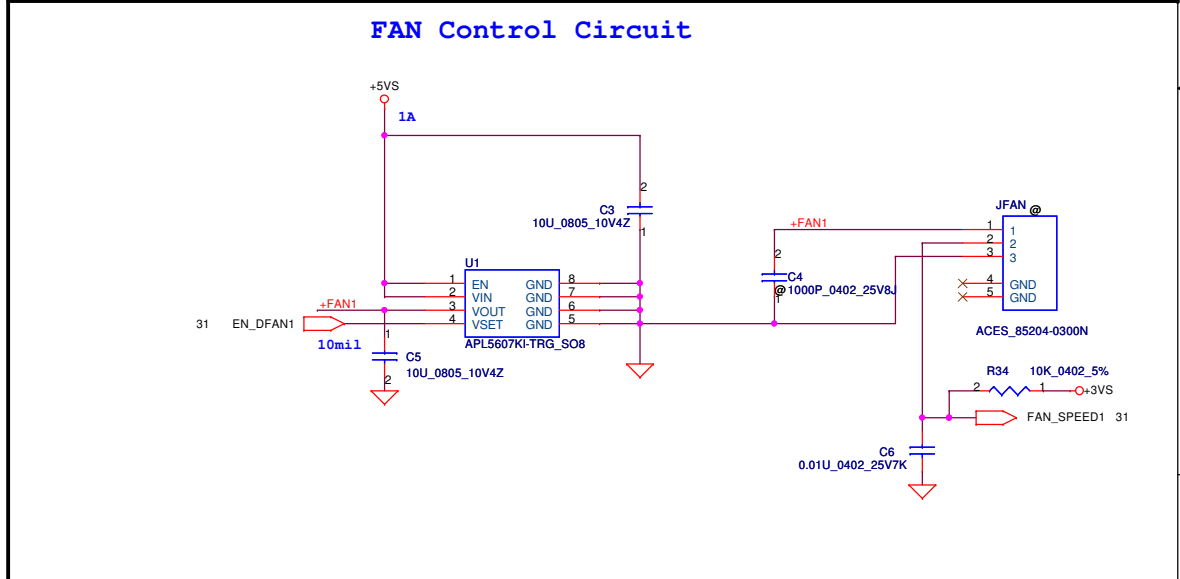
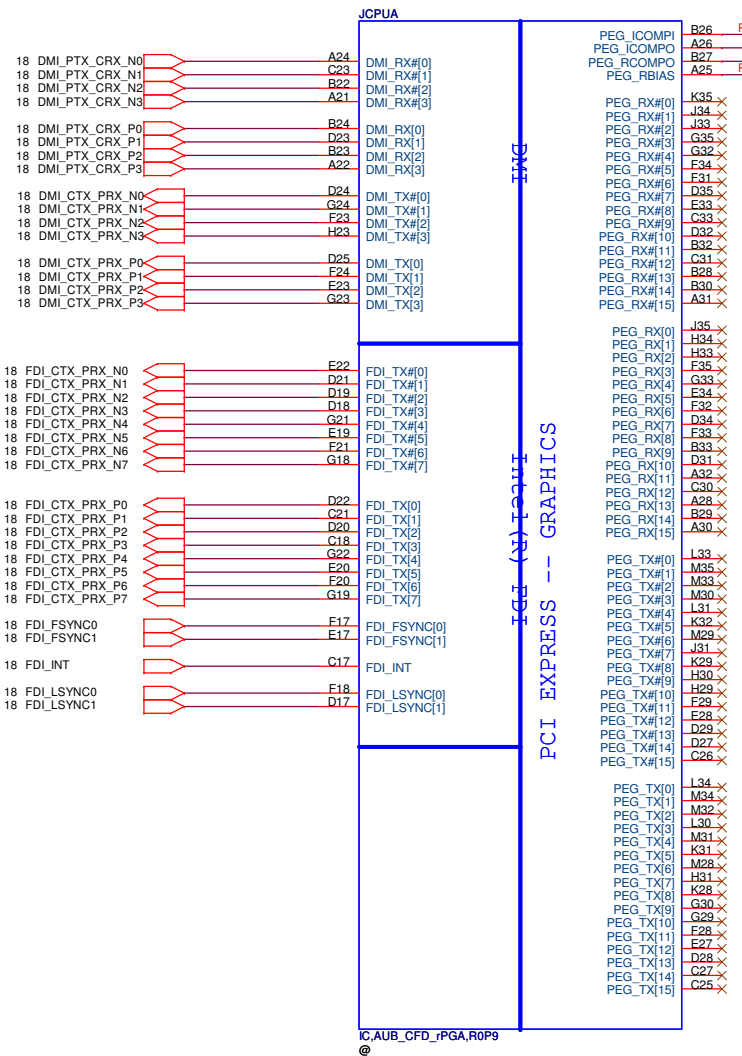
**EC SM Bus2 Address**

Power	Device	HEX	Address
+3VS	PCH	96 H	1001 0110 b

STATE	SIGNAL	SLP_S3#	SLP_S4#	SLP_S5#
Full ON		HIGH	HIGH	HIGH
S1 (Power On Suspend)		HIGH	HIGH	HIGH
S3 (Suspend to RAM)		LOW	HIGH	HIGH
S4 (Suspend to Disk)		LOW	LOW	HIGH
S5 (Soft OFF)		LOW	LOW	LOW
G3		LOW	LOW	LOW

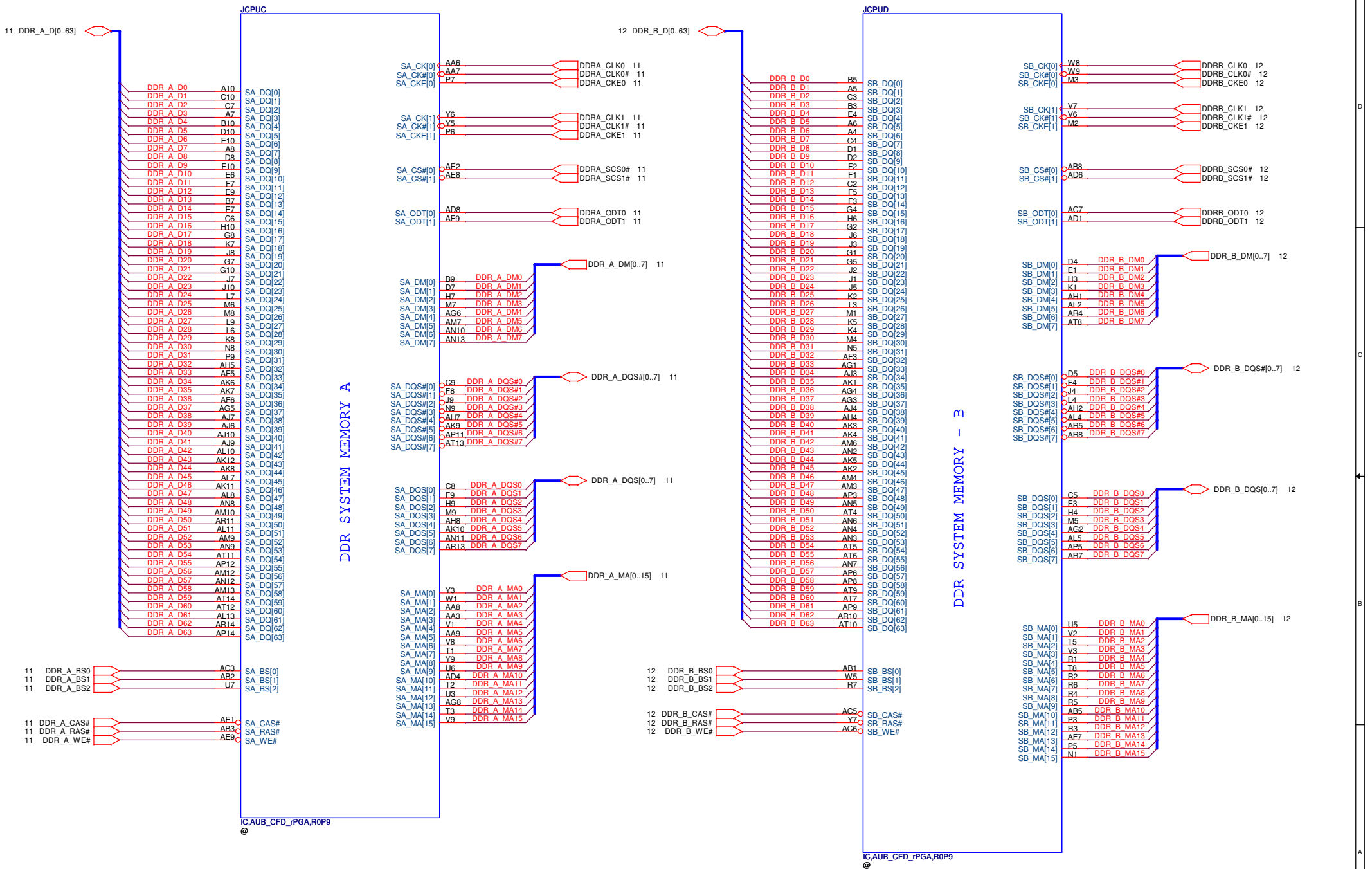


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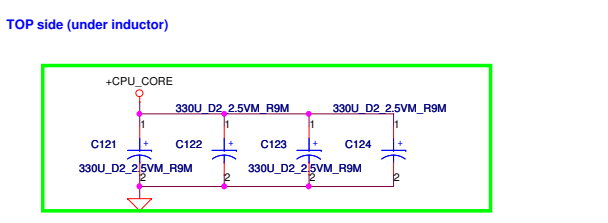
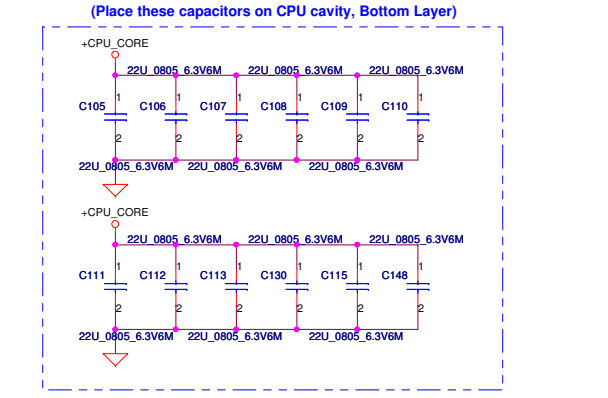
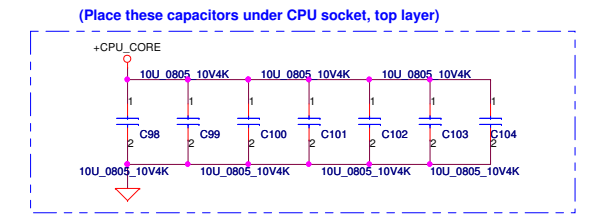
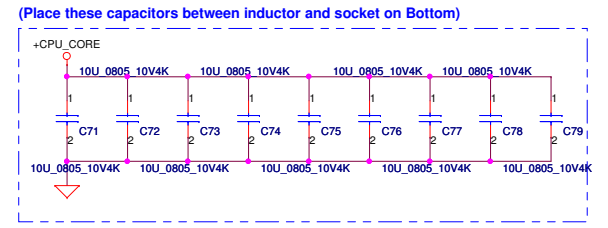
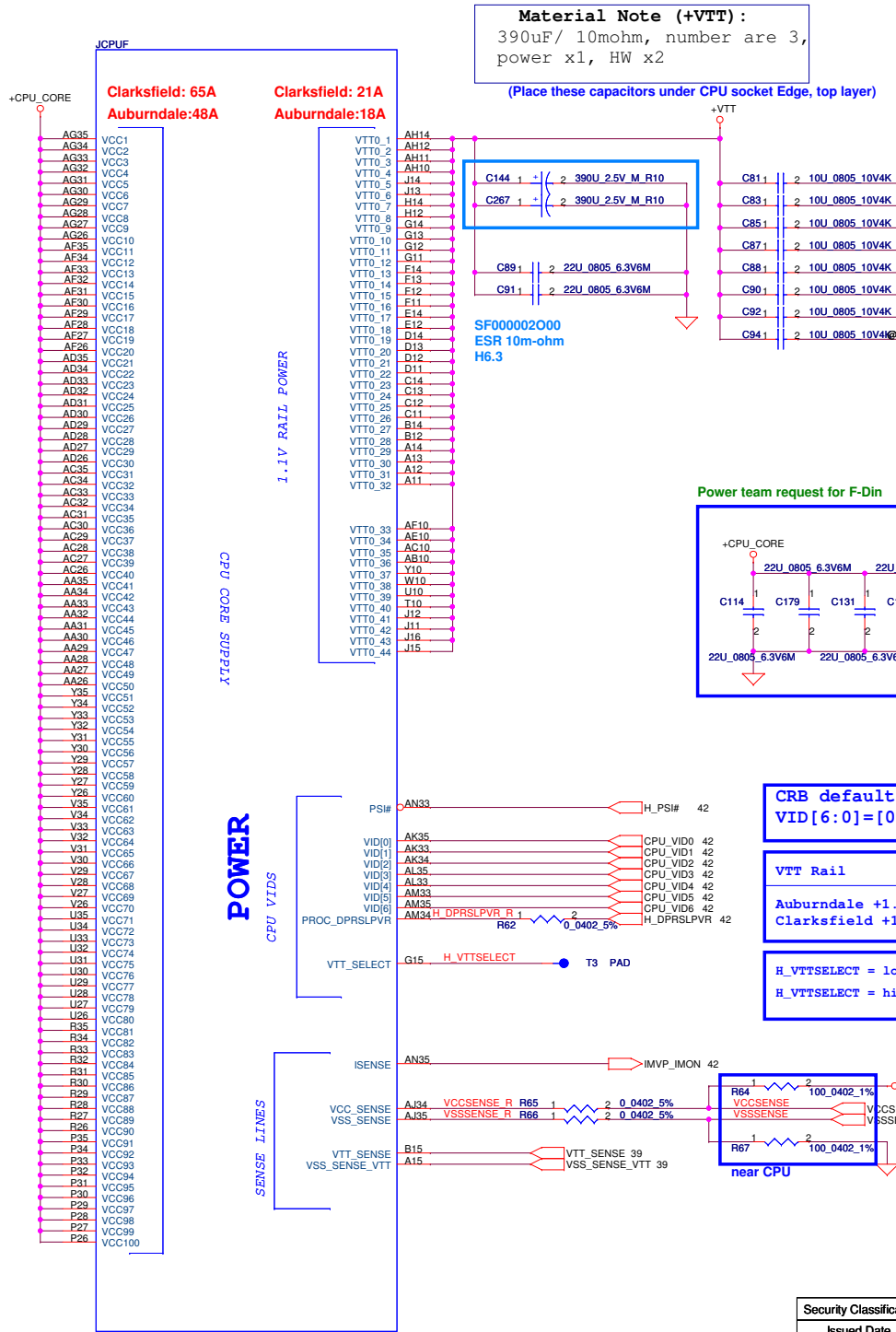


Remove Cap, for EMI

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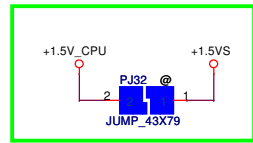
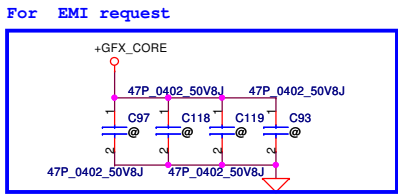
**Check list:**

+CPU\_CORE: 6x 470uF, 12x 22uF, 17x 10uF

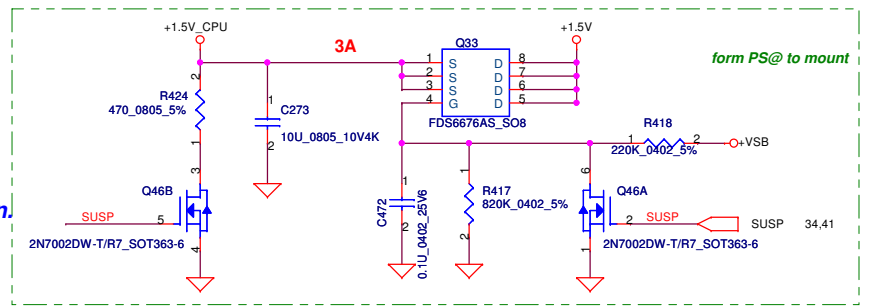
+VTT: 4x 330uF, 7x 22uF, 8x 10uF

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				CPU POWER-1	
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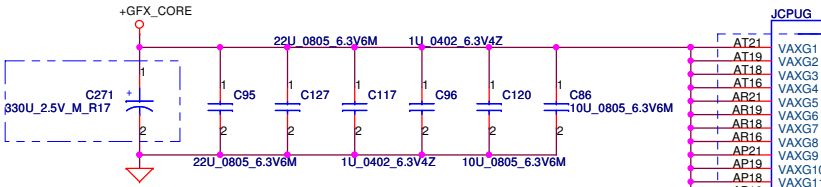


7/22 modified for cost down.

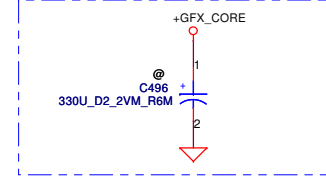


form PS@ to mount

Change C271 to 4.5mm height OS-CON at PVT



Add C496 Co-Layout with C271



For POLY Cap.  
0714 --> C271 mount, C496 unmount

- AT21 VAXG1
- AT19 VAXG2
- AT18 VAXG3
- AT16 VAXG4
- AR21 VAXG5
- AR19 VAXG6
- AR18 VAXG7
- AR16 VAXG8
- AP21 VAXG9
- AP19 VAXG10
- AP18 VAXG11
- AN21 VAXG12
- AN19 VAXG13
- AN18 VAXG14
- AM21 VAXG15
- AM19 VAXG16
- AM18 VAXG17
- AM16 VAXG18
- AM16 VAXG19
- AM16 VAXG20
- AL21 VAXG21
- AL19 VAXG22
- AL18 VAXG23
- AK21 VAXG24
- AK19 VAXG25
- AK18 VAXG26
- AK16 VAXG27
- AJ21 VAXG28
- AJ19 VAXG29
- AJ18 VAXG30
- AJ16 VAXG31
- AH21 VAXG32
- AH19 VAXG33
- AH18 VAXG34
- AH16 VAXG35
- AH16 VAXG36

- GRAPHICS SENSE LINES
- VAXG\_SENSE
- VSSAXG\_SENSE
- GRAPHICS VIDS
- GFX\_VID[0]
- GFX\_VID[1]
- GFX\_VID[2]
- GFX\_VID[3]
- GFX\_VID[4]
- GFX\_VID[5]
- GFX\_VID[6]
- GFX\_VR\_EN
- GFX\_DPRSLPVR
- GFX\_IMON

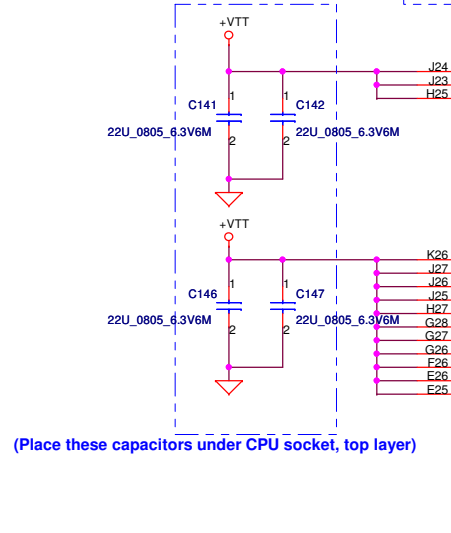
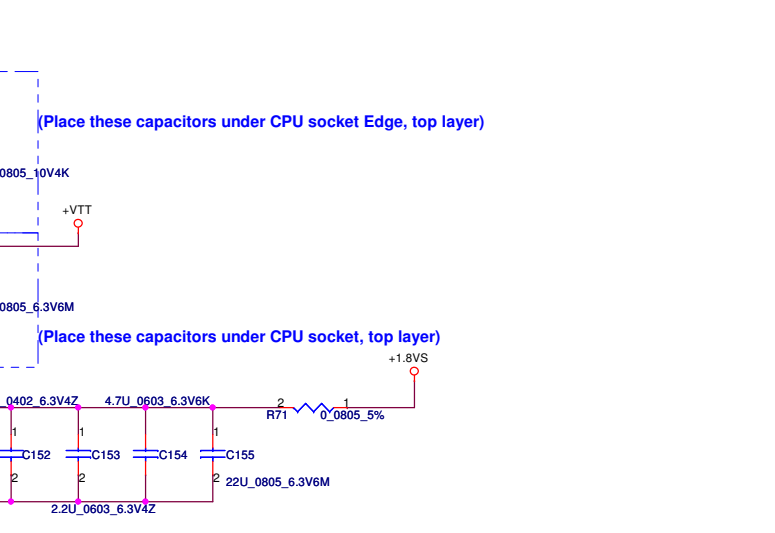
- POWER
- CLARKSFIELD: 5A
- AUBURDLE: 3A
- DDR3 - 1.5V RAILS
- VDDQ01
- VDDQ02
- VDDQ03
- VDDQ04
- VDDQ05
- VDDQ06
- VDDQ08
- VDDQ09
- VDDQ10
- VDDQ11
- VDDQ12
- VDDQ13
- VDDQ14
- VDDQ15
- VDDQ16
- VDDQ17
- VDDQ18

- 1.1V
- VTT0\_59
- VTT0\_60
- VTT0\_61
- VTT0\_62
- VTT1\_63
- VTT1\_64
- VTT1\_65
- VTT1\_66
- VTT1\_67
- VTT1\_68

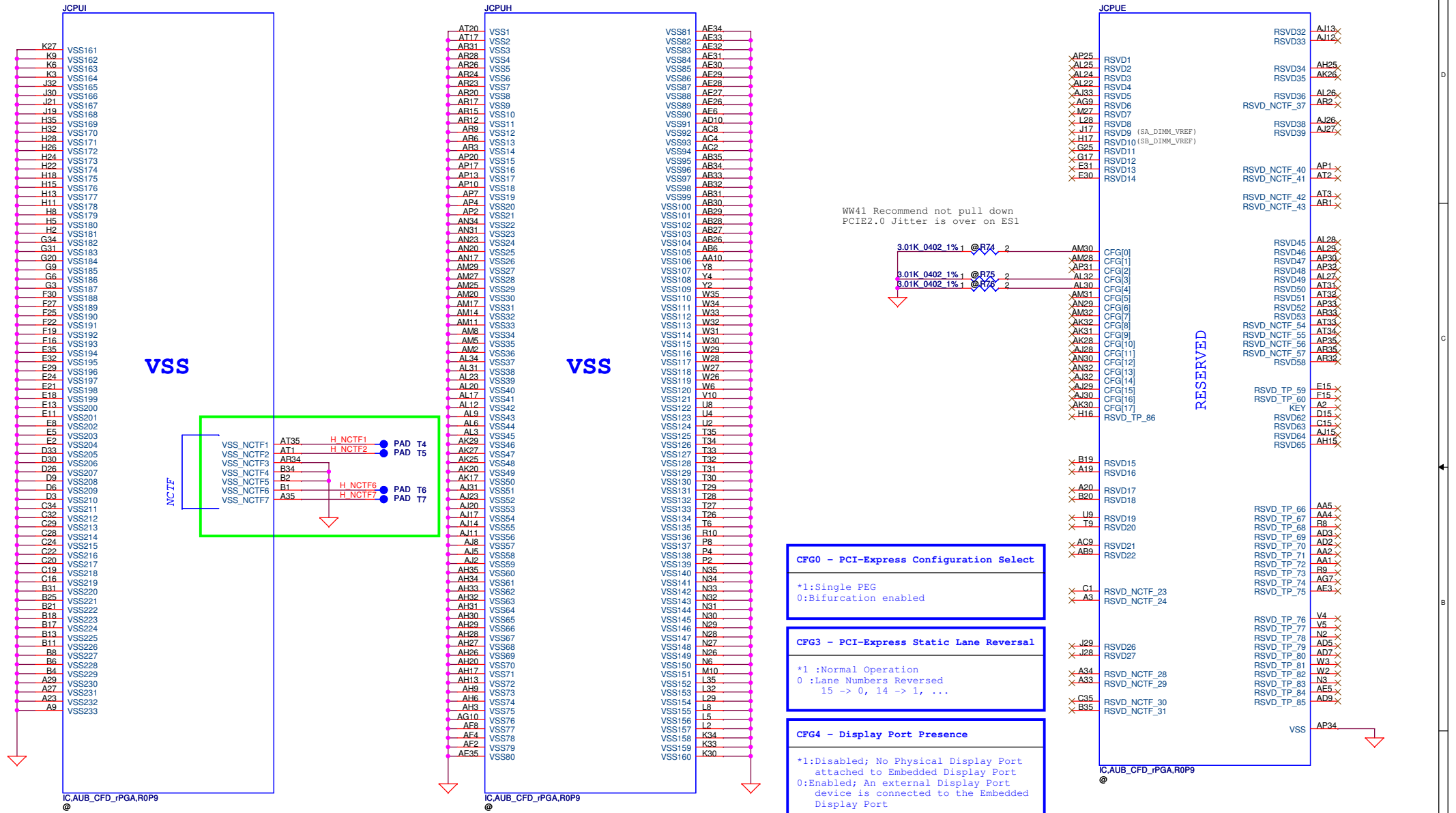
- 1.8V
- VCCPLL1
- VCCPLL2
- VCCPLL3

- FDI
- VTT1\_45
- VTT1\_46
- VTT1\_47

- PEG & DM1
- VTT1\_48
- VTT1\_49
- VTT1\_50
- VTT1\_51
- VTT1\_52
- VTT1\_53
- VTT1\_54
- VTT1\_55
- VTT1\_56
- VTT1\_57
- VTT1\_58



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WW41 Recommend not pull down  
PCIE2.0 Jitter is over on ES1

**CFG0 - PCI-Express Configuration Select**  
\*1:Single PEG  
0:Bifurcation enabled

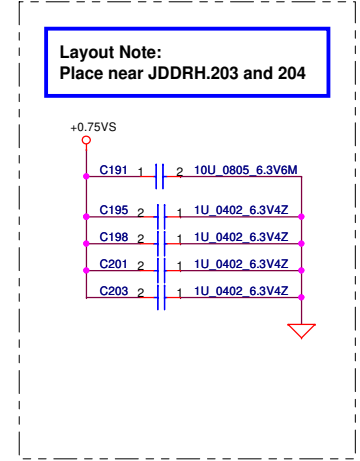
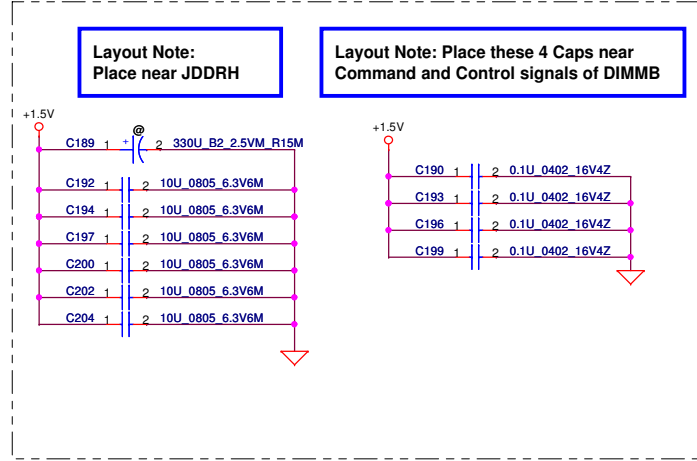
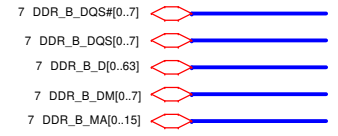
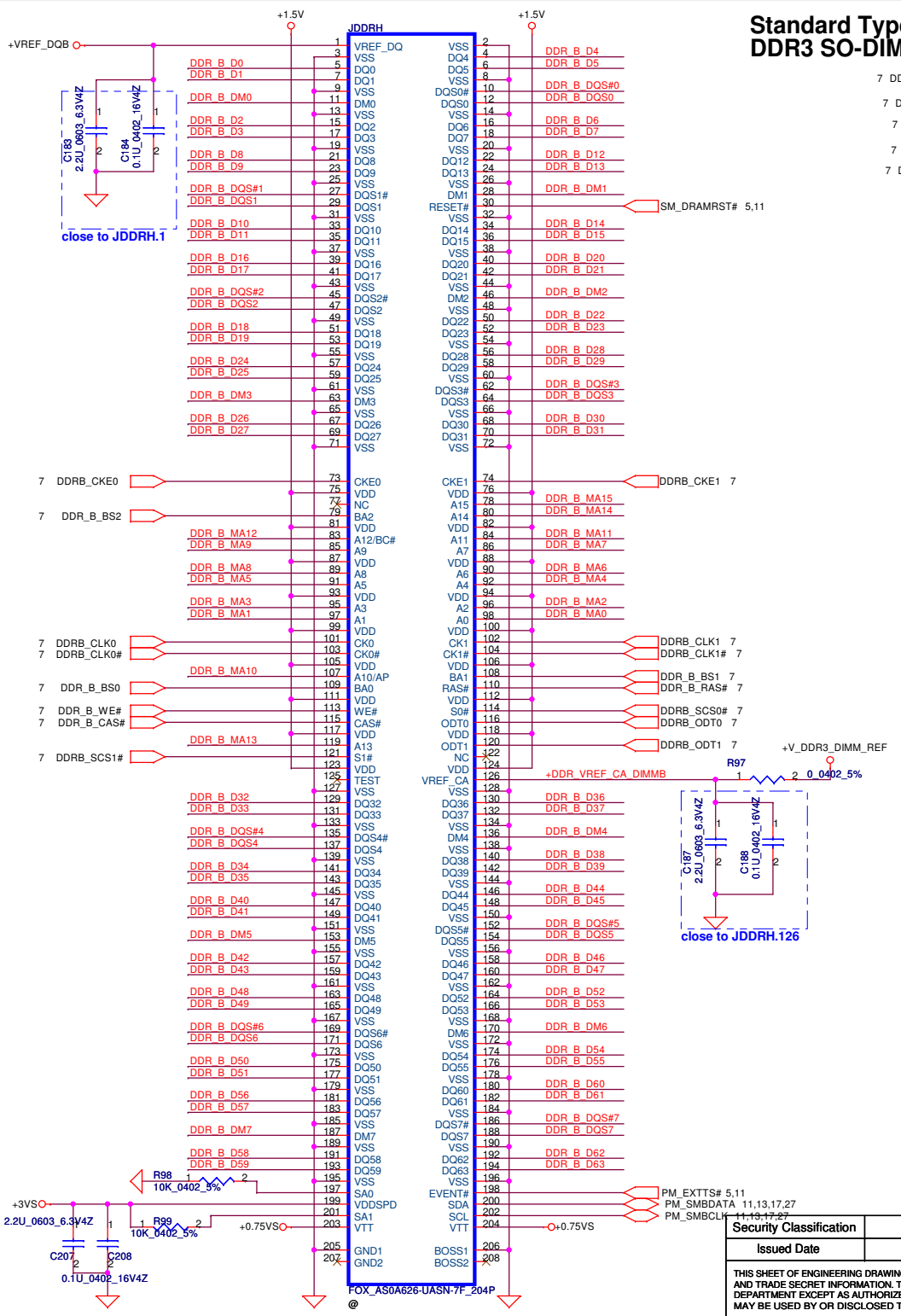
**CFG3 - PCI-Express Static Lane Reversal**  
\*1 :Normal Operation  
0 :Lane Numbers Reversed  
15 -> 0, 14 -> 1, ...

**CFG4 - Display Port Presence**  
\*1:Disabled; No Physical Display Port  
attached to Embedded Display Port  
0:Enabled; An external Display Port  
device is connected to the Embedded  
Display Port

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# Standard Type DDR3 SO-DIMM B

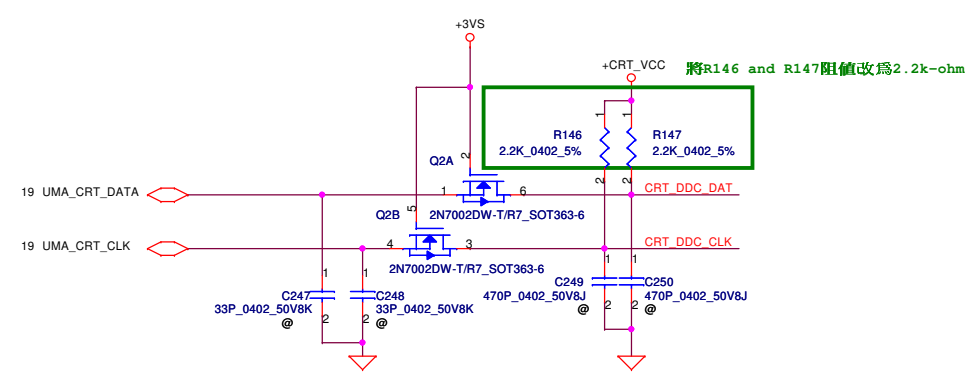
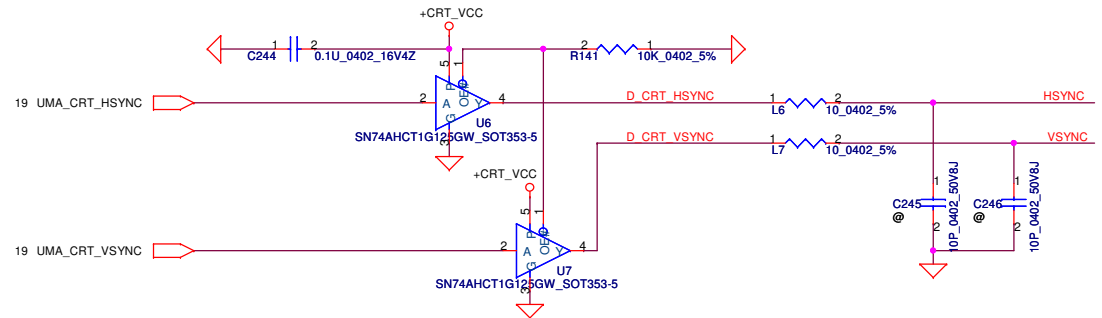
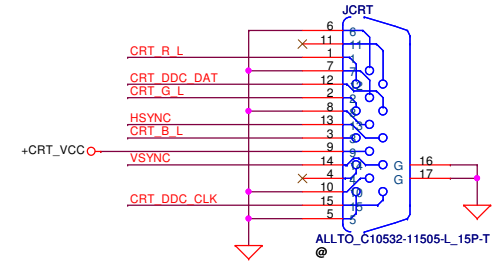
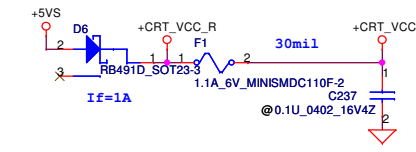
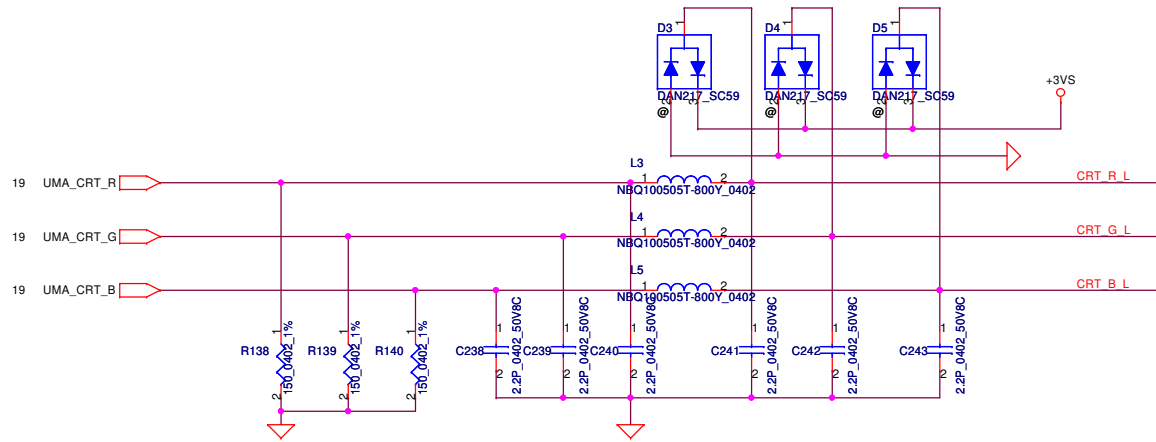


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Title <b>DDRIII-SODIMM1</b>			
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# CRT CONNECTOR

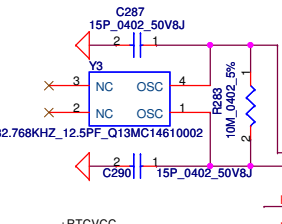
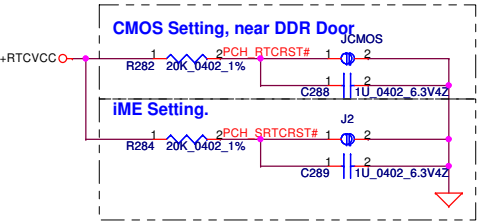


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**0624 --> Remove BIOS ROM Debug Circuit**

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**Integrated SUS 1.05V VRM Enable**

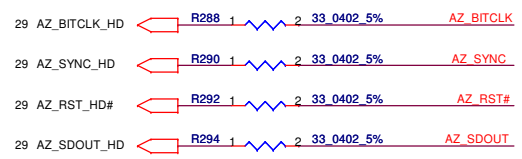
PCH_INTVRMEN	High - Enable Internal VRs (must be always pulled high)
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**HDA\_SYNC**  
 This signal has a weak internal pull down.  
 H=>On Die PLL is supplied by 1.5V  
 L=>On Die PLL is supplied by 1.8V

**HDA\_SDO**  
 This signal has a weak internal pull down.  
 This signal can't PU

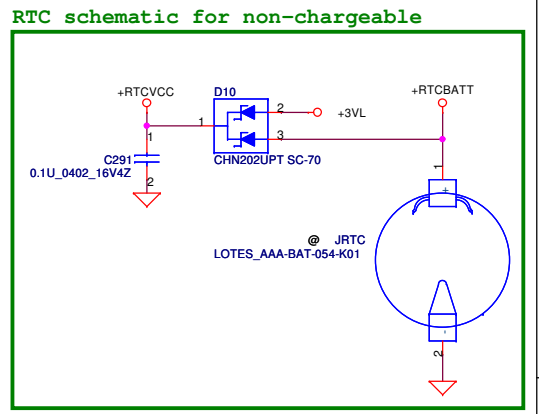
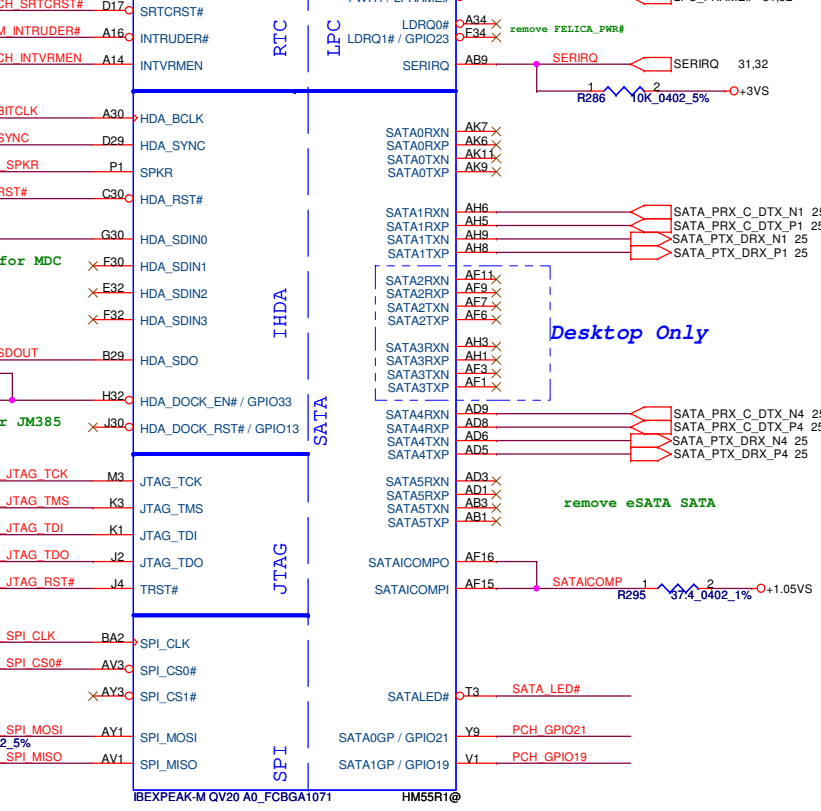
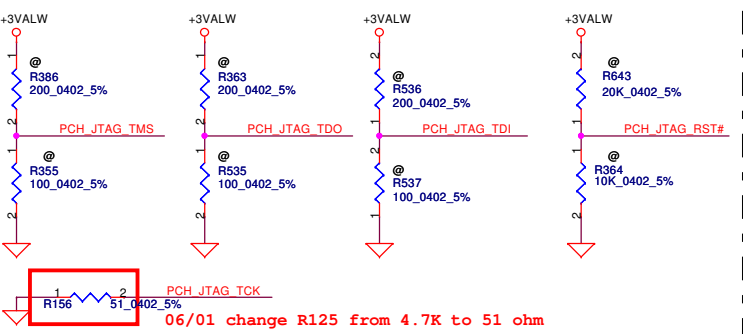
**Flash Descriptor Security Override**

HDA_DOCK_EN#	Low = Enabled High = Disabled *
--------------	------------------------------------



**ITPM Enabled Internal: Pull down 20k**

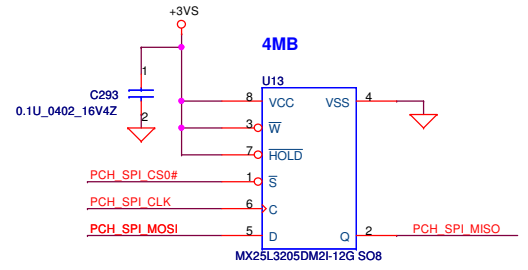
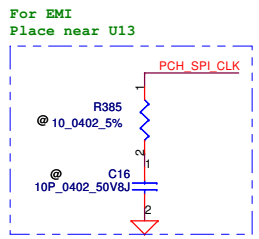
SPI_MOSI	High = Enabled Low = Disabled (Default)
----------	--



1ST HDD

Desktop Only

SATA ODD



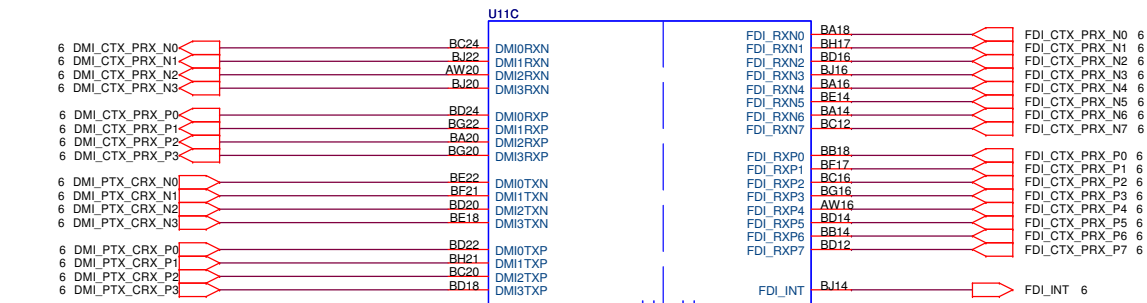
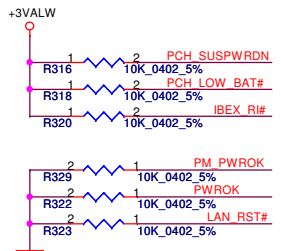
PCH_Pin	RefDes	PCH JTAG Enable		PCH JTAG Disable (Default)	
		ES1	ES2	ES1	ES2
PCH_JTAG_TDO	R358	No Install	200ohm	No Install	No Install
PCH_JTAG_TMS	R355	No Install	100ohm	No Install	No Install
PCH_JTAG_TDI	R354	100ohm	100ohm	No Install	No Install
PCH_JTAG_TDI	R536	200ohm	200ohm	20Kohm	No Install
PCH_JTAG_TDI	R537	100ohm	100ohm	10Kohm	No Install
PCH_JTAG_TCK	R156	51ohm	51ohm	51ohm	51ohm
PCH_JTAG_RST#	R643	20Kohm	20Kohm	No Install	No Install
PCH_JTAG_RST#	R353	10Kohm	10Kohm	No Install	No Install

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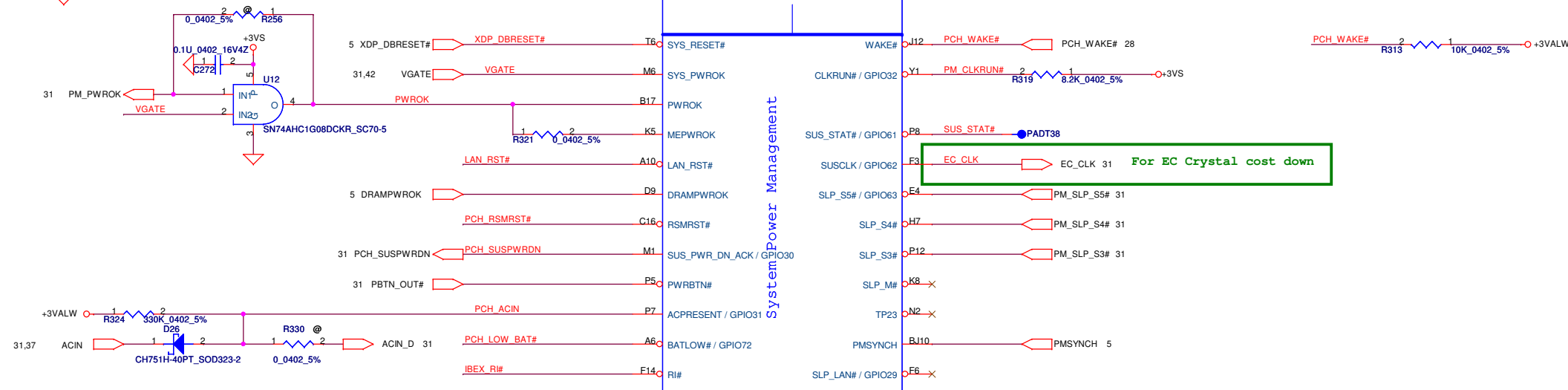
Compal Electronics, Inc.		
PCH-SPI/SATA/LPC/RTC/HDA		
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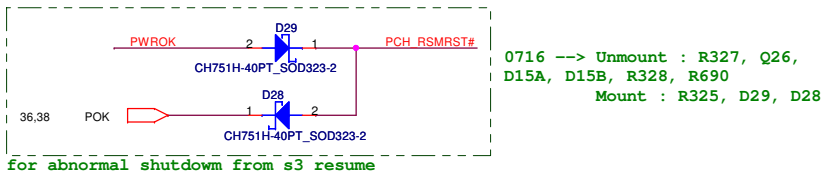
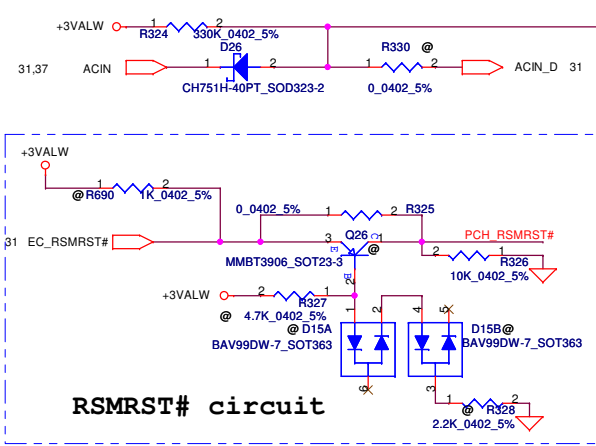




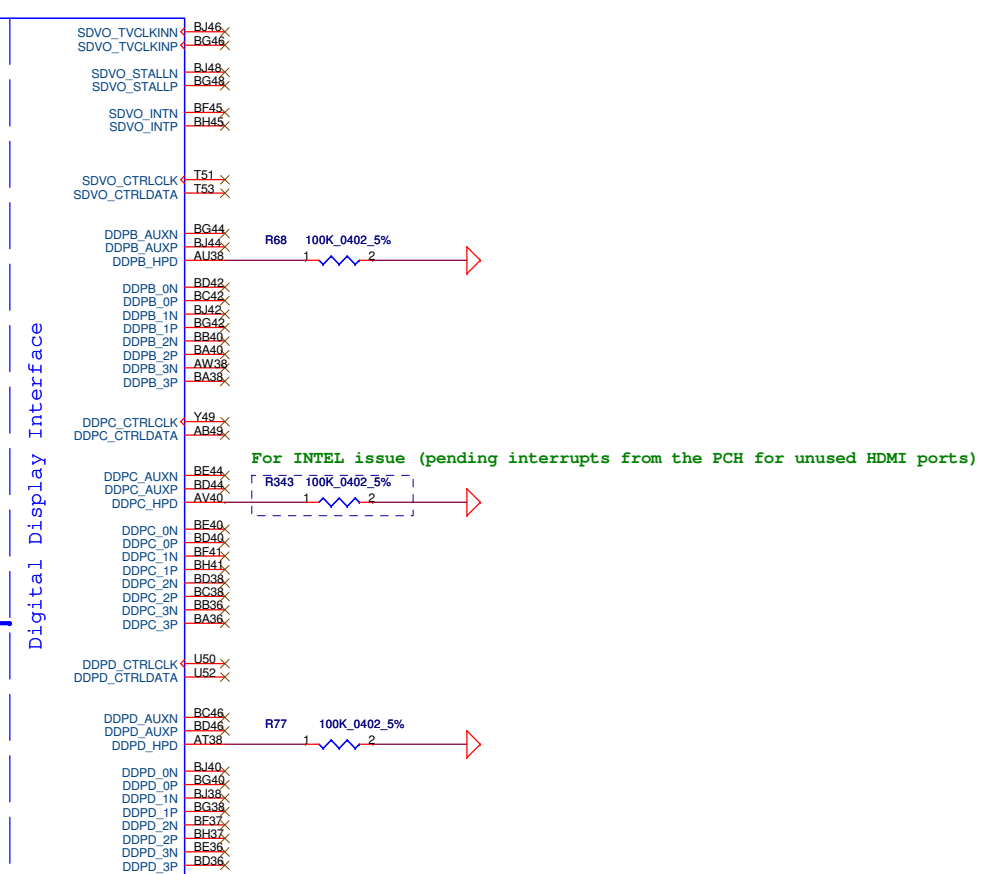
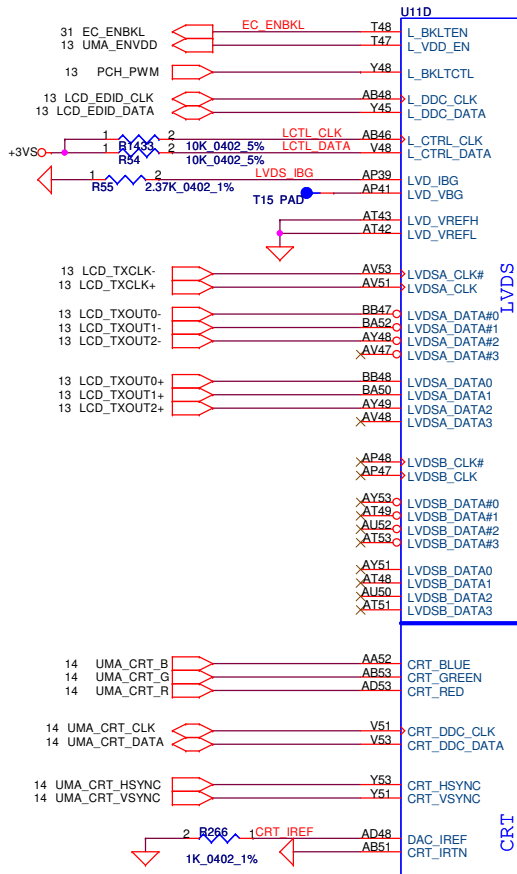
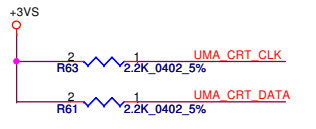
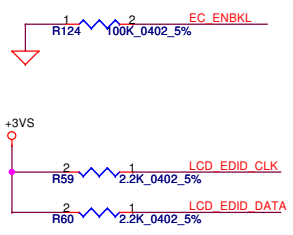
Close to PCH



System Power Management

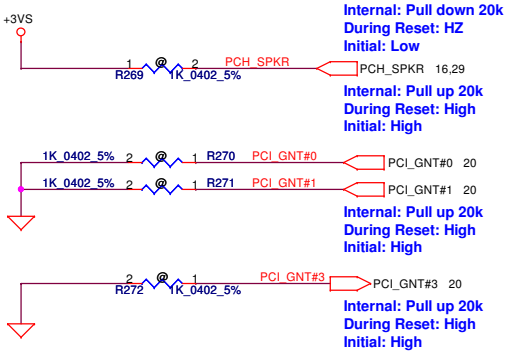


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				PCH-DMI/FDI/PWM	
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				PWWAA LA6842P M/B	
				Date:	Wednesday, July 28, 2010
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				Rev	0.2

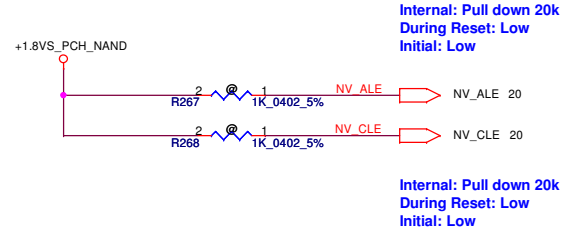


For INTEL issue (pending interrupts from the PCH for unused HDMI ports)

# PCH Strap Pin



<b>NO REBOOT Strap</b>		
PCH_SPKR	Low= Disable	High= Enable
<b>Boot BIOS Strap</b>		
PCI_GNT#1	PCI_GNT#0	Boot BIOS Location
0	0	LPC
0	1	Reserved (NAND)
1	0	PCI
1	1	SPI (Default)
<b>A16 Swap Override Strap</b>		
PCI_GNT#3	Low= A16 swap override Enable	High= A16 swap override Disable



<b>Danbury Technology Enabled</b>	
NV_ALE	High = Enabled Low = Disabled (Default)
<b>DMI Termination Voltage</b>	
NV_CLE	Low= Set to Vss (Default) High= Set to Vcc

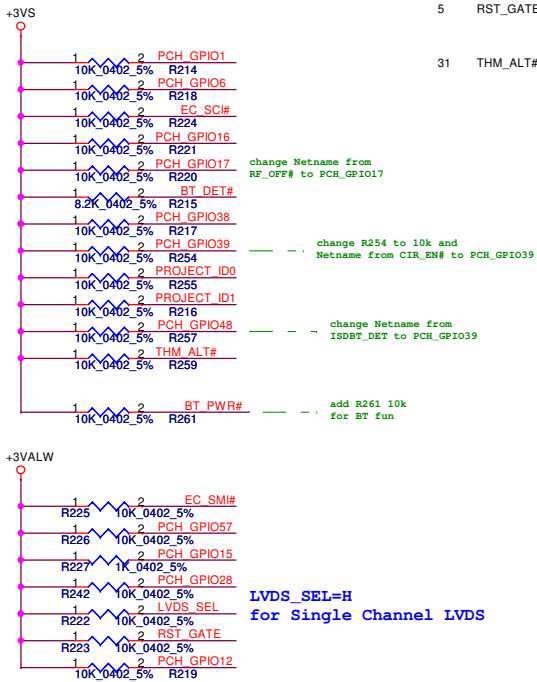


**GPIO8**  
Not pull down  
Internal: Pull up 20k  
During Reset: High  
Initial: High

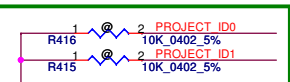
**GPIO15**  
a Strong pull up may be needed  
for GPIO Functionality  
Internal: Pull down 20k  
During Reset: Low  
Initial: Low

**On-Die PLL VR**  
PCH\_GPIO27 High = Enabled (Default)  
Low = Disabled

PROJECT_ID			
Name	ID0	ID1	
NBQAA 11.6/13.3"	L	L	
NBQAA 14"	L	H	
*NBQAA 16"	H	L	
NALAA 17.3"	H	H	

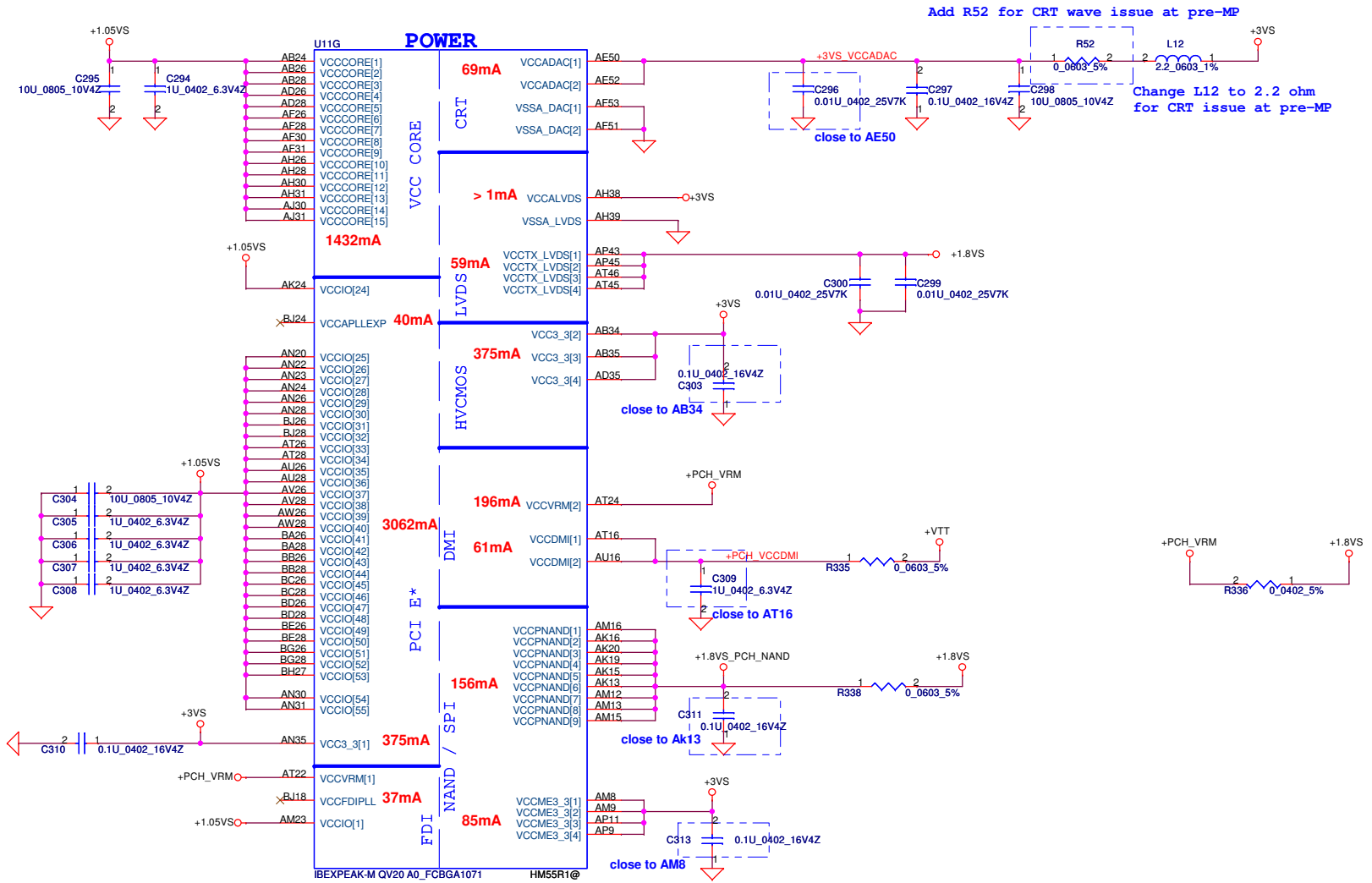


LVDS\_SEL=H  
for Single Channel LVDS

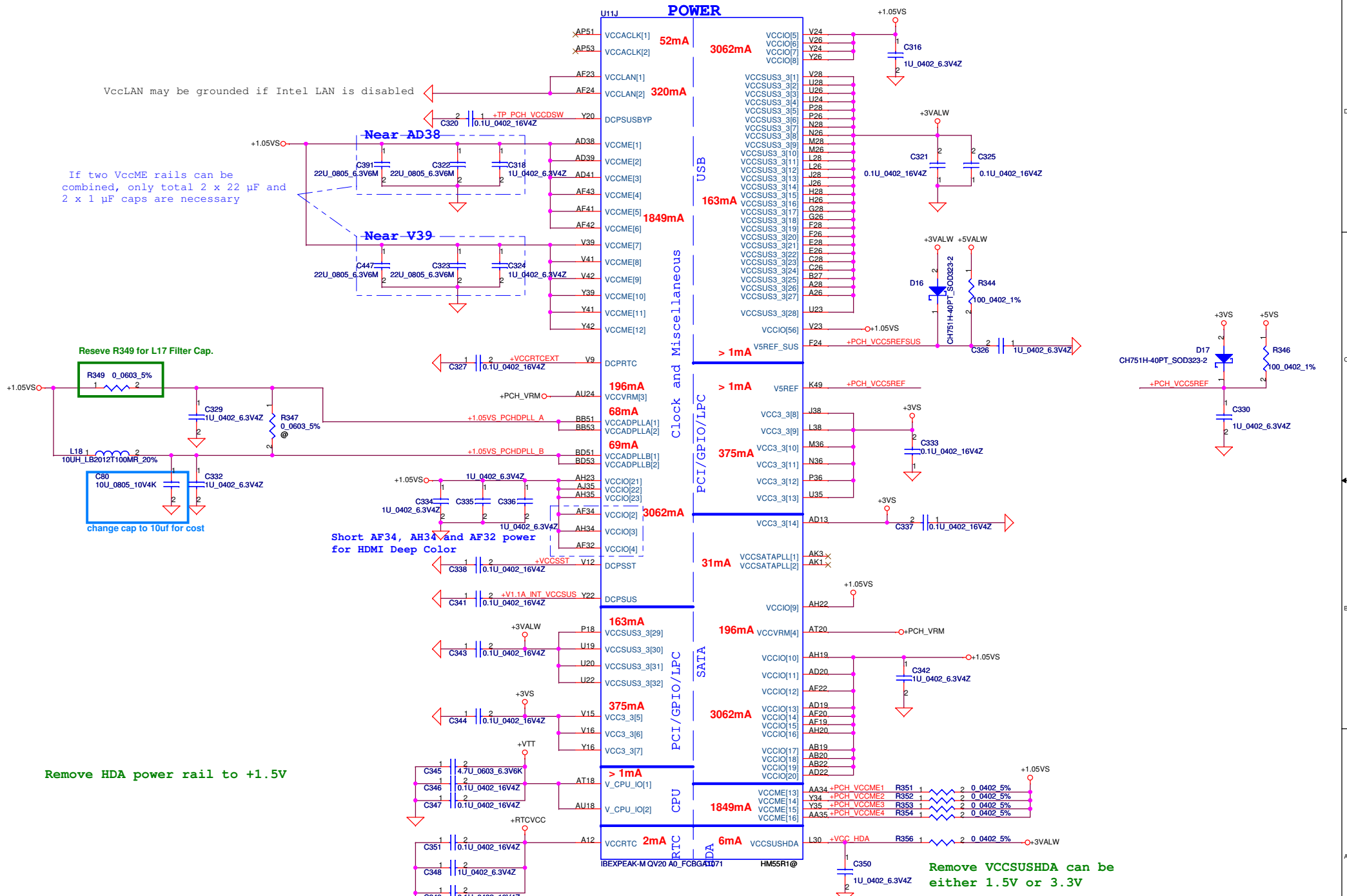


Not pull low  
internal pull up  
Internal: Pull up 20k  
During Reset: High  
Initial: High

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Size	Document Number	Rev		Date	
Custom	PWWAA LA6842P M/B	0.2		Wednesday, July 28, 2010	
				Sheet	23 of 45



U11		H49	
AY7	VSS[159]	VSS[259]	H5
B11	VSS[160]	VSS[260]	J24
B15	VSS[161]	VSS[261]	K11
B19	VSS[162]	VSS[262]	K43
B23	VSS[163]	VSS[263]	K47
B31	VSS[164]	VSS[264]	K7
B35	VSS[165]	VSS[265]	L14
B39	VSS[166]	VSS[266]	L18
B43	VSS[167]	VSS[267]	L2
B47	VSS[168]	VSS[268]	L22
B7	VSS[169]	VSS[269]	L32
BC12	VSS[170]	VSS[270]	L36
BB16	VSS[171]	VSS[271]	L40
BB20	VSS[172]	VSS[272]	L52
BB24	VSS[173]	VSS[273]	M12
BB30	VSS[174]	VSS[274]	M16
BB34	VSS[175]	VSS[275]	M20
BB38	VSS[176]	VSS[276]	M38
BB42	VSS[177]	VSS[277]	M34
BB49	VSS[178]	VSS[278]	M38
BB5	VSS[179]	VSS[279]	M42
BB8	VSS[180]	VSS[280]	M46
BC10	VSS[181]	VSS[281]	M49
BC14	VSS[182]	VSS[282]	M5
BC18	VSS[183]	VSS[283]	M8
BC2	VSS[184]	VSS[284]	N24
BC22	VSS[185]	VSS[285]	P11
BC32	VSS[186]	VSS[286]	P22
BC36	VSS[187]	VSS[287]	P30
BC40	VSS[188]	VSS[288]	P32
BC44	VSS[189]	VSS[289]	P34
BC52	VSS[190]	VSS[290]	P42
BH0	VSS[191]	VSS[291]	P45
BD48	VSS[192]	VSS[292]	P47
BD49	VSS[193]	VSS[293]	R2
BD5	VSS[194]	VSS[294]	R52
BE12	VSS[195]	VSS[295]	T12
BE16	VSS[196]	VSS[296]	T41
BE20	VSS[197]	VSS[297]	T46
BE24	VSS[198]	VSS[298]	T49
BE30	VSS[199]	VSS[299]	T5
BE34	VSS[200]	VSS[300]	T8
BE38	VSS[201]	VSS[301]	U30
BE42	VSS[202]	VSS[302]	U31
BE46	VSS[203]	VSS[303]	U32
BE48	VSS[204]	VSS[304]	U34
BE50	VSS[205]	VSS[305]	P38
BE6	VSS[206]	VSS[306]	V11
BE8	VSS[207]	VSS[307]	V16
BF3	VSS[208]	VSS[308]	V19
BF49	VSS[209]	VSS[309]	V20
BF51	VSS[210]	VSS[310]	V22
BG18	VSS[211]	VSS[311]	V30
BG24	VSS[212]	VSS[312]	V31
BG4	VSS[213]	VSS[313]	V32
BG50	VSS[214]	VSS[314]	V34
BH11	VSS[215]	VSS[315]	V35
BH15	VSS[216]	VSS[316]	V38
BH19	VSS[217]	VSS[317]	V43
BH23	VSS[218]	VSS[318]	V45
BH31	VSS[219]	VSS[319]	V46
BH35	VSS[220]	VSS[320]	V47
BH39	VSS[221]	VSS[321]	V49
BH43	VSS[222]	VSS[322]	V5
BH47	VSS[223]	VSS[323]	V7
BH7	VSS[224]	VSS[324]	V8
C12	VSS[225]	VSS[325]	W2
C50	VSS[226]	VSS[326]	W52
D51	VSS[227]	VSS[327]	Y11
E12	VSS[228]	VSS[328]	Y12
E16	VSS[229]	VSS[329]	Y15
E24	VSS[230]	VSS[330]	Y19
E30	VSS[231]	VSS[331]	Y23
E34	VSS[232]	VSS[332]	Y28
E38	VSS[233]	VSS[333]	Y30
E42	VSS[234]	VSS[334]	Y31
E46	VSS[235]	VSS[335]	Y32
E48	VSS[236]	VSS[336]	Y38
E6	VSS[237]	VSS[337]	Y43
E8	VSS[238]	VSS[338]	Y46
F49	VSS[239]	VSS[339]	P49
F5	VSS[240]	VSS[340]	Y5
F5	VSS[241]	VSS[341]	Y6
G10	VSS[242]	VSS[342]	Y8
G18	VSS[243]	VSS[343]	P24
G2	VSS[244]	VSS[344]	T43
G22	VSS[245]	VSS[345]	AD51
G32	VSS[246]	VSS[346]	AT8
G36	VSS[247]	VSS[347]	AD47
G40	VSS[248]	VSS[348]	Y47
G44	VSS[249]	VSS[349]	AT12
G52	VSS[250]	VSS[350]	AM6
AF39	VSS[251]	VSS[351]	AT13
H16	VSS[252]	VSS[352]	AM5
H20	VSS[253]	VSS[353]	AK45
H30	VSS[254]	VSS[354]	AK38
H34	VSS[255]	VSS[355]	AV14
H38	VSS[256]	VSS[356]	
H42	VSS[257]	VSS[357]	
	VSS[258]	VSS[358]	

IBEXPEAK-M QV20 A0\_FCBGA1071 HM55R1@

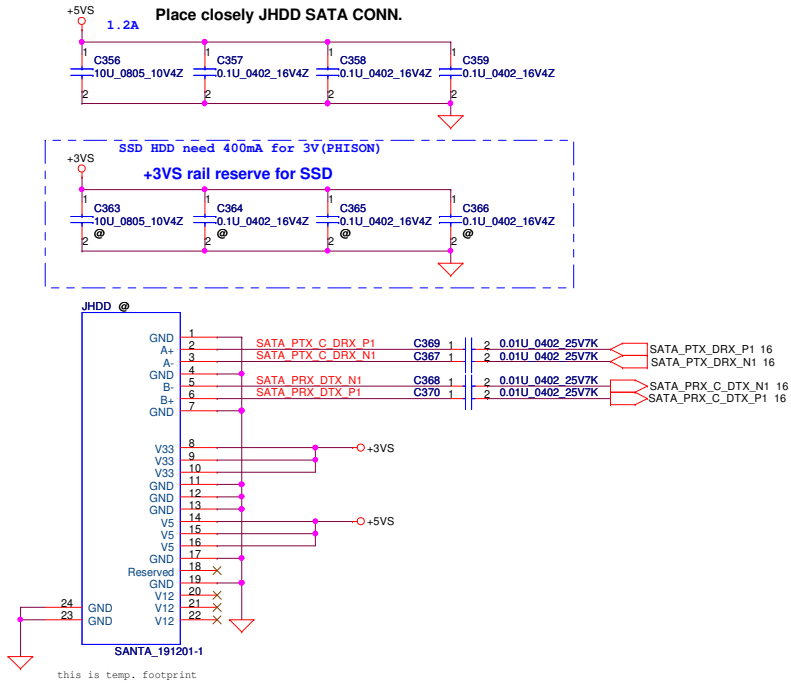
U11H		AK30	
AA19	VSS[1]	VSS[80]	AK31
AA20	VSS[2]	VSS[81]	AK32
AA22	VSS[3]	VSS[82]	AK34
AA24	VSS[4]	VSS[83]	AK35
AA26	VSS[5]	VSS[84]	AK38
AA28	VSS[6]	VSS[85]	AK43
AA30	VSS[7]	VSS[86]	AK44
AA31	VSS[8]	VSS[87]	AK45
AA32	VSS[9]	VSS[88]	AK49
AB11	VSS[10]	VSS[89]	AK5
AB15	VSS[11]	VSS[90]	AK8
AB23	VSS[12]	VSS[91]	AL2
AB30	VSS[13]	VSS[92]	AL52
AB31	VSS[14]	VSS[93]	AM11
AB32	VSS[15]	VSS[94]	BM44
AB39	VSS[16]	VSS[95]	AD24
AB43	VSS[17]	VSS[96]	AM20
AB47	VSS[18]	VSS[97]	AM22
AB5	VSS[19]	VSS[98]	AM24
AB5	VSS[20]	VSS[99]	AM26
AB5	VSS[21]	VSS[100]	AM28
AC2	VSS[22]	VSS[101]	BA42
AC52	VSS[23]	VSS[102]	AM30
AD11	VSS[24]	VSS[103]	AM31
AD12	VSS[25]	VSS[104]	AM32
AD16	VSS[26]	VSS[105]	AM34
AD23	VSS[27]	VSS[106]	AM35
AD30	VSS[28]	VSS[107]	AM38
AD31	VSS[29]	VSS[108]	AM39
AD32	VSS[30]	VSS[109]	AM42
AD34	VSS[31]	VSS[110]	AU20
AU22	VSS[32]	VSS[111]	AM46
AD42	VSS[33]	VSS[112]	AV22
AD46	VSS[34]	VSS[113]	AM49
T12	VSS[35]	VSS[114]	AM7
AD7	VSS[36]	VSS[115]	AM7
AE2	VSS[37]	VSS[116]	AA50
AE4	VSS[38]	VSS[117]	BB10
AE12	VSS[39]	VSS[118]	AN32
Y13	VSS[40]	VSS[119]	AN50
AA49	VSS[41]	VSS[120]	AN52
AF35	VSS[42]	VSS[121]	AP12
AP13	VSS[43]	VSS[122]	AP2
AN34	VSS[44]	VSS[123]	AP46
AF45	VSS[45]	VSS[124]	AP49
AF46	VSS[46]	VSS[125]	AP5
AF49	VSS[47]	VSS[126]	AP8
AE5	VSS[48]	VSS[127]	AP82
AF8	VSS[49]	VSS[128]	AT11
AG2	VSS[50]	VSS[129]	AT128
AG52	VSS[51]	VSS[130]	AH48
AH11	VSS[52]	VSS[131]	AT32
AH15	VSS[53]	VSS[132]	AT36
AH18	VSS[54]	VSS[133]	AT41
AH24	VSS[55]	VSS[134]	AT47
AH32	VSS[56]	VSS[135]	AT7
AV18	VSS[57]	VSS[136]	AV12
AH43	VSS[58]	VSS[137]	AV16
AH47	VSS[59]	VSS[138]	AV20
AH7	VSS[60]	VSS[139]	AV24
AJ19	VSS[61]	VSS[140]	AV30
AJ2	VSS[62]	VSS[141]	AV34
AJ20	VSS[63]	VSS[142]	AV38
AJ22	VSS[64]	VSS[143]	AV42
AJ23	VSS[65]	VSS[144]	AV46
AJ25	VSS[66]	VSS[145]	AV49
AJ26	VSS[67]	VSS[146]	AV5
AJ28	VSS[68]	VSS[147]	AV8
AJ32	VSS[69]	VSS[148]	AW14
AJ34	VSS[70]	VSS[149]	AW18
AT5	VSS[71]	VSS[150]	AW2
AJ4	VSS[72]	VSS[151]	AW2
AK12	VSS[73]	VSS[152]	BF9
AN41	VSS[74]	VSS[153]	AW32
AN19	VSS[75]	VSS[154]	AW36
AK26	VSS[76]	VSS[155]	AW40
AK22	VSS[77]	VSS[156]	AW52
AK23	VSS[78]	VSS[157]	AY11
AK28	VSS[79]	VSS[158]	AY43
		VSS[159]	AY47

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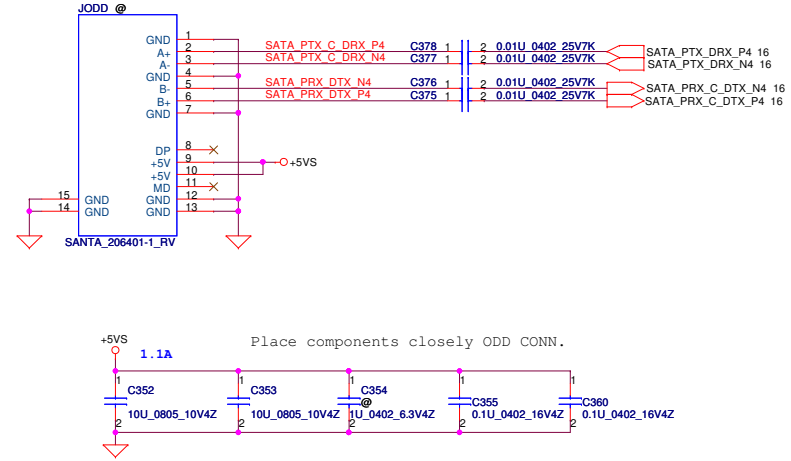
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Size	Document Number	Rev		0.2	
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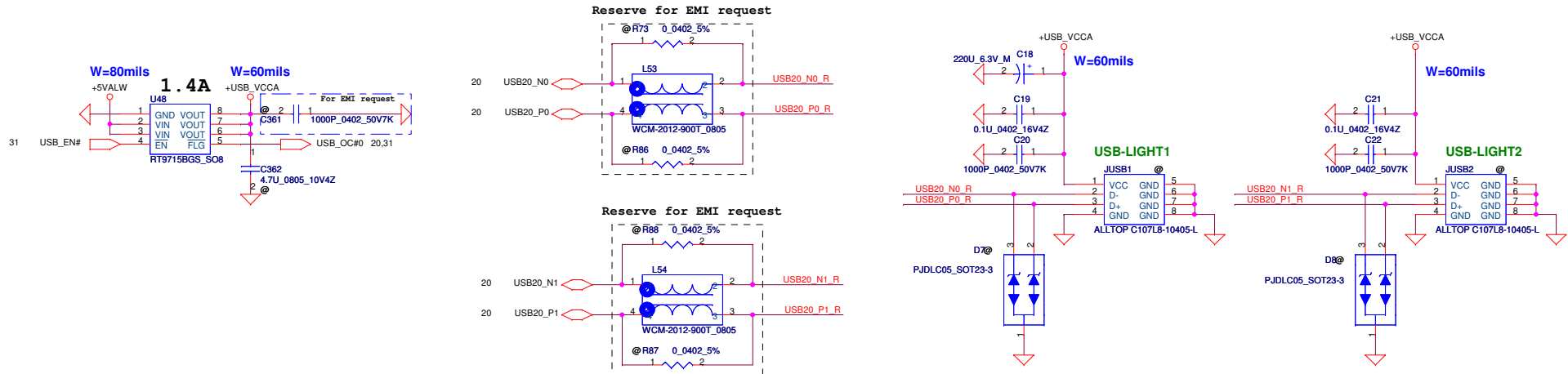
## SATA HDD Conn.



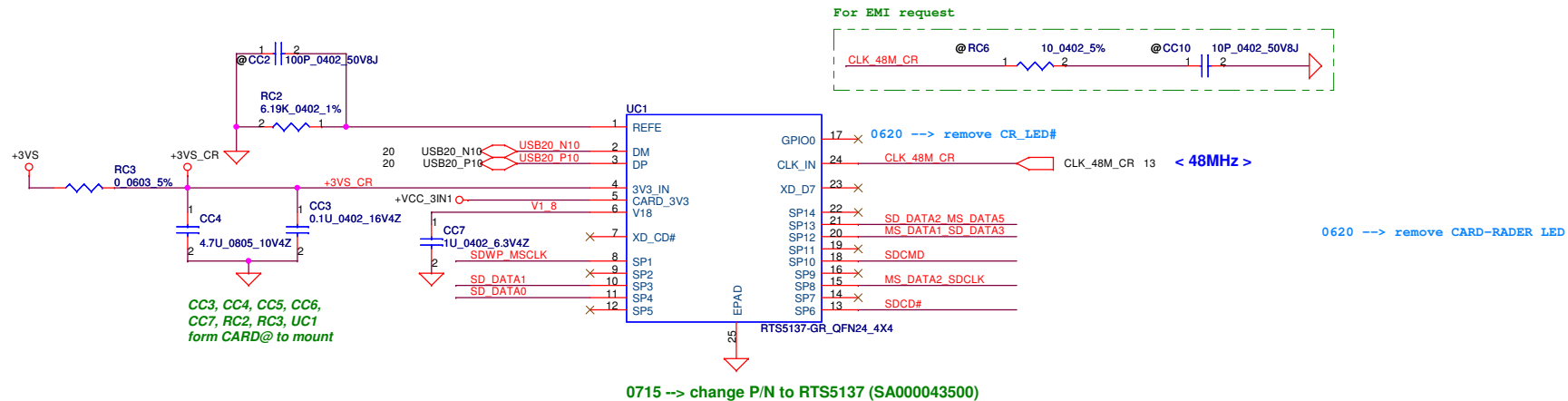
## SATA ODD Conn



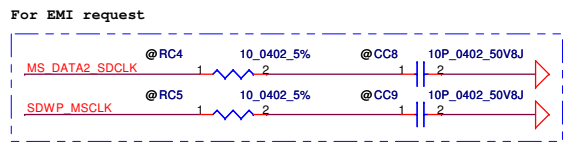
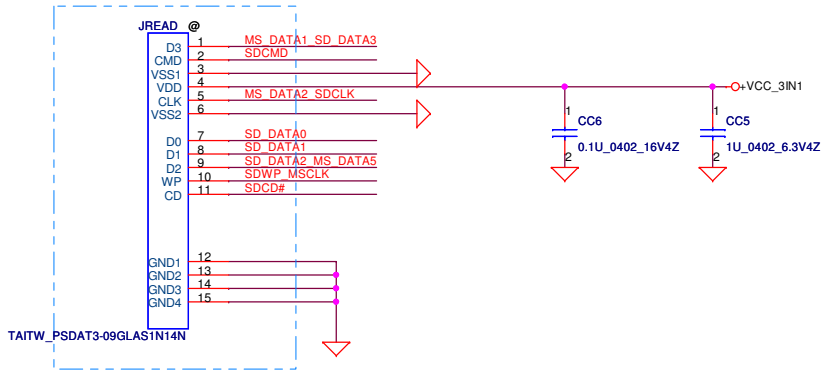
## USB Conn. (2 Port)



Security Classification		Compal Secret Data		Title	
Issued Date	2010/06/21	Deciphered Date	2011/06/21	SATA-HDD/ODD/USB	
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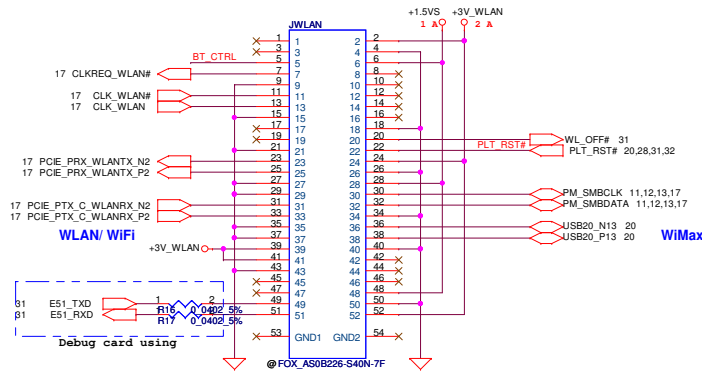
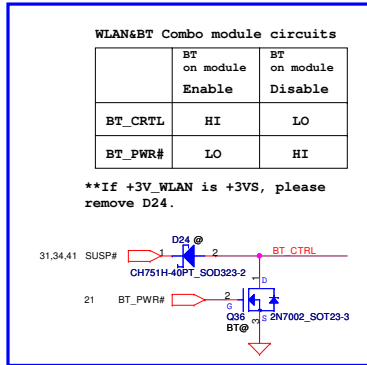


< 2 in 1 Card Reader >  
 0624 --> change CARDREADER conn.

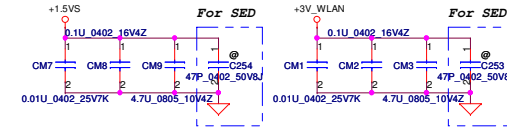
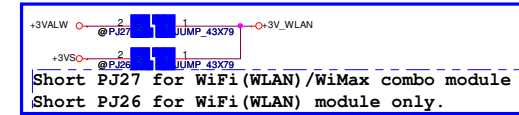


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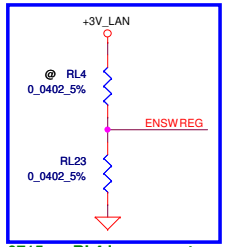
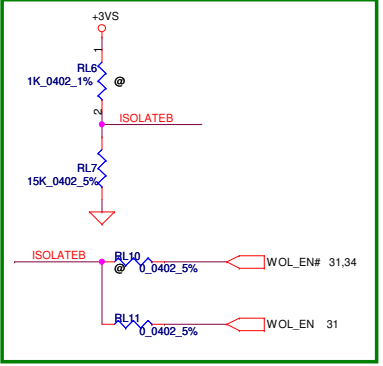
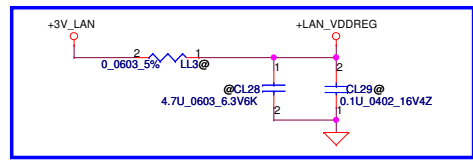
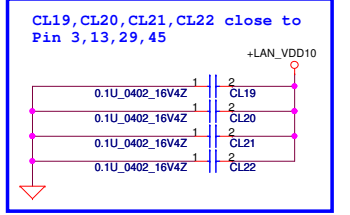
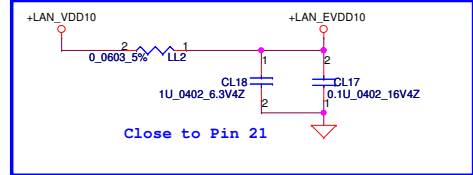
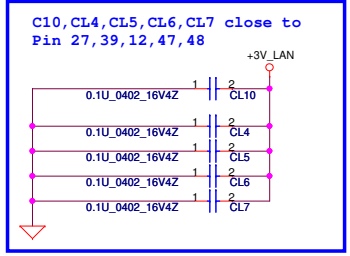
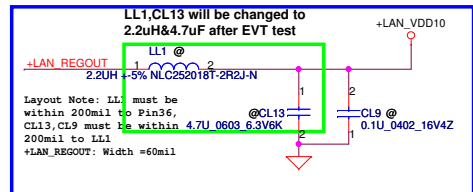
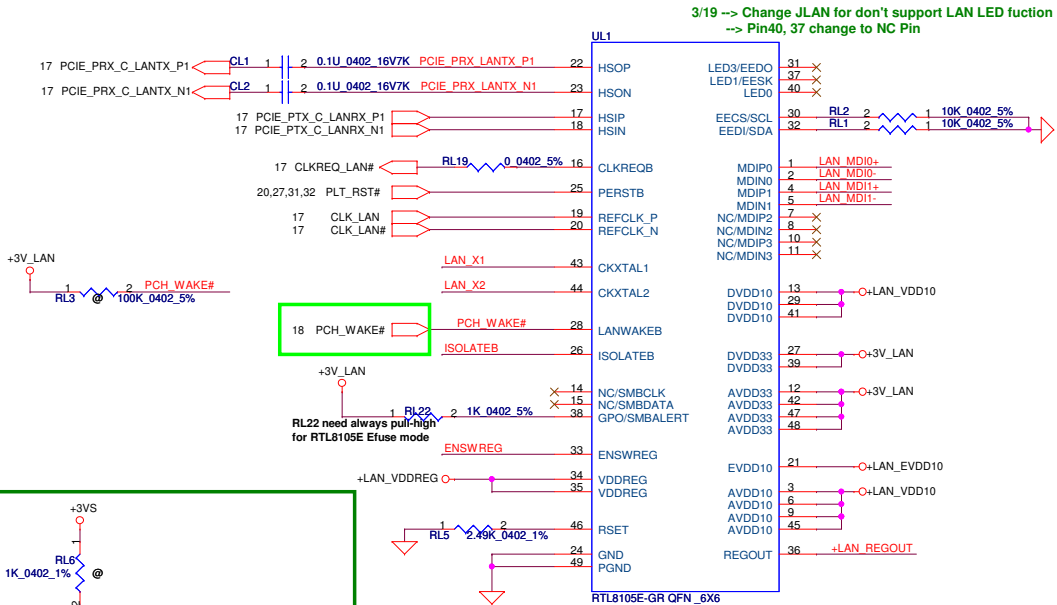
# PCIe Mini Card-WLAN/WiMax



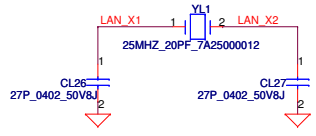
## Slot#1 Half PCIe Mini Card-WLAN/WiMax



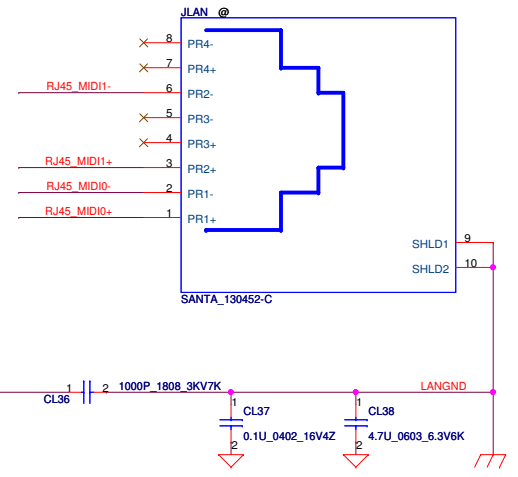
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Issued Date	2010/06/21	Deciphered Date	2011/06/21	
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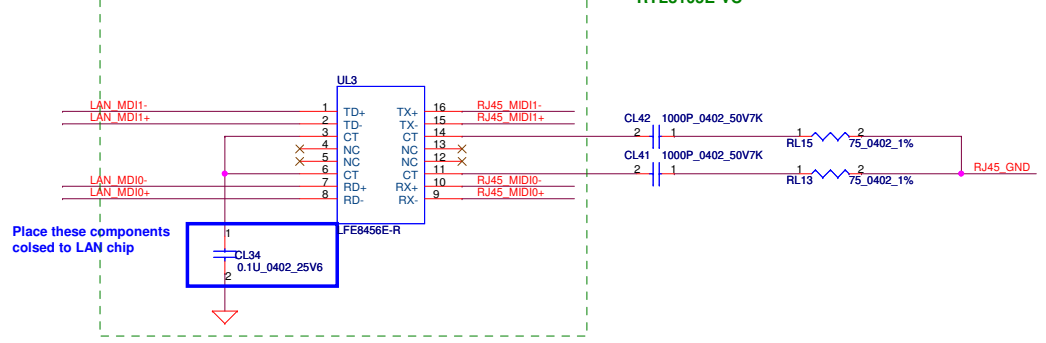
4/2->remove RL8, RL9, CL11



LAN Conn.

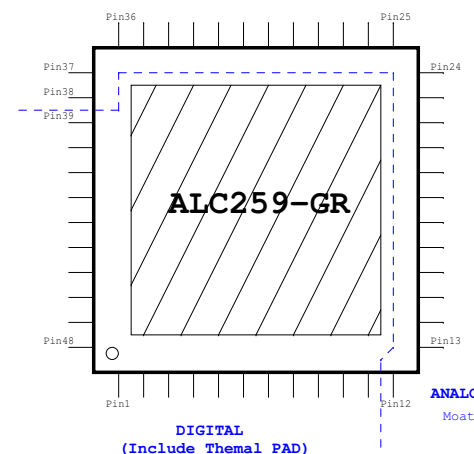
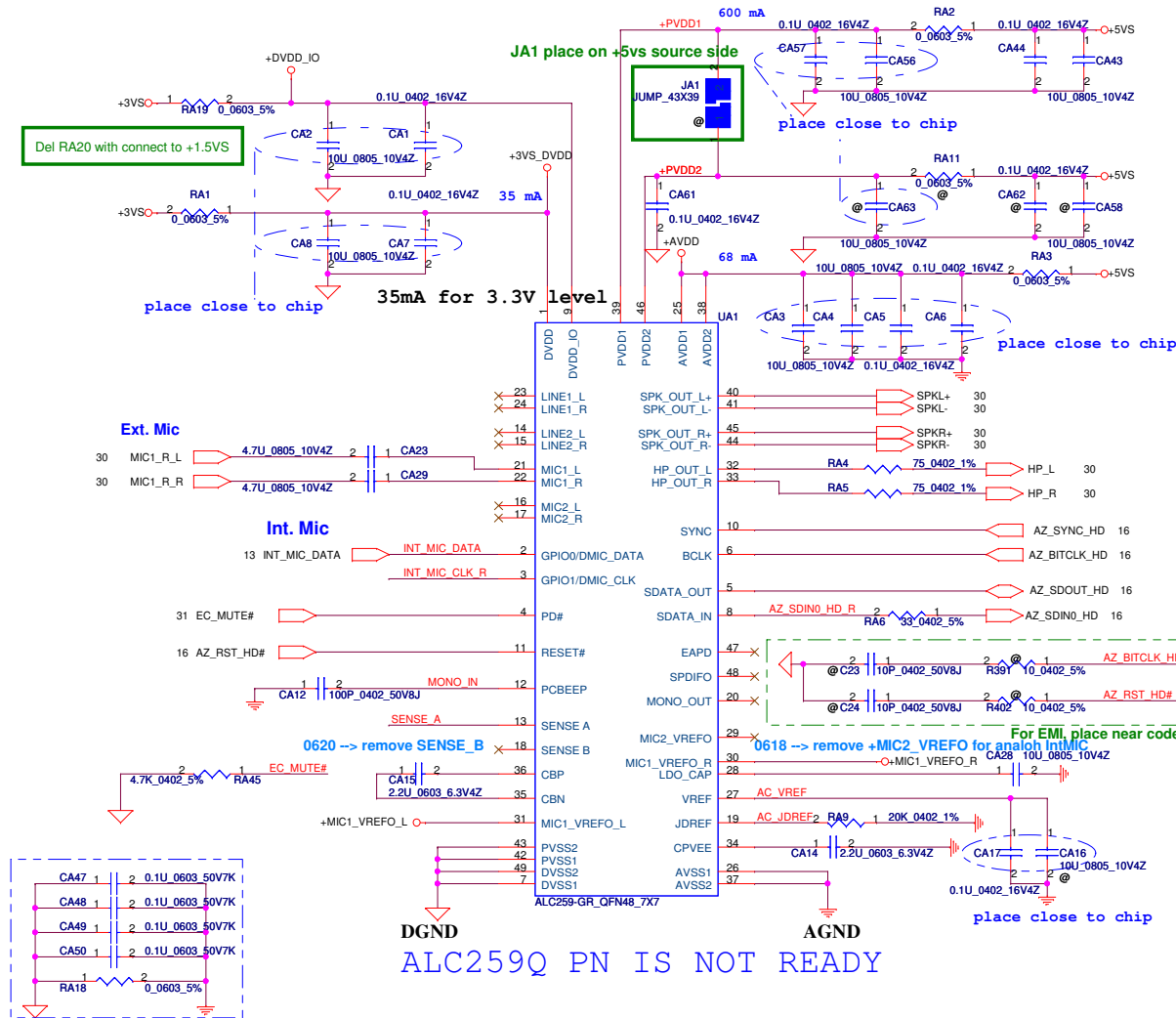


3/29 --> swap Line and PHY signal

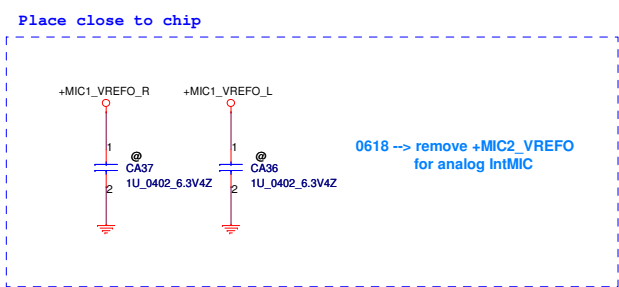
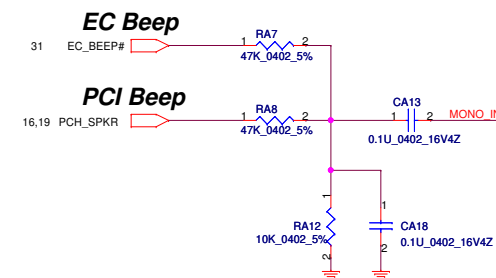


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Size Custom	Document Number	Rev		0.2
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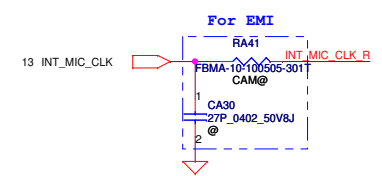
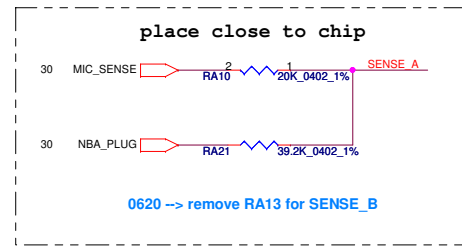
# Codec



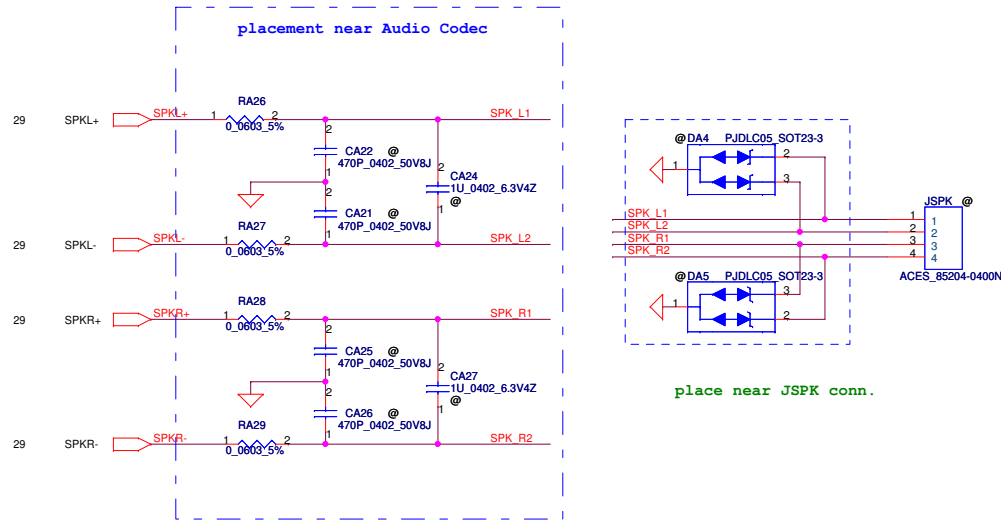
## Beep sound



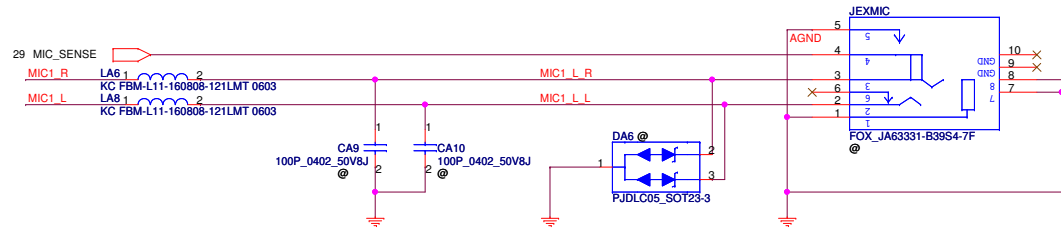
Sense Pin	Impedance	Codec Signals	Function
SENSE A	39.2K	PORT-I (PIN 32, 33)	Headphone out
	20K	PORT-B (PIN 21, 22)	Ext. MIC
	10K	PORT-C (PIN 23, 24)	
	5.1K	(PIN 48)	
	39.2K	PORT-E (PIN 14, 15)	



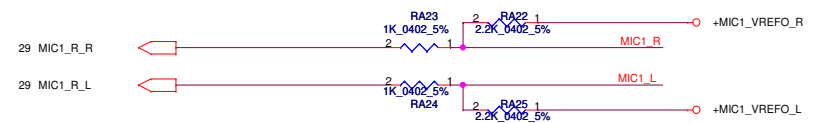
# Speaker Connector



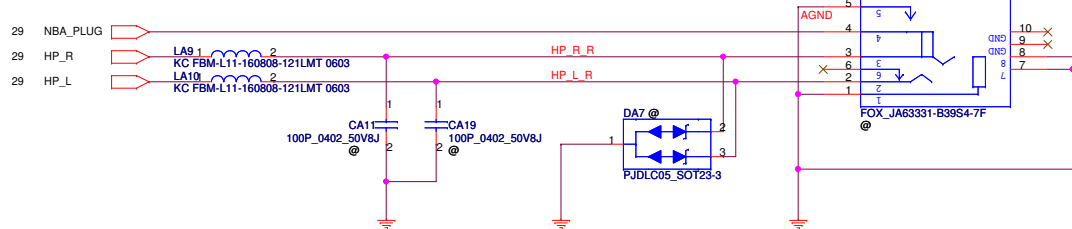
# Ex.MIC JACK



# Ext.MIC/LINE IN



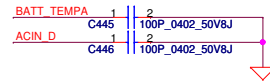
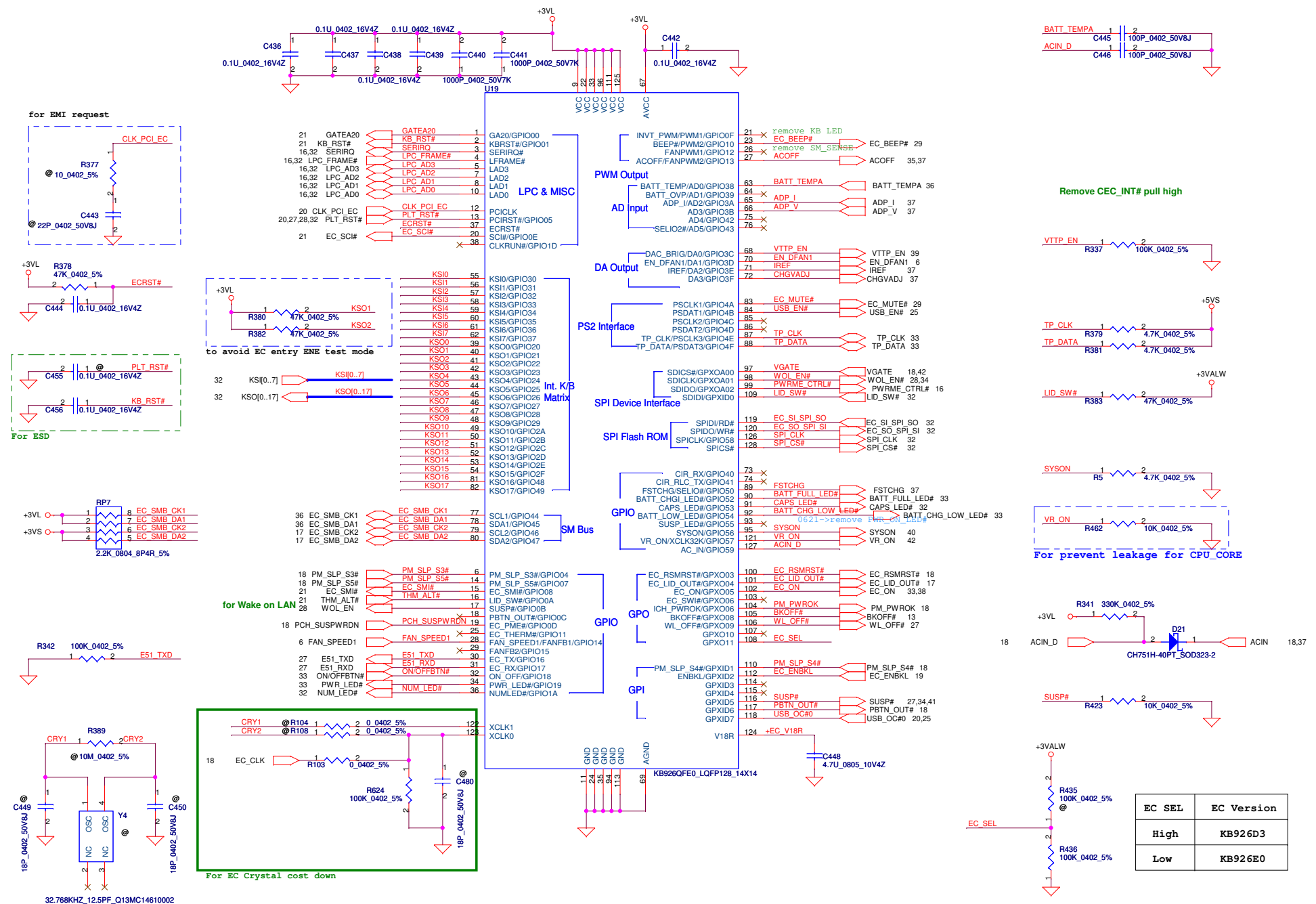
# Head Phone JACK



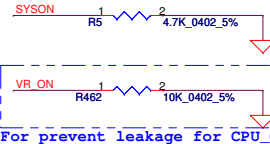
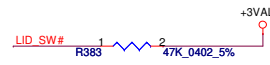
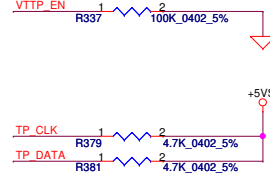
# Int. Mic

0618 --> remove Analog IntMIC, and change to DIGITAL MIC

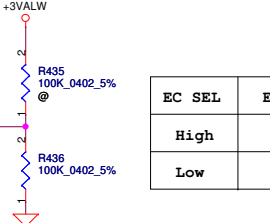
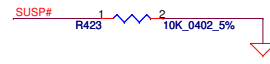
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Remove CEC\_INT# pull high



For prevent leakage for CPU\_CORE

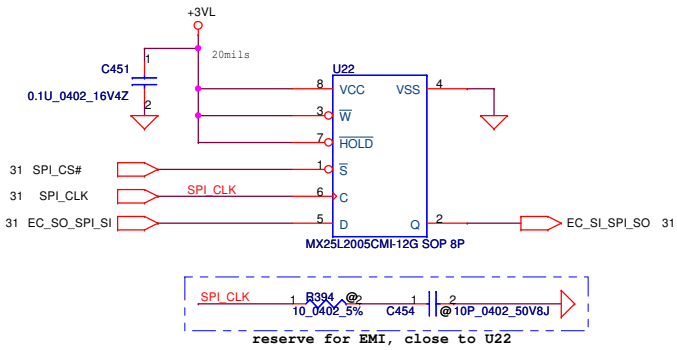


EC SEL	EC Version
High	KB926D3
Low	KB926E0

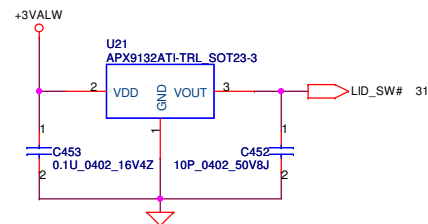
Remove PM\_SLP\_S4#/S5# AND Gate

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# SPI Flash (256KB)

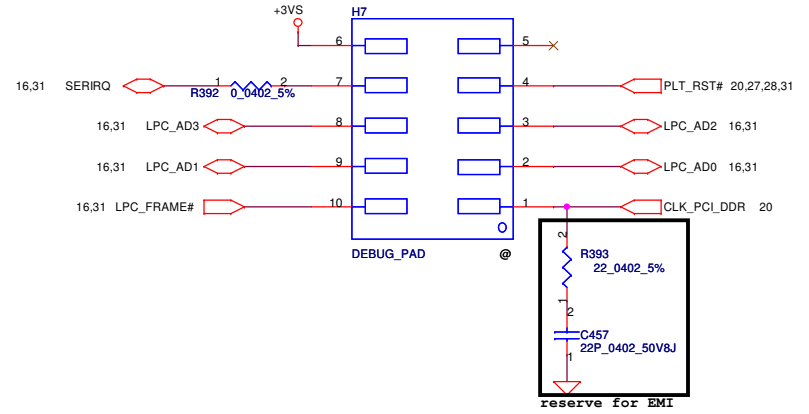


# Lid SW



# LPC Debug Port

Please place the PAD under DDR DIMM.



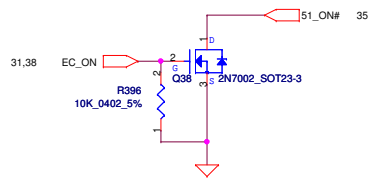
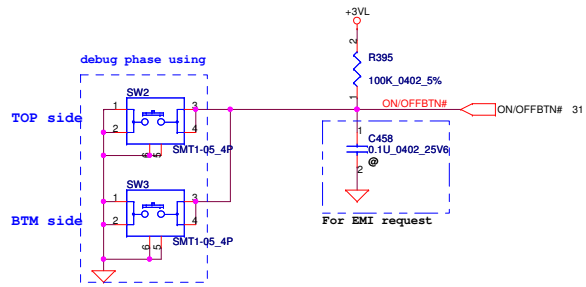
# KEYBOARD CONN.



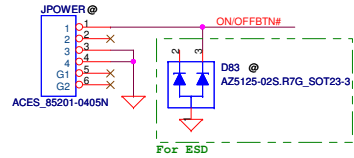
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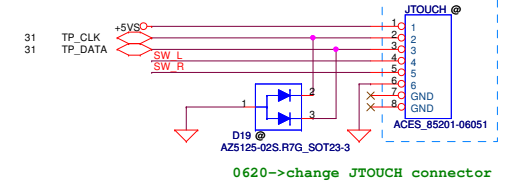
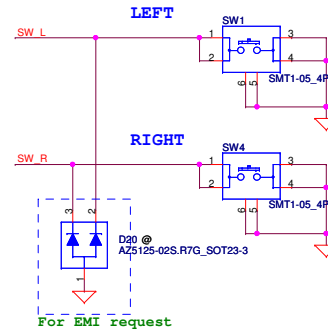
### Power Button



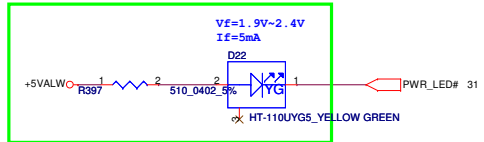
### PWR/B to MB Conn.



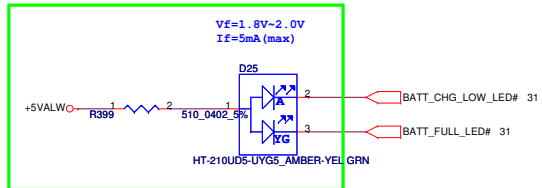
### TP Button/Conn.



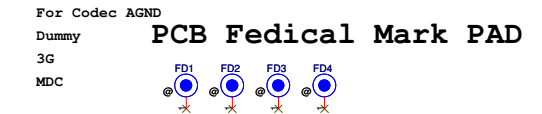
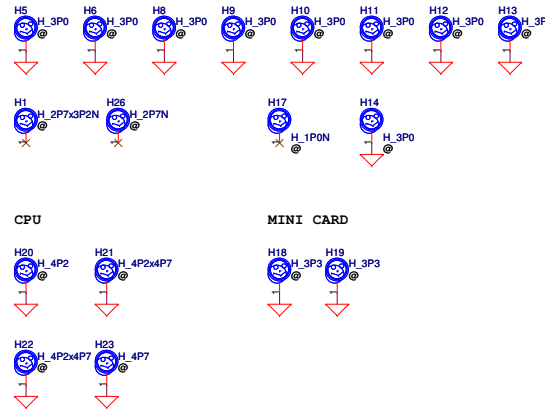
### POWER/SUSPEND LED



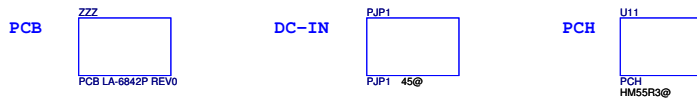
### BATT CHARGE/FULL LED



### Screw Hole

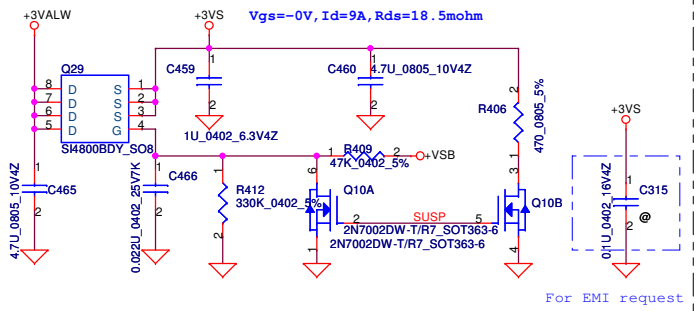


### ISPD

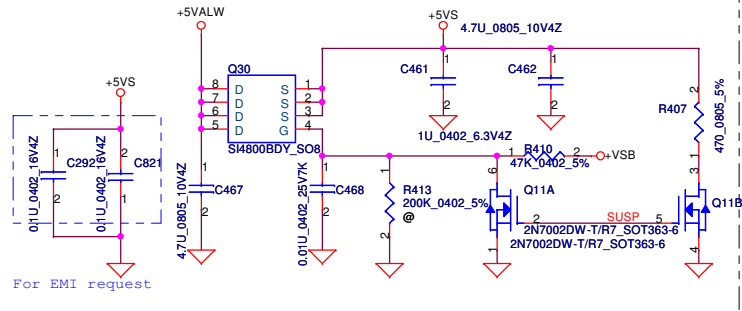


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Title	PWR BTN/Can. Sensor/TP/LEDs			
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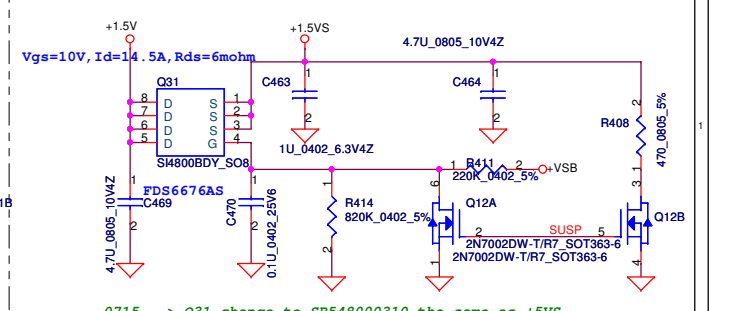
**+3VALW TO +3VS**



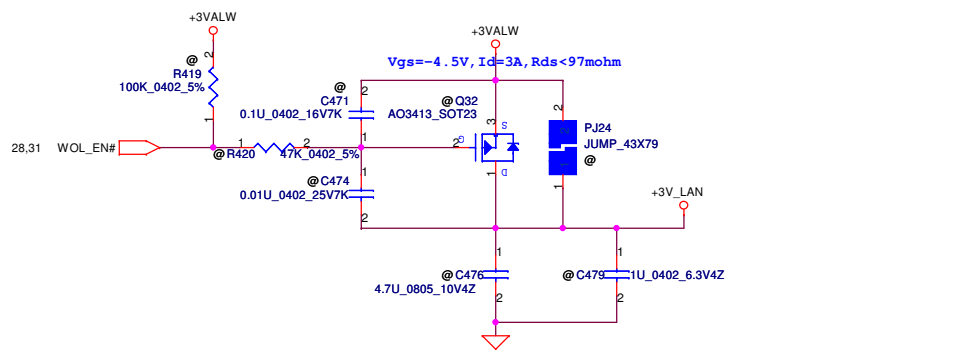
**+5VALW TO +5VS**



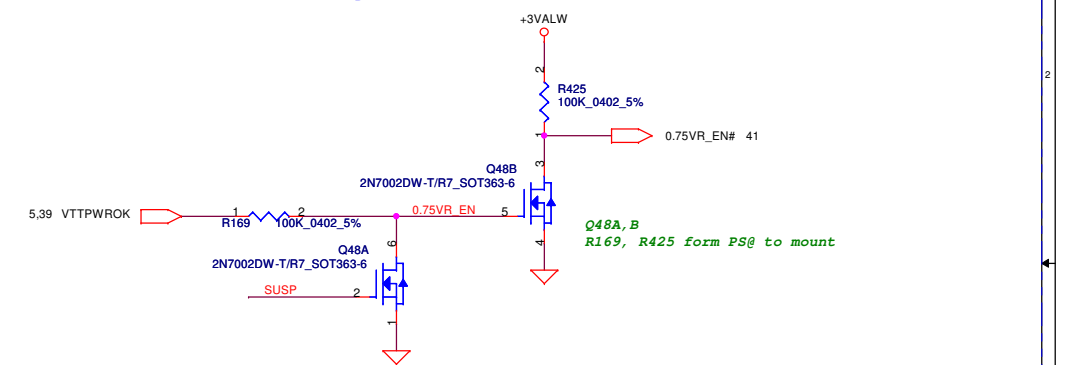
**+1.5V to +1.5VS**



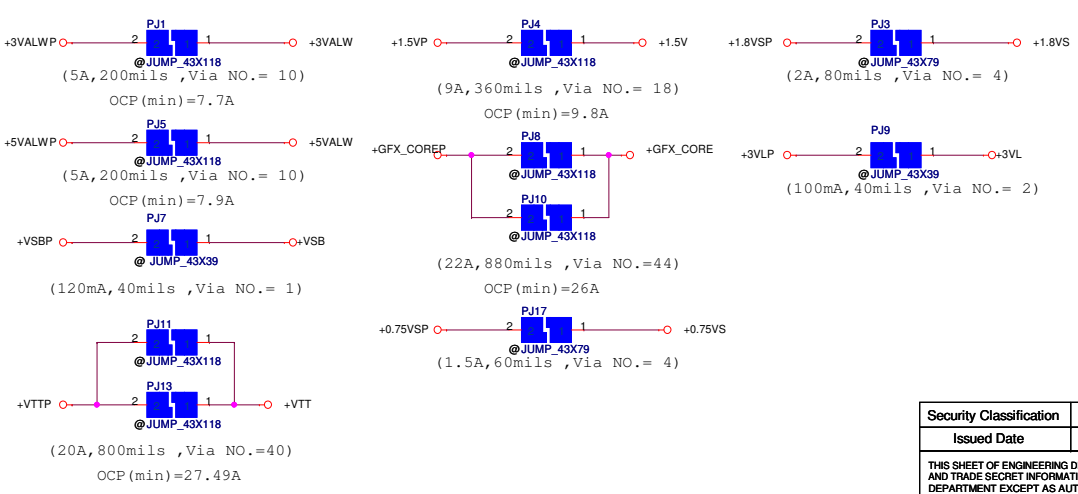
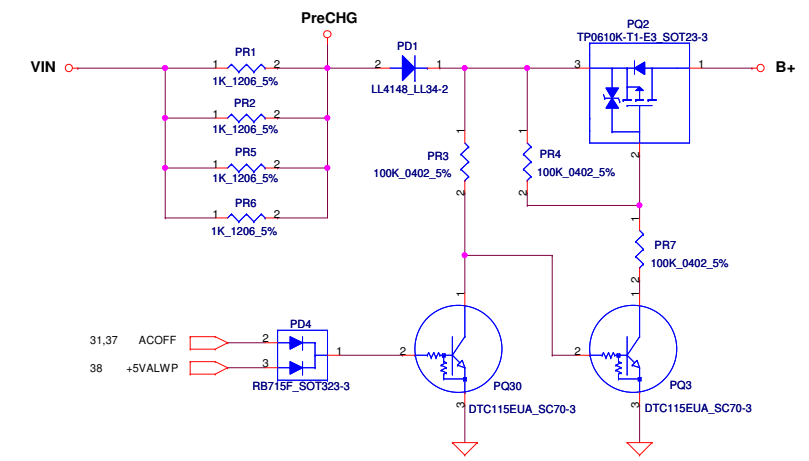
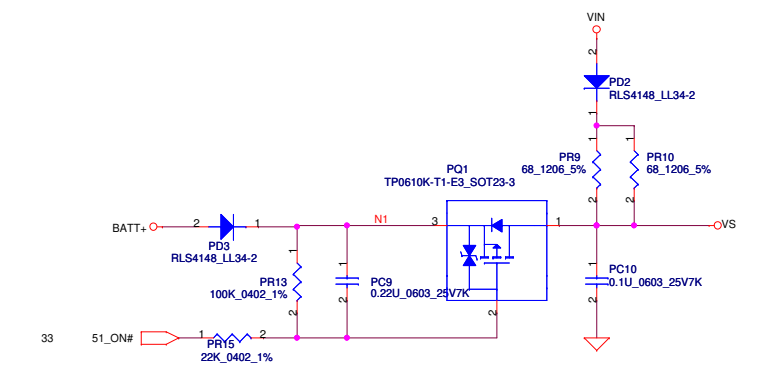
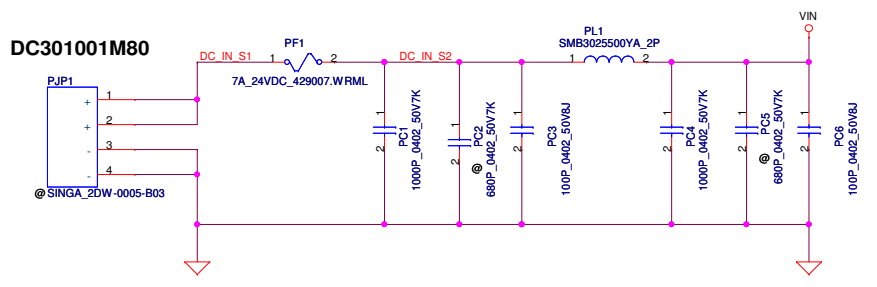
**+3VALW TO +3V\_LAN**



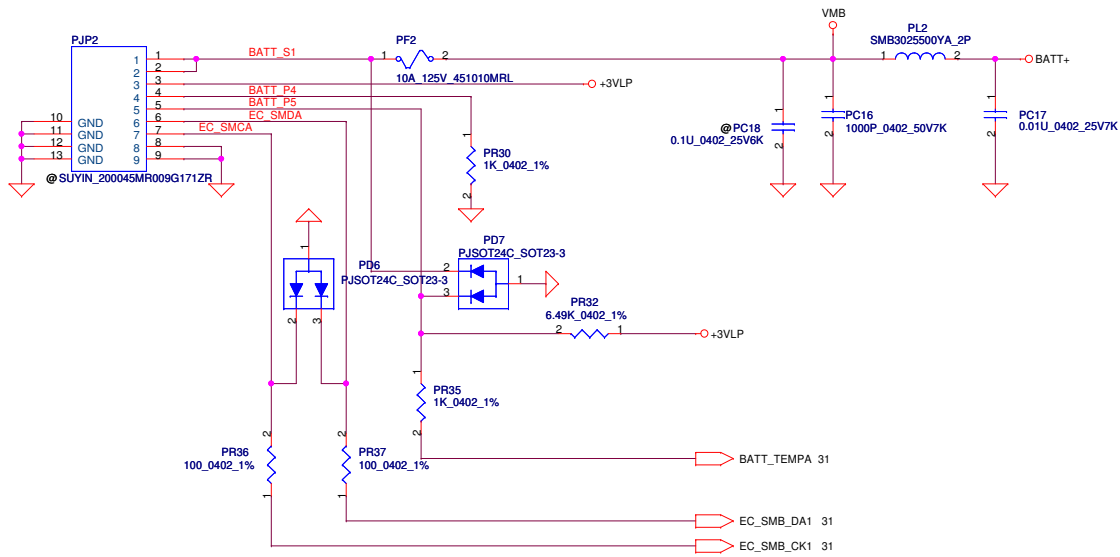
**For S3 CPU Power Saving**



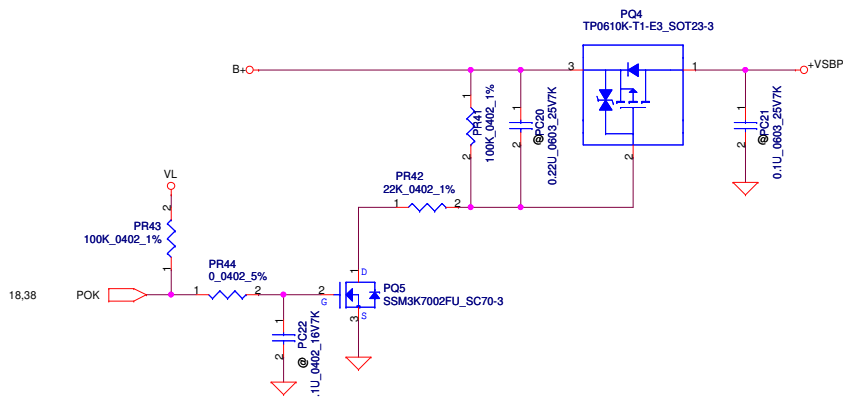
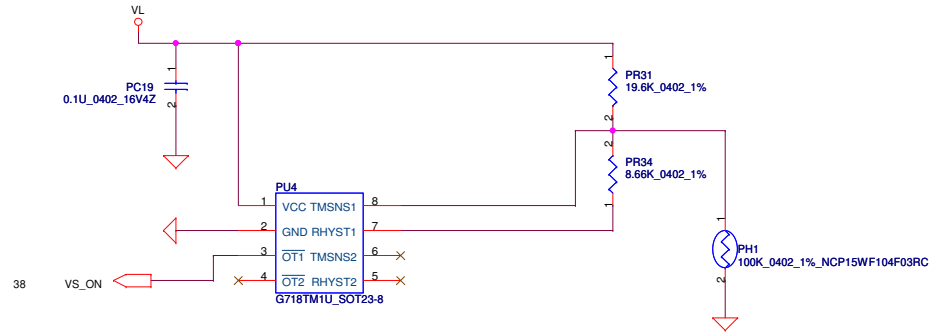
**DC301001M80**



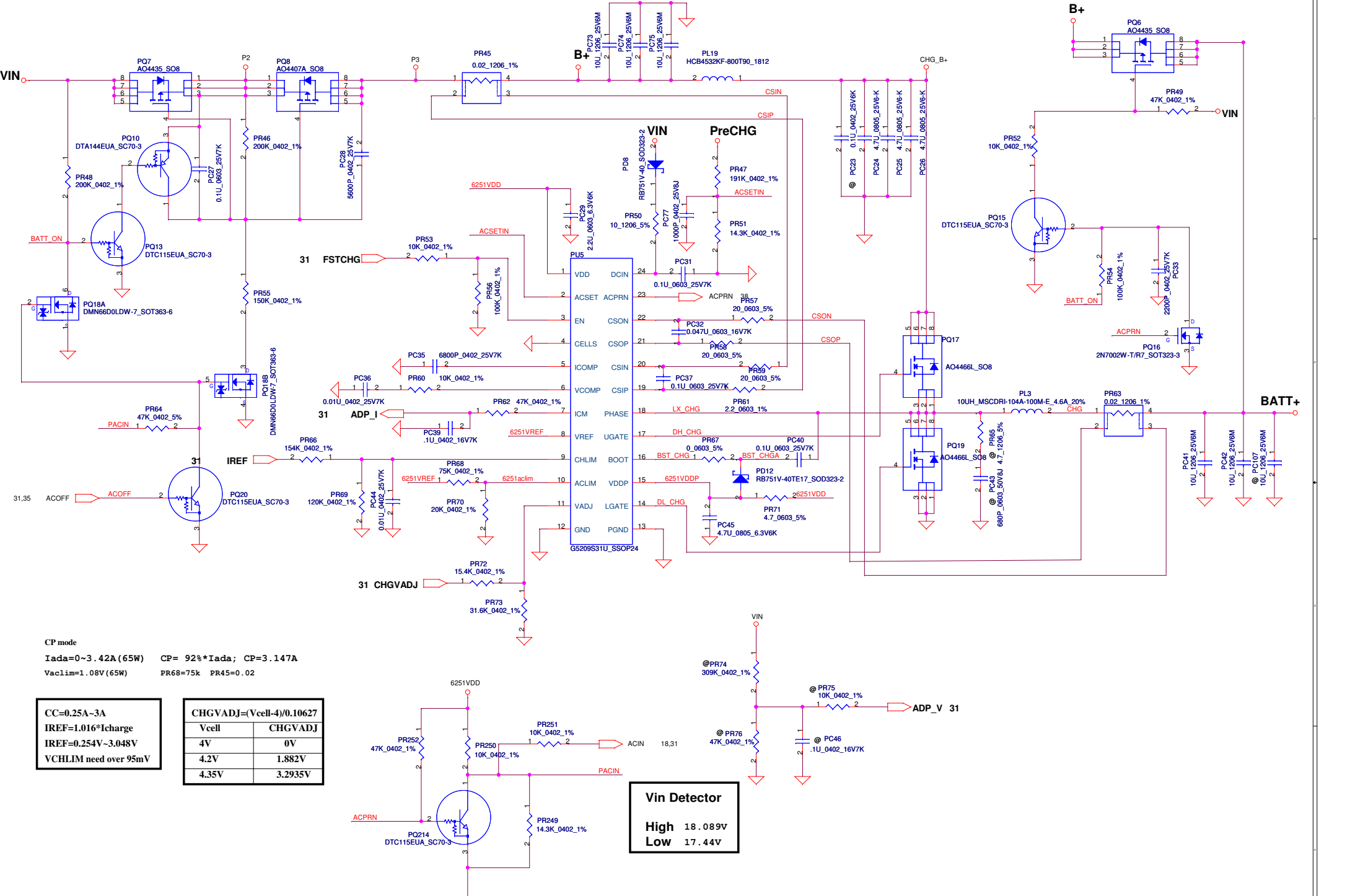
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								DCIN / DETECTOR
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PH1 under CPU botten side :  
 CPU thermal protection at 95degree C  
 Recovery at 56 degree C



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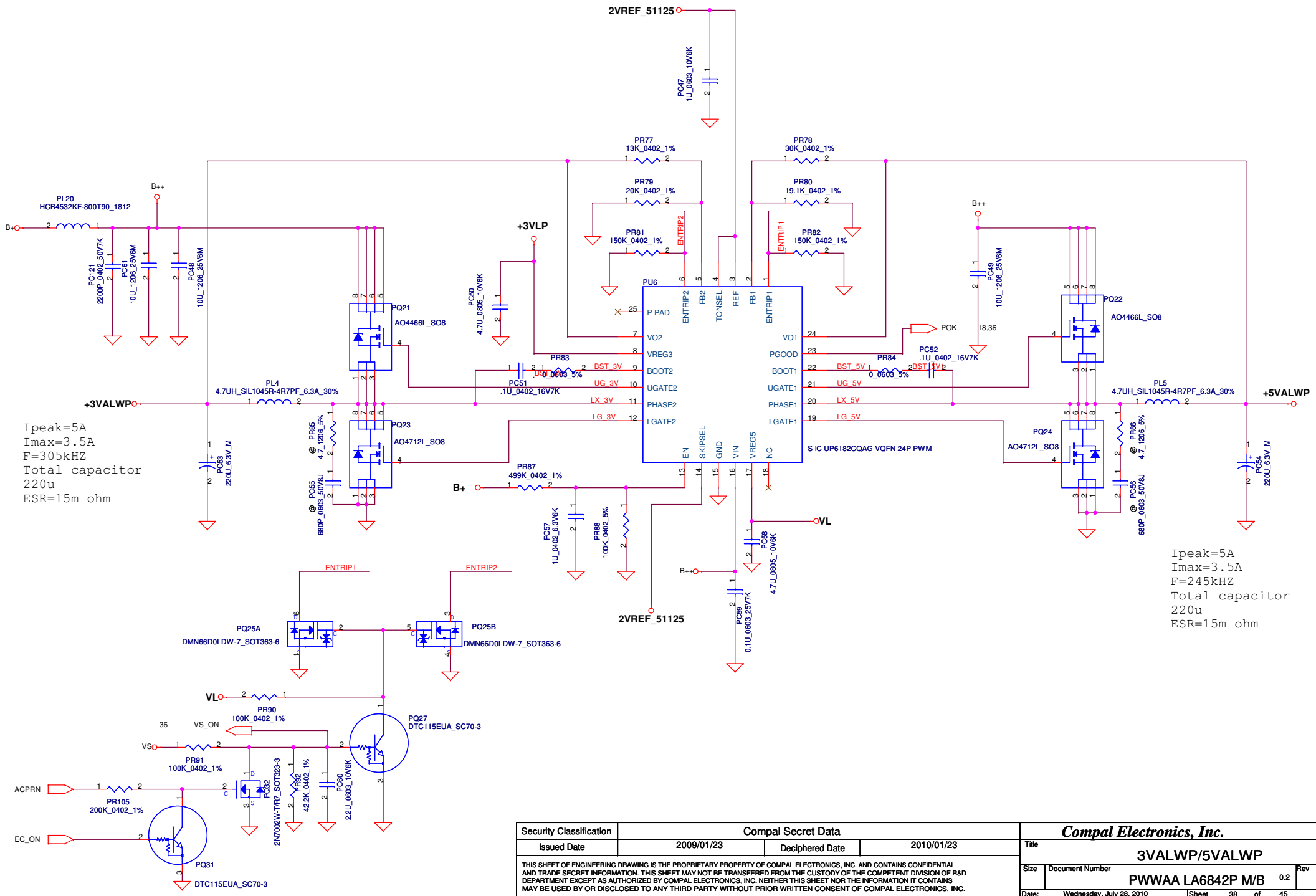


CP mode  
 $I_{ada} = 0 \sim 3.42A (65W)$  CP =  $92\% * I_{ada}$ ; CP = 3.147A  
 $V_{acLim} = 1.08V (65W)$  PR68 = 75k PR45 = 0.02

CC = 0.25A ~ 3A  
 $I_{REF} = 1.016 * I_{charge}$   
 $I_{REF} = 0.254V \sim 3.048V$   
 VCHLIM need over 95mV

CHGVADJ = $(V_{cell} - 4) / 0.10627$	
V <sub>cell</sub>	CHGVADJ
4V	0V
4.2V	1.882V
4.35V	3.2935V

**Vin Detector**  
 High 18.089V  
 Low 17.44V

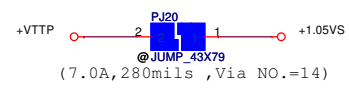
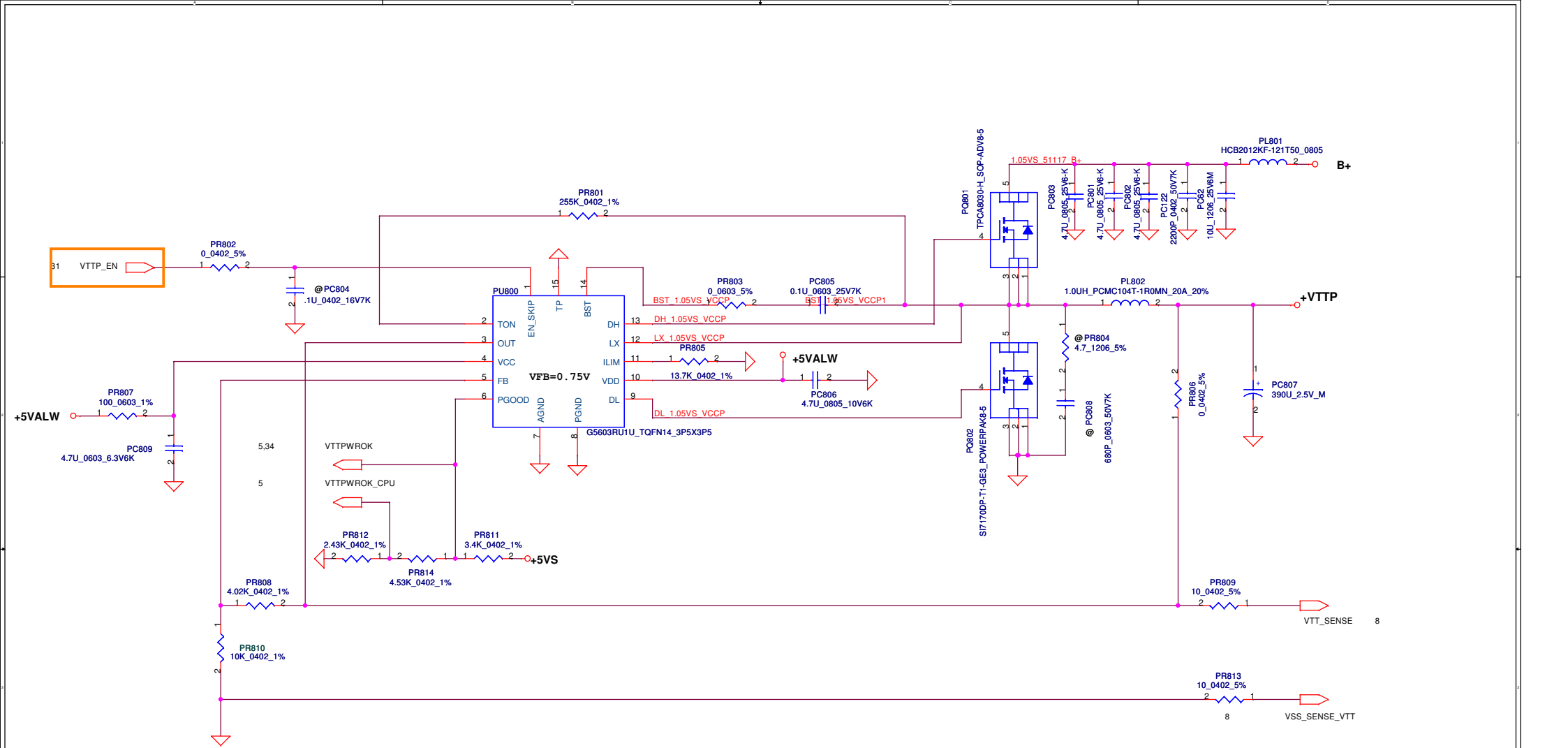


$I_{peak}=5A$   
 $I_{max}=3.5A$   
 $F=305kHz$   
 Total capacitor  
 220u  
 ESR=15m ohm

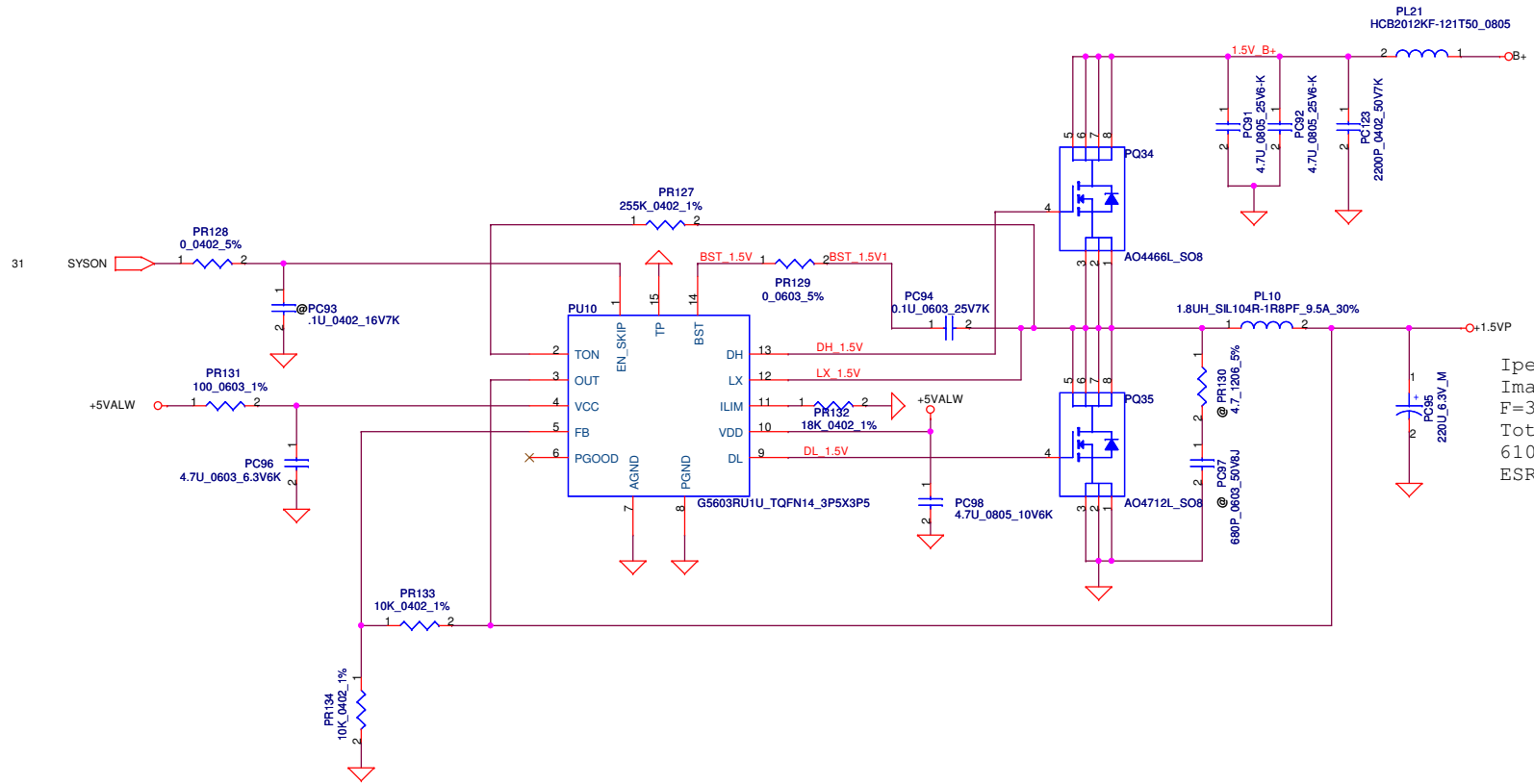
$I_{peak}=5A$   
 $I_{max}=3.5A$   
 $F=245kHz$   
 Total capacitor  
 220u  
 ESR=15m ohm

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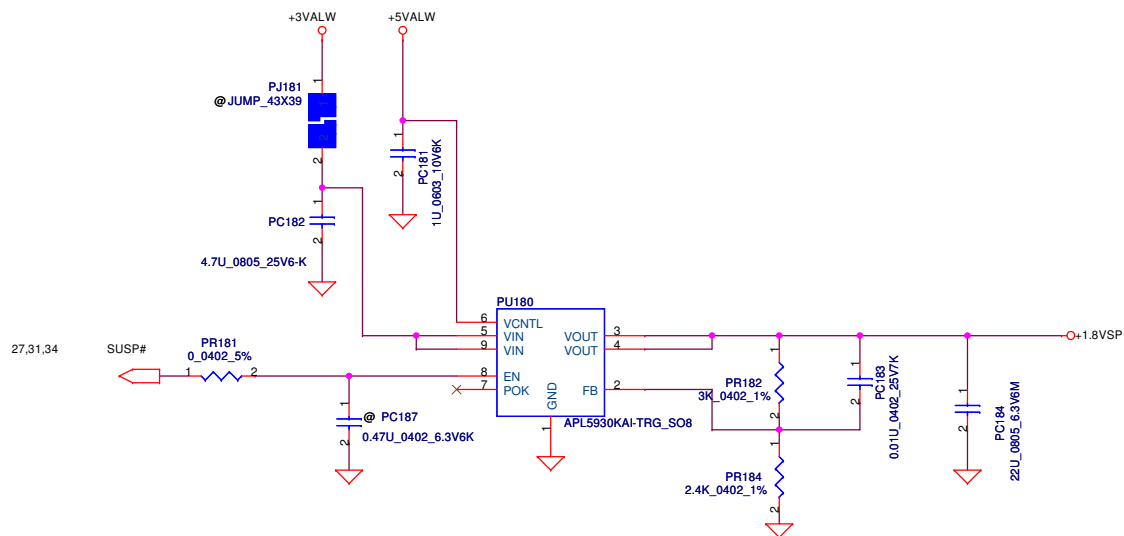
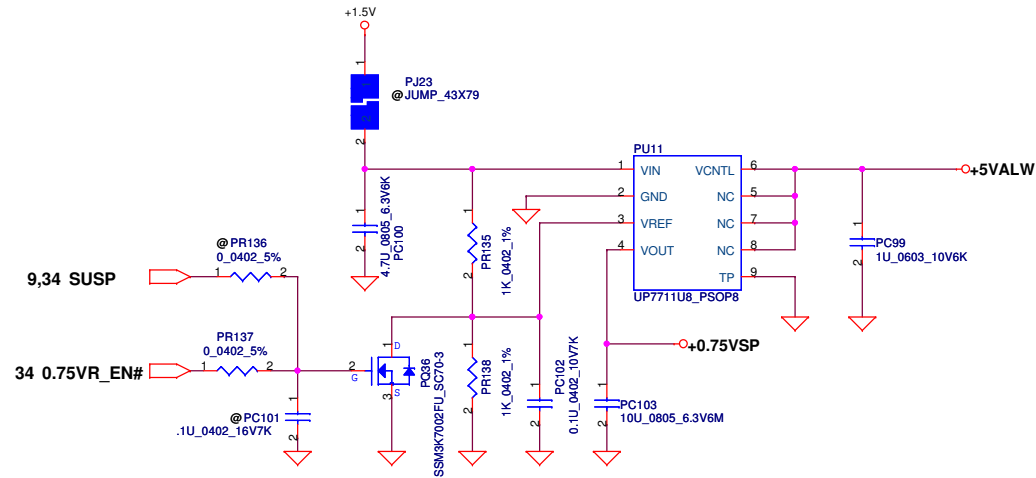
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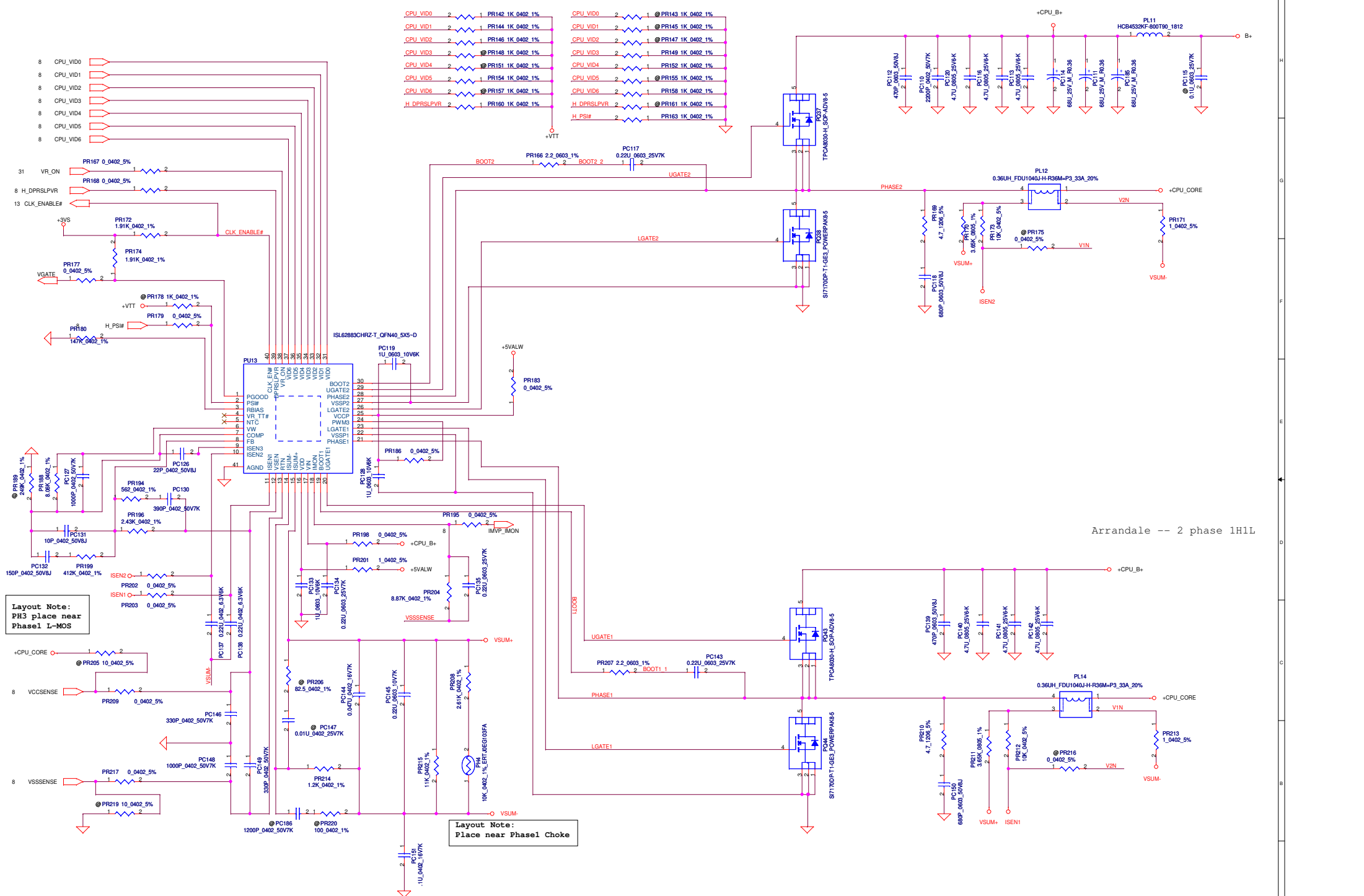
$I_{peak}=9A$   
 $I_{max}=6.3A$   
 $F=313kHz$   
 Total capacitor  
 610u  
 $ESR=5m\ \Omega$

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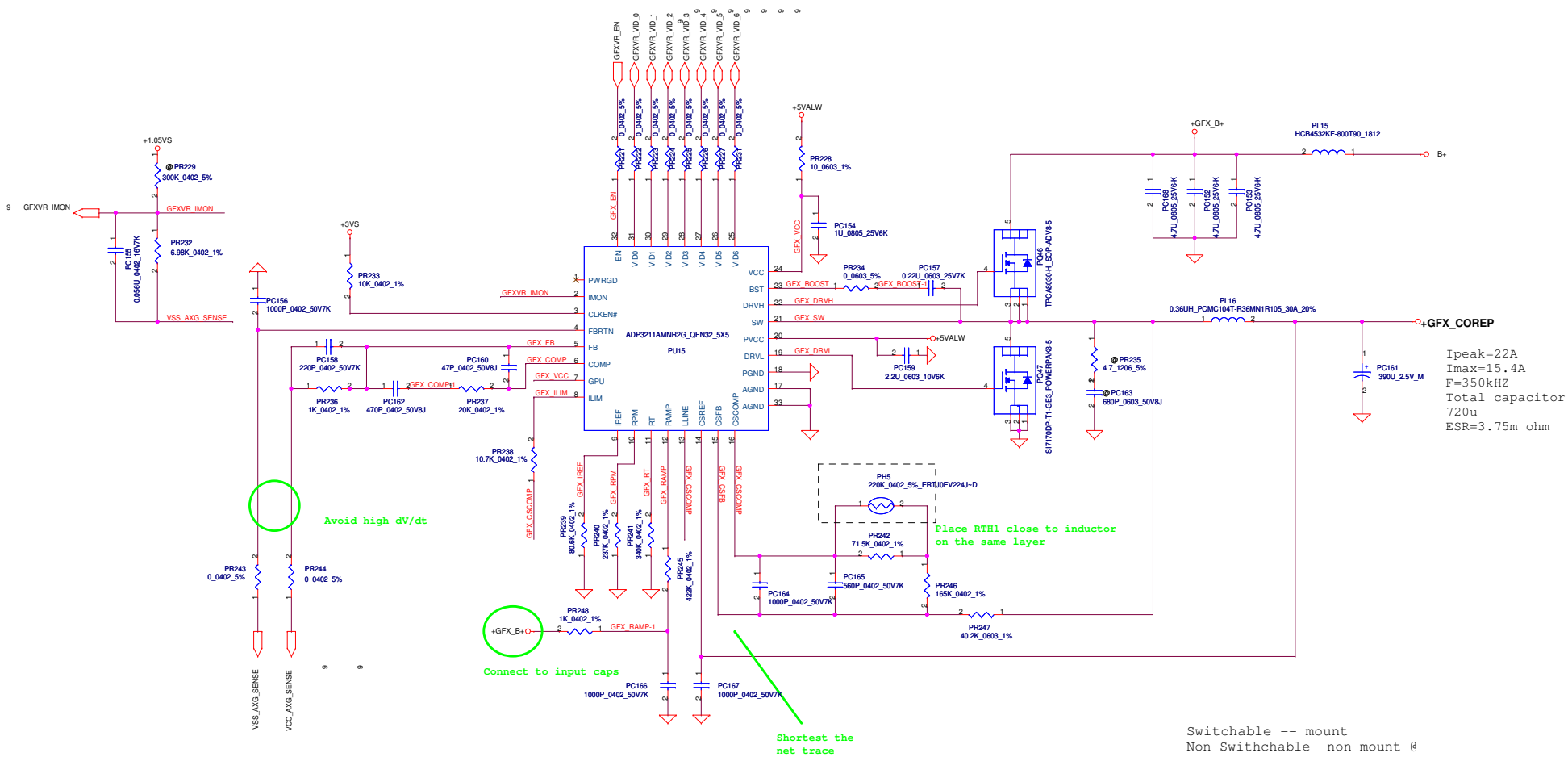


Arrandale -- 2 phase 1H1L

Layout Note:  
PH3 place near  
Phasel L-MOS

Layout Note:  
Place near Phasel Choke

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I<sub>peak</sub>=22A  
 I<sub>max</sub>=15.4A  
 F=350kHz  
 Total capacitor  
 720u  
 ESR=3.75m ohm

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NO	DATE	PAGE	MODIFICATION LIST	PURPOSE
2010/07/13		42	Change PL12,PL14 to SH00000IN00	BOM modify
2010/07/13		43	Change PL16 to SH00000IN00	BOM modify
2010/07/23		36	Change PC19 to SE070104Z80	BOM modify
2010/07/26		36	Add PD6,PD7	EMI request
2010/07/26		37	Add PC73,PC74,PC75(10U_1206)	EMI request
2010/07/26		38	Add PC121(2200P_0402),PC61(10U_1206)	EMI request
2010/07/26		39	Add PC122(2200P_0402),PC62(10U_1206)	EMI request
2010/07/26		40	Add PC123(2200P_0402)	EMI request

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				Size	Document Number
				PWWAA LA6842P M/B	
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				Sheet	44 of 45
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**PIR (Product Improve Record)**

PWWAA LA-6842P SCHEMATIC CHANGE LIST

REVISION CHANGE: 0.1 TO 0.2

GERBER-OUT DATE: 2010/07/31

NO DATE PAGE MODIFICATION LIST

PURPOSE

1. 20100714 / Page13 --> add 10u Cap to +1.5VS\_CK505 For eSATA transmit issue ---> not add 10u Cap into schematic yet

NWQAA LA-6061P SCHEMATIC CHANGE LIST

REVISION CHANGE: 1.0 TO 2.0

GERBER-OUT DATE: 2010/03/19

NO DATE PAGE MODIFICATION LIST

PURPOSE

NO	DATE	PAGE	MODIFICATION LIST	PURPOSE
1	3/17	29	Change cardreader to JMB385/389	For customer request
2	3/18	31	Remove D86	For ESD request
3	3/18	22	Add R52	For CRT wave issue
4	3/19	22	Change L12 to 2.2 ohm	For CRT wave issue
5	3/22	15	Add D54	For HDMI CEC issue
6	3/24	13	Change C213 to 1U	For NALAA ESATA performance low issue

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Issued Date	2010/06/21	Deciphered Date	2011/06/21	Title	
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				Size	Document Number
Custom	PWWAA LA6842P M/B	0.2			
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