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Schematics Document

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Title: ***Cover Page***

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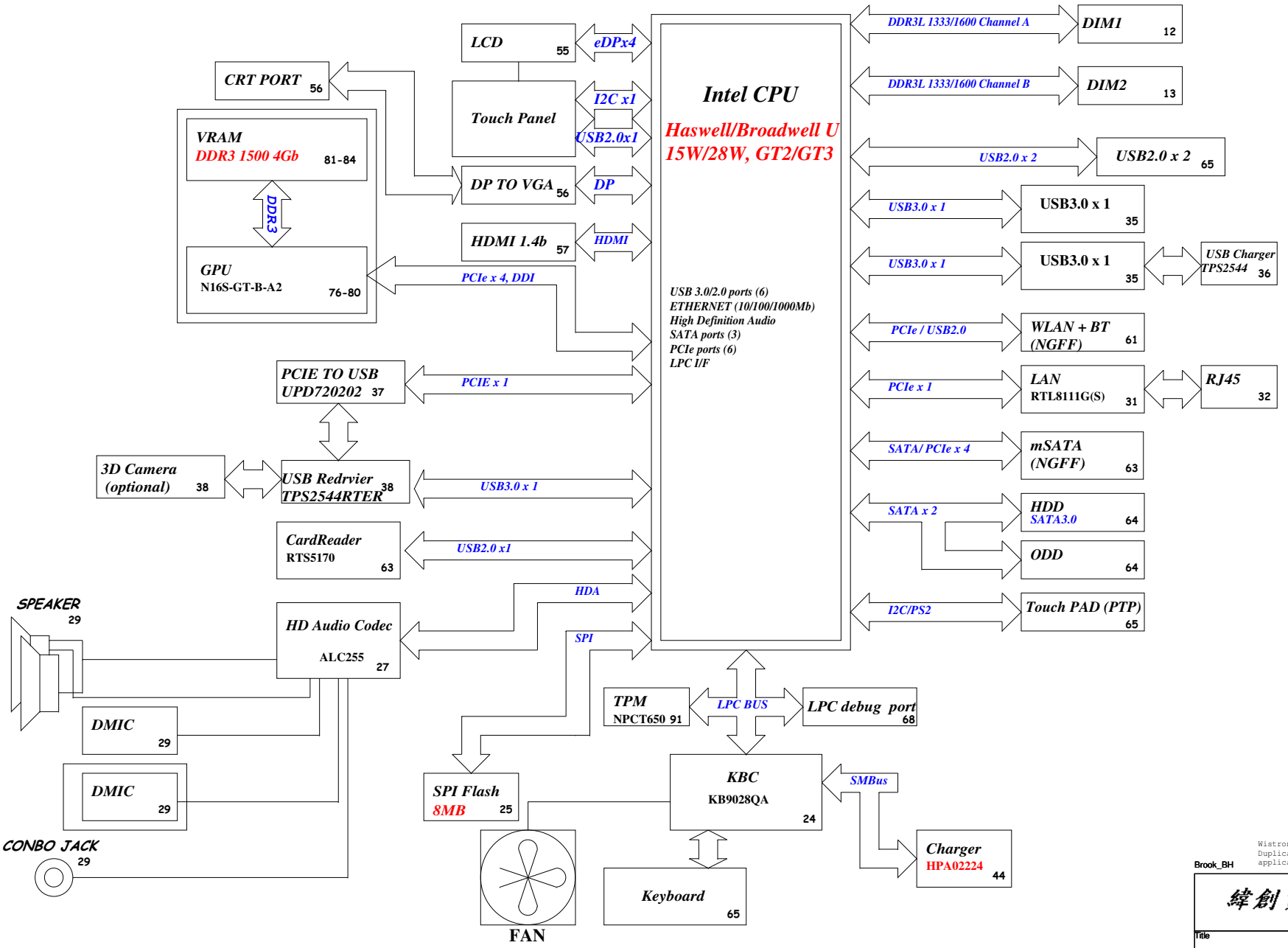
BROOK ULT Board Block Diagram

Project code : 4PD04X010001
PCB P/N : 14276
Revision : -1M



CHARGER HPA02224	44
INPUTS	OUTPUTS
DCBATOUT	BT+

SYSTEM DC/DC RT6575B	45
INPUTS	OUTPUTS
DCBATOUT	5V_S5 3D3V_S5

CPU DC/DC RT6575B	46-47
INPUTS	OUTPUTS
DCBATOUT	VCC_CORE

SYSTEM DC/DC TPS51716	48
INPUTS	OUTPUTS
DCBATOUT	1D05V_S0

SYSTEM DC/DC RT8231	49
INPUTS	OUTPUTS
DCBATOUT	1D35V_S3

SYSTEM LDO S13390D15	51
INPUTS	OUTPUTS
3D3V_S5	1D3V_S5

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Title: Block Diagram

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Date: Wednesday, February 04, 2015 | Sheet 2 of 106

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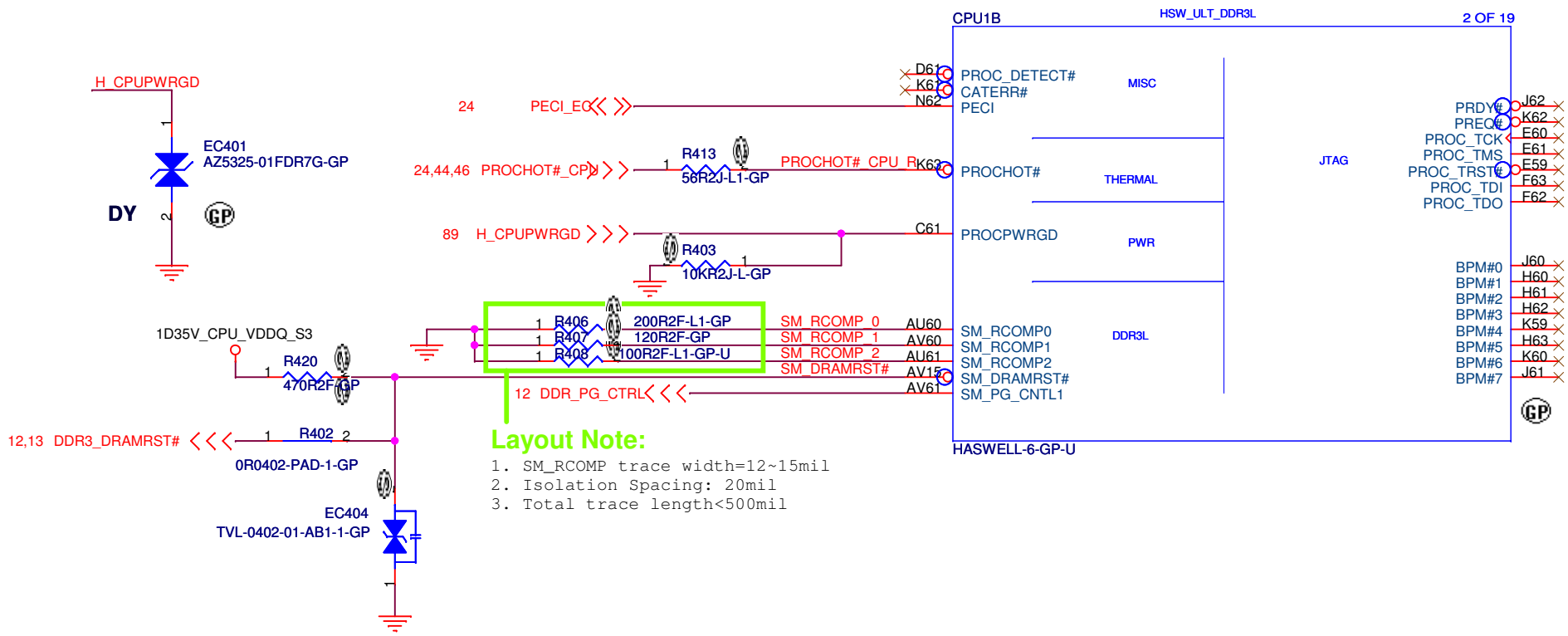

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Title: **CPU (THERMAL/CLOCK/PM)**

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Date: Wednesday, February 04, 2015 Sheet 4 of 106

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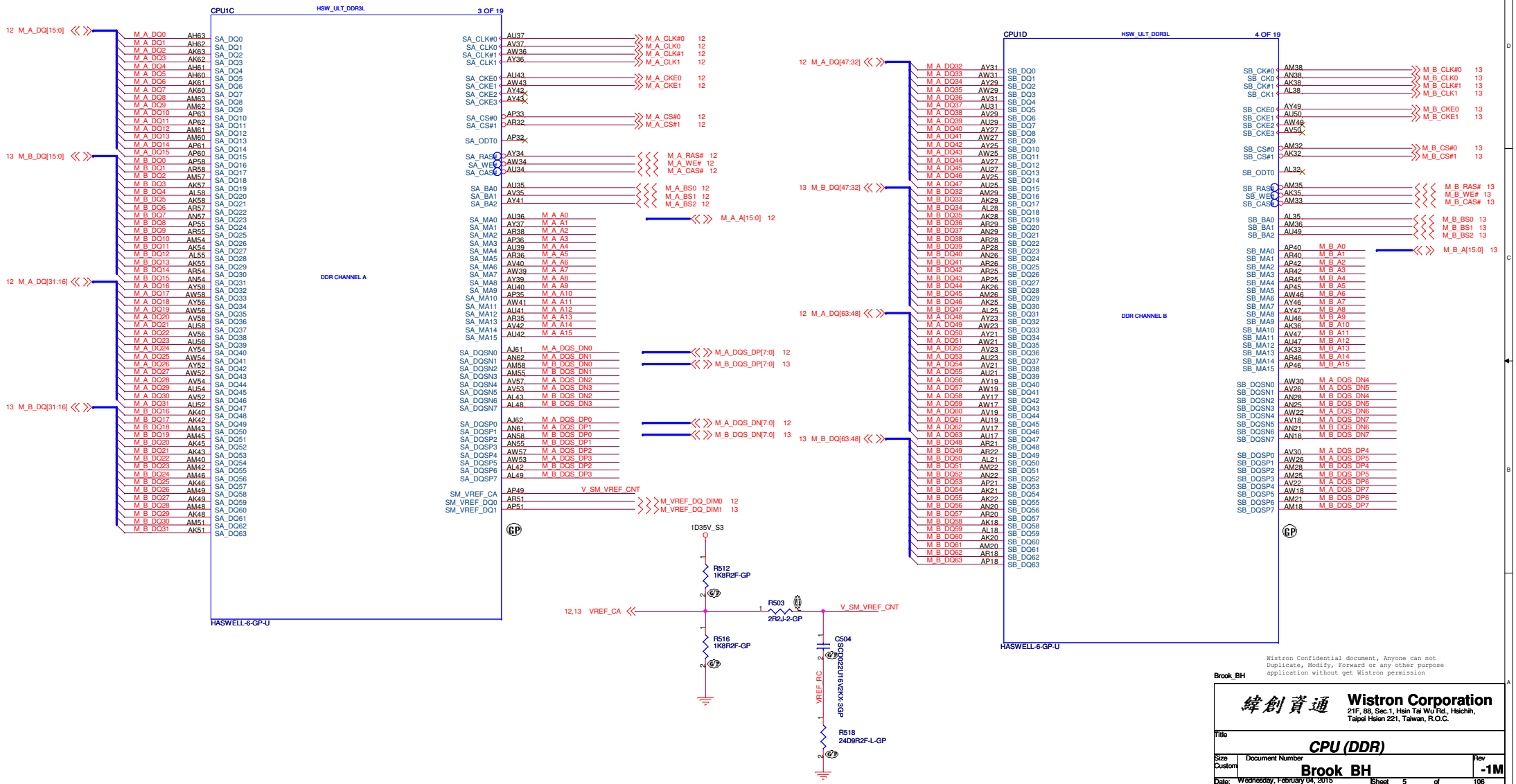
SSID = CPU



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Title: CPU (DDR)

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Date: Wednesday, February 04, 2015 Sheet 5 of 106

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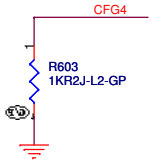
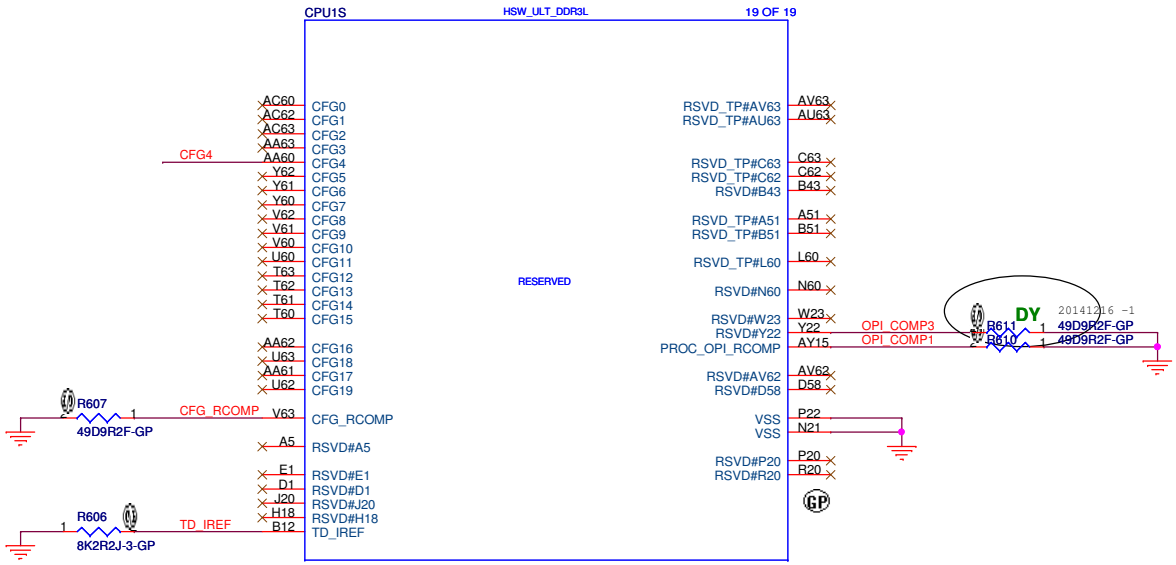
SSID = CPU

Pin Name	System Pull-up/Pull-down	Schematic Notes	✔
CFG[19:0]		Please refer to the *Crescent Bay and (??) Platforms - Debug Port Design Guide (DPDG)* .	

Note: Processor strap CFG[4] should be pulled low to enable embedded DisplayPort*

eDP Enable	
CFG4	1:Disable
	0:Enable





Signal Name	Description	Direction/ Buffer Type
CFG[19:0]	**Configuration Signals:** The CFG signals have a default value of '1' if not terminated on the board. Refer to the appropriate platform design guide for pull-down recommendations when a logic low is desired. • **CFG[3:0]:** Reserved configuration lane. A test point may be placed on the board for these lanes. • PCI Express* Static x16 Lane Numbering Reversal. — — • • **CFG[4]: eDP enable** — 1 = Disabled — 0 = Enabled • **[19:5]:** Reserved configuration lanes. A test point may be placed on the board for these lands.	I/O GTL
CFG_RCOMP	Configuration resistance compensation.	-
FC_x	FC signals are signals that are available for compatibility with other processors. A test point may be placed on the board for these lands. Refer to the appropriate platform design guide for implementation details.	

continued...

7.4 Reserved or Unused Signals

The following are the general types of reserved (RSVD) signals and connection guidelines:

- RSVD – these signals should not be connected
- RSVD_TP – these signals should be routed to a test point
- RSVD_NCTF – these signals are non-critical to function and may be left un-connected

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Title: **CPU (CFG)**

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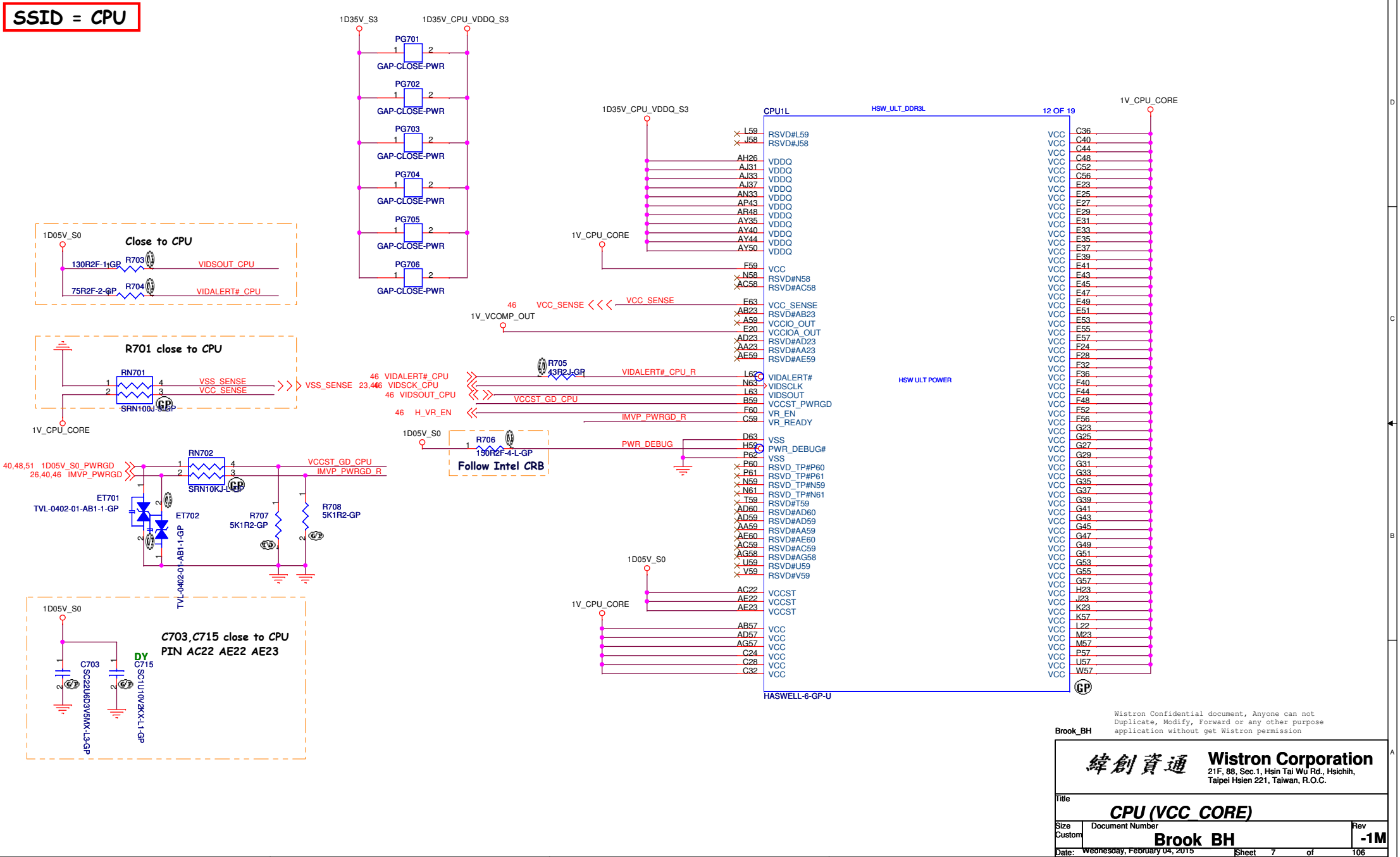
SSID = CPU



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Title: CPU (VCC_CORE)

Size	Document Number	Rev
Custom	Brook_BH	-1M

Date: Wednesday, February 04, 2015 Sheet 7 of 106

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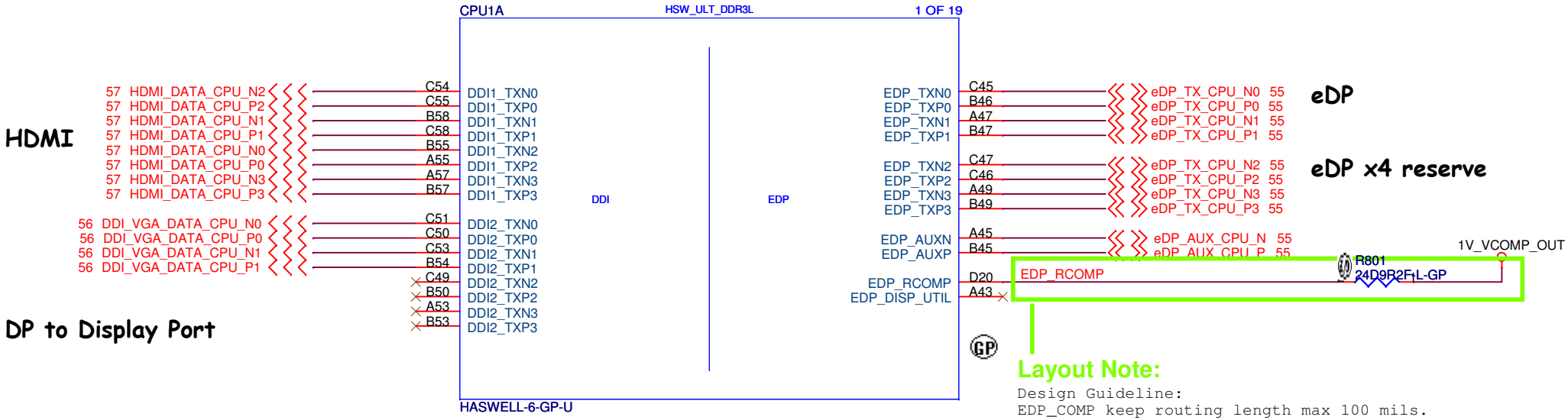
SSID = CPU



Layout Note:

Design Guideline:
EDP_COMP keep routing length max 100 mils.
Trace Width:20 mils.

Signal	Trace Width	Isolation Spacing	Resistor Value	Length
eDP_RCOMP	20 mils	25 mils	24.9 Ω ±1%	Max = 100 mils

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Title: ***CPU (DDI/EDP)***

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1D35V_CPU_VDDQ_S3

Power current=3A

C1040 SC10U6D3V3MX-L-GP
C1035 SC10U6D3V3MX-L-GP
DY
C1036 SC10U6D3V3MX-L-GP
C1037 SC10U6D3V3MX-L-GP
C1038 SC10U6D3V3MX-L-GP
C1039 SC10U6D3V3MX-L-GP

EC1006 SC2D2U10V3KX-L-GP
EC1007 SC2D2U10V3KX-L-GP
EC1008 SC2D2U10V3KX-L-GP
EC1009 SC2D2U10V3KX-L-GP

For Intel Recommend EE Part

1V_CPU_CORE

Power current=40A

PC1010 SC22U6D3V5MX-L3-GP
PC1009 SC22U6D3V5MX-L3-GP
PC1007 SC22U6D3V5MX-L3-GP
PC1006 SC22U6D3V5MX-L3-GP
PC1005 SC22U6D3V5MX-L3-GP
PC1002 SC22U6D3V5MX-L3-GP

PC1020 SC22U6D3V5MX-L3-GP
PC1019 SC22U6D3V5MX-L3-GP
PC1018 SC22U6D3V5MX-L3-GP
PC1017 SC22U6D3V5MX-L3-GP
PC1016 SC22U6D3V5MX-L3-GP
PC1015 SC22U6D3V5MX-L3-GP
PC1013 SC22U6D3V5MX-L3-GP
PC1012 SC22U6D3V5MX-L3-GP

1V_CPU_CORE

DY
EC1001 SC22U6D3V5MX-L3-GP
DY
EC1002 SC22U6D3V5MX-L3-GP
DY
EC1003 SC22U6D3V5MX-L3-GP
DY
EC1004 SC22U6D3V5MX-L3-GP
DY
EC1005 SC22U6D3V5MX-L3-GP
DY
EC1016 SC22U6D3V5MX-L3-GP

1V_CPU_CORE

15WDY/28W
PT1001
ST220U2VDM-8-GP

1V_CPU_CORE

C1002 SC1U10V2KX-L1-GP
C1003 SC1U10V2KX-L1-GP
C1004 SC1U10V2KX-L1-GP
C1005 SC1U10V2KX-L1-GP

For Intel Recommend EE Part

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Title: CPU (Power CAP1)

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擺放電容的位置請參考 Page 21,每個位置如下

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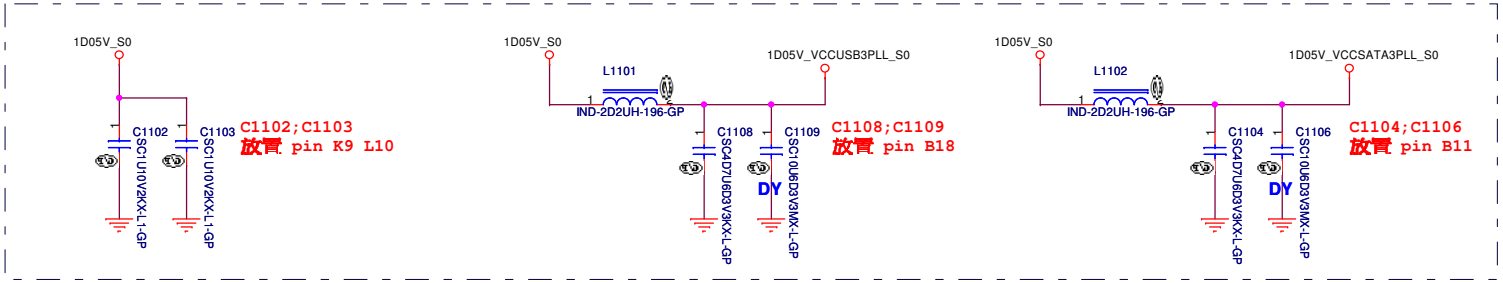

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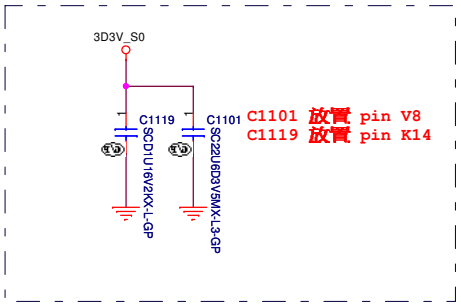

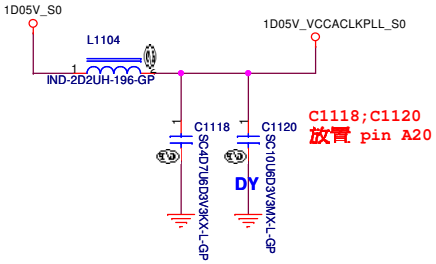

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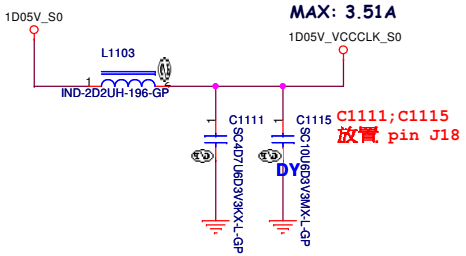

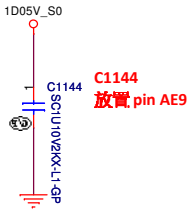

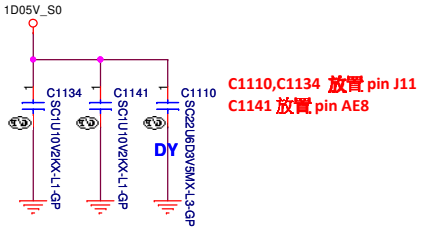

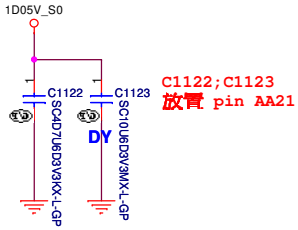

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Title: CPU (Power CAP2)

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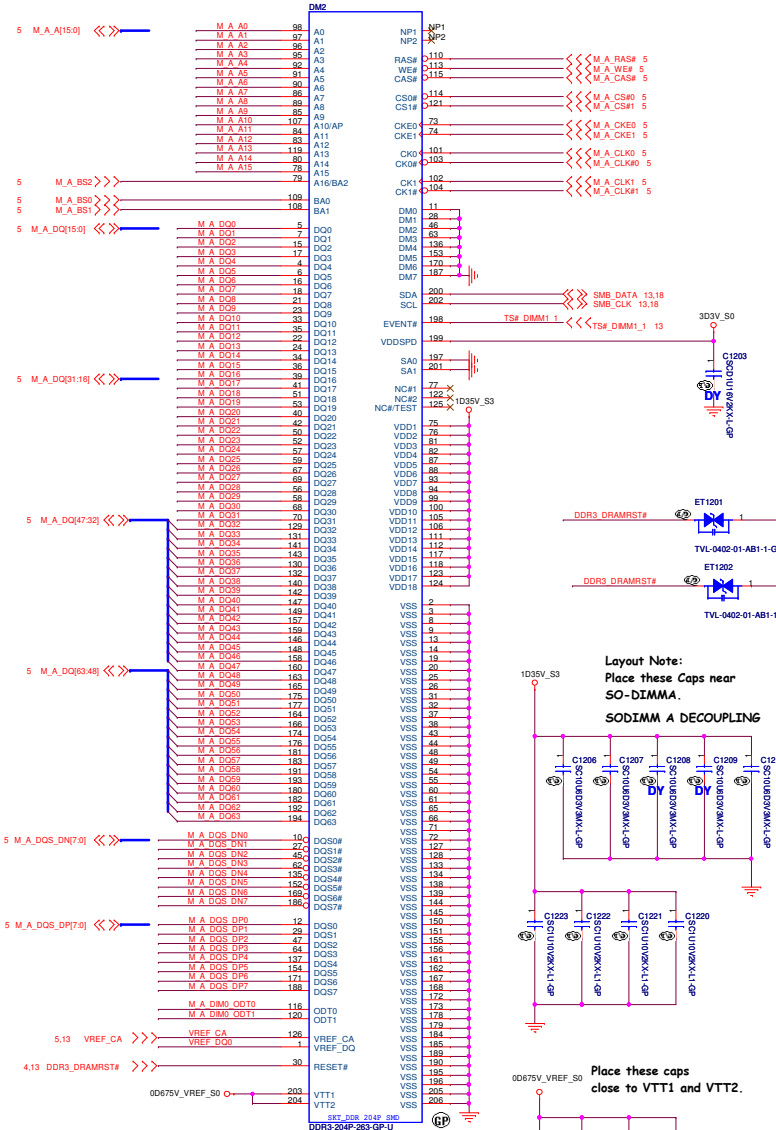
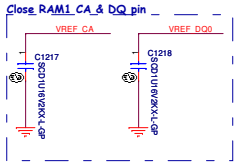
SSID = MEMORY



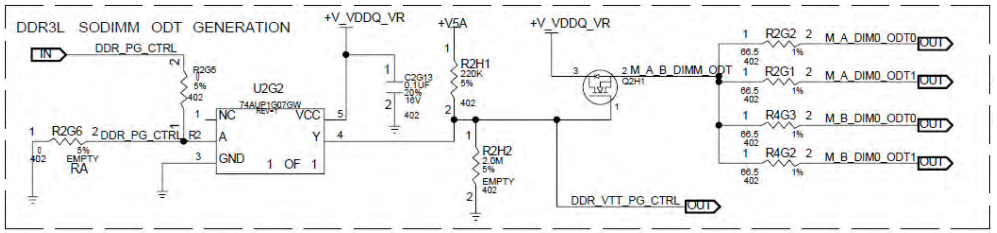


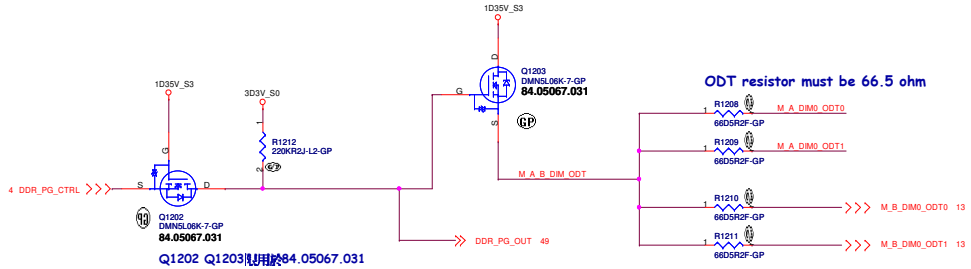
Note:
If SA0 DIM0 = 0, SA1_DIM0 = 0
SO-DIMMA SPD Address is 0xA0
SO-DIMMA TS Address is 0x30

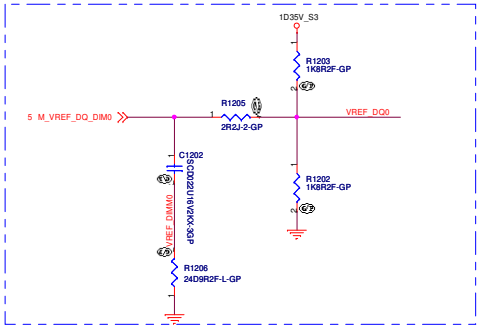
If SA0 DIM0 = 1, SA1_DIM0 = 0
SO-DIMMA SPD Address is 0xA2
SO-DIMMA TS Address is 0x32

SODIMM Memory Connectivity and Topology
ODT Signal Connectivity and Support
For DDR3L SODIMM designs, Intel recommends ODT signals not to be routed between CPU and DIMM on platform, leave ODT at CPU as no-connect (open), and tie DIMM ODT to VDDQ through FET and resistor. The reason for this additional ODT-control circuitry on the platform is to save power dissipation by turning off VDDQ to VTT path during low power states, as ODT signal is terminated to VTT through RTT on SODIMM. The ODT value for DDR3L SODIMM 1-DPC platform will be encoded in the write command and use RTT_NOM = Off and RTT_WR = (60,120) Ohm.

- CPU ODT output would be NOCON
- SODIMM ODT input should be tied to VDDQ through a FET and a resistor to support low power states.







For Intel Recommend Close to DIMM

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Title: **DDR3-SODIMM1**

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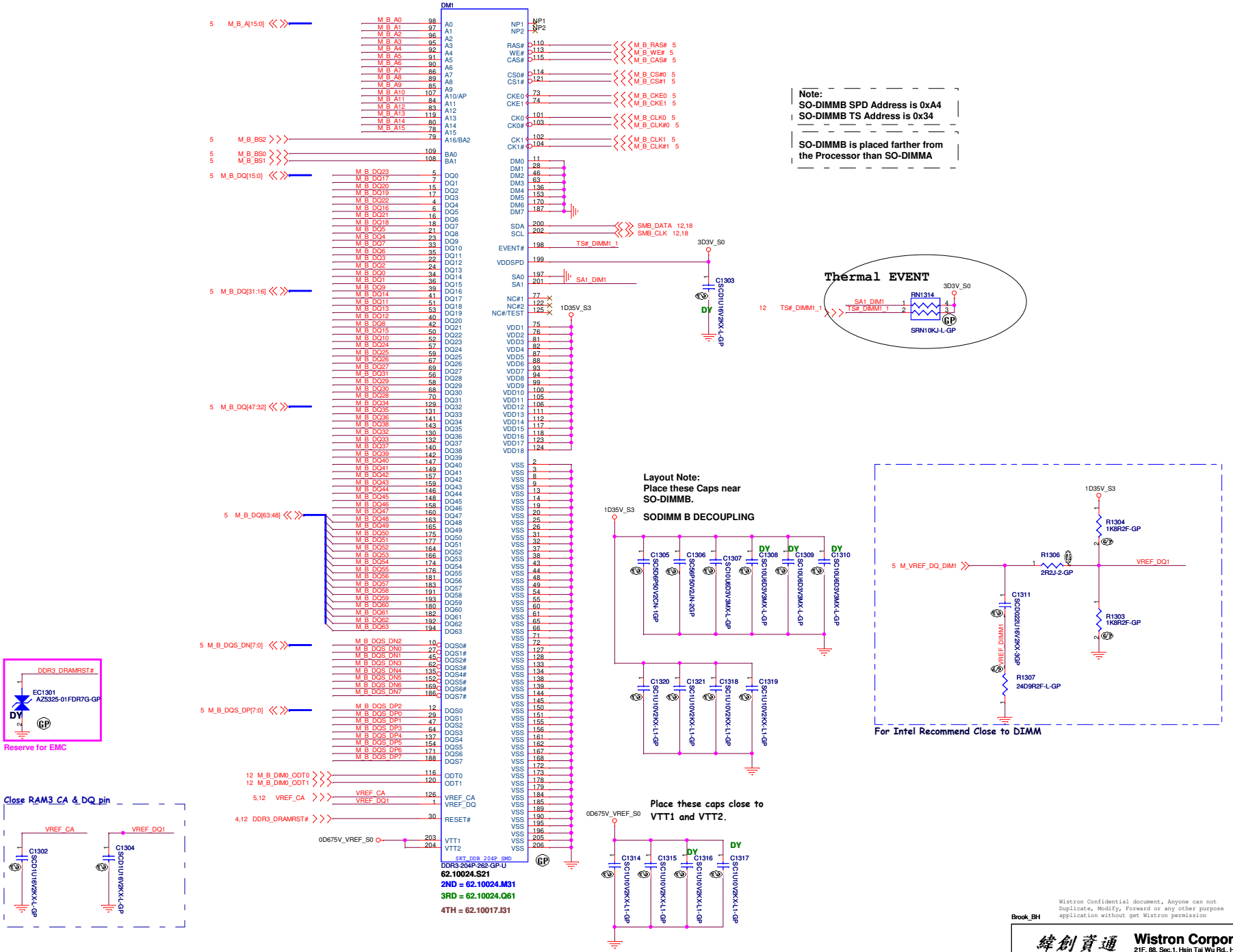
SSID = MEMORY



Note:
SO-DIMMB SPD Address is 0xA4
SO-DIMMB TS Address is 0x34

SO-DIMMB is placed farther from the Processor than SO-DIMMA

Thermal EVENT

Layout Note:
Place these Caps near SO-DIMMB.

SODIMM B DECOUPLING

For Intel Recommend Close to DIMM

Place these caps close to VTT1 and VTT2.

Reserve for EMC

Close RAM3 CA & DQ pin

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Title: DDR3-SODIMM2

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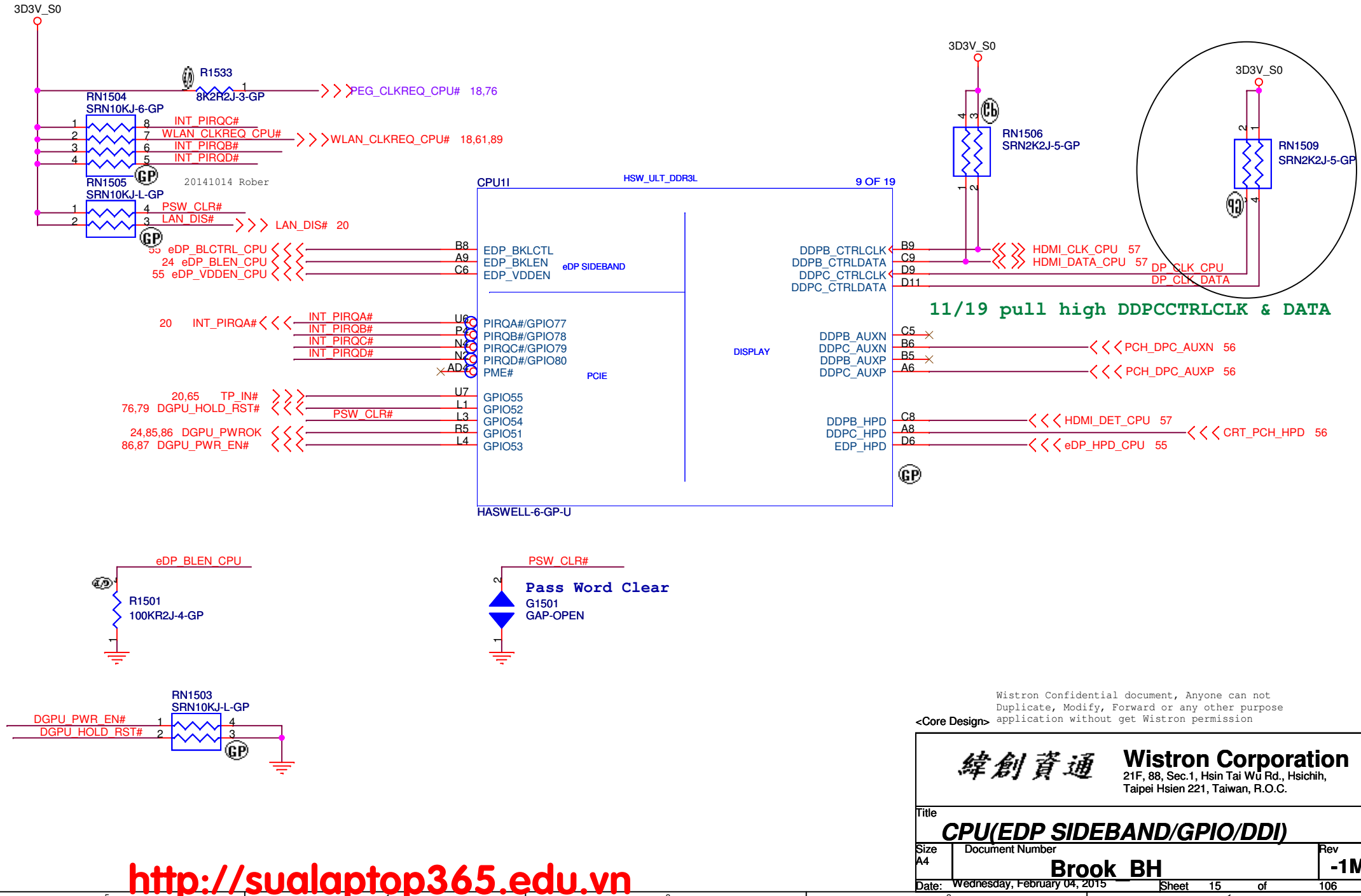

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<Core Design>

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Title: ***CPU(EDP SIDEBAND/GPIO/DDI)***

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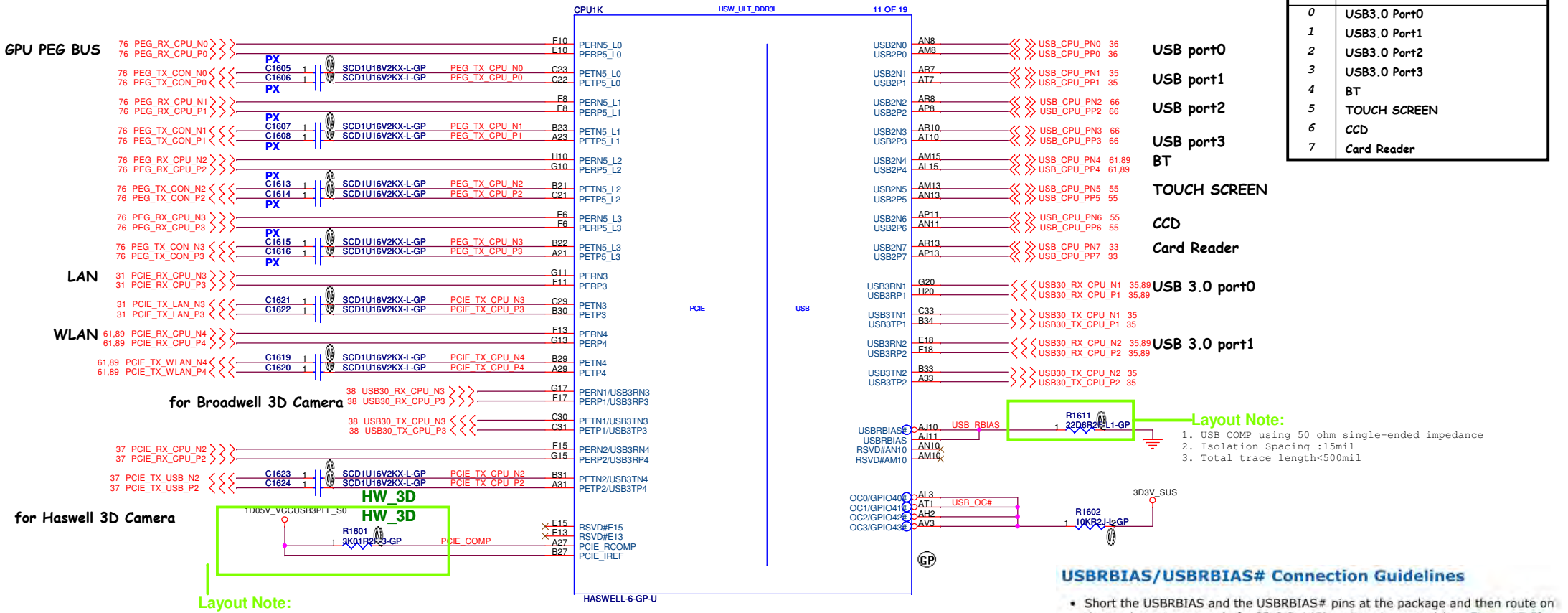

USB Table

Pair	Device
0	USB3.0 Port0
1	USB3.0 Port1
2	USB3.0 Port2
3	USB3.0 Port3
4	BT
5	TOUCH SCREEN
6	CCD
7	Card Reader

Layout Note:

1. USB_COMP using 50 ohm single-ended impedance
2. Isolation Spacing :15mil
3. Total trace length<500mil

Layout Note:

1. PCIE_RCOMP/ PCIE_IREF trace width=12~15mil
2. Isolation Spacing: 12mil
3. Total trace length<500mil

Signal	Trace Width	Isolation Spacing	Resistor Value	Length
PCIE_RCOMP	4 mils min (breakout) 12-15 mils (trace) **Note:** Must maintain low DC resistance routing (<0.2 ohm).	At least 12 mils to any adjacent high speed I/O.	3k ohm ±1% pulled to VCCUSB3PLL.	Max total = 500 mils
PCIE_IREF	4 mils min (breakout) 12-15 mils (trace) **Note:** Must maintain low DC resistance routing (<0.2 ohm).	At least 12 mils to any adjacent high speed I/O.	No resistor. Must connect directly to VCCUSB3PLL.	Max total = 500 mils

USBRBIAS/USBRBIAS# Connection Guidelines

- Short the USBRBIAS and the USBRBIAS# pins at the package and then route on the top layer to one end of a 22.6 Ω ±1% resistor to ground (see Figure 15-2).
- Route signal using 50 ohm single-ended impedance and 500 mils (12.7-mm) max trace length and no longer than 450 mils to resistor.
- Avoid routing next to clock pins or under stitching capacitors. Recommended minimum spacing to other signal traces is 15 mils (0.381 mm).

Signal	Trace Width	Isolation Spacing	Resistor Value	Length
PCIE_RCOMP	4 mils min (breakout) 12-15 mils (trace) **Note:** Must maintain low DC resistance routing (<0.2 ohm).	At least 12 mils to any adjacent high speed I/O.	3k ohm ±1% pulled to VCCUSB3PLL.	Max total = 500 mils
PCIE_IREF	4 mils min (breakout) 12-15 mils (trace) **Note:** Must maintain low DC resistance routing (<0.2 ohm).	At least 12 mils to any adjacent high speed I/O.	No resistor. Must connect directly to VCCUSB3PLL.	Max total = 500 mils

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Title: **CPU (PCI/USB)**

Size: A3 | Document Number: **Brook_BH** | Rev: **-1M**

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Bit	Description
31:3	Reserved
2	**WAKE# Pin Deep Sx Enable (WAKE_PIN__DSX_EN)** - R/W. When this bit is '1', the PCI Express WAKE# pin is monitored while in Deep Sx, supporting wake from Deep Sx due to assertion of this pin. In this case the platform must externally pull-up the pin to the DSW (instead of pulling-up to the SUS as historically been the case). When this bit is '0': • Deep Sx configurations: The PCH internal pull-down on the WAKE# pin is enabled in Deep Sx and during G3 exit and the pin is not monitored during this time. • Deep Sx disabled configurations: The PCH internal pull-down on the WAKE# pin is never enabled. **NOTE:** Deep Sx disabled configuration must leave this bit at '0'.

DSWODVREN – On Die DSW VR Enable	
HIGH	Enabled (DEFAULT)
LOW	Disabled

3D3V_RTC_AUX — R1717 330KR2J-L-GP — DSWODVREN

3D3V_SUS — R1728 10KR2J-L-GP — PM_SUS_STAT#

3D3V_S0 — RN1712 SRN10KJ-6-GP (GP) — MSATA_PEDET2 — SYS_RESET# — MSATA_PEDET1 — MSATA_PEDET2 19 — MSATA_PEDET1 19

20141216 -1

CPU1H — HSW_ULT_DDR3L — 8 OF 19 — SYSTEM POWER MANAGEMENT

SUSACK# — PM_SUSACK# — SYS_RESET# — SYS_PWROK_R — SYS_PWROK — PCH_PWROK — APWROK — PLTRST# — RSMRST# — SUSWARN#/SUSPWRDNACK#/GPIO30 — PWRBTN# — ACPRESENT/GPIO31 — BATLOW#/GPIO72 — SLP_S0# — SLP_WLAN#/GPIO29

DSWVRMEN — DPWROK — WAKE# — DSWODVREN — PCH_DPWROK — PM_RSMRST# — PCH_PCIE_WAKE# 24,31,61,63

CLKRUN#/GPIO32 — PM_CLKRUN#_EC 24,91

SUS_STAT#/GPIO60 — PM_SUS_STAT# 91

SUSCLK/GPIO62 — SUS_CLK_CPU — SUS_CLK_CPU 61,63

SLP_S5#/GPIO63

SLP_S4 — PM_SLP_S4# 24,49

SLP_S3 — PM_SLP_S3# 24,40,48,51

SLP_A

SLP_SUS — PM_SLP_SUS# — PM_SLP_SUS# 24,39

SLP_LAN

HASWELL-6-GP-U

R1724 0R0402-PAD-1-GP — 24 SYS_PWROK — 40 PCH_PWROK — 24,31,37,40,61,63,68,89,91 PLTRST#_PCH

R1727 10KR2J-L-GP — 24 PM_SUSWARN# — 20,24,89 PM_PWRBTN# — 24 AC_PRESENT — 20 BATLOW#

R1739 0R0402-PAD-1-GP — PM_RSMRST#

PCH_PWROK — EC1701 AZ5325-01FDR7G-GP — DY — PLTRST#_PCH — EC1702 AZ5325-01FDR7G-GP — DY

Cloes to CPU

PM_SUSWARN# — R1738 0R2J-L-GP — PM_SUSACK#

DY_DS3 R1737 0R2J-L-GP — PCH_DPWROK — KBC_DPWROK 24

DY_DS3 R1732 10KR2J-L-GP

3D3V_AUX_S5 — Non_DS3 R1709 100KR2J-L-GP — R1716 10KR2J-L-GP — Q1701 2N7002KDW-GP — 3V_5V_POK_# — PM_RSMRST# — 3V_5V_POK_C

R1712 1KR2J-L-GP — RSMRST#_KBC 24

R1740 0R0402-PAD-1-GP — 3V_5V_POK 45

DY_DS3 R1721 0R2J-L-GP — PM_SLP_SUS#

84.2N702.A3F
2nd = 75.00601.07C
3rd = 84.2N702.F3F

3D3V_S5 — RN1701 SRN10KJ-6-GP — AC_PRESENT — RTC_DET# — PCH_PCIE_WAKE# — MCP_GPIO12 20 — RTC_DET# 20,25 — PCH_PCIE_WAKE# 24,31,61,63

R1702 1KR2J-L2-GP — 3D3V_SUS — PM_SUSWARN#

R1719 10KR2J-L-GP — 3D3V_S0 — PM_CLKRUN#_EC — PM_CLKRUN#_EC 24,91

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Size: A3 | Document Number: Brook_BH | Rev: -1M

Date: Wednesday, February 04, 2015 | Sheet 17 of 106

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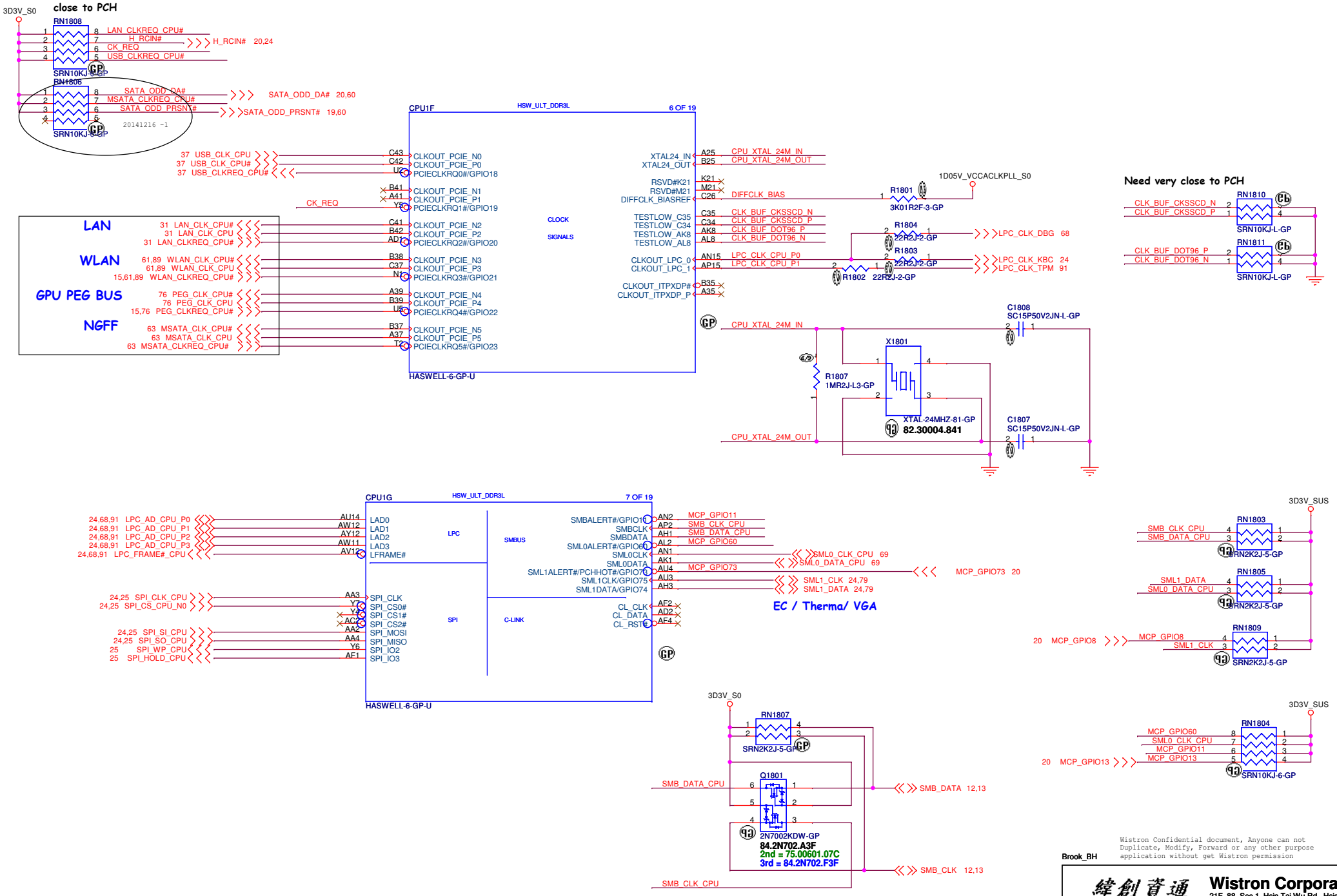

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Size	Document Number	Rev
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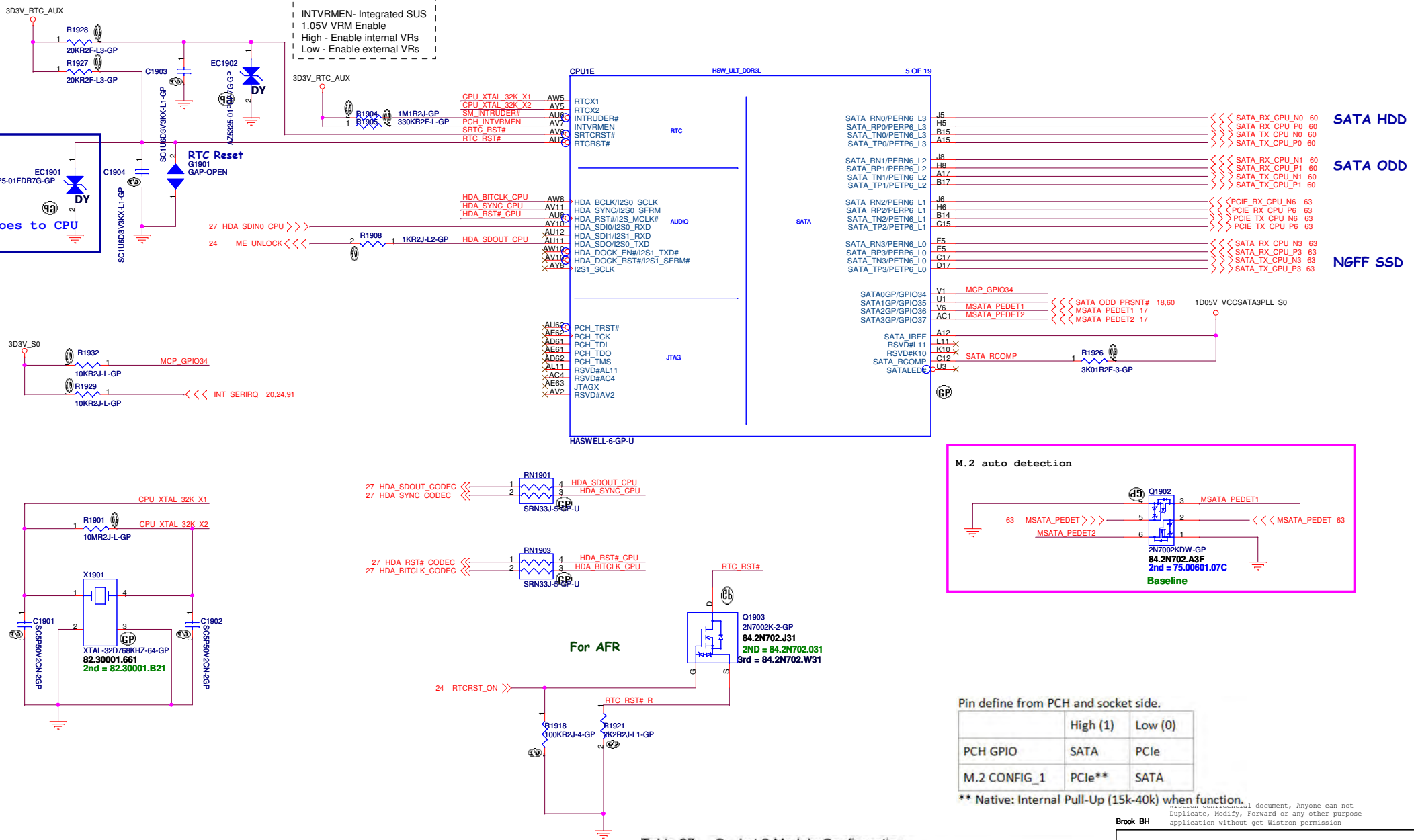

Pin define from PCH and socket side.

	High (1)	Low (0)
PCH GPIO	SATA	PCIe
M.2 CONFIG_1	PCIe**	SATA

** Native: Internal Pull-Up (15k-40k) when function.

Table 27. Socket 2 Module Configuration

State #	Module Configuration Decodes CONFIG_0 (Pin 21)	CONFIG_1 (Pin 69)	CONFIG_2 (Pin 75	CONFIG_3 (Pin 1)	Module Type and Main Host Interface[1]	Port Configuration[2]
0	GND	GND	GND	GND	SSD – SATA	N/A
	GND	N/C	GND	GND	SSD – PCIe	N/A

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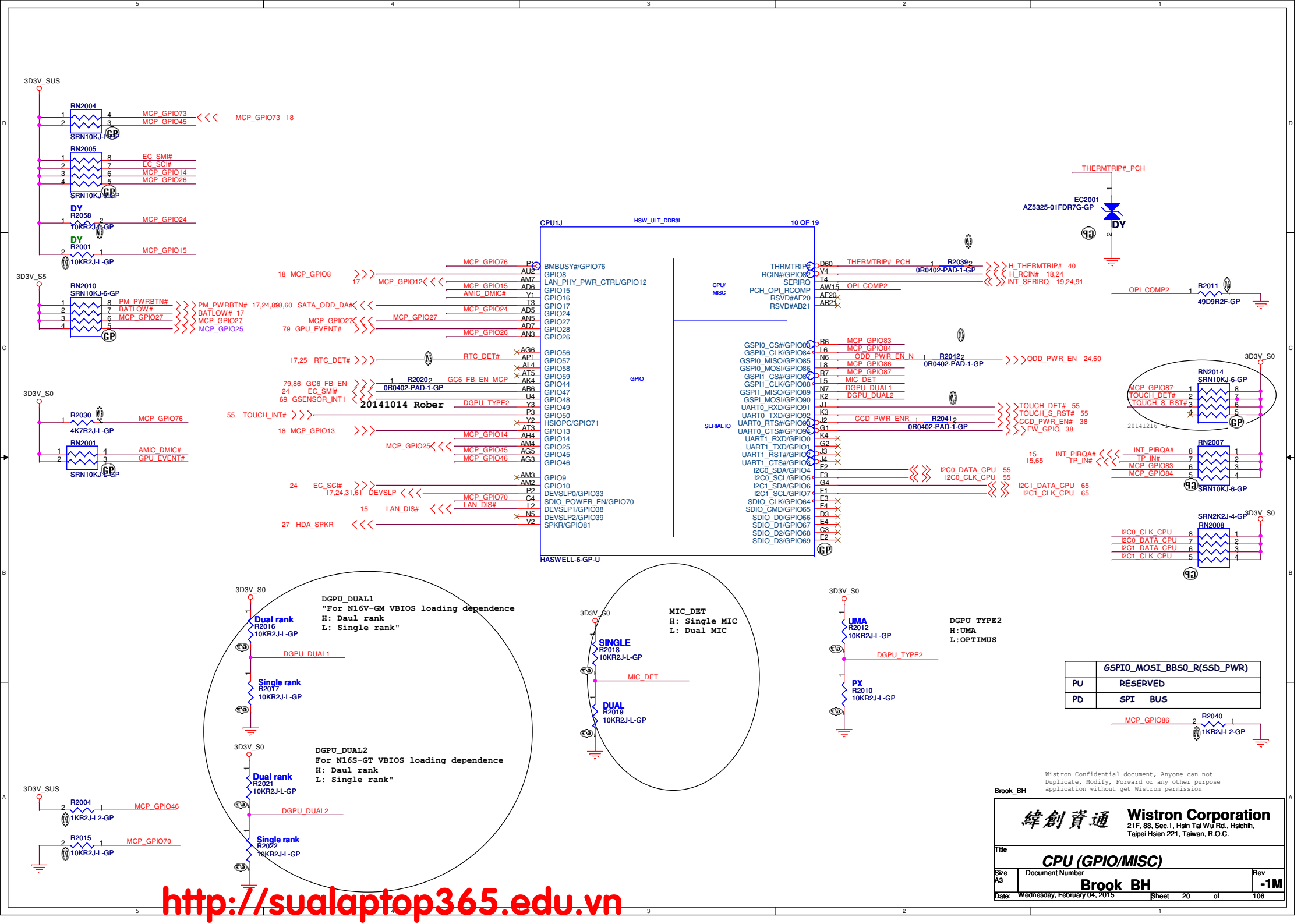
3D3V_SUS
RN2004
MCP_GPIO73
MCP_GPIO45
SRN10KJ-L-GP
RN2005
EC_SMI#
EC_SCI#
MCP_GPIO14
MCP_GPIO26
DY
R2058
MCP_GPIO24
10KR2J-L-GP
R2001
MCP_GPIO15
3D3V_S5
RN2010
SRN10KJ-6-GP
PM_PWRBTN#
BATLOW#
MCP_GPIO27
MCP_GPIO25
3D3V_S0
R2030
4K7R2J-L-GP
RN2001
AMIC_DMIC#
GPU_EVENT#
CPU1J
HSW_ULT_DDR3L
10 OF 19
BMBUSY#/GPIO76
GPIO8
LAN_PHY_PWR_CTRL/GPIO12
GPIO15
GPIO16
GPIO17
GPIO24
GPIO27
GPIO28
GPIO26
GPIO56
GPIO57
GPIO58
GPIO59
GPIO44
GPIO47
GPIO48
GPIO49
GPIO50
HSIOPC/GPIO71
GPIO13
GPIO14
GPIO25
GPIO45
GPIO46
GPIO9
GPIO10
DEVSLP0/GPIO33
SDIO_POWER_EN/GPIO70
DEVSLP1/GPIO38
DEVSLP2/GPIO39
SPKR/GPIO81
GPIO
CPU MISC
SERIAL IO
THERMTRIP#
RCIN#/GPIO8
SERIRQ
PCH_OPI_RCOMP
RSVD#AF20
RSVD#AB21
GSPI0_CS#/GPIO83
GSPI0_CLK/GPIO84
GSPI0_MISO/GPIO85
GSPI0_MOSI/GPIO86
GSPI1_CS#/GPIO87
GSPI1_CLK/GPIO88
GSPI1_MISO/GPIO89
GSPI_MOSI/GPIO90
UART0_RXD/GPIO91
UART0_TXD/GPIO92
UART0_RTS#/GPIO93
UART0_CTS#/GPIO94
UART1_RXD/GPIO0
UART1_TXD/GPIO1
UART1_RST#/GPIO2
UART1_CTS#/GPIO3
I2C0_SDA/GPIO4
I2C0_SCL/GPIO5
I2C1_SDA/GPIO6
I2C1_SCL/GPIO7
SDIO_CLK/GPIO64
SDIO_CMD/GPIO65
SDIO_D0/GPIO66
SDIO_D1/GPIO67
SDIO_D2/GPIO68
SDIO_D3/GPIO69
HASWELL-6-GP-U
THERMTRIP#_PCH
EC2001
AZ5325-01FDR7G-GP
R2039
0R0402-PAD-1-GP
H_THERMTRIP# 40
H_RCIN# 18,24
INT_SERIRQ 19,24,91
OPI_COMP2
R2011
49D9R2F-GP
R2042
ODD_PWR_EN 24,60
R2041
TOUCH_DET# 55
TOUCH_S_RST# 55
CCD_PWR_EN# 38
FW_GPIO 38
I2C0_DATA_CPU 55
I2C0_CLK_CPU 55
I2C1_DATA_CPU 65
I2C1_CLK_CPU 65
RN2014
SRN10KJ-6-GP
RN2007
RN2008
SRN2K2J-4-GP
R2020
GC6_FB_EN_MCP
20141014 Rober
DGPU_TYPE2
DGPU_DUAL1
"For N16V-GM VBIOS loading dependence
H: Daul rank
L: Single rank"
Dual rank
R2016
10KR2J-L-GP
Single rank
R2017
10KR2J-L-GP
DGPU_DUAL2
For N16S-GT VBIOS loading dependence
H: Daul rank
L: Single rank"
R2021
R2022
MIC_DET
H: Single MIC
L: Dual MIC
SINGLE
R2018
DUAL
R2019
DGPU_TYPE2
H:UMA
L:OPTIMUS
UMA
R2012
PX
R2010
GSPIO_MOSI_BBSO_R(SSD_PWR)
PU
RESERVED
PD
SPI BUS
R2040
1KR2J-L2-GP
R2004
R2015
10KR2J-L-GP
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Title
CPU (GPIO/MISC)
Size A3
Document Number
Brook_BH
Rev -1M
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Sheet 20 of 106
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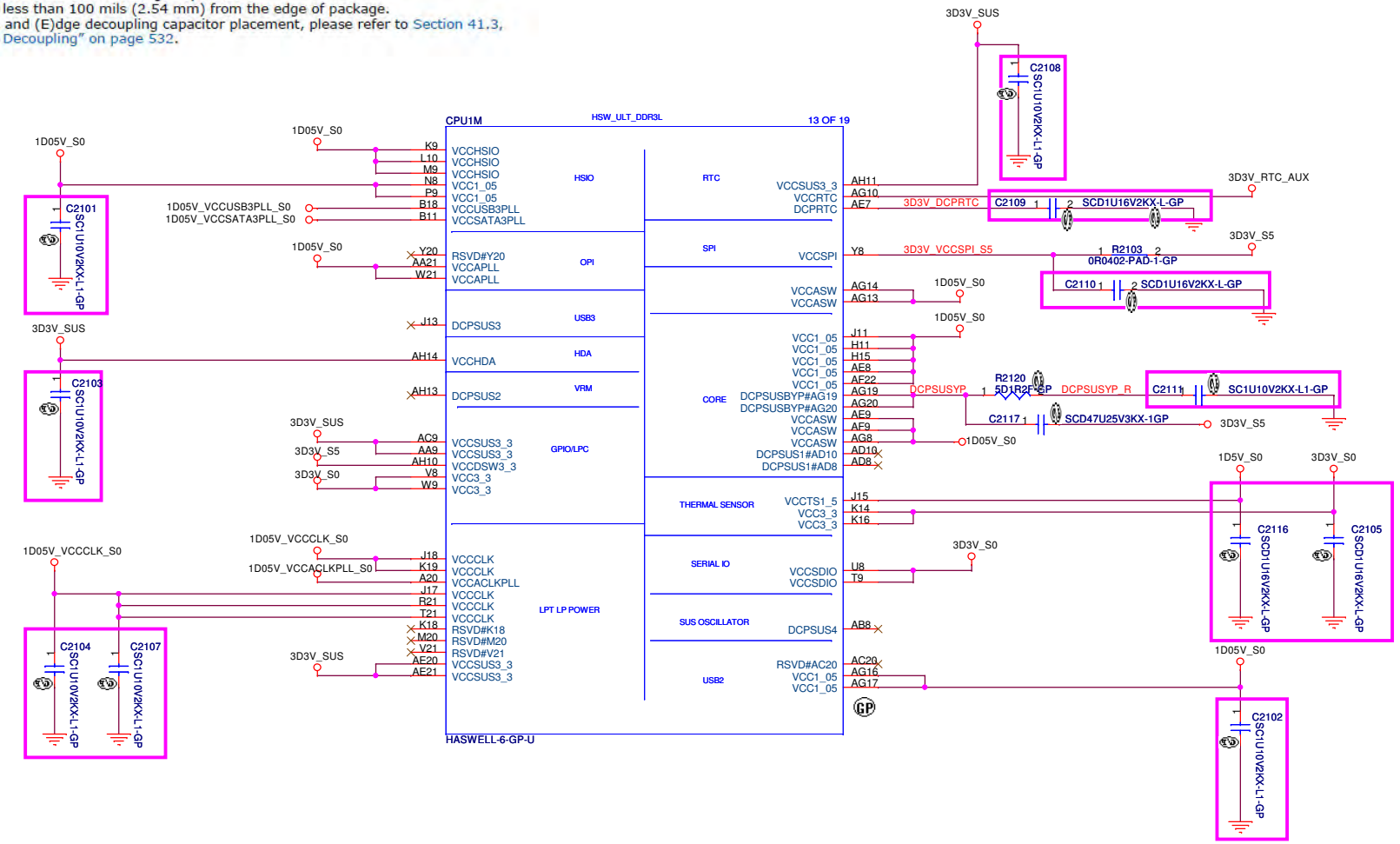
Notes:

1. Required only on external SUS.
2. Placeholder only. Does not need to be stuffed.
3. The following pins are not to be connected and be left floating. Test point is optional on these pins: AC20, Y20, K18, M20, V21.
4. Note that some decoupling capacitors are shared between more than 1 rail. Follow the "Place capacitors near balls" instructions above to ensure this sharing is optimized.
5. Capacitors should be placed less than 100 mils (2.54 mm) from the edge of package.
6. For description of (R)unway, and (E)dge decoupling capacitor placement, please refer to Section 41.3, "Loop Inductance Reduction Decoupling" on page 532.



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Title: **CPU (POWER1)**

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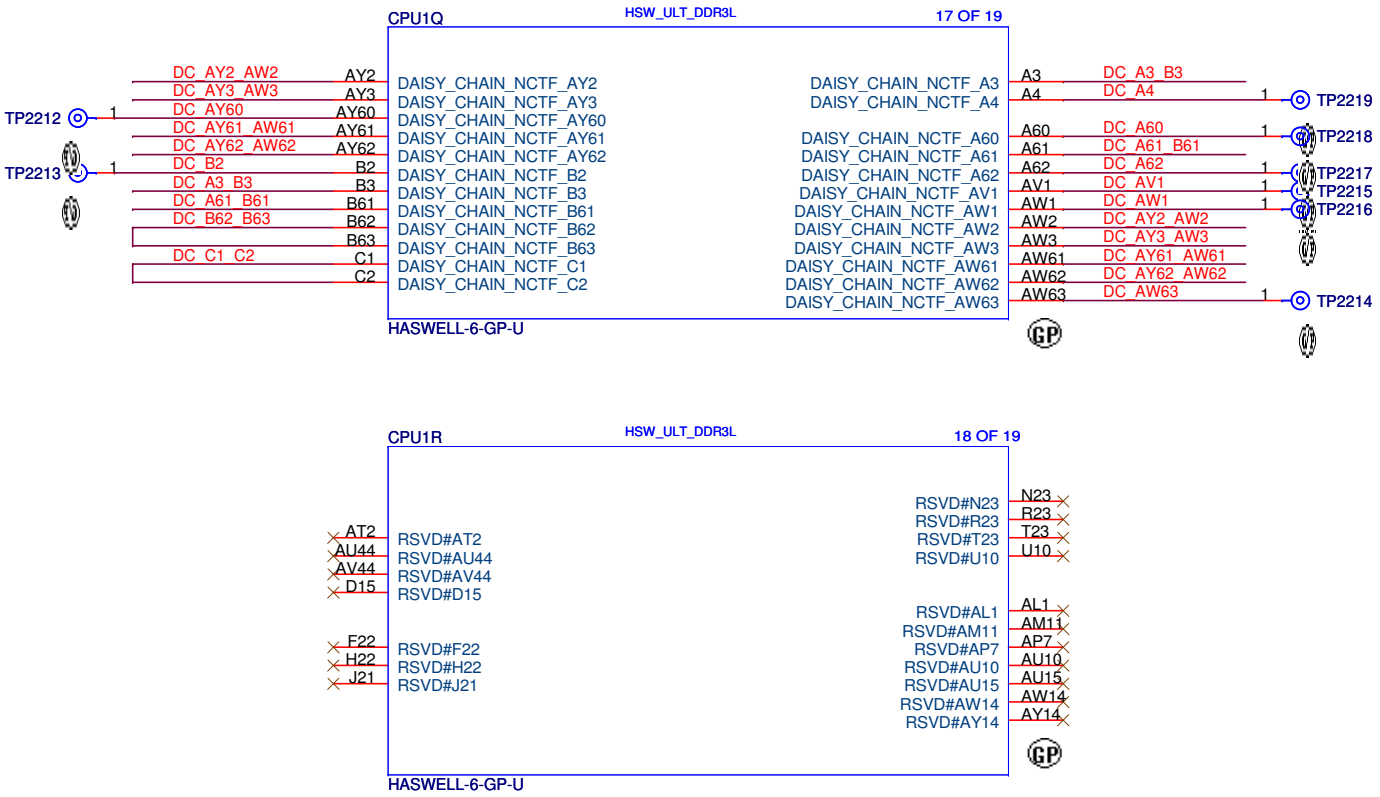

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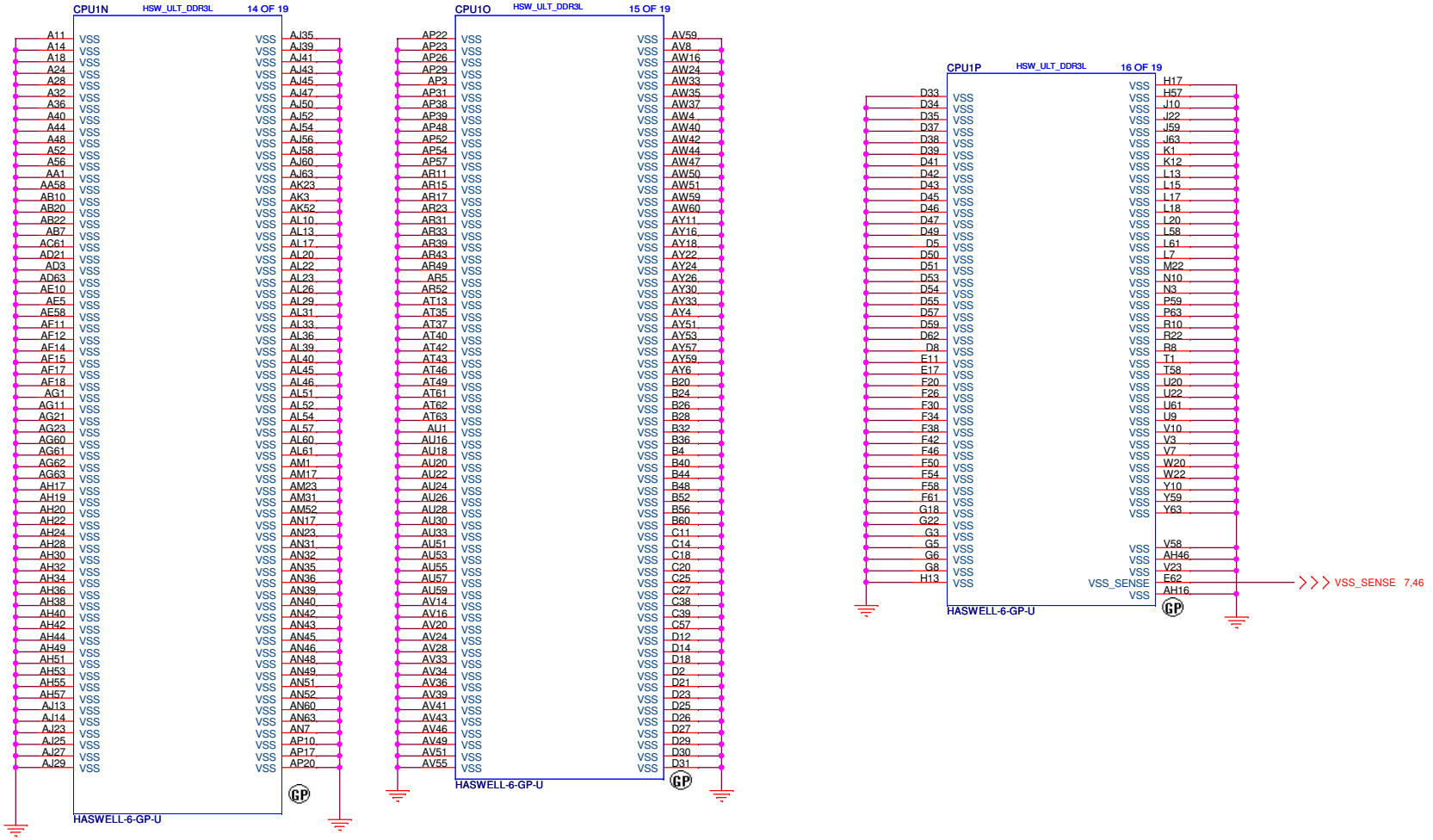

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Title: **CPU (VSS)**

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SSID = KBC

For EC power consumption reserver

Close to the EC

11/18 RN7904 to RN2404

20141014 Rober

Rober change 11/17

< ---CPU/GPU

< ---BATTER /CHARGER

< ---Touch Pad

OPMODE (Pin70)

GPIO0 High Active

LPC

MODEL_ID_AD	Pull-Low Register	Pull-High Register	Typical Voltage
Brook_H_UMA/Brook_SL_UMA	100.0 K	10.0 K	3.000 V
Brook_H_DIS/Brook_SL_DIS	100.0 K	20.0 K	2.750 V
Brook_B_UMA	100.0 K	33.0 K	2.481 V
Brook_B_DIS	100.0 K	47.0 K	2.245 V
Reserved for project use	100.0 K	64.9 K	2.001 V
Reserved for project use	100.0 K	76.8 K	1.867 V
Reserved for project use	100.0 K	100.0 K	1.650 V
Reserved for project use	100.0 K	143.0 K	1.358 V
Reserved for project use	100.0 K	174.0 K	1.204 V
Reserved for project use	100.0 K	215.0 K	1.048 V

PCB_VER_AD	Pull-Low Register	Pull-High Register	Typical Voltage	Max Voltage	KBC Firmware Setting	
SA	100.0 K	10.0 K	3.000 V	3.005 V	>= 2.875 V	
SB	100.0 K	20.0 K	2.750 V	2.759 V	>= 2.616 V	< 2.875 V
SC	100.0 K	33.0 K	2.481 V	2.493 V	>= 2.363 V	< 2.616 V
-1	100.0 K	47.0 K	2.245 V	2.259 V	>= 2.123 V	< 2.363 V
Reserved for project use	100.0 K	64.9 K	2.001 V	2.017 V	>= 1.934 V	< 2.123 V
Reserved for project use	100.0 K	76.8 K	1.867 V	1.883 V	>= 1.758 V	< 1.934 V
Reserved for project use	100.0 K	100.0 K	1.650 V	1.667 V	>= 1.504 V	< 1.758 V
Reserved for project use	100.0 K	143.0 K	1.358 V	1.374 V	>= 1.281 V	< 1.504 V
Reserved for project use	100.0 K	174.0 K	1.204 V	1.220 V	>= 1.126 V	< 1.281 V
Reserved for project use	100.0 K	215.0 K	1.048 V	1.062 V	>= 0.524 V	< 1.126 V

ADT_TYPE_AD	Pull-Low Register	Pull-High Register	Typical Voltage	Max Voltage	KBC Firmware Setting	
65W	N/A	100.0 K	3.300 V		>= 3.000 V	
90W	100.0 K	N/A	3.000 V			< 0.150 V
33W	10.0 K	100.0 K	0.300 V	0.305 V	>= 0.150 V	< 0.425 V
45W	20.0 K	100.0 K	0.550 V	0.559 V	>= 0.425 V	< 0.684 V
120W	33.0 K	100.0 K	0.818 V	0.831 V	>= 0.684 V	< 0.937 V
135W	47.0 K	100.0 K	1.055 V	1.070 V	>= 0.937 V	< 1.177 V
150W	64.9 K	100.0 K	1.299 V	1.315 V	>= 1.177 V	< 1.366 V
Reserved	76.8 K	100.0 K	1.433 V	1.450 V	>= 1.366 V	< 1.542 V
Reserved	100.0 K	100.0 K	1.650 V	1.667 V	>= 1.542 V	< 1.842 V

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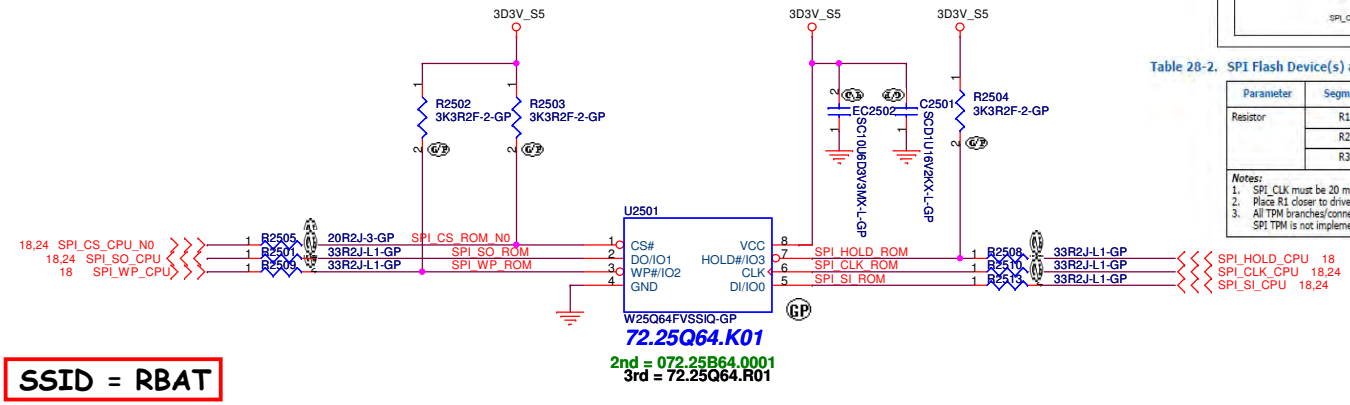
SSID = Flash.ROM

SPI FLASH ROM (8M byte) for PCH

SPI ROM Equal length need to less than 500mil

```
SPI FLASH ROM (8M byte)
1ST= 072.02564.0001(AMIC  A25LQ64M)
2ND=072.25B64.0001(Gigadevice  GD25B64BSIGR)

purge=72.25Q64.K01 (WINBOND  W25Q64FVSSIQ)
72.25647.00A (MXIC  MX25L6473EM2I)
```



72.25Q64.K01

2nd = 072.25B64.0001

3rd = 72.25Q64.R01

Figure 28-1. SPI Topology (Single Device)

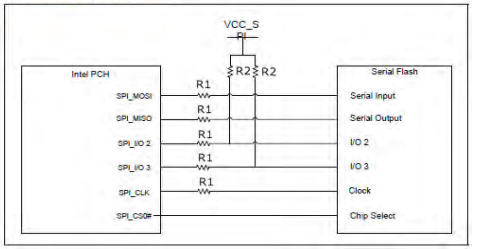
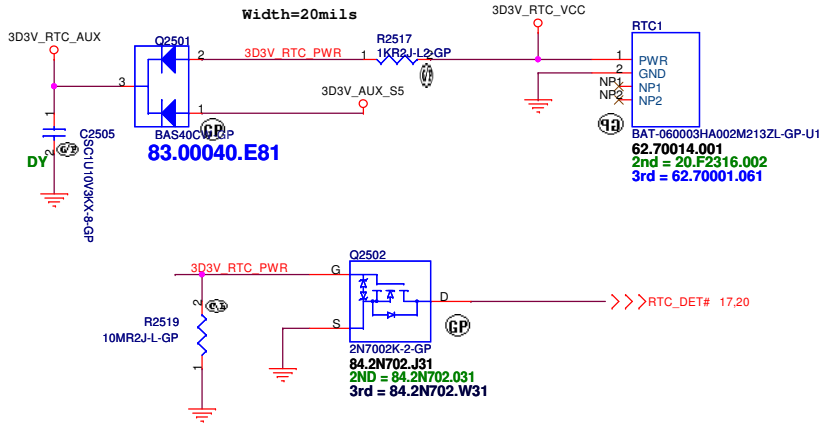


Table 28-2. SPI Flash Device(s) and TPM Routing Guideline (Sheet 2 of 2)

Parameter	Segment	Stackup	Unit	Routing Recommendation
Resistor	R1		ohm	15
	R2		ohm	1k
	R3		ohm	33

Notes:
1. SPI_CLK must be 20 mils spacing from any other high frequency (>1 GHz) signal.
2. Place R1 closer to driver side to effectively damping the undershoot and overshoot.
3. All TPM branches/connections (TPM_MOSI, TPM_MISO, TPM_CLK, and PCH_CS2#) can be left as NC if SPI TPM is not implemented.

SSID = RBAT



83.00040.E81

62.70014.001

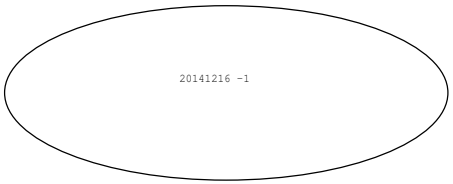
2nd = 20.F2316.002

3rd = 62.70001.061

84.2N702.J31

2ND = 84.2N702.031

3rd = 84.2N702.W31



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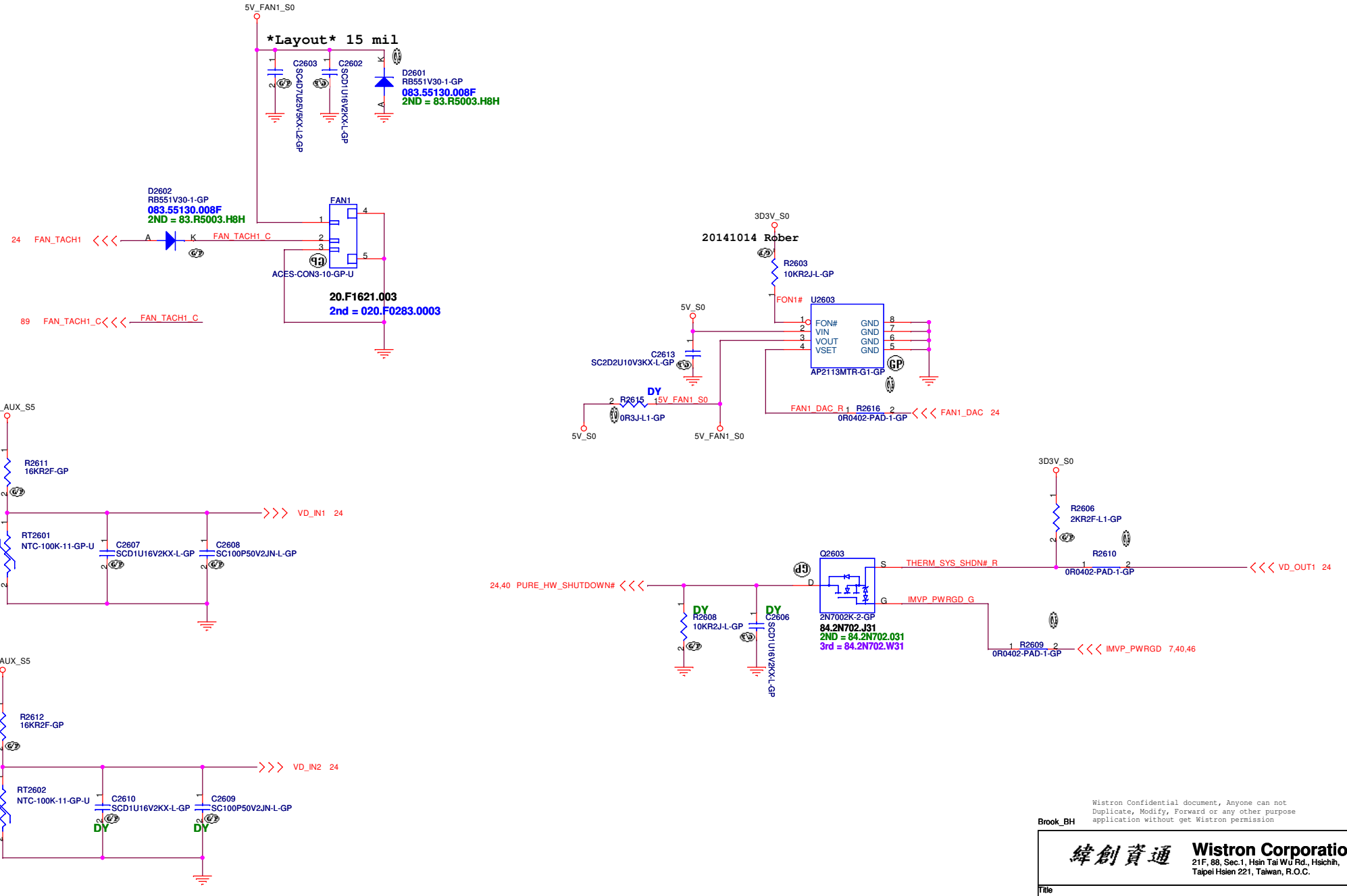

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Title: Thermal 7718/Fan Controllor P2793

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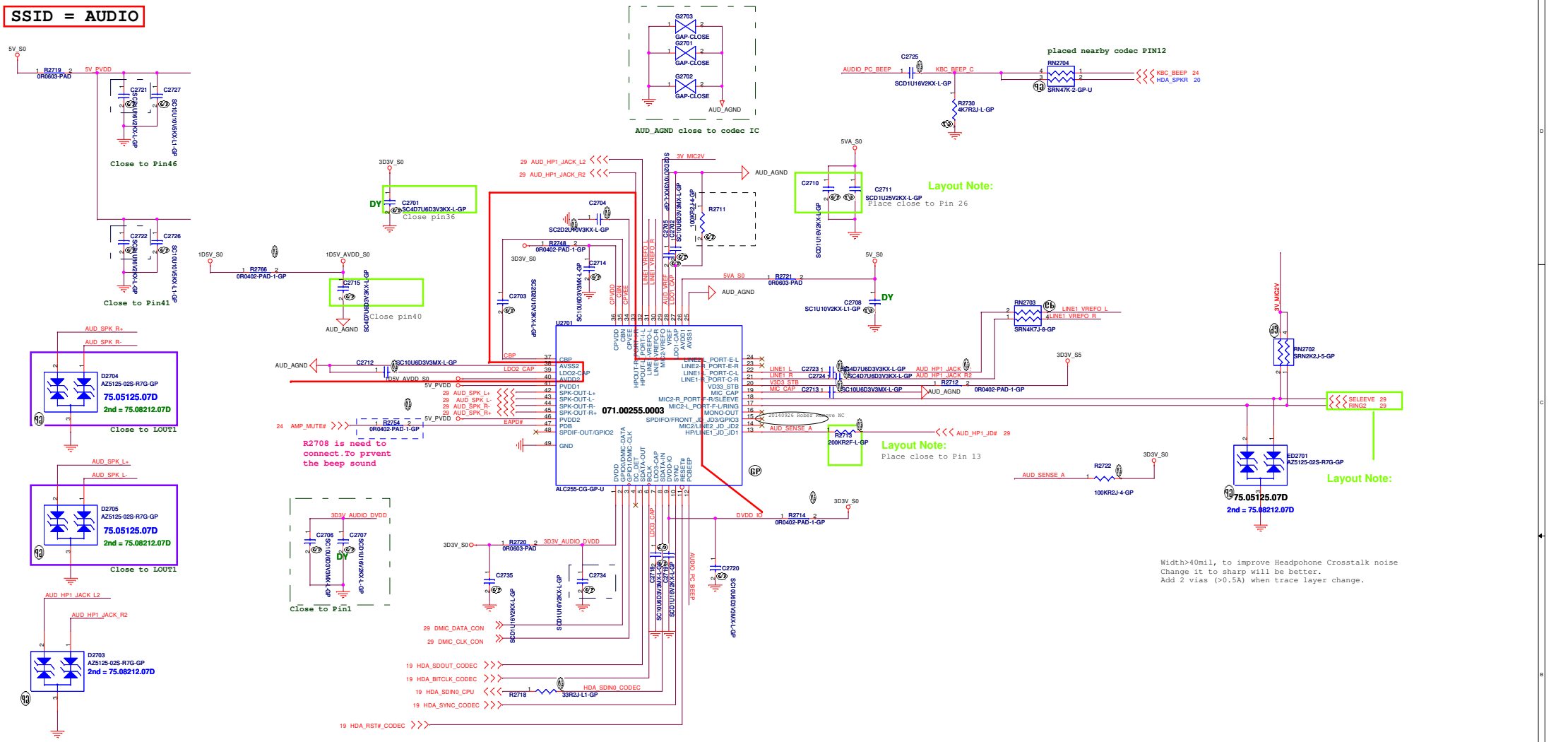
SSID = AUDIO



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Title: ***Audio Codec ALC255***

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SSID = AUDIO

Speaker

11/19 EMI Change

27 AUD_SPK_L- — EL2914 — BLM15PX121SN1D-GP — AUD_SPK1_L- CON
27 AUD_SPK_L+ — EL2915 — BLM15PX121SN1D-GP — AUD_SPK1_L+ CON
27 AUD_SPK_R- — EL2916 — BLM15PX121SN1D-GP — AUD_SPK1_R- CON
27 AUD_SPK_R+ — EL2917 — BLM15PX121SN1D-GP — AUD_SPK1_R+ CON

SPK1
20.F1621.004
2nd = 020.F0155.0004
ES-CON4-17-GP-U1

EC2901 SC1KP50V2KX-L-1-GP
EC2902 SC1KP50V2KX-L-1-GP
EC2915 SC1KP50V2KX-L-1-GP
EC2920 SC1KP50V2KX-L-1-GP

Layout Note:
Trace width=40mil

AUD_SPK1_L- CON <<< AUD_SPK1_L-_CON 89
AUD_SPK1_L+ CON <<< AUD_SPK1_L+_CON 89
AUD_SPK1_R- CON <<< AUD_SPK1_R-_CON 89
AUD_SPK1_R+ CON <<< AUD_SPK1_R+_CON 89

AFTP TESTPOINT

Combo Jack

R2910 0R0402-PAD-1-GP
Q2901 2N7002K-2-GP
84.2N702.J31
2ND = 84.2N702.031
AUD_HP1_JD#_R
AUD_HP1_JD#
C2902
R2901 100KR2J-4-GP
SC10U6D3V3MX-L-GP
AUD_AGND
DY

3D3V_S0
R2905 10KR2J-L-GP
AUD_HP1_JD#_TYPE
R2906 0R0402-PAD-1-GP
AUD_AGND

0527_SB

27 RING2 — R2920 0R0402-PAD-1-GP — RING2_R
27 AUD_HP1_JACK_L2 — ER2913 33D4R3F-GP — AUD_HP1_JACK_L1
27 AUD_HP1_JACK_R2 — ER2912 33D4R3F-GP — AUD_HP1_JD#_TYPE
27 SELEEVE — R2921 0R0402-PAD-1-GP — AUD_HP1_JD#_R, AUD_HP1_JACK_R1, SELEEVE_R

AUD1
AUDIO-JK506-GP-U
022.10002.0951

EC2923 EC2921 EC2922 EC2912 EC2913 EC2914 SC22P50V2JN-L-GP
AUD_AGND
DY

AUD_HP1_JD#_R <<< AUD_HP1_JD#_R 89
AUD_HP1_JACK_R1 <<< AUD_HP1_JACK_R1 89
AUD_HP1_JACK_L1 <<< AUD_HP1_JACK_L1 89
RING2_R <<< RING2_R 89
SELEEVE_R <<< SELEEVE_R 89
AUD_HP1_JD#_TYPE <<< AUD_HP1_JD#_TYPE 89

AFTP TESTPOINT

DUAL / SINGLE
R2917 0R2J-L-GP
R2916 0R2J-L-GP
DUAL/SINGAL
DMIC_DATA_R
MIC2
ENHANCE CS GND VDD DATA CLK
DMIC_DATA_CON_R
DMIC_CLK_CON_R
3D3V_S0
MICROPHONE-105-GP-U
082.40011.0001

MIC1
DUAL
DMIC_DATA_R1
DMIC_CLK_CON_R1
MICROPHONE-105-GP-U
082.40011.0001

DMIC_CLK_CON_R — R2909 0R0402-PAD-1-GP — DMIC_CLK_CON 27
DMIC_DATA_CON_R — R2911 0R0402-PAD-1-GP — DMIC_DATA_CON 27
DMIC_CLK_CON_R1 — 0R2J-L-GP — R2912 DMIC_CLK_CON
DY DY DY DUAL
EC2903 EC2904 EC2905 SC4D7P50V2BN-GP

DMIC_DATA_R
R2919 0R2J-L-GP
SINGLE

DMIC_DATA_R1 — 0R2J-L-GP — R2913 DMIC_DATA_R
DY DUAL
EC2906 SC4D7P50V2BN-GP

DUAL MIC=082.40011.0001
SINGALE MIC=082.40011.0011
Single MIC 2nd=082.40002.0031

CLK_CON_MIC3
DATA_CON_MIC3
DY DY
EC2908 EC2907 SC4D7P50V2BN-GP

MIC3
3D3V_S0
CLK_CON_MIC3 — R2914
DATA_CON_MIC3 — R2915
0R0402-PAD-1-GP
DMIC_CLK_CON 27
DMIC_DATA_CON 27
PTWO-CON4-9-GP-U1
DY

11/30 SB

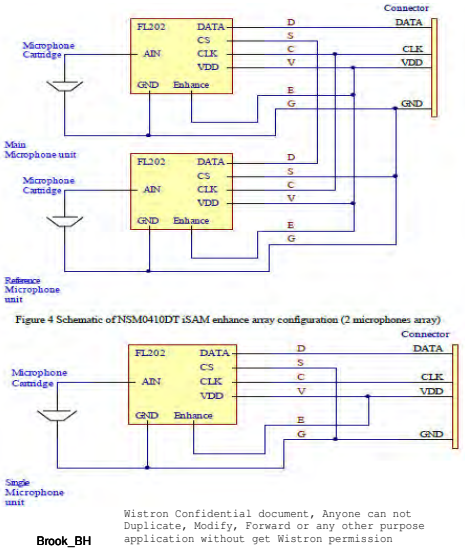

Figure 4 Schematic of NSM0410DT iSAM enhance array configuration (2 microphones array)

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Title: Audio Jack
Size: A3
Document Number: Brook_BH
Rev: -1M
Date: Thursday, February 12, 2015
Sheet 29 of 106

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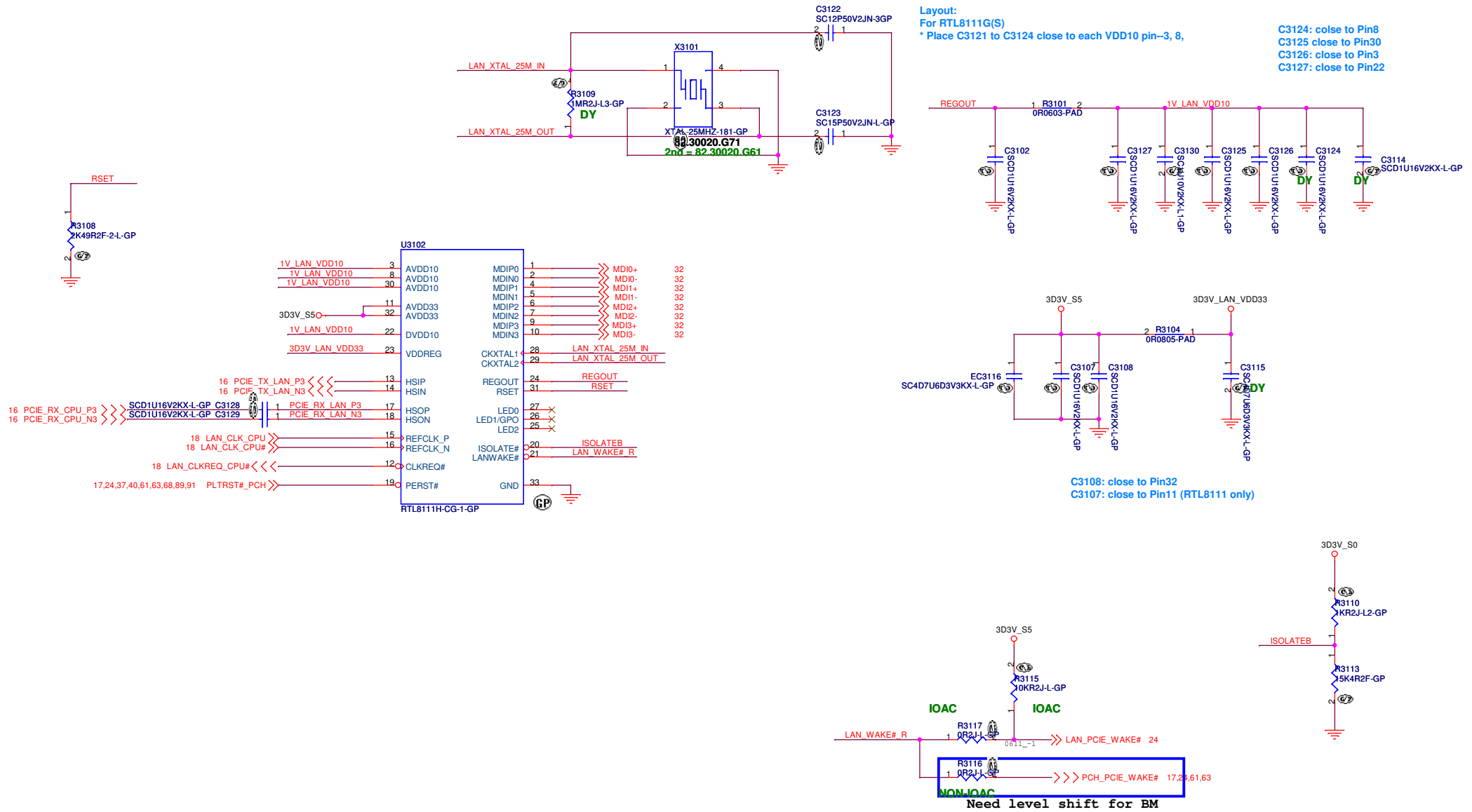

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Title: **LAN (RTL8111G(S))**

Size	Document Number	Rev
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Date: Wednesday, February 04, 2015 Sheet 31 of 106

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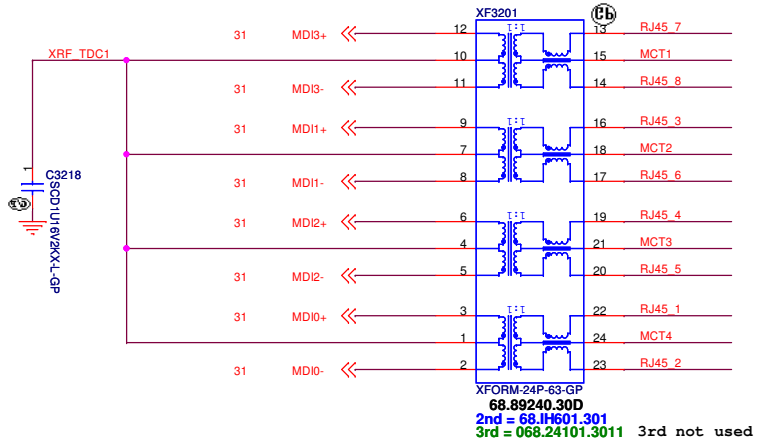
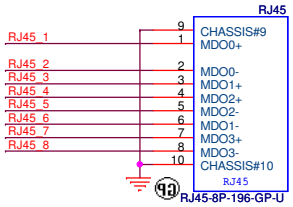
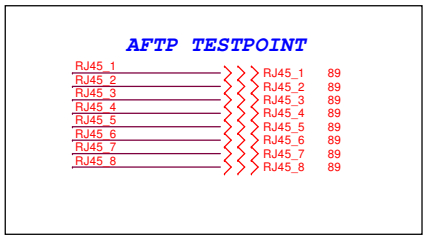
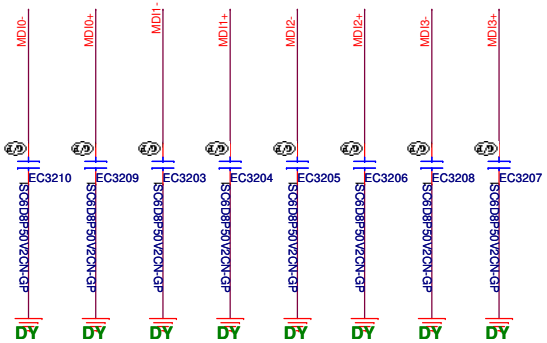
SSID = LAN

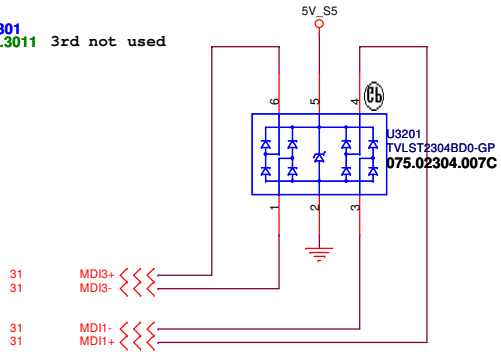


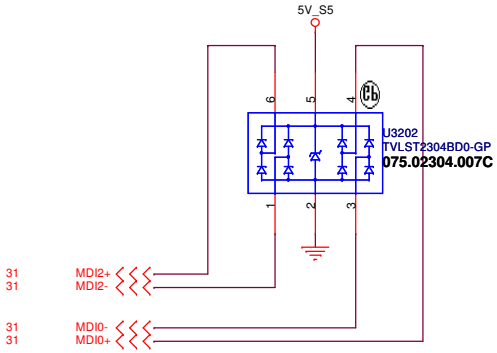


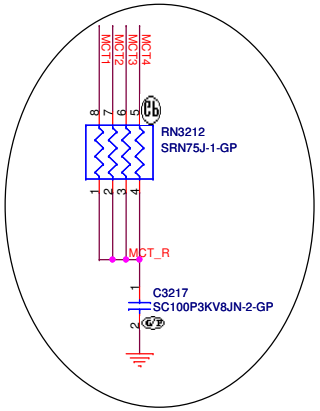
022.10001.00F1
2nd = 022.10001.0F21











12/23 修改家電下鄉 PD

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Title: **(LAN+VGA) CONNECTOR**

Size: A3 | Document Number: **Brook_BH** | Rev: **-1M**

Date: Wednesday, February 04, 2015 | Sheet 32 of 106

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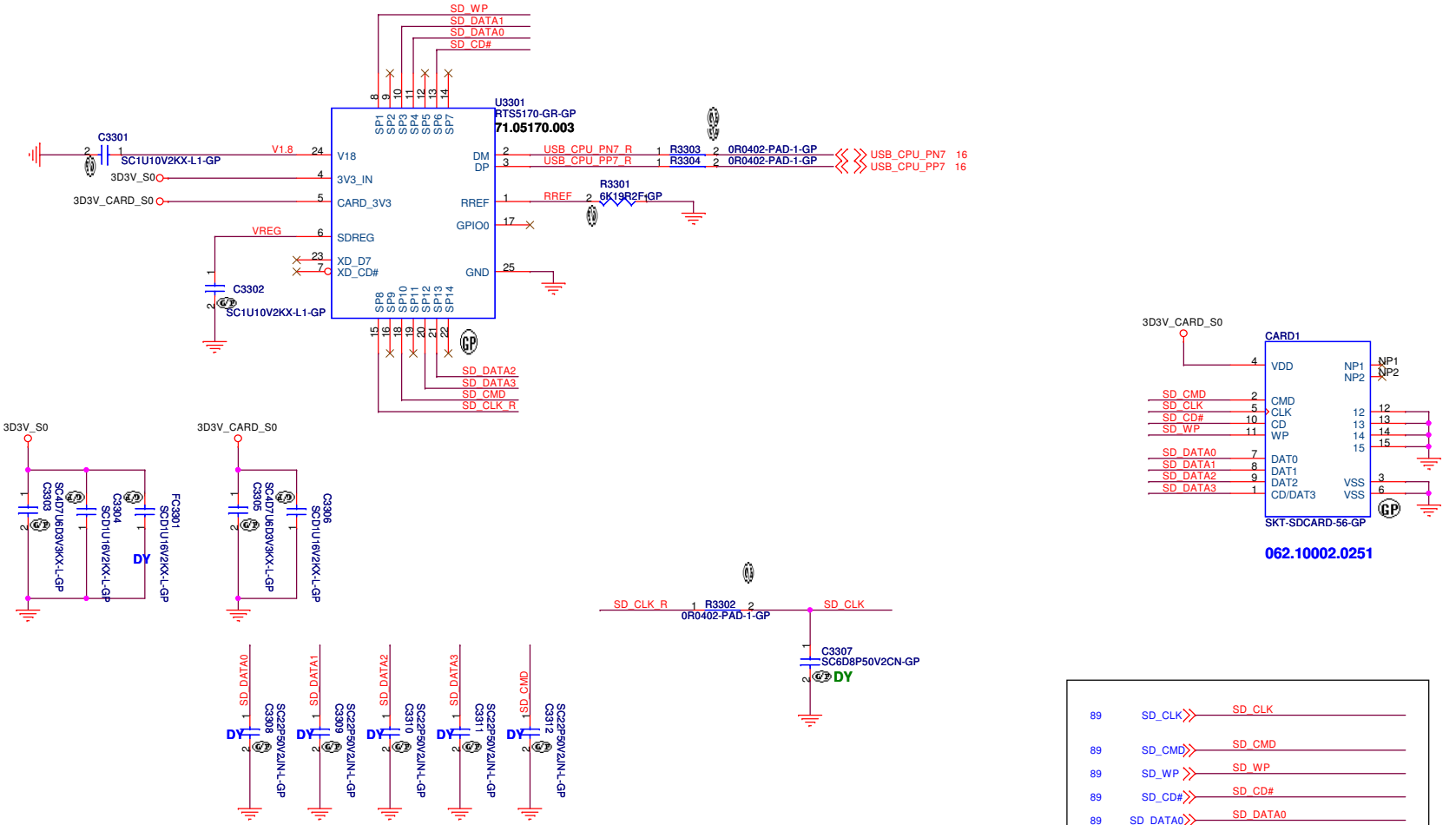

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Title: **Card Reader CONN (Reserved)**

Size	Document Number	Rev
A3	Brook_BH	-1M

Date: Wednesday, February 04, 2015 Sheet 33 of 106

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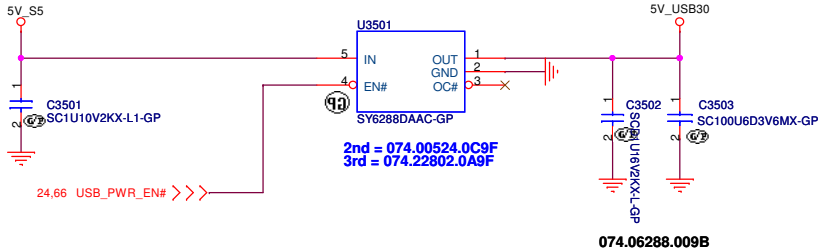
Low Active 2A



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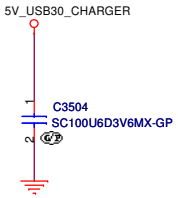
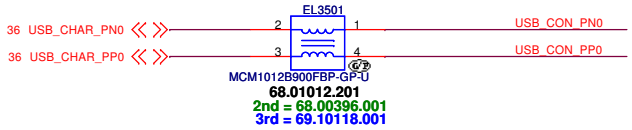


USB 3.0 Connector Pin definition		
1	POWER	
2	USB 2.0 D-	
3	USB 2.0 D+	
4	GND	
5	StdA_SSRX-	SuperSpeed RX
6	StdA_SSRX+	
7	GND	
8	StdA_SSTX-	SuperSpeed TX
9	StdA_SSTX+	



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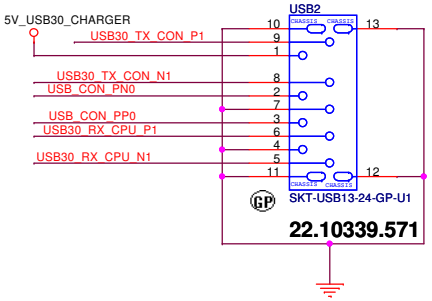

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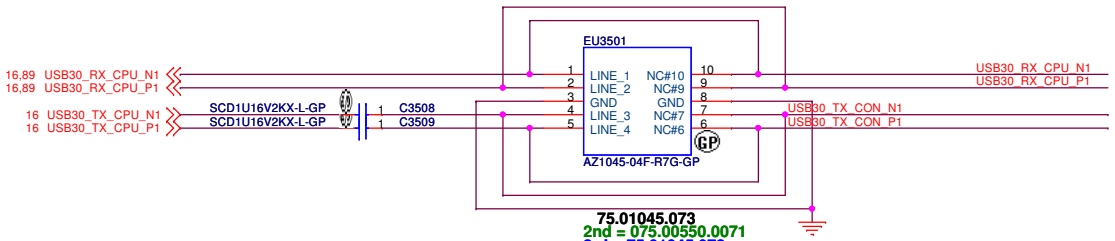

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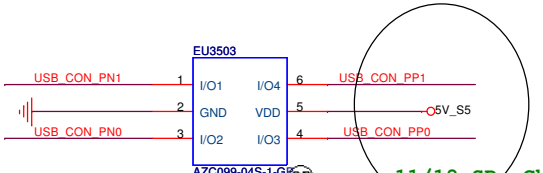

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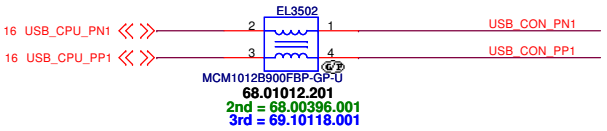
11/18 SB Change to 5V_S5

AFTP TESTPOINT

USB30_TX_CON_P1	USB30_TX_CON_P1 89
USB30_TX_CON_N1	USB30_TX_CON_N1 89
USB_CON_PN0	USB_CON_PN0 89
USB_CON_PP0	USB_CON_PP0 89
USB30_RX_CPU_P1	USB30_RX_CPU_P1 16,89
USB30_RX_CPU_N1	USB30_RX_CPU_N1 16,89
USB30_TX_CON_P2	USB30_TX_CON_P2 89
USB30_TX_CON_N2	USB30_TX_CON_N2 89
USB_CON_PN1	USB_CON_PN1 89
USB_CON_PP1	USB_CON_PP1 89
USB30_RX_CPU_P2	USB30_RX_CPU_P2 16,89
USB30_RX_CPU_N2	USB30_RX_CPU_N2 16,89



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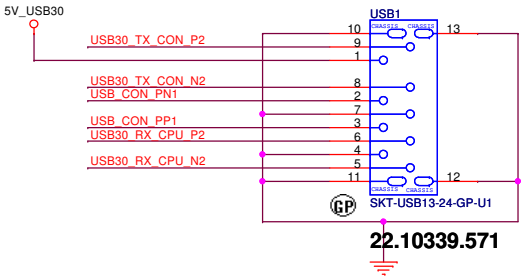

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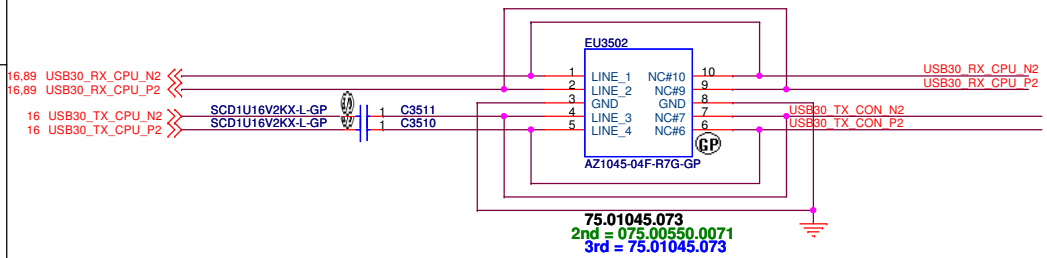

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Title: **USB_3.0**

Size	Document Number	Rev
A3	Brook_BH	-1M

Date: Tuesday, February 10, 2015 Sheet 35 of 106

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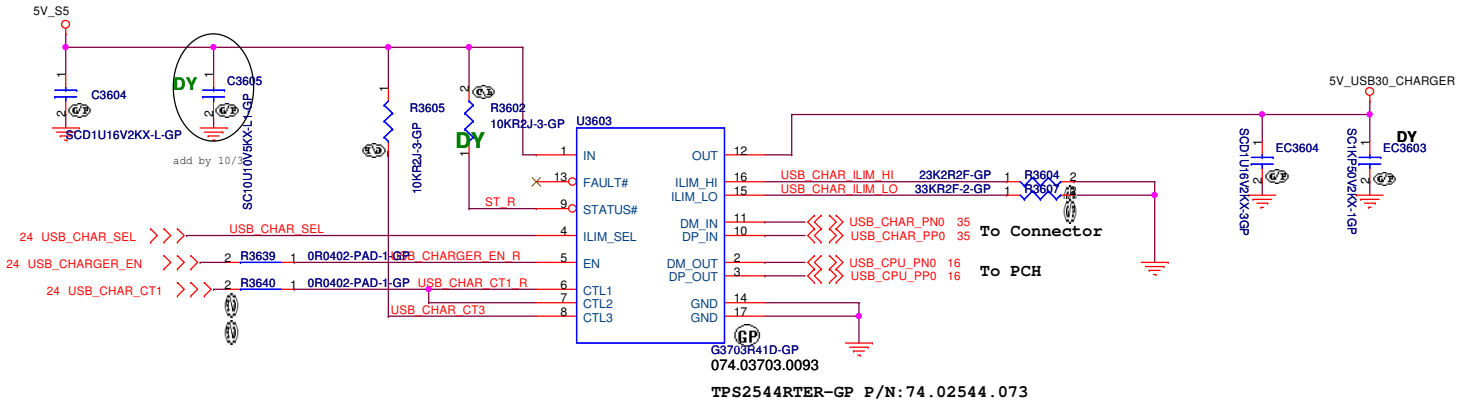

	Device Control Pins			
Flow Line Condition	CTL1	CTL2	CTL3	ILIM_SEL
DCH	0	0	0	X
CDP	1	1	1	1
SDP2	1	1	1	0
SDP1	1	1	0	X
	0	1	0	X
DCP_SHORT	1	0	0	X
DCP_DIVIDER	1	0	1	X
DCP_Auto	0	0	1	0
	0	1	1	X

3.Electrical Safety for USB3.0 Port

2.0 A <= Measurement value <= 2.2 A : Pass

1.9 A <= Measurement value < 2.0 A or 2.2 A < Measurement value <= 2.4 A : Marginal

If this result is "Marginal", 4 more samples (Total 5 samples) must be measured for each port.

And it must be confirmed that the values of 5 samples can meet our requirement (1.9 A ~ 2.4 A).

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Title: **USB Charger**

Size	Document Number	Rev
A3	Brook_BH	-1M

Date: Wednesday, February 04, 2015 Sheet 36 of 106

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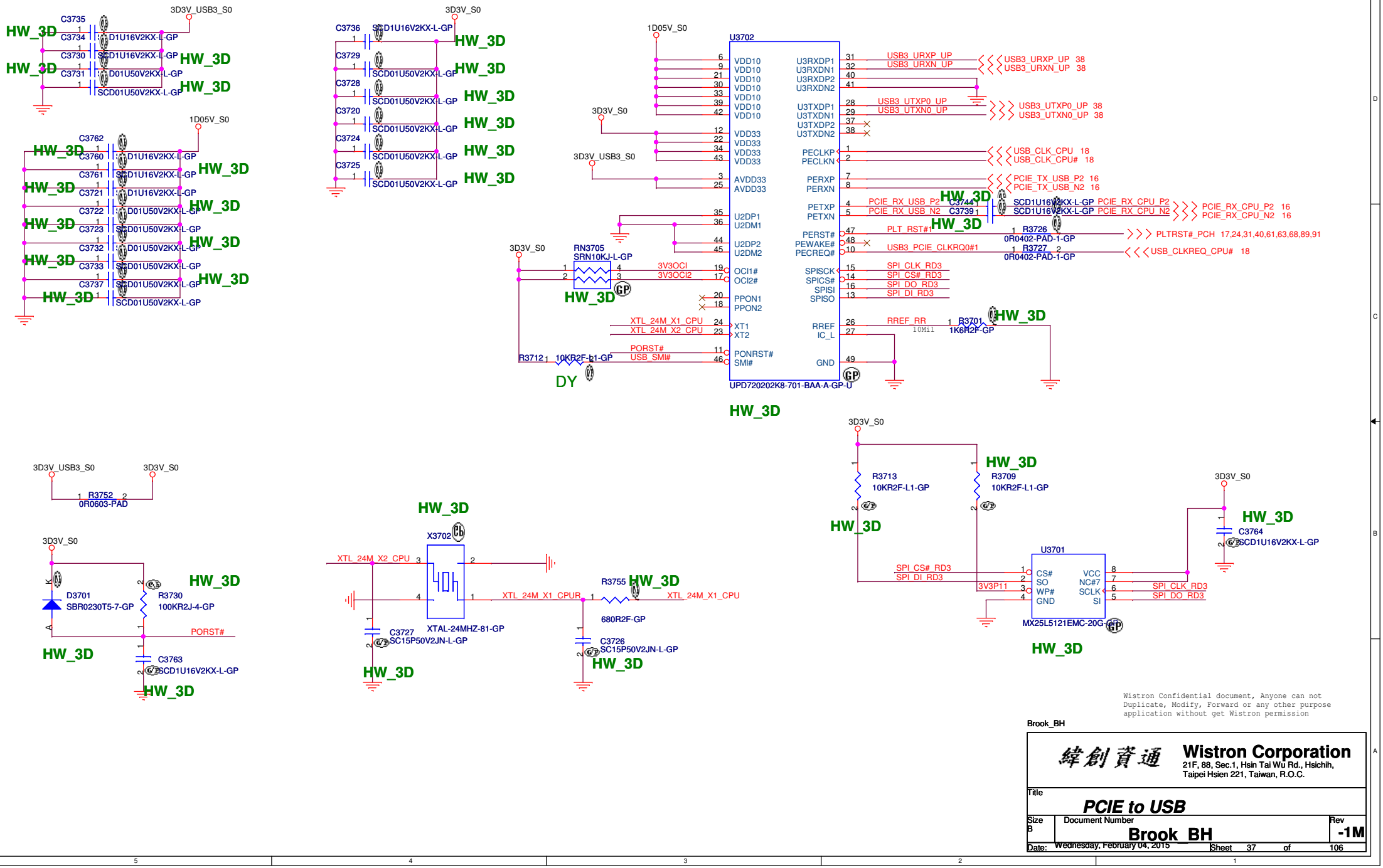

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Title: **PCIE to USB**

Size	Document Number	Rev
B	Brook_BH	-1M

Date: Wednesday, February 04, 2015 Sheet 37 of 106

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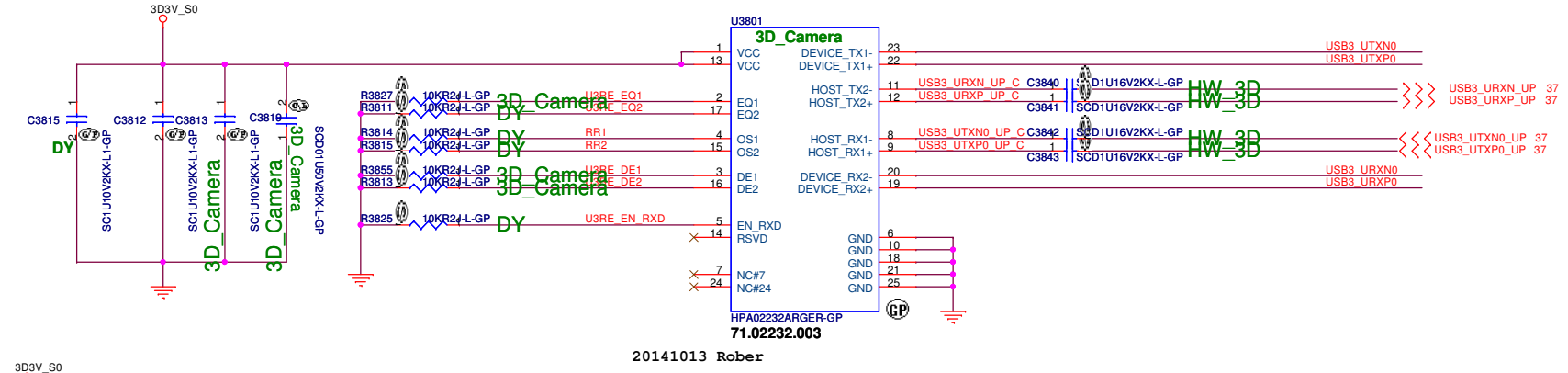
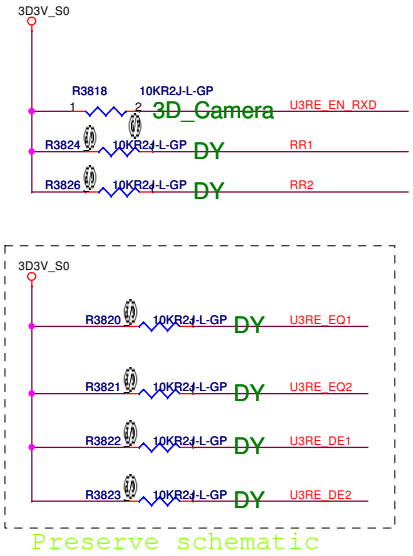
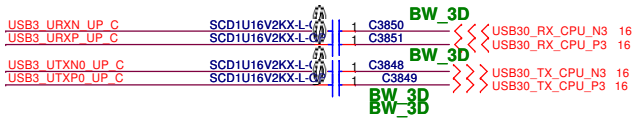
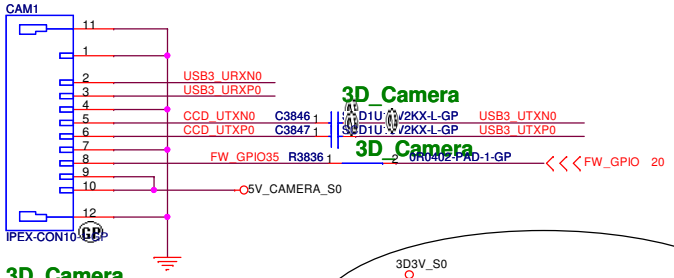


20141013 Rober



for Broadwell 3D Camera





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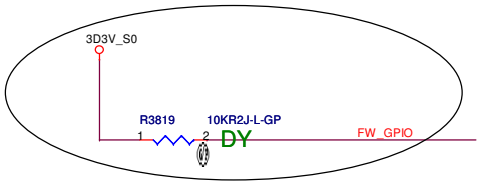
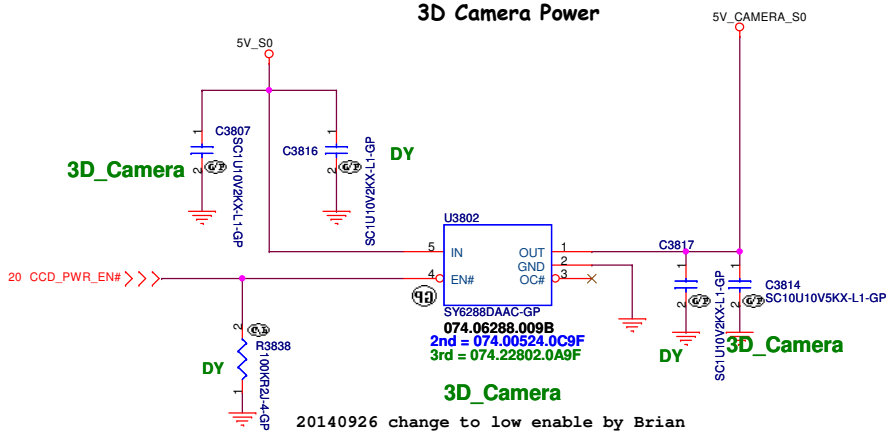


3D Camera Power



20140926 change to low enable by Brian

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Title: USB Redriver

Size: A3 | Document Number: Brook_BH | Rev: -1M

Date: Wednesday, February 04, 2015 | Sheet 38 of 106

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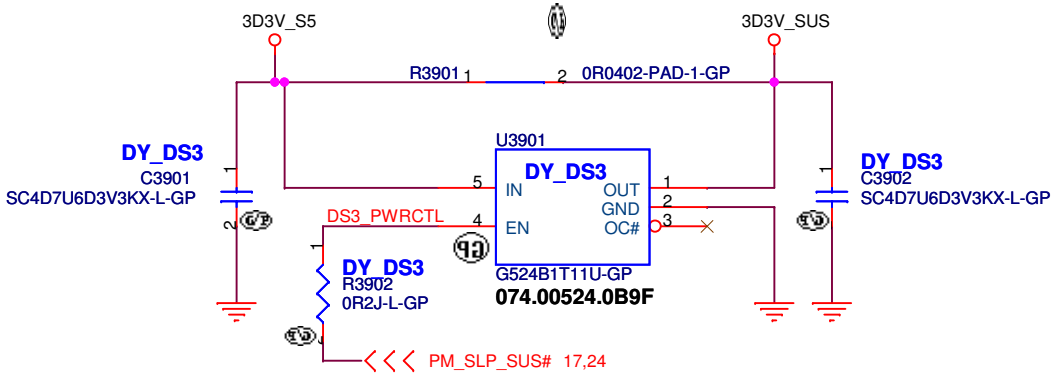

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Title: ***DS3***

Size	Document Number	Rev
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Date: Wednesday, February 04, 2015 Sheet 39 of 106

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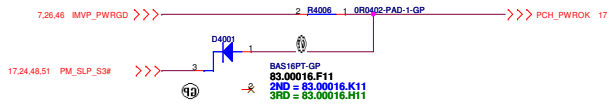
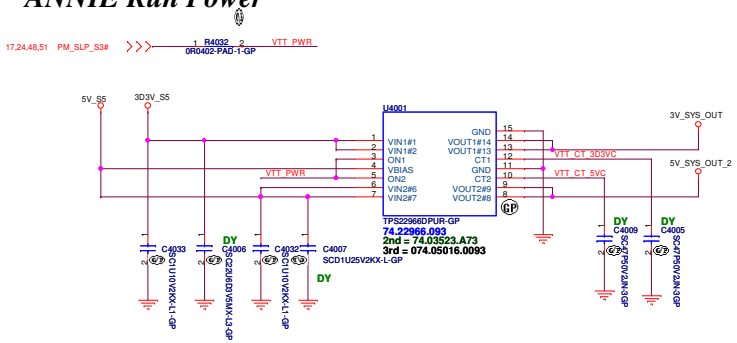
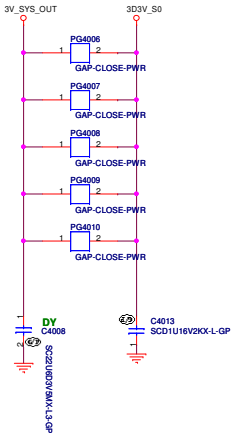
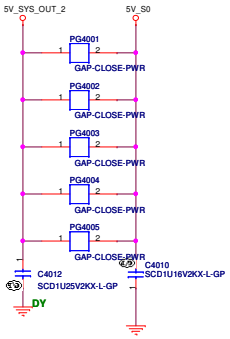
Power Sequence



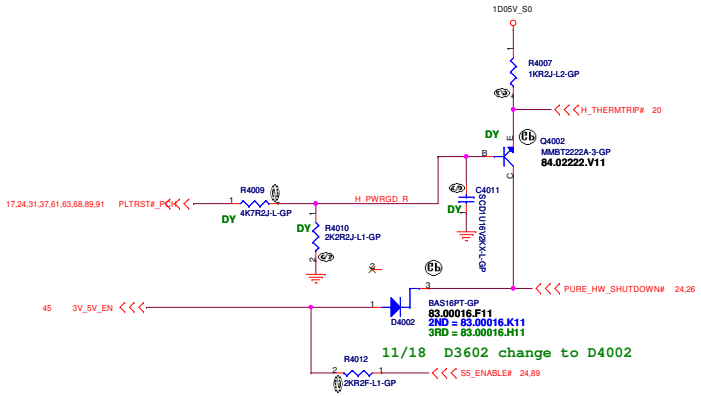
ANNIE Run Power

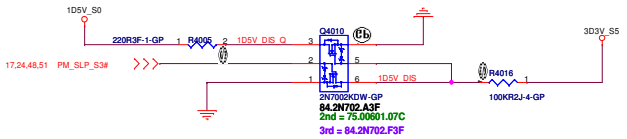






Discharge circuit





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Title: Connected Standby1

Size: A2 | Document Number: Brook_BH | Rev: -1M

Date: Wednesday, February 04, 2015 | Sheet 40 of 106

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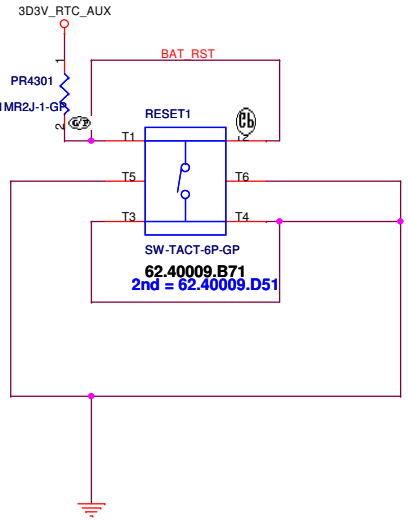
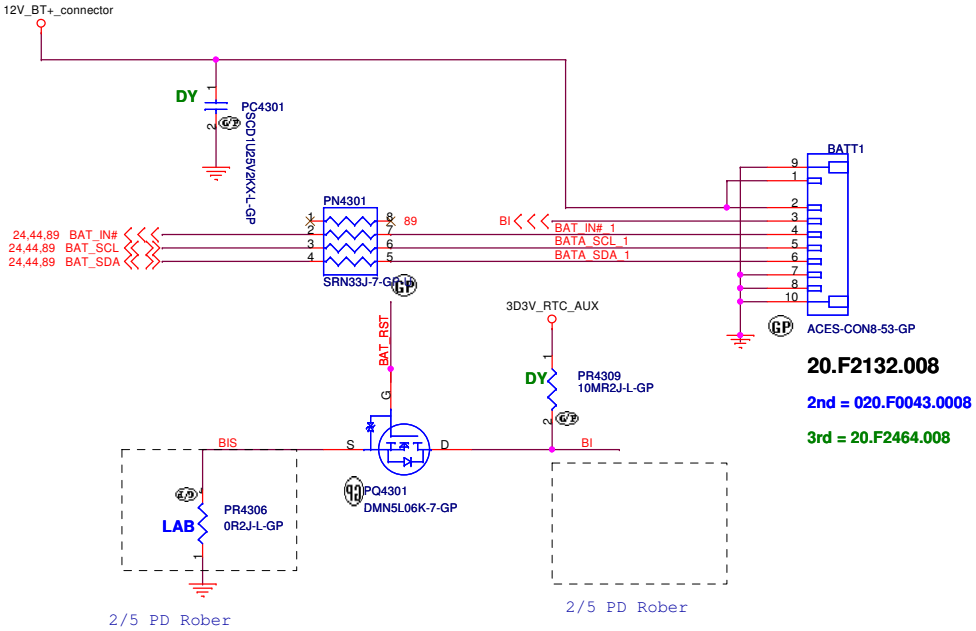
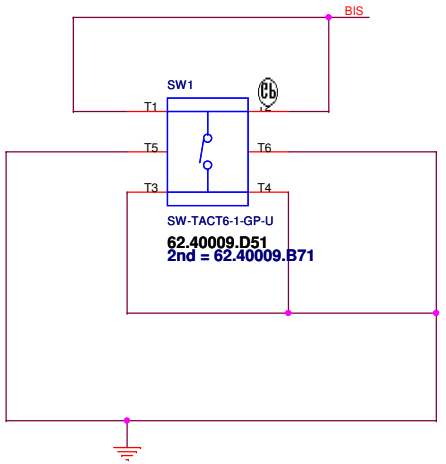
Battery Reset



Battery Connector

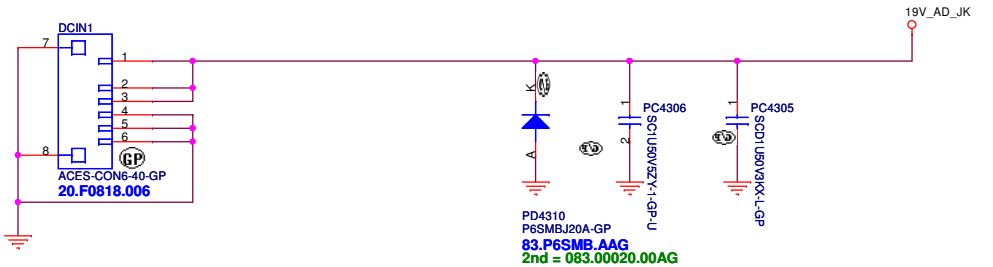


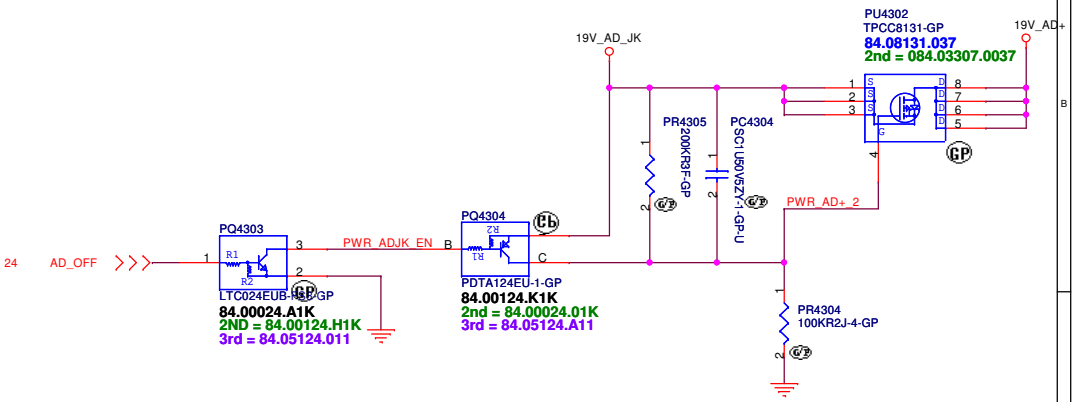
Battery Insert



ANNIE solution

Adaptor in to generate DCBATOUT





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Title	***DCIN JACK&BATT CONN***	
Size A3	Document Number **Brook_BH**	Rev **-1M**
Date: Thursday, February 05, 2015	Sheet 43 of 106	

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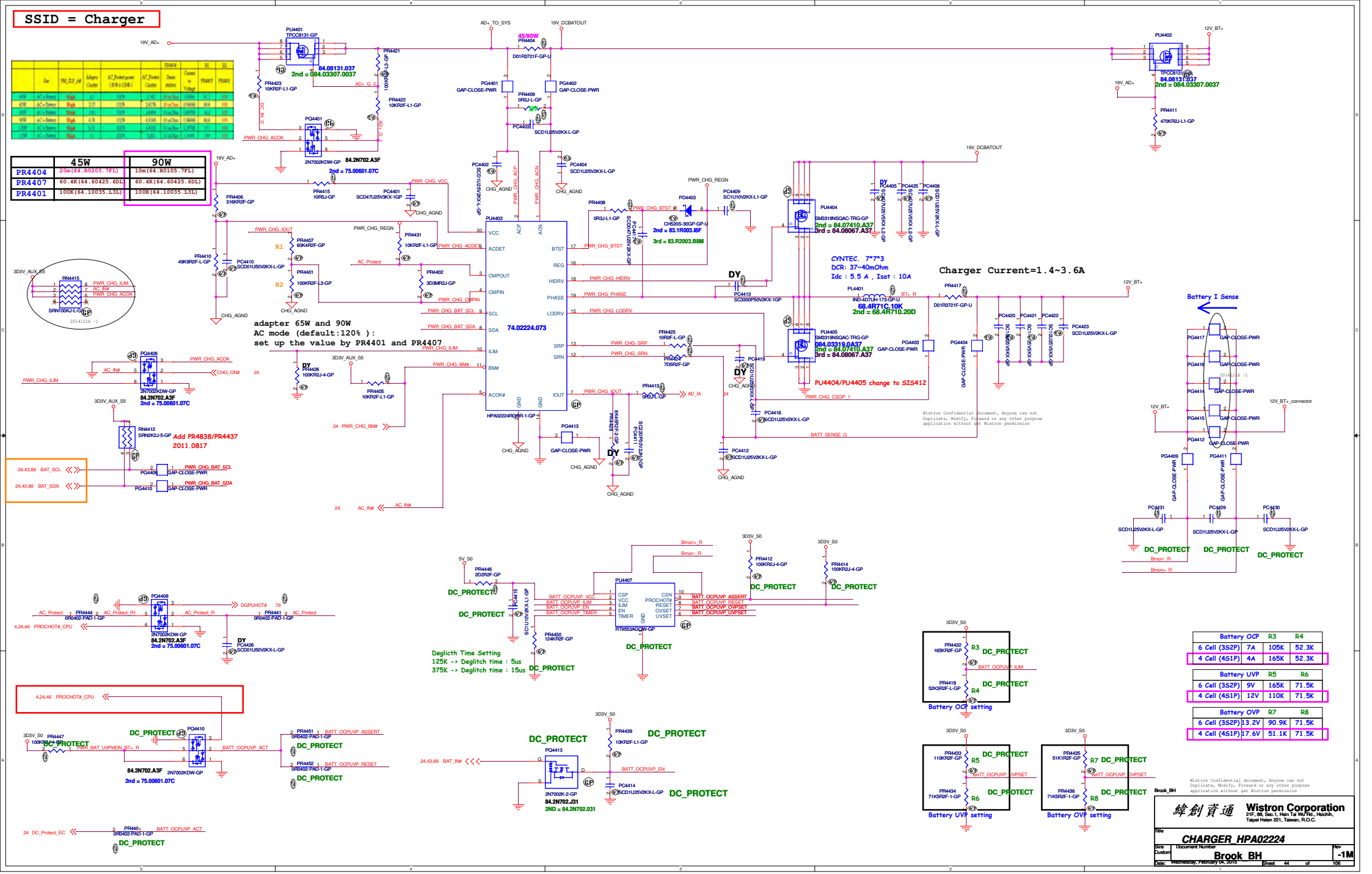

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SSID = PWR.Plane.Regulator_3p3v5v

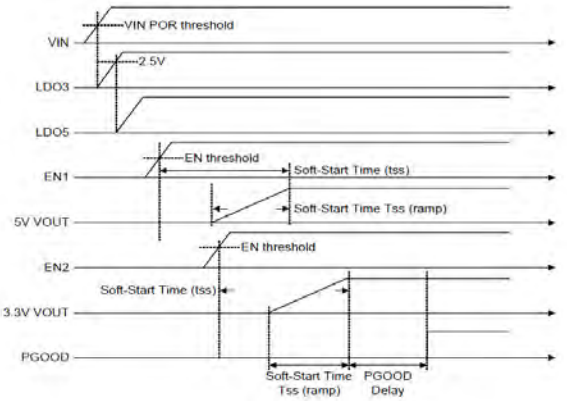
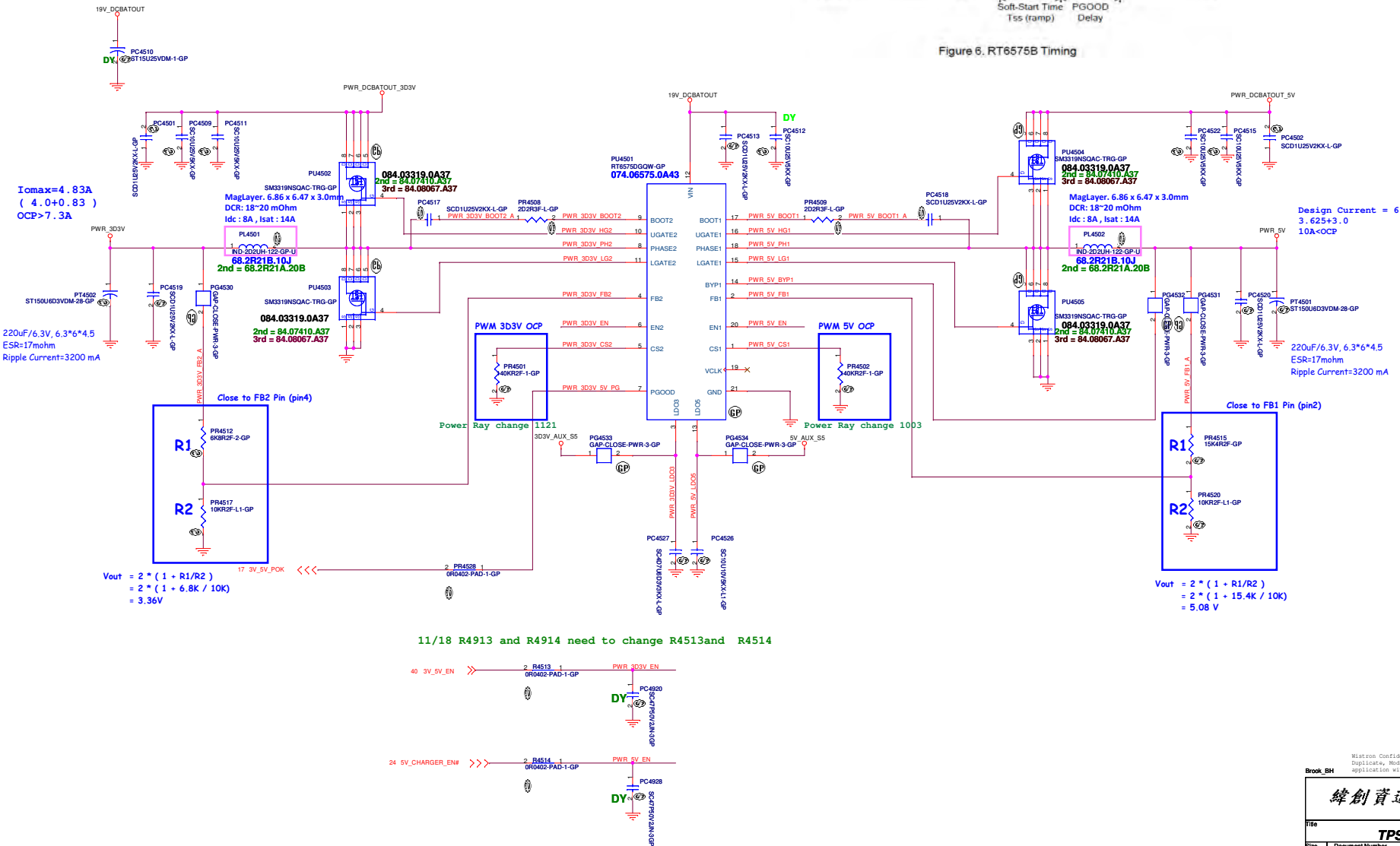


Figure 6. RT6575B Timing



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Title: TPS51225_5V/3D3V

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Date: Wednesday, February 04, 2015 | Sheet 45 of 106

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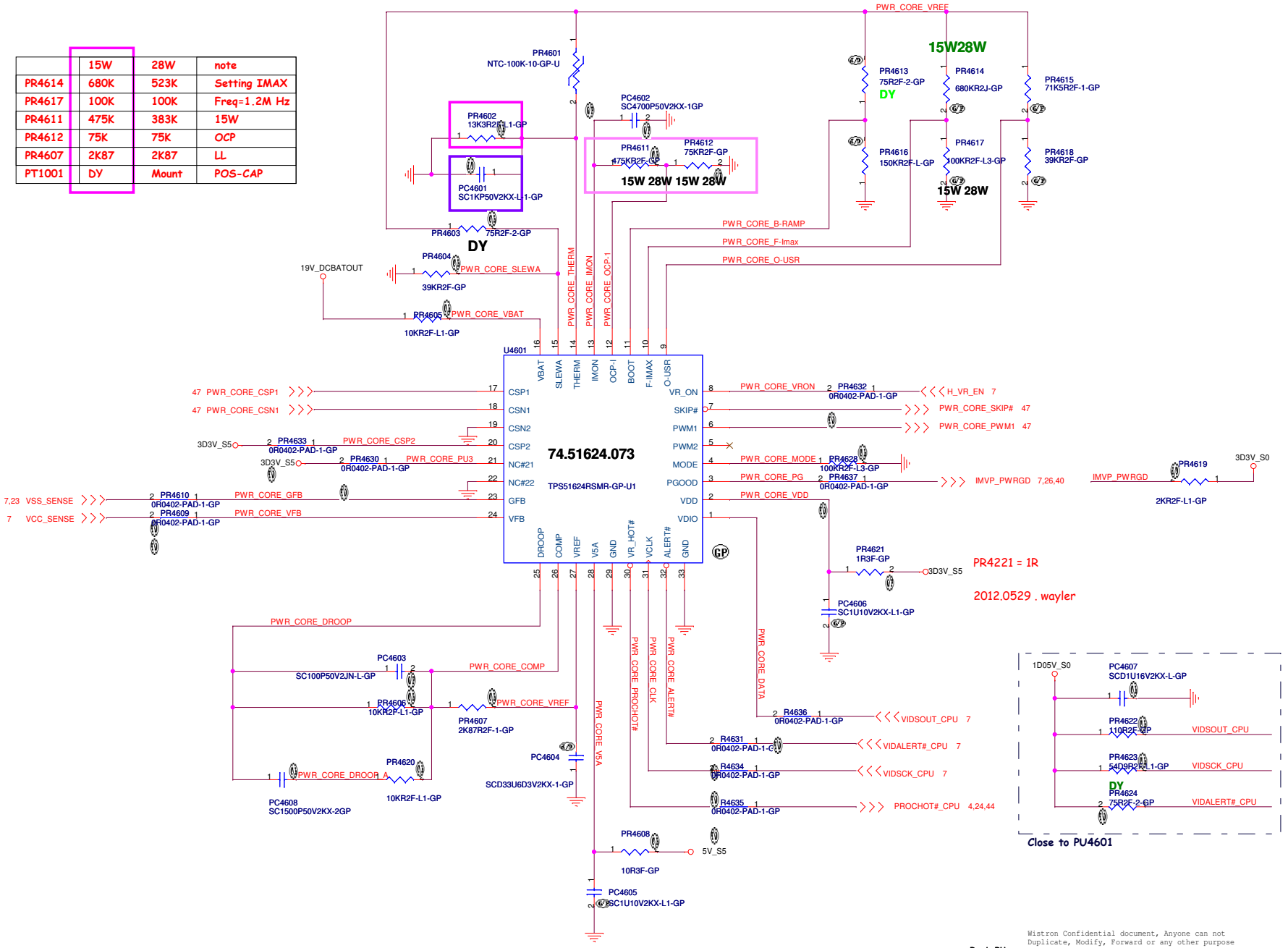
SSID = CPU.Regulator

	15W	28W	note
PR4614	680K	523K	Setting IMAX
PR4617	100K	100K	Freq=1.2M Hz
PR4611	475K	383K	15W
PR4612	75K	75K	OCP
PR4607	2K87	2K87	LL
PT1001	DY	Mount	POS-CAP



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Title: TPS51624_CPUCORE(1/2)

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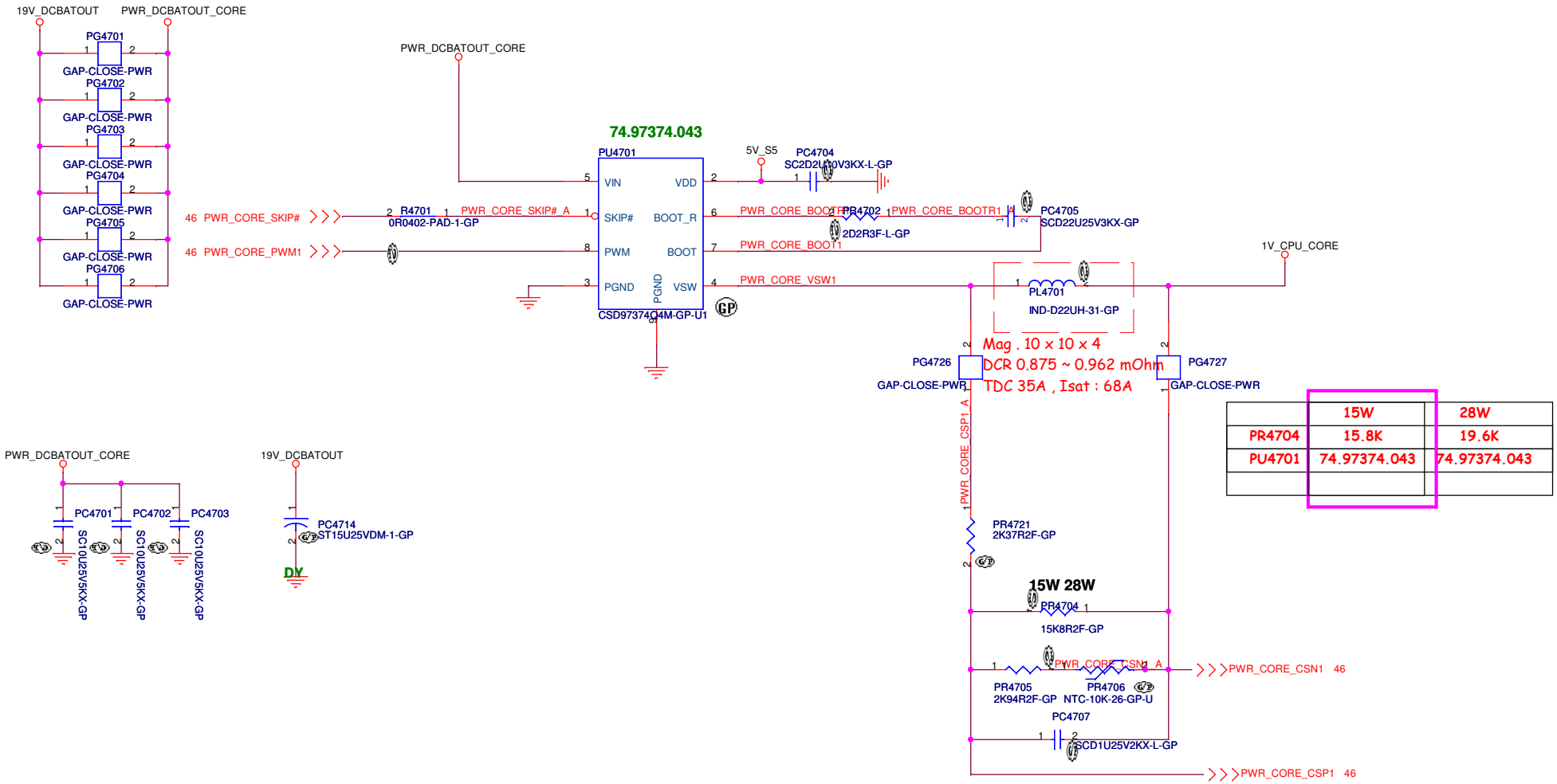

	15W	28W
PR4704	15.8K	19.6K
PU4701	74.97374.043	74.97374.043

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Title: TPS51624_CPUCORE(2/2)

Size: B | Document Number: Brook_BH | Rev: -1M

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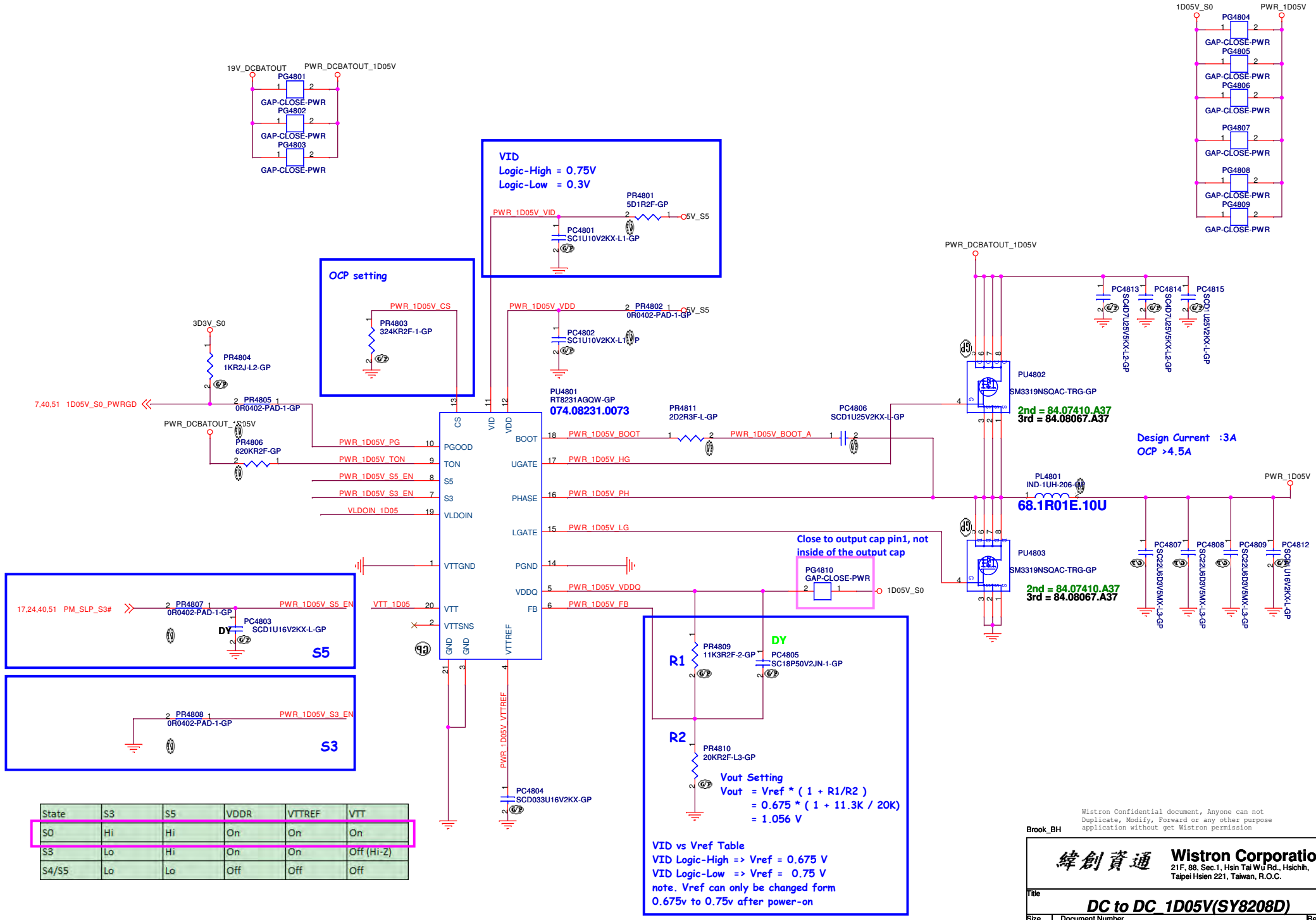

State	S3	S5	VDDR	VTTREF	VTT
S0	Hi	Hi	On	On	On
S3	Lo	Hi	On	On	Off (Hi-Z)
S4/S5	Lo	Lo	Off	Off	Off

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Title: **DC to DC_1D05V(SY8208D)**

Size	Document Number	Rev
A3	Brook_BH	-1M

Date: Thursday, February 05, 2015 Sheet 48 of 106

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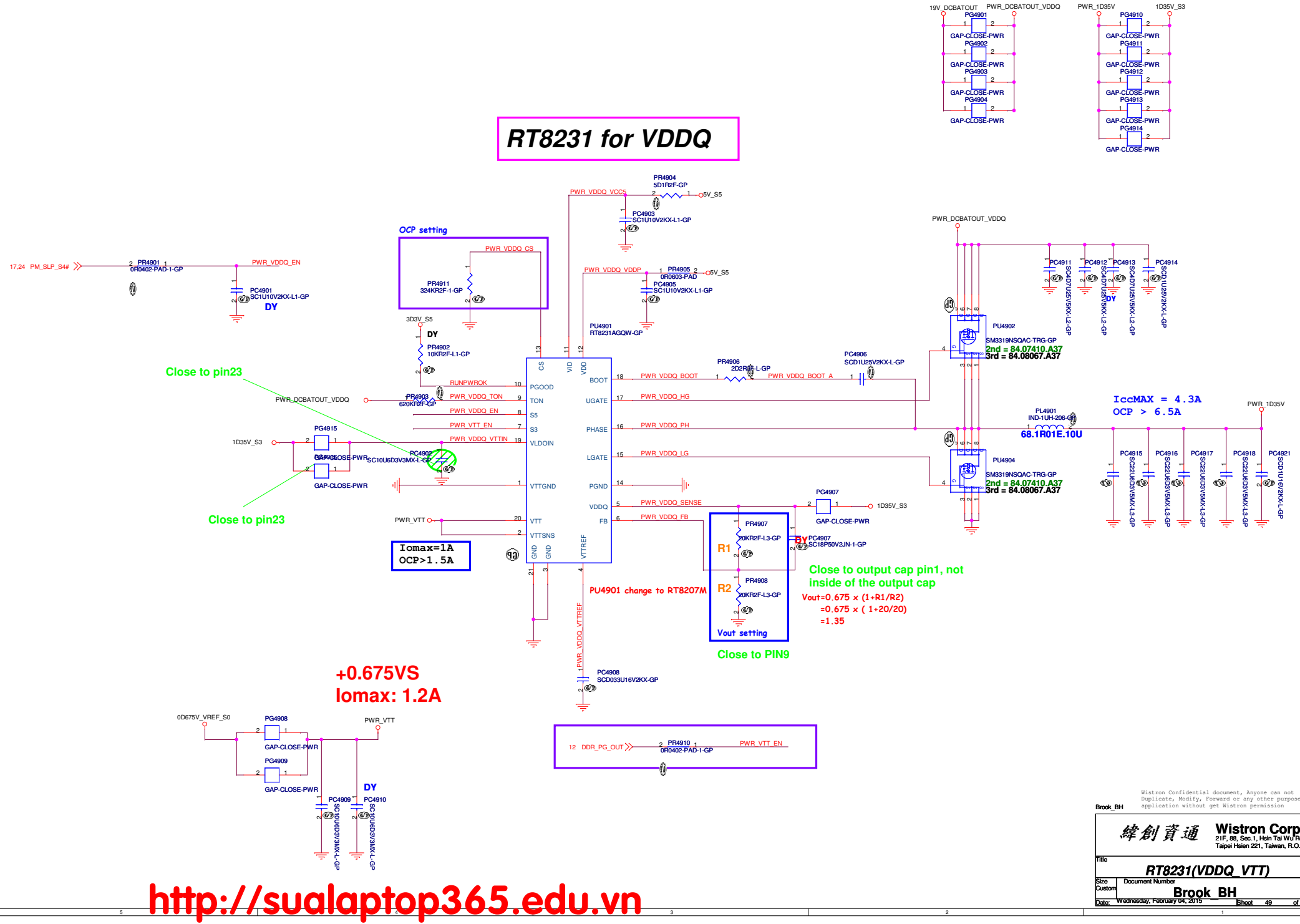
SSID = PWR.Plane.Regulator_1p2v0p6v

RT8231 for VDDQ



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Title: RT8231(VDDQ_VTT)

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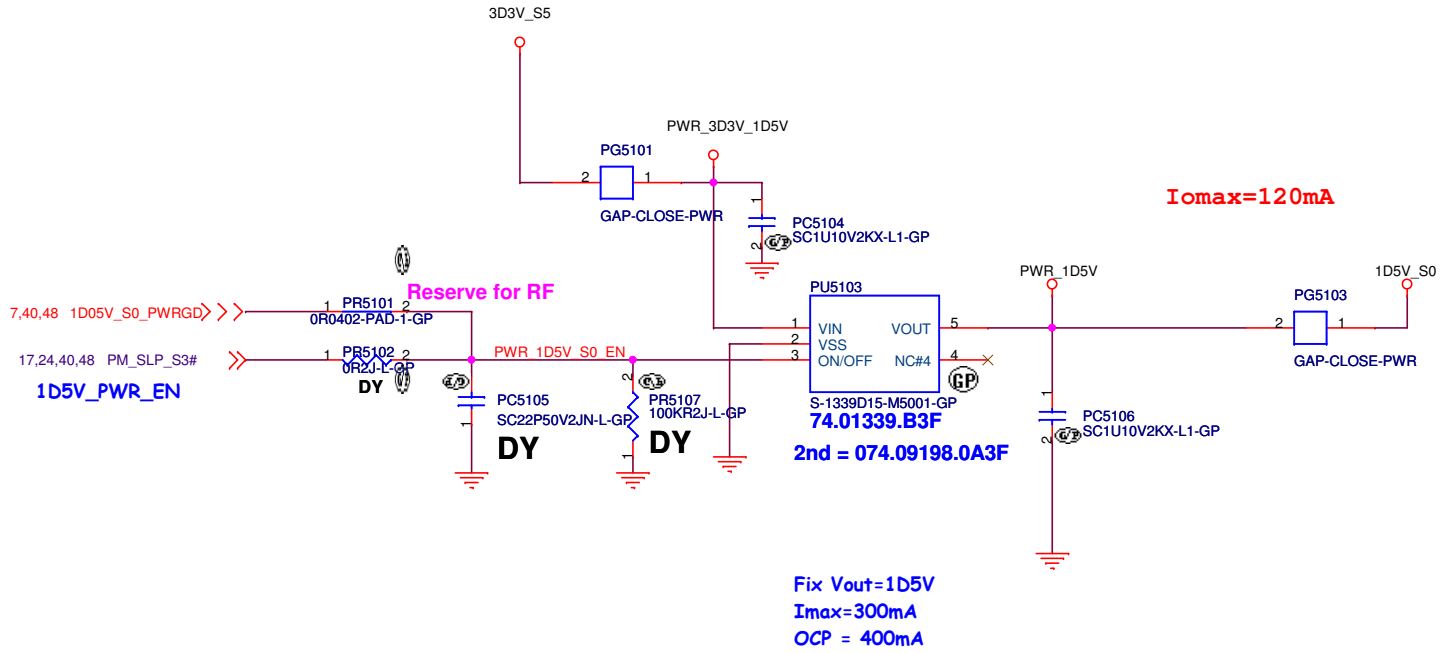
TLV70215 for 1D5V_S0
Enable=1.5V
Disable=0.4V



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Title: 1D5V_S0 SYW232

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Date: Wednesday, February 04, 2015 | Sheet 51 of 106

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Main Func = LCD

Pin count		
1		GND
2		eDP_AUX_CON_P
3		eDP_AUX_CON_N
4		GND
5		eDP_TX_CON_P0
6		eDP_TX_CON_N0
7		GND
8		eDP_TX_CON_P1
9		eDP_TX_CON_N1
10	Display	GND
11		eDP_TX_CON_P2
12		eDP_TX_CON_N2
13		GND
14		eDP_TX_CON_P3
15		eDP_TX_CON_N3
16		eDP_HPD_CON
17		LCDVDD(3V)
18		LCDVDD(3V)
19		LCDVDD(3V)
20		LCDVDD(3V)
21		TOUCH_DET#
22		TOUCH_GND/ TOUCH_RST
23		TOUCH_EN/ TOUCH_INT
24	Touch	Touch_PWR(3V/5V)
25		USB_PN6/ SCL
26		USB_PP6/ SDA
27		3D3V_CAMERA_S0
28	CCD	USB_CAMERA_P
29		USB_CAMERA_N
30		GND
31	GND	GND
32		GND
33		GND
34		
35		
36		
37		DCBATOUT_LCD
38		DCBATOUT_LCD
39	DCBATOUT	DCBATOUT_LCD
40		DCBATOUT_LCD

LCD1

eDP_AUX_CON_P → C5501 SCD1U16V2KX-L-GP → eDP_AUX_CPU_P 8
eDP_AUX_CON_N → C5505 SCD1U16V2KX-L-GP → eDP_AUX_CPU_N 8
eDP_TX_CON_P0 → C5506 SCD1U16V2KX-L-GP → eDP_TX_CPU_P0 8
eDP_TX_CON_N0 → C5507 SCD1U16V2KX-L-GP → eDP_TX_CPU_N0 8
eDP_TX_CON_P1 → C5517 SCD1U16V2KX-L-GP → eDP_TX_CPU_P1 8
eDP_TX_CON_N1 → C5518 SCD1U16V2KX-L-GP → eDP_TX_CPU_N1 8
eDP_TX_CON_P2 → C5519 SCD1U16V2KX-L-GP → eDP_TX_CPU_P2 8
eDP_TX_CON_N2 → C5520 SCD1U16V2KX-L-GP → eDP_TX_CPU_N2 8
eDP_TX_CON_P3 → C5521 SCD1U16V2KX-L-GP → eDP_TX_CPU_P3 8
eDP_TX_CON_N3 → C5522 SCD1U16V2KX-L-GP → eDP_TX_CPU_N3 8
eDP_HPD_CON
3D3V_LCDVDD_PWR → R5501 0R0805-PAD → 3D3V_LCDVDD_S0

TOUCH_DETR# → R5524 33R2J-L1-GP → TOUCH_DET# 20
TOUCH_S_RST#_R → 33R2J-L1-GP → TOUCH_S_RST# 20
TOUCH_INTR# R5522 → 33R2J-L1-GP → TOUCH_INT# 20
TS_S0 → 33R2J-L1-GP
TS_USB_CON_N
TS_USB_CON_P
USB_CON_PP6
USB_CON_PN6
3D3V_CAMERA_S0
eDP_BLEN_CON
eDP_BLCTRL_CON → R5520 33R2J-L1-GP → eDP_BLCTRL_CPU 15
19V_DCBATOUT_LCD
STAR-CON-GP

R5526 0R2J-L-GP → TS_USB
R5515 33R2J-L1-GP → TS_I2C

TS

20140926 Rober

20.K0809.040
2nd = 20.K0678.040

Inverter Power

19V_DCBATOUT_LCD → C5502 SC4D7U25V5KX-L2-GP
C5504 SCD1U25V2KX-L-GP
F5501 POLYSW-1D1A24V-GP-U
69.50007.A31
2nd = 69.50007.A41
19V_DCBATOUT

eDP_BLEN_CON → RN5513 SRN1KJ-7-GP → BLON_OUT 24
eDP_HPD_CON → eDP_HPD_CPU 15
eDP_HPD_CON → RN5514 SRN100KJ-7-GP
eDP_BLEN_CON

20141216 -1

TS_I2C

R5523 0R2J-L-GP
R5524 0R2J-L-GP
I2C0_DATA_CPU 20
I2C0_CLK_CPU 20

TS_I2C
TS_USB
TS_USB_CON_P
TS_USB_CON_N
EL5503
MCM1012B900FBP-GP-U
68.01012.201
2nd = 68.00396.001
3rd = 69.10118.001
USB_CPU_PP5 16
USB_CPU_PN5 16

USB_CON_PP6 → EL5504 → USB_CPU_PP6 16
USB_CON_PN6 → USB_CPU_PN6 16
MCM1012B900FBP-GP-U
68.01012.201
2nd = 68.00396.001
3rd = 69.10118.001

USB_CON_PP6 → USB_CON_PP6 89
USB_CON_PN6 → USB_CON_PN6 89
TS_USB_CON_N → TS_USB_CON_N 89
TS_USB_CON_P → TS_USB_CON_P 89
3D3V_CAMERA_S0 → 3D3V_CAMERA_S0 89
TOUCH_DETR# → TOUCH_DETR# 89
TOUCH_S_RST#_R → TOUCH_S_RST#_R 89
TS_S0 → TS_S0 89
eDP_TX_CON_P3 → eDP_TX_CON_P3 89
eDP_TX_CON_N3 → eDP_TX_CON_N3 89
eDP_TX_CON_P2 → eDP_TX_CON_P2 89
eDP_TX_CON_N2 → eDP_TX_CON_N2 89
eDP_AUX_CON_P → eDP_AUX_CON_P 89
eDP_AUX_CON_N → eDP_AUX_CON_N 89
eDP_TX_CON_P0 → eDP_TX_CON_P0 89
eDP_TX_CON_N0 → eDP_TX_CON_N0 89
3D3V_LCDVDD_PWR → 3D3V_LCDVDD_PWR 89
eDP_TX_CON_P1 → eDP_TX_CON_P1 89
eDP_TX_CON_N1 → eDP_TX_CON_N1 89
TOUCH_INTR# → TOUCH_INTR# 89
eDP_HPD_CON 89
eDP_BLEN_CON 89
eDP_BLCTRL_CON 89

AFTP TESTPOINT

T-COM Power

3D3V_LCDVDD_S0 → C5511 SC4D7U6D3V3KX-L-GP
C5508 SCD1U16V2KX-L-GP
C5509 SC1U10V2KX-L-GP
DY
3D3V_S0 → C5512 SC4D7U6D3V3KX-L-GP

15 eDP_VDDEN_CPU
Layout 40 mil
U5501 RT9724GB-GP
EN, GND, VOUT, VIN#5, VIN#4
R5509 100KR2J-4-GP
74.09724.09F
2ND = 74.03514.07F

USB_CON_PN6 → EU5504 AZC099-04S-1-GP → USB_CON_PP6
TS_USB_CON_N
TS_USB_CON_P
I/O1, I/O2, I/O3, I/O4, GND, VDD → 5V_S0
75.09904.07C
2nd = 75.00005.C7C
3rd = 075.01256.007C

Camera Power

3D3V_S0 → F5510 POLYSW-1D1A6V-9-GP-U → 3D3V_CAMERA_S0
69.48001.081
2ND = 69.50011.081
C5513 SC10U10V5KX-L1-GP
C5514 SCD1U16V2KX-L-GP

Touch panel Power

TS_S0
3D3V_S0 → R5744 DY 0R3J-L1-GP
5V_S0 → R5745 0R3J-L1-GP
TS
C5515 SC10U10V5KX-L1-GP
C5516 SCD1U16V2KX-L-GP
TS
20141216 -1

<Core Design>

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Title: LCD Connector
Size: A3
Document Number: Brook_BH
Rev: -1M
Date: Thursday, February 12, 2015
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SSID = Display

VGA RTD2168

Embedded LDO

Select VCCK_V12 source from external 1.2V or embedded LDO

3D3V_S0 — R5611 4K7R2J-L-GP — LDO_EN

C5603 SCD1U16V2KX-L-GP — 1D2V_VCCK_S0

20141013 Rober

close to pin25

LDO_EN(PIN21)	
0	1
VCCK_V12 from External 1.2V	VCCK_V12 from Embedded LDO

CRT_HPD — R5644 0R0402-PAD-1-GP — CRT_PCH_HPD 15

R5617 100KR2J-4-GP

3D3V_AVCC_S0 — L5604 PBY100505T-600Y-N-GP — C5618 SC10U10V5KX-L1-GP — C5616 SCD1U16V2KX-L-GP

close to pin24

3D3V_S0 — C5620 SCD1U16V2KX-L-GP

close to pin5

3D3V_DAC_S0 — L5605 PBY100505T-600Y-N-GP — C5619 SC10U10V5KX-L1-GP — C5617 SCD1U16V2KX-L-GP

close to pin9

C5621 SCD1U16V2KX-L-GP

close to pin20

CRT_RED — L5601 BLM18BB220SN-GP — C5604 SC10P50V2JN-L1-GP — C5605 SC10P50V2JN-L1-GP — CRT_RED_CON

CRT_GREEN — L5602 BLM18BB220SN-GP — C5606 SC10P50V2JN-L1-GP — C5607 SC10P50V2JN-L1-GP — CRT_GREEN_CON

CRT_BLUE — L5603 BLM18BB220SN-GP — C5608 SC10P50V2JN-L1-GP — C5609 SC10P50V2JN-L1-GP — CRT_BLUE_CON

RN5610 SRN150J-1-GP — RN5611 SRN150J-1-GP

those compoent need to close

L5601~3 change to 68.00084.B61

U5601 RTD2168-CGT-GP

3D3V_AVCC_S0	24 AVCC_33	HPD 1	CRT_HPD
1D2V_VCCK_S0	25 AVCC_12	SMB_SCL 2	SMB_SCL
	5 DVCC_33	SMB_SDA 3	SMB_SDA
3D3V_S0	20 DVCC_33	VGA_SCL 4	CRT_DDCCLK_CON
		VGA_SDA 6	CRT_DDCDATA_CON
1D2V_VCCK_S0	19 VCCK_12		
3D3V_DAC_S0	9 VDD_DAC_33	VSYNC 7	CRT_VSYNC
		HSYNC 8	CRT_HSYNC
LDO_EN	21 LDO_EN	RED_P 15	CRT_RED
		RED_N 16	
DP_AUX_CON_P	26 AUX_P	GREEN_P 12	CRT_GREEN
DP_AUX_CON_N	27 AUX_N	GREEN_N 13	
DDI_VGA_DATA_C_P0	29 LANE0P	BLUE_P 10	CRT_BLUE
DDI_VGA_DATA_C_N0	30 LANE0N	BLUE_N 11	
DDI_VGA_DATA_C_P1	31 LANE1P	POL1_SDA 22	POL1_SDA
DDI_VGA_DATA_C_N1	32 LANE1N	POL2_SCL 23	POL1_SCL
	17 XI/CKIN	GND_DAC 14	
	18 XO	GND 33	
RRX	28 RRX		

RN5612 SRN4K7J-8-GP — 20141216 -1

15 PCH_DPC_AUXP — C5615 SCD1U16V2KX-L-GP — DP_AUX_CON_P

15 PCH_DPC_AUXN — C5614 SCD1U16V2KX-L-GP — DP_AUX_CON_N

8 DDI_VGA_DATA_CPU_P0 — C5613 SCD1U16V2KX-L-GP — DDI_VGA_DATA_C_P0

8 DDI_VGA_DATA_CPU_N0 — C5612 SCD1U16V2KX-L-GP — DDI_VGA_DATA_C_N0

8 DDI_VGA_DATA_CPU_P1 — C5611 SCD1U16V2KX-L-GP — DDI_VGA_DATA_C_P1

8 DDI_VGA_DATA_CPU_N1 — C5610 SCD1U16V2KX-L-GP — DDI_VGA_DATA_C_N1

20140926 Rober

R5610 12KR2F-L-GP

20141013 Rober

5V_CRT_S0 — 5V_HDMI_S0 — D5601 CH551H-30PT-GP

83.R5003.C8F

2ND = 83.R5003.H8H

3rd = 83.5R003.08F

RN5601 SRN2K2J-5-GP

CRT_DDCDATA_CON — CRT_DDCCLK_CON

C5622 SCD1U16V2KX-L-GP — C5623 SC2D2U10V3KX-L-GP — 1D2V_VCCK_S0

close to pin19

CRT_VSYNC — R5605 36R2F-1-GP — C5601 SC10P50V2JN-L1-GP — CRT_VSYNC_CON

CRT_HSYNC — R5606 36R2F-1-GP — C5602 SC10P50V2JN-L1-GP — CRT_HSYNC_CON

CRT_DDCDATA_CON
CRT_DDCCLK_CON
CRT_RED_CON
CRT_GREEN_CON
CRT_BLUE_CON
CRT_VSYNC_CON
CRT_HSYNC_CON

CRT_DDCDATA_CON 89
CRT_DDCCLK_CON 89
CRT_RED_CON 89
CRT_GREEN_CON 89
CRT_BLUE_CON 89
CRT_VSYNC_CON 89
CRT_HSYNC_CON 89

AFTP TESTPOINT

Mode Configure Table(Power On Latch)

3D3V_S0 — R5613 4K7R2J-L-GP (DY) — POL1_SDA — R5614 4K7R2J-L-GP

3D3V_S0 — R5615 4K7R2J-L-GP — POL1_SCL — R5616 4K7R2J-L-GP (DY)

POL2_SCL(PIN23) \ POL1_SDA(PIN22)	0	1
0	X	EP MODE
1	ROM ONLY MODE	EEPROM MODE

RTD2168 Supports three operation mode for systemdesign.
Reserve 4.7K resistor pull high/low for mode selection
ROM ONLY Mode: PIN22 pull low, PIN23 pull high
EP Mode: PIN22 pull high, PIN23 pull low
EEPROM Mode: PIN22 pull high, PIN23 pull high

EEPROM MODE

3D3V_S0 — U5602 CAT24C128YI-GT3-GP — A0 A1 A2 GND (DY) VCC WP SCL SDA — POL1_SCL — POL1_SDA

VEDOR CHECK

In EEPROM mode,an additional EEPROM is needed. EEPROM should configure with following conditions. 1- EEPROM with a size of 16K-Byte
ROM or EEPROM mode: connect to PCH SMBUS
2- EEPROM device should be 2-byte addressing device
3- Slave address should configure as 0xA8

5V_CRT_S0 — C5632 SCD1U16V2KX-L-GP

CRT1 D-SUB-15-155-GP-U

CRT_DDCDATA_CON	12	VCC_CRT	9
CRT_DDCCLK_CON	15	DDCDATA_ID1	
		DDCCLK_ID3	
CRT_RED_CON	1	CRT_RED	
CRT_GREEN_CON	2	CRT_GREEN	
CRT_BLUE_CON	3	CRT_BLUE	
CRT_VSYNC_CON	14	VSYNC	
CRT_HSYNC_CON	13	HSYNC	
		NC#4	4
		NC#11	11
		GND	5
		GND	6
		GND	7
		GND	8
		GND	10
		GND	16
		GND	17

20.20984.015

2nd = 20.20938.015

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Title: VGA RTD2168

Size: A3 | Document Number: Brook_BH | Rev: -1M

Date: Thursday, February 12, 2015 | Sheet 56 of 106

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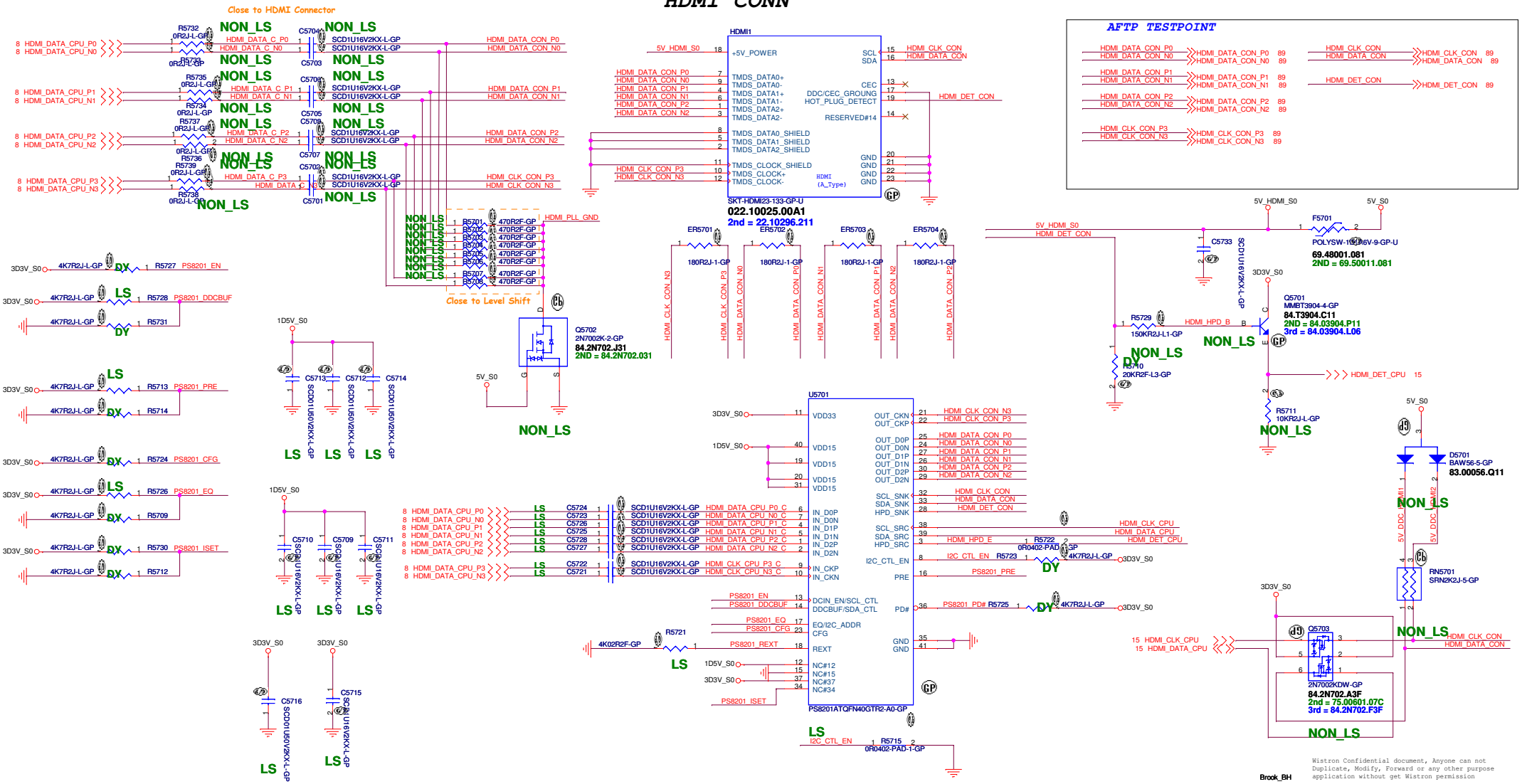
SSID = VIDEO

HDMI Level Shifter & CONN

HDMI CONN



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Title	HDMI Level Shifter&Conn	
Size: Custom	Document Number: Brook_BH	Rev: -1M
Date: Wednesday, February 04, 2015	Sheet 57 of 106	

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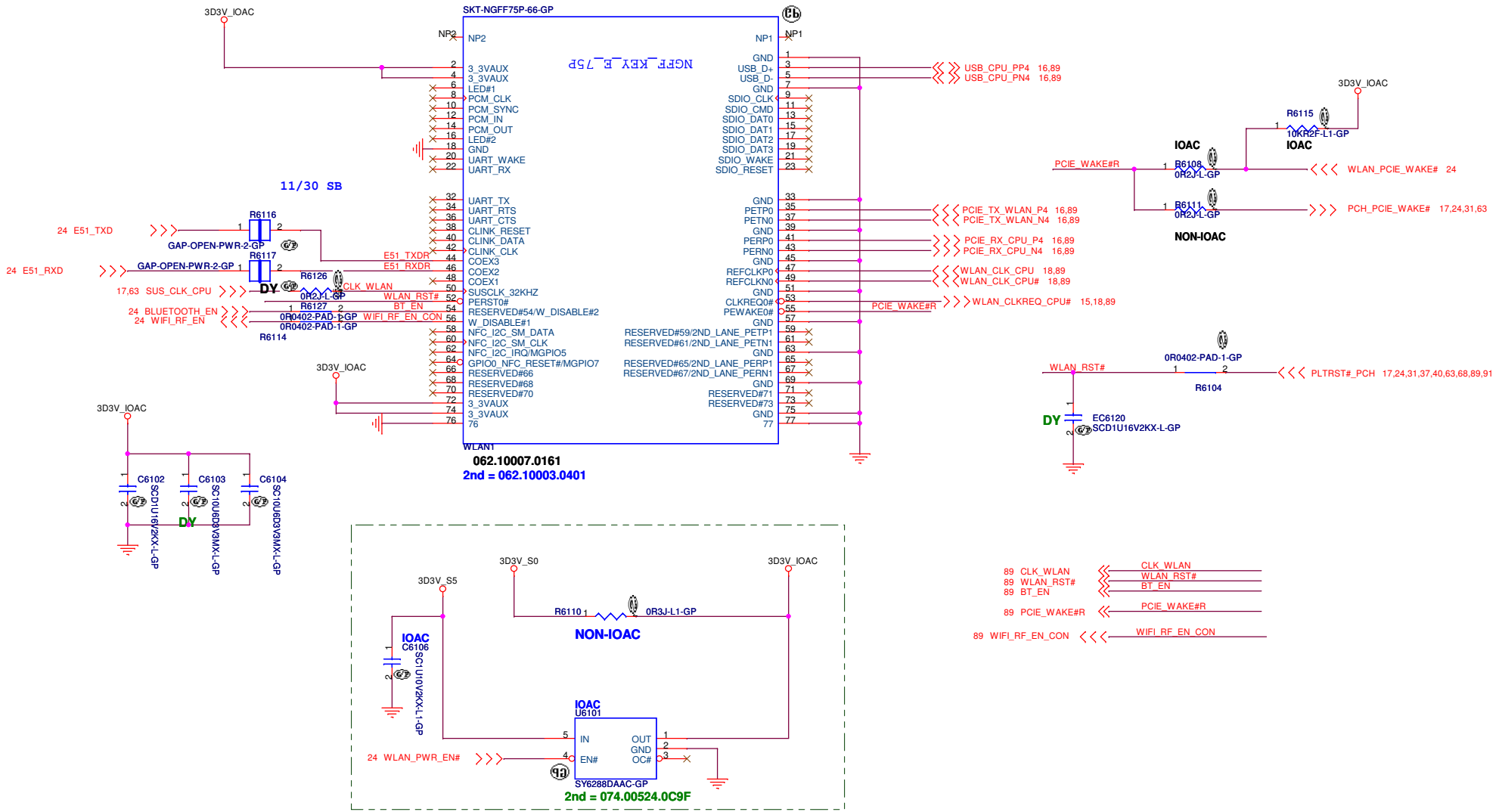
SSID = Wireless

Mini Card Connector(802.11a/b/g/n)



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<Core Design>

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Title: Mini Card WLAN

Size	Document Number	Rev
A3	Brook BH	-1M

Date: Wednesday, February 11, 2015 Sheet 61 of 106

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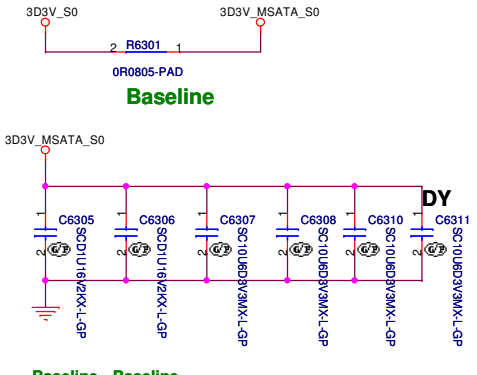
SSID = mSATA

Mini Card Connector(mSATA)



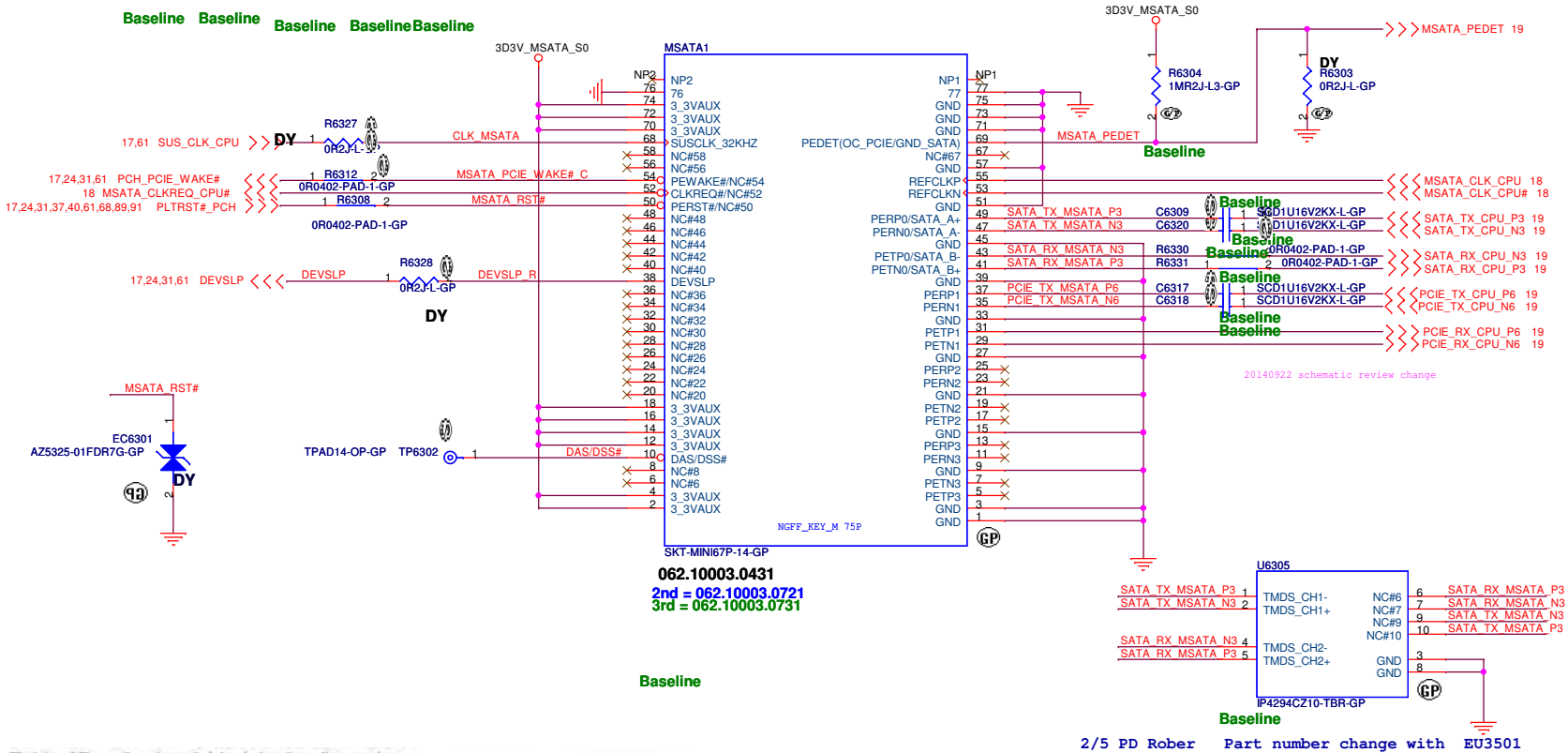
17.2.6 General Guidelines for mSATA (Gen 2 and Gen 3) Routing on SATA/PCIe muxed Ports

The below table summarizes the AC cap requirements on the motherboard when using the SATA/PCIe muxed ports.

Table 17-6. SATA/PCIe Gen 2 and Gen 3 Capacitor Values

Condition	PCIe Only	SATA Only	PCIe/SATA
PCH Tx	100 nF	10 nF	100 nF
PCH Rx	None	10 nF[2]	None[3]

Notes:
1. For PCIe only application, please refer to the PCIe guidelines for details.
2. For SATA only application, both PCH Tx and PCH Rx channels need to have 10 nF caps on the motherboard. This option supports all SATA devices. However, the PCH Rx 10 nF capacitor can be removed if DC coupled ODDs/devices are NOT used.
3. For PCIe/SATA muxed application, a 100 nF AC cap is required on motherboards for PCH Tx channel and NO AC cap is required on motherboard for the PCH Rx channel. This option DOES NOT support DC coupled ODDs/Devices.



Pin define from PCH and socket side.

	High (1)	Low (0)
PCH GPIO	SATA	PCIe
M.2 CONFIG_1	PCIe**	SATA

** Native: Internal Pull-Up (15k-40k) when function.

Table 27. Socket 2 Module Configuration

State #	Module Configuration Decodes CONFIG_0 (Pin 21)	CONFIG_1 (Pin 69)	CONFIG_2 (Pin 75)	CONFIG_3 (Pin 1)	Module Type and Main Host Interface[1]	Port Configuration[2]
0	GND	GND	GND	GND	SSD – SATA	N/A
1	GND	N/C	GND	GND	SSD – PCIe	N/A

Pin define from PCH and socket side.

	High (1)	Low (0)
PCH GPIO	SATA	PCIe
M.2 CONFIG_1	PCIe**	SATA

** Native: Internal Pull-Up (15k-40k) when function.

2/5 PD Rober Part number change with EU3501

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<Core Design>

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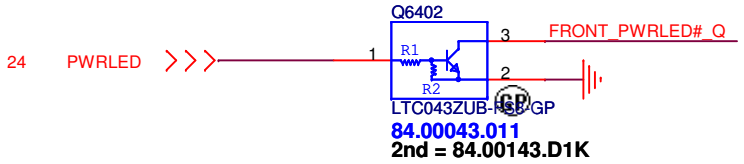
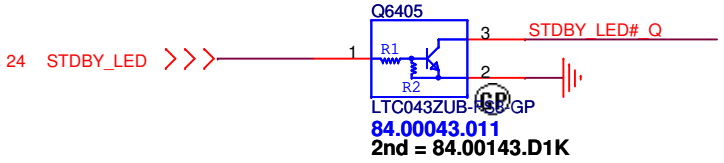
SSID = User.Interface

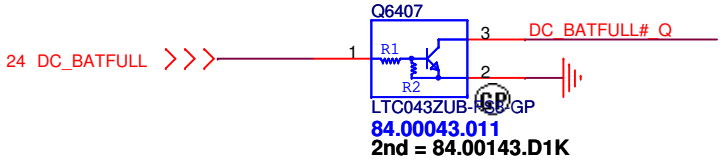
Power Button_LED



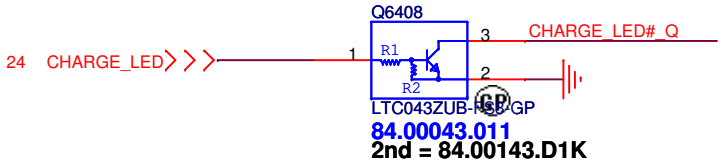
Power STDBY_LED

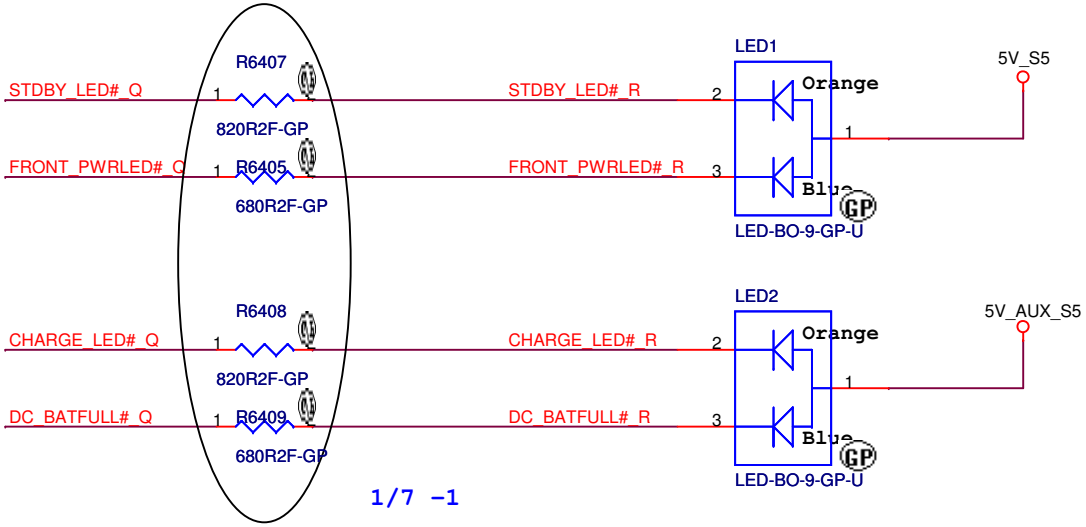


Battery LED2 (DC_BATFULL)

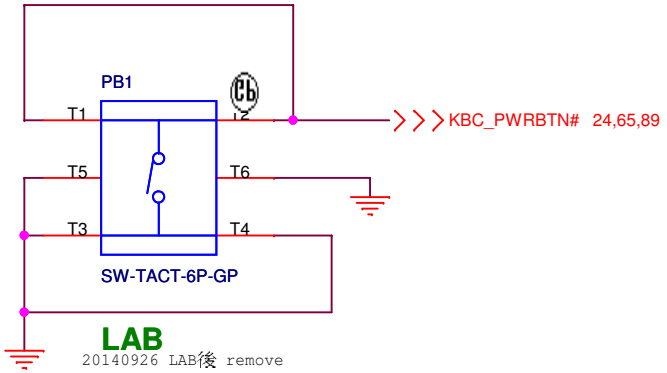


Battery LED1 (CHARGE)





Power Button



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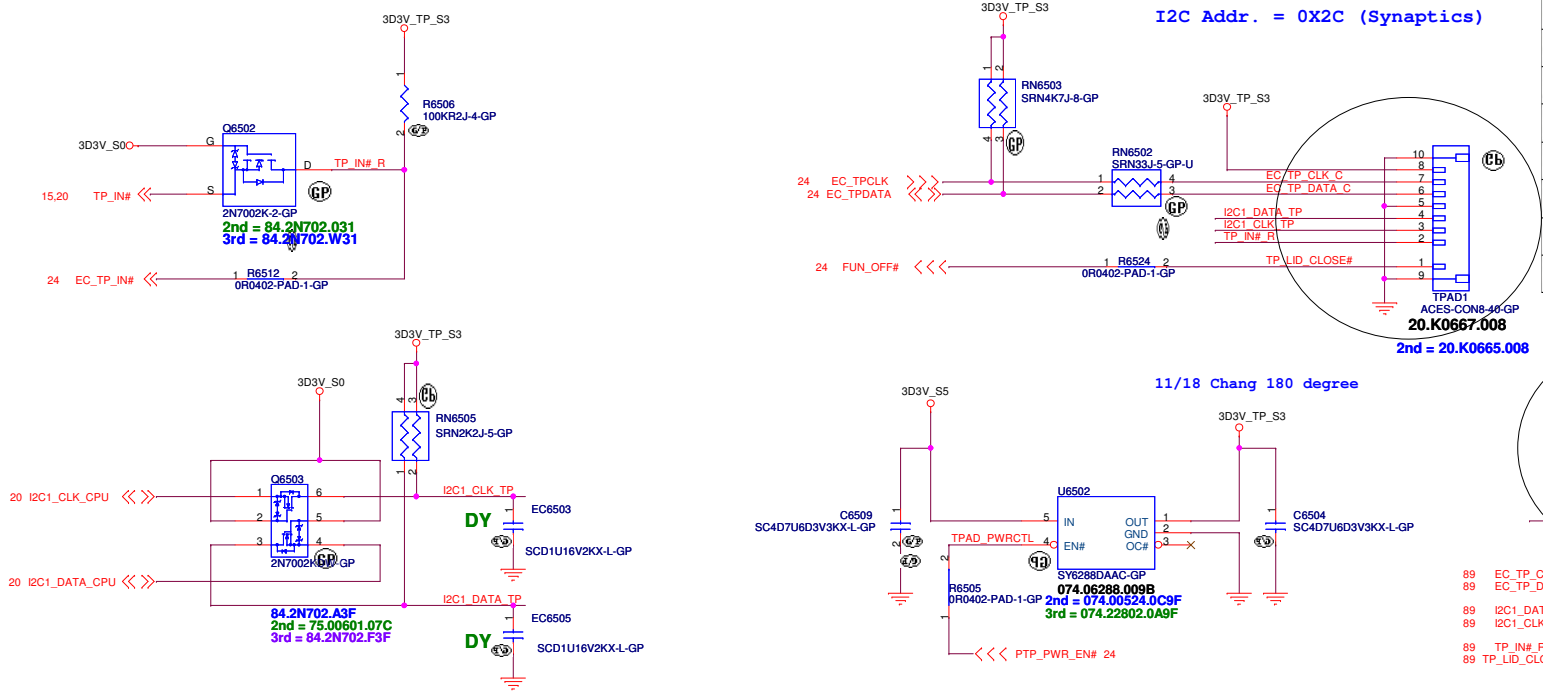
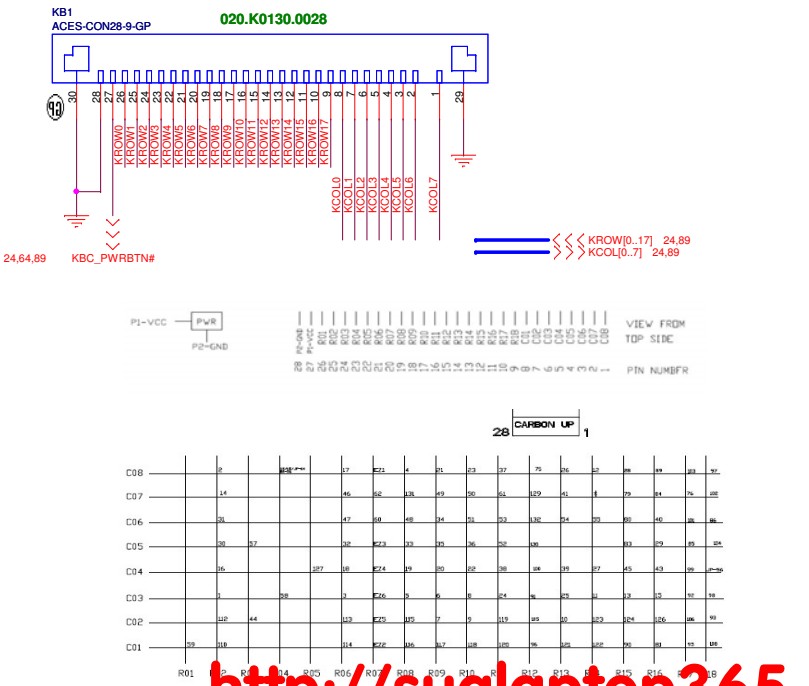
Precision Touch Pad

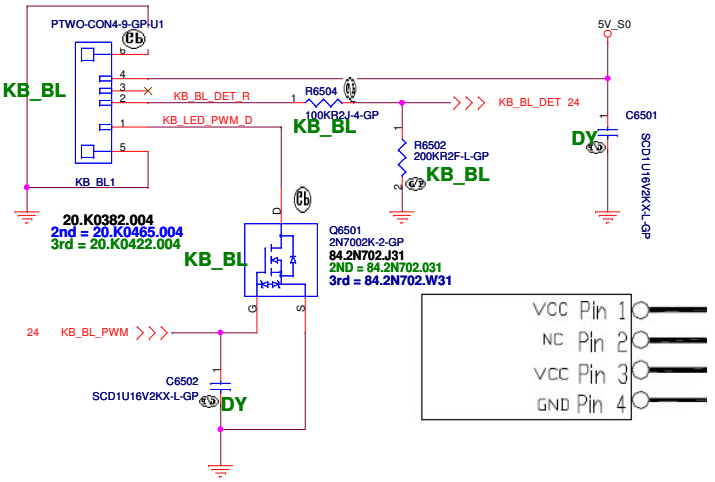
I2C Addr. = 0X2C (Synaptics)



Pin Number	Pin Name	Description
1	VDD	Power Supply Voltage
2	PS2_CLK	PS/2 Clock
3	PS2_DAT	PS/2 Data
4	GND	Ground
5	I2C_DATA	I²C Data
6	I2C_CLK	I²C Clock
7	ATTN	Attention
8	SENSOR OFF	Sensor Off

Internal KeyBoard Connector





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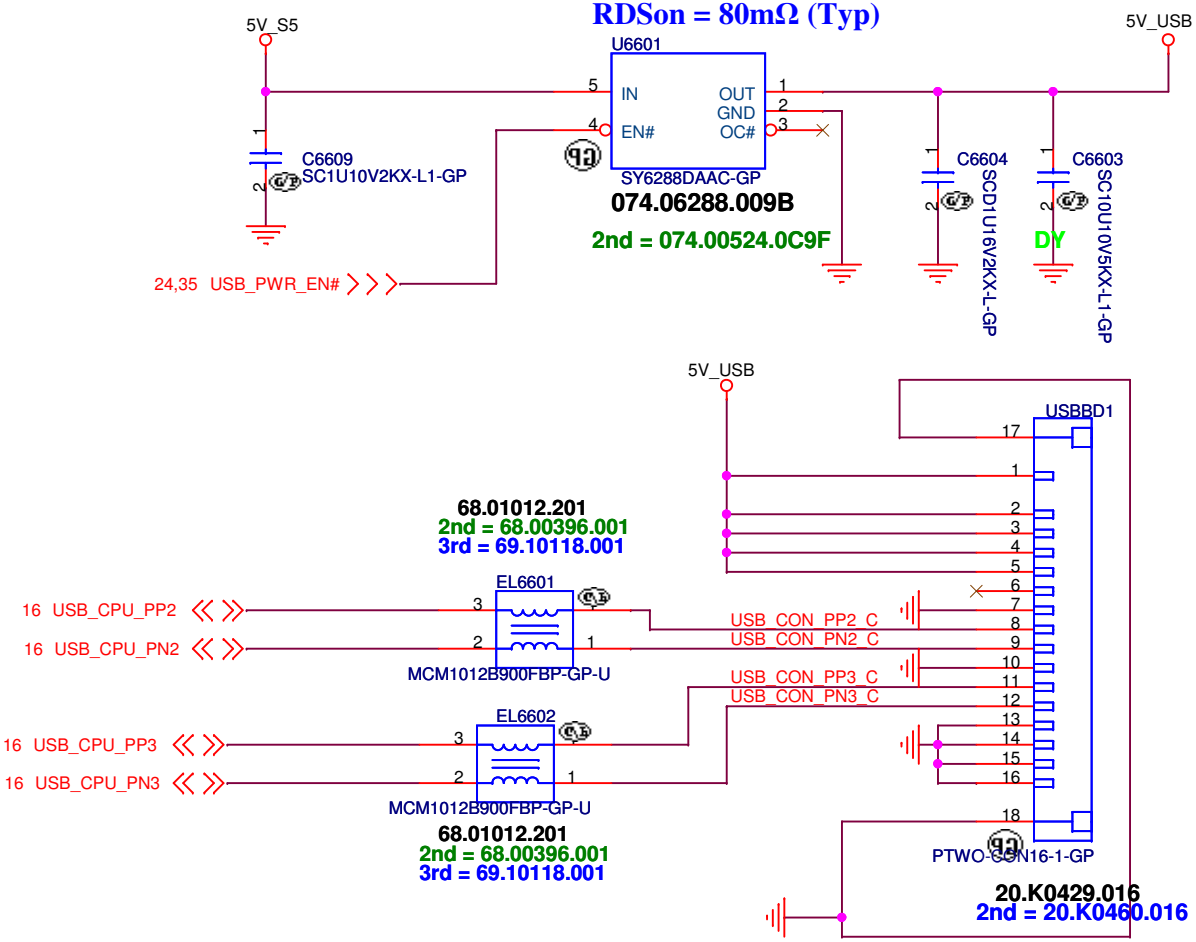

USB_CON_PN2_C >> USB_CON_PN2_C 89

USB_CON_PP2_C >> USB_CON_PP2_C 89

USB_CON_PN3_C >> USB_CON_PN3_C 89

USB_CON_PP3_C >> USB_CON_PP3_C 89

AFTP TEST POINT

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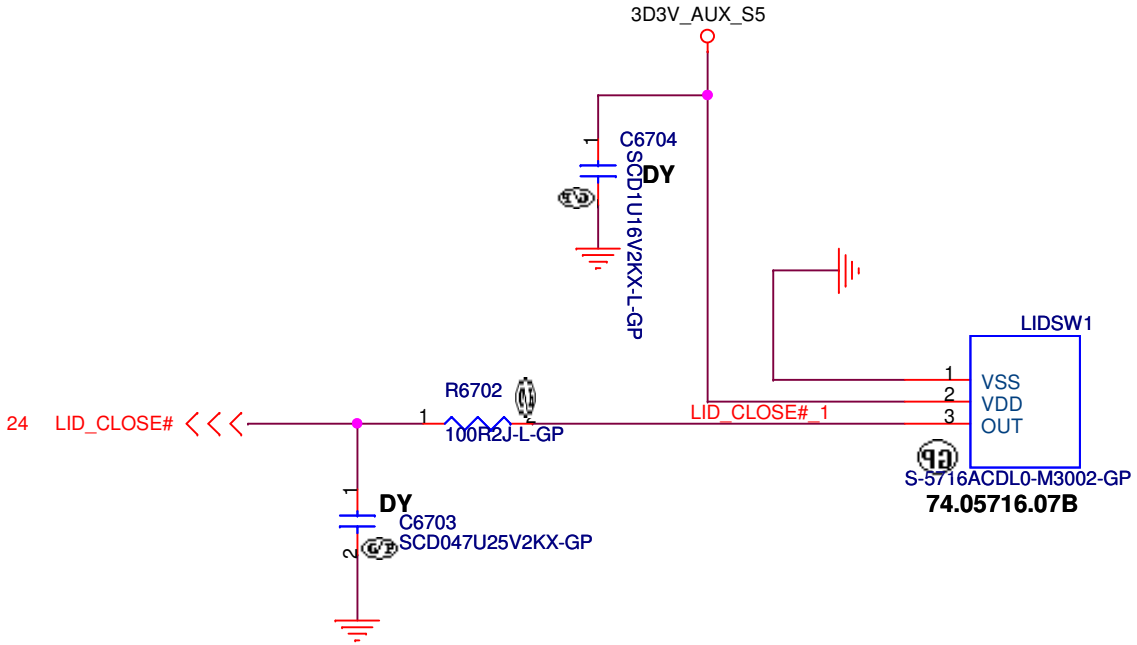

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Title

Hall Sensor

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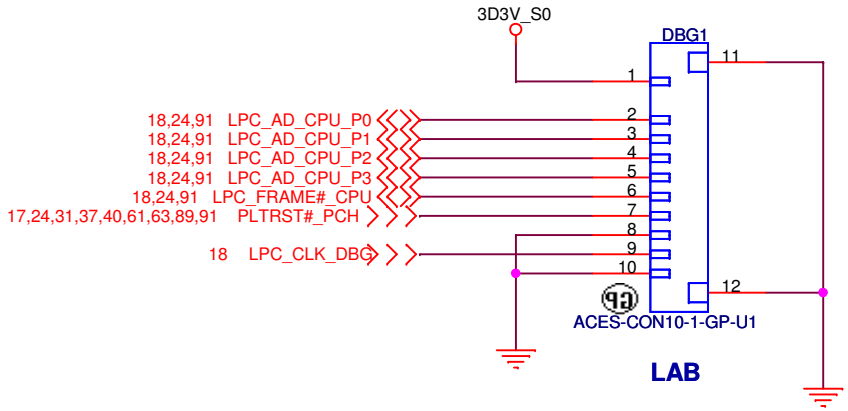

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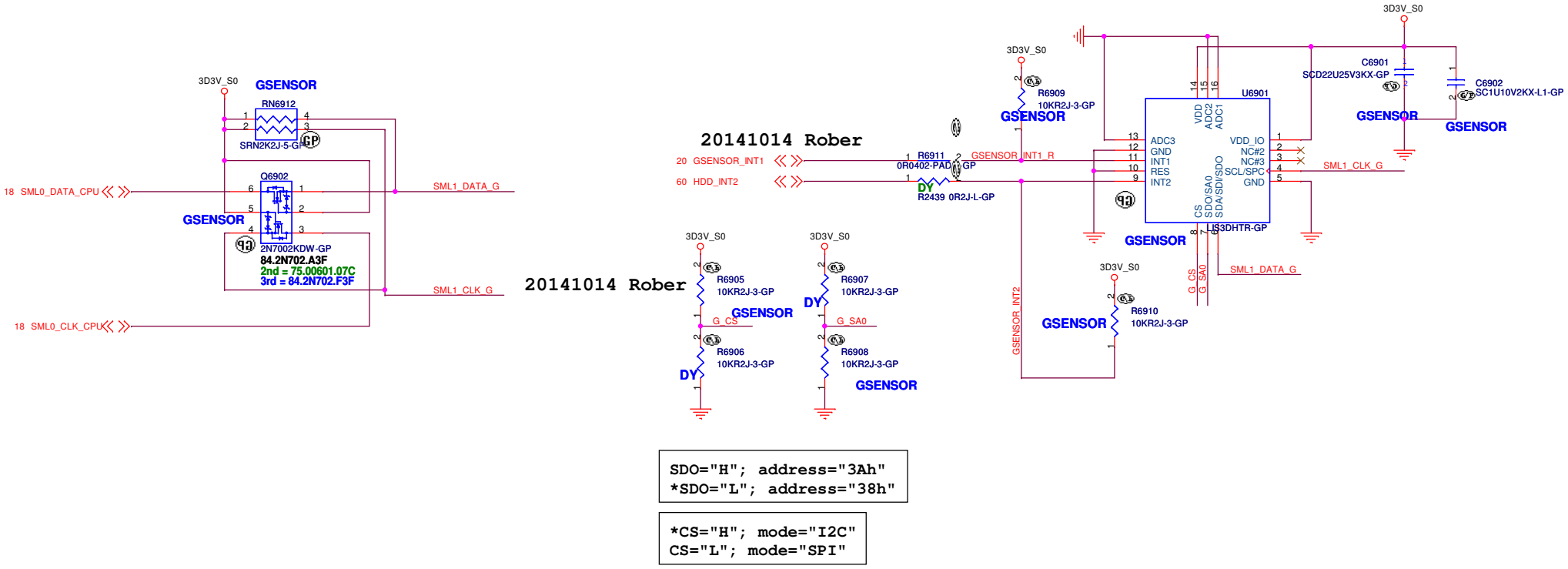
SSID = User.Interface

G Sensor

Note
- no via, trace, under the sensor (keep out area around 2mm)
- stay away from the screw hole or metal shield soldering joints
- design PCB pad based on our sensor LGA pad size (add 0.1mm)
- solder stencil opening to 90% of the PCB pad size
- mount the sensor near the center of mass of the NB as possible as you can



SDO="H"; address="3Ah"
*SDO="L"; address="38h"

*CS="H"; mode="I2C"
CS="L"; mode="SPI"

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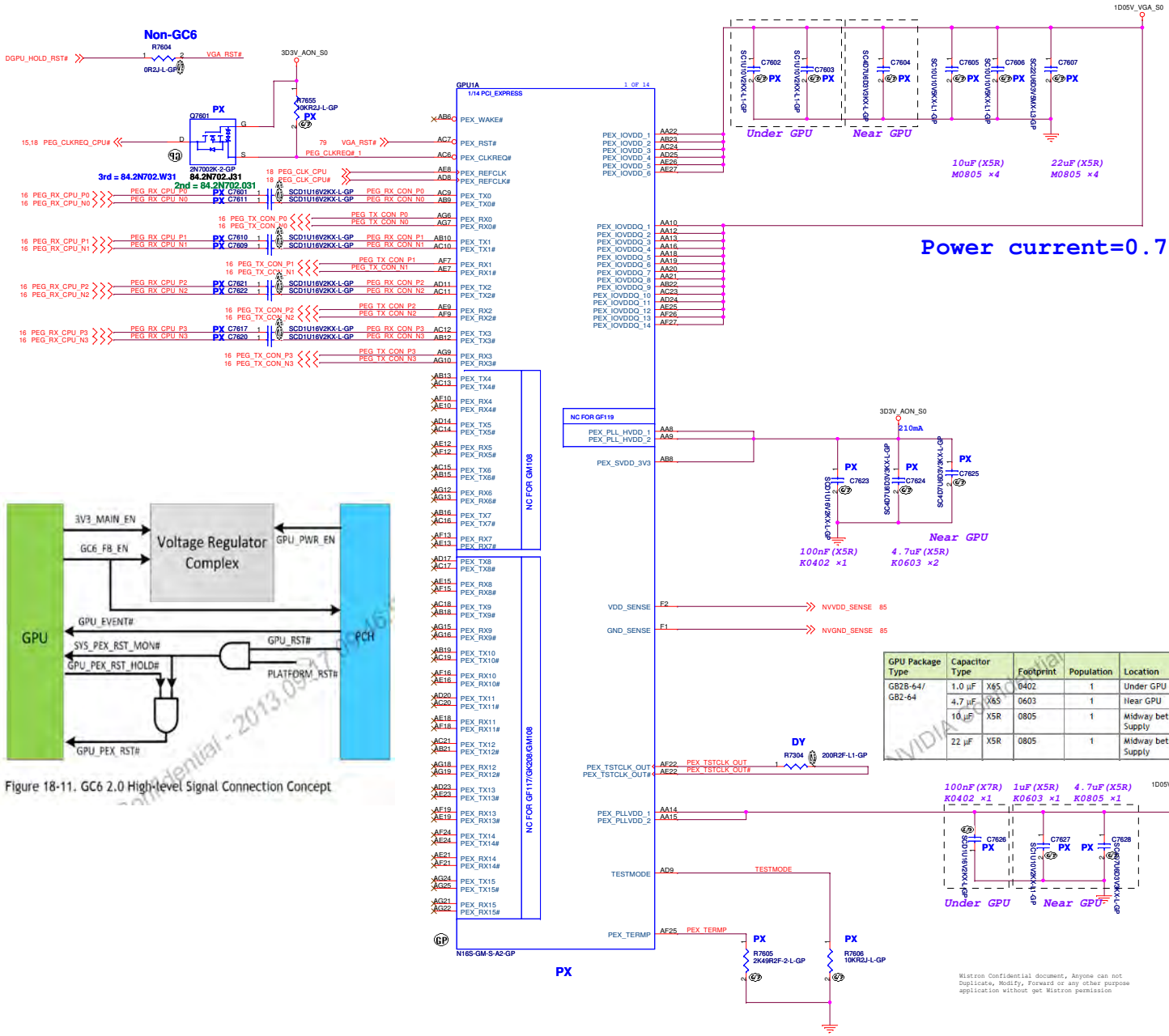

Figure 18-11. GC6 2.0 High-level Signal Connection Concept

3.4.2 PCI Express Power Decoupling and Filtering

Table 3-16. PEX_IOVDD/Q Power Rail Combined

GPU Package Type	Capacitor Type		Footprint	Population	Location
GB2B-64/ GB2-64	1.0 µF	X6S	0402	1	Under GPU
	4.7 µF	X6S	0603	1	Near GPU
	10 µF	X5R	0805	1	Midway between GPU and Power Supply
	22 µF	X5R	0805	1	Midway between GPU and Power Supply
GB4B-128 GB3B-256	1.0 µF	X6S	0402	4	Under GPU
	4.7 µF	X6S	0603	2	Near GPU
	10 µF	X5R	0805	4	Midway between GPU and Power Supply
	22 µF	X5R	0805	4	Midway between GPU and Power Supply

GPU Package Type	Capacitor Type		Footprint	Population	Location
GB2B-64/ GB2-64	1.0 µF	X6S	0402	1	Under GPU
	4.7 µF	X6S	0603	1	Near GPU
	10 µF	X5R	0805	1	Midway between GPU and Power Supply
	22 µF	X5R	0805	1	Midway between GPU and Power Supply

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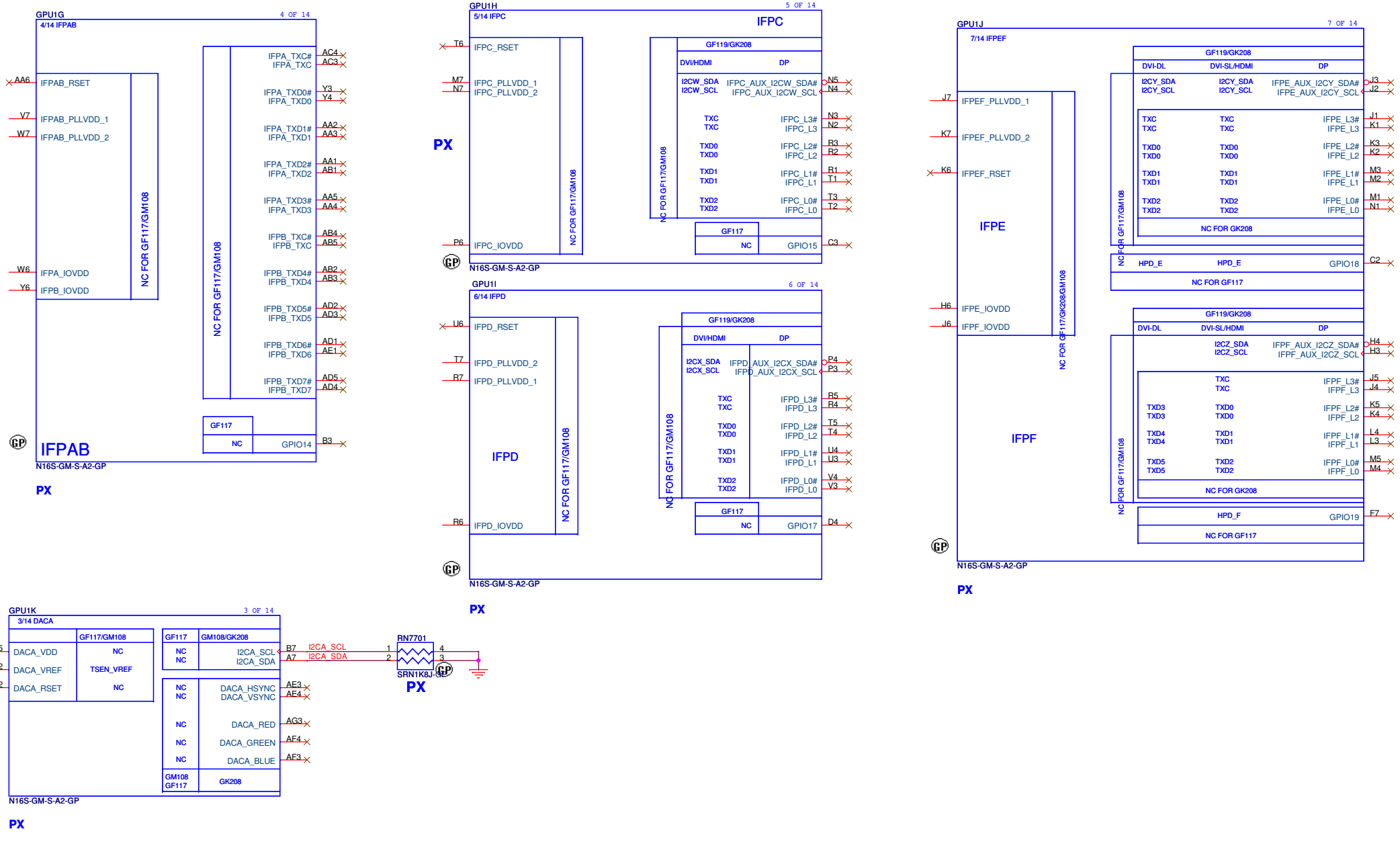

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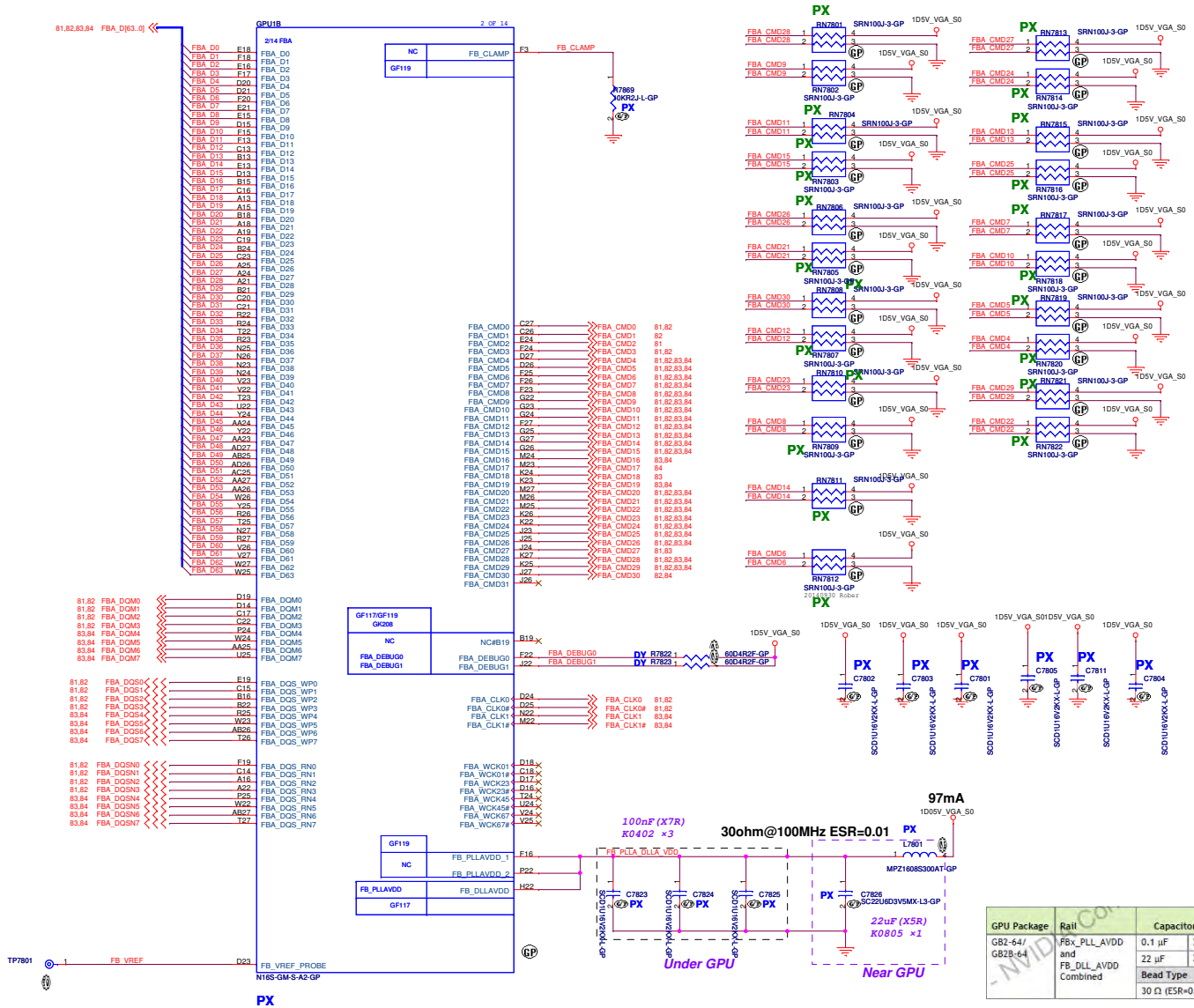


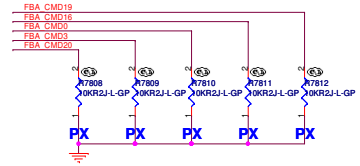
Table 6-4. Mode E Command Mapping

N16x DDR3 Mode E	Rank 0		Rank 1	
	Data Bits [31:0]	Data Bits [63:32]	Data Bits [31:0]	Data Bits [63:32]
FBx_CMD0	ODT		ODT	
FBx_CMD1			CS1*	
FBx_CMD2	CS0*			
FBx_CMD3	CKE		CKE	
FBx_CMD4	A9	A9	A11	A11
FBx_CMD5	A6	A6	A7	A7
FBx_CMD6	A3	A3	BA1	BA1
FBx_CMD7	A0	A0	A12	A12
FBx_CMD8	A8	A8	A8	A8
FBx_CMD9	A12	A12	A0	A0
FBx_CMD10	A1	A1	A2	A2
FBx_CMD11	RAS*	RAS*	RAS*	RAS*
FBx_CMD12	A13	A13	A14	A14
FBx_CMD13	BA1	BA1	A3	A3
FBx_CMD14	A14	A14	A13	A13
FBx_CMD15	CAS*	CAS*	CAS*	CAS*
FBx_CMD16		ODT		ODT
FBx_CMD17				CS1*
FBx_CMD18		CS0*		
FBx_CMD19		CKE		CKE
FBx_CMD20	RST	RST	RST	RST
FBx_CMD21	A7	A7	A6	A6
FBx_CMD22	A4	A4	A5	A5
FBx_CMD23	A11	A11	A9	A9
FBx_CMD24	A2	A2	A1	A1
FBx_CMD25	A10	A10	WE*	WE*
FBx_CMD26	A5	A5	A4	A4
FBx_CMD27	BA2	BA2		
FBx_CMD28	WE*	WE*	A10	A10
FBx_CMD29	BA0	BA0	BA0	BA0
FBx_CMD30		BA2	BA2	
FBx_CMD31				
FBx_CMD32				
FBx_CMD33[1]				
FBx_CMD34	DBG0[2]			
FBx_CMD35	DBG1[2]			

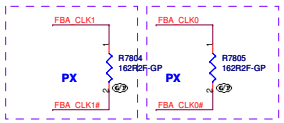
Notes:
1. Not available in GB2-64 and GB2B-64 packages.
2. GPU debug pins; not connected to DRAM. See section 6.1.11.

GPU Package	Rail	Capacitor Type		Footprint	Population	Location
GB2-64/ GB2B-64	FBx_PLL_AVDD and FB_DLL_AVDD Combined	0.1 µF	X7R	0402	2	Under GPU
		22 µF	X5R	0805	1	Near GPU
		Bead Type				
		30 Ω (ESR=0.010 Ω)		0603	1	Near GPU

Memory ODTx, CKEx and RST Termination



FBCLK Termination placed near each VRAM at board edge side



CHECK N16 Design guide P.98 Table 6-7

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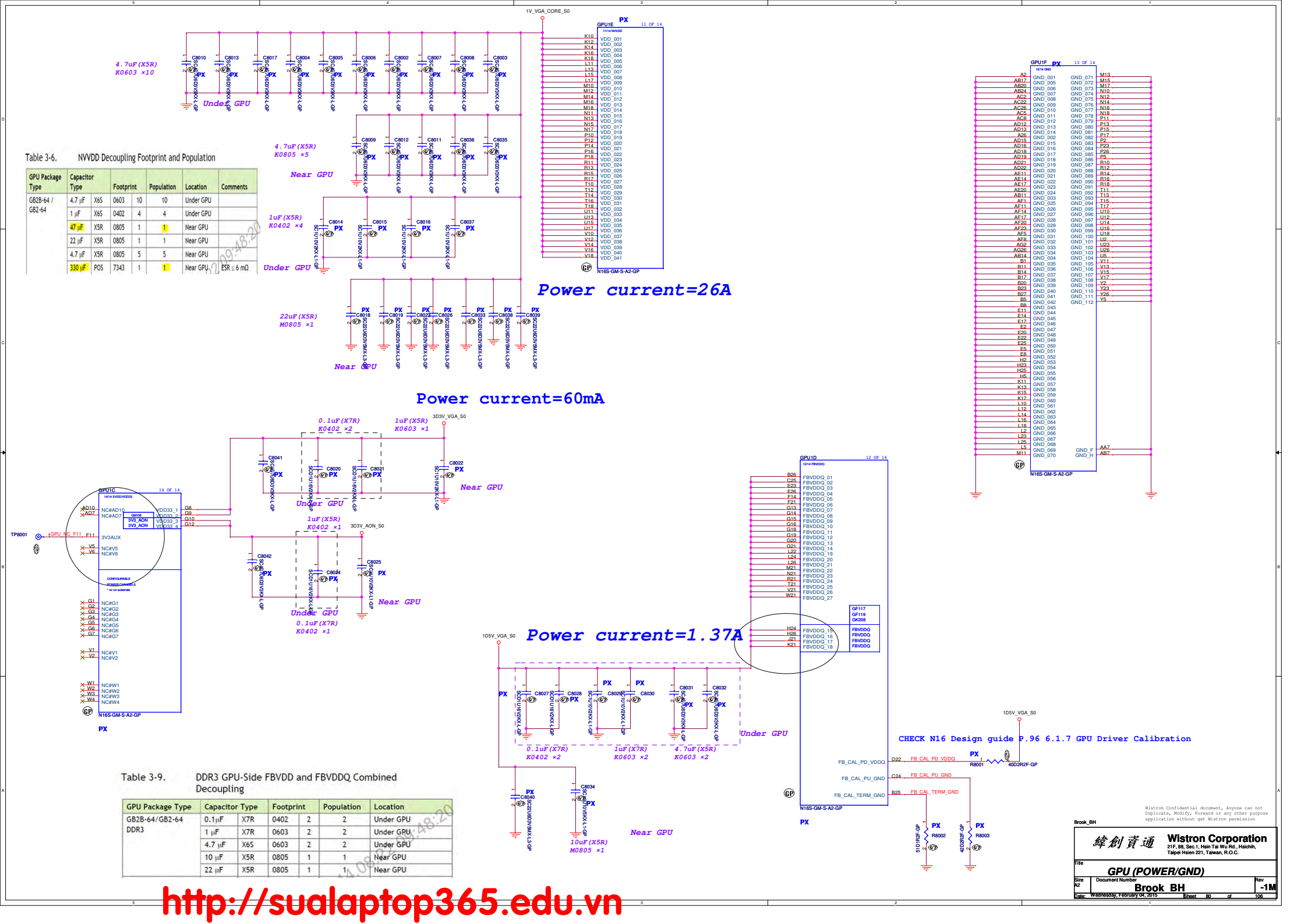

Table 3-6. NVVDD Decoupling Footprint and Population

GPU Package Type	Capacitor Type		Footprint		Population	Location	Comments
GB2B-64 / GB2-64	4.7 µF	X6S	0603	10	10	Under GPU	
	1 µF	X6S	0402	4	4	Under GPU	
	47 µF	X5R	0805	1	1	Near GPU	
	22 µF	X5R	0805	1	1	Near GPU	
	4.7 µF	X5R	0805	5	5	Near GPU	
	330 µF	POS	7343	1	1	Near GPU	ESR ≤ 6 mΩ

Table 3-9. DDR3 GPU-Side FBVDD and FBVDDQ Combined Decoupling

GPU Package Type	Capacitor Type		Footprint		Population	Location
GB2B-64/GB2-64 DDR3	0.1µF	X7R	0402	2	2	Under GPU
	1 µF	X7R	0603	2	2	Under GPU
	4.7 µF	X6S	0603	2	2	Under GPU
	10 µF	X5R	0805	1	1	Near GPU
	22 µF	X5R	0805	1	1	Near GPU

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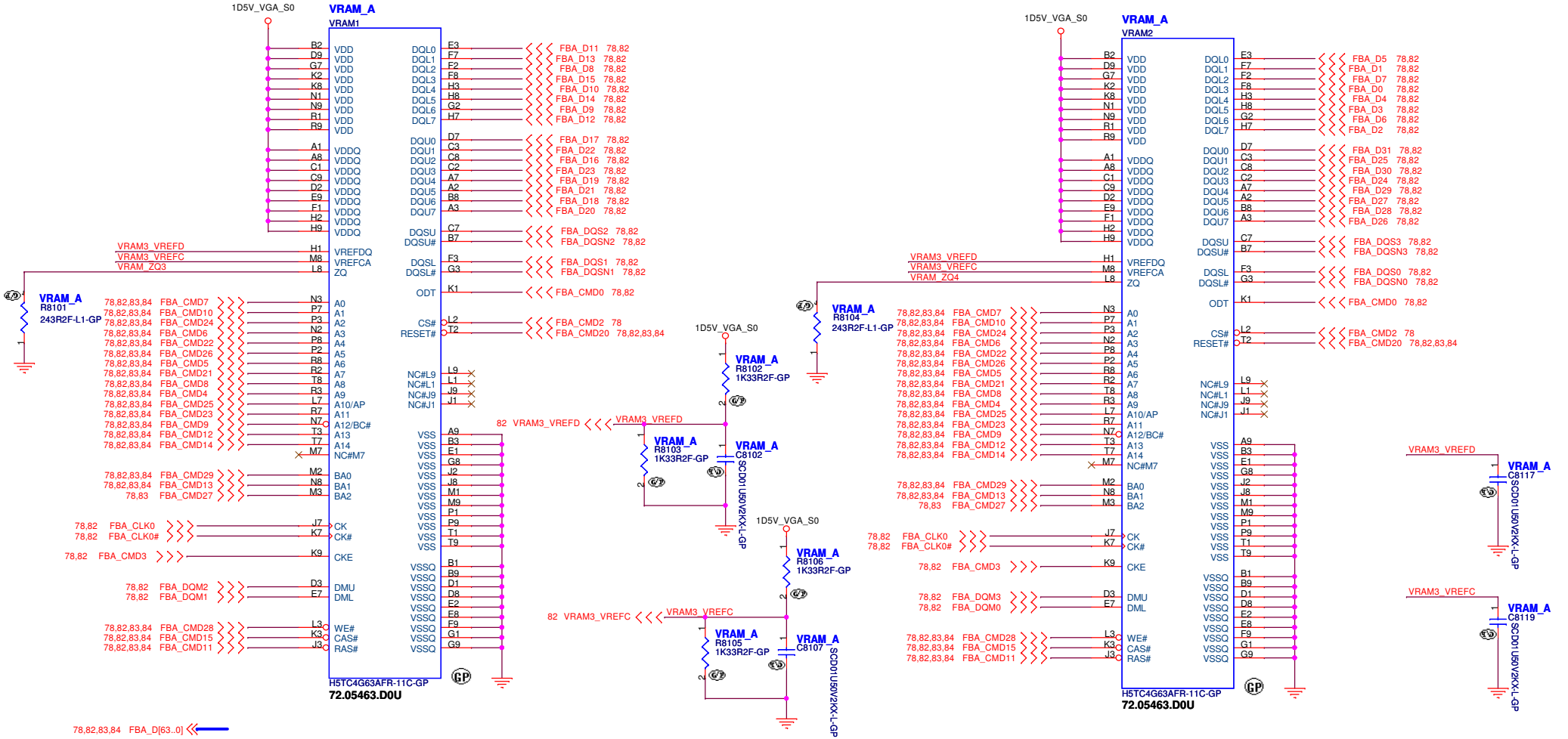


FOR VRAM1

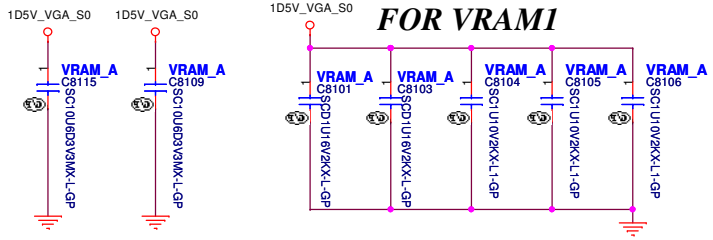
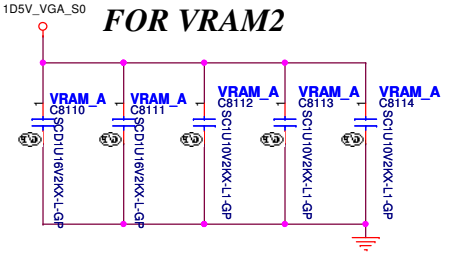


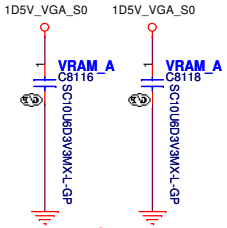
Table 3-11. DDR3 per Memory FBVDD/Q Decoupling

Capacitor Type			Population FBVDDQ	Population FBVDD	Location
FBVDD/Q Combinod					
0.1 µF	X7R	0402	2		Under DRAM
1.0 µF	X7R	0603	4		Under DRAM
10 µF	X5R	0805	0		Close to DRAM
FBVDD/Q Separate					
0.1 µF	X7R	0402	4	2	Under DRAM
1.0 µF	X7R	0603	3	1	Under DRAM
10 µF	X5R	0805	0	0	Close to DRAM

Note: *Location is close to DRAM for clamshell mode.

FOR VRAM2





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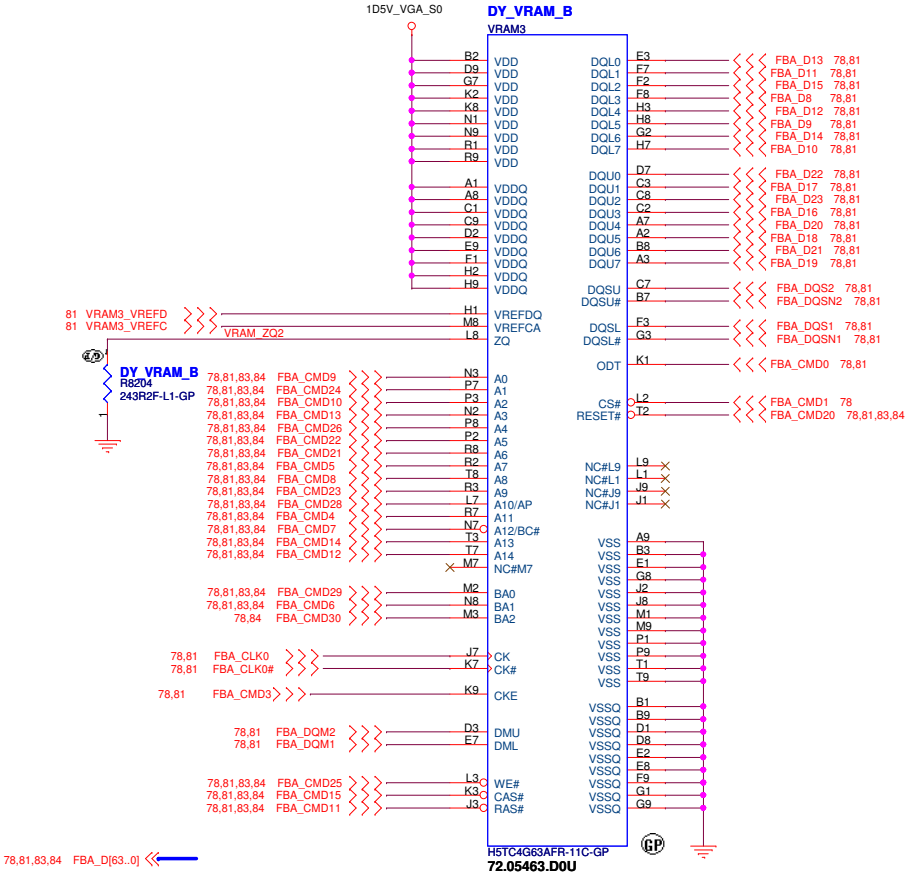

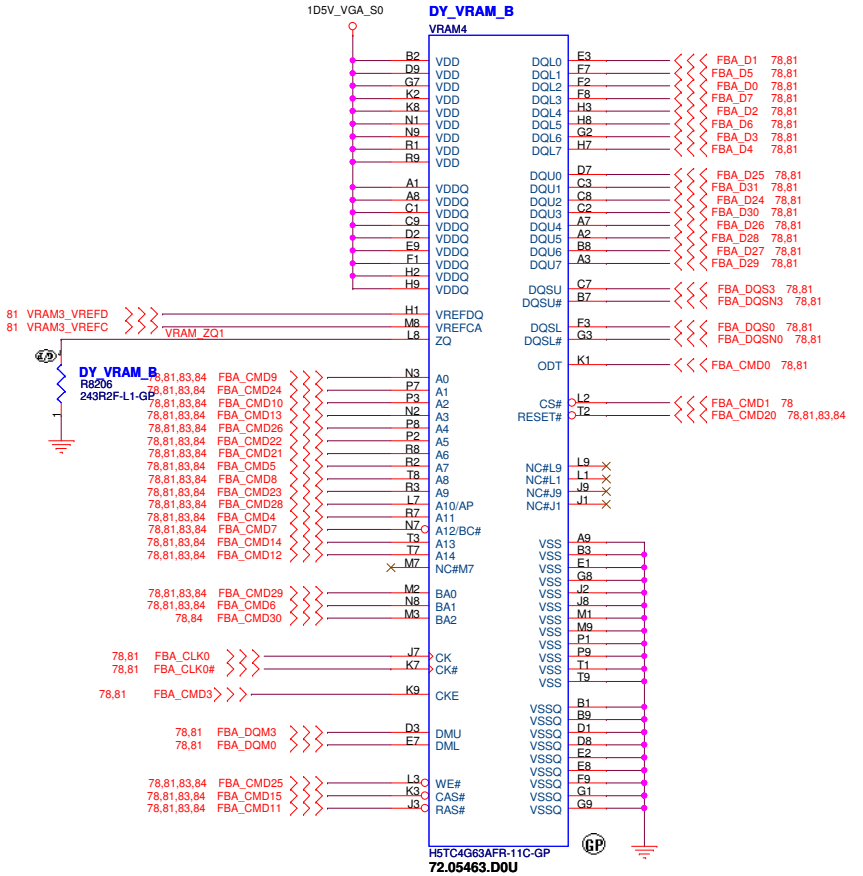

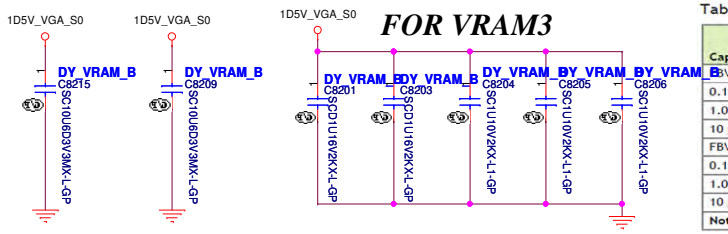

Table 3-11. DDR3 per Memory FBVDD/Q Decoupling

Capacitor Type			Population		Location
			FBVDDQ	FBVDD	
FBVDD/Q Combined					
0.1 µF	X7R	0402	2		Under DRAM
1.0 µF	X7R	0603	4		Under DRAM
10 µF	X5R	0805	0		Close to DRAM
FBVDD/Q Separate					
0.1 µF	X7R	0402	4	2	Under DRAM
1.0 µF	X7R	0603	3	1	Under DRAM
10 µF	X5R	0805	0	0	Close to DRAM

Note: *Location is close to DRAM for clamshell mode.

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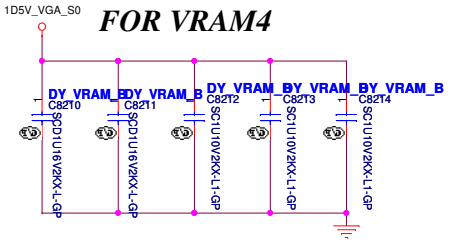

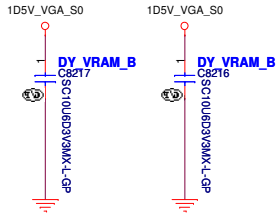

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Title: GPU-VRAM3,4 (2/4)

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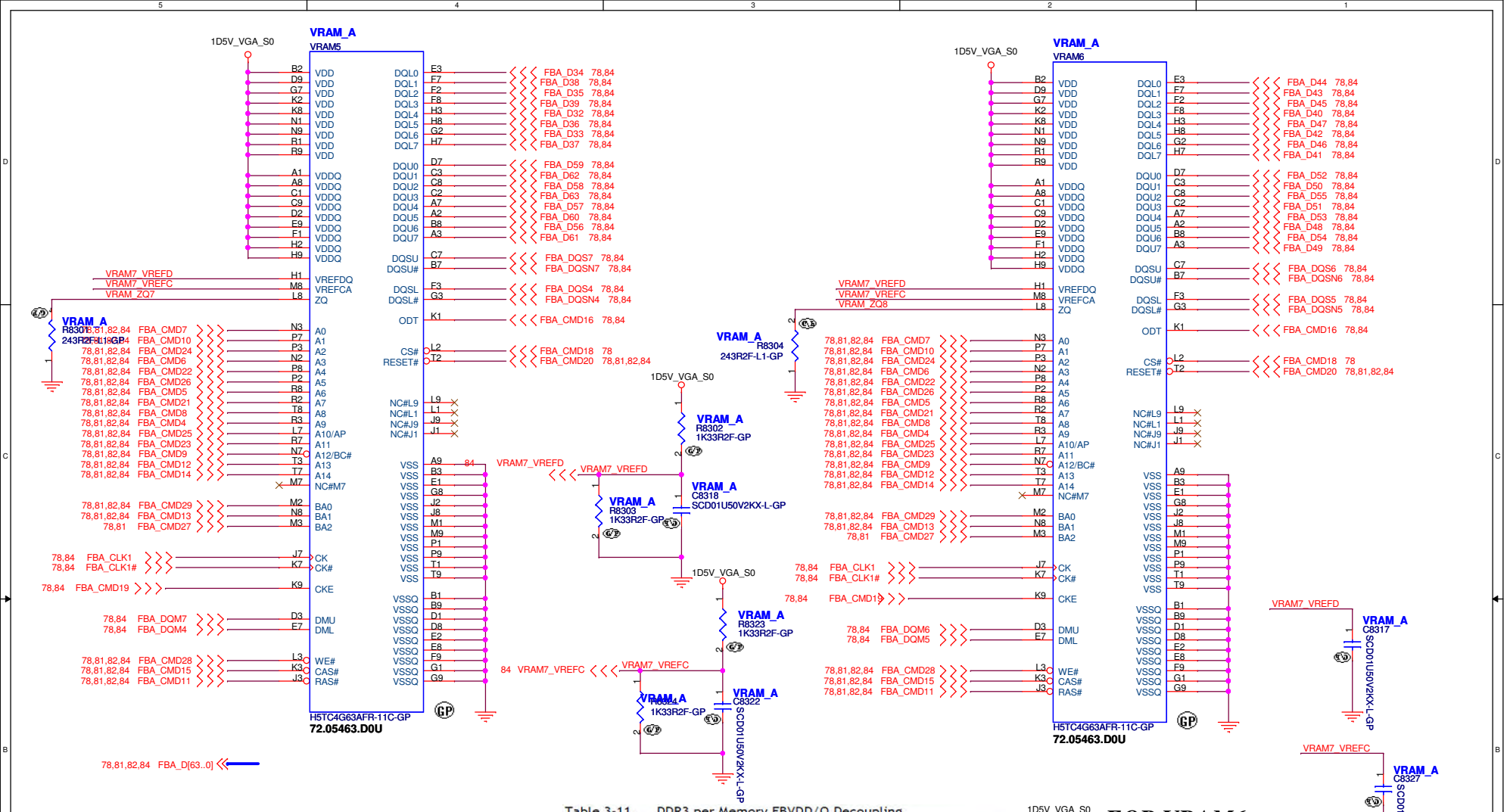

Table 3-11. DDR3 per Memory FBVDD/Q Decoupling

Capacitor Type			Population FBVDDQ	Population FBVDD	Location
FBVDD/Q Combined					
0.1 µF	X7R	0402	2		Under DRAM
1.0 µF	X7R	0603	4		Under DRAM
10 µF	X5R	0805	0		Close to DRAM
FBVDD/Q Separate					
0.1 µF	X7R	0402	4	2	Under DRAM
1.0 µF	X7R	0603	3	1	Under DRAM
10 µF	X5R	0805	0	0	Close to DRAM

Note: *Location is close to DRAM for clamshell mode.

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Title: GPU-VRAM7,8 (4/4)

Size	Document Number	Rev
Custom	Brook_BH	-1M

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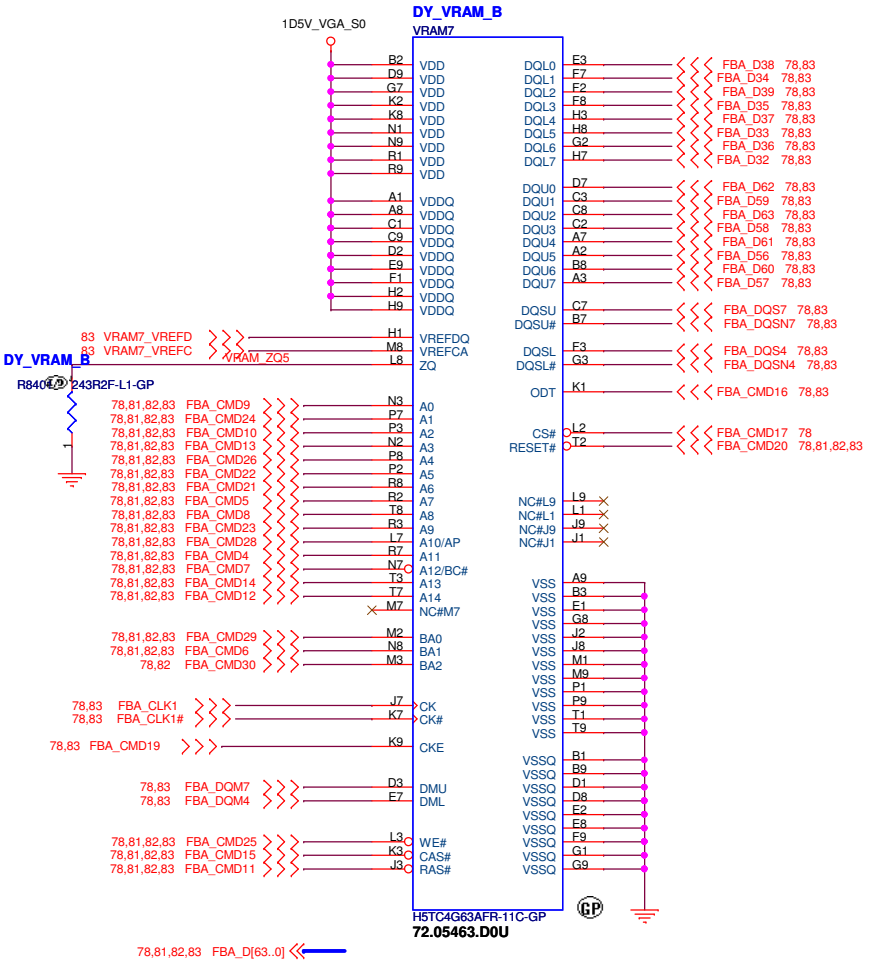

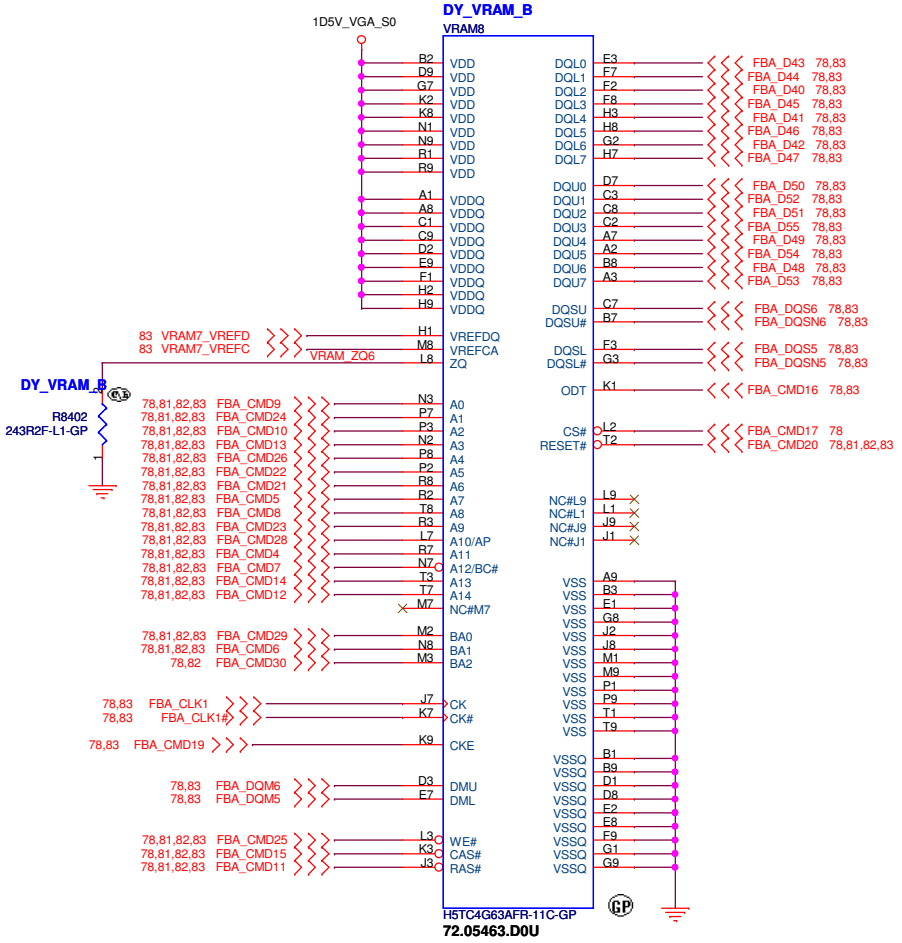

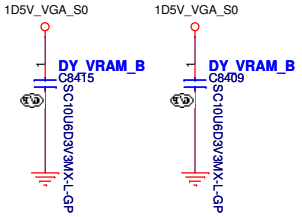

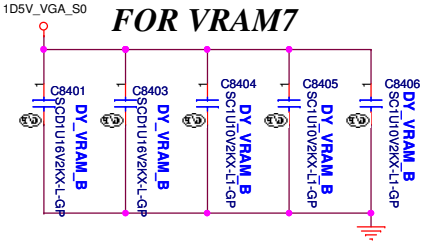

Table 3-11. DDR3 per Memory FBVDD/Q Decoupling

Capacitor Type			Population FBVDDQ	Population FBVDD	Location
FBVDD/Q Combined					
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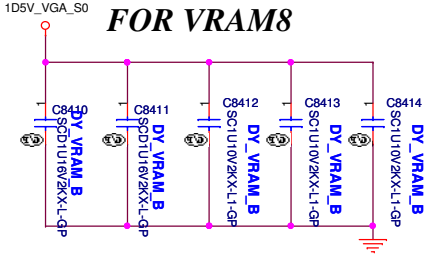
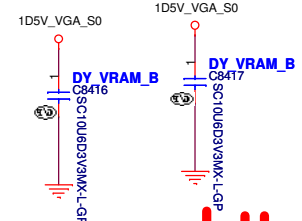
1.0 µF	X7R	0603	4		Under DRAM
10 µF	X5R	0805	0		Close to DRAM
FBVDD/Q Separato					
0.1 µF	X7R	0402	4	2	Under DRAM
1.0 µF	X7R	0603	3	1	Under DRAM
10 µF	X5R	0805	0	0	Close to DRAM

Note: *Location is close to DRAM for clamshell mode.





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Title: GPU-VRAM7,8 (4/4)

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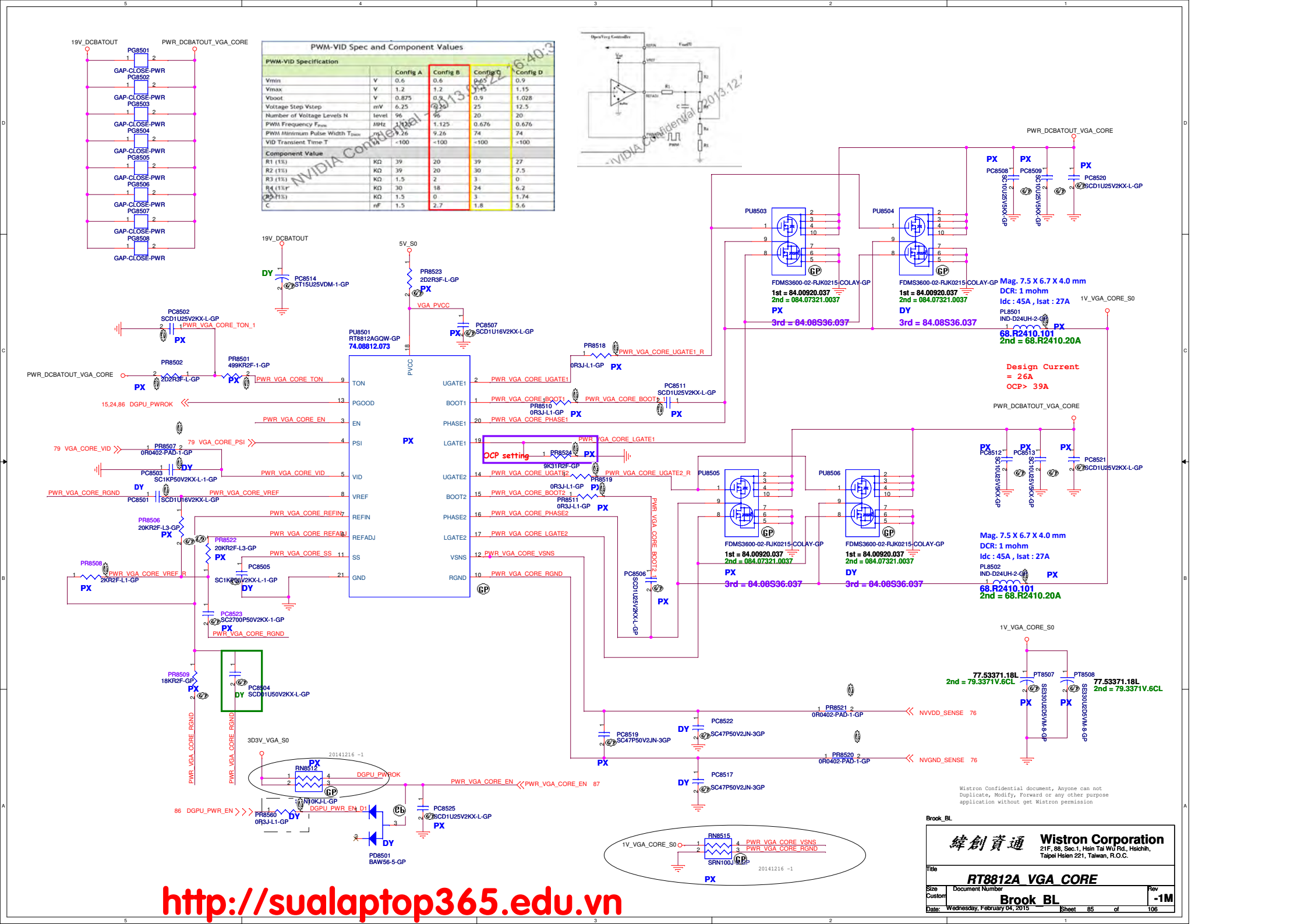
PWM-VID Spec and Component Values
PWM-VID Specification
Config A
Config B
Config C
Config D
Vmin
Vmax
Vboot
Voltage Step Vstep
Number of Voltage Levels N
PWM Frequency F
PWM Minimum Pulse Width T
VID Transient Time T
Component Value
R1 (1%)
R2 (1%)
R3 (1%)
R4 (1%)
R5 (1%)
C
NVIDIA Confidential
19V_DCBATOUT
PWR_DCBATOUT_VGA_CORE
PU8501
RT8812AGQW-GP
74.08812.073
PU8503
PU8504
PU8505
PU8506
FDMS3600-02-RJK0215-COLAY-GP
1st = 84.00920.037
2nd = 084.07321.0037
3rd = 84.08S36.037
Mag. 7.5 X 6.7 X 4.0 mm
DCR: 1 mohm
Idc : 45A , Isat : 27A
PL8501
PL8502
IND-D24UH-2-GP
68.R2410.101
2nd = 68.R2410.20A
Design Current
= 26A
OCP> 39A
OCP setting
1V_VGA_CORE_S0
3D3V_VGA_S0
5V_S0
NVVDD_SENSE
NVGND_SENSE
77.53371.18L
2nd = 79.3371V.6CL
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RT8812A_VGA_CORE
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-1M
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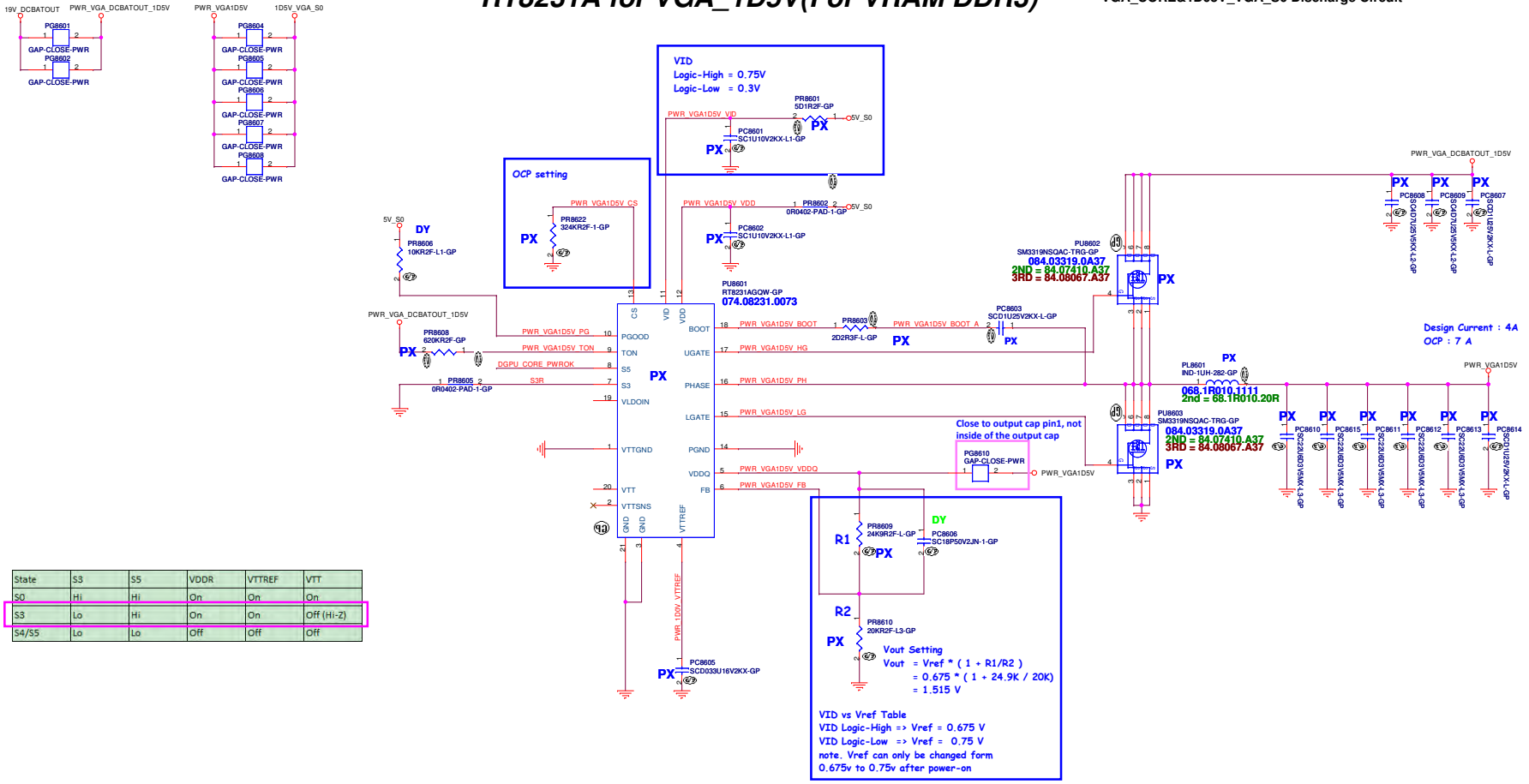
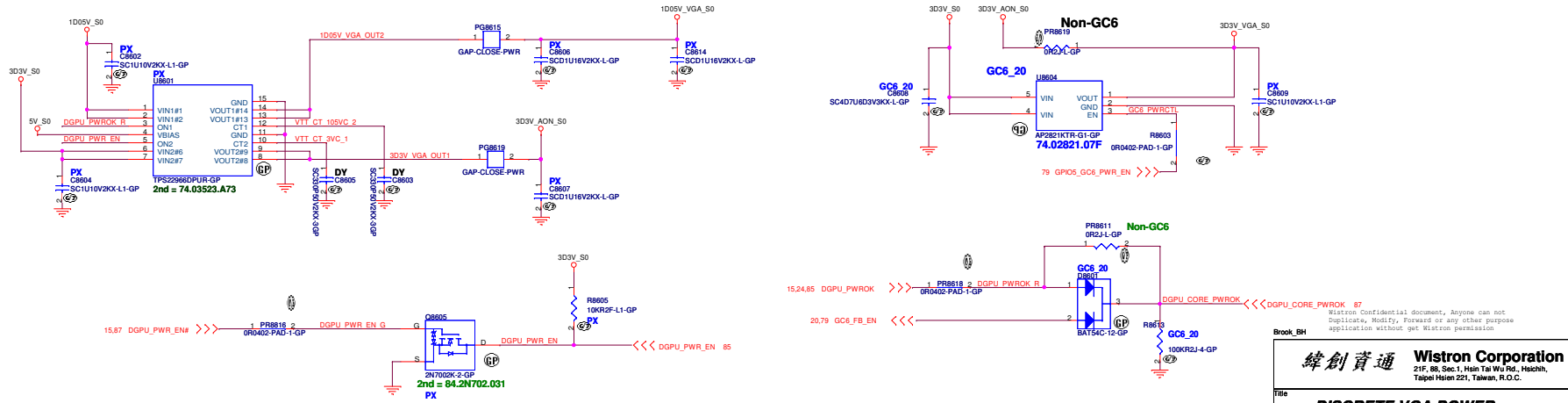
RT8231A for VGA_1D5V(For VRAM DDR3)

VGA_CORE&1D05V_VGA_S0 Discharge Circuit



State	S3	S5	VDDR	VTTREF	VTT
S0	Hi	Hi	On	On	On
S3	Lo	Hi	On	On	Off (Hi-Z)
S4/S5	Lo	Lo	Off	Off	Off

3D3V_S0 to 3D3V_VGA_S0
1D05V_S0 to 1D05V_VGA_S0



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Title: DISCRETE VGA POWER

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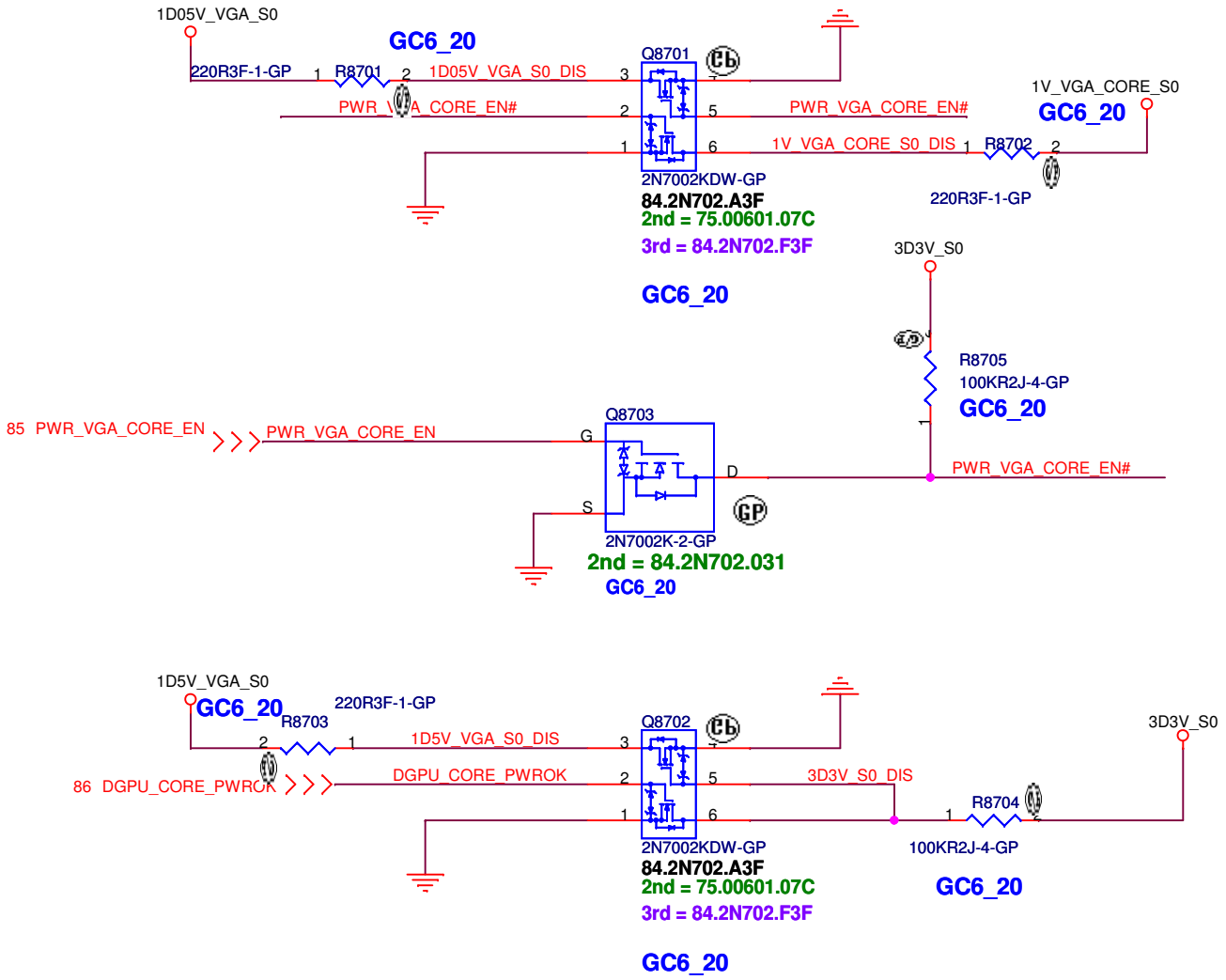

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Title: **DISCHARGE**

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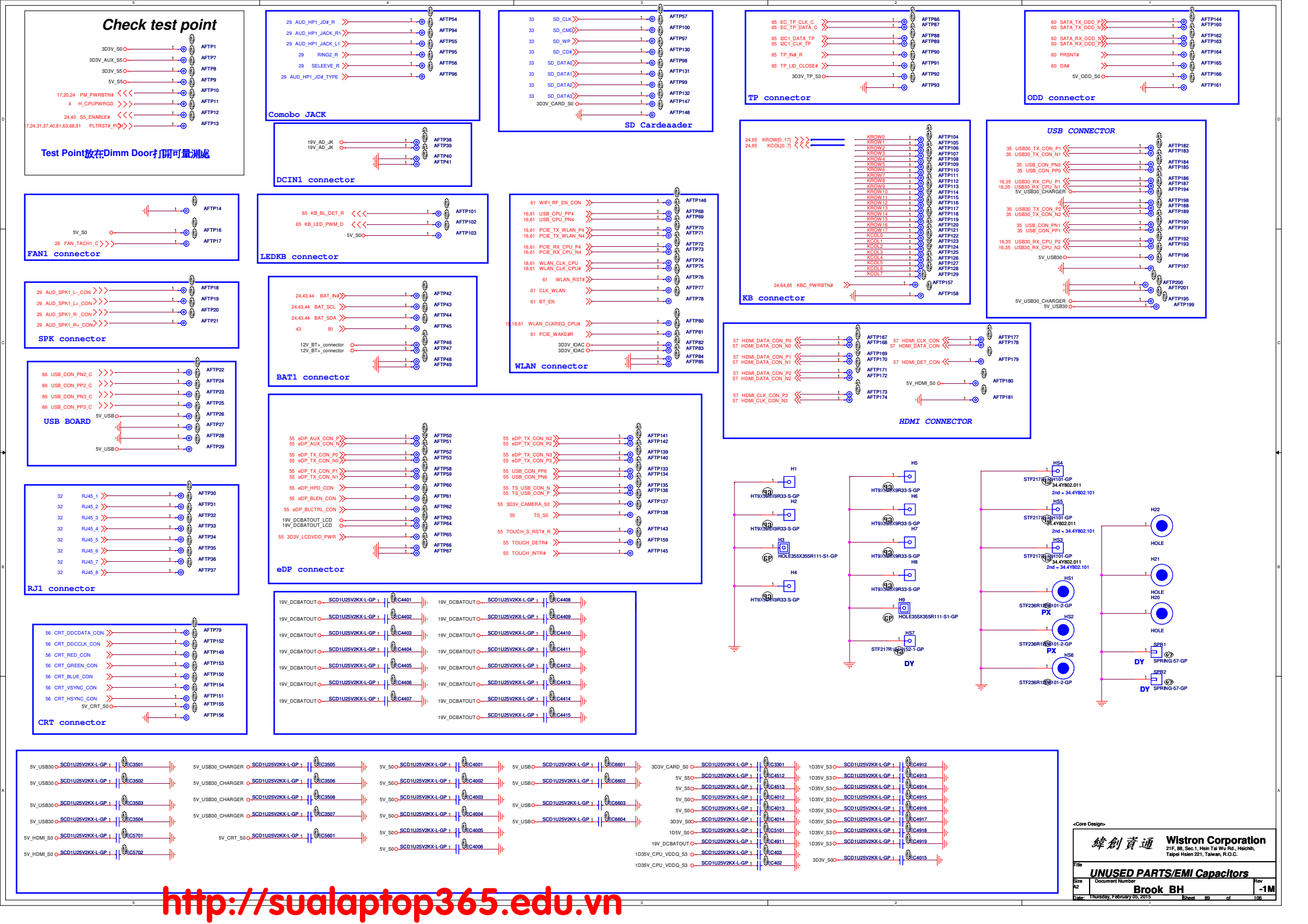
Check test point
Test Point放在Dimm Door打開可量測處
Comobo JACK
DCIN1 connector
SD Cardeaader
TP connector
ODD connector
FAN1 connector
LEDKB connector
KB connector
USB CONNECTOR
SPK connector
BAT1 connector
WLAN connector
USB BOARD
HDMI CONNECTOR
eDP connector
RJ1 connector
CRT connector
UNUSED PARTS/EMI Capacitors
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-1M
Thursday, February 05, 2015
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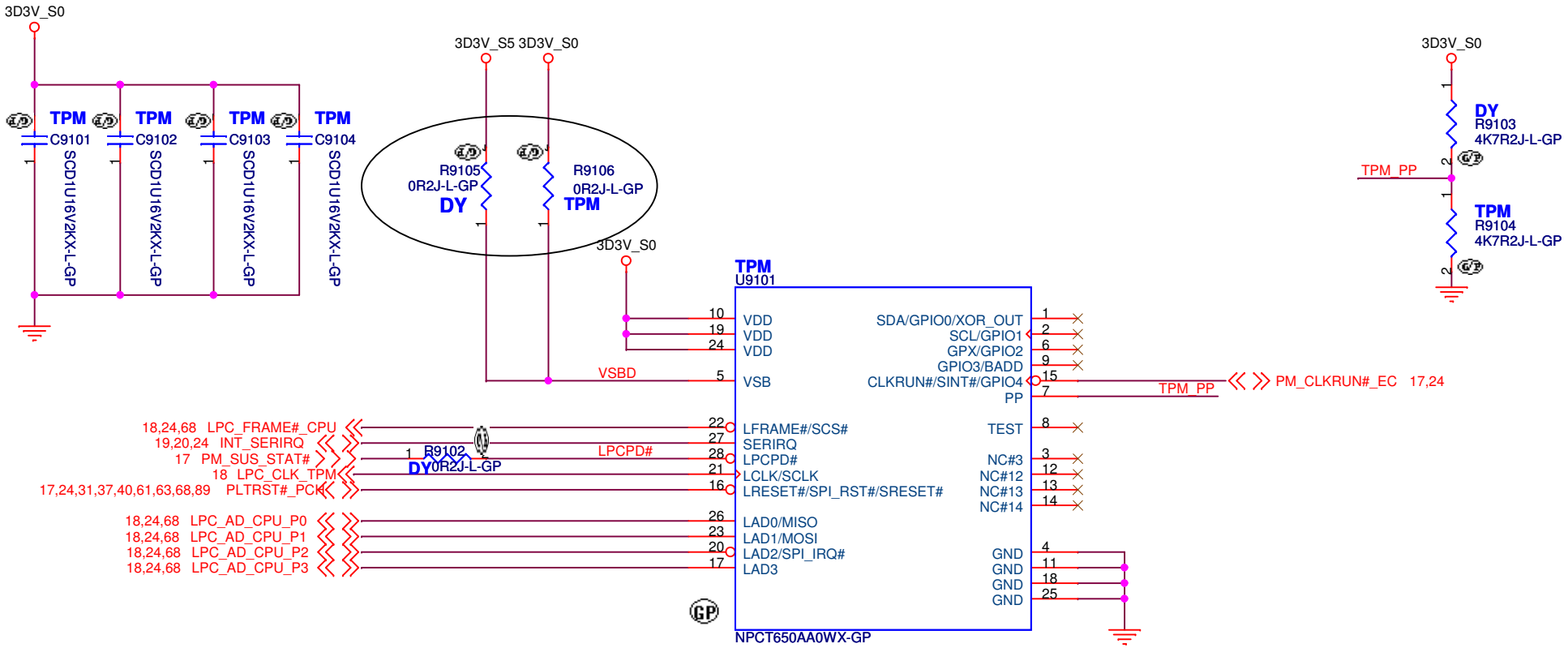

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Title: ***TPM (NPCT650)***

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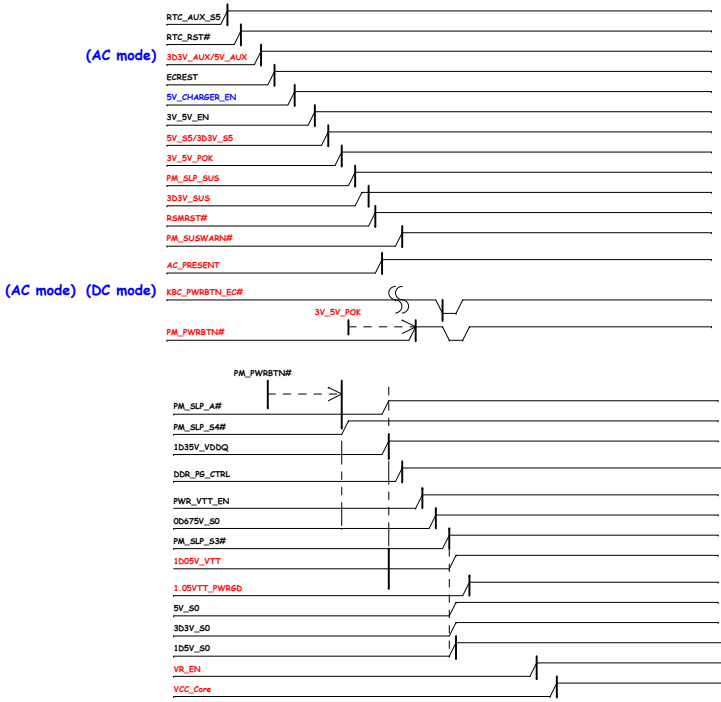
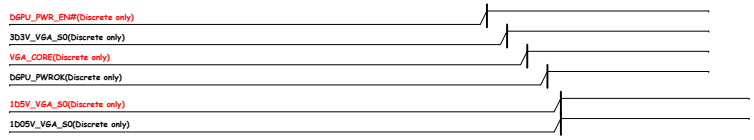
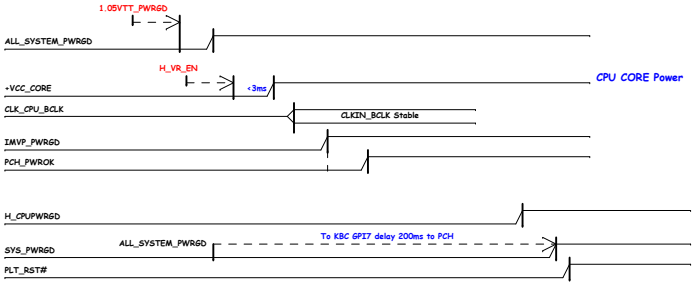
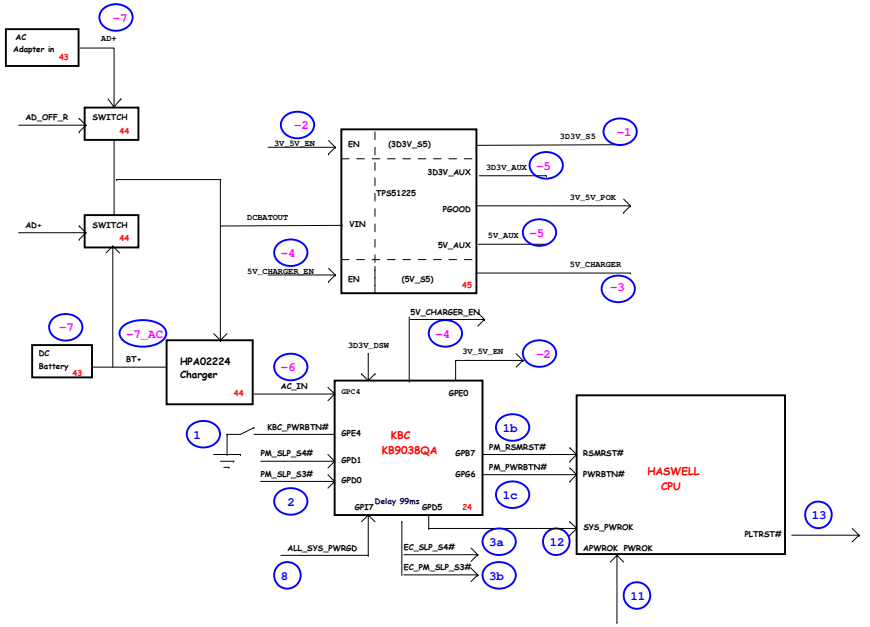
Intel-Power Up Sequence

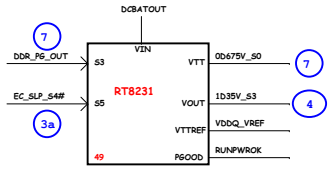


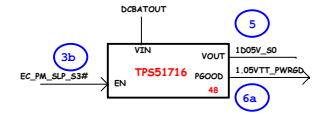


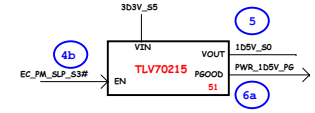


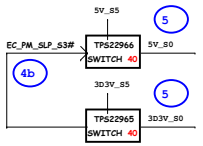
HASWELL POWER UP SEQUENCE DIAGRAM

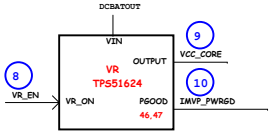


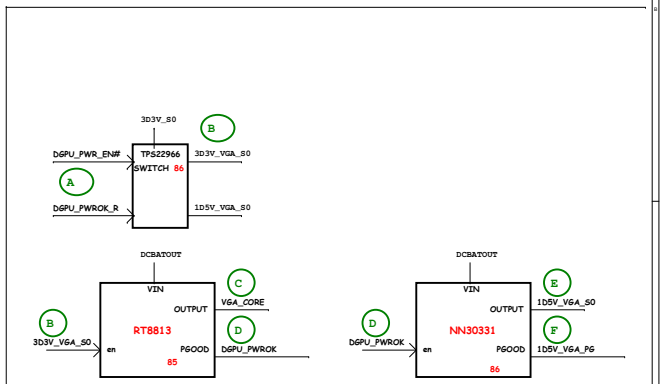












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Title: Power Sequence

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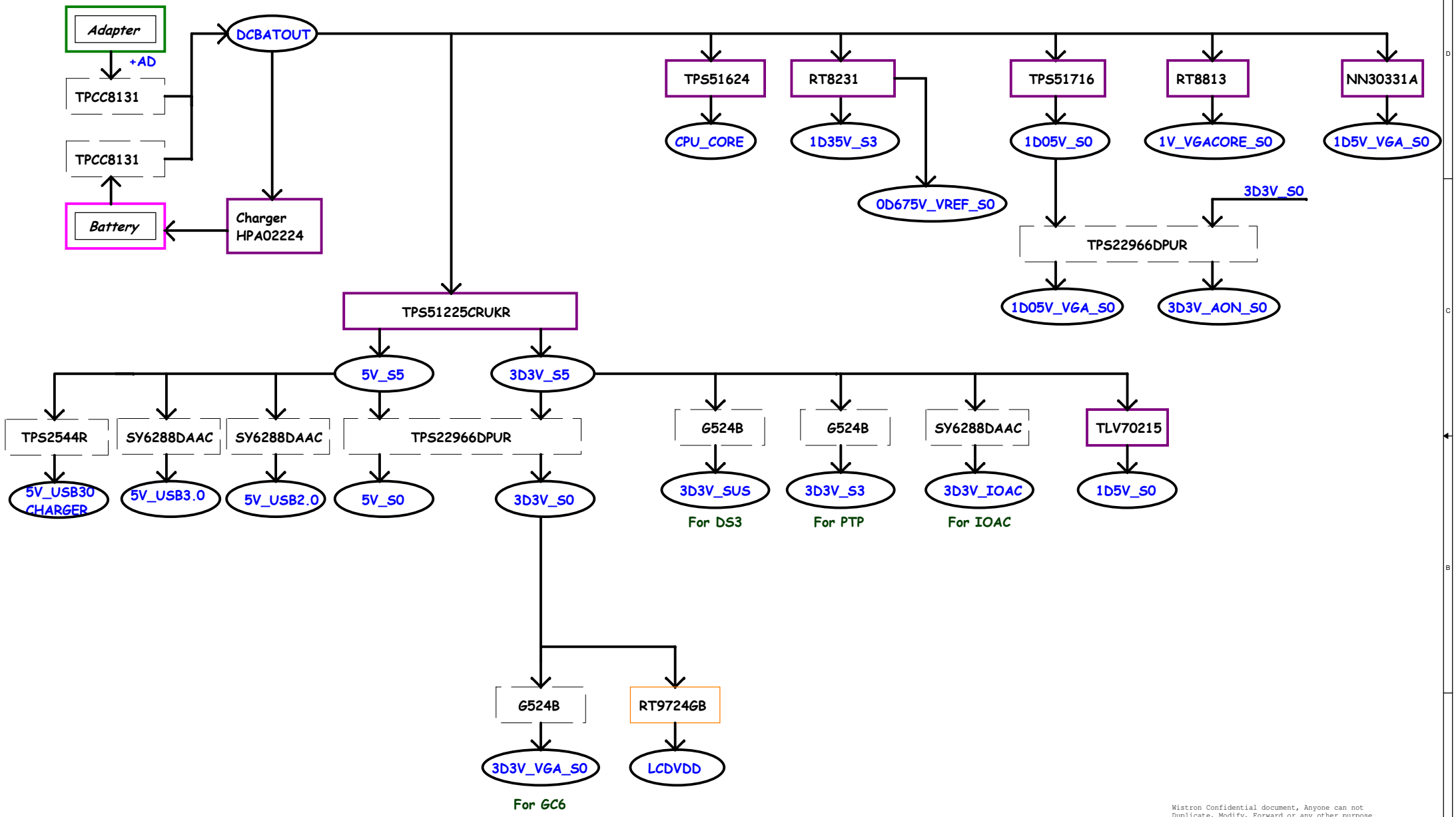

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Title: Power Block Diagram

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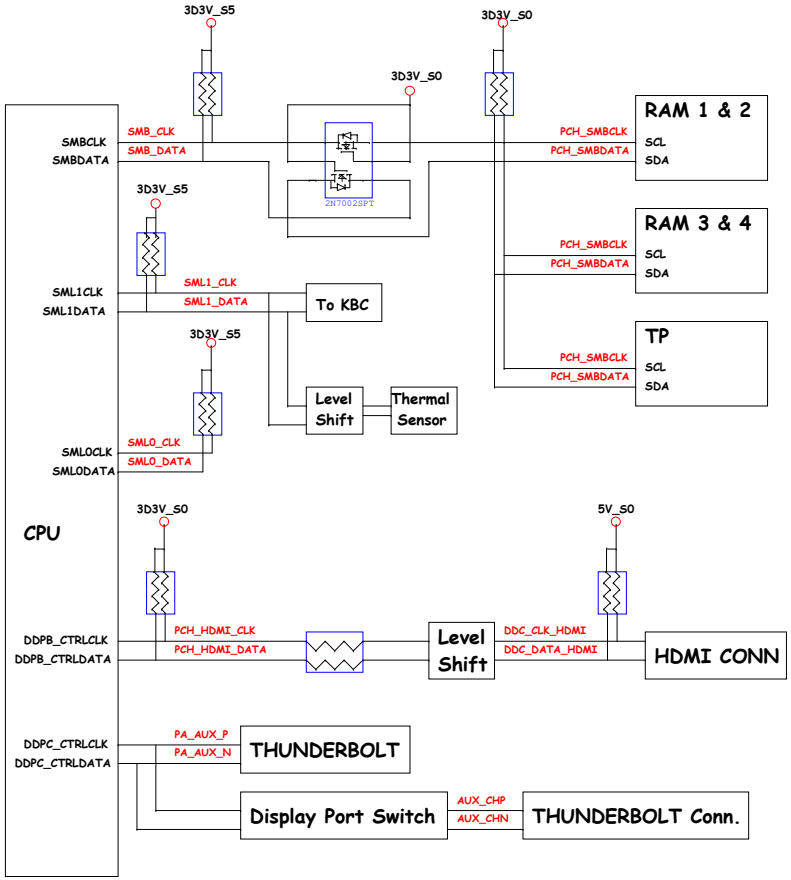
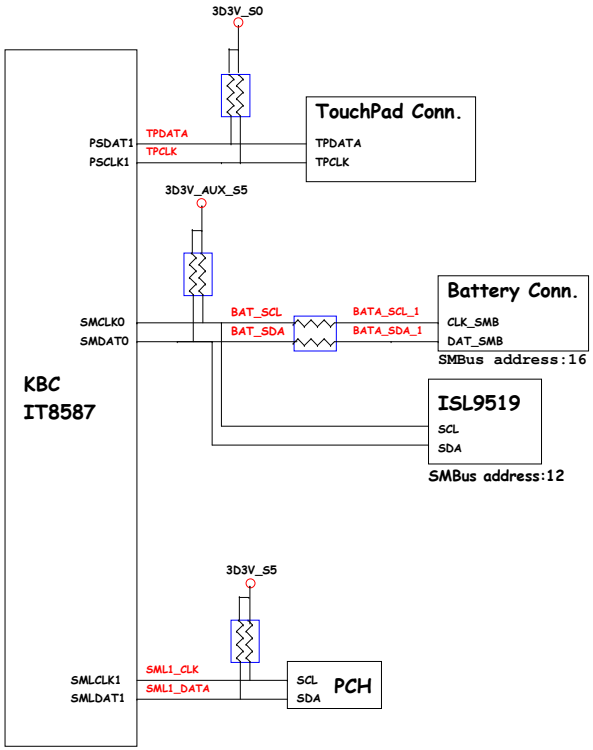
PCH SMBus Block Diagram



KBC SMBus Block Diagram



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Title: SMBUS BLOCK DIAGRAM

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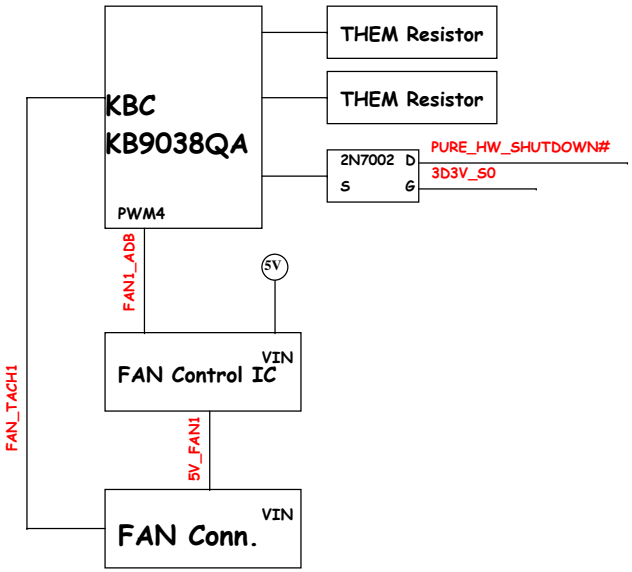
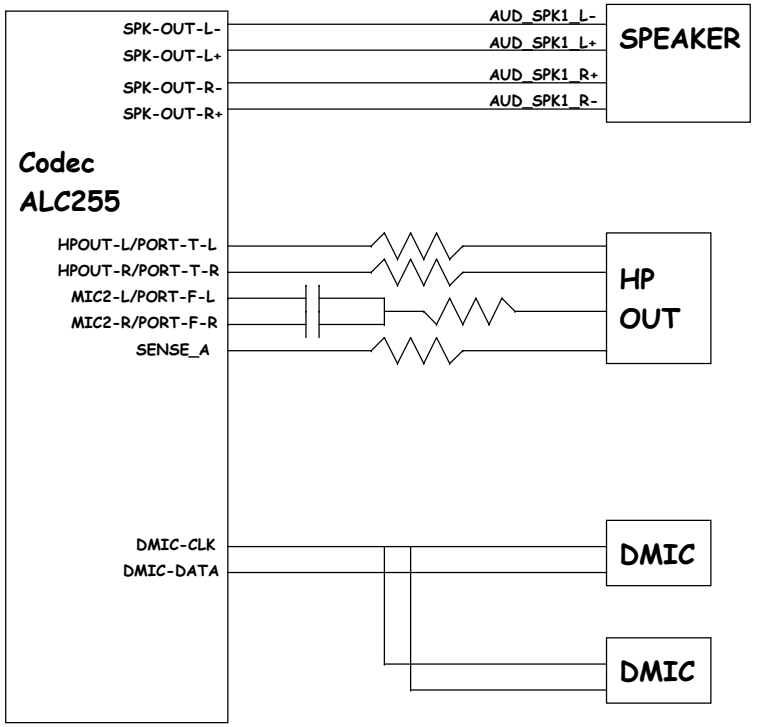
Thermal Block Diagram



Audio Block Diagram



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Title: **THERMAL/AUDIO BLOCK DIAGRAM**

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