


# Wistron Confidential

## MV1

2010/1/21

REV :MV-01

<Core Design>	
	
<small>Wistron Incorporated 21F, 88, Hsin Tai Wu Rd Hsichih, Taipei</small>	
<b>Cover</b>	
<small>Title</small>	
<small>Size</small> A3	<small>Document Number</small> <b>PATEK</b>
<small>Date</small> Thursday, January 21, 2010	<small>Rev</small> -1
<small>Sheet 1 of 50</small>	



## RS880M strapping

<b>STRAP_DEBUG_BUS_GPIO_ENABLEb</b> Enables the Test Debug Bus using GPIO. (PIN: RS880M--> VSYNC) 0 : Enable * 1 : Disable
<b>RS880: Enableg Side port memory ( RS880 use HSYNC)</b> * 0 : Enable 1 : Disable
<b>SUS_STAT#</b> Selects Loading of STRAPS From EEPROM *1 : Bypass the loading of EEPROM straps and use Hardware Default Values 0 : I2C Master can load strap values from EEPROM if connected, or use default values if not connected

## SB820M strapping

Note: SB820 has 15K internal PU FOR PCI\_AD[27:23]

	PCI_AD27	PCI_AD26	PCI_AD25	PCI_AD24	PCI_AD23
<b>PULL HIGH</b>	USE PCI PLL (DEFAULT)	Disable ILA AUTORUN (DEFAULT)	USE FC PLL (DEFAULT)	USE DEFAULT PCIE STRAPS (DEFAULT)	Disable PCI MEM BOOT (DEFAULT)
<b>PULL LOW</b>	BYPASS PCI PLL	Enable ILA AUTORUN	BYPASS FC PLL	USE EEPROM PCIE STRAPS	Enable PCI MEM BOOT

	AZ_SDOUTh	PCI_CLK1	PCI_CLK2	PCI_CLK3	PCI_CLK4	LPC_CLK_KBC (LPCCLK0)	LPC_CLK_DB (LPCCLK1)	SB_GPO200 , SB_GPO199 ROM TYPE:
<b>PULL HIGH</b>	LOW POWER MODE	Allow PCIE GEN2 DEFAULT	WatchDOG (NB_PWRGD) ENABLED	USE DEBUG STRAPS	non_Fusion CLOCK mode DEFAULT	ENABLE EC	CLKGEN ENABLED (Use Internal)	H, H = Reserved H, L = SPI ROM DEFAULT
<b>PULL LOW</b>	PERFORMANCE MODE DEFAULT	Force PCIE GEN1	WatchDog (NB_PWRGD) DISABLED DEFAULT	IGNORE DEBUG STRAPS DEFAULT	Fusion CLOCK mode	DISABLE EC DEFAULT	CLKGEN DISABLED (Use External) DEFAULT	L, H = LPC ROM L, L = FWH ROM

## SMBUS Control Table

	SOURCE	BATT	THERMAL SENSOR	CLK GEN	SODIMM	G-SENSOR	SMSC1098	SB-TSI
AB1A_DATA AB1A_CLK	SMSC1098	V	X	X	X	X	X	X
SB_SMB_CLK1 SB_SMB_DAT1	SB820M	X	X	X	X	X	X	X
SB_SMB_CLK0 SB_SMB_DAT0	SB820M	X	V	V	V	V	X	X
CPU_SID_SB700 CPU_SID_SB700	CPU	X	X	X	X	X	X	V

## PCIE routing

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LANE 0	LAN
LANE 3	NEW CARD
LANE 4	WLAN

## USB table

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Pair	Device
	USB-FSD1 FPR
	USB-9 Bluetooth
	USB-8 WLAN
	USB-7 WWAN
	USB-6 USB Card Reader
	USB-5 Right Side
	USB-4 USB Camera
	USB-3 Right Side
	USB-2 Left Side (e-SATA combo)
	USB-1 New Card
	USB-0 Left Side (S/W Debug port)

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<b>NOTES</b>		
File		
Size A3	Document Number	Rev
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SEC 3 OF 8 MEMORY\_A

M_A_DQ63	AA12	MA_DATA63
M_A_DQ62	AB12	MA_DATA62
M_A_DQ61	AA14	MA_DATA61
M_A_DQ60	AB14	MA_DATA60
M_A_DQ59	W11	MA_DATA59
M_A_DQ58	Y12	MA_DATA58
M_A_DQ57	AD13	MA_DATA57
M_A_DQ56	AB15	MA_DATA56
M_A_DQ55	AB15	MA_DATA55
M_A_DQ54	AB15	MA_DATA54
M_A_DQ53	AB17	MA_DATA53
M_A_DQ52	Y17	MA_DATA52
M_A_DQ51	AD18	MA_DATA51
M_A_DQ50	W14	MA_DATA50
M_A_DQ49	Y16	MA_DATA49
M_A_DQ48	AD17	MA_DATA48
M_A_DQ47	Y16	MA_DATA47
M_A_DQ46	AD18	MA_DATA46
M_A_DQ45	AD21	MA_DATA45
M_A_DQ44	AB21	MA_DATA44
M_A_DQ43	AB18	MA_DATA43
M_A_DQ42	AA18	MA_DATA42
M_A_DQ41	AA20	MA_DATA41
M_A_DQ40	Y20	MA_DATA40
M_A_DQ39	AA20	MA_DATA39
M_A_DQ38	V22	MA_DATA38
M_A_DQ37	W21	MA_DATA37
M_A_DQ36	Y22	MA_DATA36
M_A_DQ35	AA21	MA_DATA35
M_A_DQ34	AB22	MA_DATA34
M_A_DQ33	AB24	MA_DATA33
M_A_DQ32	Y24	MA_DATA32
M_A_DQ31	H20	MA_DATA31
M_A_DQ30	H20	MA_DATA30
M_A_DQ29	E22	MA_DATA29
M_A_DQ28	E21	MA_DATA28
M_A_DQ27	H18	MA_DATA27
M_A_DQ26	H24	MA_DATA26
M_A_DQ25	F20	MA_DATA25
M_A_DQ24	F20	MA_DATA24
M_A_DQ23	C23	MA_DATA23
M_A_DQ22	B22	MA_DATA22
M_A_DQ21	F18	MA_DATA21
M_A_DQ20	E18	MA_DATA20
M_A_DQ19	E20	MA_DATA19
M_A_DQ18	D22	MA_DATA18
M_A_DQ17	C19	MA_DATA17
M_A_DQ16	G18	MA_DATA16
M_A_DQ15	G17	MA_DATA15
M_A_DQ14	C17	MA_DATA14
M_A_DQ13	E14	MA_DATA13
M_A_DQ12	E14	MA_DATA12
M_A_DQ11	H17	MA_DATA11
M_A_DQ10	E17	MA_DATA10
M_A_DQ9	E15	MA_DATA9
M_A_DQ8	H15	MA_DATA8
M_A_DQ7	E13	MA_DATA7
M_A_DQ6	H11	MA_DATA6
M_A_DQ5	H12	MA_DATA5
M_A_DQ4	C13	MA_DATA4
M_A_DQ3	G14	MA_DATA3
M_A_DQ2	H14	MA_DATA2
M_A_DQ1	F12	MA_DATA1
M_A_DQ0	G12	MA_DATA0

M\_A\_A15[0..8]

MA_DM7	Y13	M_A_DM7
MA_DM6	AB16	M_A_DM6
MA_DM5	Y19	M_A_DM5
MA_DM4	AC24	M_A_DM4
MA_DM3	F24	M_A_DM3
MA_DM2	E19	M_A_DM2
MA_DM1	C15	M_A_DM1
MA_DM0	E12	M_A_DM0

M\_A\_CLK\_DDR1[8]

M\_A\_CLK\_DDR2[8]

M\_A\_CLK\_DDR2R[8]

M\_A\_B\_S92[8]

M\_A\_RAS#

M\_A\_CAS#

M\_A\_WE#

M\_A\_CS1#

M\_A\_CS1#

M\_A\_CKE1[8]

M\_A\_CS1#

M\_A\_CS1#

M\_A\_CS1#

M\_A\_CS1#

M\_A\_CS1#

M\_A\_CS1#

SEC 4 OF 8 MEMORY\_B

M_B_DQ63	AD11	MB_DATA63
M_B_DQ62	AE11	MB_DATA62
M_B_DQ61	AE14	MB_DATA61
M_B_DQ60	AE14	MB_DATA60
M_B_DQ59	Y11	MB_DATA59
M_B_DQ58	AB11	MB_DATA58
M_B_DQ57	AC12	MB_DATA57
M_B_DQ56	AE13	MB_DATA56
M_B_DQ55	AE16	MB_DATA55
M_B_DQ54	AE16	MB_DATA54
M_B_DQ53	AC18	MB_DATA53
M_B_DQ52	AE19	MB_DATA52
M_B_DQ51	AE14	MB_DATA51
M_B_DQ50	AD15	MB_DATA50
M_B_DQ49	AE18	MB_DATA49
M_B_DQ48	AE18	MB_DATA48
M_B_DQ47	AD20	MB_DATA47
M_B_DQ46	AC20	MB_DATA46
M_B_DQ45	AF23	MB_DATA45
M_B_DQ44	AE24	MB_DATA44
M_B_DQ43	AE20	MB_DATA43
M_B_DQ42	AE20	MB_DATA42
M_B_DQ41	AE22	MB_DATA41
M_B_DQ40	AC22	MB_DATA40
M_B_DQ39	AE25	MB_DATA39
M_B_DQ38	AD26	MB_DATA38
M_B_DQ37	AA25	MB_DATA37
M_B_DQ36	AA26	MB_DATA36
M_B_DQ35	AE24	MB_DATA35
M_B_DQ34	AD24	MB_DATA34
M_B_DQ33	AA23	MB_DATA33
M_B_DQ32	AD24	MB_DATA32
M_B_DQ31	C24	MB_DATA31
M_B_DQ30	G23	MB_DATA30
M_B_DQ29	D26	MB_DATA29
M_B_DQ28	C26	MB_DATA28
M_B_DQ27	G26	MB_DATA27
M_B_DQ26	G26	MB_DATA26
M_B_DQ25	E24	MB_DATA25
M_B_DQ24	E24	MB_DATA24
M_B_DQ23	C24	MB_DATA23
M_B_DQ22	B24	MB_DATA22
M_B_DQ21	C20	MB_DATA21
M_B_DQ20	B20	MB_DATA20
M_B_DQ19	C26	MB_DATA19
M_B_DQ18	D24	MB_DATA18
M_B_DQ17	A21	MB_DATA17
M_B_DQ16	D20	MB_DATA16
M_B_DQ15	D16	MB_DATA15
M_B_DQ14	D18	MB_DATA14
M_B_DQ13	D14	MB_DATA13
M_B_DQ12	C16	MB_DATA12
M_B_DQ11	A20	MB_DATA11
M_B_DQ10	A19	MB_DATA10
M_B_DQ9	A16	MB_DATA9
M_B_DQ8	A15	MB_DATA8
M_B_DQ7	A15	MB_DATA7
M_B_DQ6	D12	MB_DATA6
M_B_DQ5	C14	MB_DATA5
M_B_DQ4	D11	MB_DATA4
M_B_DQ3	A14	MB_DATA3
M_B_DQ2	A14	MB_DATA2
M_B_DQ1	A11	MB_DATA1
M_B_DQ0	C11	MB_DATA0

M\_B\_A15[0..8]

M\_B\_A15[0..8]

M\_B\_A15[0..8]

M\_B\_A15[0..8]

M\_B\_A15[0..8]

M\_B\_A15[0..8]

M\_B\_A15[0..8]

M\_B\_A15[0..8]

M\_B\_A15[0..8]

M\_B\_A15[0..8]

MB_DM7	AD12	M_B_DM7
MB_DM6	AC16	M_B_DM6
MB_DM5	AE22	M_B_DM5
MB_DM4	AB20	M_B_DM4
MB_DM3	E25	M_B_DM3
MB_DM2	A22	M_B_DM2
MB_DM1	B16	M_B_DM1
MB_DM0	A12	M_B_DM0

MB_DQ5	AE12	M_B_DQ5
MB_DQ4	AE21	M_B_DQ4
MB_DQ3	AC26	M_B_DQ3
MB_DQ2	F26	M_B_DQ2
MB_DQ1	A24	M_B_DQ1
MB_DQ0	D18	M_B_DQ0

MB_DQ5	AE12	M_B_DQ5
MB_DQ4	AE21	M_B_DQ4
MB_DQ3	AC26	M_B_DQ3
MB_DQ2	F26	M_B_DQ2
MB_DQ1	A24	M_B_DQ1
MB_DQ0	D18	M_B_DQ0

MB_DQ5	AE12	M_B_DQ5
MB_DQ4	AE21	M_B_DQ4
MB_DQ3	AC26	M_B_DQ3
MB_DQ2	F26	M_B_DQ2
MB_DQ1	A24	M_B_DQ1
MB_DQ0	D18	M_B_DQ0

MB_CLK5_P	F22	M_B_CLK_DDR1
MB_CLK5_N	F22	M_B_CLK_DDR1
MB_CLK1_P	A17	M_B_CLK_DDR2
MB_CLK1_N	A18	M_B_CLK_DDR2
MB_CLK7_P	AE18	M_B_CLK_DDR2
MB_CLK7_N	AE18	M_B_CLK_DDR2

MB_BANK	J26	M_B_B_S92
MB_BANK1	U26	M_B_B_S91
MB_BANK	R24	M_B_B_S90
MB_RAS#	U25	M_B_RAS#
MB_CAS#	U24	M_B_CAS#
MB_WE#	U23	M_B_WE#

MB1_CS0	U22	M_B_CS1#
MB0_CS1	W22	M_B_CS1#
MB1_CS1	V26	M_B_CS0#
MB_CKE1	H26	M_B_CKE1
MB_CKE0	J26	M_B_CKE0

MB1_ODT0	Y26	MB1_ODT1
MB0_ODT1	W23	M_B_ODT1
MB0_ODT0	W26	M_B_ODT0

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File: CPU(2/4) DDR III

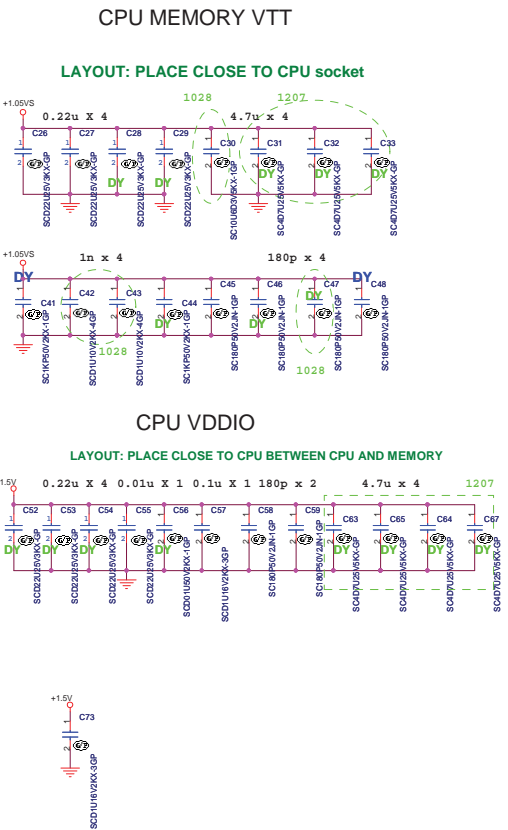
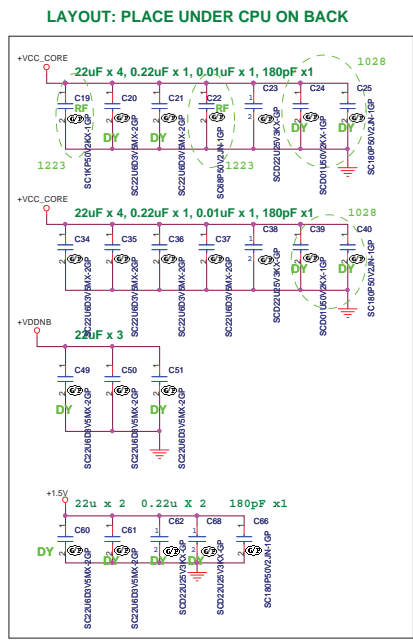
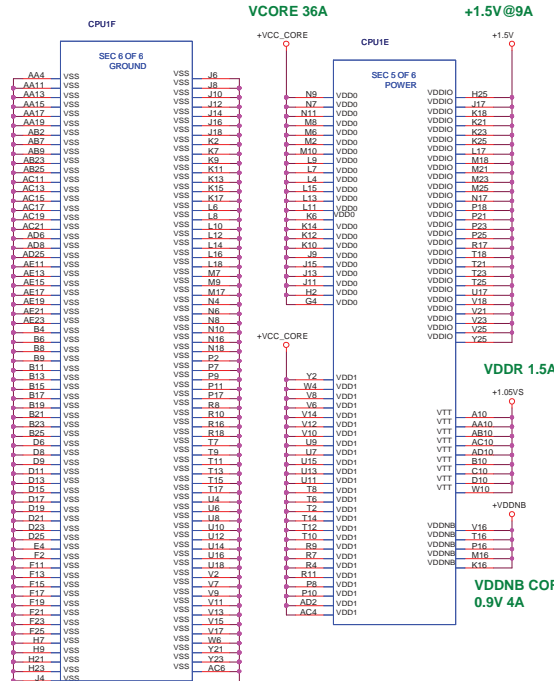
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File: **CPU(4/4) POWER**

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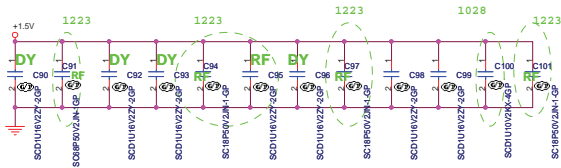




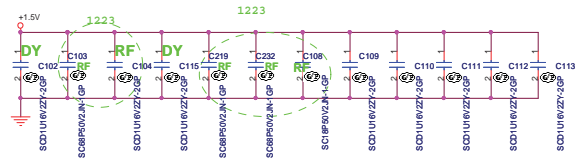
DE-COUPLING FOR CHANNEL A SODIMM



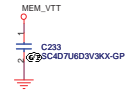
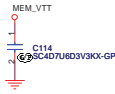
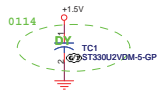
DE-COUPLING FOR CHANNEL B SODIMM



DE-COUPLING FOR CHANNEL A SODIMM (ONE CAP PER POWER PIN)



DE-COUPLING FOR CHANNEL B SODIMM (ONE CAP PER POWER PIN)

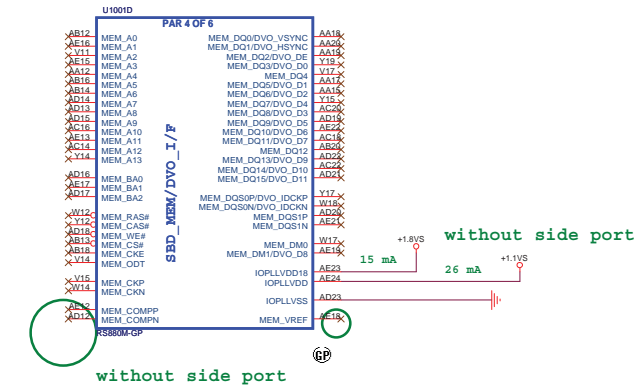


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<b>walstron</b>		Wistron Incorporated 21F, 88, Hsin Tai Wu Rd Hsichih, Taipei	
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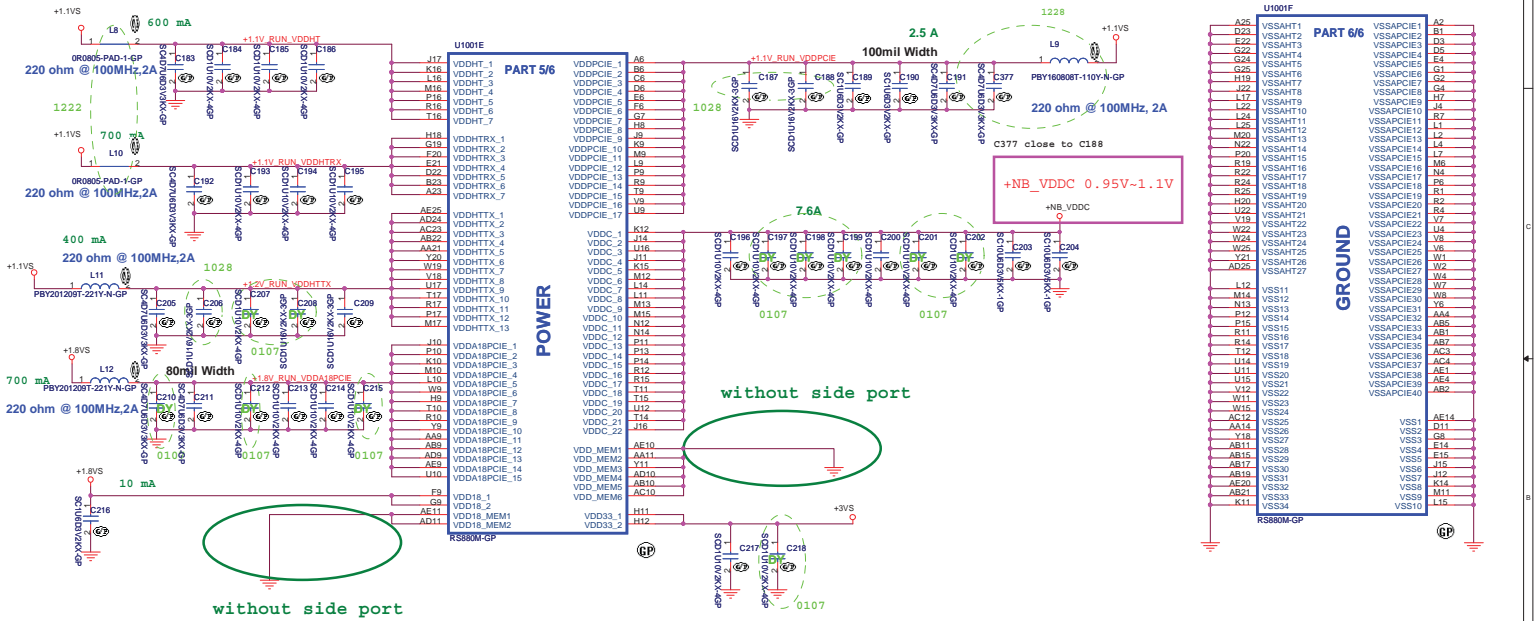
**walstron** Wistron Incorporated  
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Hsichih, Taipei

Title: **RS880M Side Port(3/4)**

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**SSID = N.B**



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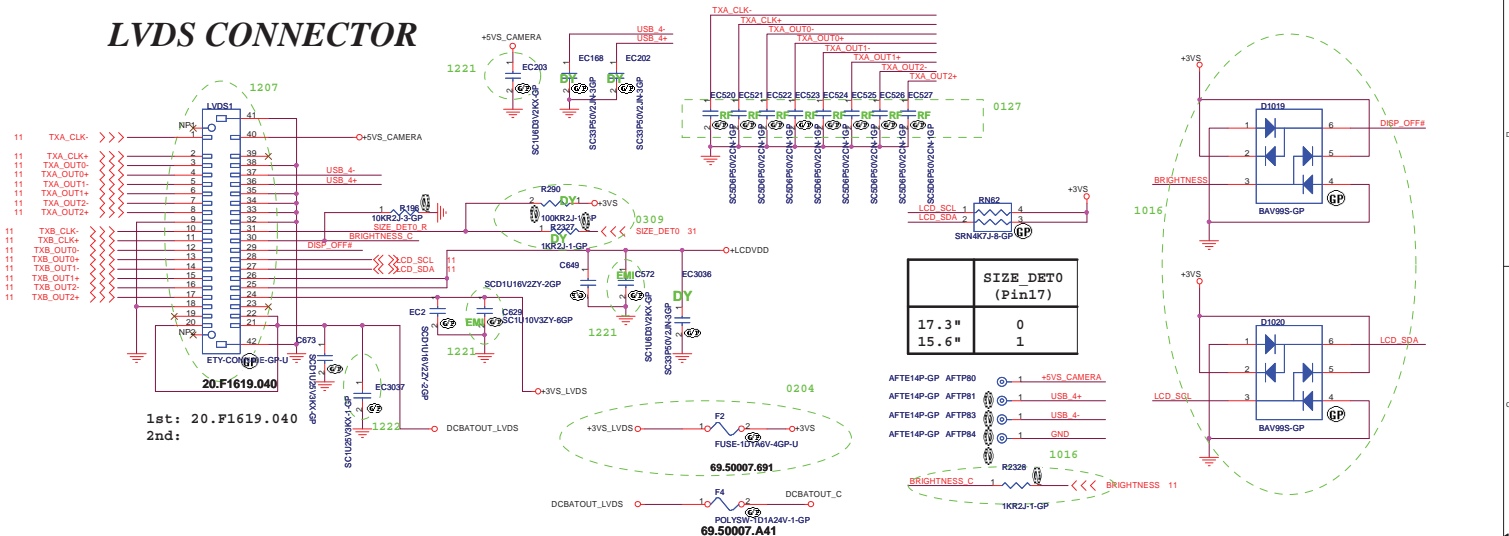
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Size A3 Document Number **PATEK** Rev **-1**

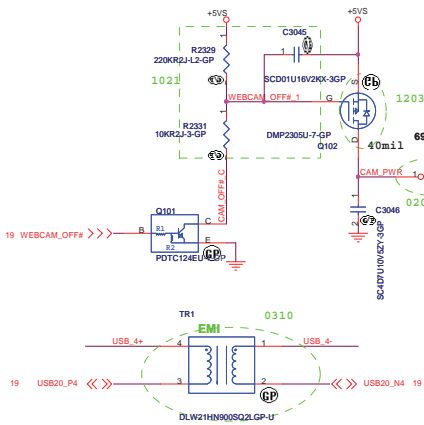
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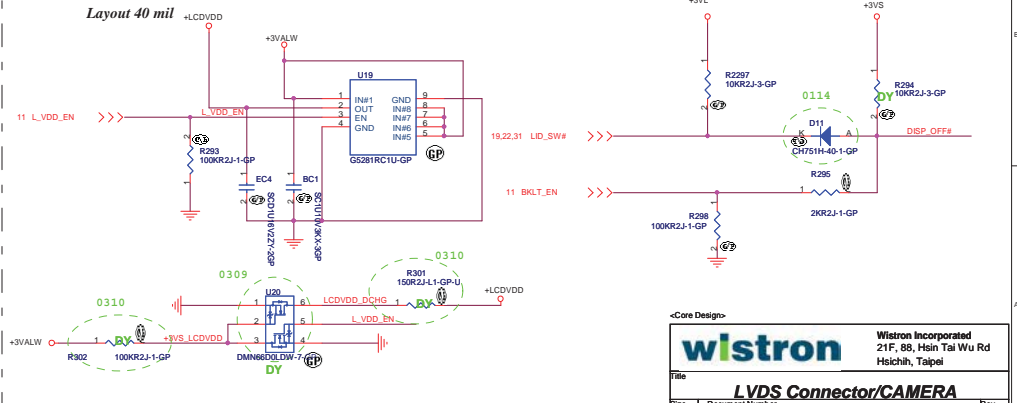
# LVDS CONNECTOR



# Camera Power&Interface



# LCD Power&Discharge



<Core Design>

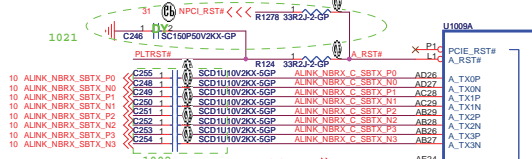
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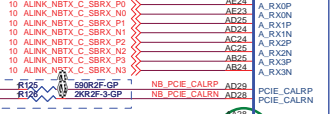
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Size A3 Document Number **PATEK** Rev **-1**

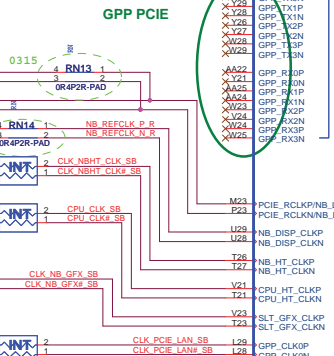
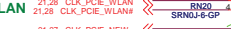
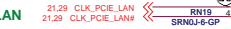
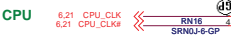
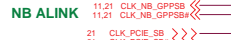
Date: Monday, March 16, 2010 Sheet 15 of 50



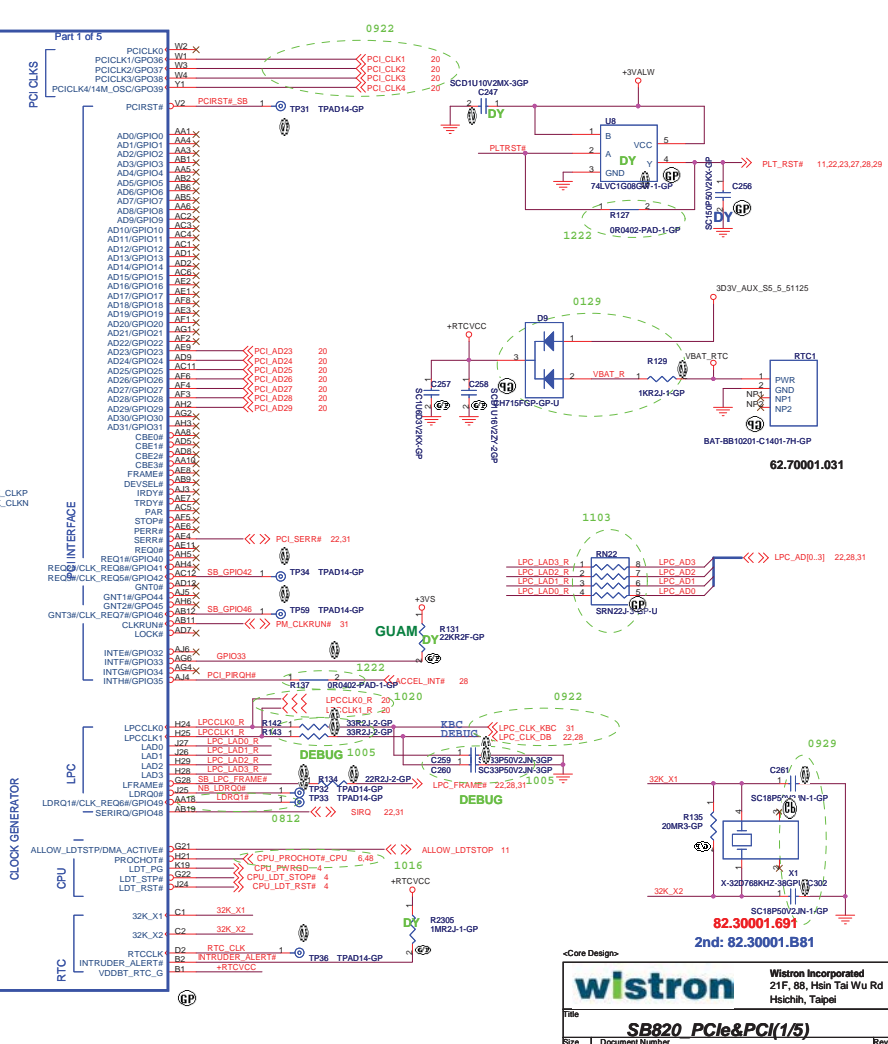
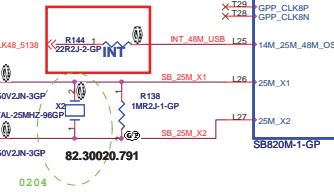
Place R <100ms form pins AD28, AD29



**GPP PCIE**



Device CLK1 sel:  
bit[1:0]=10, 48Mhz



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File: **SB200 PCIe&PCI(1/5)**  
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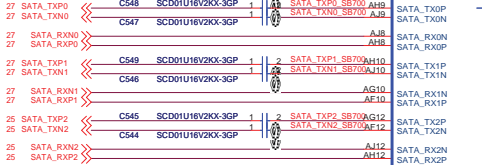
Rev: **PATEK**  
Rev: **-1**



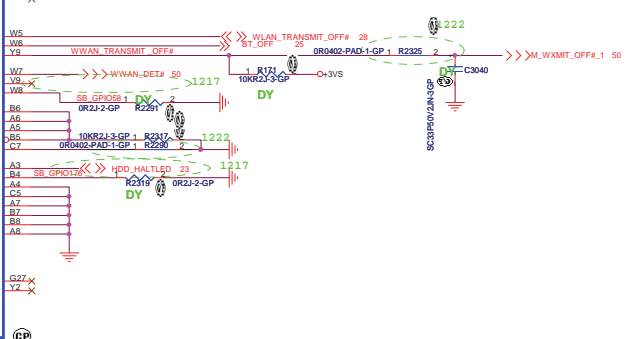
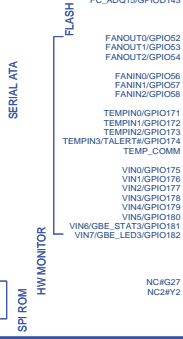
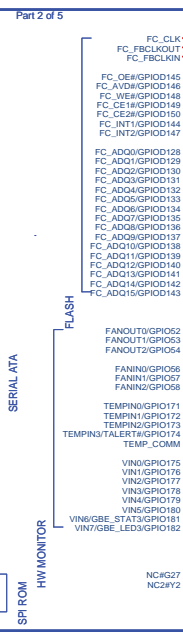
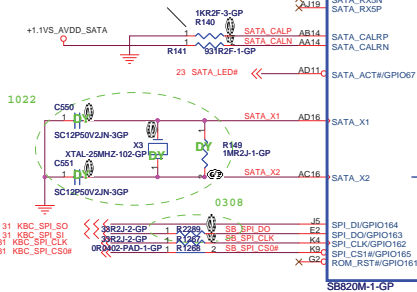
SSID = S.B

PLACE SATA AC DECOUPLING CAPS CLOSE TO SB700

SATA HDD  
SATA ODD  
ESATA



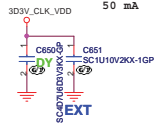
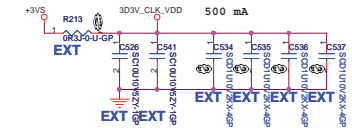
Very Close to SB820





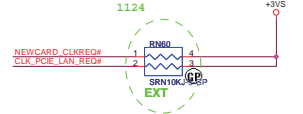
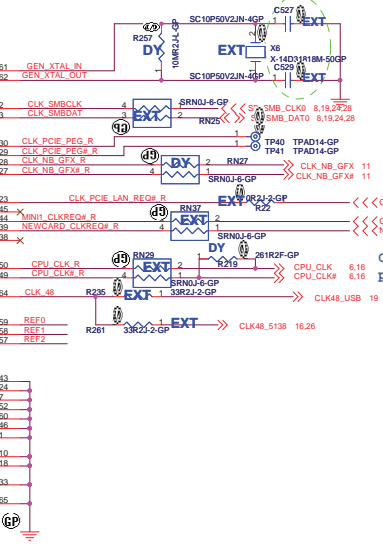
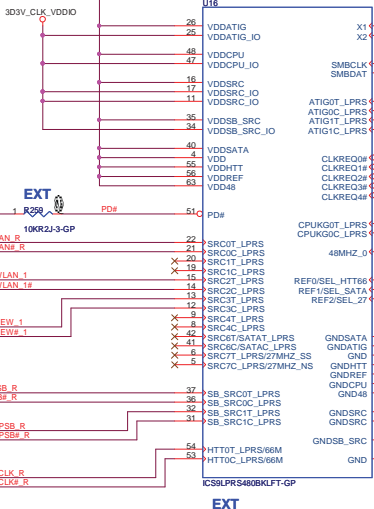
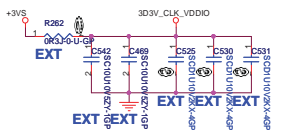






Due to PLL issue on current clock chip, the SBlncK clock need to come from SRC clocks for RS740 and RS780. Future clock chip revision will fix this.

Clock chip has internal serial terminations for differential pairs, external resistors are reserved for debug purpose.



LAN 16,29 CLK\_PCIE\_LAN 16,29 CLK\_PCIE\_LAN

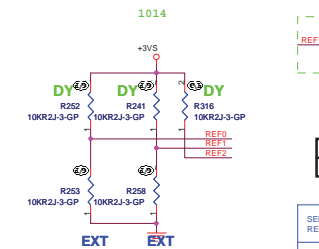
WLAN 16,28 CLK\_PCIE\_WLAN 16,28 CLK\_PCIE\_WLAN

NEW 16,27 CLK\_PCIE\_NEW 16,27 CLK\_PCIE\_NEW#

SB 16 CLK\_PCIE\_SB 16 CLK\_PCIE\_SB#

NB ALINK 11,16 CLK\_NB\_GPPSB 11,16 CLK\_NB\_GPPSB#

NB HT 11,16 CLK\_NBHT\_CLK 11,16 CLK\_NBHT\_CLK#



OSC 14M NB	
RS880M	1.1V 158R/90.9R

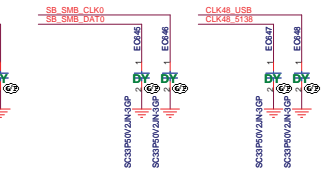
SEL_SATA	REF1	1	100 MHz non-spreading differential SRC clock
SEL_HTT66 <td>REF0</td> <td>1</td> <td>100 MHz spreading differential SRC clock</td>	REF0	1	100 MHz spreading differential SRC clock
REF0	REF1	0	66 MHz 3.3V single ended HTT clock
REF0	REF2	0	100 MHz differential HTT clock

default  
CPU\_CLK (200MHz)

NB CLOCK INPUT TABLE

NB CLOCKS	RS880M
HT_REFCLKP	100M DIFF
HT_REFCLKN	100M DIFF
REFCLK_P	14M SE (1.1V)
REFCLK_N	ref
GF_X_REFCLK	100M DIFF(IN/OUT)*
GPP_REFCLK	NC or 100M DIFF OUTPUT 100M DIFF
GPPSB_REFCLK	100M DIFF

\* RS880M can be used as clock buffer to output two PCIe reference clocks. By default, chip will configured as input mode, BIOS can program it to output mode.



<Core Design>

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File: **CLKMG IC9LPRS480**

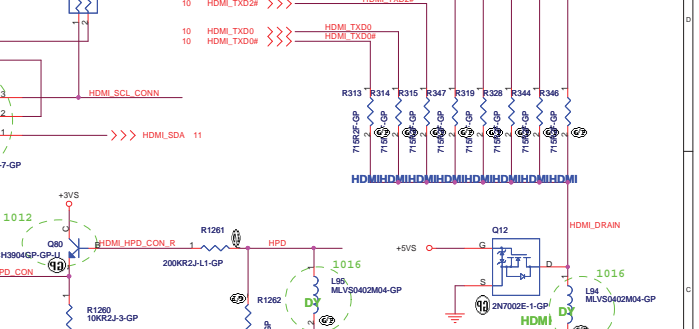
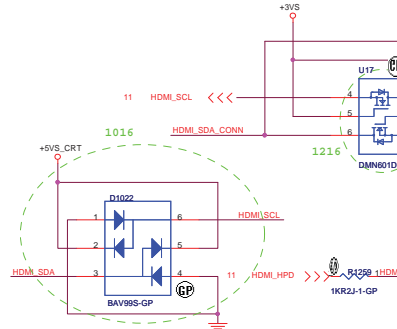
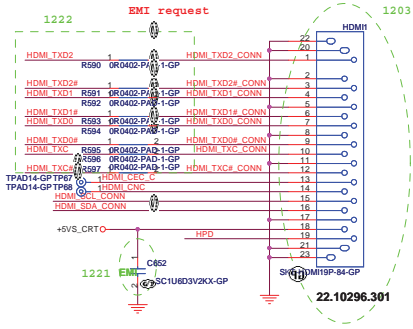
Size A3 Document Number: **PATEK**

Date: Monday, March 16, 2010 Sheet 21 of 50

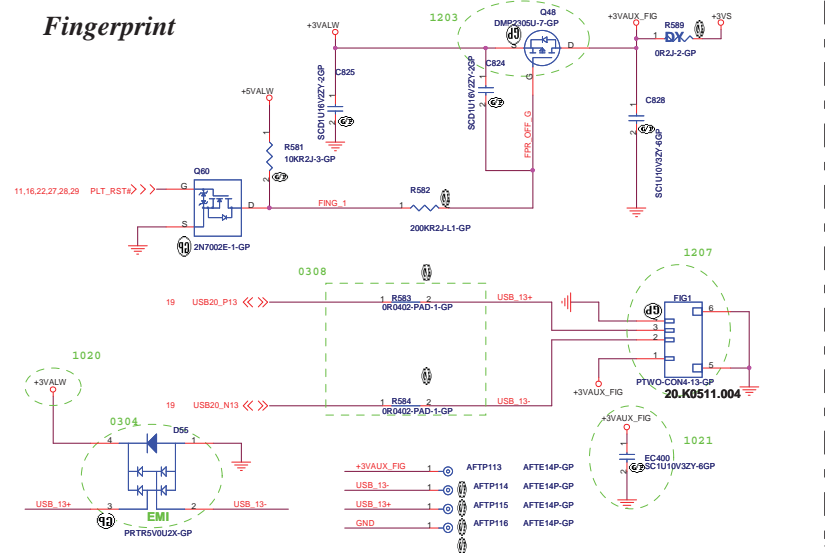
Rev -1



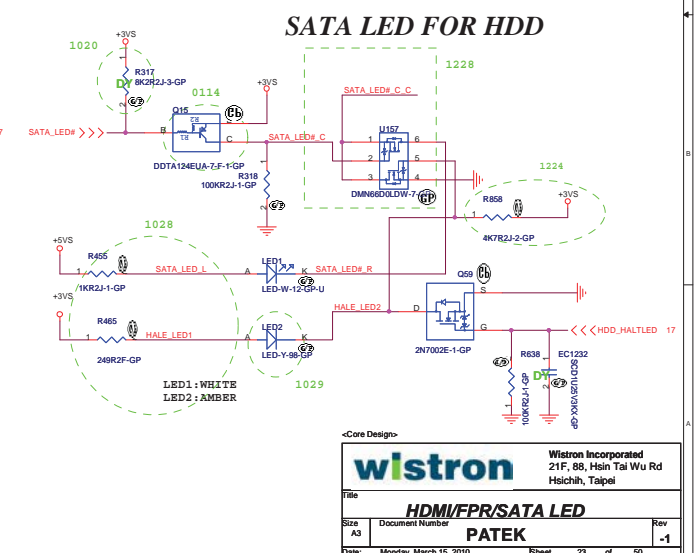
# HDMI Connector



# Fingerprint



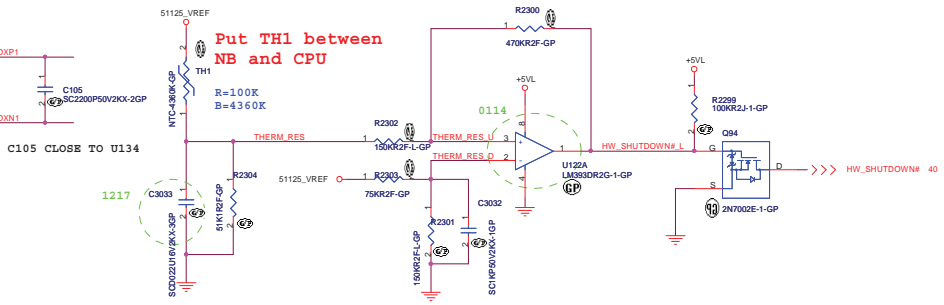
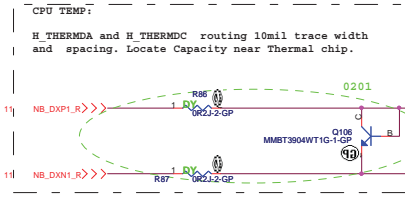
# SATA LED FOR HDD



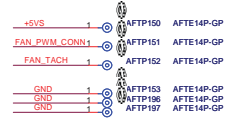
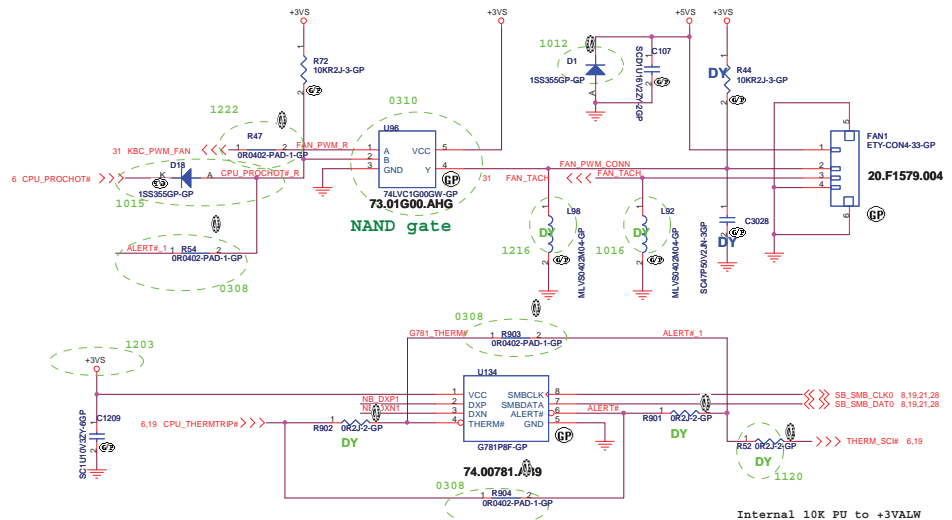
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Hsichih, Taipei

File: **HDMI/FPR/SATA LED**  
Size: A3 Document Number: **PATEK** Rev: -1  
Date: Monday, March 16, 2010 Sheet: 23 of 50



### 4 WIRE PWM Fan Control Circuit



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 Hsichih, Taipei

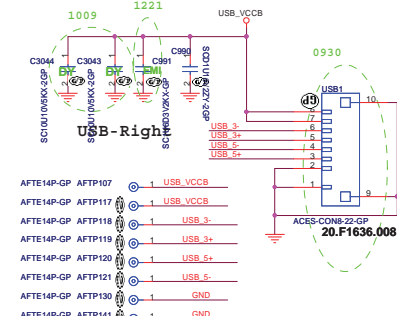
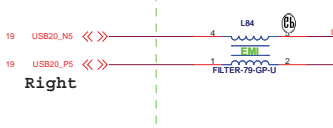
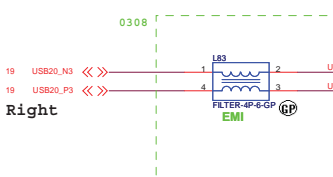
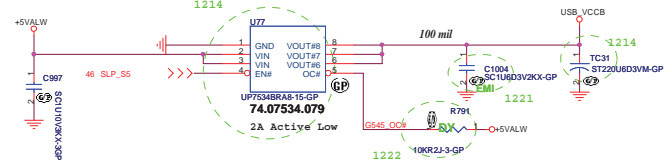
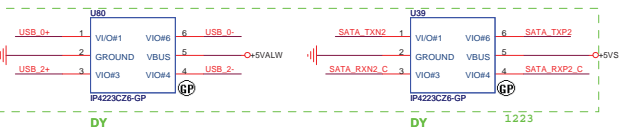
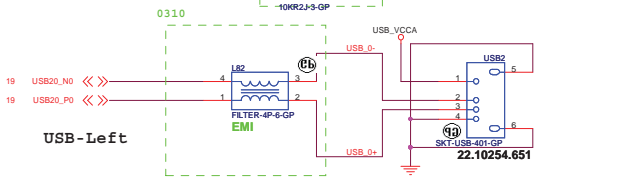
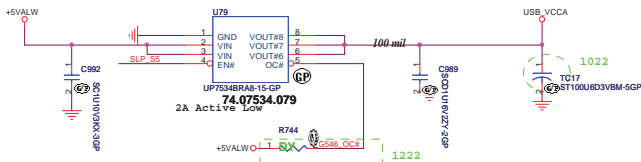
**781 THERMAL PATEK**

File: 781 THERMAL PATEK  
 Size: Document Number  
 Date: Monday, March 15, 2010 Sheet 24 of 50

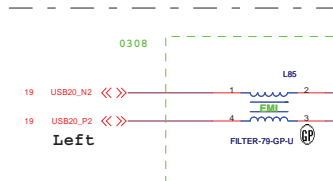
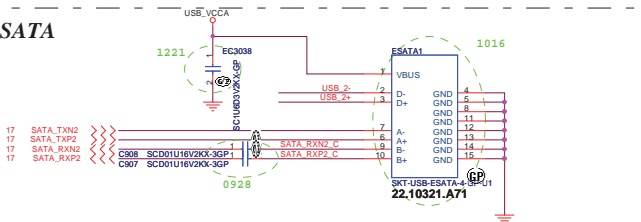
Internal 10K PU to +3VALW



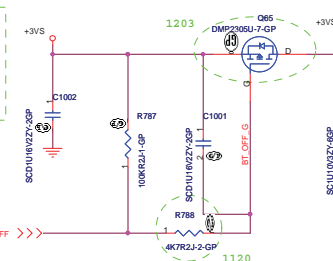
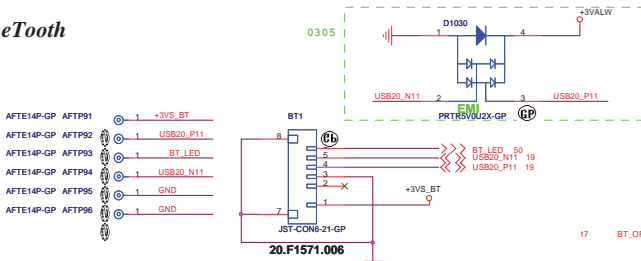
# USB & E-SATA POWER



# E-SATA



# BlueTooth



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File: **USB/BT/ESATA CONN**

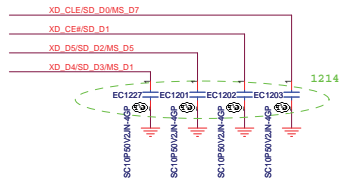
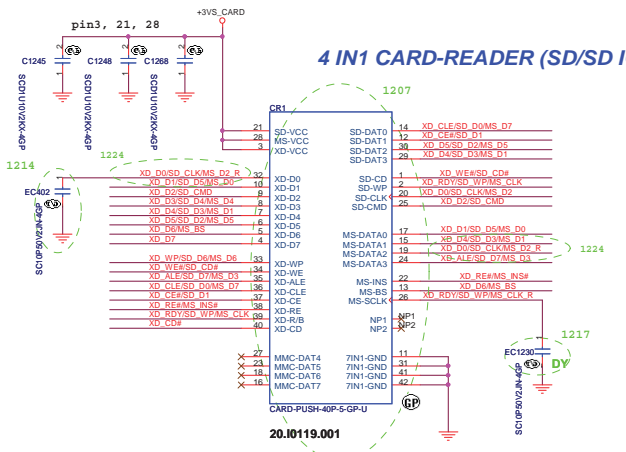
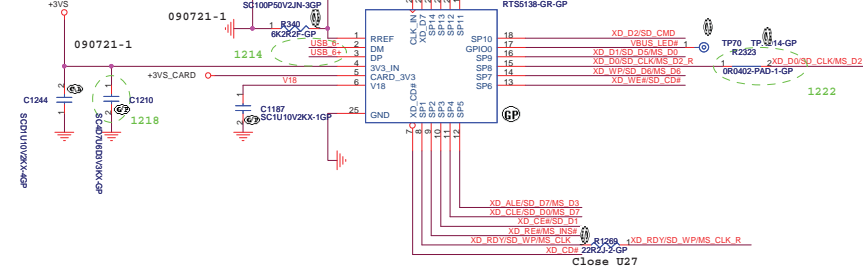
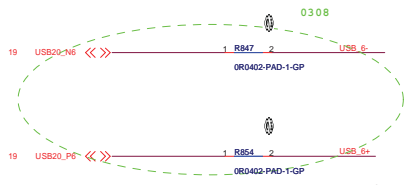
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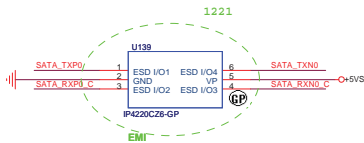
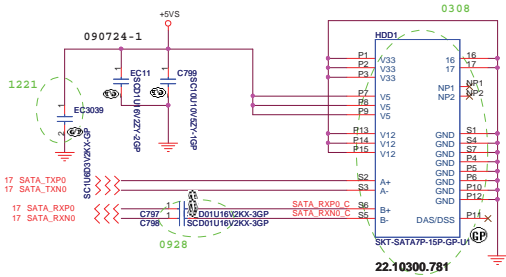
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Hsichih, Taipei

**CardReader RTS5138**

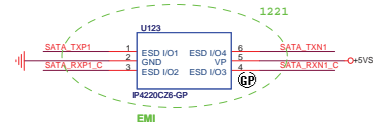
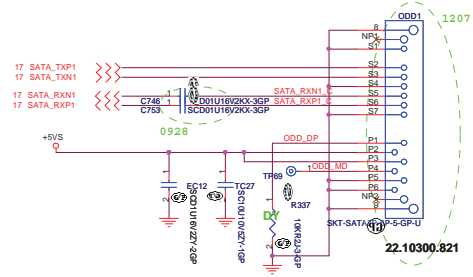
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Size	Document Number		
AS	<b>PATEK</b>		-1
Date:	Monday, March 16, 2010	Sheet 28 of 50	

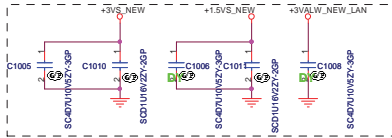
# SATA HD Connector



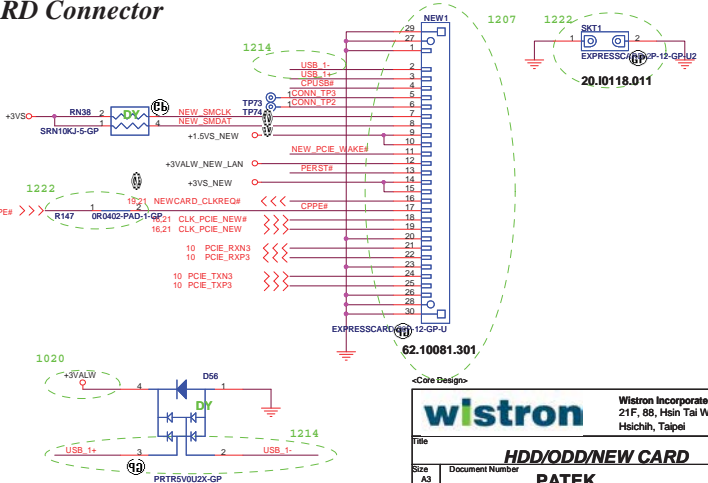
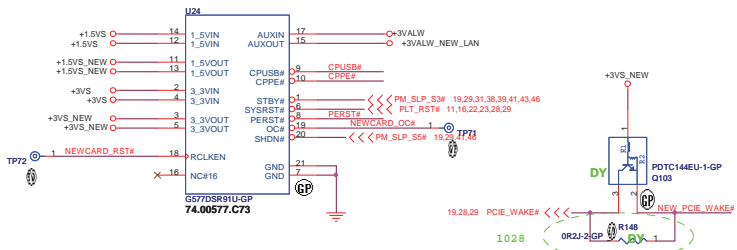
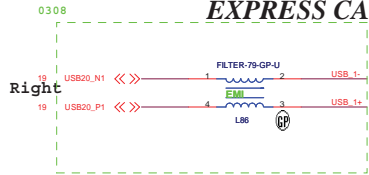
# ODD Connector



Place them Near to Connector



# EXPRESS CARD Connector



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Hsinchi, Taipei

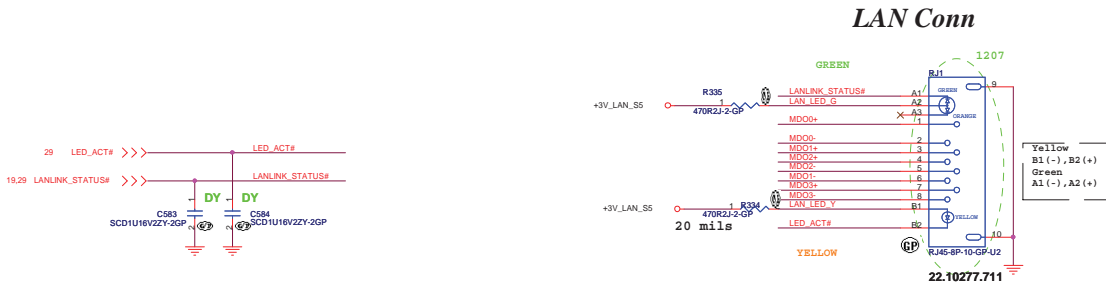
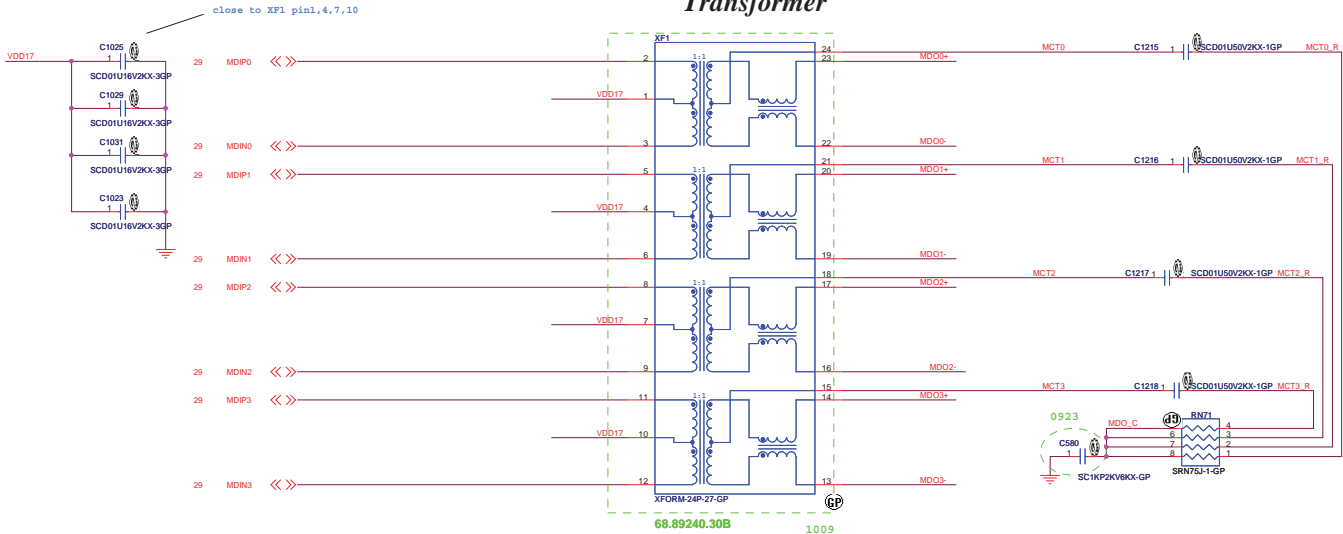
**HDD/ODD/NEW CARD**

**PATEK**

File: \_\_\_\_\_  
Size A3 Document Number \_\_\_\_\_ Rev \_\_\_\_\_  
Date: Monday, March 15, 2010 Sheet 27 of 50







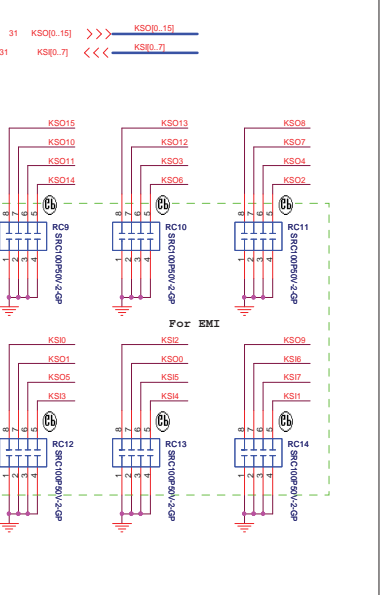
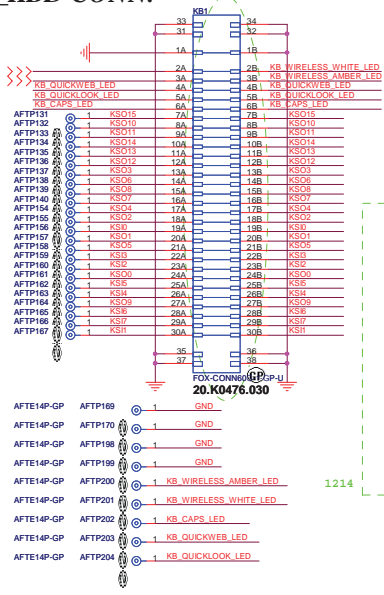
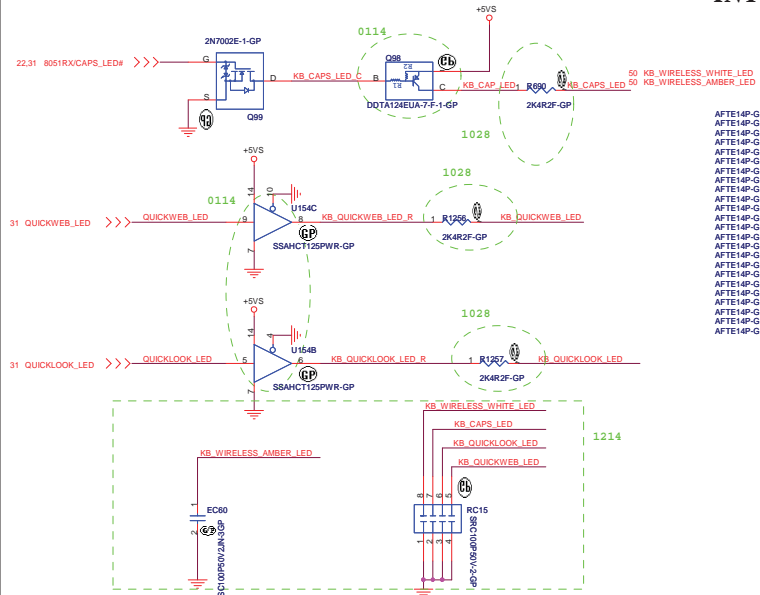
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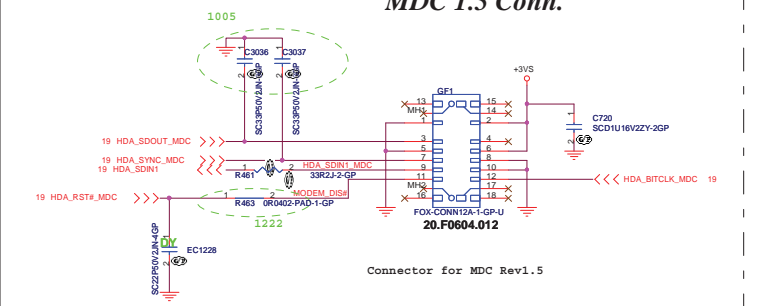
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<b>PATEK</b>		-1
Date: Monday, March 16, 2010	Sheet 30 of 50	



# INT\_KBD CONN.

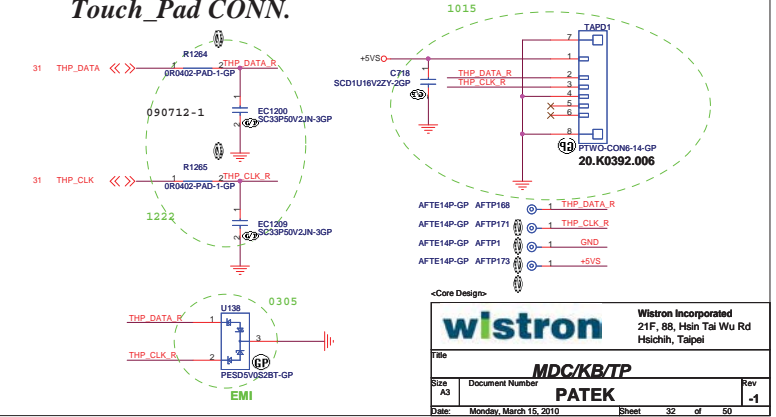


# MODEM MDC 1.5 Conn.



Connector for MDC Rev1.5

# Touch\_Pad CONN.



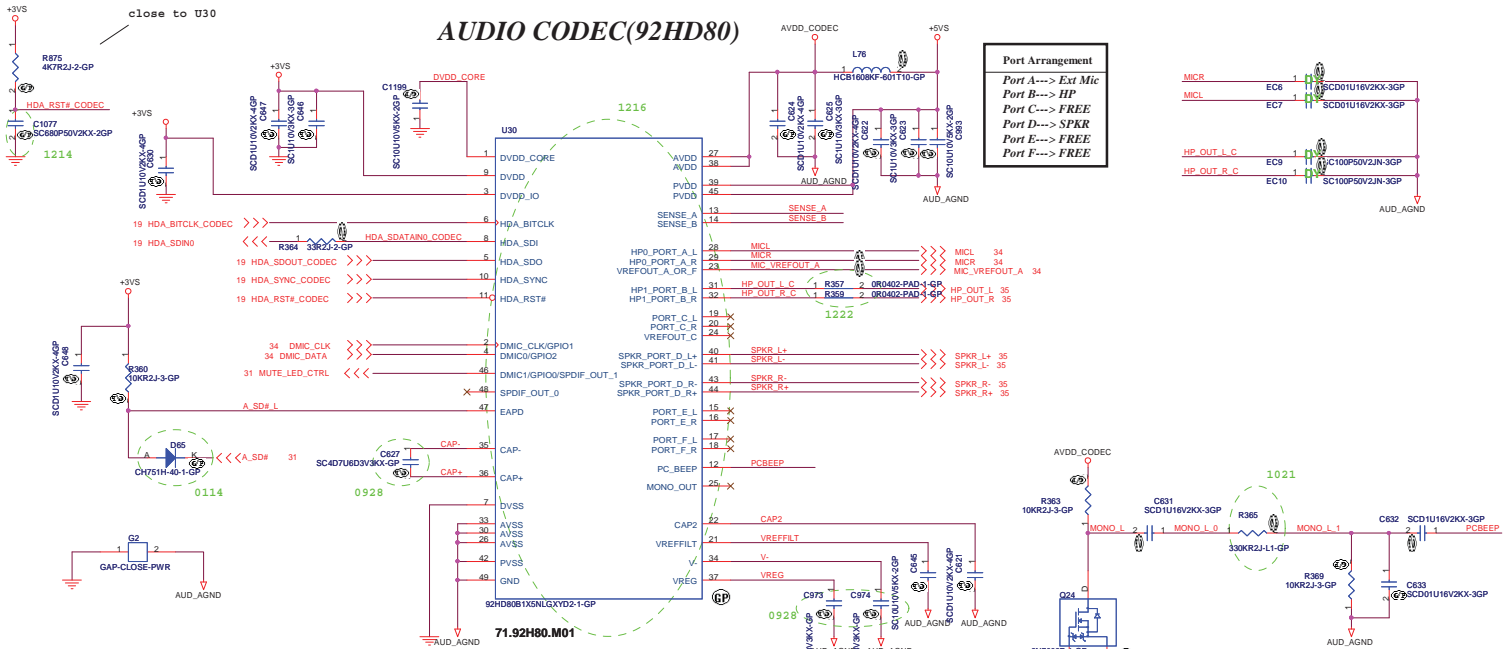
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Hsichih, Taipei

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Size	Document Number	A3	Rev
Date:	Monday, March 15, 2010	Sheet	32 of 50

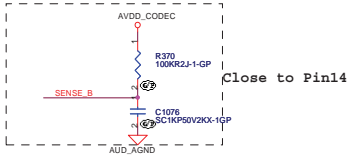
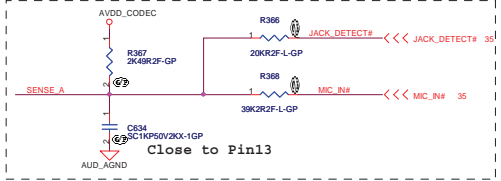
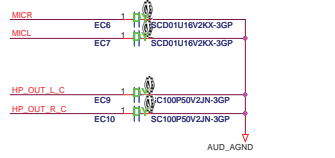


# AUDIO CODEC(92HD80)

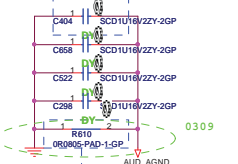


**Port Arrangement**

- Port A--> Ext Mic
- Port B--> HP
- Port C--> FREE
- Port D--> SPKR
- Port E--> FREE
- Port F--> FREE

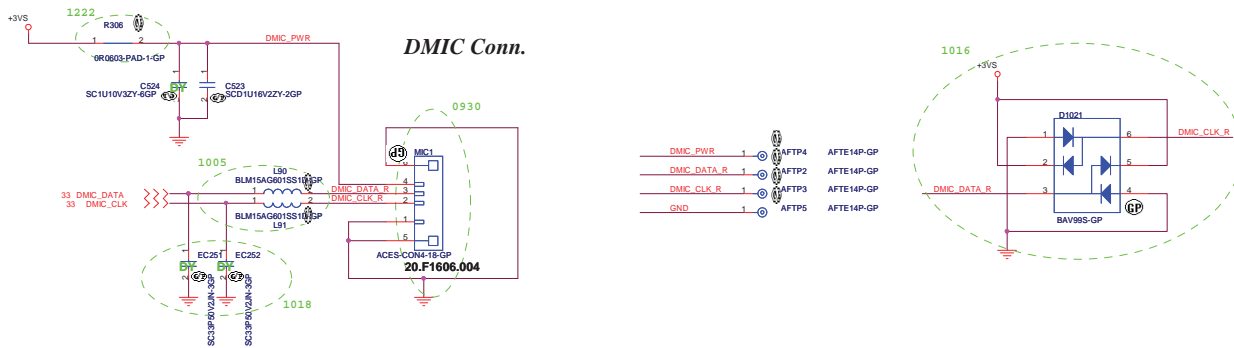


Place close to Codec chip

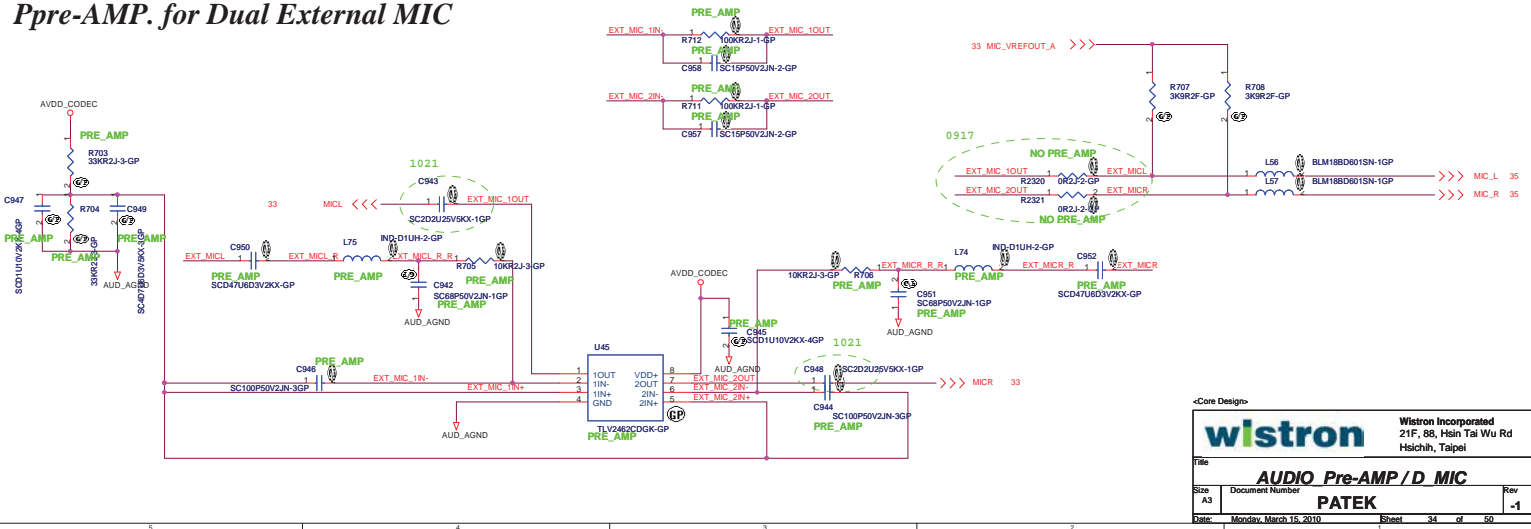


audio ground must be connect to digital ground with an 80 mil copper bridge located directly under codec to prevent ESD latch up.

# Dual Internal Digital MIC



# Ppre-AMP. for Dual External MIC



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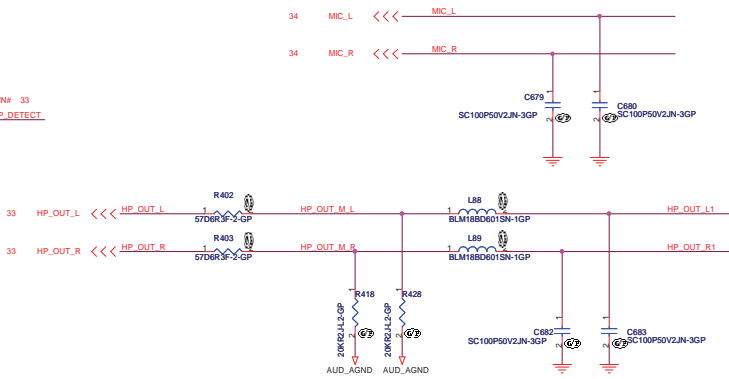
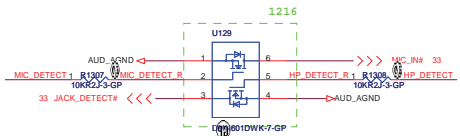
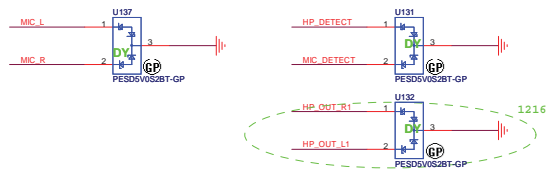
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File: **AUDIO Pre-AMP / D MIC**

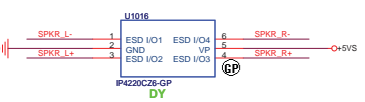
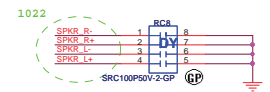
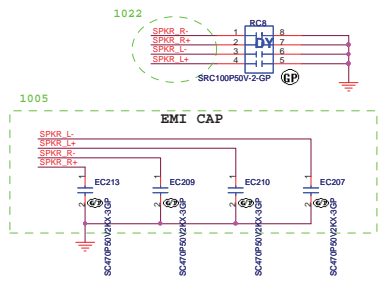
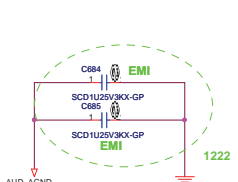
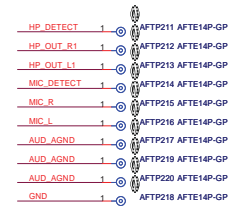
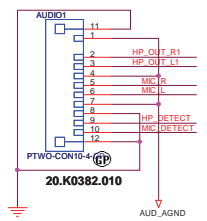
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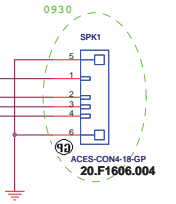
Date: Monday, March 16, 2010 Sheet 34 of 50



### AUDIO Conn.



### Speaker Conn.



**WISTRON**

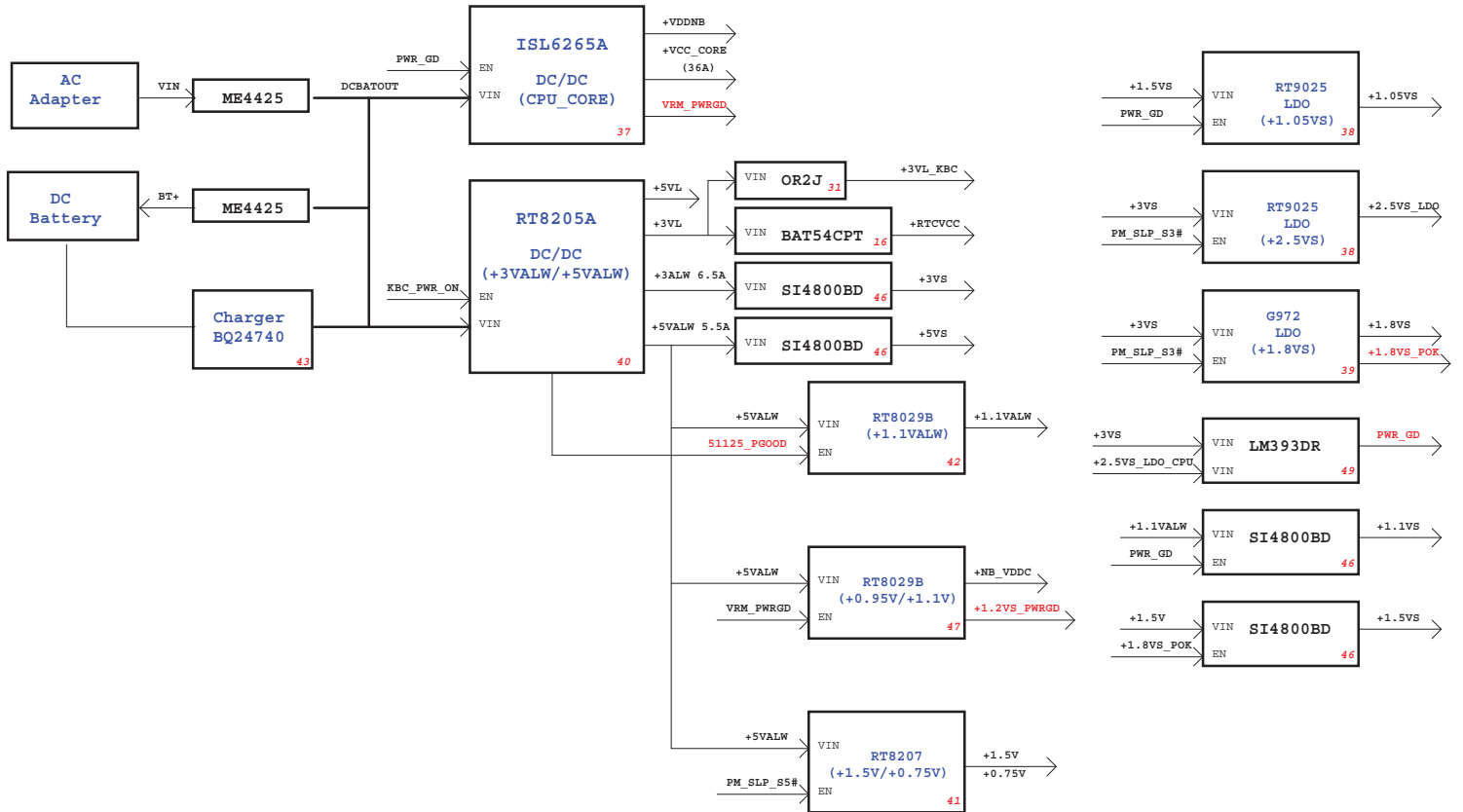
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Hsinchu, Taipei

File: **AUDIO JACK**

Size: A3 Document Number: **PATEK** Rev: **-1**

Date: Monday, March 15, 2010 Sheet: 35 of 50

# Patek UMA Power Block Diagram



<Core Design>

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Hsichih, Taipei

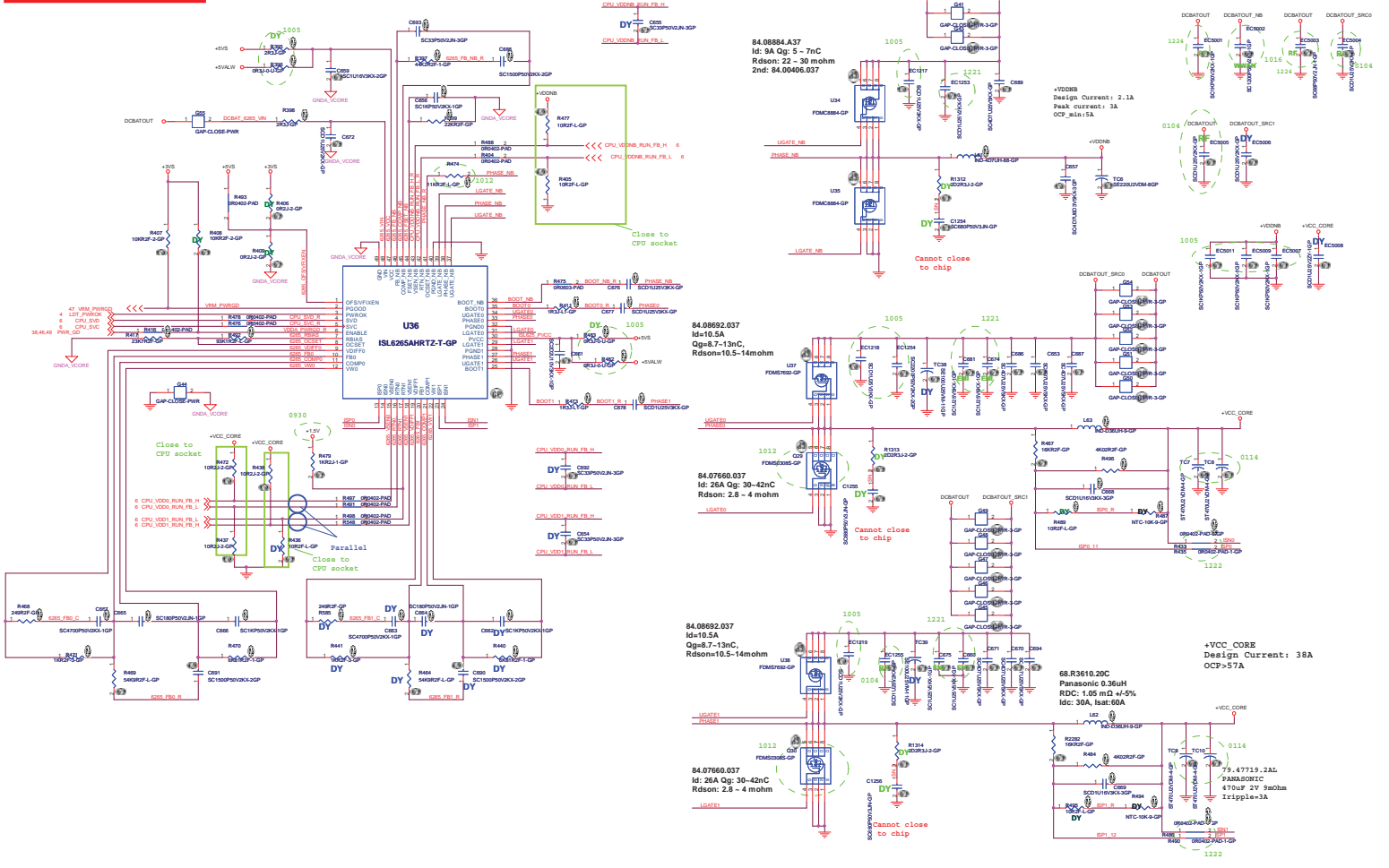
**Power Block Diagram**

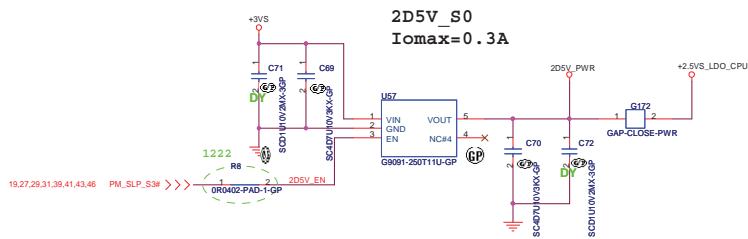
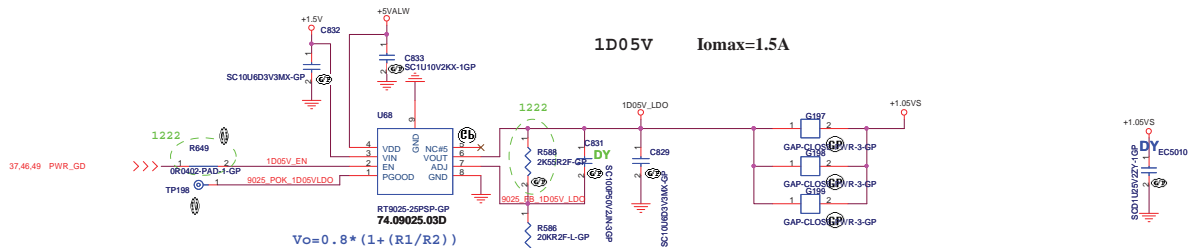
Title

Size A3 Document Number **PATEK** Rev -1

Date: Thursday, January 21, 2010 Sheet 38 of 50

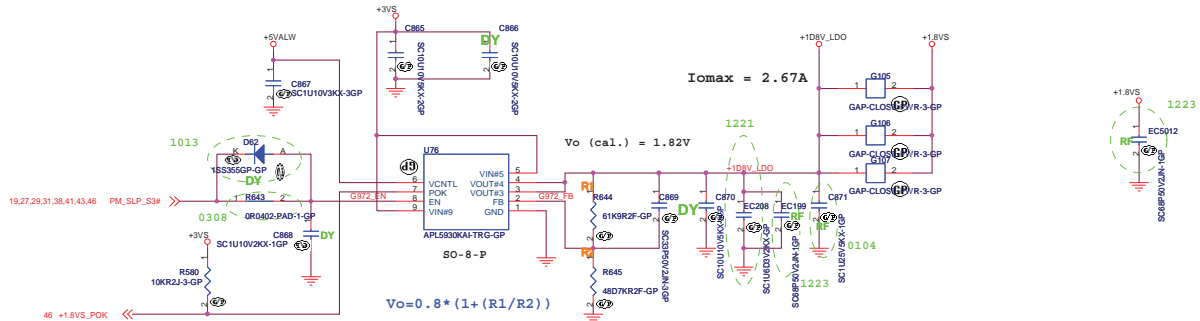
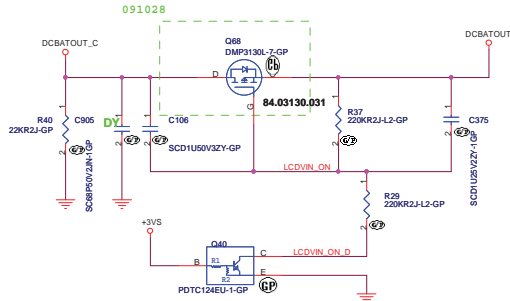
**SSID = CPU.Regulator**





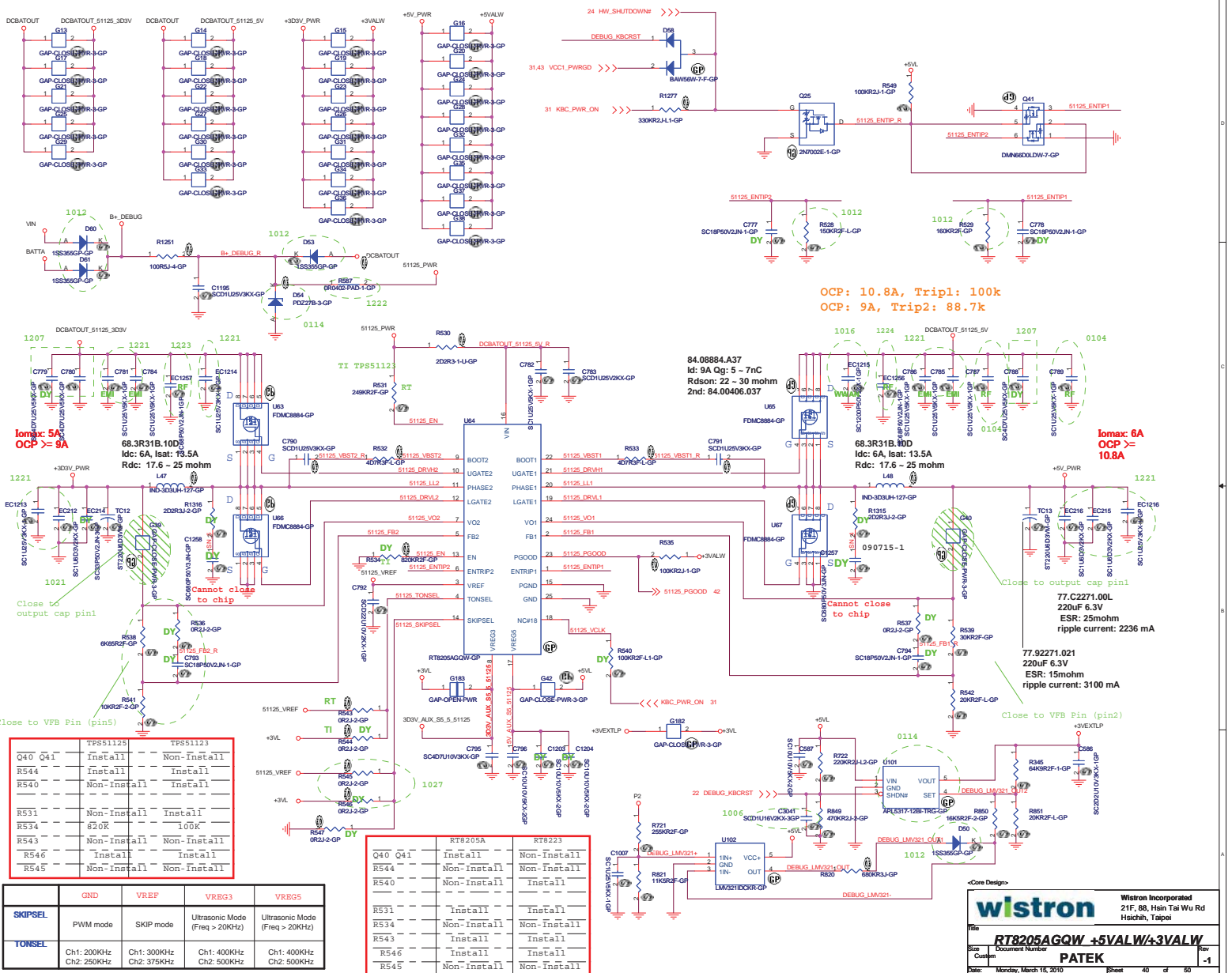
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		Wistron Incorporated 21F, 88, Hsin Tai Wu Rd Hsichih, Taipei	
		Title <b>RT8209B +1.05VS / +2.5VS</b>	Document Number <b>PATEK</b>
Date: Monday, March 16, 2010	Sheet 38	of 50	



<Core Design>

		Wistron Incorporated 21F, 88, Hsin Tai Wu Rd Hsichih, Taipei	
		Title <b>G972 +1.8VS</b>	Document Number <b>PATEK</b>
Date Monday, March 15, 2010	Sheet 38	of 50	



Imax 5A  
OCP > 8A

OCP: 10.8A, Trip1: 100k  
OCP: 9A, Trip2: 88.7k

Imax 6A  
OCP > 10.8A

	TP551123	TP551123
Q40 Q41	Install	Non-Install
R544	Install	Install
R540	Non-Install	Install
R531	Non-Install	Install
R534	620K	105K
R543	Non-Install	Non-Install
R546	Install	Install
R545	Non-Install	Non-Install

	RT8205A	RT8223
Q40 Q41	Install	Non-Install
R544	Non-Install	Non-Install
R540	Non-Install	Install
R531	Install	Install
R534	Non-Install	Non-Install
R543	Install	Install
R546	Install	Install
R545	Non-Install	Non-Install

	GNID	VREFP	VREG3	VREG5
SKIPSEL	PWM mode	SKIP mode	Ultrasonic Mode (Freq > 20KHz)	Ultrasonic Mode (Freq > 20KHz)
TONSEL	Ch1: 200KHz Ch2: 250KHz	Ch1: 300KHz Ch2: 375KHz	Ch1: 400KHz Ch2: 500KHz	Ch1: 400KHz Ch2: 500KHz

**wlstron**

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File: **RT8205AGQW +5VALW+3VALW**

Rev: **1**

Docu. Number: **PATEK**

Date: Monday, March 18, 2010 Sheet 40 of 50

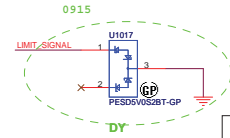
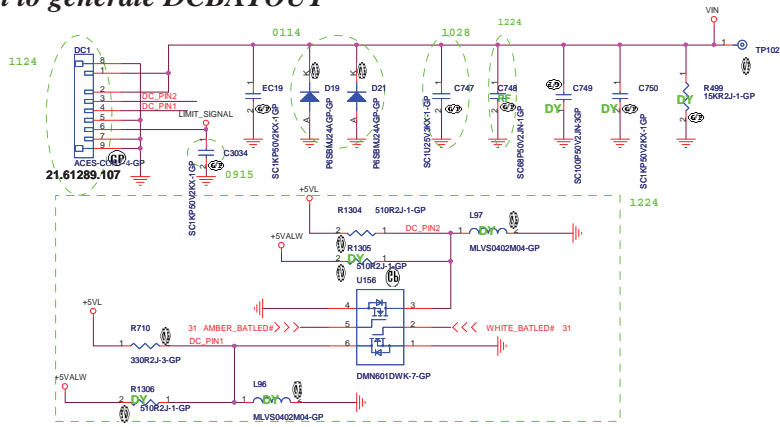








# Adaptor in to generate DCBATOUT

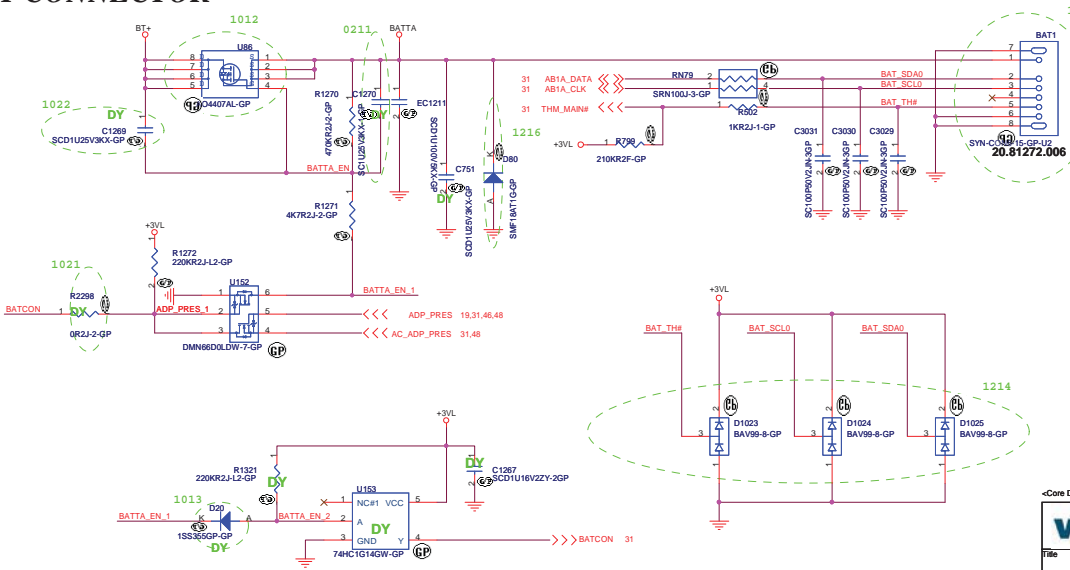


	AMBER ON	WHITE ON	ALL OFF
AMBER	-	+	-
WHITE	+	-	-

White LED:  
 PIN1 (+)  
 PIN2 (-)  
 Amber LED:  
 PIN1 (-)  
 PIN2 (+)

- VIN 1 AFTP188 AFTE14P-GP
- VIN 1 AFTP189 AFTE14P-GP
- VIN 1 AFTP190 AFTE14P-GP
- LIMIT\_SIGNAL 1 AFTP191 AFTE14P-GP
- DC\_PIN2 1 AFTP192 AFTE14P-GP
- DC\_PIN1 1 AFTP193 AFTE14P-GP
- GND 1 AFTP194 AFTE14P-GP
- GND 1 AFTP195 AFTE14P-GP

# BATTERY CONNECTOR



- AFTP14P-GP AFTP205 1 BATT+
- AFTP14P-GP AFTP180 1 BATT+
- AFTP14P-GP AFTP181 1 BAT\_SDA0
- AFTP14P-GP AFTP182 1 BAT\_SCL0
- AFTP14P-GP AFTP183 1 BAT\_TH#
- AFTP14P-GP AFTP184 1 GND
- AFTP14P-GP AFTP185 1 GND
- AFTP14P-GP AFTP186 1 GND
- AFTP14P-GP AFTP187 1 GND

<Core Design>

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 Hsichih, Taipei

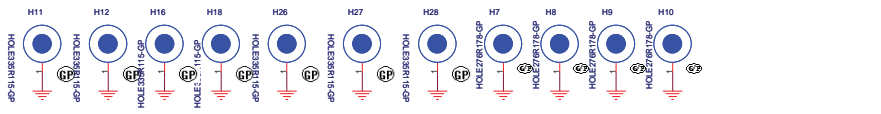
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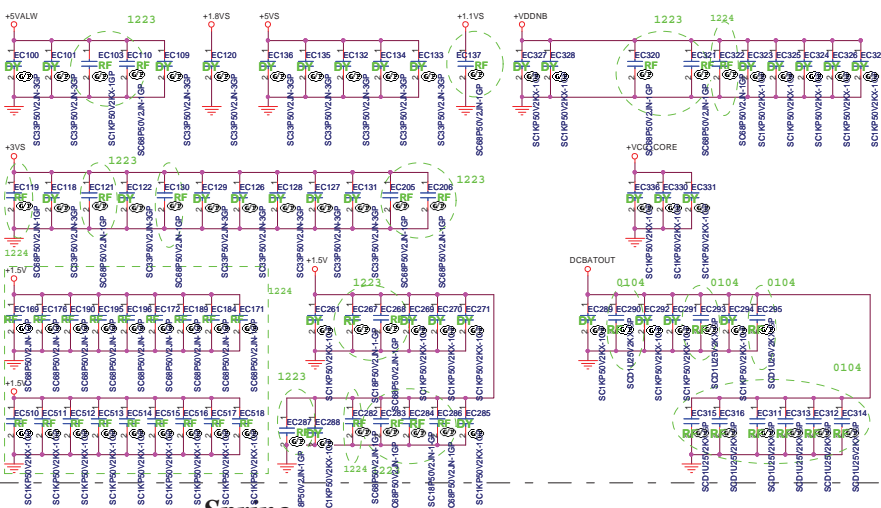
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 Date: Monday, March 15, 2010 Sheet 44 of 50

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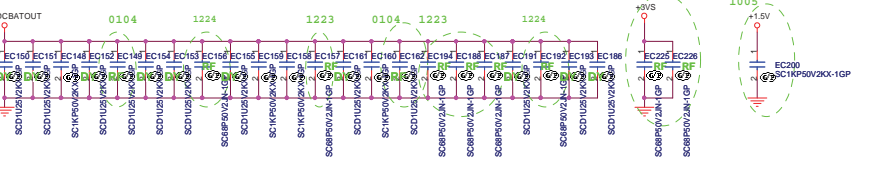
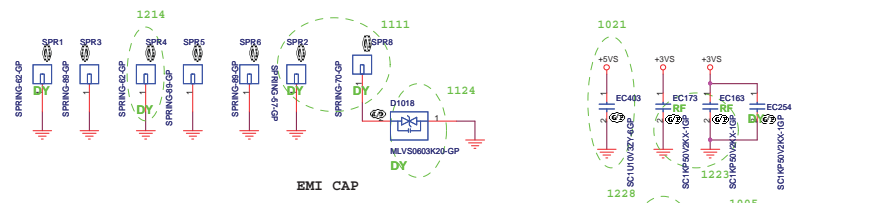
# HOLE



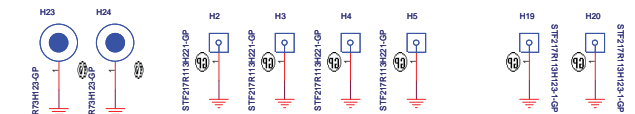
Bottom Side for RF



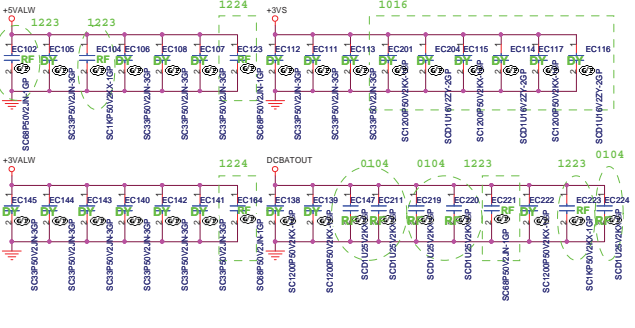
# Spring



# Stand Off

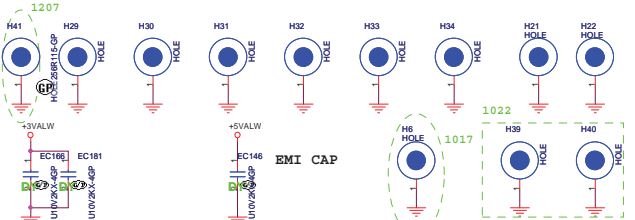


Top Side for RF



# Ground PAD

P/N: ZZ.0HOLE.XXX

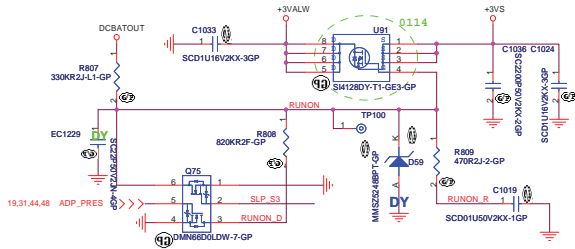


•Core Design

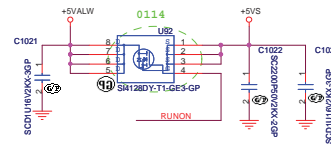
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Hsinchu, Taipei

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Size	Document Number	Rev
A3	<b>PATEK</b>	-1
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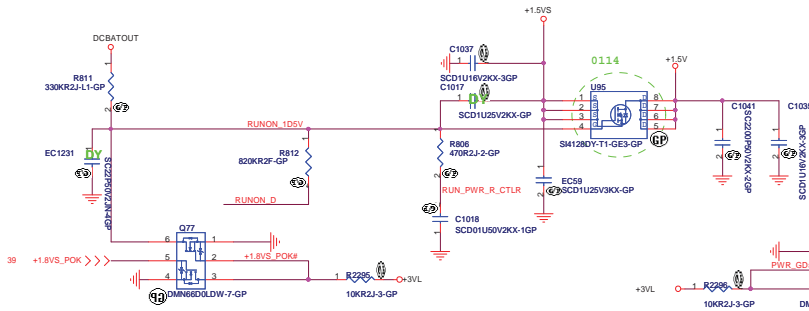
### +3VALW to +3VS Transfer



### +5VALW to +5VS Transfer



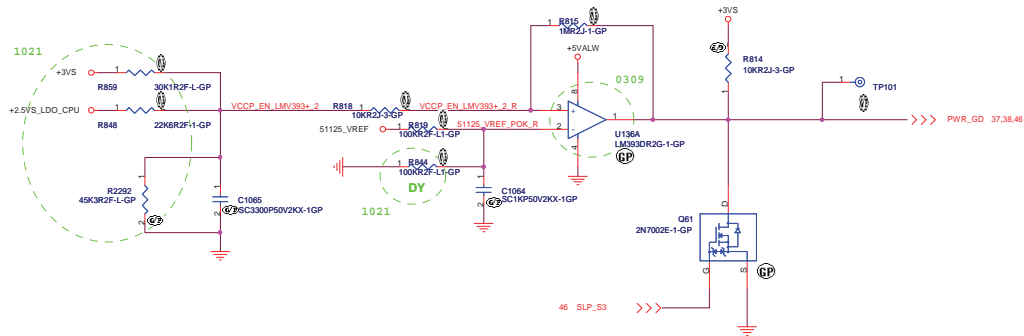
### +1.5V to +1.5VS Transfer











<Core Design>

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		<b>POK CKT</b>	
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# Mini-Card--WWAN Full minicard

AFTE14P-GP AFTP106	1	UM_PWR
AFTE14P-GP AFTP106	2	UM_DATA
AFTE14P-GP AFTP109	3	UM_CLK
AFTE14P-GP AFTP110	4	UM_RST
AFTE14P-GP AFTP111	5	UM_VPP
AFTE14P-GP AFTP112	6	M_WXMIT_OFF#
AFTE14P-GP AFTP125	7	WWAN_LED# C
AFTE14P-GP AFTP126	8	WWAN_DET#
AFTE14P-GP AFTP127	9	USB20_N7
AFTE14P-GP AFTP128	10	USB20_P7
AFTE14P-GP AFTP129	11	+3VS_WWAN
AFTE14P-GP AFTP142	12	+3VS_WWAN
AFTE14P-GP AFTP143	13	+3VS_WWAN
AFTE14P-GP AFTP144	14	+3VS_WWAN
AFTE14P-GP AFTP145	15	+3VS_WWAN
AFTE14P-GP AFTP208	16	GND
AFTE14P-GP AFTP209	17	GND
AFTE14P-GP AFTP210	18	GND

