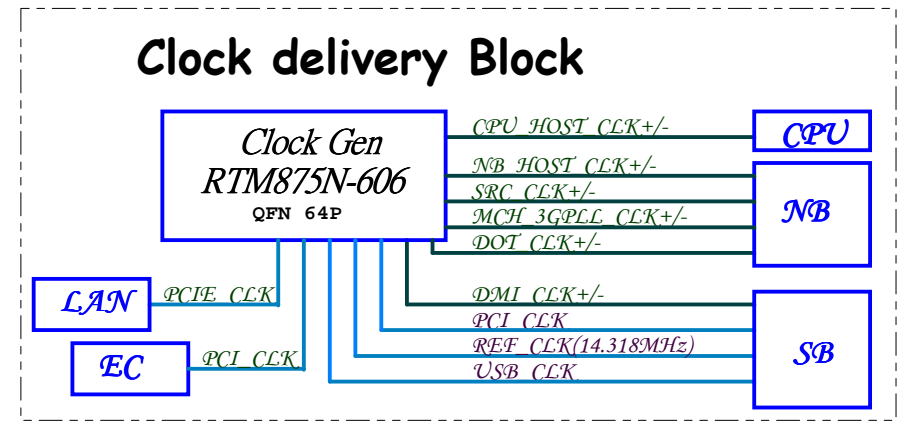
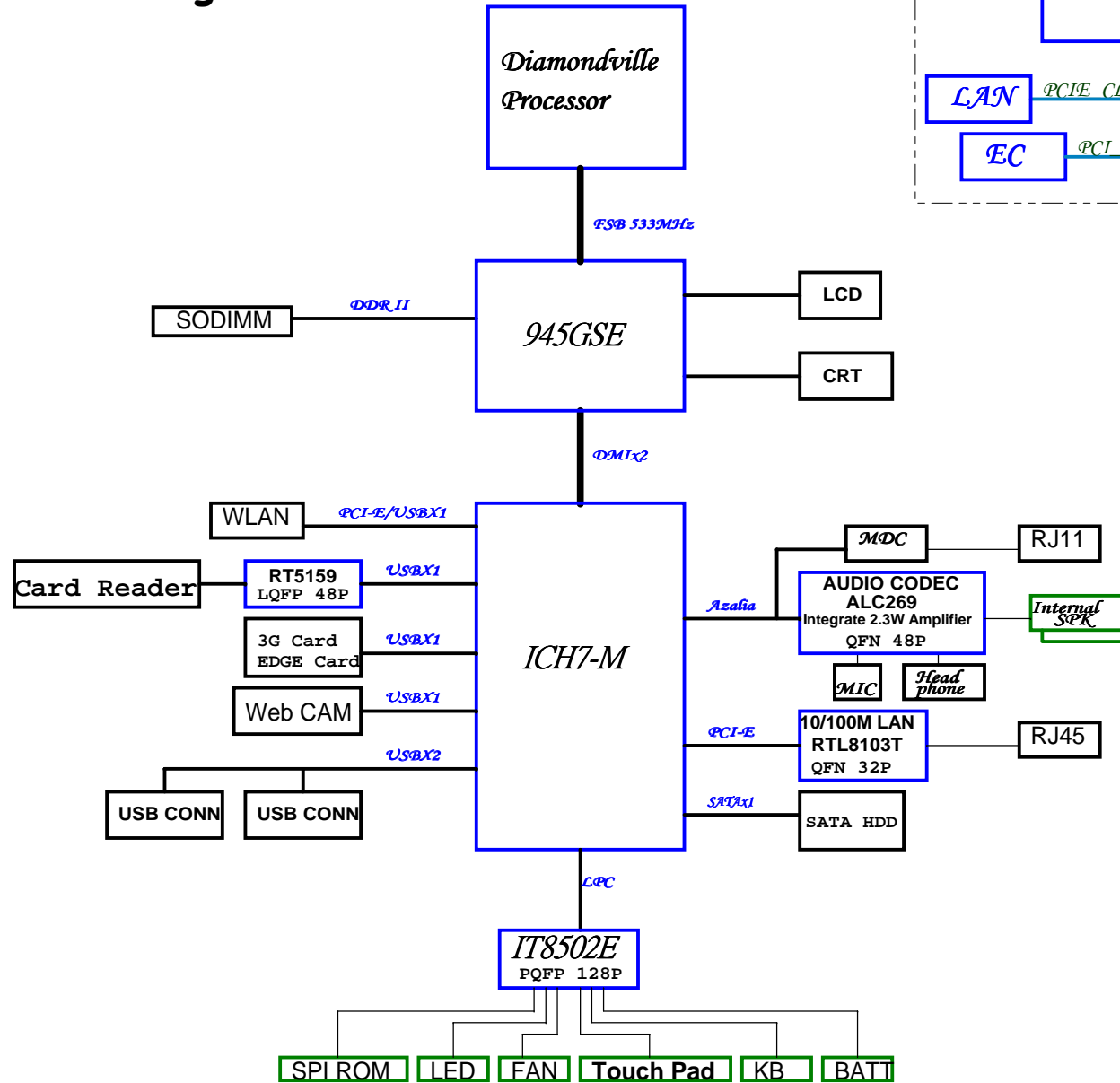
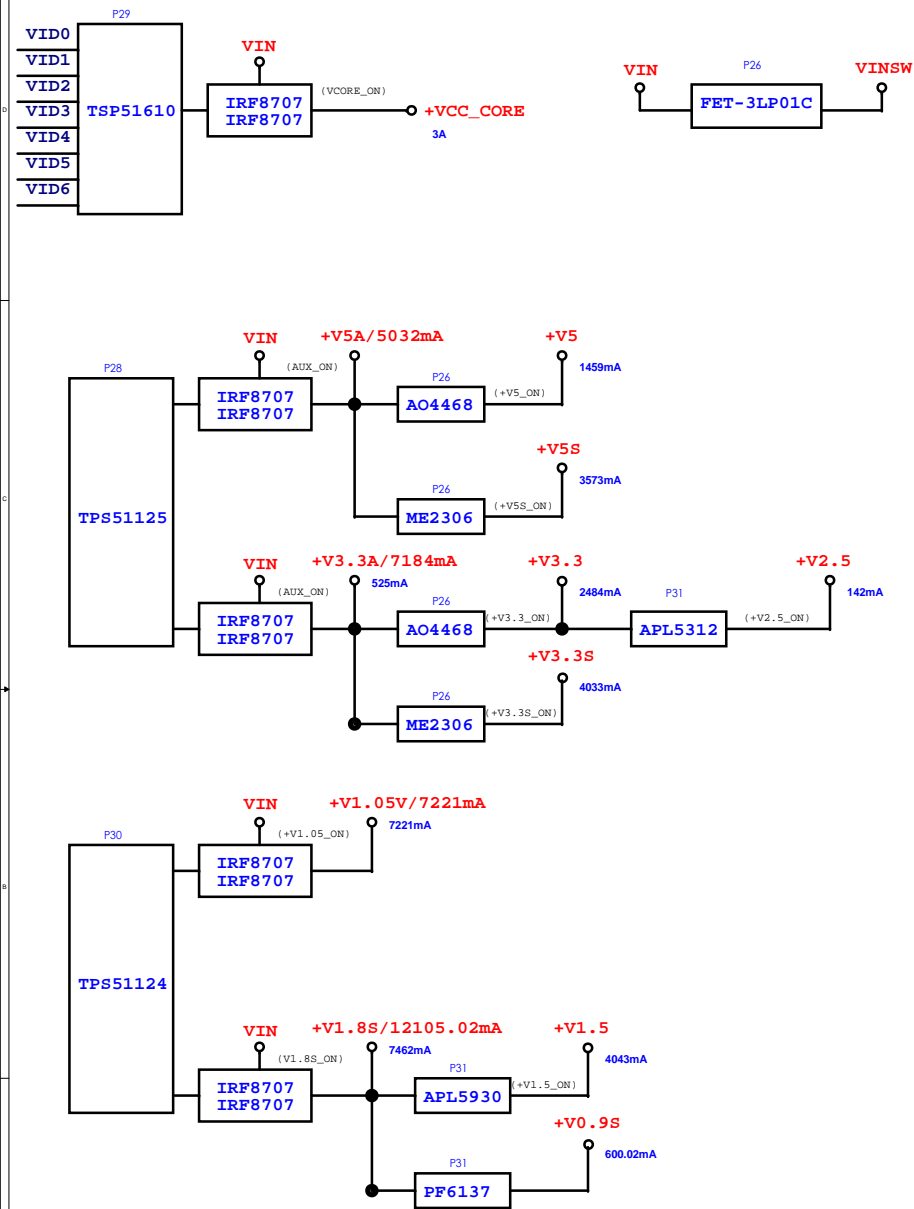




# V10II1 System Block Diagram



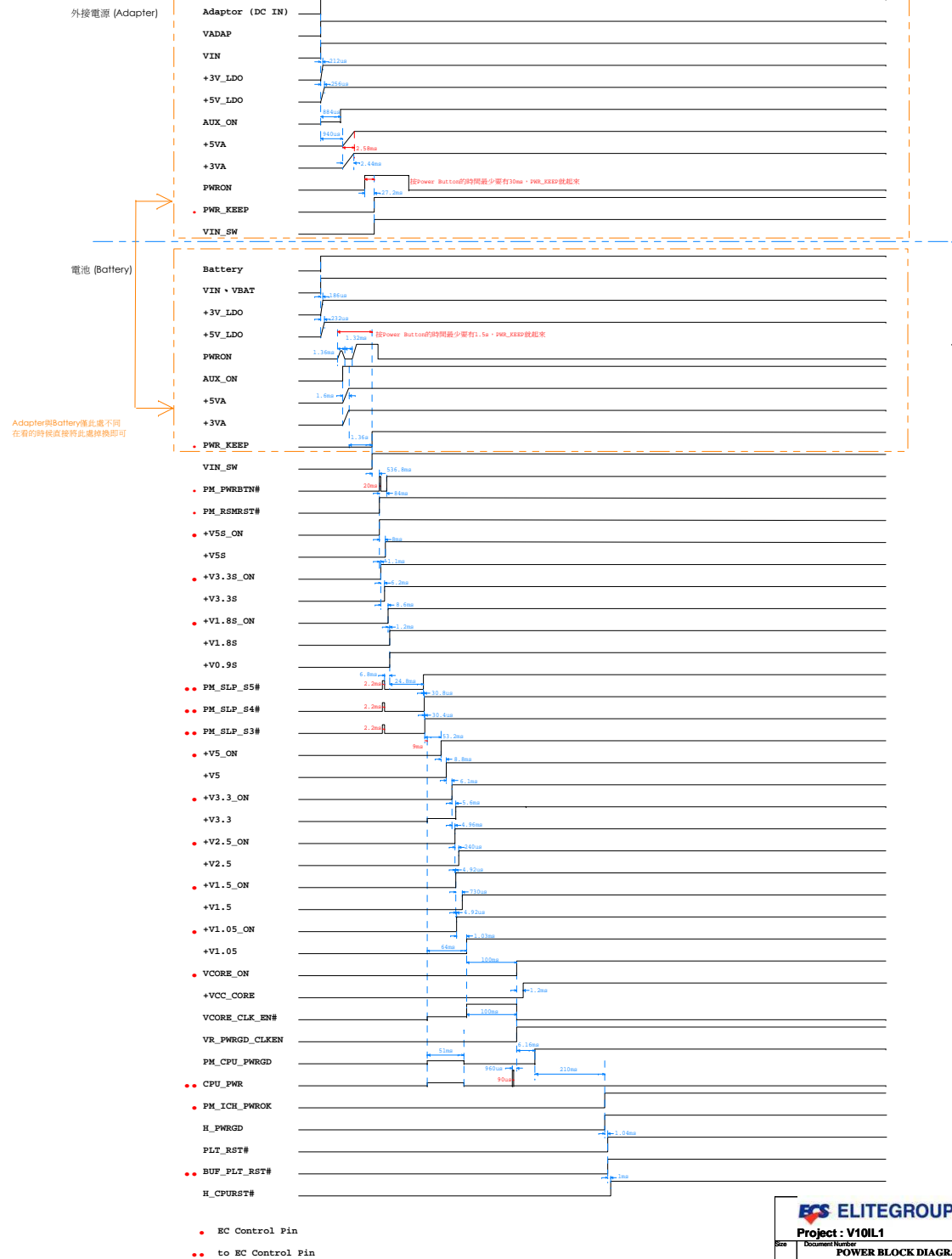
# POWER BLOCK DIAGRAM



V10ILX M/B Power Rail State :

	+*V_LDO	+*VA	+*VS	+*V	CLK
AC/DC S0/MoEf (Full On)	ON	ON	ON	ON	ON
AC/DC S3/MoEf (STR)	ON	ON	ON	OFF	Only MCH BCLK
AC/DC S4/MoEf (STD)	ON	ON	OFF	OFF	OFF
AC S5/MoEf (Soft Off)	ON	ON	OFF	OFF	OFF
DC S5/MoEf (Soft Off)	ON	OFF	OFF	OFF	OFF

# POWER Sequence



ITE8502E GPIO	
GPA0	BTL_BEEP
GPA1	EC_BL_PWM
GPA2	NC
GPA3	3G_EC
GPA4	CHG_R_LED#
GPA5	CHG_G_LED#
GPA6	NC
GPA7	NC
GPB0	NC
GPB1	SMB_CLK_GEN
GPB2	SMB_DATA_GEN
GPB3	SMB_CLK_BAT#R
GPB4	SMB_DATA_BAT
GPB5	H_A20GATE
GPB6	H_RCIN#
GPB7	PWR_KEEP
GPC0	NC
GPC1	NC
GPC2	NC
GPC3	PWR_LED
GPC4	NC
GPC5	+V2.5_ON
GPC6	NC
GPC7	BT_EN#
GPD0	AC_IN
GPD1	WEBCAM_EN
GPD2	PLT_RST#_EC
GPD3	EC_SCI#
GPD4	EC_EXTSMI#
GPD5	NC
GPD6	Low Voltage#
GPD7	PM_PWRBTN#
GPE0	BKL_EC
GPE1	MUTE_AMP#
GPE2	PM_RSMRST#
GPE3	PM_SYSRST#
GPE4	PWR_SW
GPE5	PM_SLP_S3#
GPE6	PM_SLP_S4#
GPE7	LID#
GPF0	RF_LED
GPF1	RF_OFF#
GPF2	NC
GPF3	NC
GPF4	PS2_CLK_TP
GPF5	PS2_DATA_TP
GPF6	NC
GPF7	NC
GPG0	3G_ONECH
GPG1	+V1.8S_ON
GPG2	PLFRAME#
GPG6	+V1.5_ON
GPH0	PM_ICH_PWR0K
GPH1	VCORE_ON
GPH2	+V5_ON
GPH3	+V3.3_ON
GPH4	+V3.3S_ON
GPH5	+V5S_ON
GPH6	+V1.05_ON

3/23名稱修正·3G\_EC#改為3G\_EC

02/13 更換GPIO  
GPC4 01/19 因應G-SENEOR所新增  
02/13 更換GPIO  
04/09 B Phase已無使用·刪除

1/19 +V5S\_ON移除不用  
1/20 pin16因應BLUETOOTH所新增

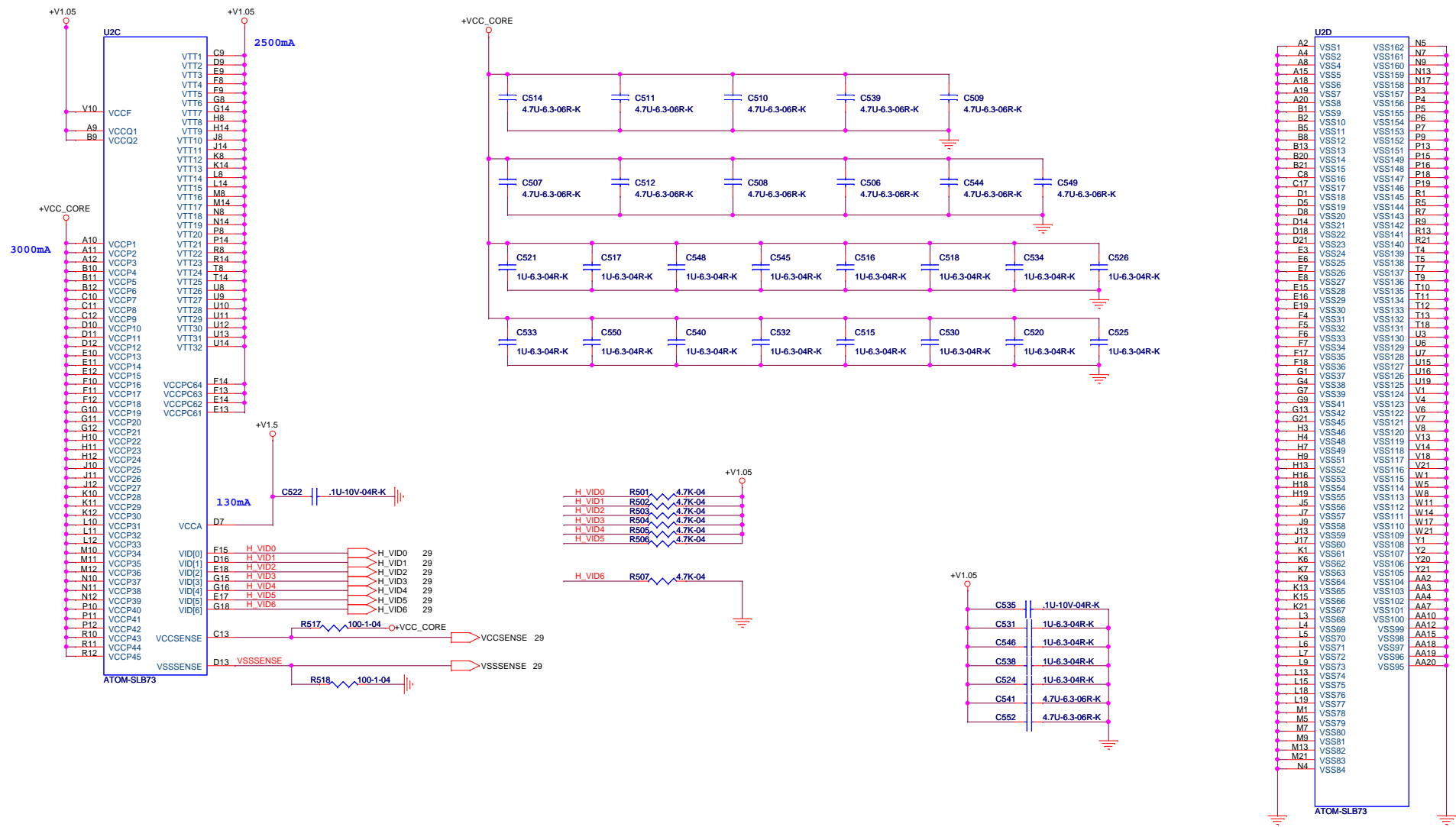
02/06 新增Low Voltage#

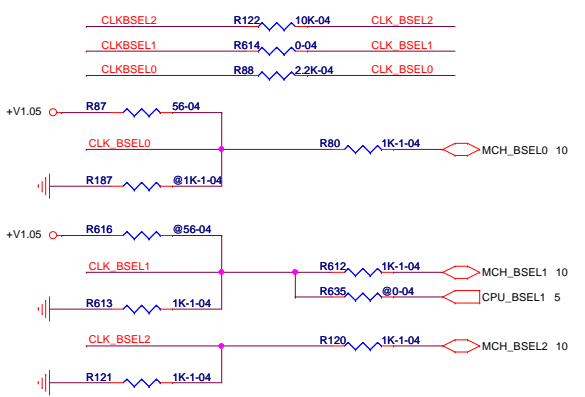
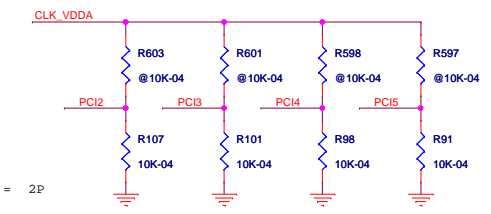
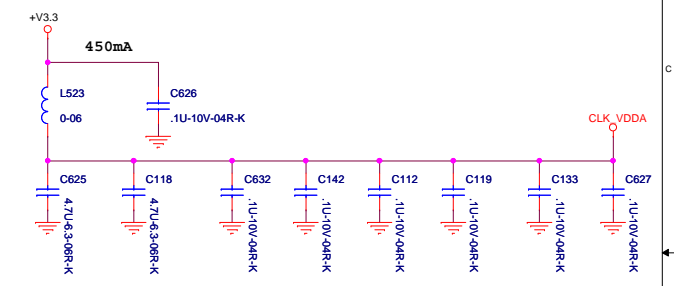
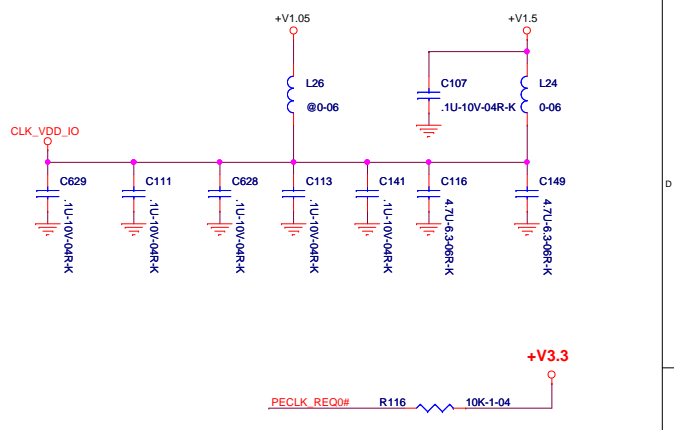
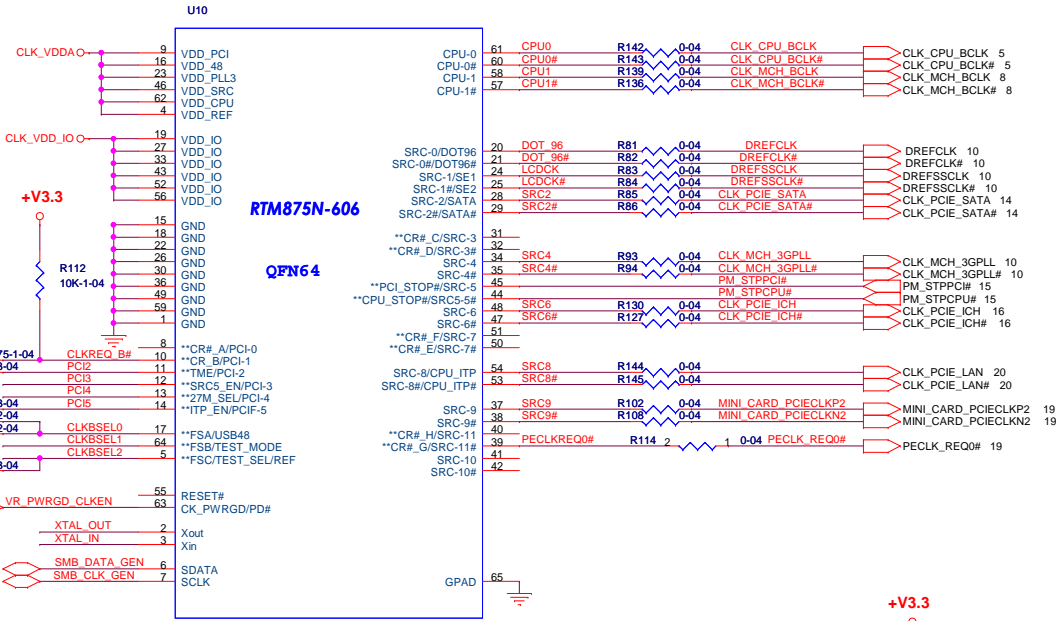
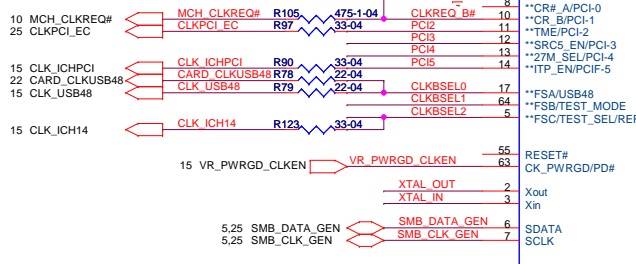
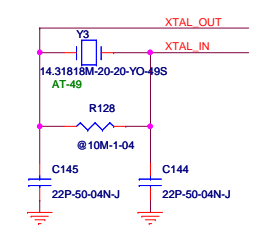
1/17 更名為3G\_ONECH

1/17新增

ITE8502E GPIO	
GPIO0	BATT_TEMP
GPI1	ADAPTOR_I
GPI2	BAT_I
GPI3	BAT_V
GPI4	SAFTY_PROTECT
GPI5	EC_PROCHOT#
GPI6	CPU_PWR
GPI7	PM_SLP_S5#
GPJ0	Fast-charge-EN
GPJ1	CHG_I
GPJ2	FAN_CTRL0
GPJ3	SENBAT_V
GPJ4	CHG_V
GPJ5	CHG_ON



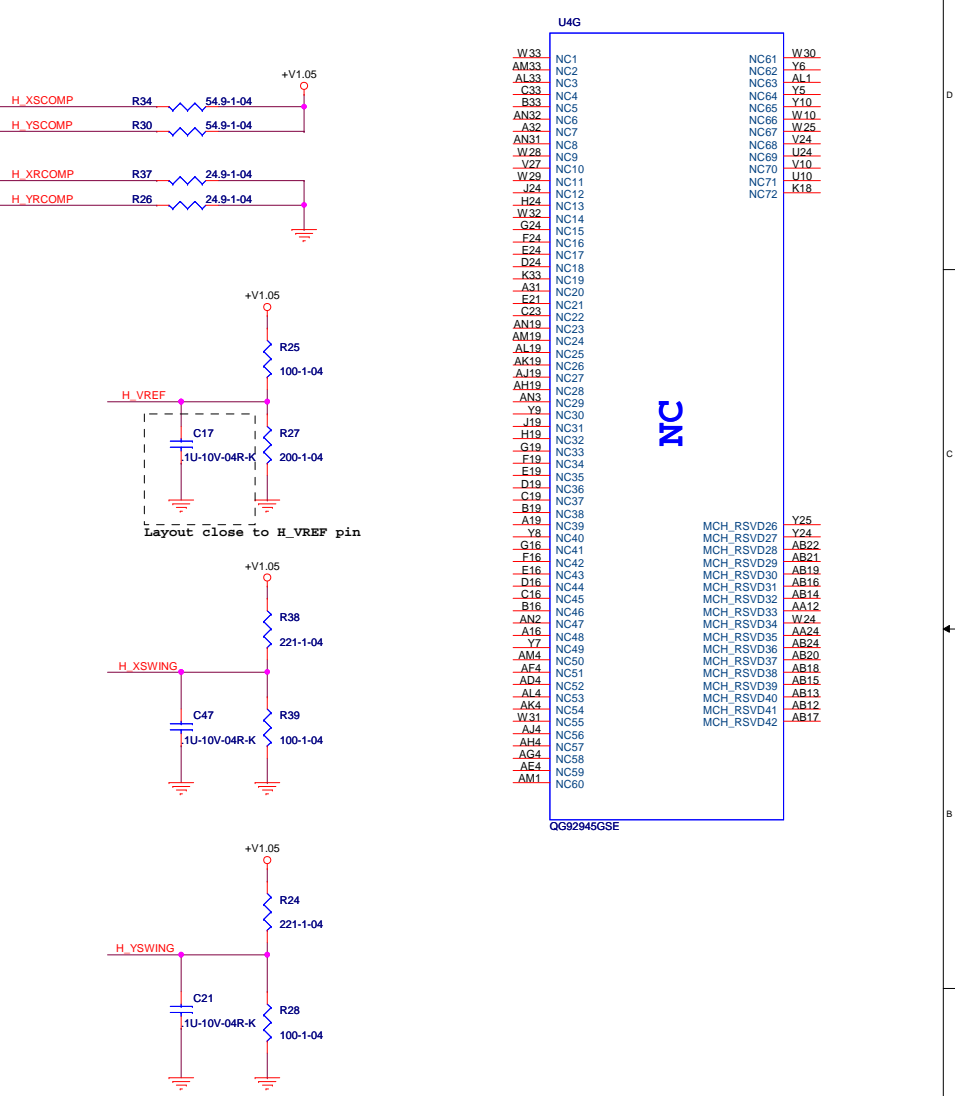
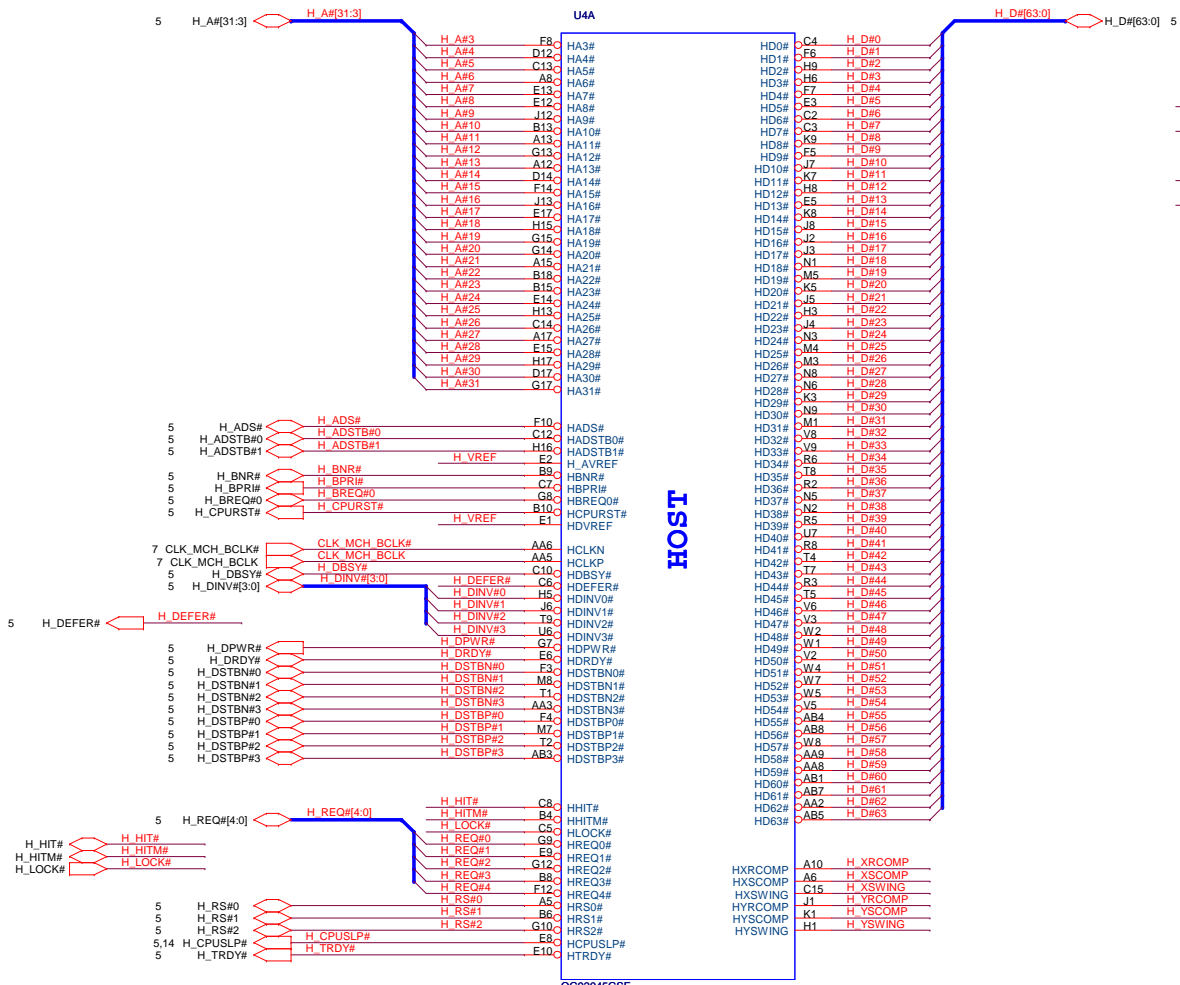




	PULL HIGH	PULL LOW
PCI-2	NO OVERCLOCKING	NORMAL RUN
PCI-3	Pin 45/44 is SRC5	Pin 20/21 is SRC-0 Pin 24/25 is 27/27SS
PCI-4	Pin 20/21 is SRC-0 Pin 24/25 is 27/27SS	Pin 20/21 is DOT96 Pin 24/25 is SRC-1
PCI-5	Pin 54/53 is CUIPTP	Pin 54/53 is SRC8

BSEL2	BSEL1	BSEL0	CPU
FSC	FSB	FSA	CPU
0	0	0	266
0	0	1	133
0	1	0	200
0	1	1	166
1	0	0	333
1	0	1	100
1	1	0	400
1	1	1	200

**FCS ELITEGROUP**  
 Project : V10L1  
 Size Document Number Rev B  
 SCHEMATICS Clock Generator RTM875N-606  
 Date: Tuesday, May 19, 2009 Sheet 7 of 32





12 M\_A\_DQ[63:0]

M_A DQ[63:0]	U4C	SA	SA
M_A_DQ0	AC31	SA_DQ0	SA_DQ0
M_A_DQ1	AB28	SA_DQ1	SA_DQ1
M_A_DQ2	AE23	SA_DQ2	SA_DQ2
M_A_DQ3	AF32	SA_DQ3	SA_DQ3
M_A_DQ4	AC33	SA_DQ4	SA_DQ4
M_A_DQ5	AB32	SA_DQ5	SA_DQ5
M_A_DQ6	AB31	SA_DQ6	SA_DQ6
M_A_DQ7	AE31	SA_DQ7	SA_DQ7
M_A_DQ8	AH31	SA_DQ8	SA_DQ8
M_A_DQ9	AK31	SA_DQ9	SA_DQ9
M_A_DQ10	AL28	SA_DQ10	SA_DQ10
M_A_DQ11	AK27	SA_DQ11	SA_DQ11
M_A_DQ12	AH30	SA_DQ12	SA_DQ12
M_A_DQ13	AL32	SA_DQ13	SA_DQ13
M_A_DQ14	AJ28	SA_DQ14	SA_DQ14
M_A_DQ15	AJ27	SA_DQ15	SA_DQ15
M_A_DQ16	AH32	SA_DQ16	SA_DQ16
M_A_DQ17	AF31	SA_DQ17	SA_DQ17
M_A_DQ18	AH27	SA_DQ18	SA_DQ18
M_A_DQ19	AF28	SA_DQ19	SA_DQ19
M_A_DQ20	AL32	SA_DQ20	SA_DQ20
M_A_DQ21	AG31	SA_DQ21	SA_DQ21
M_A_DQ22	AG28	SA_DQ22	SA_DQ22
M_A_DQ23	AJ27	SA_DQ23	SA_DQ23
M_A_DQ24	AN27	SA_DQ24	SA_DQ24
M_A_DQ25	AM26	SA_DQ25	SA_DQ25
M_A_DQ26	AJ26	SA_DQ26	SA_DQ26
M_A_DQ27	AJ25	SA_DQ27	SA_DQ27
M_A_DQ28	AL27	SA_DQ28	SA_DQ28
M_A_DQ29	AN26	SA_DQ29	SA_DQ29
M_A_DQ30	AH25	SA_DQ30	SA_DQ30
M_A_DQ31	AG26	SA_DQ31	SA_DQ31
M_A_DQ32	AM12	SA_DQ32	SA_DQ32
M_A_DQ33	AL11	SA_DQ33	SA_DQ33
M_A_DQ34	AH9	SA_DQ34	SA_DQ34
M_A_DQ35	AK9	SA_DQ35	SA_DQ35
M_A_DQ36	AM11	SA_DQ36	SA_DQ36
M_A_DQ37	AK11	SA_DQ37	SA_DQ37
M_A_DQ38	AM8	SA_DQ38	SA_DQ38
M_A_DQ39	AK8	SA_DQ39	SA_DQ39
M_A_DQ40	AG9	SA_DQ40	SA_DQ40
M_A_DQ41	AF8	SA_DQ41	SA_DQ41
M_A_DQ42	AL7	SA_DQ42	SA_DQ42
M_A_DQ43	AK6	SA_DQ43	SA_DQ43
M_A_DQ44	AF7	SA_DQ44	SA_DQ44
M_A_DQ45	AG11	SA_DQ45	SA_DQ45
M_A_DQ46	AJ6	SA_DQ46	SA_DQ46
M_A_DQ47	AH6	SA_DQ47	SA_DQ47
M_A_DQ48	AN6	SA_DQ48	SA_DQ48
M_A_DQ49	AM6	SA_DQ49	SA_DQ49
M_A_DQ50	AK3	SA_DQ50	SA_DQ50
M_A_DQ51	AL2	SA_DQ51	SA_DQ51
M_A_DQ52	AM5	SA_DQ52	SA_DQ52
M_A_DQ53	AL5	SA_DQ53	SA_DQ53
M_A_DQ54	AJ3	SA_DQ54	SA_DQ54
M_A_DQ55	AJ2	SA_DQ55	SA_DQ55
M_A_DQ56	AG2	SA_DQ56	SA_DQ56
M_A_DQ57	AF3	SA_DQ57	SA_DQ57
M_A_DQ58	AE7	SA_DQ58	SA_DQ58
M_A_DQ59	AF6	SA_DQ59	SA_DQ59
M_A_DQ60	AH6	SA_DQ60	SA_DQ60
M_A_DQ61	AG3	SA_DQ61	SA_DQ61
M_A_DQ62	AG5	SA_DQ62	SA_DQ62
M_A_DQ63	AF5	SA_DQ63	SA_DQ63

AG19  
AG21  
AG20

SB\_CAS#  
SB\_RAS#  
SB\_WE#

DDR2 SYSTEM MEMORY

TP27  
TP28

QG92946GSE

SA\_BS\_0  
SA\_BS\_1  
SA\_BS\_2

AK12	M_A_BS#0
AH11	M_A_BS#1
AG17	M_A_BS#2
AB30	M_A_DM0
AL31	M_A_DM1
AF30	M_A_DM2
AK26	M_A_DM3
AL9	M_A_DM4
AG7	M_A_DM5
AK5	M_A_DM6
AH3	M_A_DM7

M\_A\_BS[2:0] 12

M\_A\_DM[7:0] 12

SA\_DQS0  
SA\_DQS1  
SA\_DQS2  
SA\_DQS3  
SA\_DQS4  
SA\_DQS5  
SA\_DQS6  
SA\_DQS7

AC28	M_A_DQS0
AJ30	M_A_DQS1
AK33	M_A_DQS2
AL26	M_A_DQS3
AN9	M_A_DQS4
AH8	M_A_DQS5
AM2	M_A_DQS6
AE3	M_A_DQS7

M\_A\_DQS0 12  
M\_A\_DQS1 12  
M\_A\_DQS2 12  
M\_A\_DQS3 12  
M\_A\_DQS4 12  
M\_A\_DQS5 12  
M\_A\_DQS6 12  
M\_A\_DQS7 12

SA\_DQS0#  
SA\_DQS1#  
SA\_DQS2#  
SA\_DQS3#  
SA\_DQS4#  
SA\_DQS5#  
SA\_DQS6#  
SA\_DQS7#

AC29	M_A_DQS0#
AJ30	M_A_DQS1#
AK33	M_A_DQS2#
AL26	M_A_DQS3#
AN9	M_A_DQS4#
AH8	M_A_DQS5#
AM2	M_A_DQS6#
AE3	M_A_DQS7#

M\_A\_DQS0# 12  
M\_A\_DQS1# 12  
M\_A\_DQS2# 12  
M\_A\_DQS3# 12  
M\_A\_DQS4# 12  
M\_A\_DQS5# 12  
M\_A\_DQS6# 12  
M\_A\_DQS7# 12

SA\_MA0  
SA\_MA1  
SA\_MA2  
SA\_MA3  
SA\_MA4  
SA\_MA5  
SA\_MA6  
SA\_MA7  
SA\_MA8  
SA\_MA9  
SA\_MA10  
SA\_MA11  
SA\_MA12  
SA\_MA13

AJ15	M_A_A0
AM17	M_A_A1
AM15	M_A_A2
AH15	M_A_A3
AK15	M_A_A4
AN15	M_A_A5
AH18	M_A_A6
AF19	M_A_A7
AN17	M_A_A8
AL17	M_A_A9
AG16	M_A_A10
AL18	M_A_A11
AG18	M_A_A12
AL14	M_A_A13

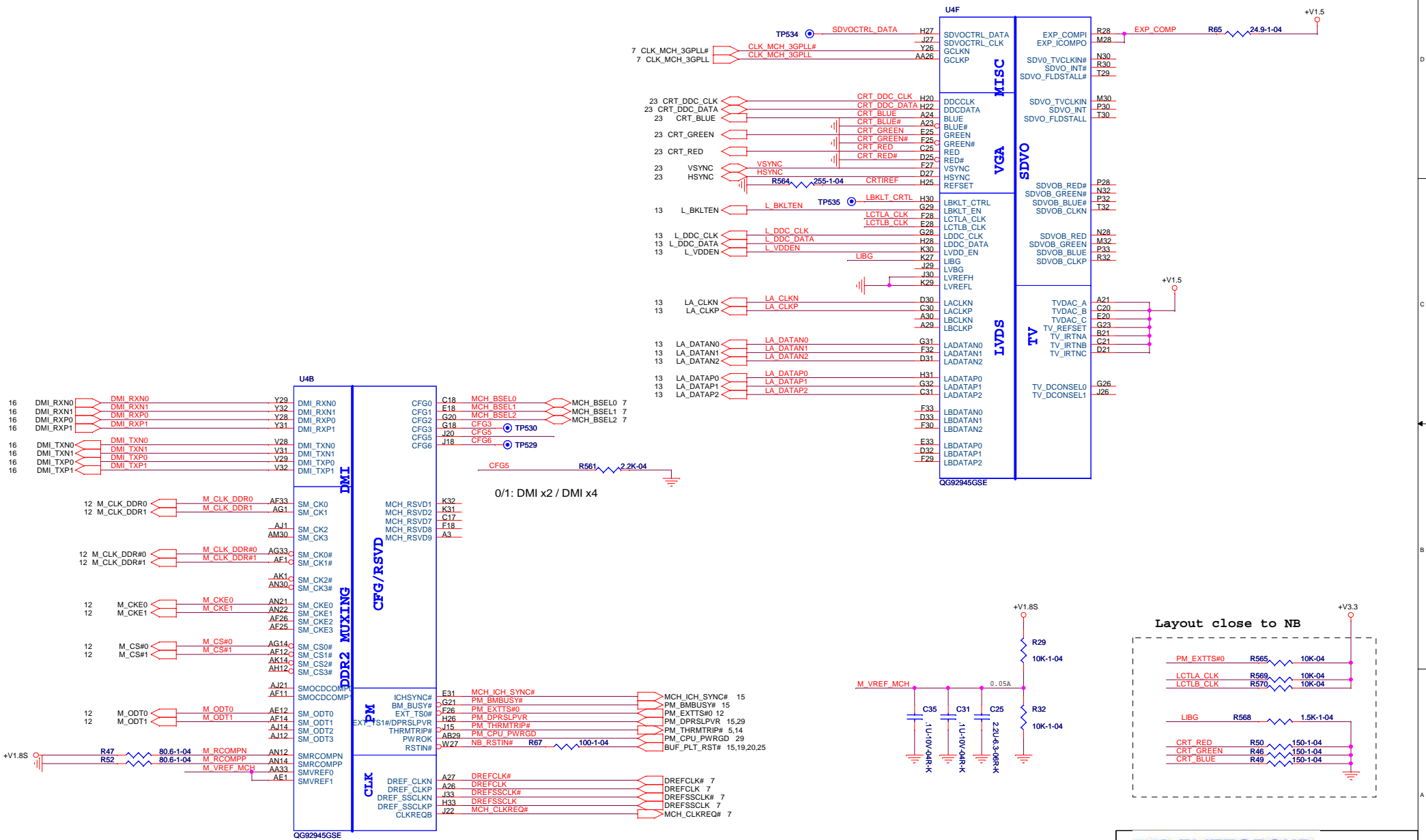
M\_A\_A[13:0] 12

M\_A\_CAS# 12  
M\_A\_RAS# 12  
M\_A\_WE# 12

+V1.05 2940mA

U4H 1250mA +V1.5

T25	VCC_NCTF1	AD25	
R25	VCC_NCTF2	AC25	
P25	VCC_NCTF3	AB25	
N25	VCC_NCTF4	AD24	
M25	VCC_NCTF5	AC24	
P24	VCC_NCTF6	AD22	
N24	VCC_NCTF7	AD21	
M24	VCC_NCTF8	AD20	
Y22	VCC_NCTF9	AD19	
W22	VCC_NCTF10	AD18	
V22	VCC_NCTF11	AD17	
U22	VCC_NCTF12	AD16	
R22	VCC_NCTF13	AD15	
P22	VCC_NCTF14	AD14	
N22	VCC_NCTF15	K14	
M22	VCC_NCTF16	AD13	
Y21	VCC_NCTF17	Y13	
W21	VCC_NCTF18	V13	
V21	VCC_NCTF19	U13	
U21	VCC_NCTF20	R13	
T21	VCC_NCTF21	T13	
R21	VCC_NCTF22	VCC_AUX_NCTF22	P13
P21	VCC_NCTF23	VCC_AUX_NCTF23	N13
N21	VCC_NCTF24	VCC_AUX_NCTF24	M13
M21	VCC_NCTF25	VCC_AUX_NCTF25	AD12
Y20	VCC_NCTF26	VCC_AUX_NCTF26	Y12
W20	VCC_NCTF27	VCC_AUX_NCTF27	W12
V20	VCC_NCTF28	VCC_AUX_NCTF28	V12
U20	VCC_NCTF29	VCC_AUX_NCTF29	U12
T20	VCC_NCTF30	VCC_AUX_NCTF30	T12
R20	VCC_NCTF31	VCC_AUX_NCTF31	R12
P20	VCC_NCTF32	VCC_AUX_NCTF32	P12
N20	VCC_NCTF33	VCC_AUX_NCTF33	N12
M20	VCC_NCTF34	VCC_AUX_NCTF34	M12
Y19	VCC_NCTF35	VCC_AUX_NCTF35	AD11
W19	VCC_NCTF36	VCC_AUX_NCTF36	AD10
V19	VCC_NCTF37	VCC_AUX_NCTF37	K10
U19	VCC_NCTF38	VCC_AUX_NCTF38	AN33
T19	VCC_NCTF39	VSS_NCTF1	AN33
R19	VCC_NCTF40	VSS_NCTF2	AA25
P19	VCC_NCTF41	VSS_NCTF3	V25
N19	VCC_NCTF42	VSS_NCTF4	U25
M19	VCC_NCTF43	VSS_NCTF5	AA22
Y18	VCC_NCTF44	VSS_NCTF6	AA21
W18	VCC_NCTF45	VSS_NCTF7	AA20
V18	VCC_NCTF46	VSS_NCTF8	AA19
U18	VCC_NCTF47	VSS_NCTF9	AA18
T18	VCC_NCTF48	VSS_NCTF10	AA17
R18	VCC_NCTF49	VSS_NCTF11	AA16
P18	VCC_NCTF50	VSS_NCTF12	AA15
N18	VCC_NCTF51	VSS_NCTF13	AA14
M18	VCC_NCTF52	VSS_NCTF14	AA13
Y17	VCC_NCTF53	VSS_NCTF15	A4
W17	VCC_NCTF54	VCC_NCTF54	A33
V17	VCC_NCTF55	VCC_NCTF55	B2
U17	VCC_NCTF56	VCC_NCTF56	AN1
T17	VCC_NCTF57	VCC_NCTF57	C1
R17	VCC_NCTF58	VCC_NCTF58	
P17	VCC_NCTF59	VCC_NCTF59	
N17	VCC_NCTF60	VCC_NCTF60	
M17	VCC_NCTF61	VCC_NCTF61	
Y16	VCC_NCTF62	VCC_NCTF62	
W16	VCC_NCTF63	VCC_NCTF63	
V16	VCC_NCTF64	VCC_NCTF64	
U16	VCC_NCTF65	VCC_NCTF65	
T16	VCC_NCTF66	VCC_NCTF66	
R16	VCC_NCTF67	VCC_NCTF67	
P16	VCC_NCTF68	VCC_NCTF68	
N16	VCC_NCTF69	VCC_NCTF69	
M16	VCC_NCTF70	VCC_NCTF70	
Y15	VCC_NCTF71	VCC_NCTF71	
W15	VCC_NCTF72	VCC_NCTF72	
V15	VCC_NCTF73	VCC_NCTF73	
U15	VCC_NCTF74	VCC_NCTF74	
T15	VCC_NCTF75	VCC_NCTF75	
R15	VCC_NCTF76	VCC_NCTF76	
P15	VCC_NCTF77	VCC_NCTF77	
N15	VCC_NCTF78	VCC_NCTF78	
M15	VCC_NCTF79	VCC_NCTF79	
Y14	VCC_NCTF80	VCC_NCTF80	
W14	VCC_NCTF81	VCC_NCTF81	
V14	VCC_NCTF82	VCC_NCTF82	
U14	VCC_NCTF83	VCC_NCTF83	
T14	VCC_NCTF84	VCC_NCTF84	
R14	VCC_NCTF85	VCC_NCTF85	
P14	VCC_NCTF86	VCC_NCTF86	
N14	VCC_NCTF87	VCC_NCTF87	
M14	VCC_NCTF88	VCC_NCTF88	
Y14	VCC_NCTF89	VCC_NCTF89	
W14	VCC_NCTF90	VCC_NCTF90	
V14	VCC_NCTF91	VCC_NCTF91	
U14	VCC_NCTF92	VCC_NCTF92	
T14	VCC_NCTF93	VCC_NCTF93	
R14	VCC_NCTF94	VCC_NCTF94	
P14	VCC_NCTF95	VCC_NCTF95	
N14	VCC_NCTF96	VCC_NCTF96	
M14	VCC_NCTF97	VCC_NCTF97	
Y14	VCC_NCTF98	VCC_NCTF98	
W14	VCC_NCTF99	VCC_NCTF99	
V14	VCC_NCTF100	VCC_NCTF100	
U14	VCC_NCTF101	VCC_NCTF101	
T14	VCC_NCTF102	VCC_NCTF102	
R14	VCC_NCTF103	VCC_NCTF103	
P14	VCC_NCTF104	VCC_NCTF104	
N14	VCC_NCTF105	VCC_NCTF105	
M14	VCC_NCTF106	VCC_NCTF106	
Y14	VCC_NCTF107	VCC_NCTF107	
W14	VCC_NCTF108	VCC_NCTF108	
V14	VCC_NCTF109	VCC_NCTF109	
U14	VCC_NCTF110	VCC_NCTF110	
T14	VCC_NCTF111	VCC_NCTF111	
R14	VCC_NCTF112	VCC_NCTF112	
P14	VCC_NCTF113	VCC_NCTF113	
N14	VCC_NCTF114	VCC_NCTF114	
M14	VCC_NCTF115	VCC_NCTF115	
Y14	VCC_NCTF116	VCC_NCTF116	
W14	VCC_NCTF117	VCC_NCTF117	
V14	VCC_NCTF118	VCC_NCTF118	
U14	VCC_NCTF119	VCC_NCTF119	
T14	VCC_NCTF120	VCC_NCTF120	
R14	VCC_NCTF121	VCC_NCTF121	
P14	VCC_NCTF122	VCC_NCTF122	
N14	VCC_NCTF123	VCC_NCTF123	
M14	VCC_NCTF124	VCC_NCTF124	
Y14	VCC_NCTF125	VCC_NCTF125	
W14	VCC_NCTF126	VCC_NCTF126	
V14	VCC_NCTF127	VCC_NCTF127	
U14	VCC_NCTF128	VCC_NCTF128	
T14	VCC_NCTF129	VCC_NCTF129	
R14	VCC_NCTF130	VCC_NCTF130	
P14	VCC_NCTF131	VCC_NCTF131	
N14	VCC_NCTF132	VCC_NCTF132	
M14	VCC_NCTF133	VCC_NCTF133	
Y14	VCC_NCTF134	VCC_NCTF134	
W14	VCC_NCTF135	VCC_NCTF135	
V14	VCC_NCTF136	VCC_NCTF136	
U14	VCC_NCTF137	VCC_NCTF137	
T14	VCC_NCTF138	VCC_NCTF138	
R14	VCC_NCTF139	VCC_NCTF139	
P14	VCC_NCTF140	VCC_NCTF140	
N14	VCC_NCTF141	VCC_NCTF141	
M14	VCC_NCTF142	VCC_NCTF142	
Y14	VCC_NCTF143	VCC_NCTF143	
W14	VCC_NCTF144	VCC_NCTF144	
V14	VCC_NCTF145	VCC_NCTF145	
U14	VCC_NCTF146	VCC_NCTF146	
T14	VCC_NCTF147	VCC_NCTF147	
R14	VCC_NCTF148	VCC_NCTF148	
P14	VCC_NCTF149	VCC_NCTF149	
N14	VCC_NCTF150	VCC_NCTF150	
M14	VCC_NCTF151	VCC_NCTF151	
Y14	VCC_NCTF152	VCC_NCTF152	
W14	VCC_NCTF153	VCC_NCTF153	
V14	VCC_NCTF154	VCC_NCTF154	
U14	VCC_NCTF155	VCC_NCTF155	
T14	VCC_NCTF156	VCC_NCTF156	
R14	VCC_NCTF157	VCC_NCTF157	
P14	VCC_NCTF158	VCC_NCTF158	
N14	VCC_NCTF159	VCC_NCTF159	
M14	VCC_NCTF160	VCC_NCTF160	
Y14	VCC_NCTF161	VCC_NCTF161	
W14	VCC_NCTF162	VCC_NCTF162	
V14	VCC_NCTF163	VCC_NCTF163	
U14	VCC_NCTF164	VCC_NCTF164	
T14	VCC_NCTF165	VCC_NCTF165	
R14	VCC_NCTF166	VCC_NCTF166	
P14	VCC_NCTF167	VCC_NCTF167	
N14	VCC_NCTF168	VCC_NCTF168	
M14	VCC_NCTF169	VCC_NCTF169	
Y14	VCC_NCTF170	VCC_NCTF170	
W14	VCC_NCTF171	VCC_NCTF171	
V14	VCC_NCTF172	VCC_NCTF172	
U14	VCC_NCTF173	VCC_NCTF173	
T14	VCC_NCTF174	VCC_NCTF174	
R14	VCC_NCTF175	VCC_NCTF175	
P14	VCC_NCTF176	VCC_NCTF176	
N14	VCC_NCTF177	VCC_NCTF177	
M14	VCC_NCTF178	VCC_NCTF178	
Y14	VCC_NCTF179	VCC_NCTF179	
W14	VCC_NCTF180	VCC_NCTF180	
V14	VCC_NCTF181	VCC_NCTF181	
U14	VCC_NCTF182	VCC_NCTF182	
T14	VCC_NCTF183	VCC_NCTF183	
R14	VCC_NCTF184	VCC_NCTF184	
P14	VCC_NCTF185	VCC_NCTF185	
N14	VCC_NCTF186	VCC_NCTF186	
M14	VCC_NCTF187	VCC_NCTF187	
Y14	VCC_NCTF188	VCC_NCTF188	
W14	VCC_NCTF189	VCC_NCTF189	



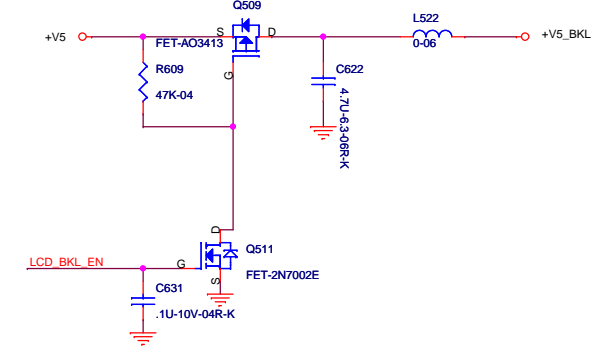
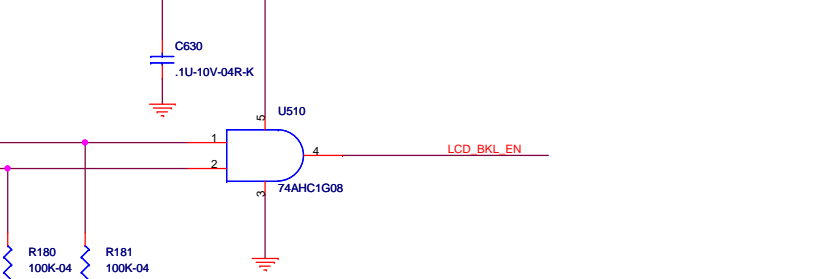
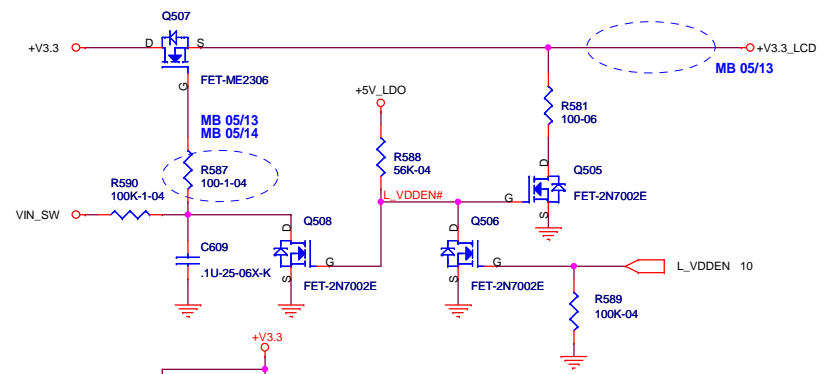
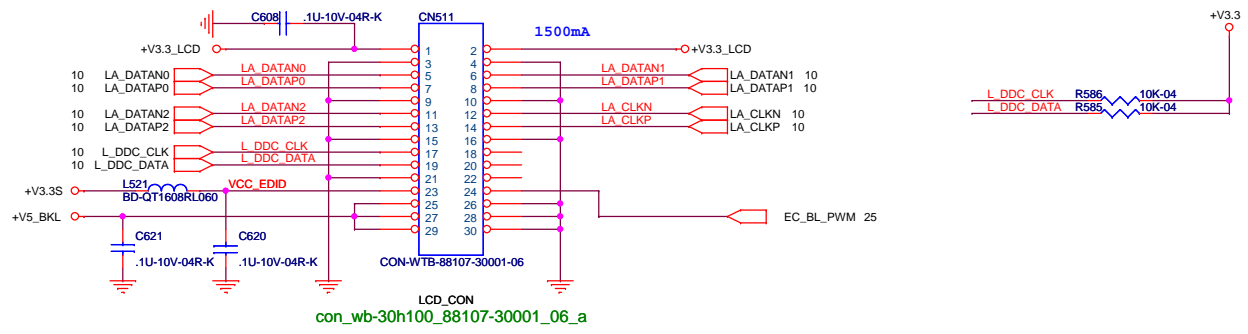
**ELITEGROUP**

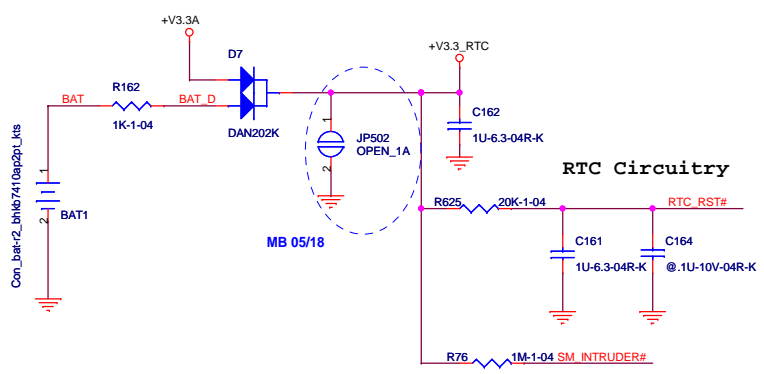
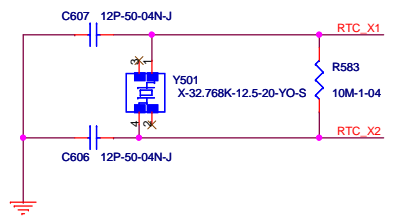
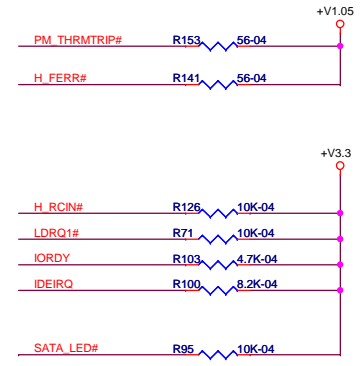
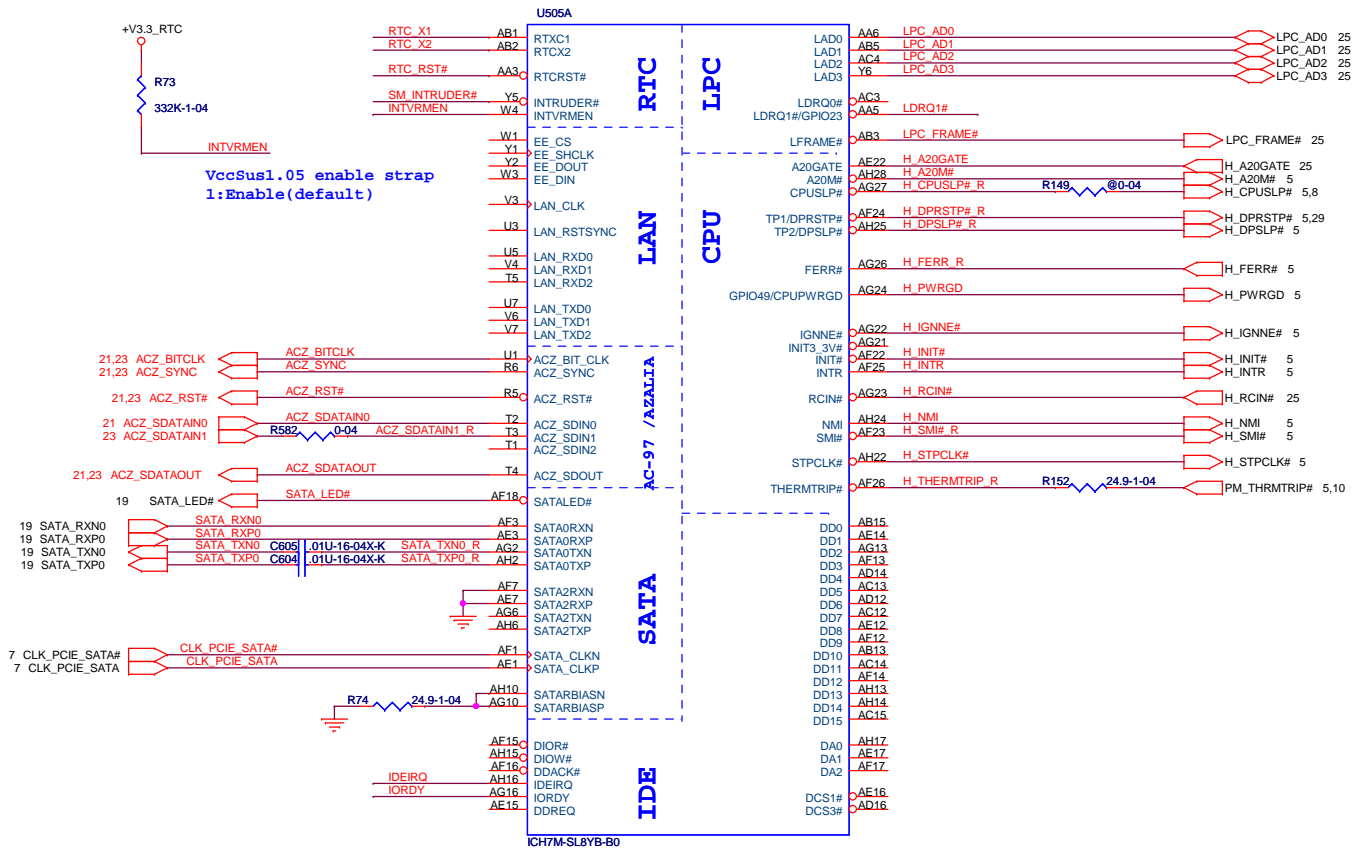
**Project : V101L1**

Size	Document Number	Rev
	<b>945GSE- DMI &amp; VGA(3/4)</b>	B
SCHEMATICS		
Date: Tuesday, May 19, 2009	Sheet	10 of 32







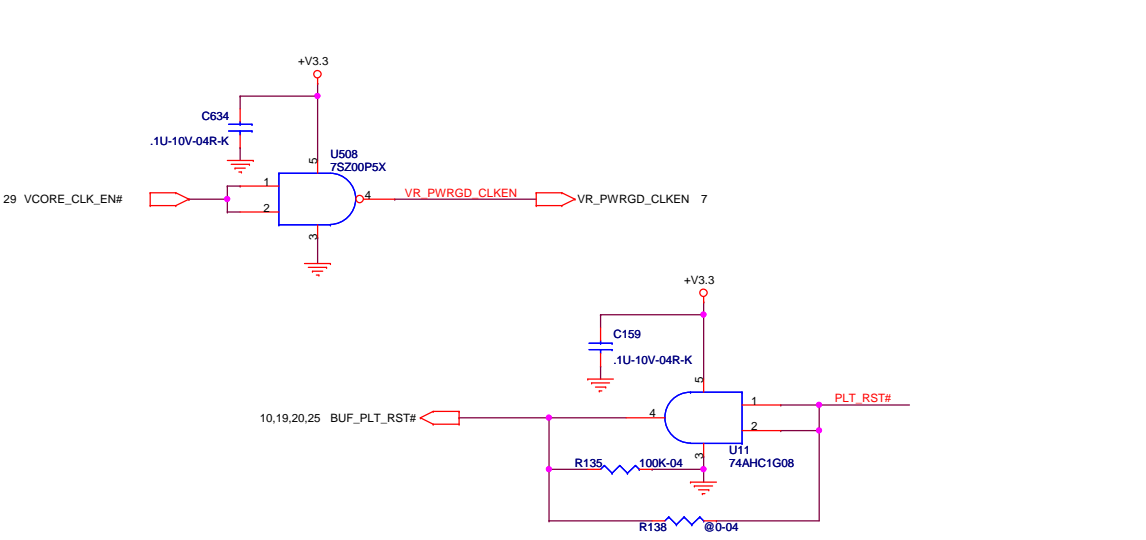
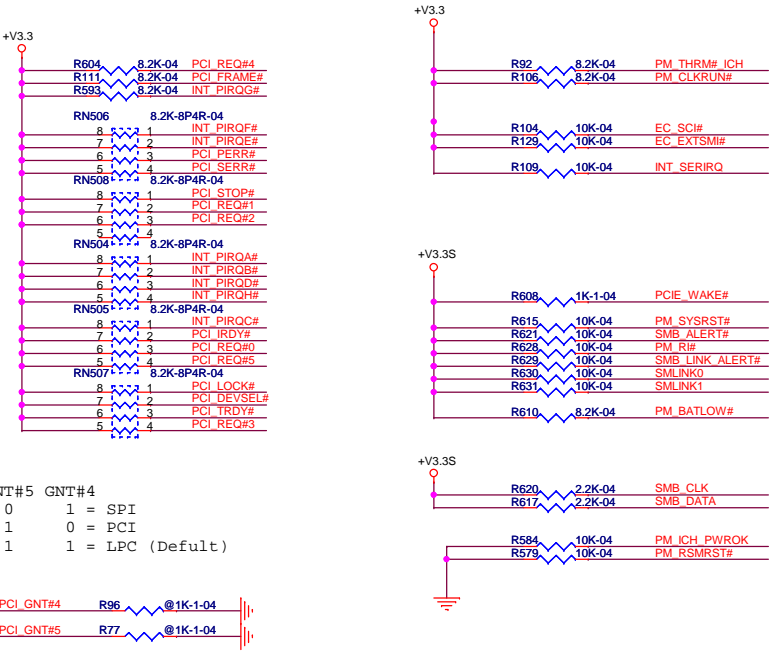
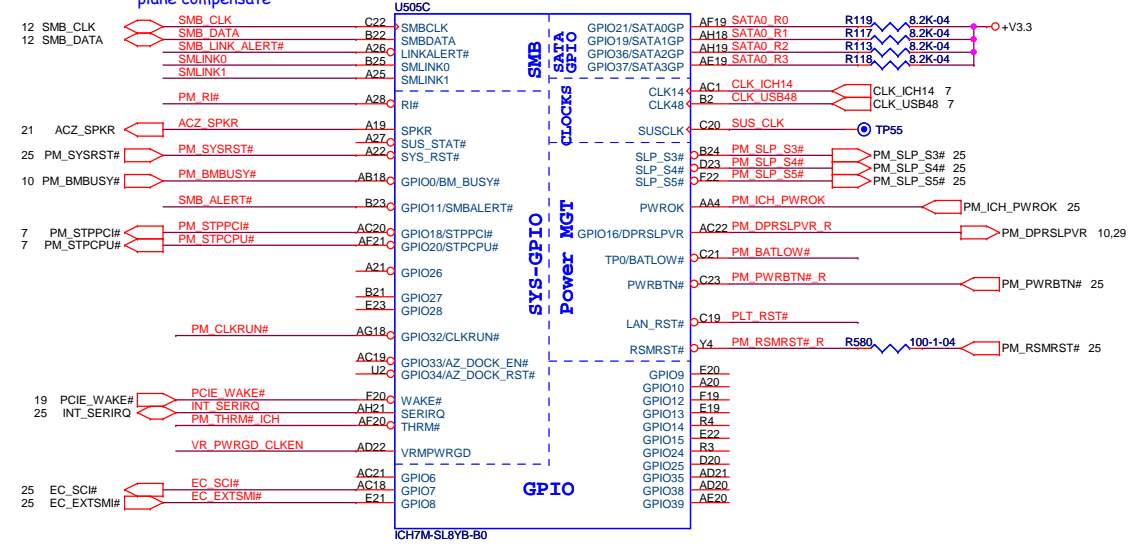
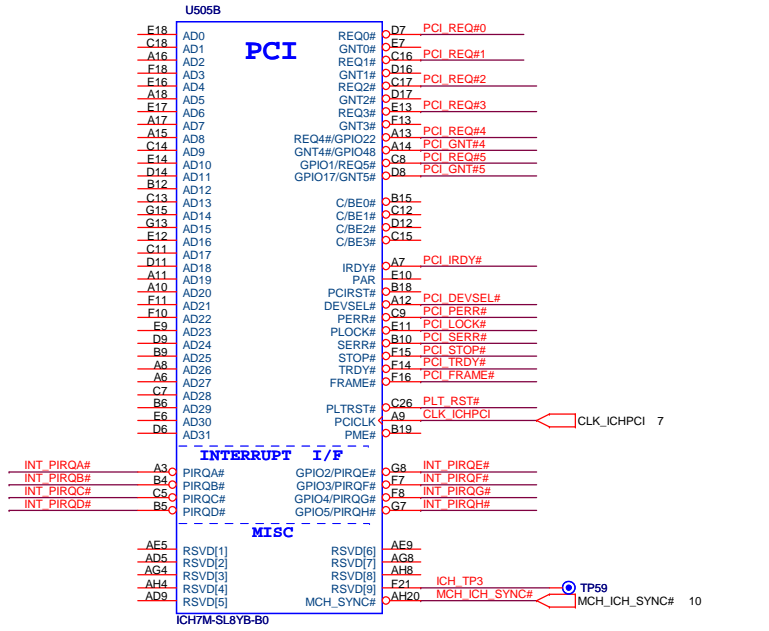


CMOS Settings    JP502  
 Clear CMOS      Short  
 Keep CMOS        Open

Disable SATA function  
 SATA[2,0]RXp/n, SATARBIAS#, SATARBIAS#, SATA\_CLKP,  
 and SATA\_CLKN signals connect to ground  
 SATA[2,0]TXp/n, SATALED# signals NC  
 VccSATAPLL should connect directly to  
 VCC 1.5v, but filter caps not required

Layout Note: Place stuffing option minimize stubs

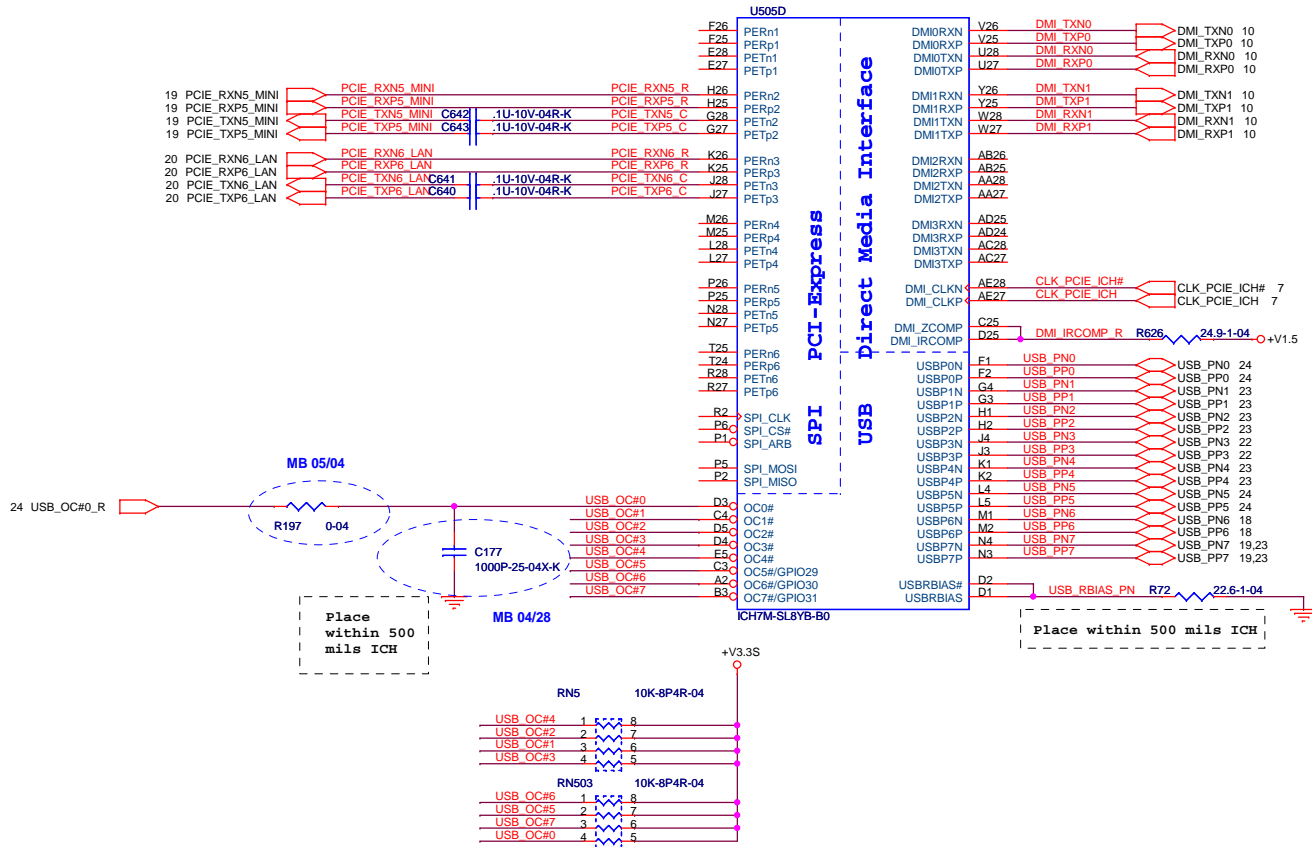
for Singal cross power plane compensate



BCS ELITEGROUP

Project : V10L1

Size	Document Number	Rev
	SB ICH7M- PCI & GPIO(2/4)	B
Date:	Tuesday, May 19, 2009	Sheet 15 of 32



**USB Ports Table**

USBP0	USBP0	M/B USB0
USBN0	USBP1	M/B USB1
USBP1	USBP2	M/B USB2
USBP2	USBP3	CARDREADER
USBP3	USBP4	3G CARD
USBP4	USBP5	BLUETOOTH
USBP5	USBP6	WEBCAM
USBP6	USBP7	MINICARD
USBP7	USBN7	SIM USB



**ELITEGROUP**

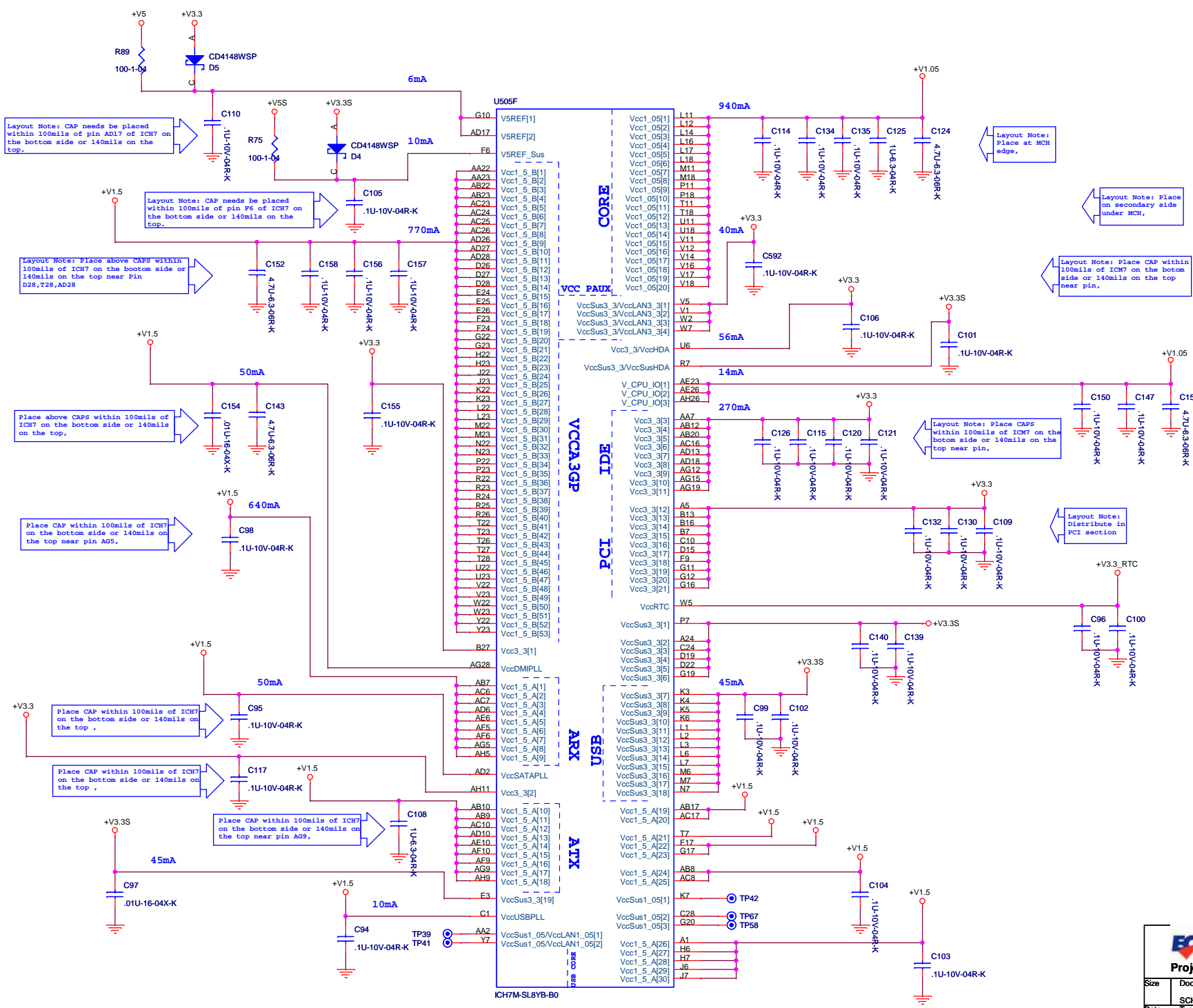
Project : V10L1

Size Document Number **SB ICH7M- PCIE & USB(3/4)** Rev B

SCHMATICS

Date: Tuesday, May 19, 2009 Sheet 16 of 32





Layout Note: CAP needs to be placed within 100mils of ICH7 on the bottom side or 140mils on the top.

Layout Note: CAP needs to be placed within 100mils of pin F6 of ICH7 on the bottom side or 140mils on the top.

Layout Note: Place above CAPS within 100mils of ICH7 on the bottom side or 140mils on the top near Pin D28, T28, AD28

Place above CAPS within 100mils of ICH7 on the bottom side or 140mils on the top.

Place CAP within 100mils of ICH7 on the bottom side or 140mils on the top near pin AG5.

Place CAP within 100mils of ICH7 on the bottom side or 140mils on the top.

Place CAP within 100mils of ICH7 on the bottom side or 140mils on the top.

Place CAP within 100mils of ICH7 on the bottom side or 140mils on the top near pin AG9.

Layout Note: Place at MCH edge.

Layout Note: Place on secondary side under MCH.

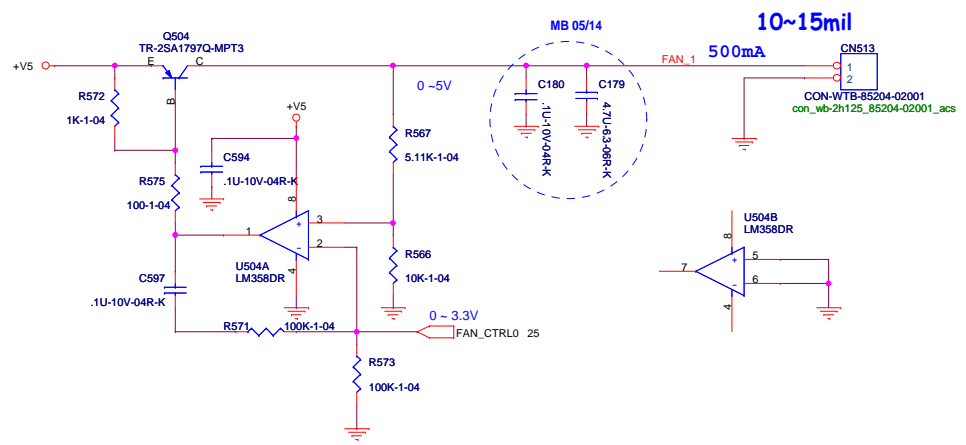
Layout Note: Place CAP within 100mils of ICH7 on the bottom side or 140mils on the top near pin,

Layout Note: Place CAPS within 100mils of ICH7 on the bottom side or 140mils on the top near pin,

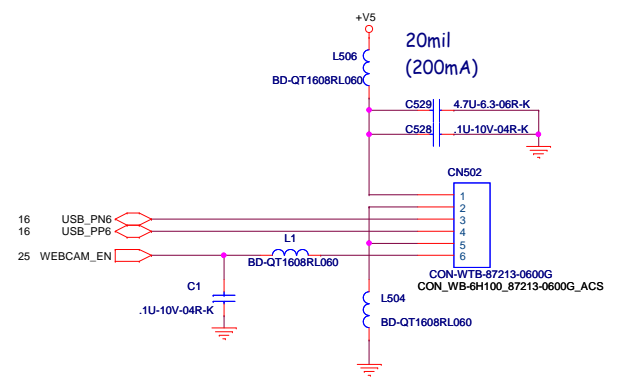
Layout Note: Distribute in PCI section

**BCS ELITEGROUP**  
 Project : V10L1  
 Size Document Number  
 SCHEMATICS SB ICH7M- POWER & GND(4/4) Rev B  
 Date: Tuesday, May 19, 2009 Sheet 17 of 32

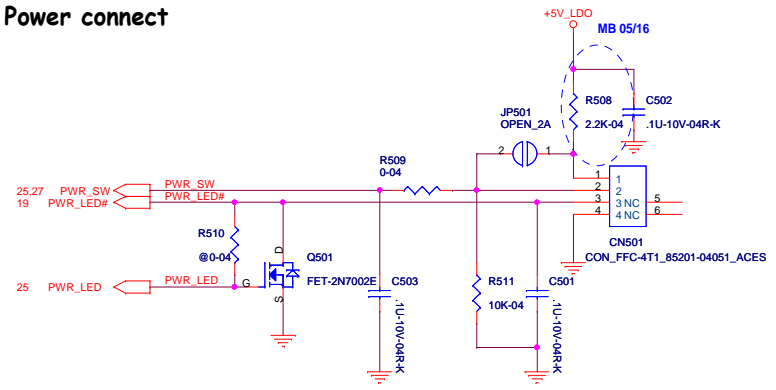
FAN control



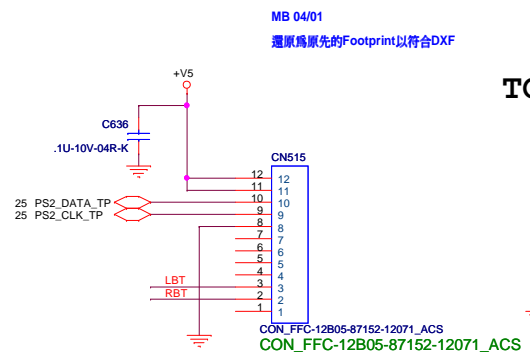
Web CAM CON



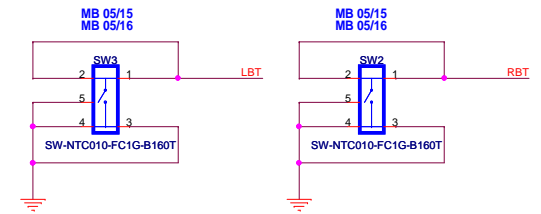
Power connect



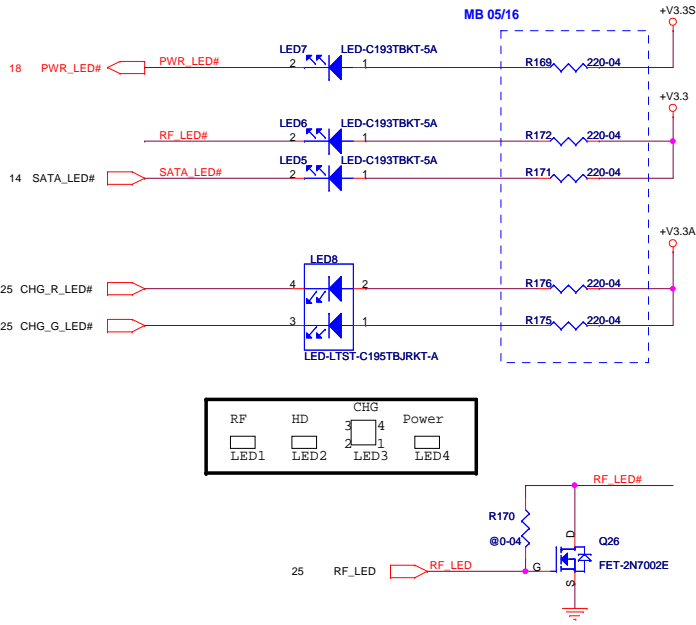
Touch PAD CON



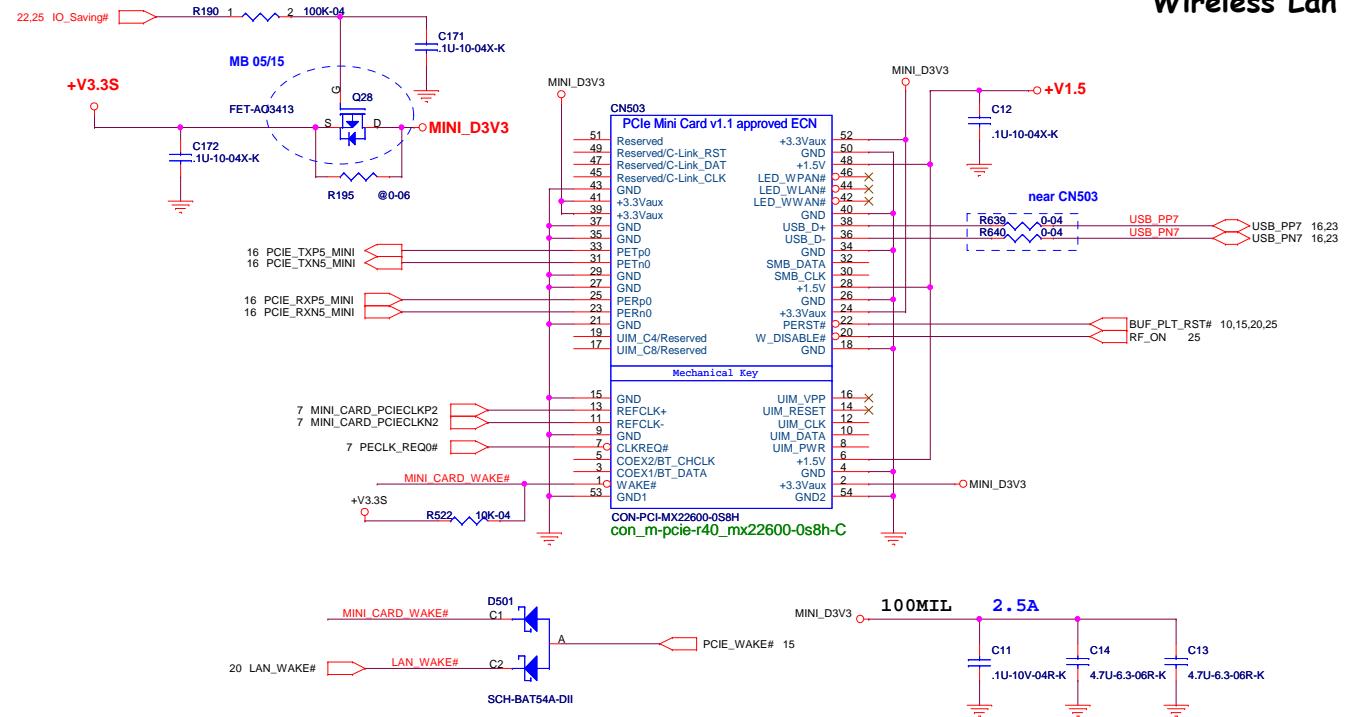
TOUCH PAD BUTTON



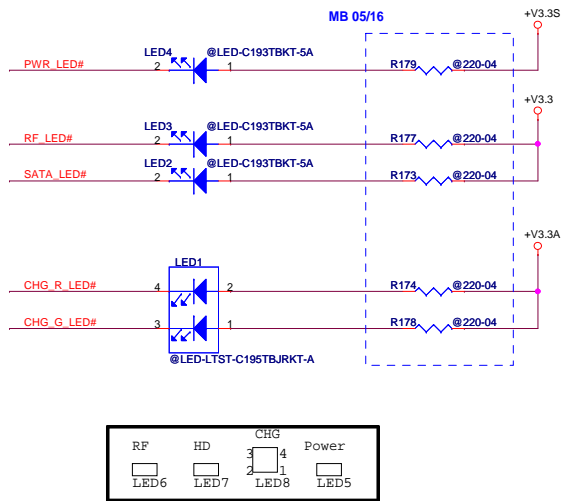
# LED Display ID1



# Wireless Lan



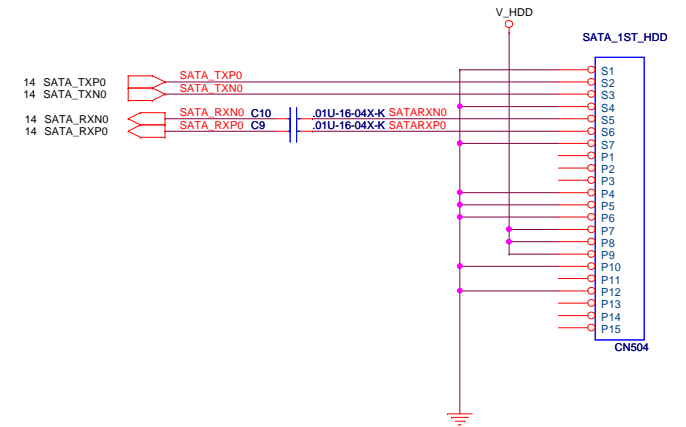
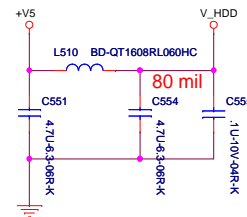
# LED Display ID2



# SATA Connector

## LAYOUT: HDD Power

+5V\_HDD: 50 mil / 700mA

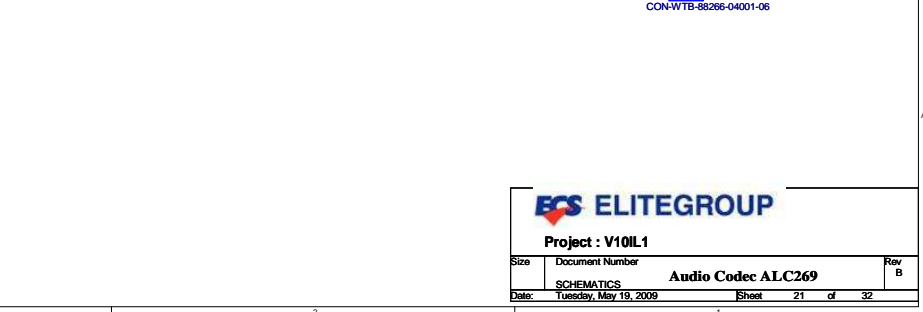
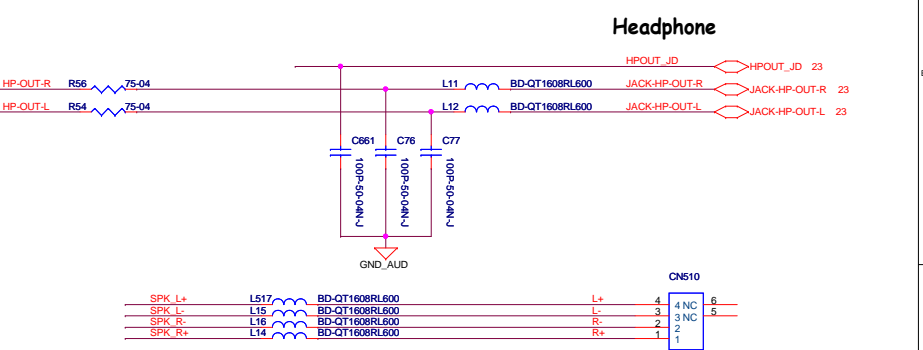
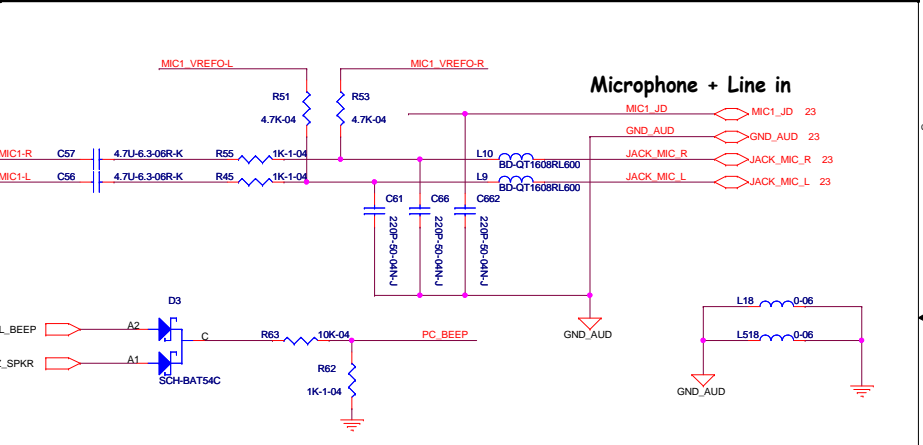
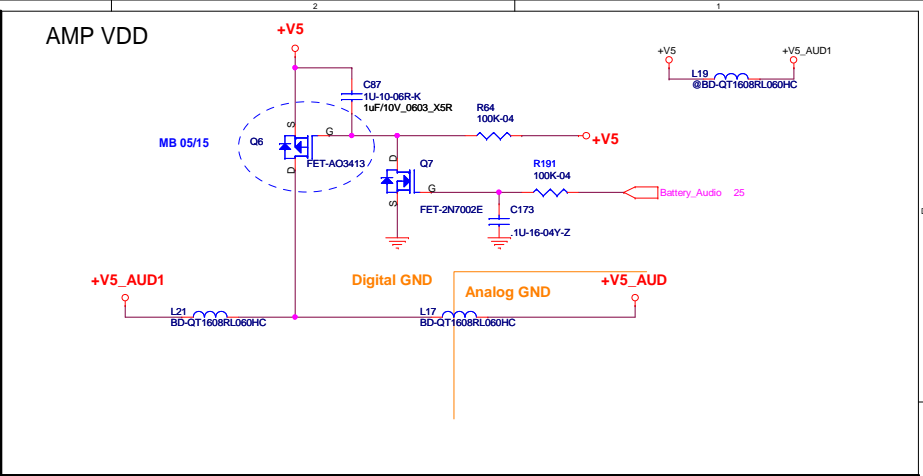
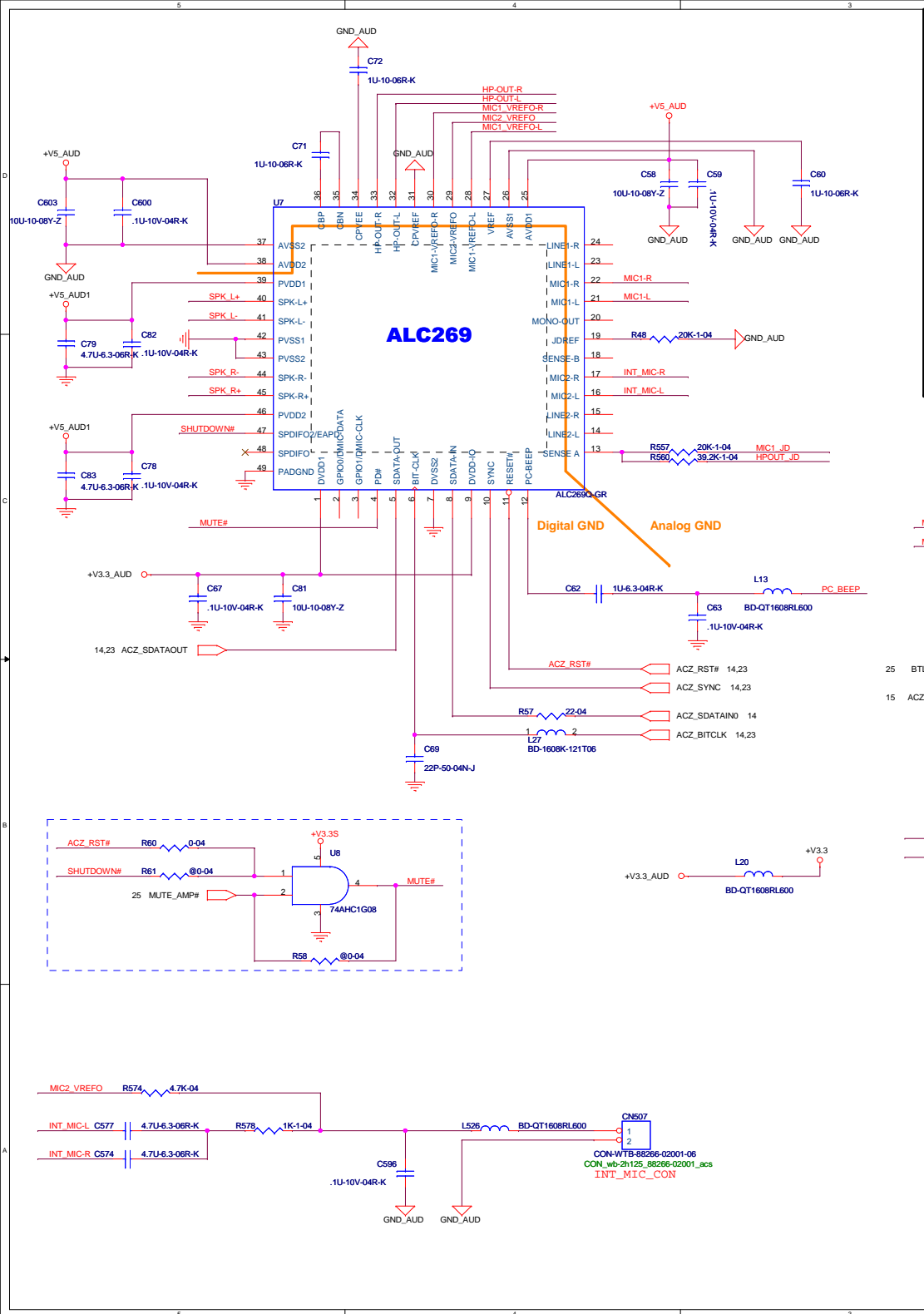


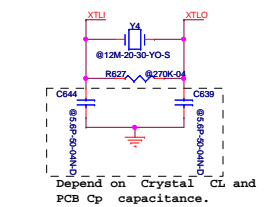
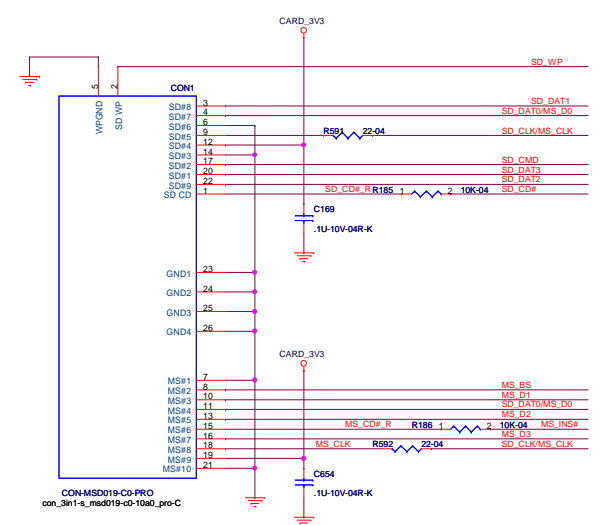
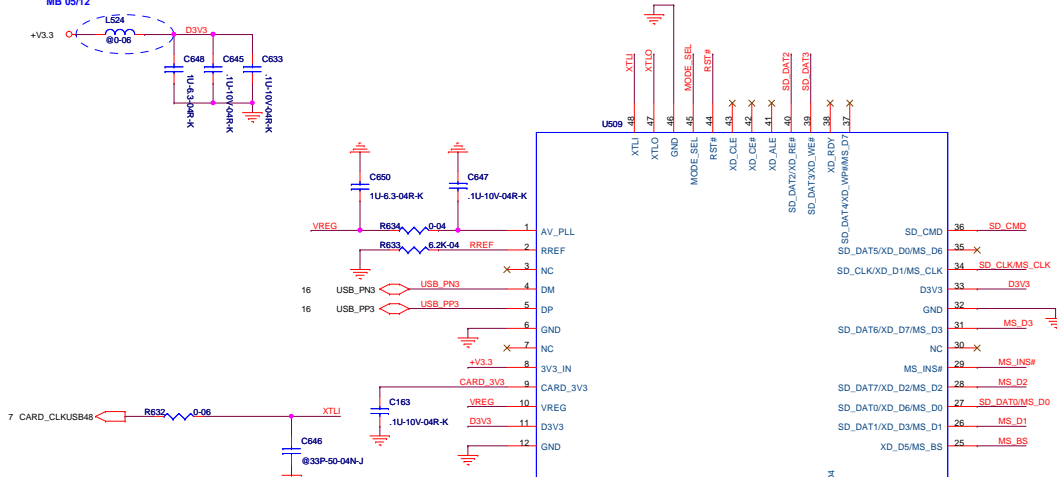
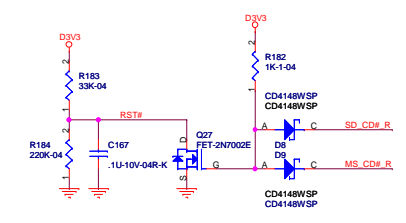
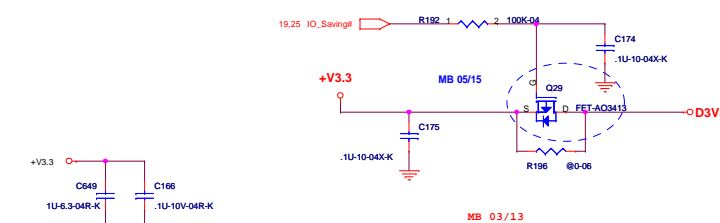
**ELITEGROUP**

Project : V10L1

Size	Document Number	Rev
	SCHMATICS	B
Date:	Tuesday, May 19, 2009	Sheet 19 of 32

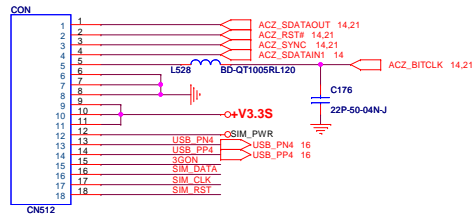




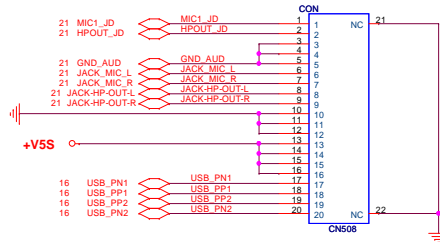


		<b>R643</b>	
CLK GEN 48MHz input		<b>0 Ohm</b>	LUN0/ALL
12MHz Crystal input		<b>Floating</b>	

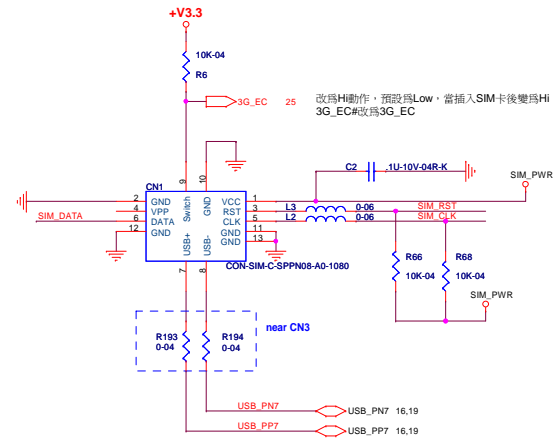
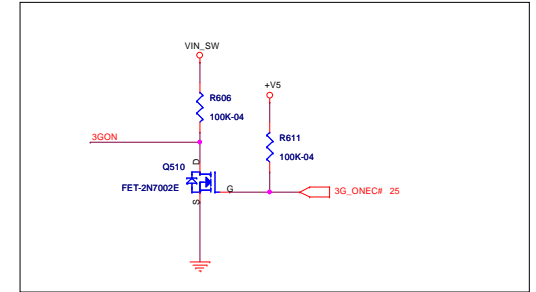
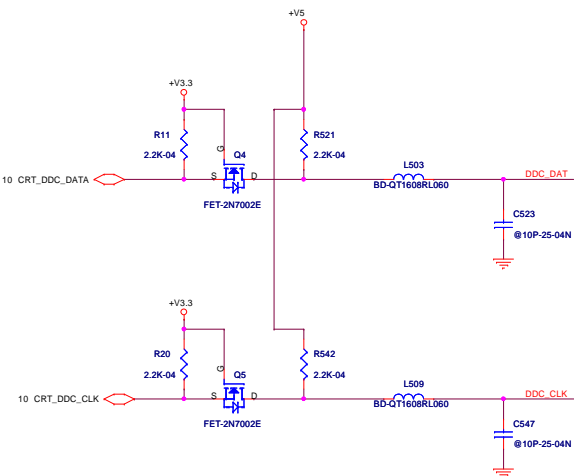
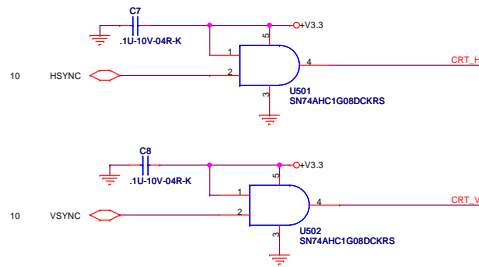
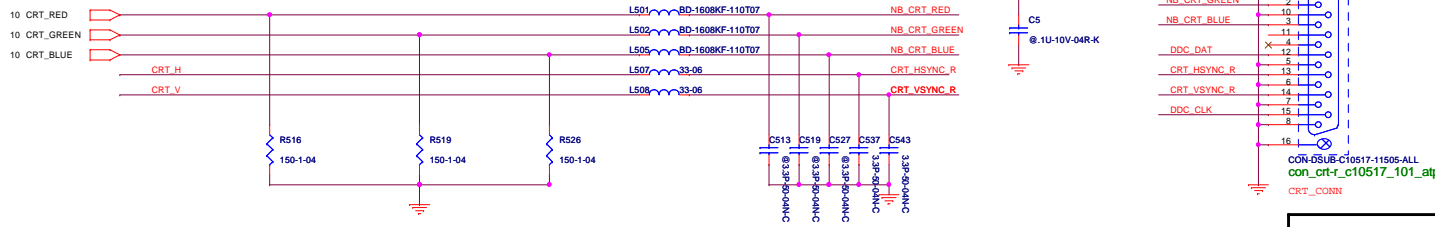
3G & MODEM CONN TO SMALL BD



USB AUDIO RJ-11 CONNECT TO SMALL BD

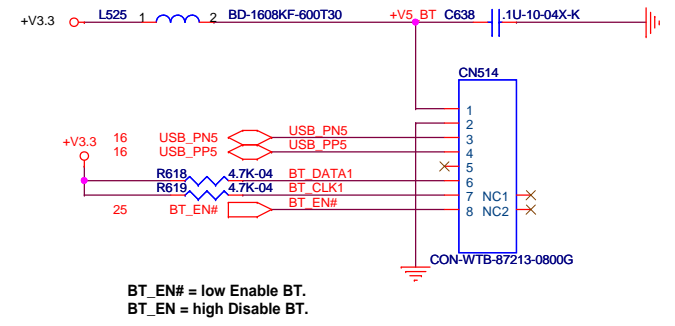
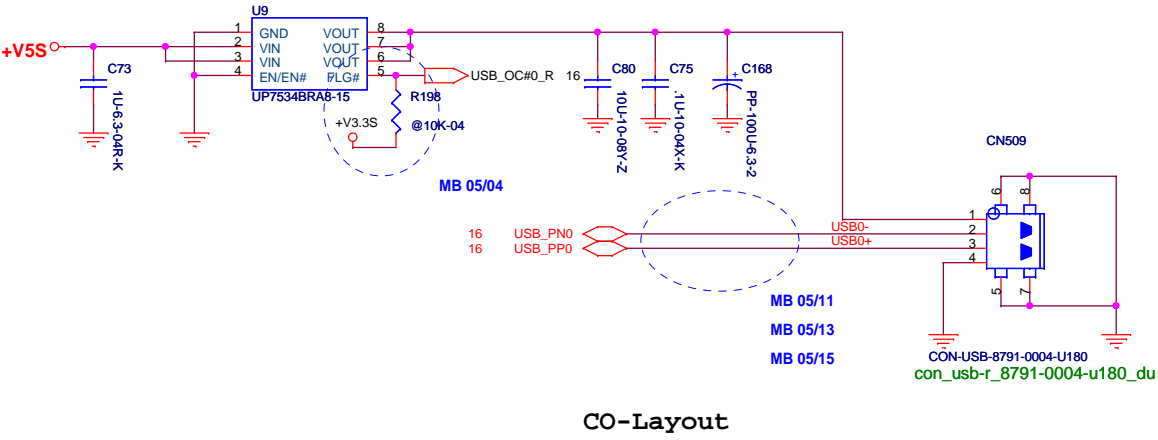


CRT



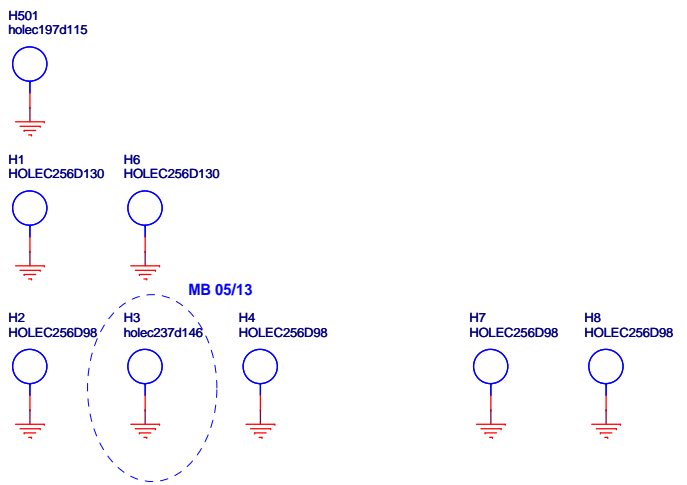
# USB Port

# BULETOOTH

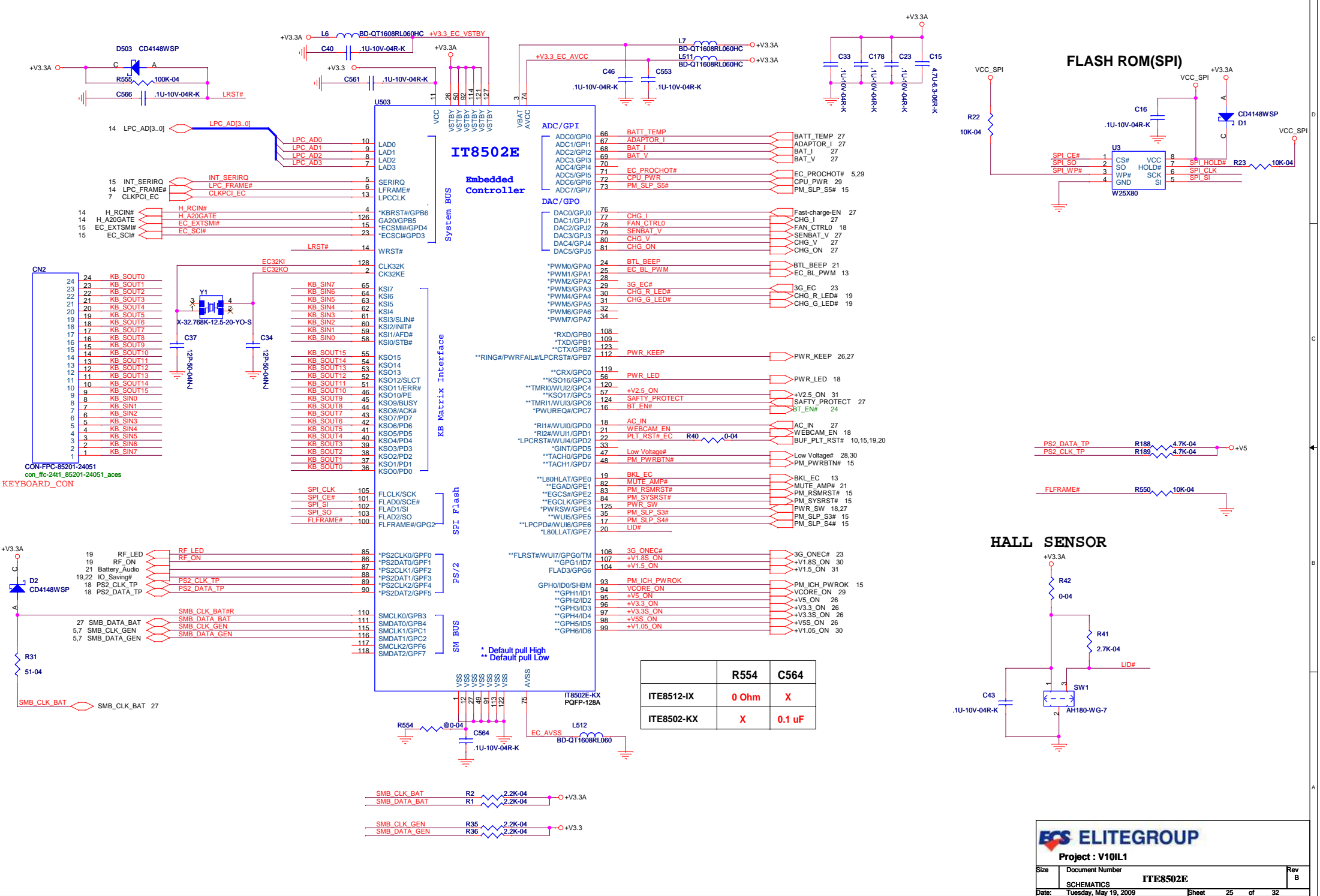


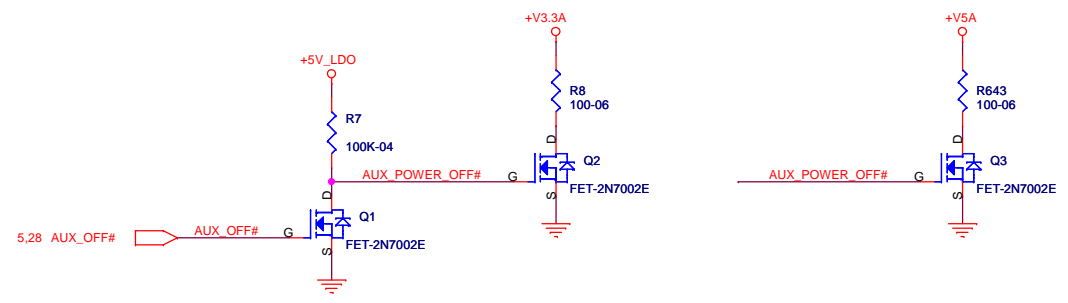
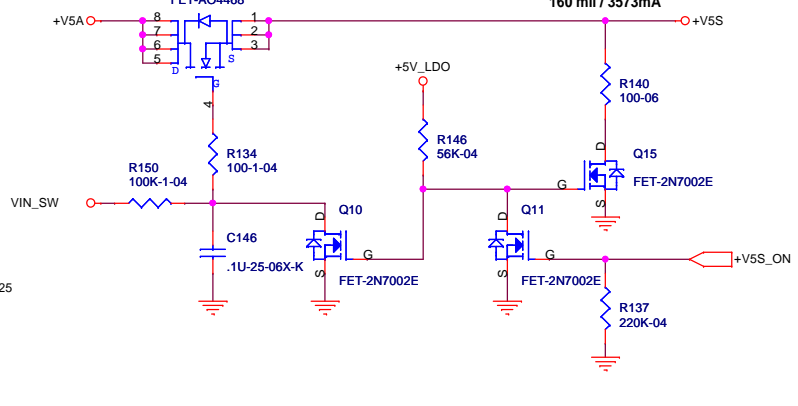
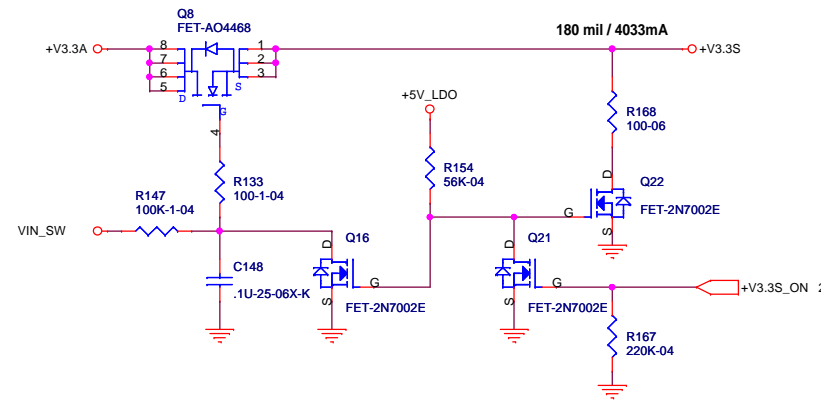
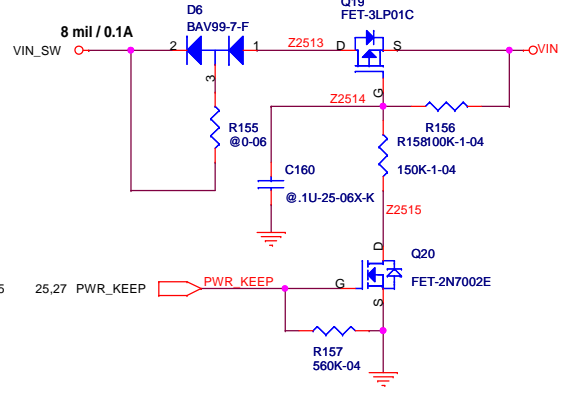
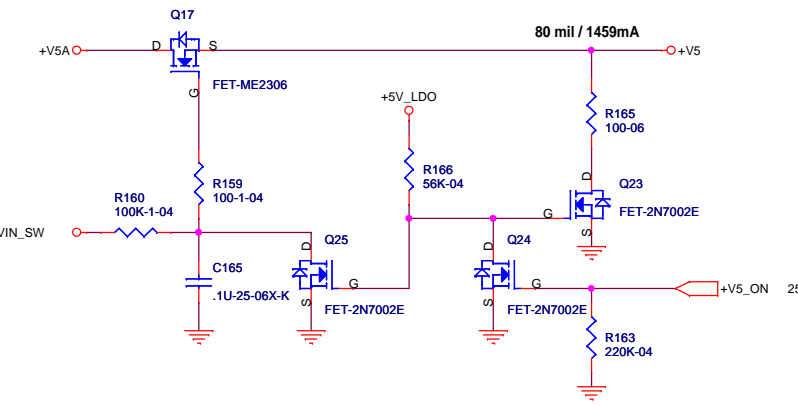
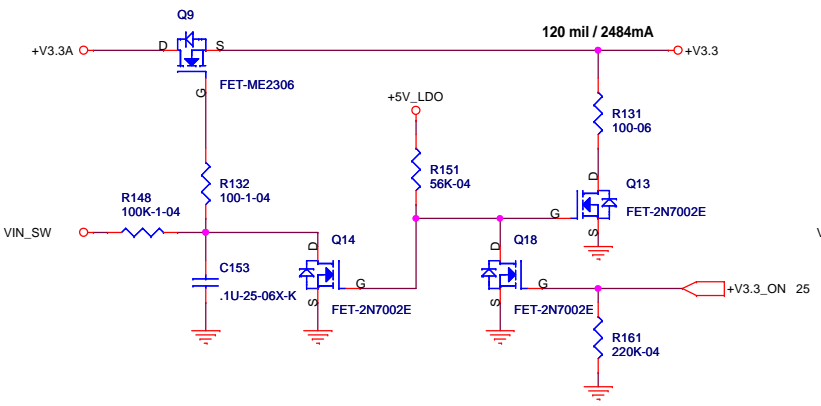
# G-SENSOR

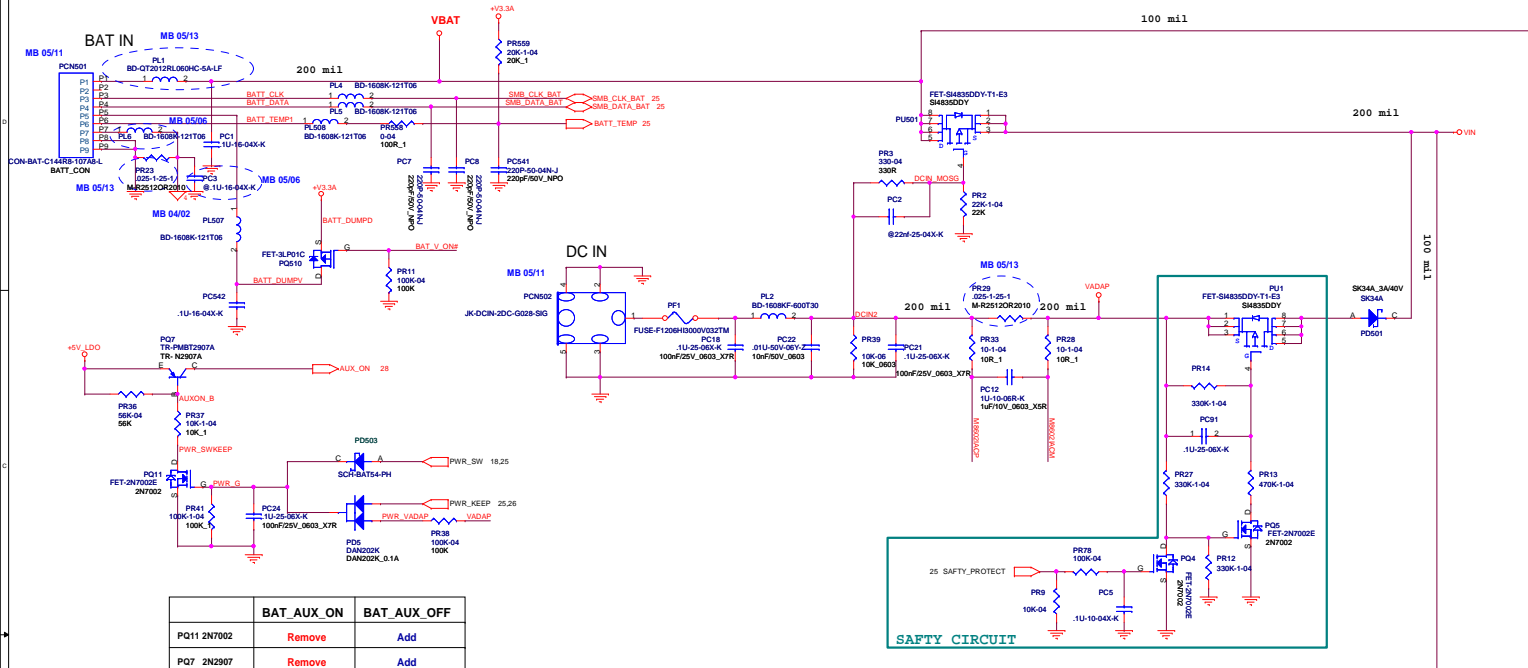
B Phase 移除 G-SENSOR FUNCTION



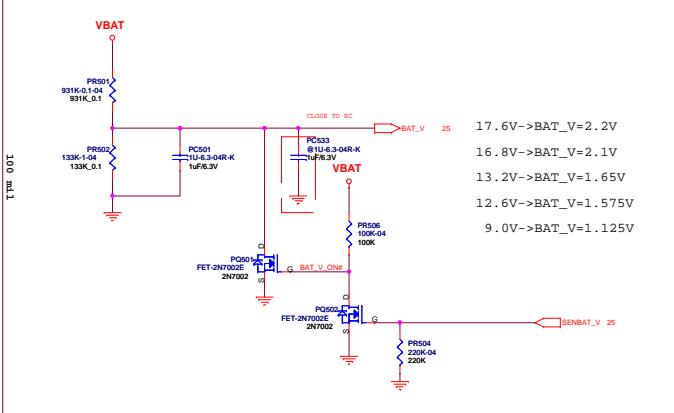






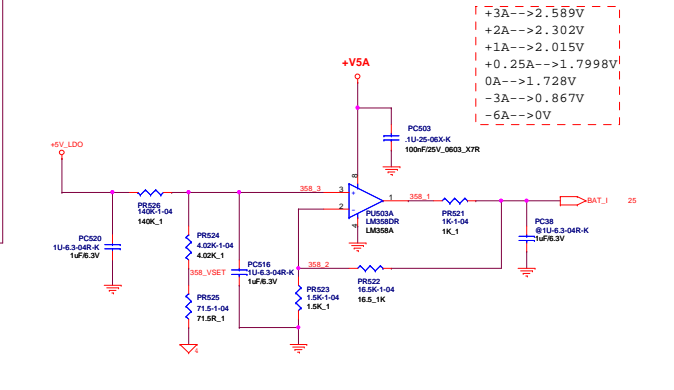


### Battery Voltage Detect



- 17.6V->BATT\_V=2.2V
- 16.8V->BATT\_V=2.1V
- 13.2V->BATT\_V=1.65V
- 12.6V->BATT\_V=1.575V
- 9.0V->BATT\_V=1.125V

### Charge / Discharge Detect



- +3A-->2.589V
- +2A-->2.302V
- +1A-->2.015V
- +0.25A-->1.798V
- 0A-->1.728V
- 3A-->0.867V
- 6A-->0V

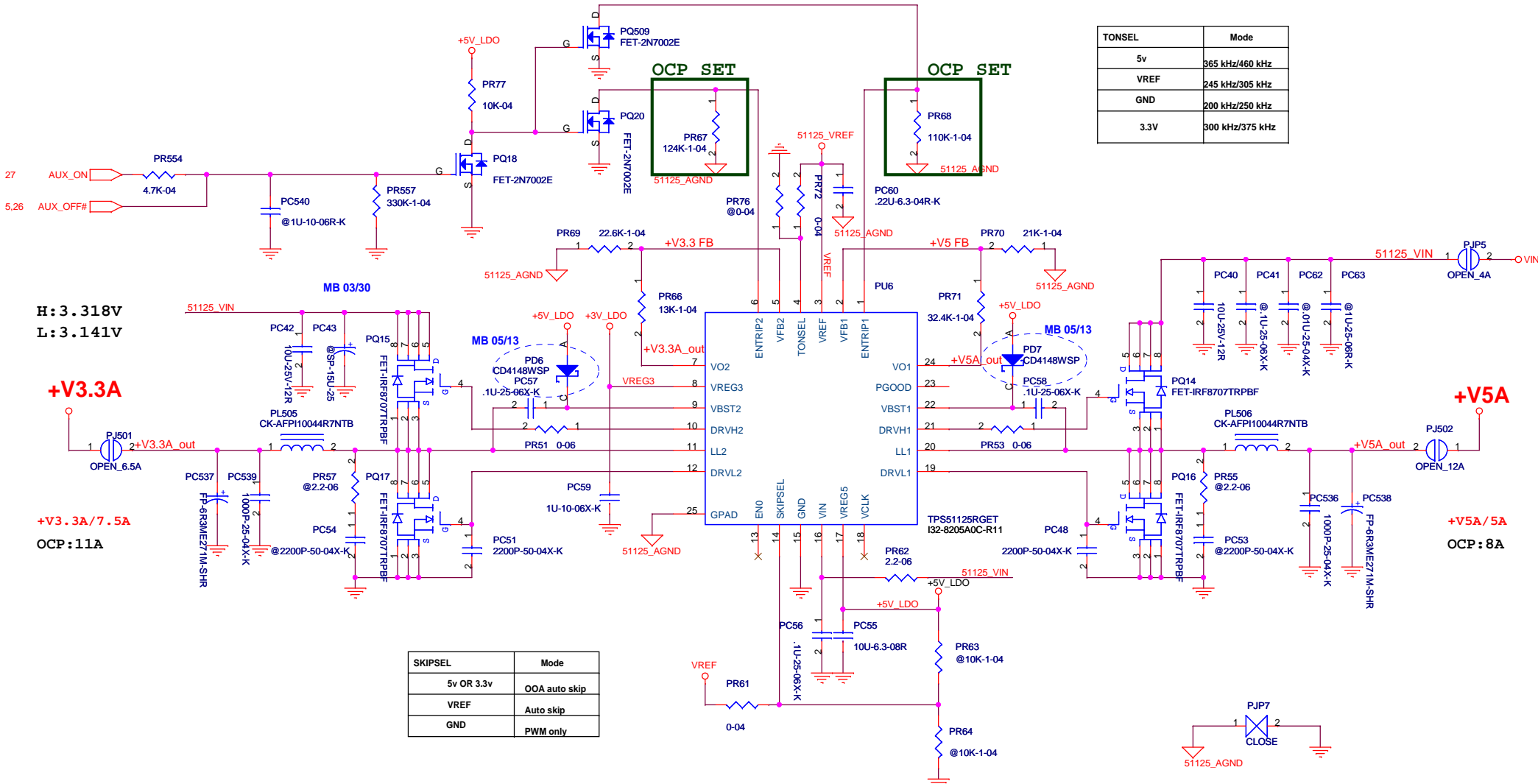
	BAT_AUX_ON	BAT_AUX_OFF
PQ11 2N7002	Remove	Add
PQ7 2N2907	Remove	Add

CHG_V	
H	16.8V (4CELL)
L	12.6V (3CELL)

CHG_ON	
L	CHARGER ON
H	CHARGER OFF

ADAPTOR_I	
1A	0.25V
1.5A	0.375V
2A	0.5V
2.5A	0.625V
3A	0.75V
3.5A	0.875V

Fast-charge-EN	CHG_I	Ich
H	3V	2.8A
H	2.1V	2.5A
H	0.6V	2A
L		
L	3V	1A
L	0.6V	0.200A
L	0.375V	0.125A



TONSEL	Mode
5v	365 kHz/460 kHz
VREF	245 kHz/305 kHz
GND	200 kHz/250 kHz
3.3V	300 kHz/375 kHz

H: 3.318V  
L: 3.141V

**+V3.3A**

+V3.3A/7.5A

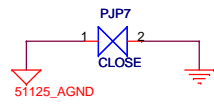
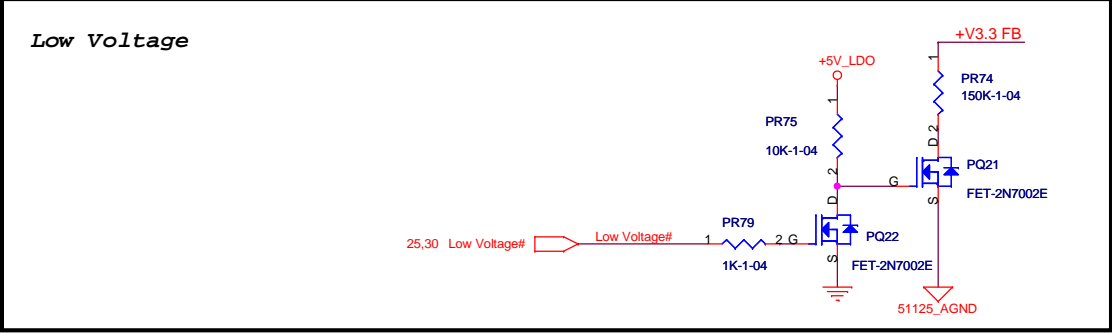
OCP: 1.1A

**+V5A**

+V5A/5A

OCP: 8A

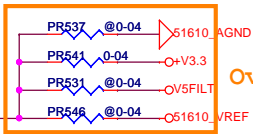
SKIPSEL	Mode
5v OR 3.3v	OOA auto skip
VREF	Auto skip
GND	PWM only



**ECS ELITEGROUP**

**Project : V10IL1**

Size	Document Number	Rev
SCHEMATICS +V3.3A/+V5A(TPSS1125)		B
Date:	Tuesday, May 19, 2009	Sheet 28 of 32

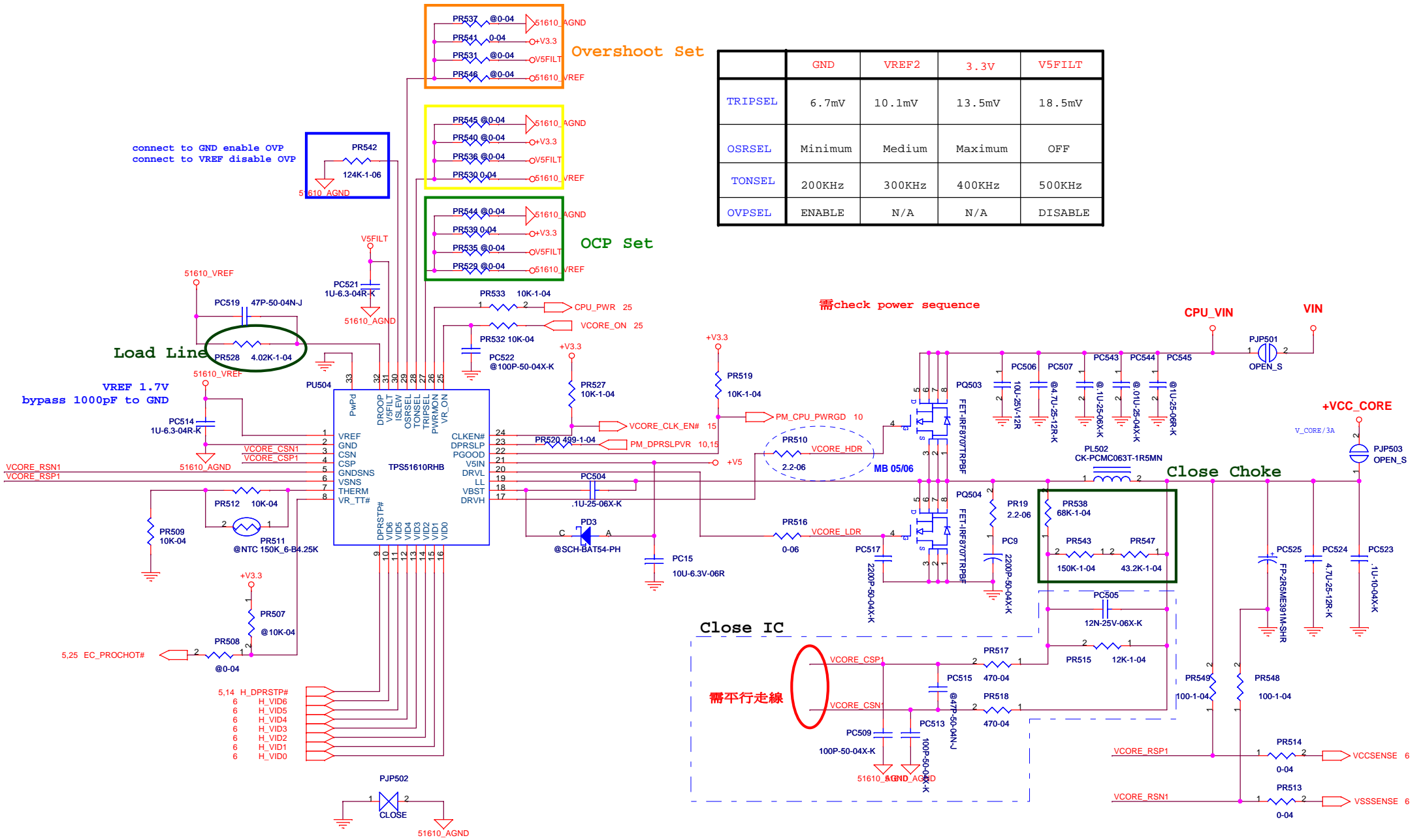


Overshoot Set



OCP Set

	GND	VREF2	3.3V	V5FILT
TRIPSEL	6.7mV	10.1mV	13.5mV	18.5mV
OSRSEL	Minimum	Medium	Maximum	OFF
TONSEL	200KHz	300KHz	400KHz	500KHz
OVPSEL	ENABLE	N/A	N/A	DISABLE



Load Line

VREF 1.7V  
bypass 1000pF to GND

需check power sequence

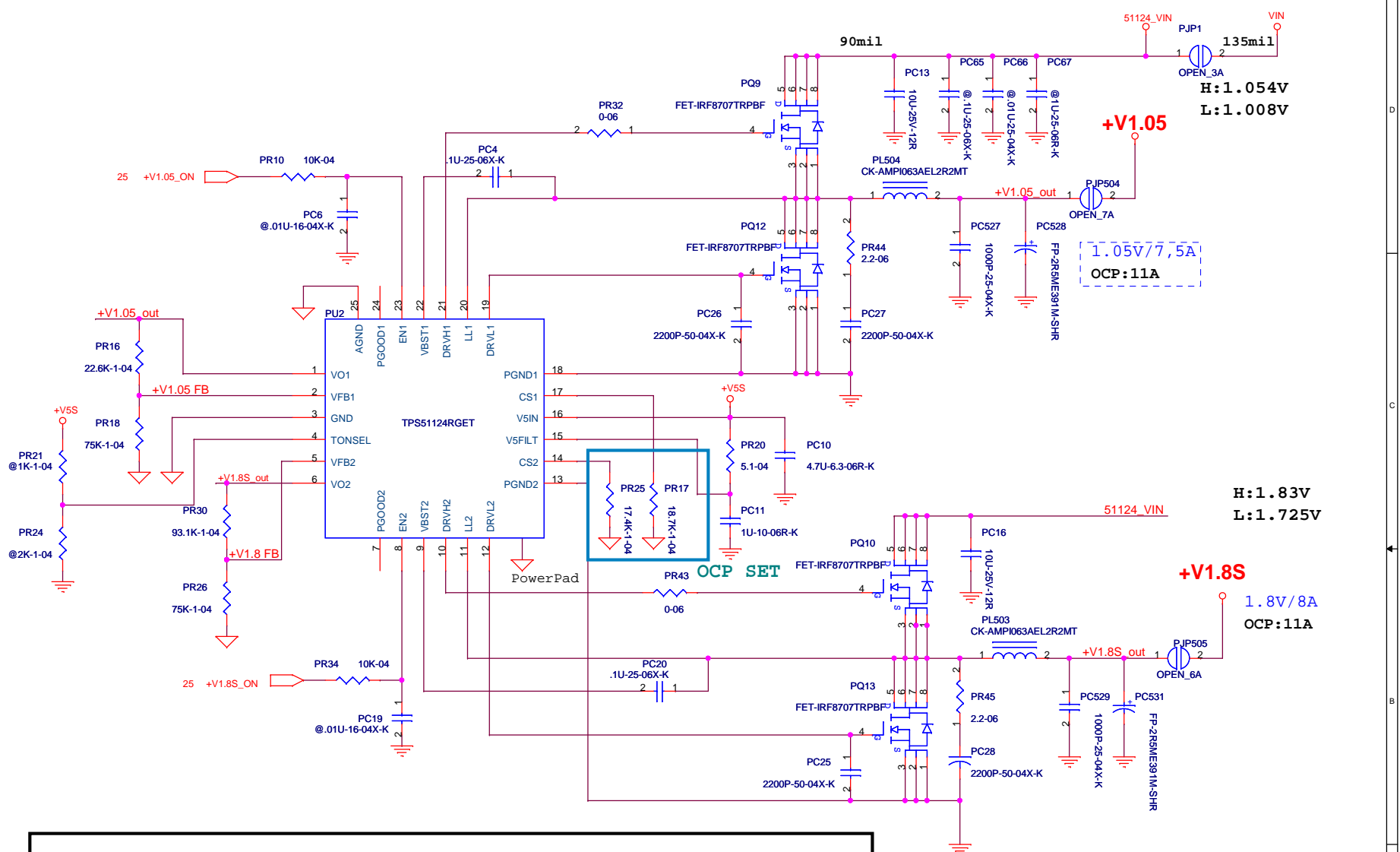
Close Choke

Close IC

需平行走線

**ELITEGROUP**  
Project : V10L1

Size	Document Number	Rev
	SCHMATICS V Core(TPS51610)	B
Date:	Tuesday, May 19, 2009	Sheet 29 of 32

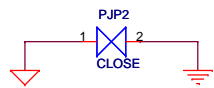
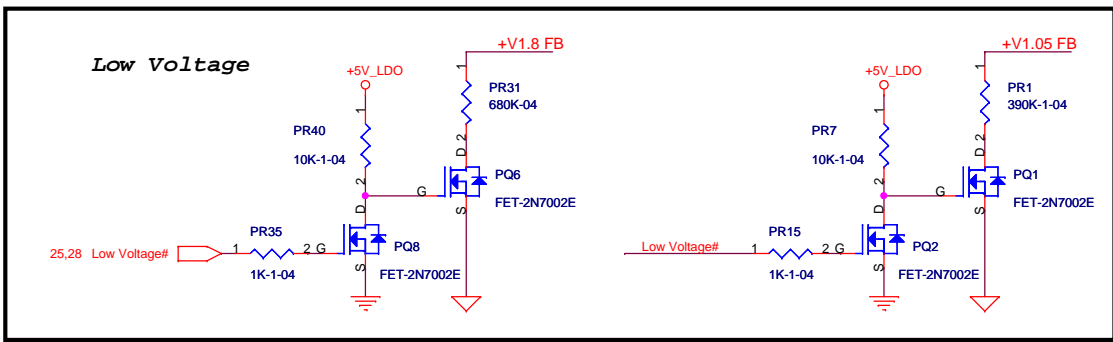


H: 1.054V  
L: 1.008V

1.05V/7.5A  
OCP: 1.1A

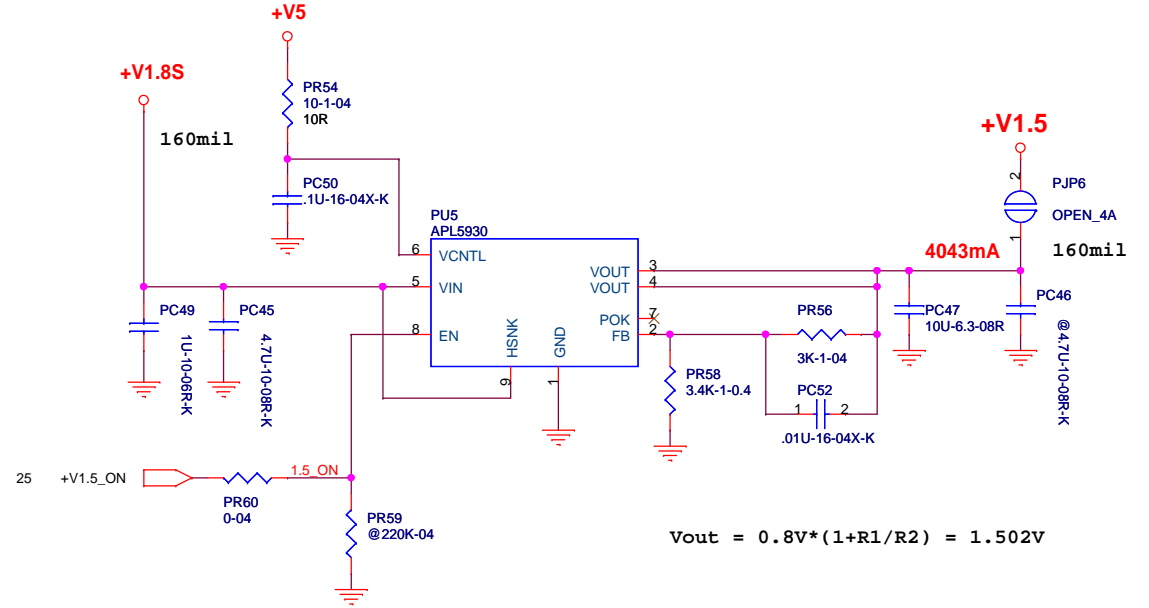
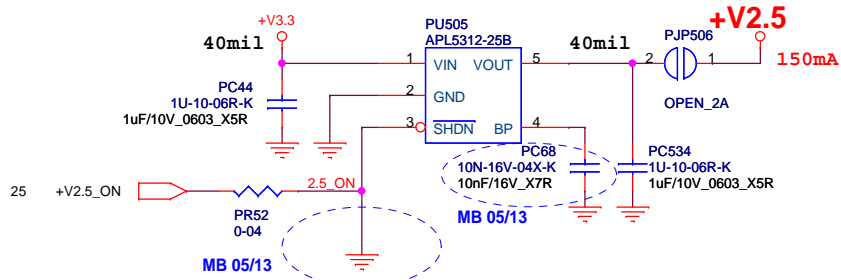
H: 1.83V  
L: 1.725V

+V1.8S  
1.8V/8A  
OCP: 1.1A

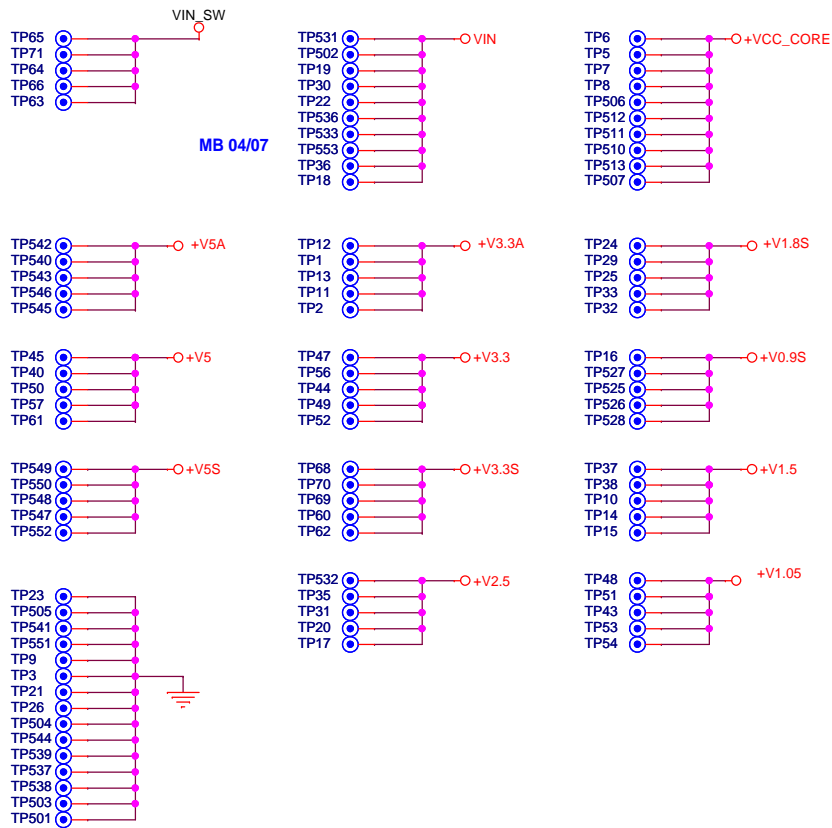


**ECS ELITEGROUP**  
Project : V10IL1

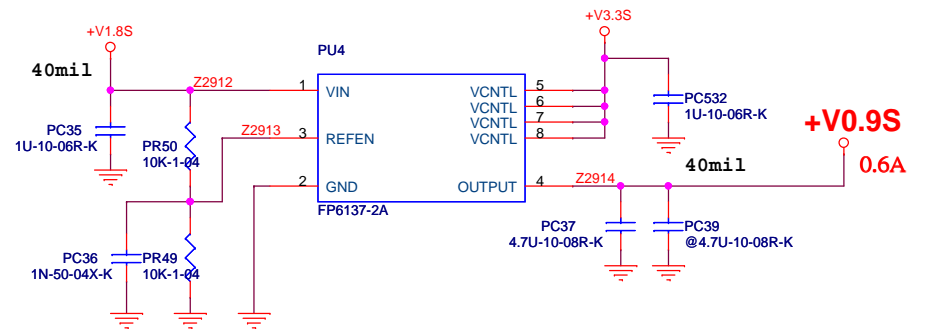
Size	Document Number	Rev
	SCHEMATICS +V1.05 (OZ8116)	B
Date: Tuesday, May 19, 2009	Sheet 30 of 32	



### POWER TP



### layout to DIMM



**ELITEGROUP**

**Project : V10L1**

Size	Document Number	Rev
	<b>+V1.5/+V0.9S/+V2.5/+V2.5S</b>	<b>B</b>
Date:	Tuesday, May 19, 2009	Sheet 31 of 32

V10L1 C phase modify list:

MB 04/28

1. page 16 新增電容C177・1000P-25-04X-K
2. page 03 修改POWER SEQ

MB 05/04

1. page 16 新增R197 0OHM 0402・上件
2. page 24 新增R198 10K OHM 0402 PULL HI +V3.3S・不上件

MB 05/06

1. page 29 PR510改阻值為2.2 ohm
2. page 27 新增PL6 BD-1608K-121T06・上件  
新增PC3 @.1U-16-04X-K・不上件

MB 05/11

1. page 25 C558改C178
2. page 24 移除L516
3. page 20 移除L8
4. Q507・Q1・Q9・Q17零件的Footprint：M-SOT23G改為M-SOT23G-1
5. PCN502的Footprint改為2DC-G028X200
6. PCN501的Footprint改為CON-BAT-C144G9-ALL

MB 05/12

1. page 22 L524改不上件

MB 05/13

1. page 23 H3改holec237d146
2. page 28 PD6・PD7上件
3. page 31 移除R553
4. page 13 移除L519
5. page 24 移除R576・R577
6. page 20 L8先加回・等EMI通知
7. page 27 PL1的Footprint改為M-R0805
8. page 27 PR503・PR23・PR29的Footprint改為M-R2512OR2010
9. page 13 PC535改名為PC68
10. page 31 R587改名為R199

MB 05/14

1. page 13 R199改名為R587
2. Q1零件的Footprint改回M-SOT23G
3. page18 C651改名C179  
C652改名C180

MB 05/15


1. page 18 SW2・SW3的Footprint改為con\_sw-t\_ntc010-dc1g-e160t\_tmecc
2. page 23 CN1的Footprint改為CON\_SIM\_SPPN08-A0-1030\_PRO
3. Q6・Q28・Q29改為FET-A03413・Footprint改為M-SOT23G\_B

MB 05/16

1. page 19 R169・R171・R172・R175・R176改為220-04  
R173・R174・R177・R178・R179改為220-04此為For ID2的零件・ID1不上件
2. page 18 R508改為2.2K-04
3. page 18 因為SW2・SW3的Footprint改為con\_sw-t\_ntc010-dc1g-e160t\_tmecc  
所以pin name也跟著做修正・A改1・B改3・C改2・D改4・E改5

MB 05/18

1. page 14 JP1更名為JP502・並更換位置・解決無法clear CMOS的問題
2. page 20 RP1移除・L8改上件

		<b>Elitegroup Computer Systems</b>	
<b>Change Notes</b>			
Title			
Size	Document Number	Rev	
	SCHMATICS	B	
Date:	Tuesday, May 19, 2009	Sheet	32 of 32