MODEL NAME : *VAZA0*
PCB NO : *LA-9262P (DAB0000I010)*
BOM P/N :

Dell/Compal Confidential

ZZZ
MB_PCB

Schematic Document

Murcielgo MLK (Haswell ULT)

2013-04-19

Rev: 1.0

Highlight the short pad for 0 ohm

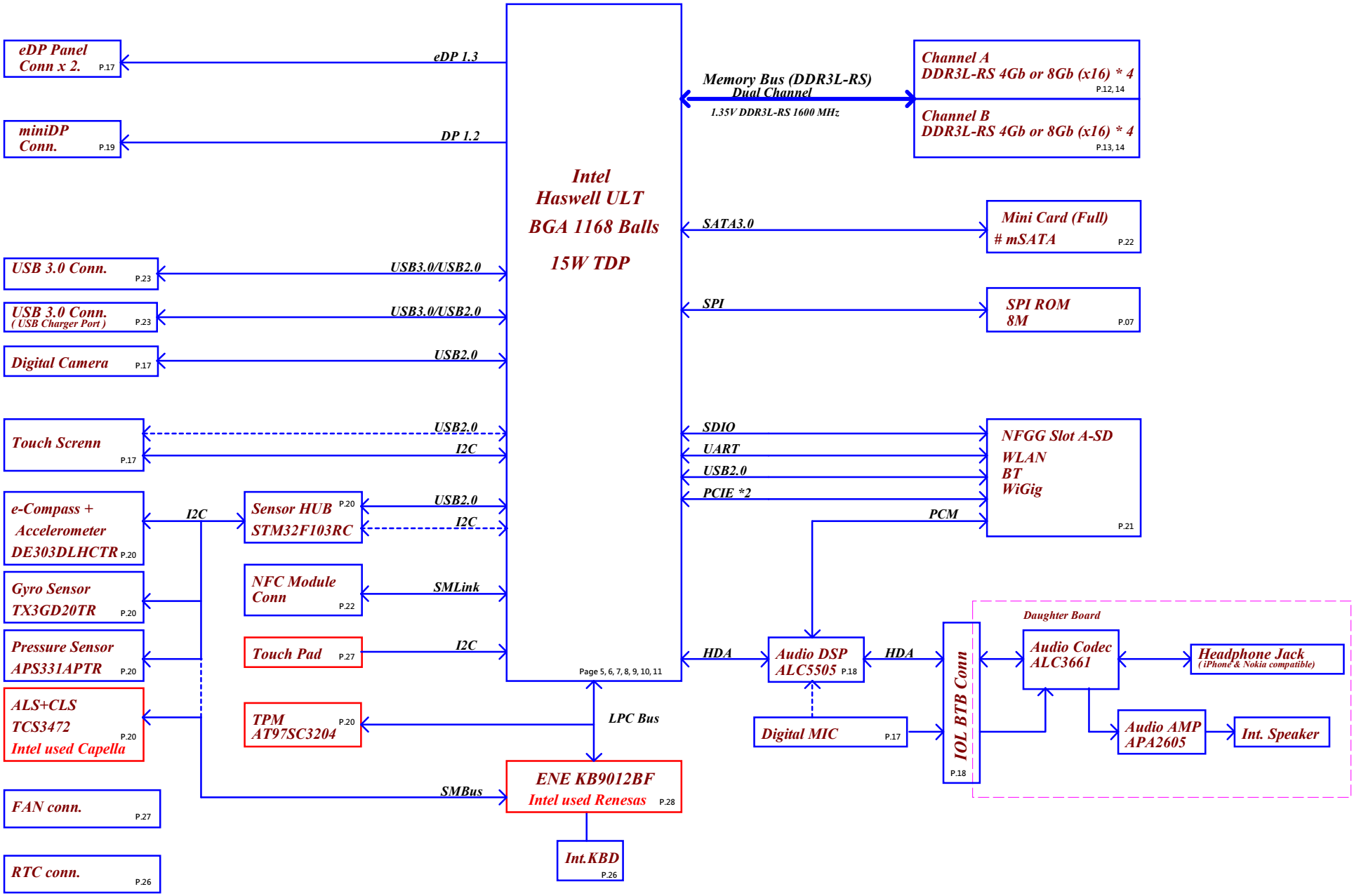
Security Classification	Compal Secret Data		
Issued Date	2011/06/02	Deciphered Date	2013/10/28

Compal Electronics, Inc.

Title: *P01-Cover Page*

Size	Document Number	Rev
	LA-9262P	1.0

Date: Friday, April 19, 2013 Sheet 1 of 45



Security Classification	Compal Secret Data		
Issued Date	2011/02/23	Deciphered Date	2013/10/28

Compal Electronics, Inc.

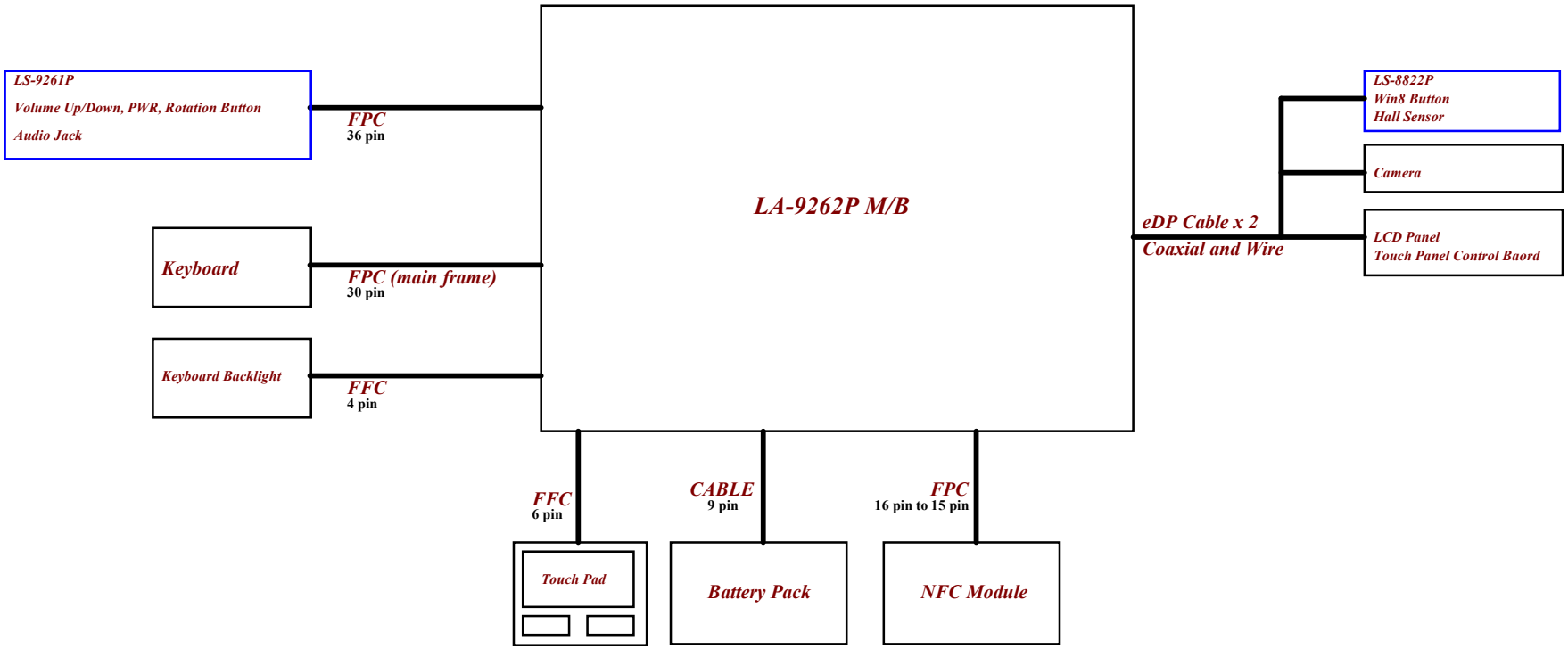
Title: P02-Block Diagram

Size | Document Number: LA-9262P | Rev: 1.0

Date: Friday, April 19, 2013 | Sheet 2 of 45

Compal Confidential

Project Code : VAZA0
File Name : LA-9262P



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Compal Electronics, Inc.

Title: **P03-DaughterB block diagram**

Size	Document Number	Rev
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Board ID Table for AD channel

Vcc	3.3V +/- 5%
Ra	100K +/- 1%

Board ID	Rb	V_{AD_BID} min	V_{AD_BID} typ	V_{AD_BID} max	EC AD3
0	0				
1	12K +/- 1%				
2	15K +/- 1%				
3	20K +/- 1%				
4	27K +/- 1%				
5	33K +/- 1%				
6	43K +/- 1%				
7	56K +/- 1%				
8	75K +/- 1%				
9	100K +/- 1%				
10	130K +/- 1%				
11	160K +/- 1%				
12	200K +/- 1%				
13	240K +/- 1%				
14	270K +/- 1%				
15	330K +/- 1%				
16	430K +/- 1%				
17	560K +/- 1%				
18	750K +/- 1%				
19	NC				

BOARD ID Table

Board ID	PCB Revision
0	CS 0.1
1	CS 0.2
2	CS 0.3
3	CS 0.4
4	CS 0.5
5	CS 1.0
6	
7	
8	
9	
10	Non-CS 0.1
11	Non-CS 0.2
12	Non-CS 0.3
13	Non-CS 0.4
14	Non-CS 1.0
15	
16	
17	
18	
19	

PCH USB Port Mapping

USB PORT#	DESTINATION
0	External USB3
1	External USB3
2	NGFF CARD WLAN
3	Touch Panel
4	Camera
5	Sensors HUB
6	
7	

SMBUS Control Table

	SOURCE	NGFF	BATT	Charger	NFC	XDP	DDR3 SPD	ALS	Touch Pad
EC_SMB_CK1 EC_SMB_DA1	KB9012		V	V					
EC_SMB_CK2 EC_SMB_DA2	KB9012							V	
PCH_SML0CLK PCH_SML0DATA	PCH	V			V				
PCH_SML1CLK PCH_SML1DATA	PCH								
MEM_SMBCLK MEM_SMBDATA	PCH					V	V		V

Link

PCH DDI Port Mapping

DDI PORT#	DESTINATION
B	mini-DP
C	

CLK

DIFFERENTIAL	DESTINATION	FLEX CLOCKS	DESTINATION
CLKOUT_PCIE0		CLKOUT_LPC_0	EC LPC
CLKOUT_PCIE1		CLKOUT_LPC_1	TPM
CLKOUT_PCIE2			
CLKOUT_PCIE3	NGFF CARD WLAN		
CLKOUT_PCIE4			
CLKOUT_PCIE5			

SATA	DESTINATION
SATA0	m-SATA
SATA1	
SATA2	
SATA3	

PCI EXPRESS	DESTINATION
Lane 1	
Lane 2	
Lane 3	NGFF CARD WLAN
Lane 4	NGFF CARD WLAN
Lane 5	
Lane 6	

Symbol Note :

: means Digital Ground

: means Analog Ground

Compal Electronics, Inc.

Title: P04-Notes List

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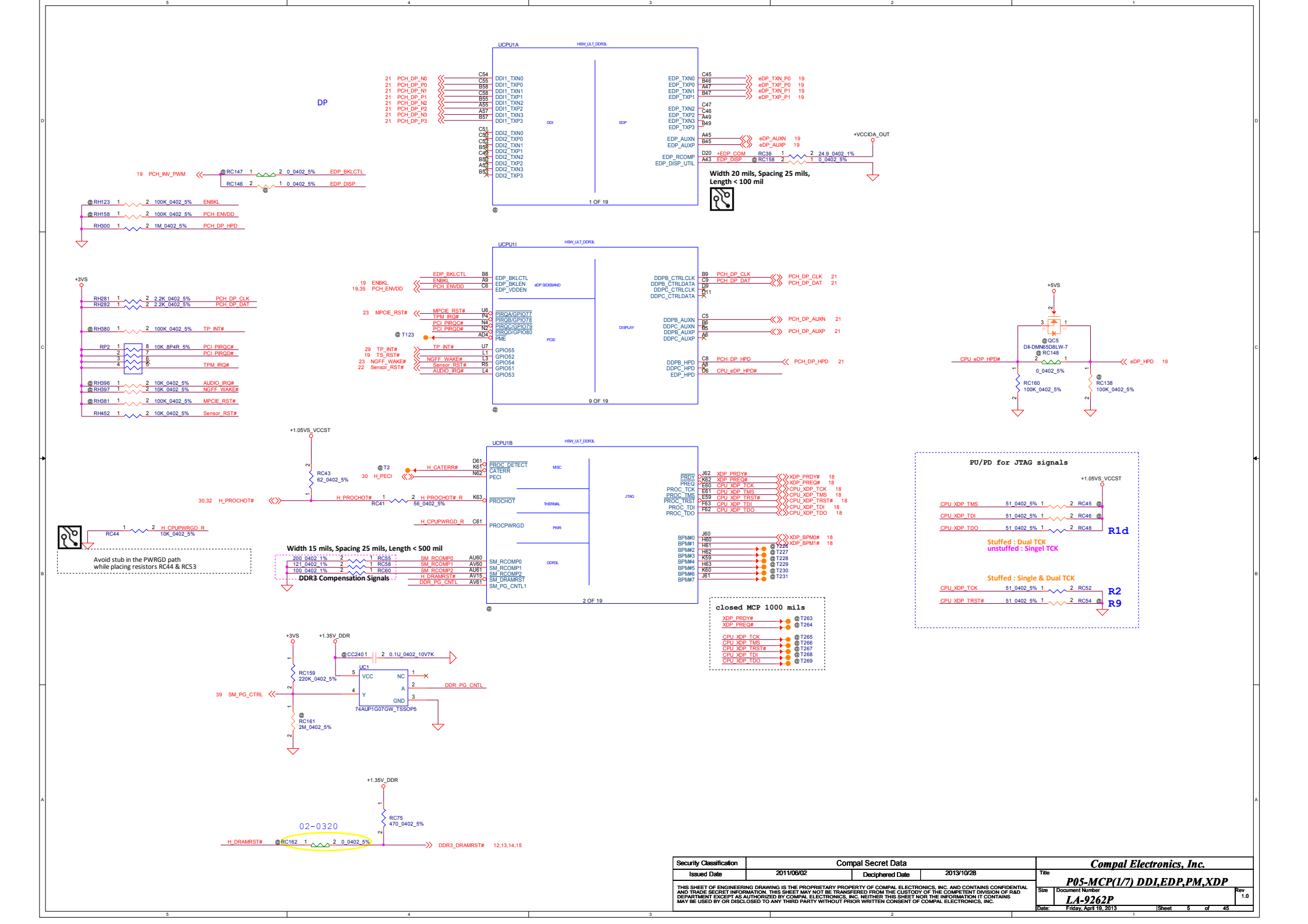

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Issued Date	2011/06/02	Deciphered Date	2013/10/28

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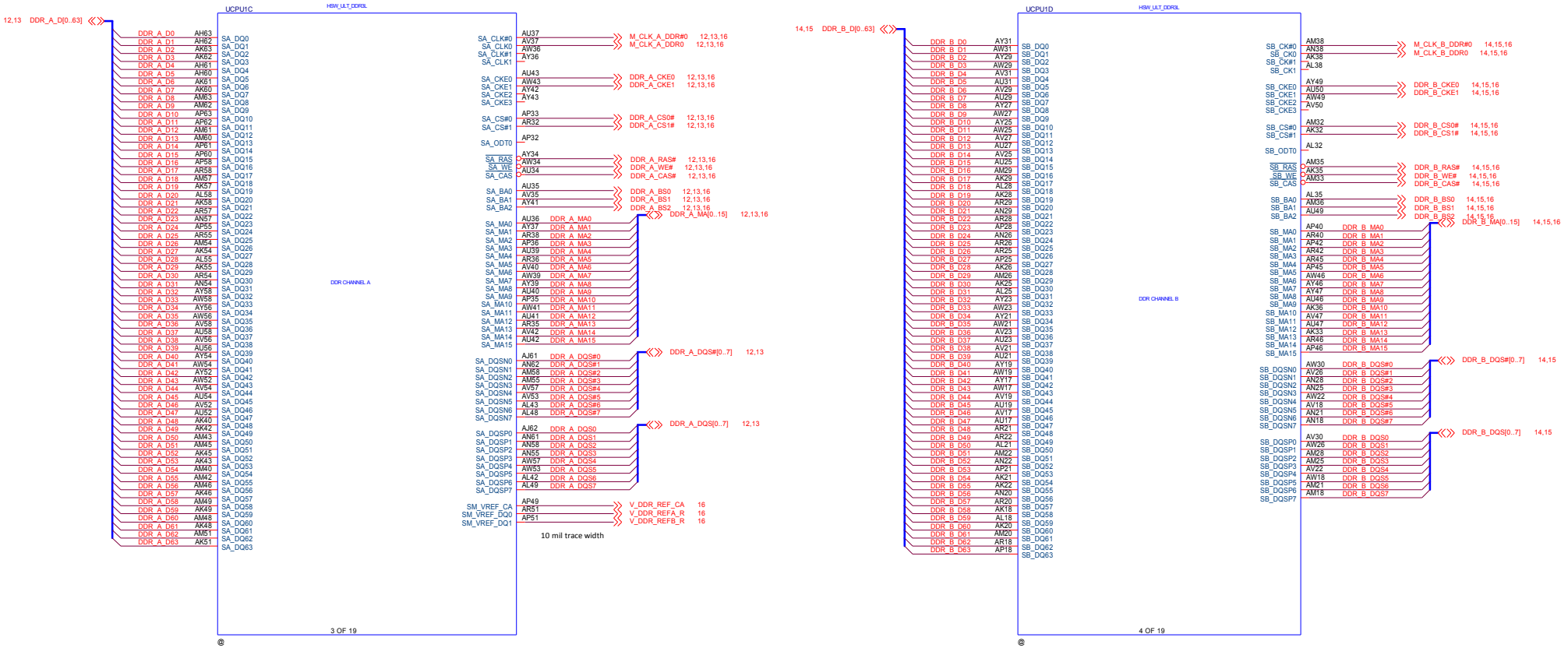
Compal Electronics, Inc.

Title: P05-MCP(1/7) DDI,EDP,PM,XDP

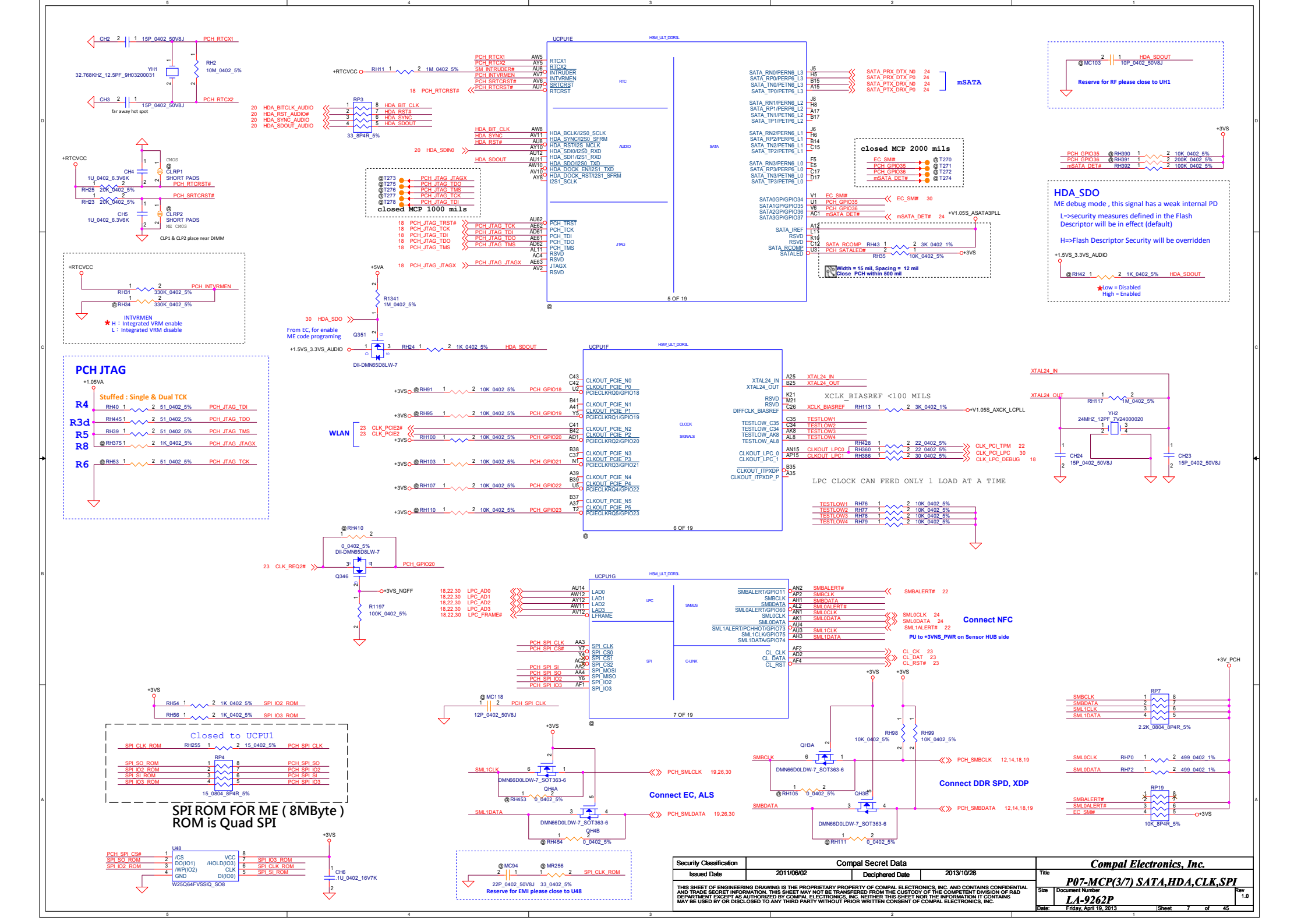
Size	Document Number	Rev
	LA-9262P	1.0

Date: Friday, April 19, 2013 Sheet 5 of 45



Security Classification	Compal Secret Data		
Issued Date	2011/06/02	Deciphered Date	2013/10/28

Compal Electronics, Inc.			
Title	P06-MCP(2/7) DDRIII		
Size	Document Number		Rev
	LA-9262P		1.0
Date:	Friday, April 19, 2013	Sheet 6 of 45	



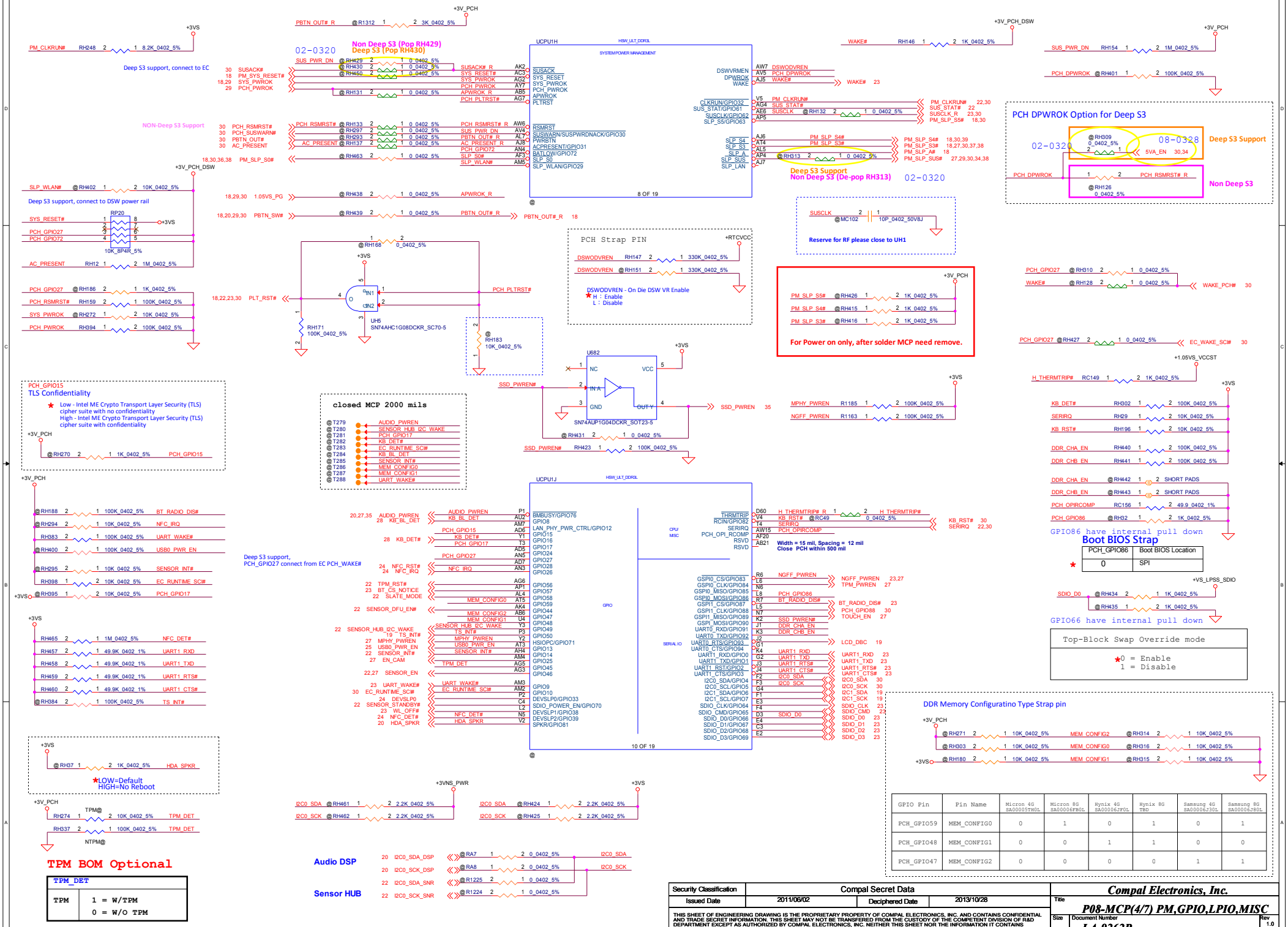
Security Classification	Compal Secret Data		
Issued Date	2011/06/02	Deciphered Date	2013/10/28

Compal Electronics, Inc.

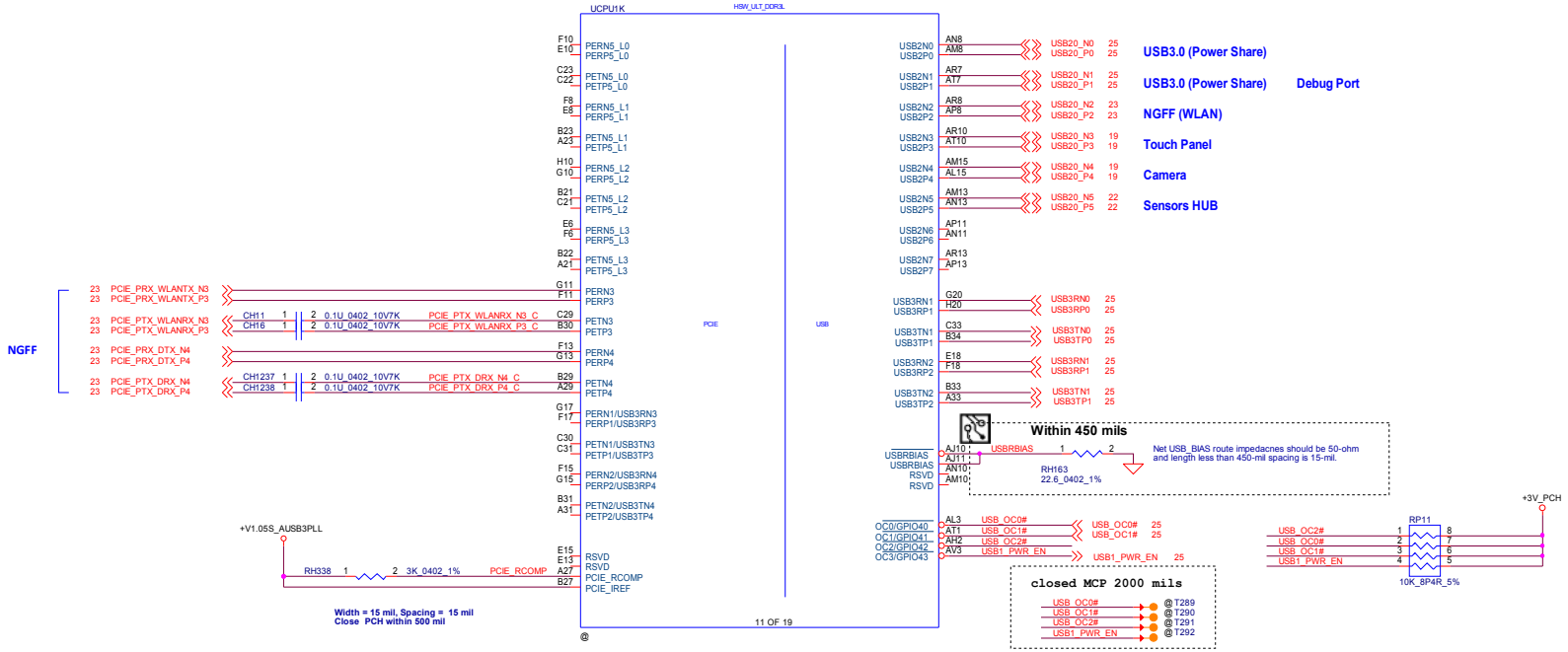
Title: P07-MCP(3/7) SATA,HDA,CLK,SPI

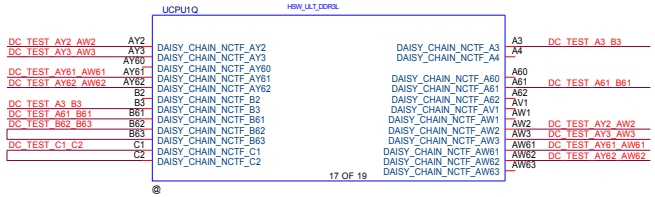
Size	Document Number	Rev
	LA-9262P	1.0

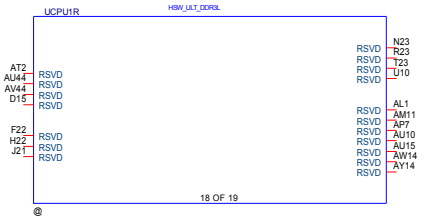
Date: Friday, April 19, 2013 Sheet 7 of 45



GPIO Pin	Pin Name	Micron 4G SA00005TH0L	Micron 8G SA00006FB0L	Hynix 4G SA00006JF0L	Hynix 8G TBD	Samsung 4G SA00006J30L	Samsung 8G SA00006J80L
PCH_GPIO59	MEM_CONFIG0	0	1	0	1	0	1
PCH_GPIO48	MEM_CONFIG1	0	0	1	1	0	0
PCH_GPIO47	MEM_CONFIG2	0	0	0	0	1	1

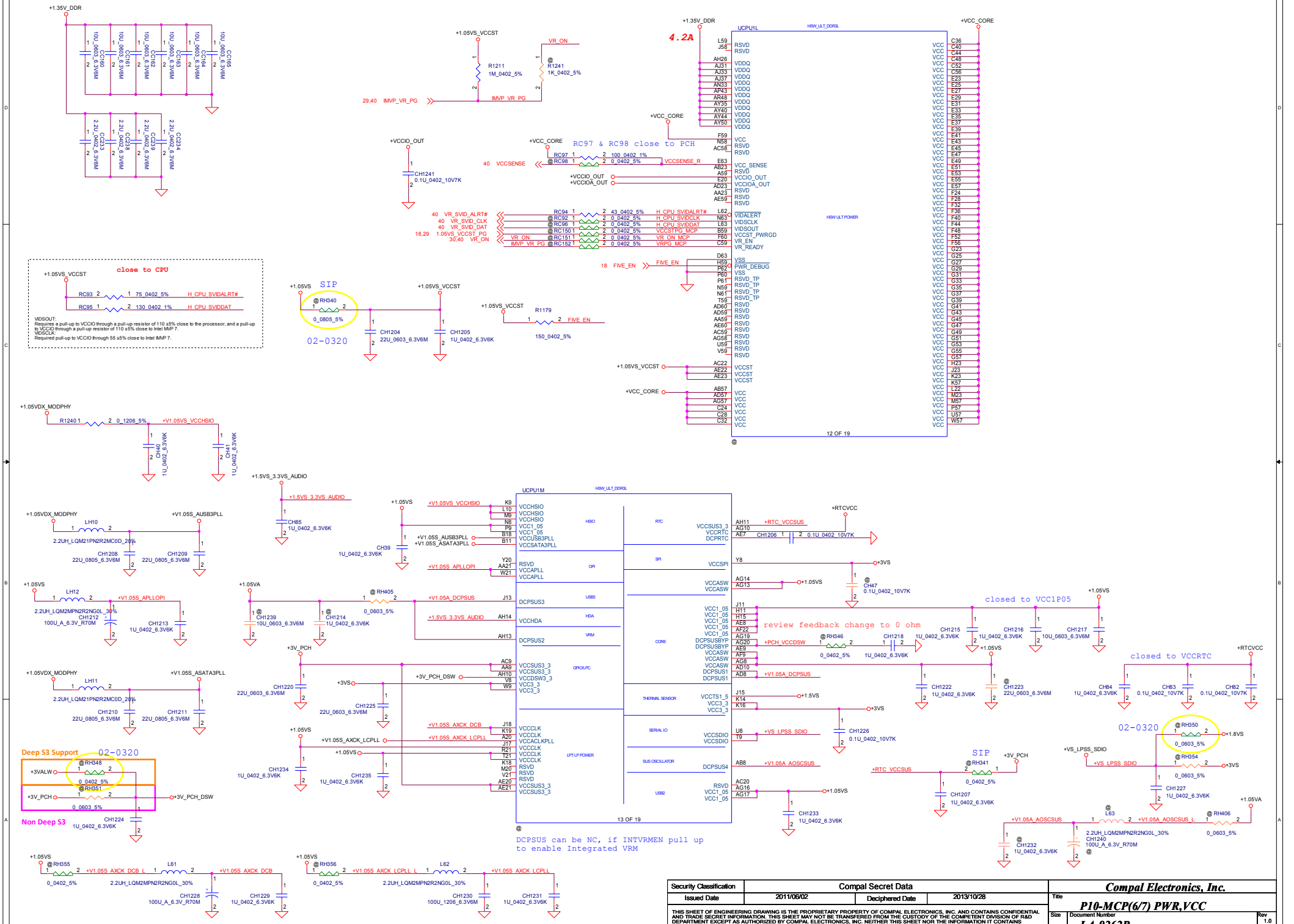






Security Classification	Compal Secret Data		
Issued Date	2011/06/02	Deciphered Date	2013/10/28

Compal Electronics, Inc.			
Title	P09-MCP(5/7) PCIE,USB		
Size	Document Number		Rev
	LA-9262P		1.0
Date:	Friday, April 19, 2013	Sheet	9 of 45



Security Classification	Compal Secret Data		
Issued Date	2011/06/02	Deciphered Date	2013/10/28

Compal Electronics, Inc.

Title: **P10-MCP(6/7) PWR,VCC**

Size	Document Number	Rev
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closed MCP 1000 mils

1K_0402_5% 2 1 RC81 CFG4

eDP Strap	
CFG4	1 : Disabled; No Physical Display Port attached to Embedded Display Port * 0 : Enabled; An external Display Port device is connected to the Embedded Display Port

49.9_0402_1% 2 1 RC153 CFG_RCOMP
49.9_0402_1% 2 1 RC154 PROC_OPI_COMP
8.2K_0402_1% 2 1 RC155 TD_IREF

Width = 15 mil, Spacing = 15 mil
Close PCH within 500 mil

@T293 CFG3

UCPU1S HSW_ULT_DDR3L

18 CFG0 AC60 CFG0
18 CFG1 AC62 CFG1
18 CFG2 AC63 CFG2
18 CFG3 CFG3 AA63 CFG3
18 CFG4 CFG4 AA60 CFG4
18 CFG5 Y62 CFG5
18 CFG6 Y61 CFG6
18 CFG7 Y60 CFG7
18 CFG8 V62 CFG8
18 CFG9 V61 CFG9
18 CFG10 V60 CFG10
18 CFG11 U60 CFG11
18 CFG12 T63 CFG12
18 CFG13 T62 CFG13
18 CFG14 T61 CFG14
18 CFG15 T60 CFG15

18 CFG16 AA62 CFG16
18 CFG18 U63 CFG18
18 CFG17 AA61 CFG17
18 CFG19 U62 CFG19

CFG_RCOMP V63 CFG_RCOMP
A5 RSVD
E1 RSVD
D1 RSVD
J20 RSVD
H18 RSVD
TD_IREF B12 TD_IREF

RESERVED

19 OF 19

RSVD_TP AV63
RSVD_TP AU63
RSVD_TP C63
RSVD_TP C62
RSVD B43
RSVD_TP A51
RSVD_TP B51
RSVD_TP L60
RSVD N60
RSVD W23
RSVD Y22
RSVD AY15 PROC_OPI_COMP
PROC_OPI_RCOMP
RSVD AV62
RSVD D58
VSS P22
VSS N21
RSVD P20
RSVD R20

UCPU1N HSW_ULT_DDR3L

14 OF 19

UCPU1O HSW_ULT_DDR3L

15 OF 19

UCPU1P HSW_ULT_DDR3L

16 OF 19

VSS_SENSE AH16 VSSSENSE_R

RC99 & RC100 close to PCH

@RC99 1 2 0_0402_5% VSSSENSE_R VSSSENSE 40
RC100 1 2 100_0402_1%

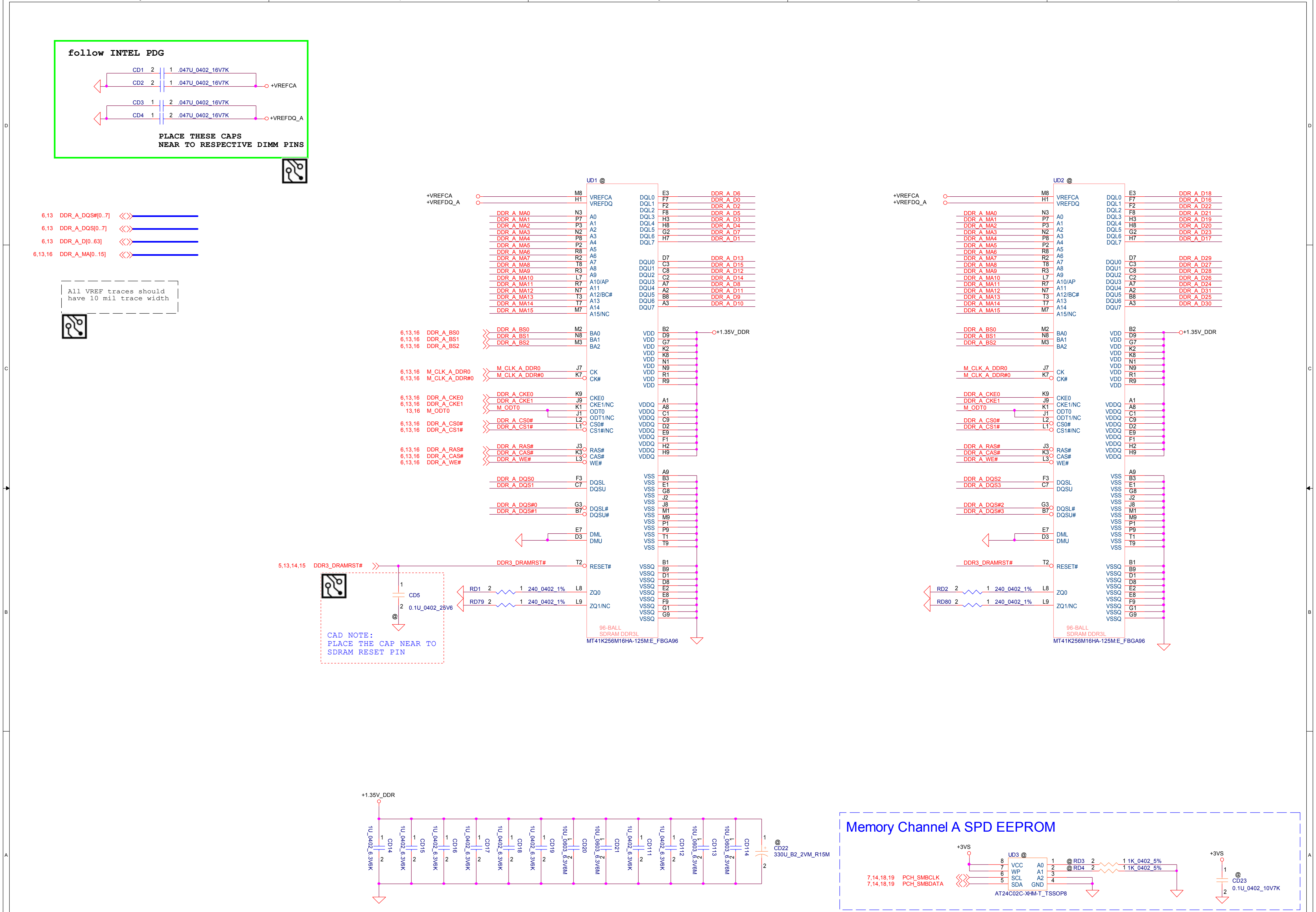
Security Classification	Compal Secret Data		
Issued Date	2011/06/02	Deciphered Date	2013/10/28

Compal Electronics, Inc.

Title: P11-MCP(7/7) PWR,VSS,CFG

Size | Document Number: LA-9262P | Rev: 1.0

Date: Friday, April 19, 2013 | Sheet 11 of 45



Security Classification	Compal Secret Data		
Issued Date	2011/06/02	Deciphered Date	2013/10/28

Compal Electronics, Inc.

Title: **P12-DDRIII Channel_A Lower**

Size | Document Number: **LA-9262P** | Rev 1.0

Date: Friday, April 19, 2013 | Sheet 12 of 45

follow INTEL PDG

CD24 2 1 .047U_0402_16V7K
CD25 2 1 .047U_0402_16V7K +VREFCA
CD26 1 2 .047U_0402_16V7K
CD27 1 2 .047U_0402_16V7K +VREFDQ_A

PLACE THESE CAPS
NEAR TO RESPECTIVE DIMM PINS

6,12 DDR_A_DQS#[0..7]
6,12 DDR_A_DQS[0..7]
6,12 DDR_A_D[0..63]
6,12,16 DDR_A_MA[0..15]

All VREF traces should have 10 mil trace width

UD4 @ / UD5 @ — MT41K256M16HA-125M:E_FBGA96 (96-BALL SDRAM DDR3L)

+VREFCA, +VREFDQ_A → VREFCA, VREFDQ
DDR_A_MA0..MA15 → A0..A15 / A15/NC
DDR_A_BS0..BS2 → BA0..BA2
M_CLK_A_DDR0, M_CLK_A_DDR#0 → CK, CK#
DDR_A_CKE0, DDR_A_CKE1, M_ODT0 → CKE0, CKE1/NC, ODT0, ODT1/NC
DDR_A_CS0#, DDR_A_CS1# → CS0#, CS1#/NC
DDR_A_RAS#, DDR_A_CAS#, DDR_A_WE# → RAS#, CAS#, WE#
DDR_A_DQS4, DDR_A_DQS5 → DQSL, DQSU
DDR_A_DQS#4, DDR_A_DQS#5 → DQSL#, DQSU#
DDR_A_DQS6, DDR_A_DQS7 → DQSL, DQSU
DDR_A_DQS#6, DDR_A_DQS#7 → DQSL#, DQSU#
DDR_A_D0..D63 → DQL0..DQL7, DQU0..DQU7
VDD, VDDQ → +1.35V_DDR
DDR3_DRAMRST# → RESET#
RD5 240_0402_1% → ZQ0
RD81 240_0402_1% → ZQ1/NC
RD6 240_0402_1% → ZQ0
RD82 240_0402_1% → ZQ1/NC

CAD NOTE:
PLACE THE CAP NEAR TO
SDRAM RESET PIN

CD28 0.1U_0402_25V6

+1.35V_DDR
CD37 1U_0402_6.3V6K
CD38 1U_0402_6.3V6K
CD39 1U_0402_6.3V6K
CD40 1U_0402_6.3V6K
CD41 1U_0402_6.3V6K
CD42 1U_0402_6.3V6K
CD43 10U_0603_6.3V6M
CD44 10U_0603_6.3V6M
CD115 1U_0402_6.3V6K
CD116 10U_0603_6.3V6M
CD117 10U_0603_6.3V6M
CD118

Security Classification	Compal Secret Data		
Issued Date	2011/06/02	Deciphered Date	2013/10/28

Compal Electronics, Inc.

Title: P13-DDRIII Channel_A Upper

Size | Document Number: LA-9262P | Rev: 1.0

Date: Friday, April 19, 2013 | Sheet 13 of 45

follow INTEL PDG

CD45 2 — 1 .047U_0402_16V7K
CD46 2 — 1 .047U_0402_16V7K — +VREFCA
CD47 1 — 2 .047U_0402_16V7K
CD48 1 — 2 .047U_0402_16V7K — +VREFDQ_B

PLACE THESE CAPS
NEAR TO RESPECTIVE DIMM PINS

6,15 DDR_B_DQS#[0..7]
6,15 DDR_B_DQS[0..7]
6,15 DDR_B_D[0..63]
6,15,16 DDR_B_MA[0..15]

All VREF traces should have 10 mil trace width

UD6 @ — MT41K256M16HA-125M:E_FBGA96
UD7 @ — MT41K256M16HA-125M:E_FBGA96

+VREFCA, +VREFDQ_B
DDR_B_MA0..MA15
DDR_B_BS0..BS2
M_CLK_B_DDR0, M_CLK_B_DDR#0
DDR_B_CKE0, DDR_B_CKE1, M_ODT2
DDR_B_CS0#, DDR_B_CS1#
DDR_B_RAS#, DDR_B_CAS#, DDR_B_WE#
DDR_B_DQS2, DDR_B_DQS3, DDR_B_DQS#2, DDR_B_DQS#3
DDR_B_D0..D63
+1.35V_DDR
5,12,13,15 DDR3_DRAMRST#
RD7 2 — 1 240_0402_1% — ZQ0
RD83 2 — 1 240_0402_1% — ZQ1/NC
96-BALL SDRAM DDR3L

CAD NOTE:
PLACE THE CAP NEAR TO SDRAM RESET PIN

CD49 0.1U_0402_25V6 @

+1.35V_DDR
CD59 1U_0402_6.3V6K
CD60 1U_0402_6.3V6K
CD61 1U_0402_6.3V6K
CD62 1U_0402_6.3V6K
CD63 1U_0402_6.3V6K
CD64 10U_0603_6.3V6M
CD65 10U_0603_6.3V6M
CD119 1U_0402_6.3V6K
CD120 1U_0402_6.3V6K
CD121 10U_0603_6.3V6M
CD122 10U_0603_6.3V6M
CD66 @ 330U_B2_2VM_R15M

Memory Channel B SPD EEPROM

+3VS
UD8 @ — AT24C02C-XHM-T_TSSOP8
VCC, WP, SCL, SDA; A0, A1, A2, GND
7,12,18,19 PCH_SMBCLK
7,12,18,19 PCH_SMBDATA
@RD9 2 — 1 1K_0402_5%
@RD10 2 — 1 1K_0402_5%
+3VS
+3VS
CD67 @ 0.1U_0402_10V7K

Security Classification	Compal Secret Data		
Issued Date	2011/06/02	Deciphered Date	2013/10/28

Compal Electronics, Inc.

Title: P14-DDRIII Channel_B Lower

Size | Document Number: LA-9262P | Rev: 1.0

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follow INTEL PDG

CD68 2 1 .047U_0402_16V7K
CD69 2 1 .047U_0402_16V7K +VREFCA

CD70 1 2 .047U_0402_16V7K
CD71 1 2 .047U_0402_16V7K +VREFDQ_B

PLACE THESE CAPS
NEAR TO RESPECTIVE DIMM PINS

6,14 DDR_B_DQS#[0..7]
6,14 DDR_B_DQS[0..7]
6,14 DDR_B_D[0..63]
6,14,16 DDR_B_MA[0..15]

All VREF traces should
have 10 mil trace width

UD9 @

+VREFCA
+VREFDQ_B
M8 VREFCA
H1 VREFDQ

DDR_B_MA0 N3 A0
DDR_B_MA1 P7 A1
DDR_B_MA2 P3 A2
DDR_B_MA3 N2 A3
DDR_B_MA4 P8 A4
DDR_B_MA5 P2 A5
DDR_B_MA6 R8 A6
DDR_B_MA7 R2 A7
DDR_B_MA8 T8 A8
DDR_B_MA9 R3 A9
DDR_B_MA10 L7 A10/AP
DDR_B_MA11 R7 A11
DDR_B_MA12 N7 A12/BC#
DDR_B_MA13 T3 A13
DDR_B_MA14 T7 A14
DDR_B_MA15 M7 A15/NC

6,14,16 DDR_B_BS0 DDR_B_BS0 M2 BA0
6,14,16 DDR_B_BS1 DDR_B_BS1 N8 BA1
6,14,16 DDR_B_BS2 DDR_B_BS2 M3 BA2

6,14,16 M_CLK_B_DDR0 M_CLK_B_DDR0 J7 CK
6,14,16 M_CLK_B_DDR#0 M_CLK_B_DDR#0 K7 CK#

6,14,16 DDR_B_CKE0 DDR_B_CKE0 K9 CKE0
6,14,16 DDR_B_CKE1 DDR_B_CKE1 J9 CKE1/NC
14,16 M_ODT2 M_ODT2 K1 ODT0
J1 ODT1/NC

6,14,16 DDR_B_CS0# DDR_B_CS0# L2 CS0#
6,14,16 DDR_B_CS1# DDR_B_CS1# L1 CS1#/NC

6,14,16 DDR_B_RAS# DDR_B_RAS# J3 RAS#
6,14,16 DDR_B_CAS# DDR_B_CAS# K3 CAS#
6,14,16 DDR_B_WE# DDR_B_WE# L3 WE#

DDR_B_DQS4 F3 DQSL
DDR_B_DQS5 C7 DQSU

DDR_B_DQS#4 G3 DQSL#
DDR_B_DQS#5 B7 DQSU#

E7 DML
D3 DMU

5,12,13,14 DDR3_DRAMRST# DDR3_DRAMRST# T2 RESET#

RD11 2 1 240_0402_1% L8 ZQ0
RD85 2 1 240_0402_1% L9 ZQ1/NC

@ CD72 0.1U_0402_25V6

CAD NOTE:
PLACE THE CAP NEAR TO
SDRAM RESET PIN

DQL0 E3 DDR_B_D39
DQL1 F7 DDR_B_D33
DQL2 F2 DDR_B_D38
DQL3 F8 DDR_B_D37
DQL4 H3 DDR_B_D34
DQL5 H8 DDR_B_D32
DQL6 G2 DDR_B_D35
DQL7 H7 DDR_B_D36

D7 DDR_B_D45
DQU0 C3 DDR_B_D47
DQU1 C8 DDR_B_D44
DQU2 C2 DDR_B_D42
DQU3 A7 DDR_B_D40
DQU4 A2 DDR_B_D46
DQU5 B8 DDR_B_D41
DQU6 A3 DDR_B_D43
DQU7

VDD B2 +1.35V_DDR
VDD D9
VDD G7
VDD K2
VDD K8
VDD N1
VDD N9
VDD R1
VDD R9

VDDQ A1
VDDQ A8
VDDQ C1
VDDQ C9
VDDQ D2
VDDQ E9
VDDQ F1
VDDQ H2
VDDQ H9

VSS A9
VSS B3
VSS E1
VSS G8
VSS J2
VSS J8
VSS M1
VSS M9
VSS P1
VSS P9
VSS T1
VSS T9

VSSQ B1
VSSQ B9
VSSQ D1
VSSQ D8
VSSQ E2
VSSQ E8
VSSQ F9
VSSQ G1
VSSQ G9

96-BALL
SDRAM DDR3L
MT41K256M16HA-125M:E_FBGA96

UD10 @

+VREFCA
+VREFDQ_B
M8 VREFCA
H1 VREFDQ

DDR_B_MA0 N3 A0
DDR_B_MA1 P7 A1
DDR_B_MA2 P3 A2
DDR_B_MA3 N2 A3
DDR_B_MA4 P8 A4
DDR_B_MA5 P2 A5
DDR_B_MA6 R8 A6
DDR_B_MA7 R2 A7
DDR_B_MA8 T8 A8
DDR_B_MA9 R3 A9
DDR_B_MA10 L7 A10/AP
DDR_B_MA11 R7 A11
DDR_B_MA12 N7 A12/BC#
DDR_B_MA13 T3 A13
DDR_B_MA14 T7 A14
DDR_B_MA15 M7 A15/NC

DDR_B_BS0 M2 BA0
DDR_B_BS1 N8 BA1
DDR_B_BS2 M3 BA2

M_CLK_B_DDR0 J7 CK
M_CLK_B_DDR#0 K7 CK#

DDR_B_CKE0 K9 CKE0
DDR_B_CKE1 J9 CKE1/NC
M_ODT2 K1 ODT0
J1 ODT1/NC

DDR_B_CS0# L2 CS0#
DDR_B_CS1# L1 CS1#/NC

DDR_B_RAS# J3 RAS#
DDR_B_CAS# K3 CAS#
DDR_B_WE# L3 WE#

DDR_B_DQS6 F3 DQSL
DDR_B_DQS7 C7 DQSU

DDR_B_DQS#6 G3 DQSL#
DDR_B_DQS#7 B7 DQSU#

E7 DML
D3 DMU

DDR3_DRAMRST# T2 RESET#

RD12 2 1 240_0402_1% L8 ZQ0
RD86 2 1 240_0402_1% L9 ZQ1/NC

DQL0 E3 DDR_B_D48
DQL1 F7 DDR_B_D52
DQL2 F2 DDR_B_D50
DQL3 F8 DDR_B_D55
DQL4 H3 DDR_B_D53
DQL5 H8 DDR_B_D51
DQL6 G2 DDR_B_D54
DQL7 H7 DDR_B_D49

D7 DDR_B_D60
DQU0 C3 DDR_B_D62
DQU1 C8 DDR_B_D61
DQU2 C2 DDR_B_D63
DQU3 A7 DDR_B_D57
DQU4 A2 DDR_B_D58
DQU5 B8 DDR_B_D56
DQU6 A3 DDR_B_D59
DQU7

VDD B2 +1.35V_DDR
VDD D9
VDD G7
VDD K2
VDD K8
VDD N1
VDD N9
VDD R1
VDD R9

VDDQ A1
VDDQ A8
VDDQ C1
VDDQ C9
VDDQ D2
VDDQ E9
VDDQ F1
VDDQ H2
VDDQ H9

VSS A9
VSS B3
VSS E1
VSS G8
VSS J2
VSS J8
VSS M1
VSS M9
VSS P1
VSS P9
VSS T1
VSS T9

VSSQ B1
VSSQ B9
VSSQ D1
VSSQ D8
VSSQ E2
VSSQ E8
VSSQ F9
VSSQ G1
VSSQ G9

96-BALL
SDRAM DDR3L
MT41K256M16HA-125M:E_FBGA96

+1.35V_DDR

CD81 1U_0402_6.3V6K
CD82 1U_0402_6.3V6K
CD83 1U_0402_6.3V6K
CD84 1U_0402_6.3V6K
CD85 1U_0402_6.3V6K
CD86 1U_0402_6.3V6K
CD87 10U_0603_6.3V6M
CD88 10U_0603_6.3V6M
CD123 1U_0402_6.3V6K
CD124 1U_0402_6.3V6K
CD125 10U_0603_6.3V6M
CD126 10U_0603_6.3V6M

Security Classification	Compal Secret Data		
Issued Date	2011/06/02	Deciphered Date	2013/10/28

Compal Electronics, Inc.

Title: P15-DDRIII Channel_B Upper

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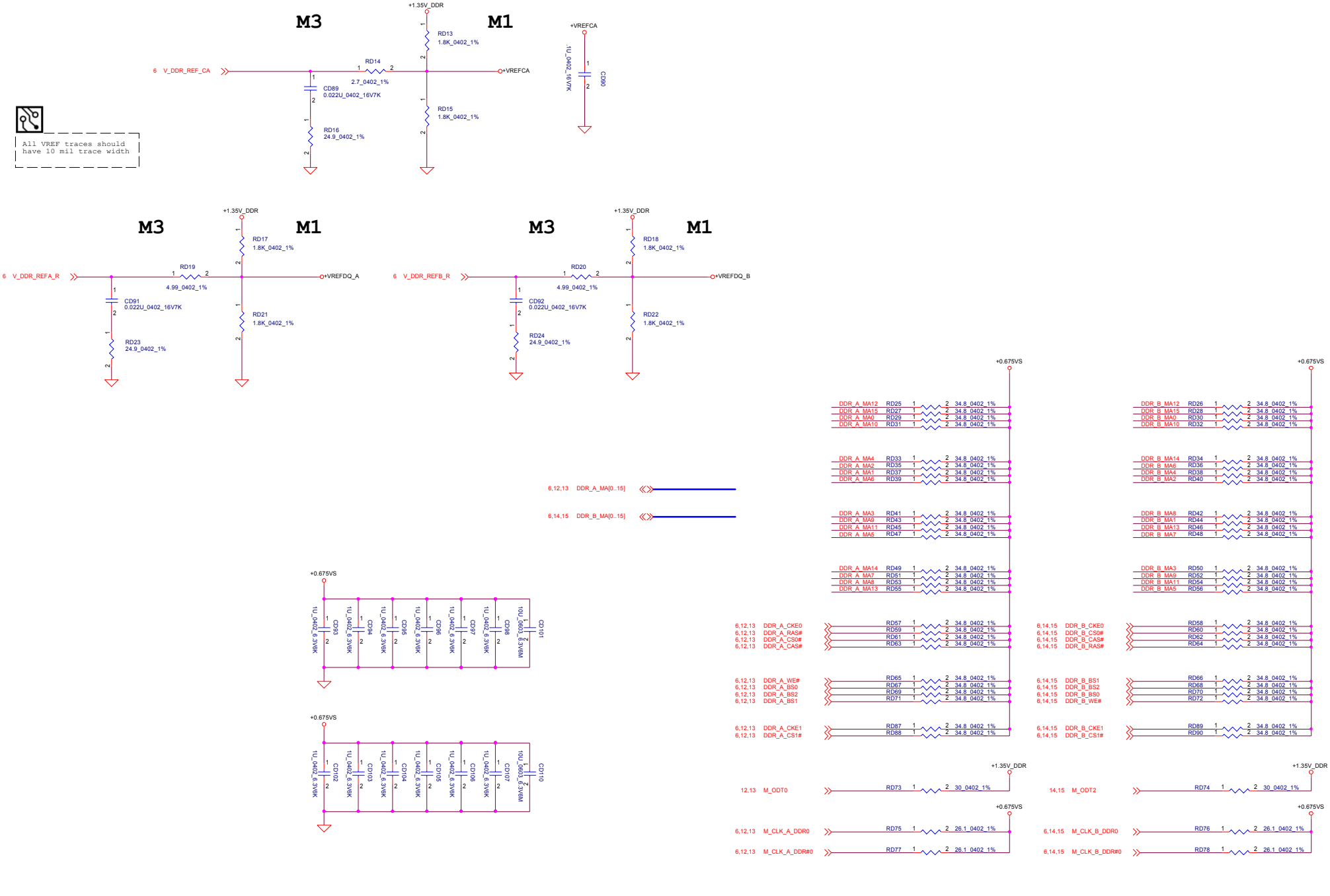

Security Classification	Compal Secret Data		
Issued Date	2011/06/02	Deciphered Date	2013/10/28

Compal Electronics, Inc.

Title: **P16-DDRIII Vref & Termination**

Size	Document Number	Rev
	LA-9262P	1.0

Date: Friday, April 19, 2013 Sheet 16 of 45

UCPU1 CPU_1.7G_GT3@
SA00006SS1L
I7-4650U

UCPU1 CPU_1.8G_GT2@
SA00006SL1L
I7-4500U

UCPU1 CPU_1.6G_GT2@
SA00006SM2L
I5-4200U

UCPU1 CPU_1.7G_GT2@
SA00006SX1L
I3-4010U

MEM_CONFIG2 MEM_CONFIG1 MEM_CONFIG0

X768G
X7641131L61
X76_8G@

X764G
X7641131L57
X76_4G@

	UD1	UD2	UD4	UD5	UD6	UD7	UD9	UD10	RH314	RH315	RH316
Micron_4G@	SA00005TH0L MT41K256M16HA-125M:E	SA00005TH0L MT41K256M16HA-125M:E	SA00005TH0L MT41K256M16HA-125M:E	SA00005TH0L MT41K256M16HA-125M:E	SA00005TH0L MT41K256M16HA-125M:E	SA00005TH0L MT41K256M16HA-125M:E	SA00005TH0L MT41K256M16HA-125M:E	SA00005TH0L MT41K256M16HA-125M:E	SD028100280 10K_0402_5%	SD028100280 10K_0402_5%	SD028100280 10K_0402_5%
Micron_8G@	SA00006FB0L MT41K512M16TNA-125M:E	SA00006FB0L MT41K512M16TNA-125M:E	SA00006FB0L MT41K512M16TNA-125M:E	SA00006FB0L MT41K512M16TNA-125M:E	SA00006FB0L MT41K512M16TNA-125M:E	SA00006FB0L MT41K512M16TNA-125M:E	SA00006FB0L MT41K512M16TNA-125M:E	SA00006FB0L MT41K512M16TNA-125M:E	SD028100280 10K_0402_5%	SD028100280 10K_0402_5%	SD028100280 10K_0402_5%
Hynix_4G@	SA00006JF0L H5TC4G63AFR-PBR	SA00006JF0L H5TC4G63AFR-PBR	SA00006JF0L H5TC4G63AFR-PBR	SA00006JF0L H5TC4G63AFR-PBR	SA00006JF0L H5TC4G63AFR-PBR	SA00006JF0L H5TC4G63AFR-PBR	SA00006JF0L H5TC4G63AFR-PBR	SA00006JF0L H5TC4G63AFR-PBR	SD028100280 10K_0402_5%	SD028100280 10K_0402_5%	SD028100280 10K_0402_5%
Hynix_8G@	SA00006Q90L H5TC8G63AMR-PBR	SA00006Q90L H5TC8G63AMR-PBR	SA00006Q90L H5TC8G63AMR-PBR	SA00006Q90L H5TC8G63AMR-PBR	SA00006Q90L H5TC8G63AMR-PBR	SA00006Q90L H5TC8G63AMR-PBR	SA00006Q90L H5TC8G63AMR-PBR	SA00006Q90L H5TC8G63AMR-PBR	SD028100280 10K_0402_5%	SD028100280 10K_0402_5%	SD028100280 10K_0402_5%
Samsung_4G@	SA00006J30L K4B4G1646B-HKK0	SA00006J30L K4B4G1646B-HKK0	SA00006J30L K4B4G1646B-HKK0	SA00006J30L K4B4G1646B-HKK0	SA00006J30L K4B4G1646B-HKK0	SA00006J30L K4B4G1646B-HKK0	SA00006J30L K4B4G1646B-HKK0	SA00006J30L K4B4G1646B-HKK0	SD028100280 10K_0402_5%	SD028100280 10K_0402_5%	SD028100280 10K_0402_5%
Samsung_8G@	SA00006J80L K4B8G1646B-MKK0	SA00006J80L K4B8G1646B-MKK0	SA00006J80L K4B8G1646B-MKK0	SA00006J80L K4B8G1646B-MKK0	SA00006J80L K4B8G1646B-MKK0	SA00006J80L K4B8G1646B-MKK0	SA00006J80L K4B8G1646B-MKK0	SA00006J80L K4B8G1646B-MKK0	SD028100280 10K_0402_5%	SD028100280 10K_0402_5%	SD028100280 10K_0402_5%

	UD1	UD2	UD4	UD5	UD6	UD7	UD9	UD10	RH314	RH180	RH316
Hynix_4G@	SA00006JF0L H5TC4G63AFR-PBR	SA00006JF0L H5TC4G63AFR-PBR	SA00006JF0L H5TC4G63AFR-PBR	SA00006JF0L H5TC4G63AFR-PBR	SA00006JF0L H5TC4G63AFR-PBR	SA00006JF0L H5TC4G63AFR-PBR	SA00006JF0L H5TC4G63AFR-PBR	SA00006JF0L H5TC4G63AFR-PBR	SD028100280 10K_0402_5%	SD028100280 10K_0402_5%	SD028100280 10K_0402_5%
Hynix_8G@	SA00006Q90L H5TC8G63AMR-PBR	SA00006Q90L H5TC8G63AMR-PBR	SA00006Q90L H5TC8G63AMR-PBR	SA00006Q90L H5TC8G63AMR-PBR	SA00006Q90L H5TC8G63AMR-PBR	SA00006Q90L H5TC8G63AMR-PBR	SA00006Q90L H5TC8G63AMR-PBR	SA00006Q90L H5TC8G63AMR-PBR	SD028100280 10K_0402_5%	SD028100280 10K_0402_5%	SD028100280 10K_0402_5%

	UD1	UD2	UD4	UD5	UD6	UD7	UD9	UD10	RH271	RH315	RH316
Samsung_4G@	SA00006J30L K4B4G1646B-HKK0	SA00006J30L K4B4G1646B-HKK0	SA00006J30L K4B4G1646B-HKK0	SA00006J30L K4B4G1646B-HKK0	SA00006J30L K4B4G1646B-HKK0	SA00006J30L K4B4G1646B-HKK0	SA00006J30L K4B4G1646B-HKK0	SA00006J30L K4B4G1646B-HKK0	SD028100280 10K_0402_5%	SD028100280 10K_0402_5%	SD028100280 10K_0402_5%
Samsung_8G@	SA00006J80L K4B8G1646B-MKK0	SA00006J80L K4B8G1646B-MKK0	SA00006J80L K4B8G1646B-MKK0	SA00006J80L K4B8G1646B-MKK0	SA00006J80L K4B8G1646B-MKK0	SA00006J80L K4B8G1646B-MKK0	SA00006J80L K4B8G1646B-MKK0	SA00006J80L K4B8G1646B-MKK0	SD028100280 10K_0402_5%	SD028100280 10K_0402_5%	SD028100280 10K_0402_5%

	UD1	UD2	UD4	UD5	UD6	UD7	UD9	UD10	RH303
Micron_8G@	SA00006FB0L MT41K512M16TNA-125M:E	SA00006FB0L MT41K512M16TNA-125M:E	SA00006FB0L MT41K512M16TNA-125M:E	SA00006FB0L MT41K512M16TNA-125M:E	SA00006FB0L MT41K512M16TNA-125M:E	SA00006FB0L MT41K512M16TNA-125M:E	SA00006FB0L MT41K512M16TNA-125M:E	SA00006FB0L MT41K512M16TNA-125M:E	SD028100280 10K_0402_5%
Hynix_8G@	SA00006Q90L H5TC8G63AMR-PBR	SA00006Q90L H5TC8G63AMR-PBR	SA00006Q90L H5TC8G63AMR-PBR	SA00006Q90L H5TC8G63AMR-PBR	SA00006Q90L H5TC8G63AMR-PBR	SA00006Q90L H5TC8G63AMR-PBR	SA00006Q90L H5TC8G63AMR-PBR	SA00006Q90L H5TC8G63AMR-PBR	SD028100280 10K_0402_5%
Samsung_8G@	SA00006J80L K4B8G1646B-MKK0	SA00006J80L K4B8G1646B-MKK0	SA00006J80L K4B8G1646B-MKK0	SA00006J80L K4B8G1646B-MKK0	SA00006J80L K4B8G1646B-MKK0	SA00006J80L K4B8G1646B-MKK0	SA00006J80L K4B8G1646B-MKK0	SA00006J80L K4B8G1646B-MKK0	SD028100280 10K_0402_5%

Security Classification	Compal Secret Data		
Issued Date	2011/06/02	Deciphered Date	2013/10/28

Compal Electronics, Inc.

Title: P17-BOM

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U663 200ps of XDP

03-0320

Topolog	Description	Be st Use for	Resistors Stuffed	Resistors ufStuffed
Default Setting: Dual TCK S can Chains (also known as "Shared JTAG" in other docum ent)	In this topology, the CPU JTAG chain will be controlled by TCK0 and TCK1 will control the PCH JTAG chain.	- Run control oper. - ME/Sx debug	R1, R2, J1d, J2d, J3d, J4d, R3, R4, R5	J1s, J2s, J3s
Single TCK scan chain (also known as "Com m on JTAG" in other docum ent)	In th is topolog y, PCH TDI- TDO and CPU TDI-TDO will be chained to form one JTAG scan chain controlled by TCK0	-B oundary Scan/ Manufacturing est	J1s , J2s , J3s , R2, R3, R4, R5	R1, J1d, J2d, J3d , J4d

J1D, J1S <200ps of the XDP Stub<200ps

J2D, J2S <200ps of the XDP Stub <200ps

J3D, J3S, R3 <200ps of the XDP Stub <200ps

J4D <200ps of the XDP

TCK0, TCK1 and TMS stub <200ps

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Issued Date	2011/06/02
Deciphered Date	2013/10/28

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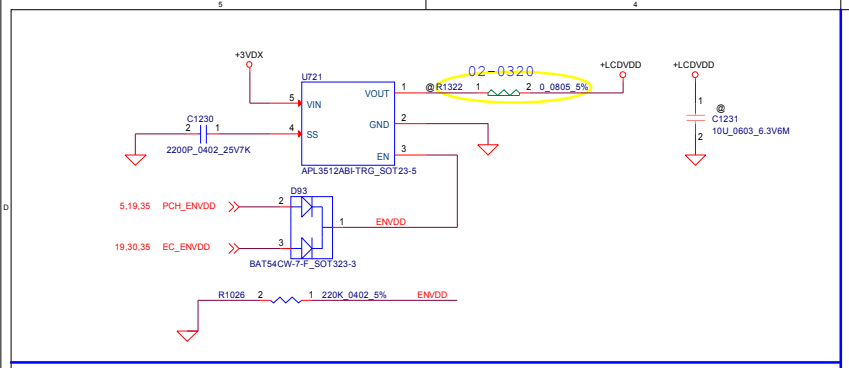
Compal Electronics, Inc.

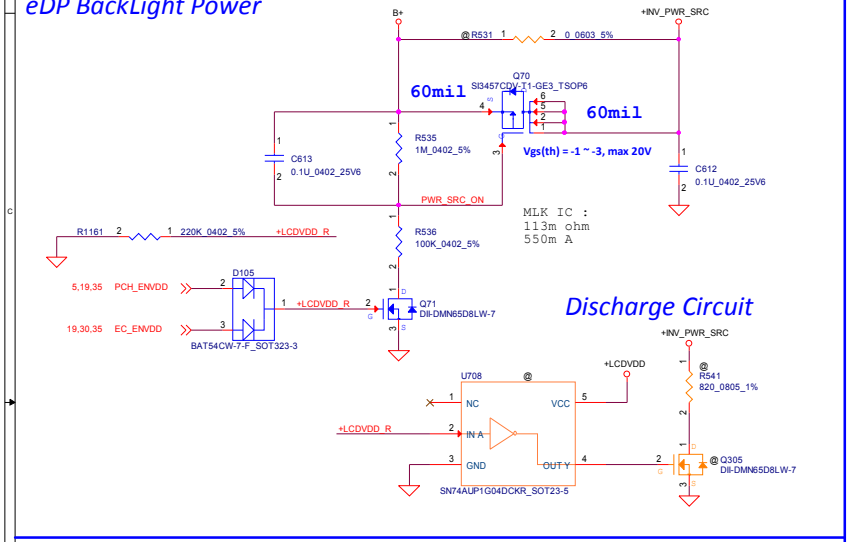
Title: P18-XDP,APS,Debug CONN

Size: | Document Number: LA-9262P | Rev: 1.0

Date: Friday, April 19, 2013 | Sheet 18 of 45

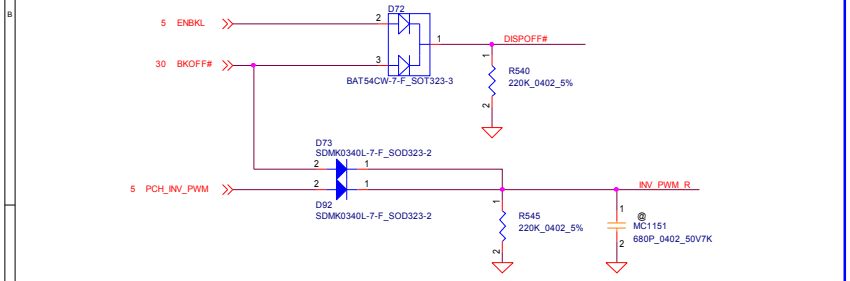


eDP BackLight Power

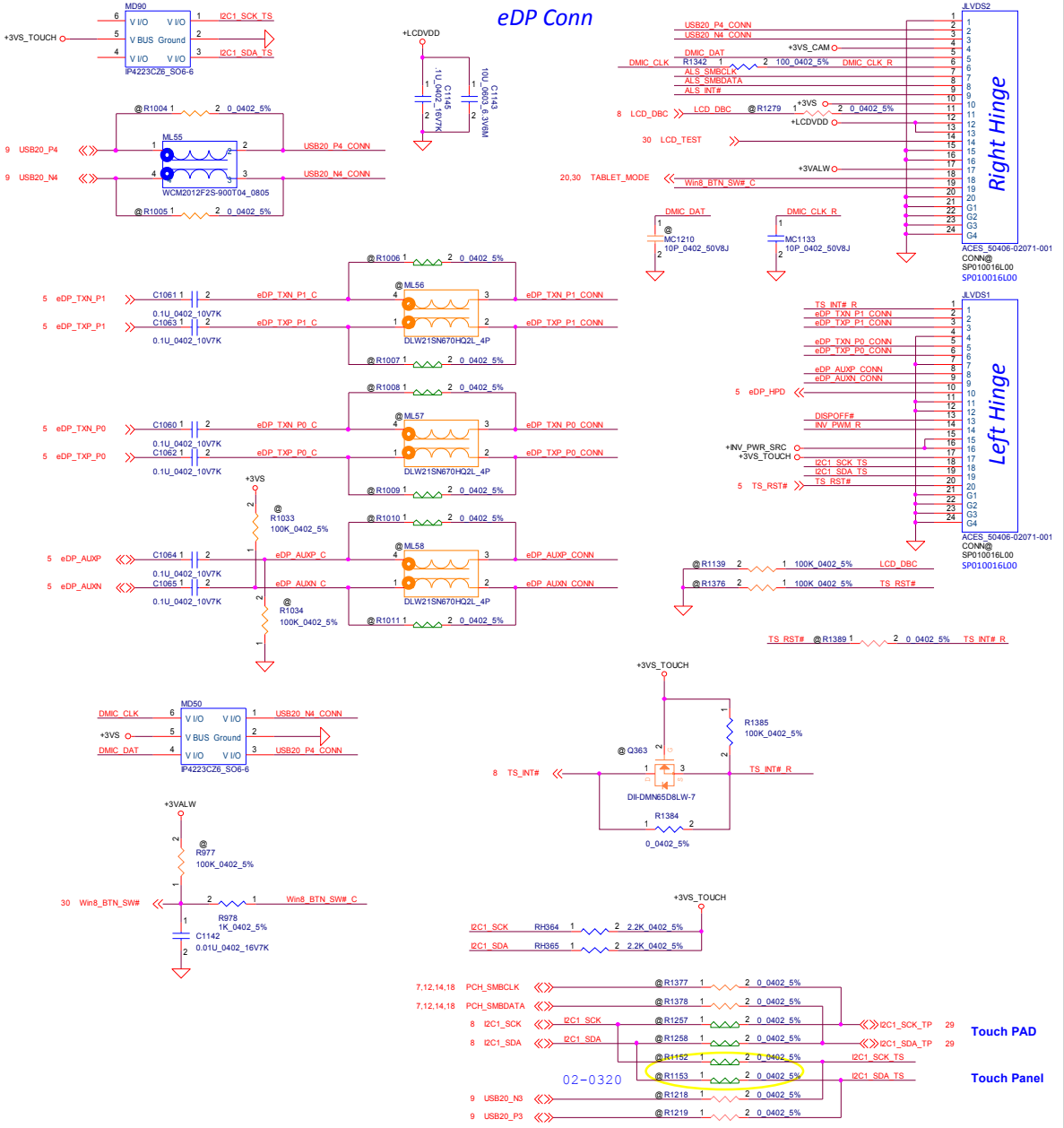


Discharge Circuit

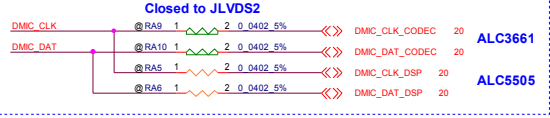
BackLight PWM Control



eDP Conn



Closed to JLVDS2

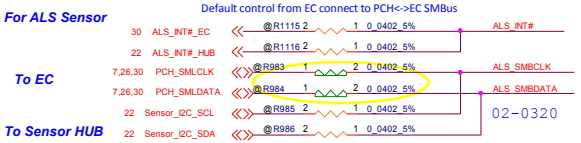


For ALS Sensor

To EC

To Sensor HUB

Default control from EC connect to PCH<->EC SMBus



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Issued Date	2011/06/02	Deciphered Date	2013/10/28

Compal Electronics, Inc.

Title: P17-eDP/ Camera CONN

Size	Document Number	Rev
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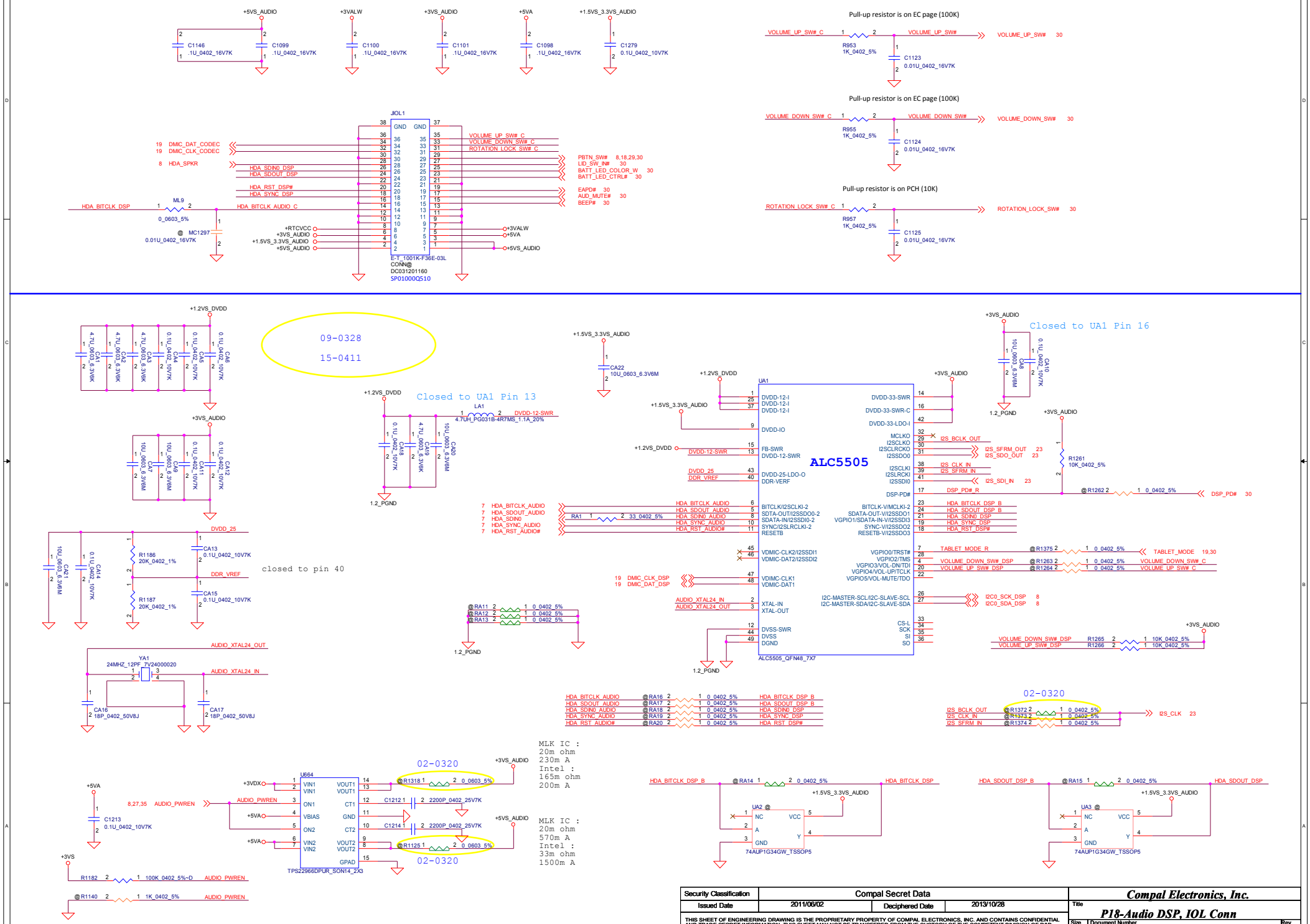
Date: Friday, April 19, 2013 Sheet 19 of 45



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Issued Date	2011/06/02	Deciphered Date	2013/10/28

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Compal Electronics, Inc.

Title: **P18-Audio DSP, IOL Conn**

Size: | Document Number: **LA-9262P** | Rev: 1.0

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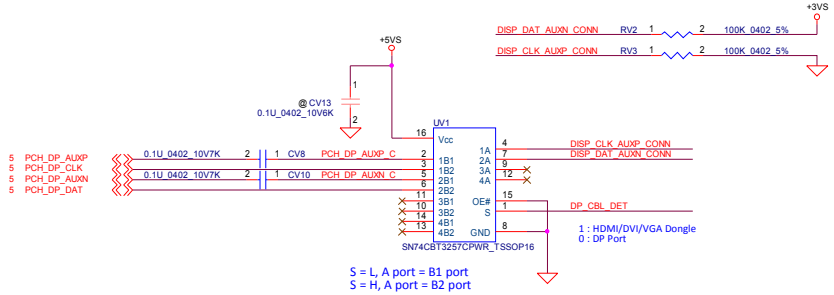
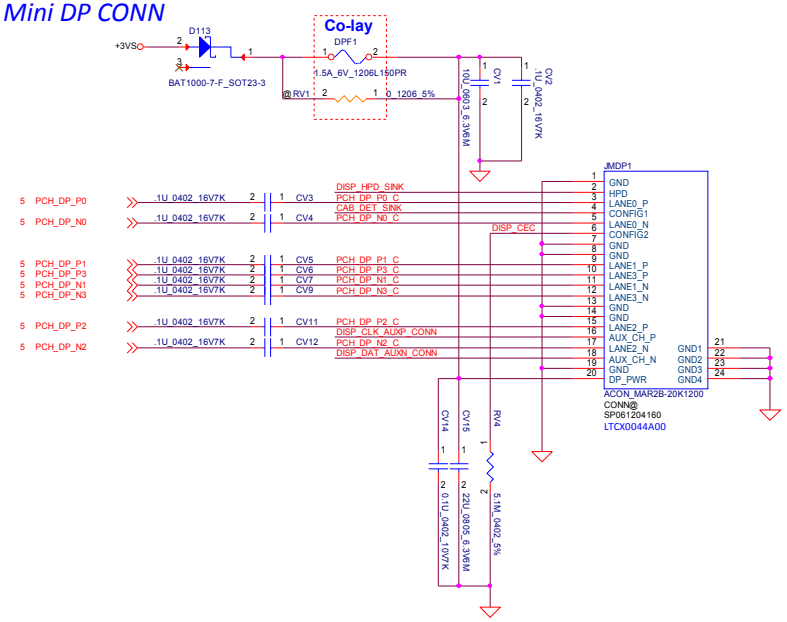
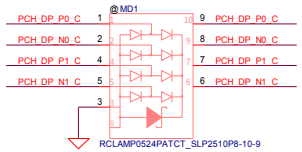


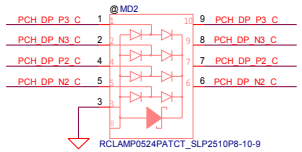
Mini DP CONN



DP Signal ESD



Place close JDP1



Security Classification	Compal Secret Data		Compal Electronics, Inc.
Issued Date	2011/06/02	Deciphered Date	2013/10/28
Title	P19-Mini DP CONN		
Size C	Document Number LA-9262P		Rev 1.0
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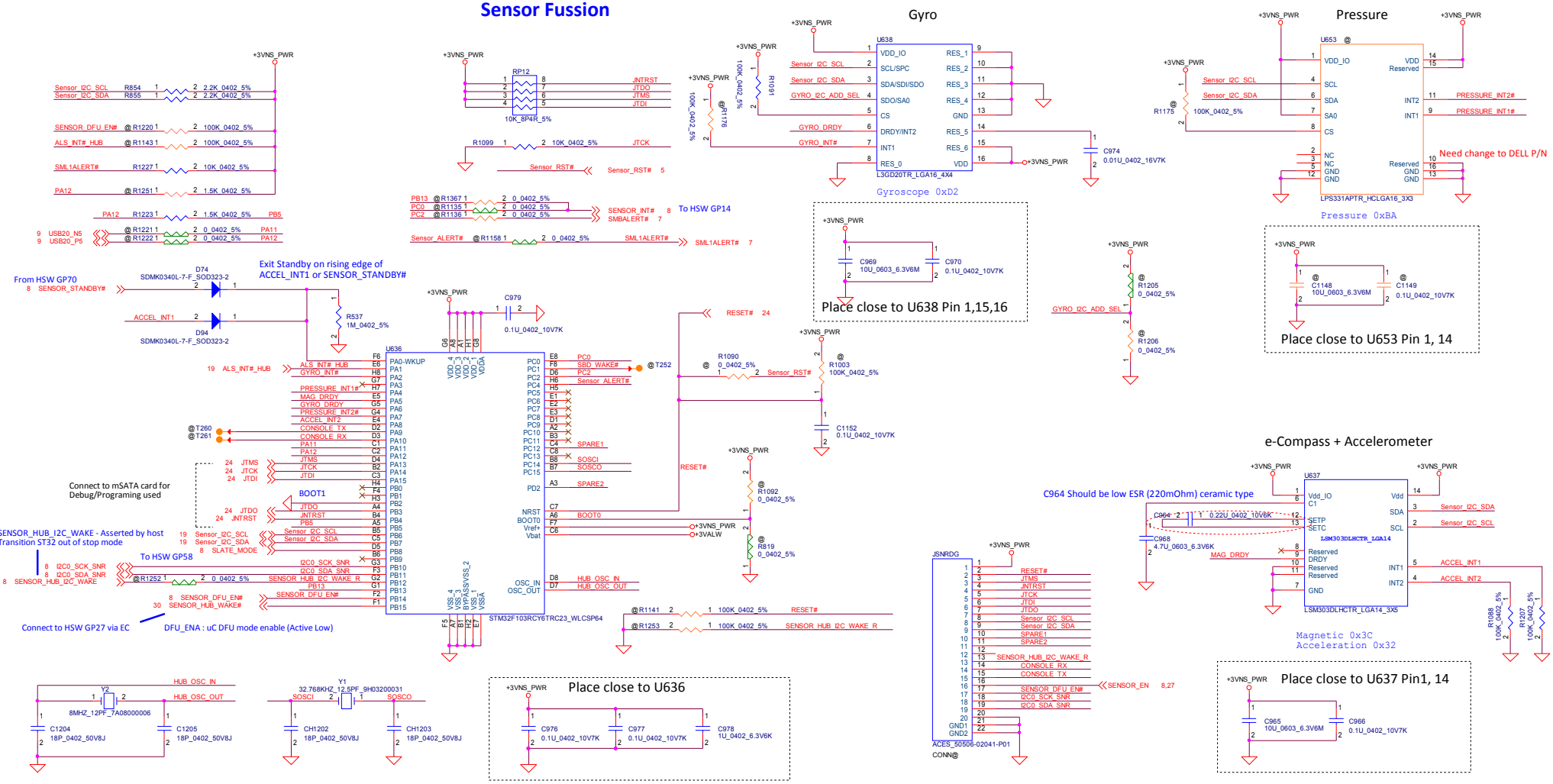
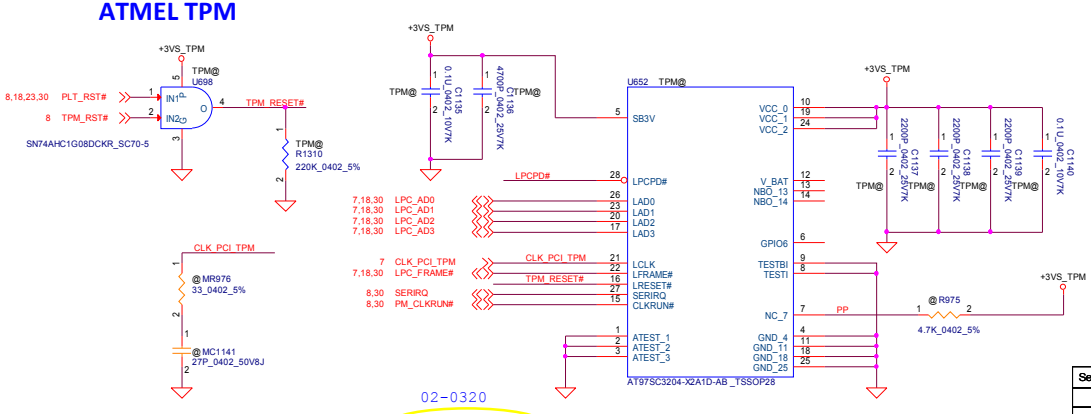
Sensor Fussion



ATMEL TPM



Security Classification	Compal Secret Data		
Issued Date	2011/06/02	Deciphered Date	2013/10/28

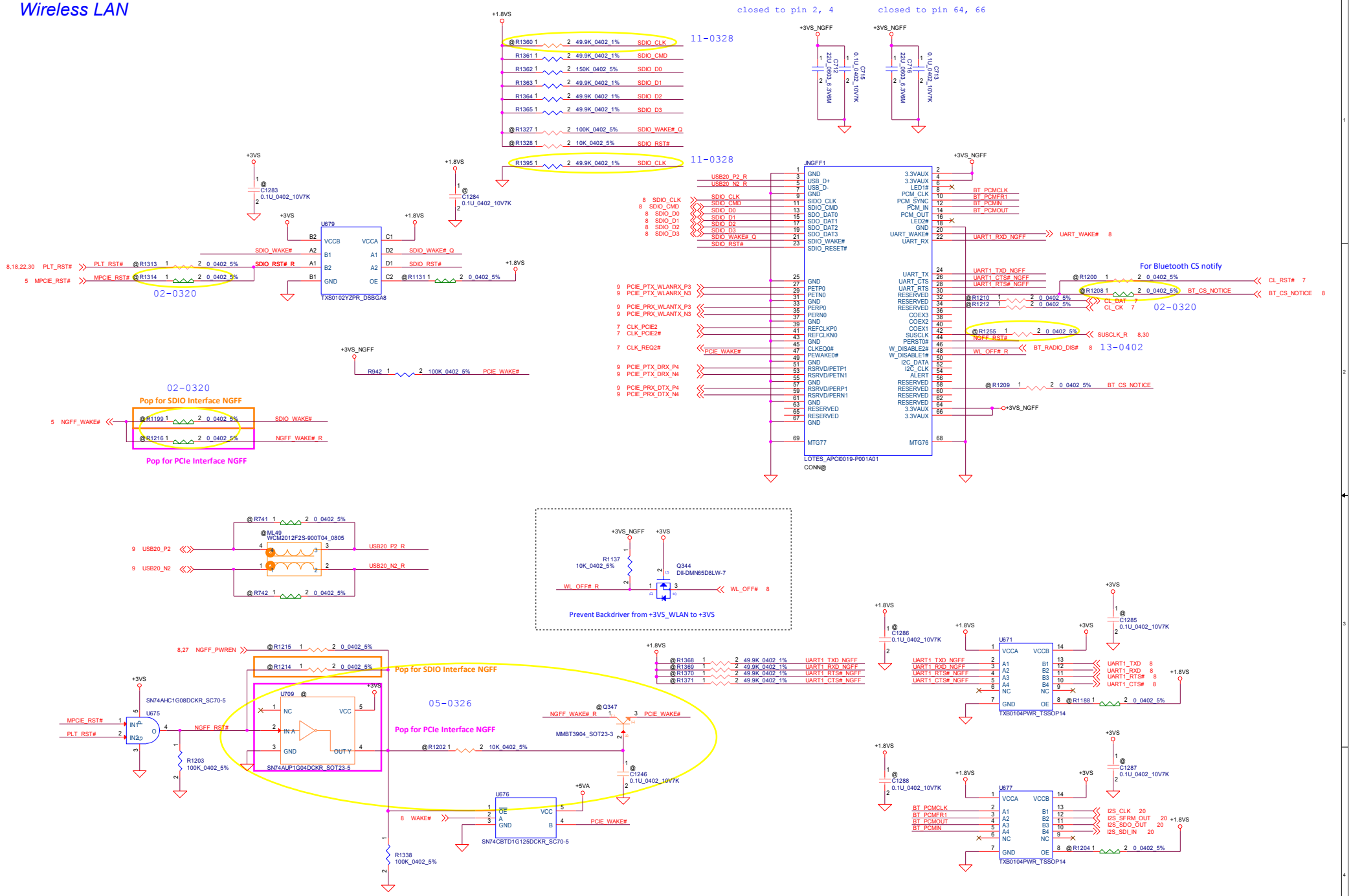
Compal Electronics, Inc.

Title: **P20-Sensor Fussion / TPM**

Size | Document Number: **LA-9262P** | Rev: 1.0

Date: Friday, April 19, 2013 | Sheet 22 of 45

Wireless LAN



Security Classification	Compal Secret Data		
Issued Date	2011/06/02	Deciphered Date	2013/10/28

Compal Electronics, Inc.

Title: **P21-WLAN / WiGig / BT**

Size | Document Number: **LA-9262P** | Rev: 1.0

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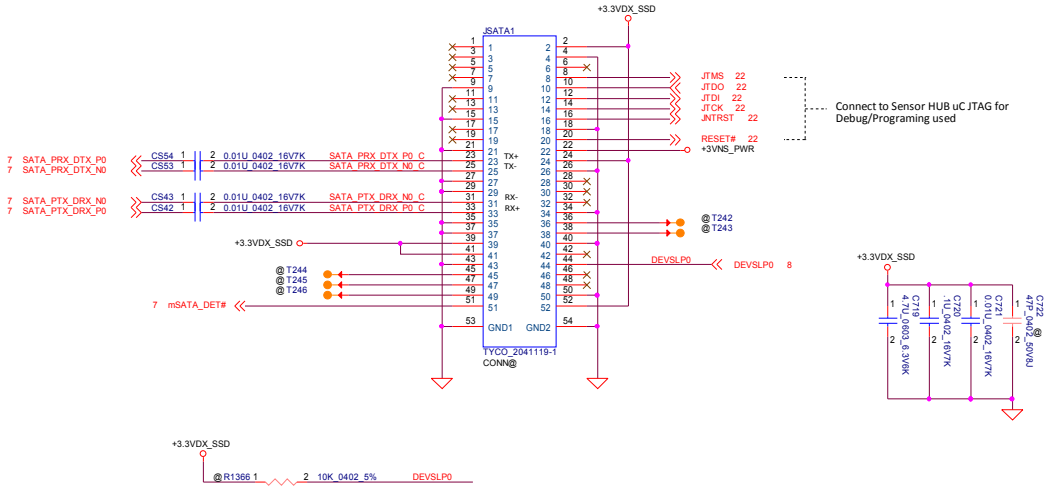
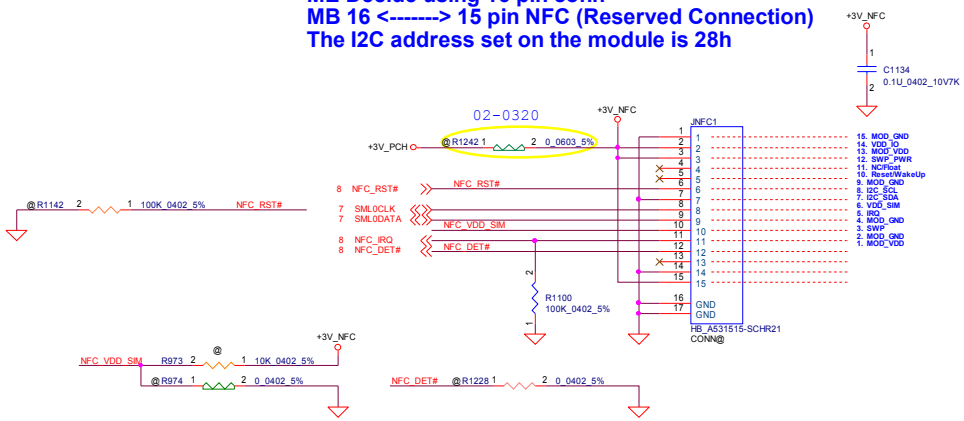
mSATA Card



ME Decide using 16 pin conn
MB 16 <-------> 15 pin NFC (Reserved Connection)
The I2C address set on the module is 28h



Security Classification	Compal Secret Data		
Issued Date	2011/06/02	Deciphered Date	2013/10/28

Compal Electronics, Inc.			
Title	P22-mSATA / NFC Conn		
Size C	Document Number LA-9262P		Rev 1.0
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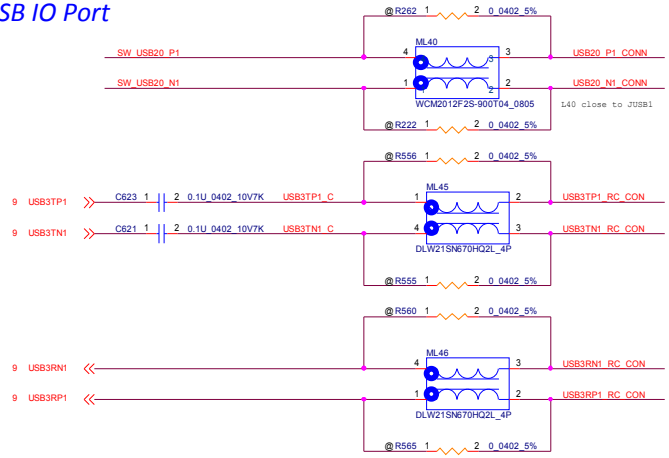
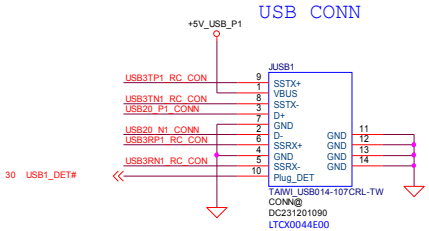
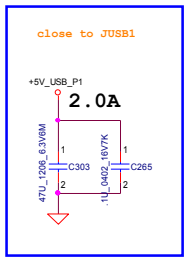
USB IO Port



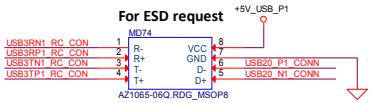
CTL1	CTL2	CTL3	ILIM_SEL	MODE
0	1	1	0	DCP_Auto
0	1	1	1	DCP_Auto
1	1	1	0	SDP
1	1	1	1	CDP

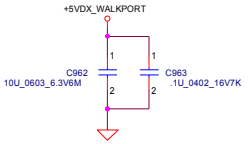
USB CONN



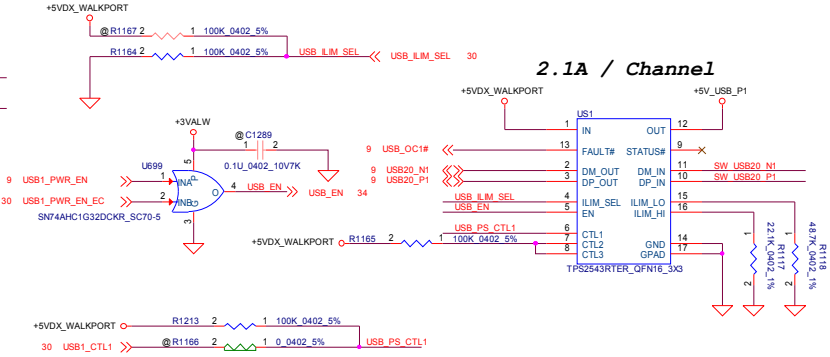


For ESD request

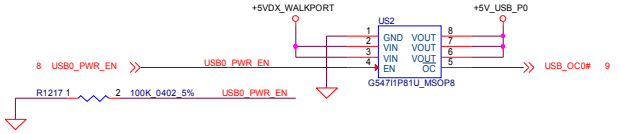


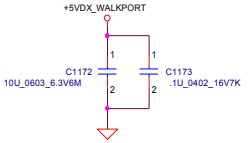


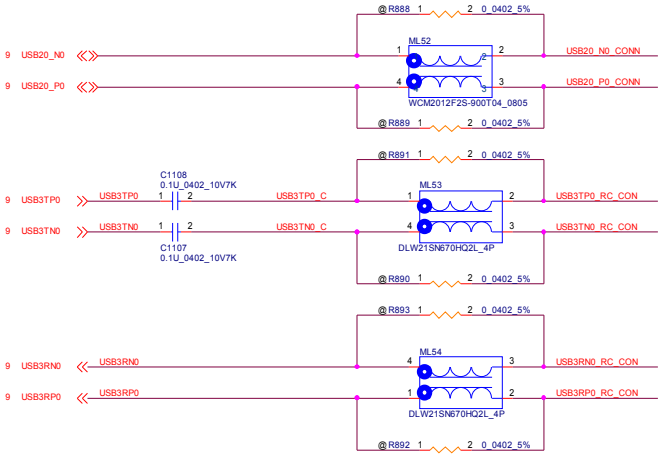
2.1A / Channel



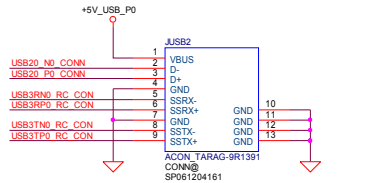
2A / Channel

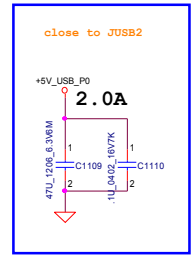




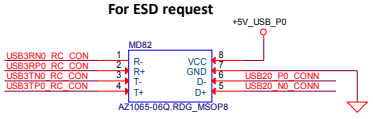


USB CONN



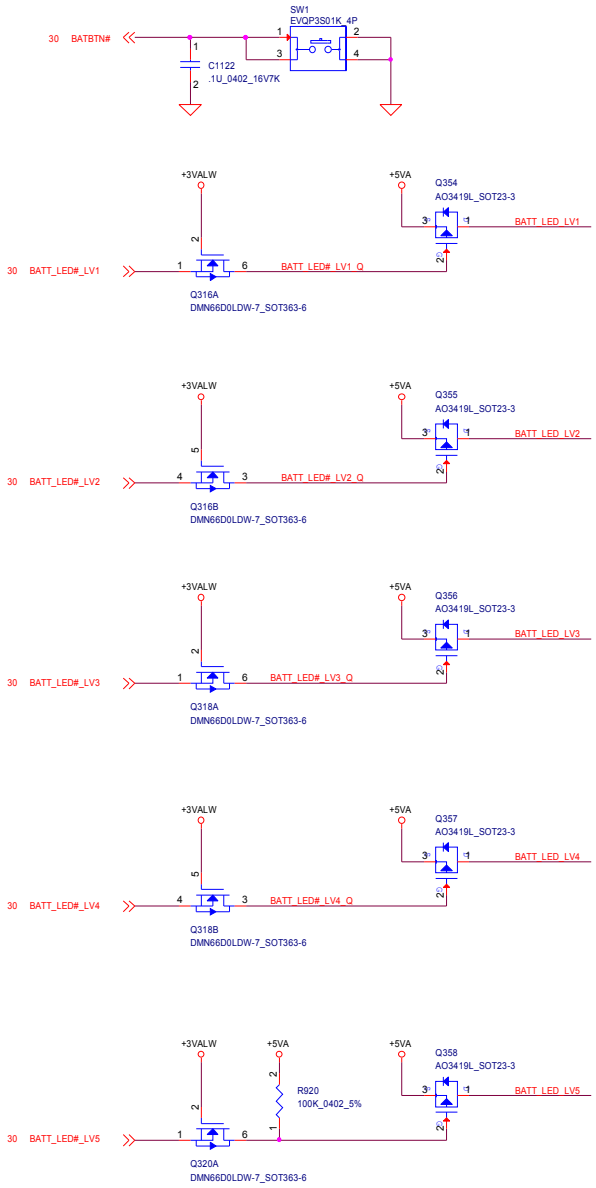


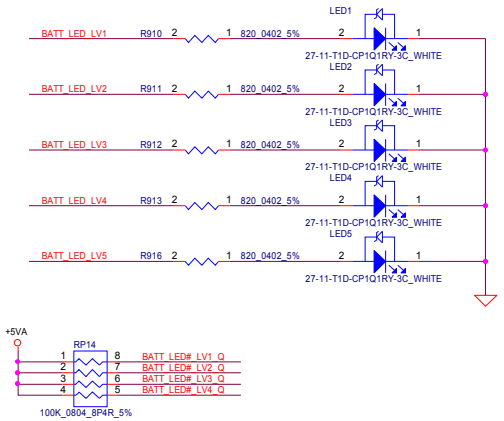
For ESD request

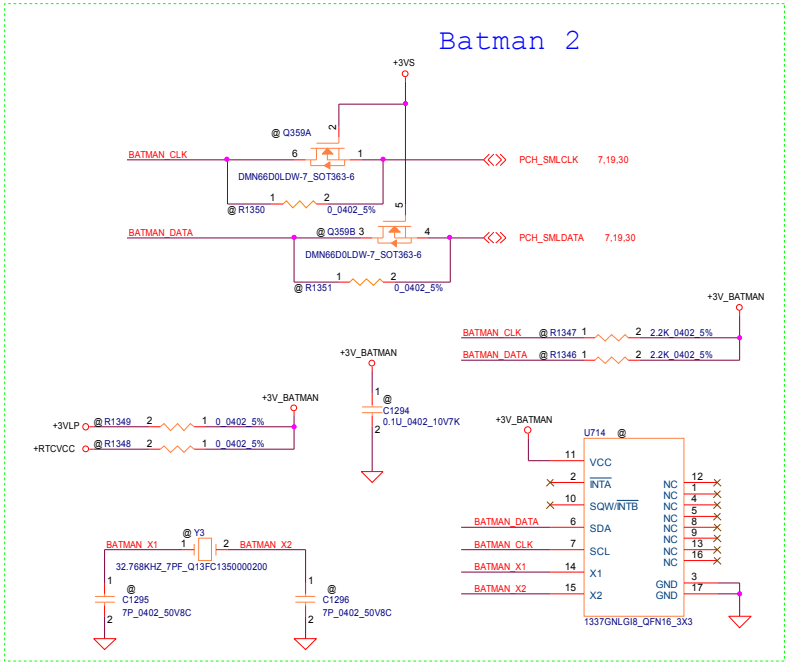


Security Classification	Compal Secret Data		
Issued Date	2011/06/02	Deciphered Date	2013/10/28

Compal Electronics, Inc.	
Title	P23-USB 3.0 IO CONN
Size	Document Number: LA-9262P
Rev	1.0
Date:	Friday, April 19, 2013
Sheet	25 of 45







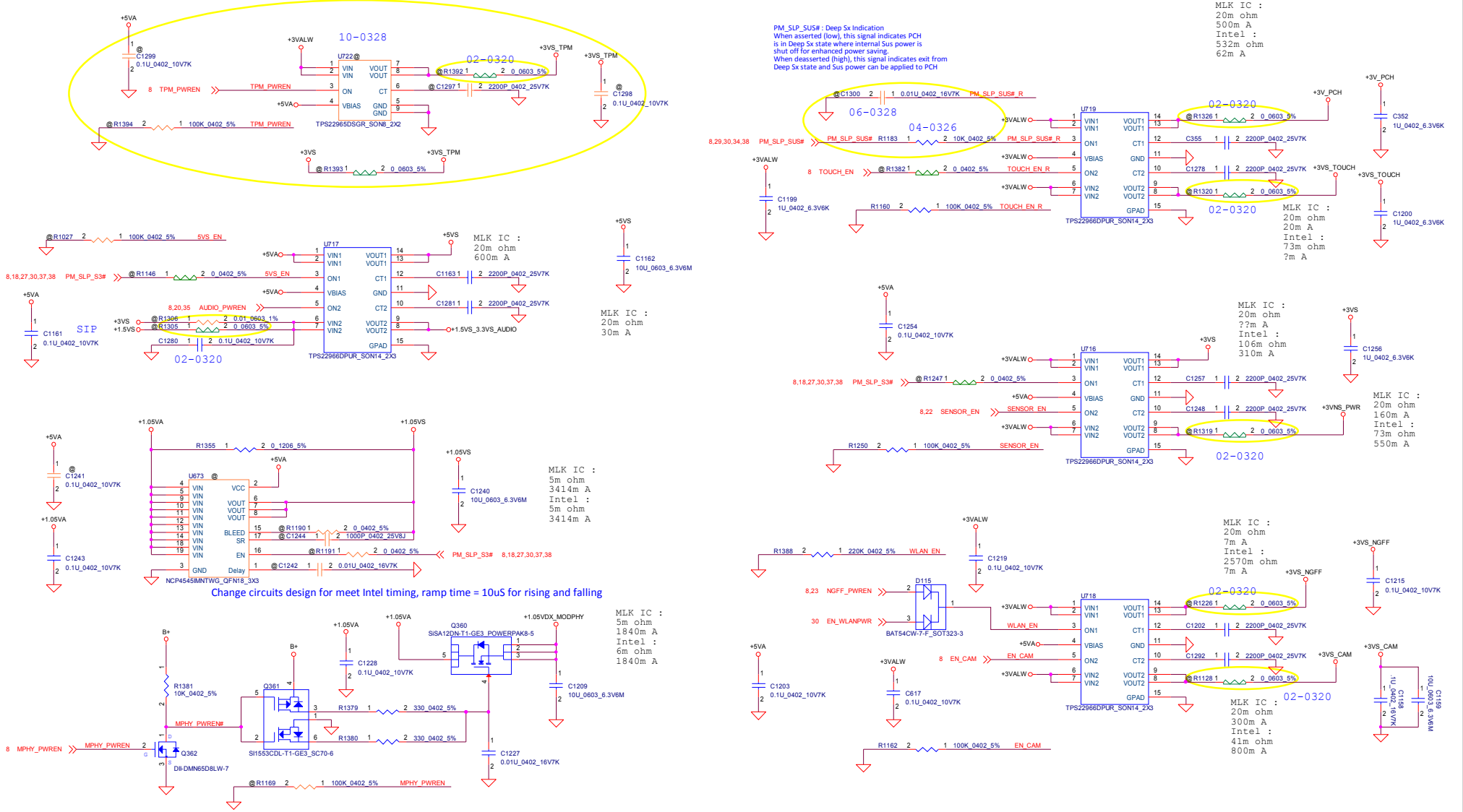
Security Classification	Compal Secret Data		
Issued Date	2011/06/02	Deciphered Date	2013/10/28

Compal Electronics, Inc.

Title: **P24-BAT LED**

Size	Document Number	Rev
	LA-9262P	1.0

Date: Friday, April 19, 2013 | Sheet 26 of 45



Security Classification	Compal Secret Data		
Issued Date	2011/06/02	Deciphered Date	2013/10/28

Compal Electronics, Inc.			
Title	P25-DC/DC Interface		
Size	Document Number		Rev
	LA-9262P		1.0
Date:	Friday, April 19, 2013	Sheet	27 of 45

FD1 FD2 FD3 FD4 FD5 FD6

FIDUCIAL_C40M80

H26 H_3P3

PCB Screw Hole

H1 H_2P3 H5 H_2P3 H6 H_2P3 H14 NUT H_3P2 CONN@ H16 H_2P0X2P5N H17 H_2P0N H3 H_4P0 H8 H_2P3

PCB Screw Hole for CPU (NUT)

H9 H_3P2 CONN@ H10 H_3P2 CONN@ H11 H_3P2 CONN@ H12 H_3P2 CONN@

PCB Screw Hole for mSATA

H13 H_4P5N CONN@

RTC Battery

+RTCBATT +3VLP RTCR1 1K_0402_5% W=20mils W=20mils RTCD1 BAT54CW-7-F_SOT323-3 W=20mils +RTCVCC CH85 1U_0402_6.3V6K

+RTCBATT JBT1 ACES_50271-00201-001 CONN@

+RTCVCC @ CLRP3 SHORT PADS 12-0328

KSO13 @C1174 KSO15 @C1175 KSO16 @C1176 KSO12 @C1177 KSO10 @C1178 KSO11 @C1179 KSO9 @C1180 KSO14 @C1181 KSO6 @C1182 KSO7 @C1183 KSO4 @C1184 KSO5 @C1185 KSI2 @C1186 KSI4 @C1187 KSI6 @C1188 KSI7 @C1189 KSI0 @C1190 KSI3 @C1191 KSI1 @C1192 KSI5 @C1193 KSO2 @C1194 KSO1 @C1195 KSO3 @C1196 KSO8 @C1197 KSO0 @C1078

2 100P_0402_50V8J

8 KB_DET#

KSI[0..7] KSI[0..7] 30

KSO[0..16] KSO[0..16] 30

INT_KBD Conn.

1 : Diagnotisc JKB1

KSI7 KSI6 KSI4 KSI2 KSI5 KSI1 KSI3 KSI0 KSO5 KSO4 KSO7 KSO6 KSO8 KSO3 KSO1 KSO2 KSO0 KSO12 KSO16 KSO15 KSO13 KSO14 KSO9 KSO11 KSO10 CAPS_LED

30 : Diagnotisc GND GND

ACES_50699-03041-001 CONN@ DC011112270 LTCX0044300

+3VS +5VS +5VS Q329 AO3419L_SOT23-3 R989 100K_0402_5% 30 CAPS_LED# DII-DMN65D8LW-7 Q326 R943 820_0402_5% CAPS_LED @C1160 0.1U_0402_10V7K

+5VS 20mil +5VS_KBL F1 0.75A_24V_1812L075-24DR-OK C1153 1U_0603_10V6K C1059 10U_0603_6.3V6M

KB_LED_PWM# 8 KB_BL_DET R944 47K_0402_5% +5VS_KBL R945 100K_0402_5% JBL1 GND1 GND2 HB_A810420-SBHR22 CONN@ LED Maximum Current is 300mA 30 KB_LED_PWM Q311 DII-DMN65D8LW-7

Intel recommend for EMI

+0.675VS MC1267 0.1U_0402_10V7K +0.675VS MC1268 0.1U_0402_10V7K

Intel recommend for EMI

+VCC_CORE MC1269 0.1U_0402_10V7K +VCC_CORE MC1270 0.1U_0402_10V7K +VCC_CORE MC1271 0.1U_0402_10V7K +VCC_CORE MC1272 0.1U_0402_10V7K

Intel recommend for EMI

B+ MC1273 0.1U_0402_16V7K B+ MC1274 0.1U_0402_16V7K B+ MC1275 0.1U_0402_16V7K

Intel recommend for EMI

+3VS MC1276 0.1U_0402_10V7K +3VS MC1277 0.1U_0402_10V7K

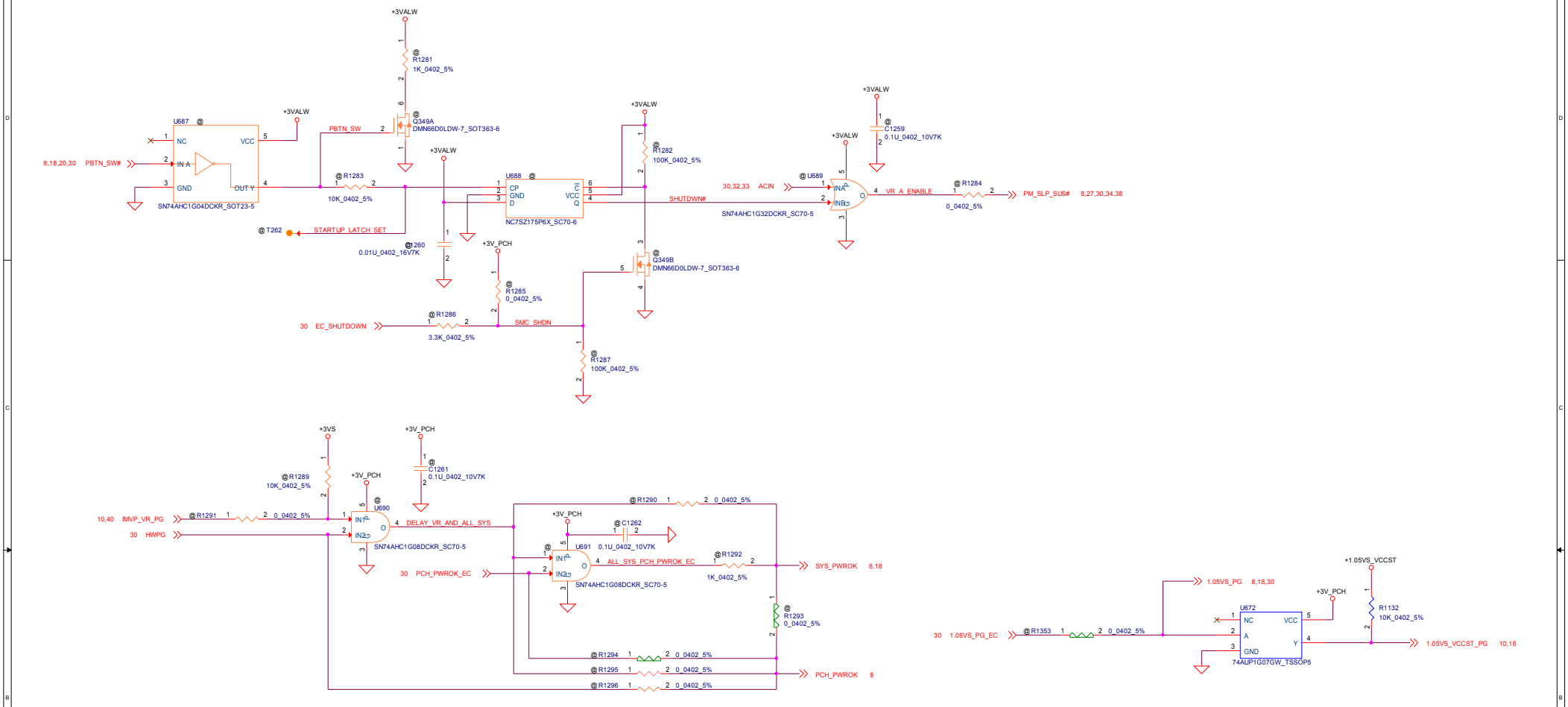
Security Classification	Compal Secret Data		
Issued Date	2011/06/02	Deciphered Date	2013/10/28

Compal Electronics, Inc.

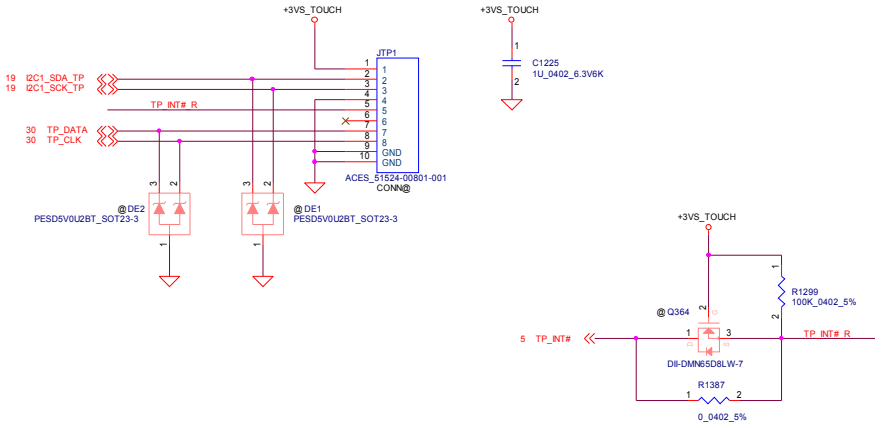
Title: P26-SCREWH/KB/RTC

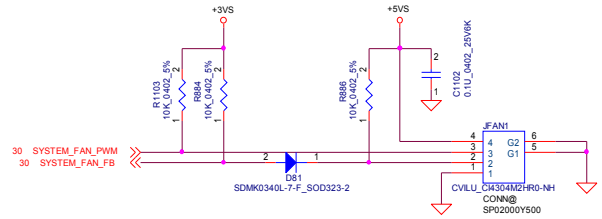
Size | Document Number: LA-9262P | Rev: 1.0

Date: Friday, April 19, 2013 | Sheet 28 of 45



Touchpad CONN





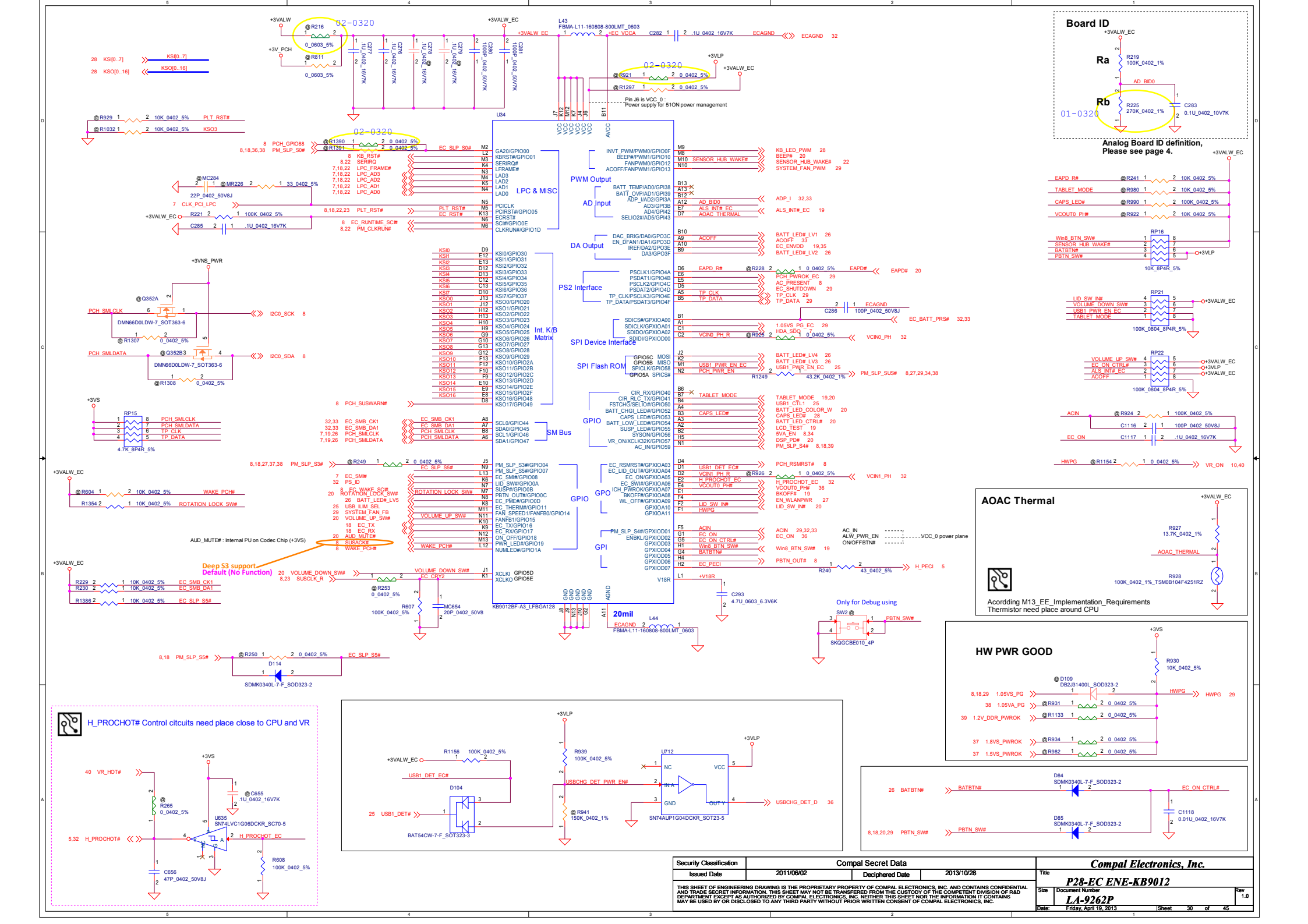
Security Classification	Compal Secret Data		
Issued Date	2011/06/02	Deciphered Date	2013/10/28

Compal Electronics, Inc.

Title: **P27-TP / FAN/PWERGD**

Size	Document Number	Rev
	LA-9262P	1.0

Date: Friday, April 19, 2013 Sheet 29 of 45


Board ID
Ra
Rb
Analog Board ID definition, Please see page 4.
AOAC Thermal
Acordding M13_EE_Implementation_Requirements
Thermistor need place around CPU
HW PWR GOOD
H_PROCHOT# Control citcuits need place close to CPU and VR
Deep S3 support
Default (No Function)
AUD_MUTE# : Internal PU on Codec Chip (+3VS)
Only for Debug using
20mil
U34
KB9012BF-A3_LFBGA128
PWM Output
AD Input
DA Output
PS2 Interface
SPI Device Interface
SPI Flash ROM
GPIO
GPO
GPI
LPC & MISC
Int. K/B Matrix
SM Bus
Security Classification
Compal Secret Data
Issued Date
2011/06/02
Deciphered Date
2013/10/28
Compal Electronics, Inc.
P28-EC ENE-KB9012
LA-9262P
Rev 1.0
Friday, April 19, 2013
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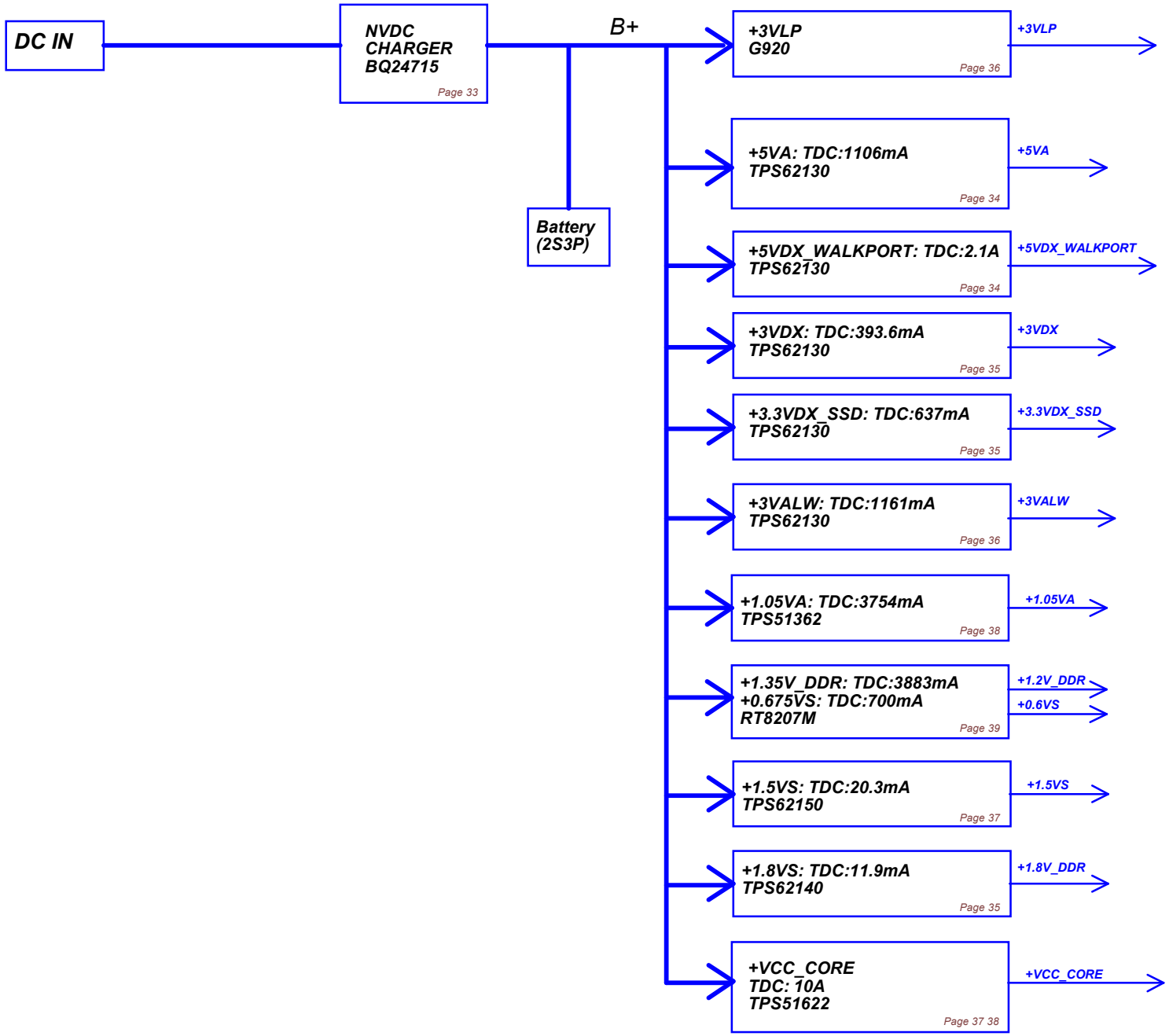
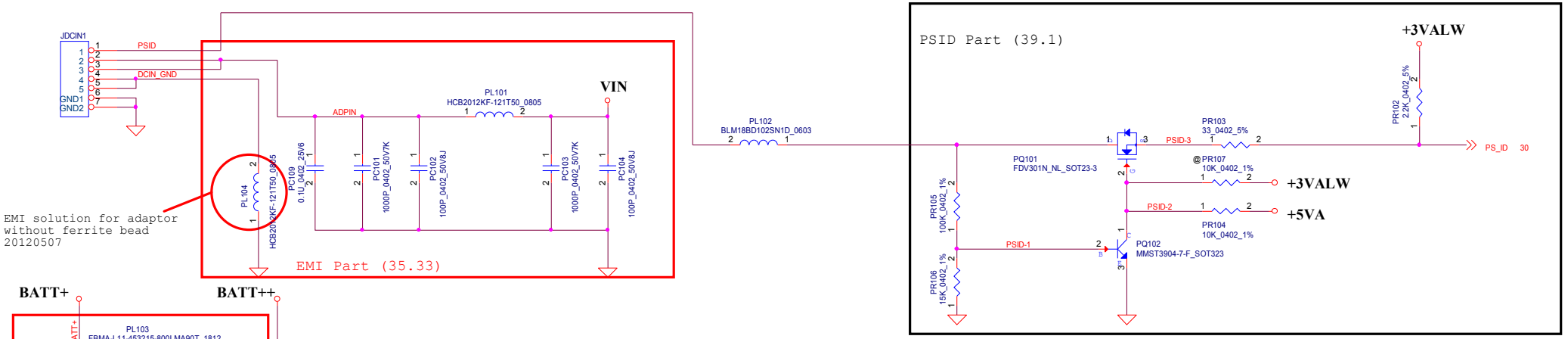
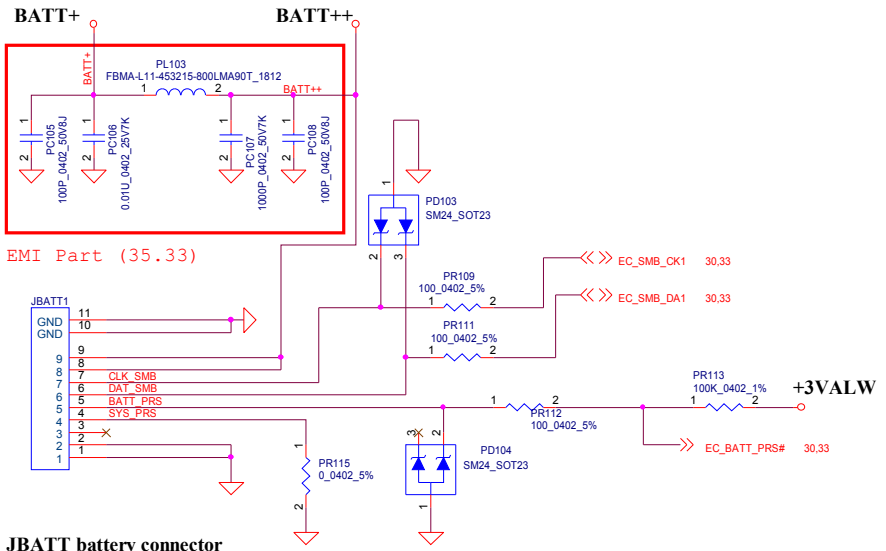


Security Classification	Compal Secret Data		Compal Electronics, Inc.
Issued Date	2011/06/02	Deciphered Date 2013/10/28	Title: P29-PWR_Block_Diagram
			Size: Document Number: LA-9262P Rev: 1.0
			Date: Friday, April 19, 2013 Sheet 31 of 45



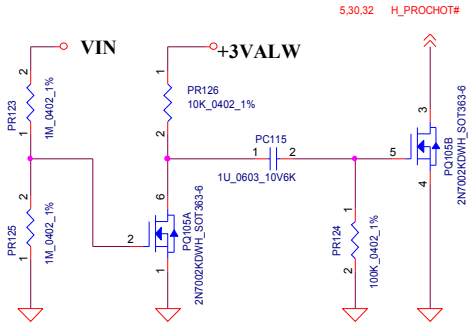


JBATT battery connector

SMART Battery:
1.GND
2.GND
3.BAT_ALERT
4.SYS_PRES
5.BATT_PRS
6.DAT_SMB
7.CLK_SMB
8.BATT++
9.BATT++

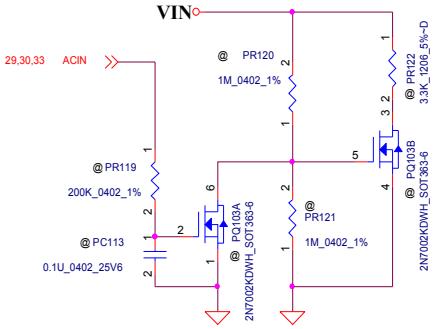
Battery protection:

asserts H_PROCHOT# when adaptor is unplugged, keep low for 10ms till SW PROCHOT# is issued by EC

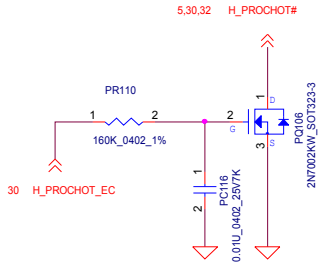


Erp lot6 Circuit

keep DNP in BOM since Dell 45W adaptor has no hiccup mode

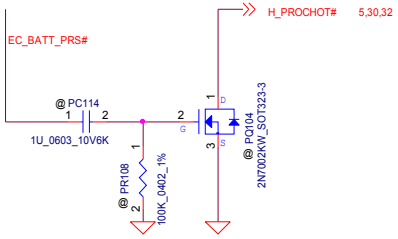


Delay adaptor OC H_PROCHOT# 2ms while hybrid power transition



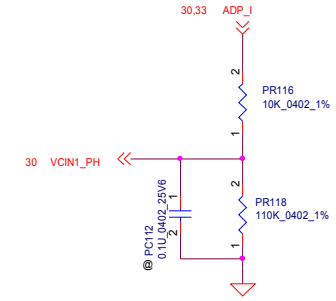
Adaptor protection:

if battery removed, adaptor only, then trigger the H_PROCHOT#, keep DNP in BOM since battery can not be removed by end user



Adaptor protection:

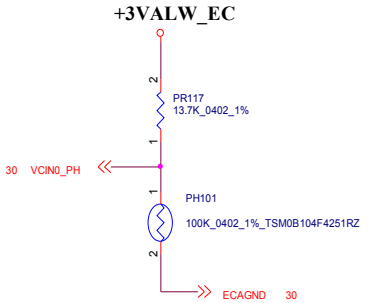
if CP and IPCC failed, adaptor output =rating 100% and over load 20W then trigger the H_PROCHOT# by EC



PH101 under CPU bottom side :

CPU thermal protection @88+-3 degree C

Recovery at 80+-3 degree C



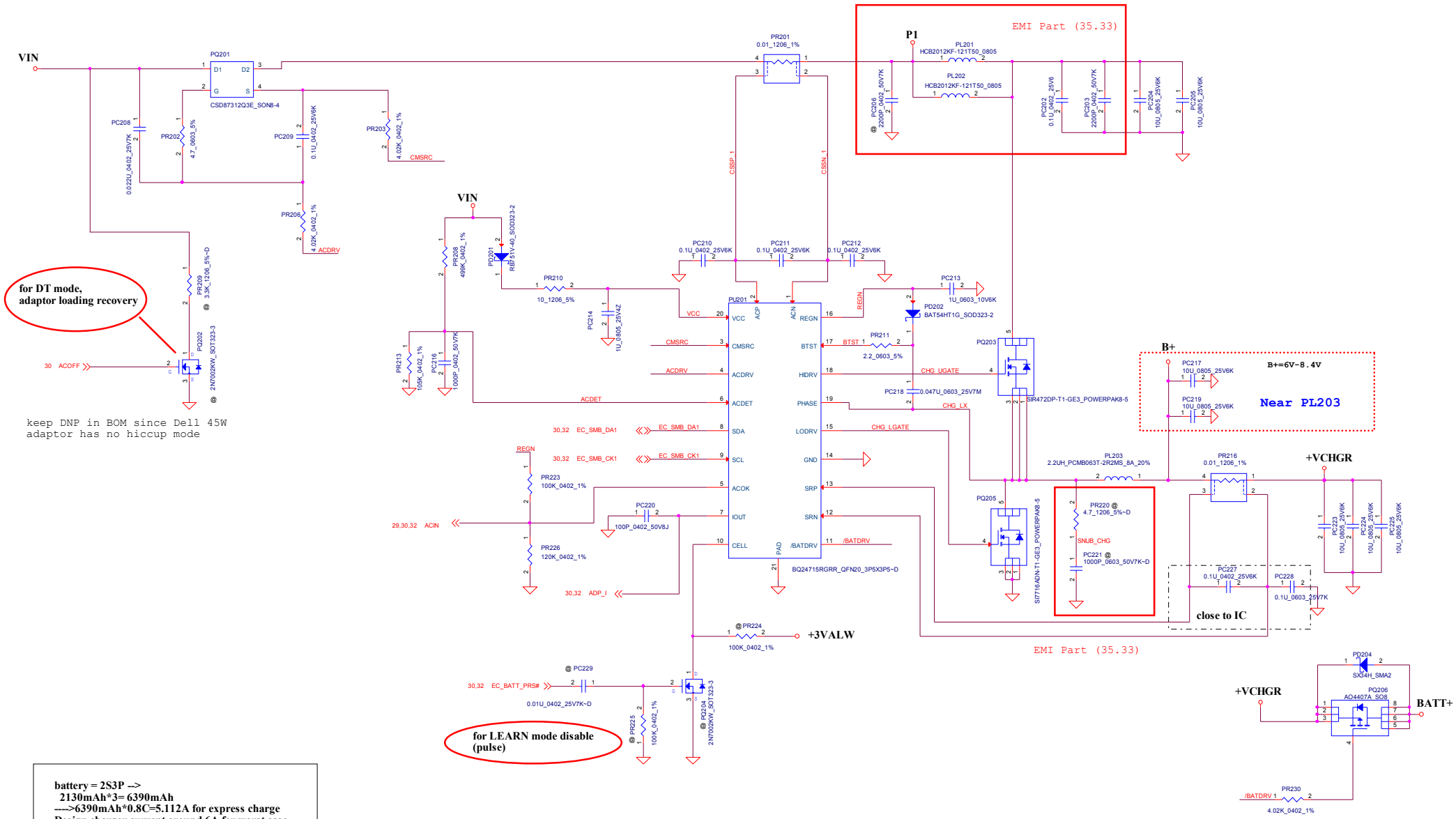
Security Classification	Compal Secret Data		
Issued Date	2011/06/02	Deciphered Date	2013/10/28

Compal Electronics, Inc.

Title: **P30-PWR_DCIN/BATT CONN/OTP**

Size | Document Number: **LA-9262P** | Rev: 1.0

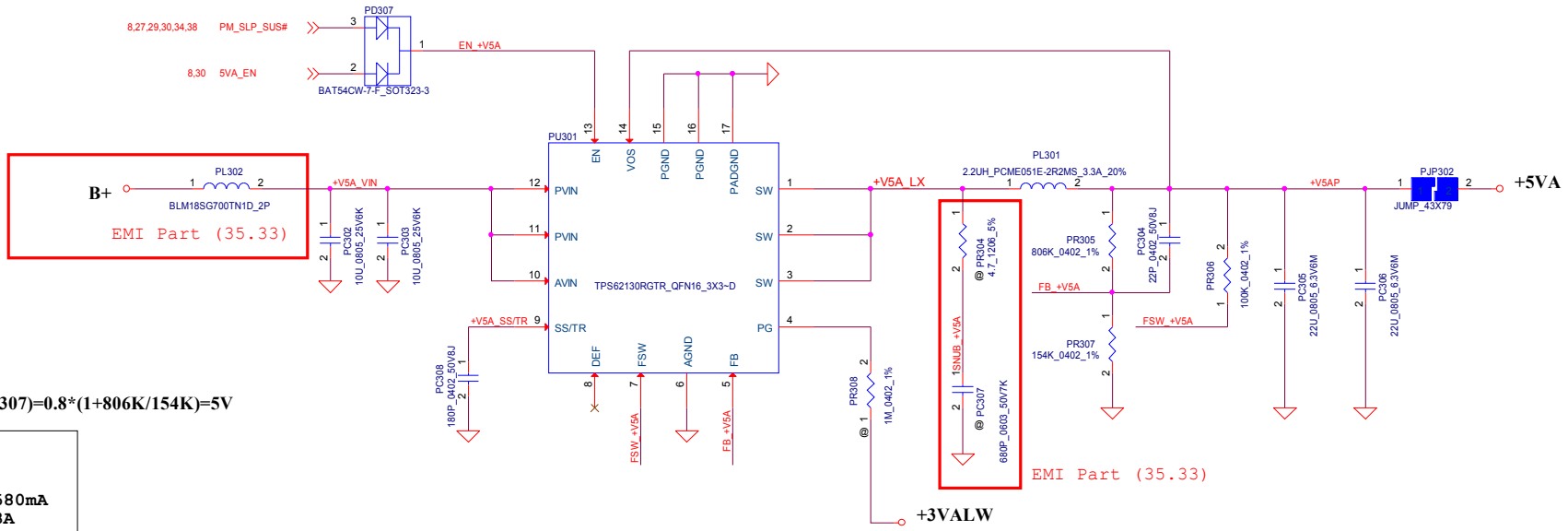
Date: Friday, April 19, 2013 | Sheet 32 of 45



battery = 2S3P -->
2130mAh*3= 6390mAh
---->6390mAh*0.8C=5.112A for express charge
Design charger current around 6A for worst case
max discharge current setting @ 7.7A (around 1.2C)

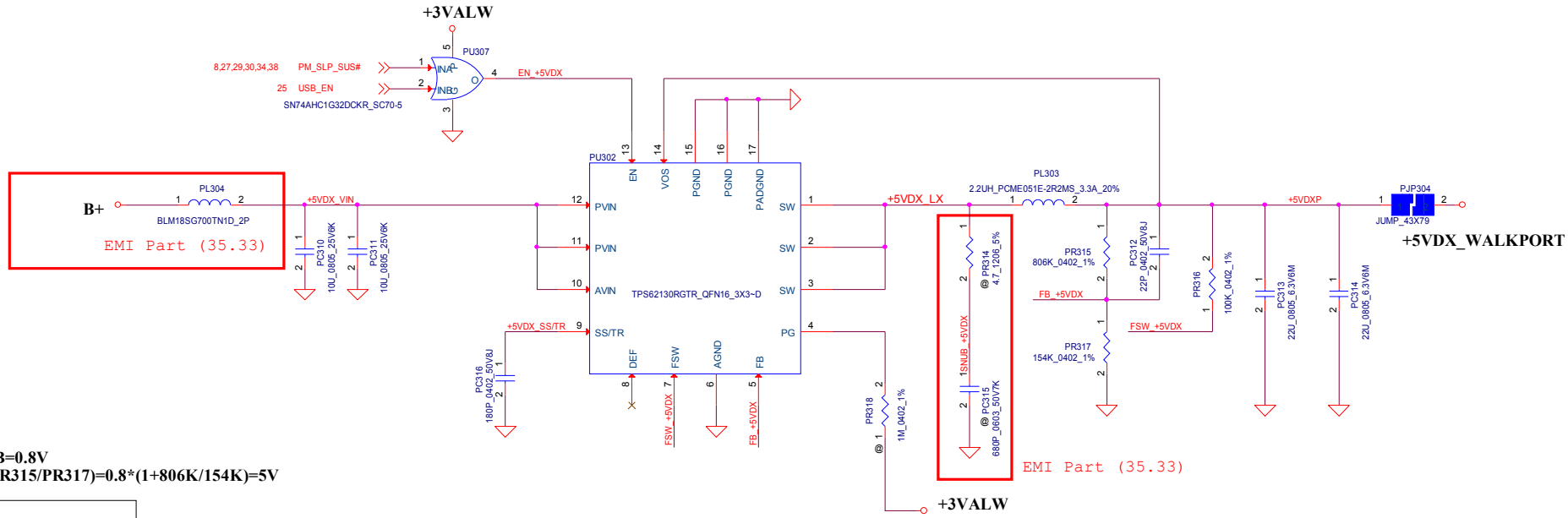
Security Classification	Compal Secret Data		
Issued Date	2011/06/02	Deciphered Date	2013/10/28

Compal Electronics, Inc.			
Title	P31-PWR_NVDC_CHARGER		
Size	Document Number		Rev
	LA-9262P		1.0
Date:	Friday, April 19, 2013	Sheet	33 of 45



<Vo=5V> VFB=0.8V
Vo=VFB*(1+PR305/PR307)=0.8*(1+806K/154K)=5V

+5VA
TDC 1106mA
Peak Current 1580mA
OCP setting @ 3A



<Vo=5V> VFB=0.8V
Vo=VFB*(1+PR315/PR317)=0.8*(1+806K/154K)=5V

+5VDX_WALKPORT
TDC 2.1A
Peak Current 3A
OCP setting @ 3A

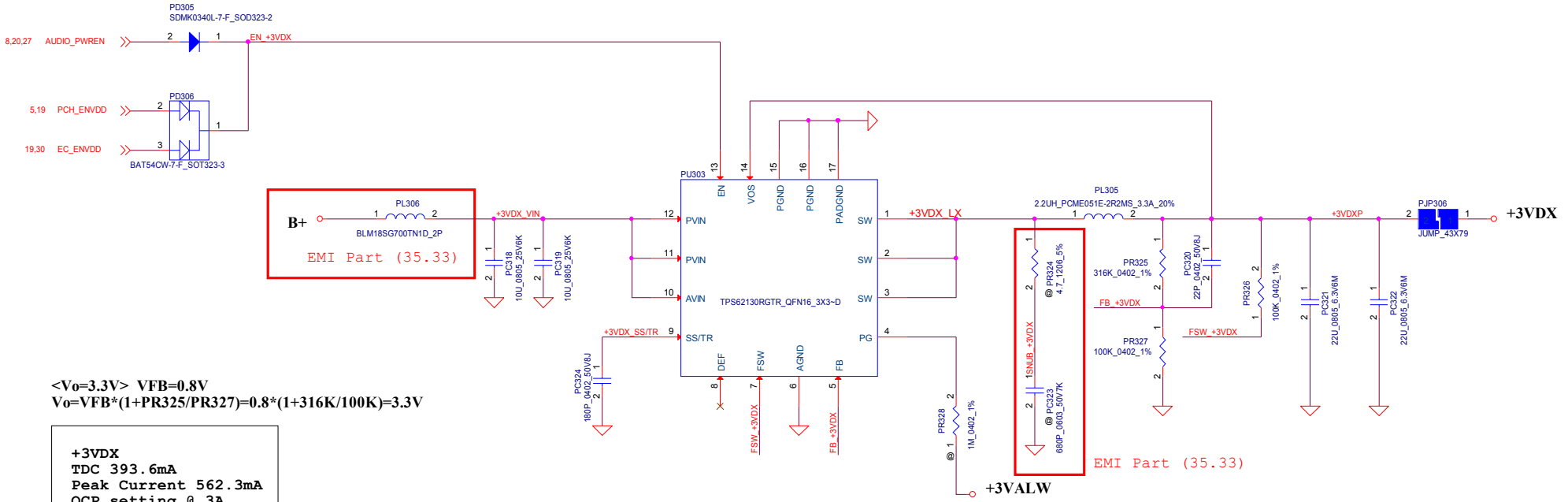
Security Classification	Compal Secret Data		
Issued Date	2011/06/02	Deciphered Date	2013/10/28

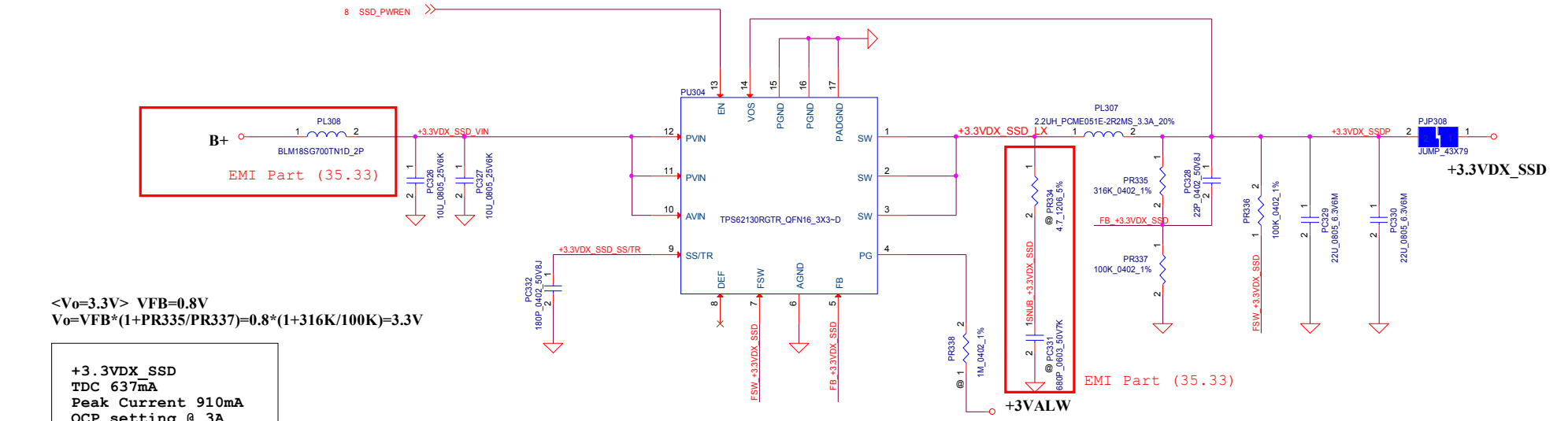
Compal Electronics, Inc.

Title: P32-PWR_+5V_VR

Size: | Document Number: LA-9262P | Rev: 1.0

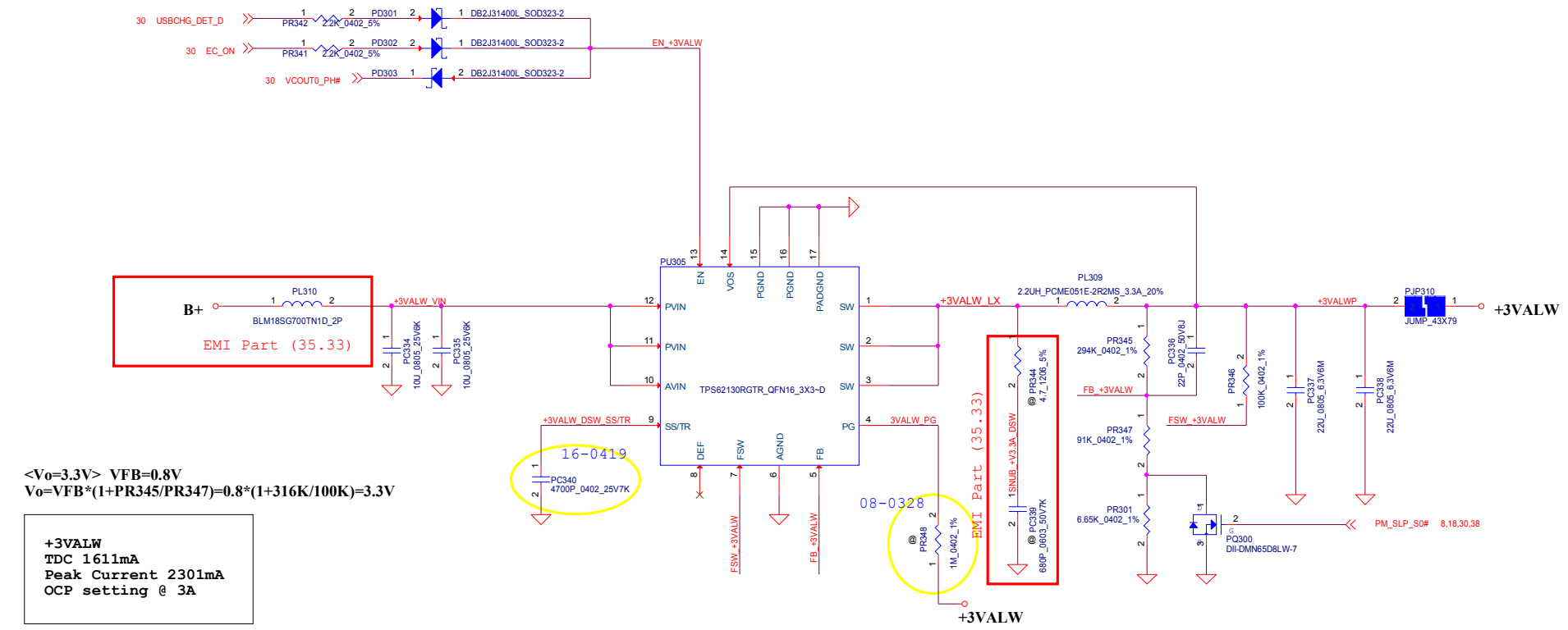
Date: Friday, April 19, 2013 | Sheet 34 of 45



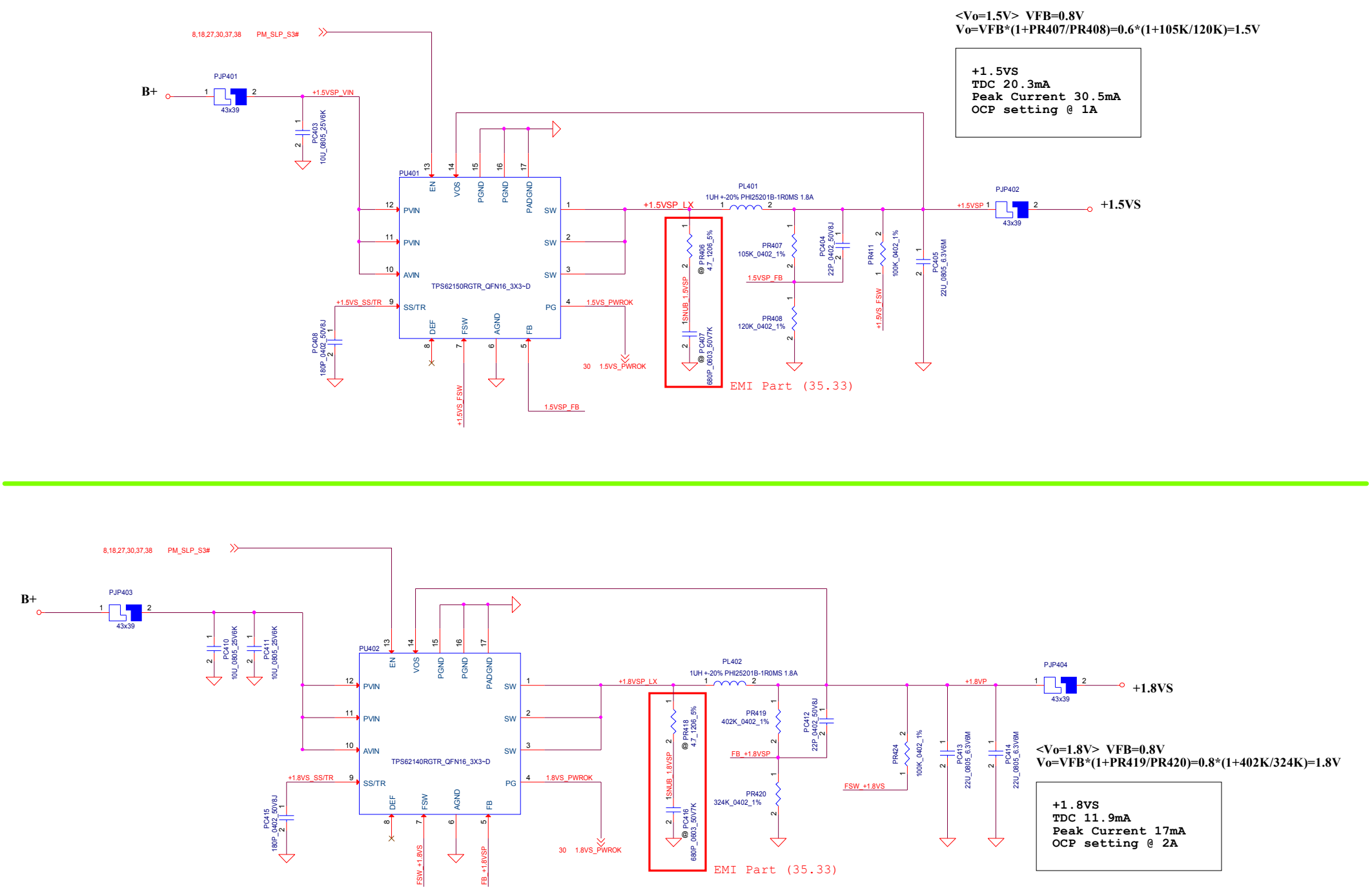


Security Classification	Compal Secret Data		
Issued Date	2011/06/02	Deciphered Date	2013/10/28

Compal Electronics, Inc.			
Title: P33-PWR_+3.3V_VR(1/2)			
Size	Document Number: LA-9262P		Rev: 1.0
Date: Friday, April 19, 2013		Sheet 35 of 45	



Security Classification	Compal Secret Data		Compal Electronics, Inc.
Issued Date	2011/06/02	Deciphered Date 2013/10/28	Title: P34-PWR_+3.3V_VR(2/2)
			Size: Document Number: LA-9262P Rev: 1.0
			Date: Friday, April 19, 2013 Sheet 36 of 45



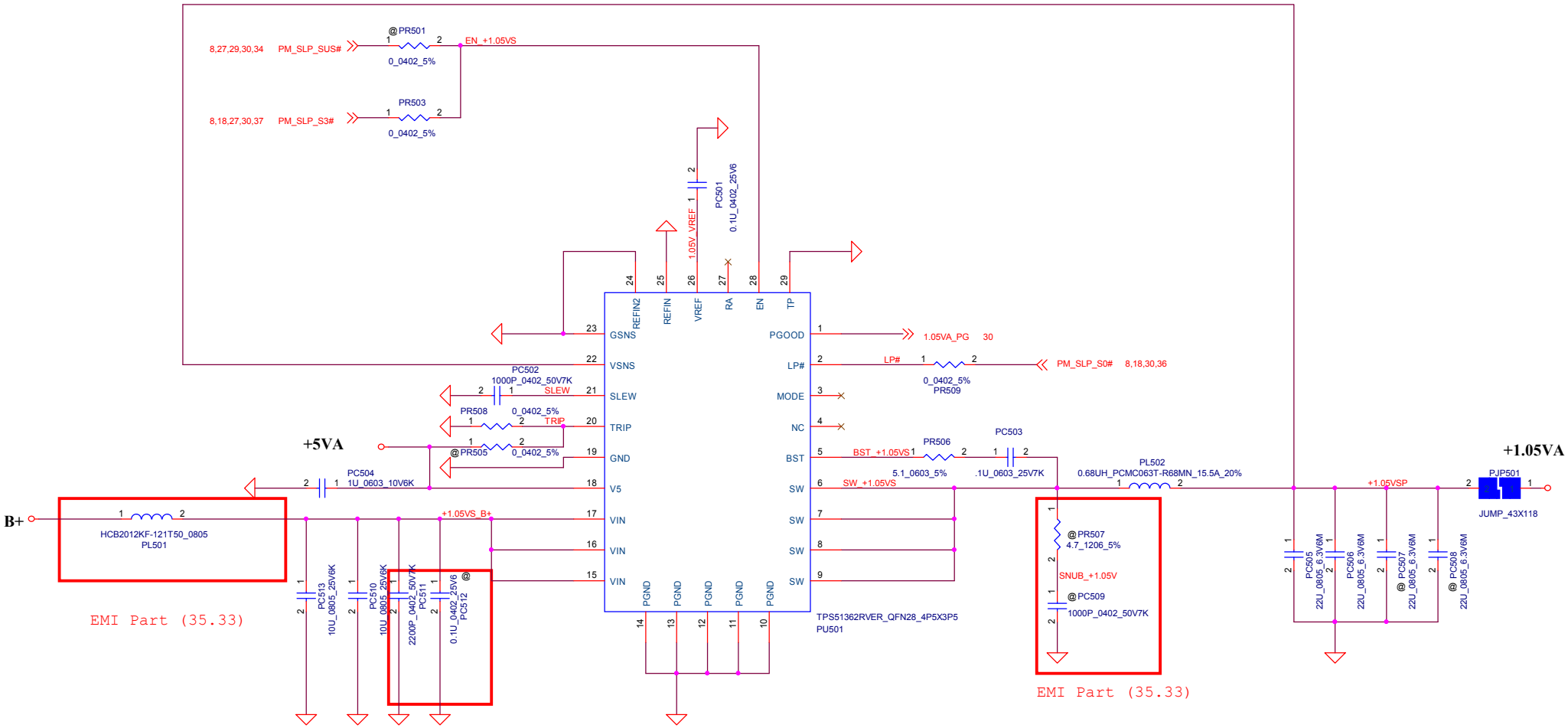
Security Classification	Compal Secret Data		
Issued Date	2011/06/02	Deciphered Date	2013/10/28

Compal Electronics, Inc.

Title: **P35-PWR_+1.5VS/+1.8V_DDR**

Size	Document Number	Rev
	LA-9262P	1.0

Date: Friday, April 19, 2013 | Sheet 37 of 45



+1.05VA
TDC 3754mA
Peak Current 3942mA
OCP setting @ 8A

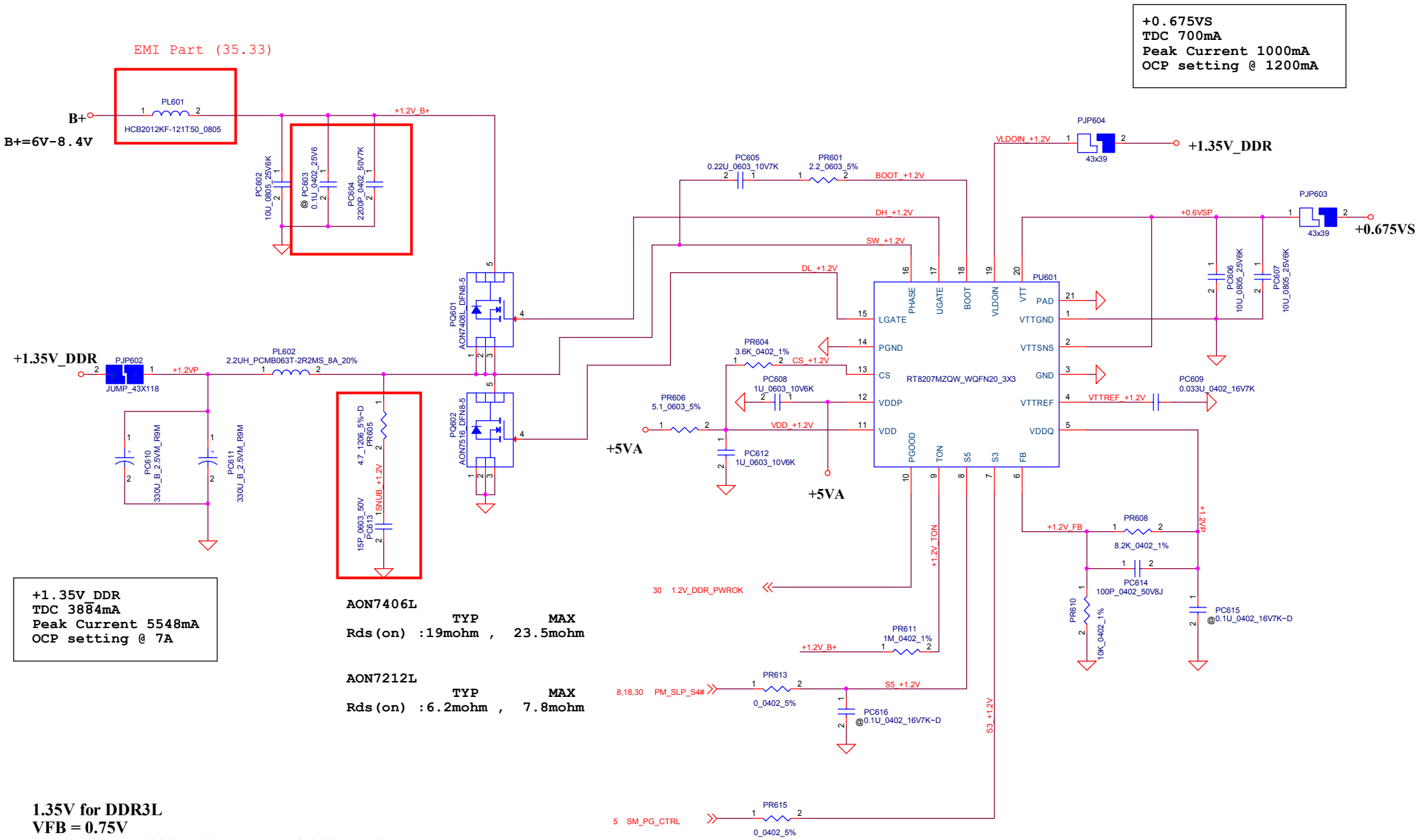
Security Classification	Compal Secret Data		
Issued Date	2011/06/02	Deciphered Date	2013/10/28

Compal Electronics, Inc.

Title: P36-PWR_+1.05VS

Size | Document Number: LA-9262P | Rev: 1.0

Date: Friday, April 19, 2013 | Sheet 38 of 45



Security Classification	Compal Secret Data		
Issued Date	2011/06/02	Deciphered Date	2013/10/28

Compal Electronics, Inc.			
Title	P37-PWR_+1.35V_DDR/+0.675VS		
Size	Document Number		Rev
	LA-9262P		1.0
Date:	Friday, April 19, 2013	Sheet	39 of 45

DC load line: 2m-OHM
TDC: 10A
IccMax: 32A
OCP: 42A
PH701 B value: 4250K 1%
PH702, PH703 B value: 3435K 1%

B+ → PJP701 JUMP_43X79 → CPU_B+

HCB2012KF-121T50_0805 @PL703

PC701 10U_0805_25V6K
PC702 10U_0805_25V6K
PC703 0.1U_0402_25V6
PC704 2200P_0402_50V7K
PC705 100U_D2_16VM_R50M

EMI Part (35.33)

close to choke
PR702 2.49K_0402_1%
PH702 10K_0402_1%_TSMDA103F34D1RZ
PR707 10.2K_0402_1%
PR708 3.01K_0402_1%
PC708 0.12U_0402_10V6K
close to IC
CSP1
CSN1

PL701 0.24UH_FDUE0630J-H-R24M-P3_22A_20%
+VCC_CORE

PR719 4.7_1206_5%~D
SNUB_phase1
PC712 15P_0603_50V

CPU_B+
PR717 10K_0402_1%

PU701 TPS51622RSM_QFN32_4X4
VBAT SLEWA THERM IMON OCP-I B-RAMP F-IMAX O-USR
CSP1 CSN1 CSN2 CSP2 PU3 N/C GFB VFB
VR_ON SKIP# PWM1 PWM2 N/C PGOOD VDD VDIO PADD
DROOP COMP VREF VSA GND VR_HOT# VCLK ALERT#

VR_ON 10,30
IMVP_VR_PG 10,29
VR_SVID_DAT
VR_SVID_ALRT#
VR_SVID_CLK
VR_HOT# 30

PR718 0_0402_5% SKIP# → SKIP#1
PR720 @ 75_0402_1%
PC710 1000P_0402_50V7K
PC713 2.2U_0603_10V7K

PU702 CSD97374CQ4M_SON8_3P5X4P5
PGND2 PWM BOOT VSW PGND1 BOOT_R VDD VIN SKIP#
PC711 0.1U_0402_25V6
PR715 0_0603_5%
SW_PHASE_1
SKIP#1

+5VS
+3VS

PR721 @ 75_0402_1% PWM1 → PWM2
PR723 @ 1.91K_0402_1%~D
PR725 1_0603_5%
PC715 1U_0603_10V6K

close to choke
PR724 2.49K_0402_1%
PH703 10K_0402_1%_TSMDA103F34D1RZ
PR728 10.2K_0402_1%
PR729 3.01K_0402_1%
PC716 0.12U_0402_10V6K
close to IC
CSP2
CSN2

PL702 0.24UH_FDUE0630J-H-R24M-P3_22A_20%
+VCC_CORE

PR734 4.7_1206_5%~D
SNUB_phase2
PC722 15P_0603_50V

PR733 0_0402_5% SKIP# → SKIP#2
PR738 @ 75_0402_1%
PC718 1000P_0402_50V7K
PC723 2.2U_0603_10V7K

PU703 CSD97374CQ4M_SON8_3P5X4P5
PC719 0.1U_0402_25V6
PR730 0_0603_5%
SW_PHASE_2

PR726 2.49K_0402_1%
PR727 10K_0402_1%
PR744 10K_0402_1%
PC724 1500P_0402_7K
PC714 @ 100P_0402_50V8J~D
PC717 0.33U_0603_10V7K
PR731 10_0603_1%
PC720 1U_0603_10V6K
+5VA

+1.05VS_VCCST
PR735 56_0402_1%
PR736 @ 75_0402_1%
PR737 130_0402_1%
PC721 0.1U_0402_25V6K

10 VR_SVID_CLK
10 VR_SVID_ALRT#
10 VR_SVID_DAT
from processor

VCCSENSE and VSSSENSE
have been already pull-high to +VCC_CORE and GND
by 100-OHM in HW side, P10 and P11

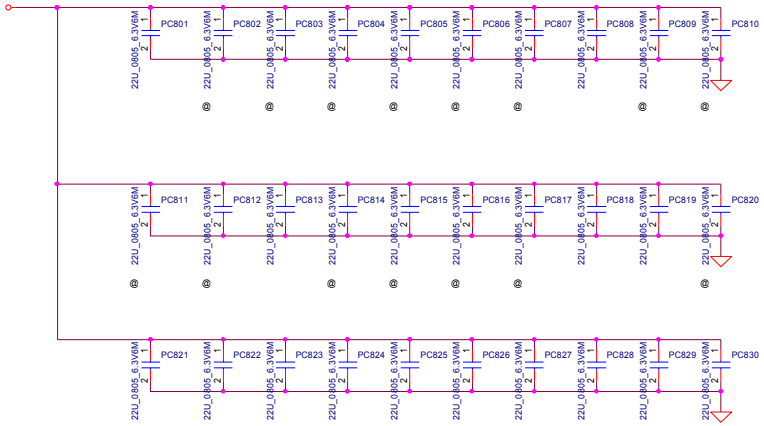
10 VCCSENSE → VFB
11 VSSSENSE → GFB

Security Classification	Compal Secret Data		
Issued Date	2011/06/02	Deciphered Date	2013/10/28

Compal Electronics, Inc.
Title: P38-PWR_CPU_CORE
Size: Document Number: LA-9262P
Rev: 1.0
Date: Friday, April 19, 2013 Sheet 40 of 45

for VCORE:2 phase ---> reserved 30pcs, 15-pcs is OK after fine-tune

+VCC_CORE



Security Classification	Compal Secret Data		
Issued Date	2011/06/02	Deciphered Date	2013/10/28

Compal Electronics, Inc.			
Title	P39-PWR_PROCESSOR_DECOUPLING		
Size	Document Number		Rev
	LA-9262P		1.0
Date:	Friday, April 19, 2013	Sheet 41 of 45	

Version Change List (P. I. R. List) Page 1

Item	Page#	Title	Date	Request Owner	Issue Description	Solution Description	Rev.
X	XX	XXX	XX'XX/XX	Compal_XX	XXXXX	Change PRXX from Xohm to XXKohm.	
	36		20121008	Compal_Power	create one more input cap for TPS51362 Vin	add PC513_10U_0805_16V6K for TPS51362's input	
	34		20121012	Compal_HW	create one more resistor for TPS62130 enable pin	add PR342_2.2K_0402_5%	
	34 35 36		20121018	Compal_Power	design change, delete PU301~PU305, TPS62130 and related components, create PU301, TPS51225 for 3.3V and 5V power rails		
	36		20121018	Compal_Power	design change, delete PU401, PU402, TPS62140 and TPS62150 and related components, create PU401and PU402, SY8003D for 1.5V and 1.8V power rails		
	34 35 36		20121023	dell	reject power design change of 3.3V, 5V, 1.8V and 1.5V		
	38		20121203	Compal_EMI	change PL501 for EMI and layout routing	change from SUPPRE_ FBMA-L11-453215-800LMA90T_1812 to HCB2012KF-121T50_0805	
	39		20121203	Compal_EMI	change PL601 for EMI and layout routing	change from SUPPRE_ FBMA-L11-453215-800LMA90T_1812 to HCB2012KF-121T50_0805	
	40		20121203	Compal_EMI	add PL703 for EMI	add PL701 HCB2012KF-121T50_0805	
	38		20121203	Compal_Power	create PR509 0_0402_5% for debug	add PR509 0_0402_5%	
	32		20121205	Compal_HW	create PR5107 10K_0402_1% for test	add PR107 10K_0402_1%	
	40		20121213	Compal_Power	fine tune VR transient	de-pop PC714, change PR711 from 150K to be 100K	
	40		20130122	Compal_Power	follow Intel's recommendation	change PR737 from 110 OHM to be 130 OHM	
	33		20130131	Compal_RF	reserved a MLCC for RF consideration	create PC206 2200P_0402_50V7K	
	40		20130221	Compal_RF	for RF noise reducing	pop PC703, PR719 and PC712, PR734 and PC722 for VCORE	
	39		20130221	Compal_RF	for RF noise reducing	pop PR605 and PC613 for DDR	

Security Classification	Compal Secret Data		
Issued Date	2011/06/02	Deciphered Date	2013/10/28

Compal Electronics, Inc.

Title: P40-PWR_PIR-1

Size | Document Number: LA-9262P | Rev: 1.0

Date: Friday, April 19, 2013 | Sheet 42 of 45

Version Change List (P. I. R. List)

Item	Page#	Title	Date	Request Owner	Issue Description	Solution Description	Rev.
X	XX	XXX	XX'XX/XX	Compal_XX	XXXXX	Change PRXX from Xohm to XXKohm.	

Security Classification	Compal Secret Data		
Issued Date	2011/06/02	Deciphered Date	2013/10/28

Compal Electronics, Inc.

Title: P41-PWR_PIR-2

Size: | Document Number: LA-9262P | Rev: 1.0

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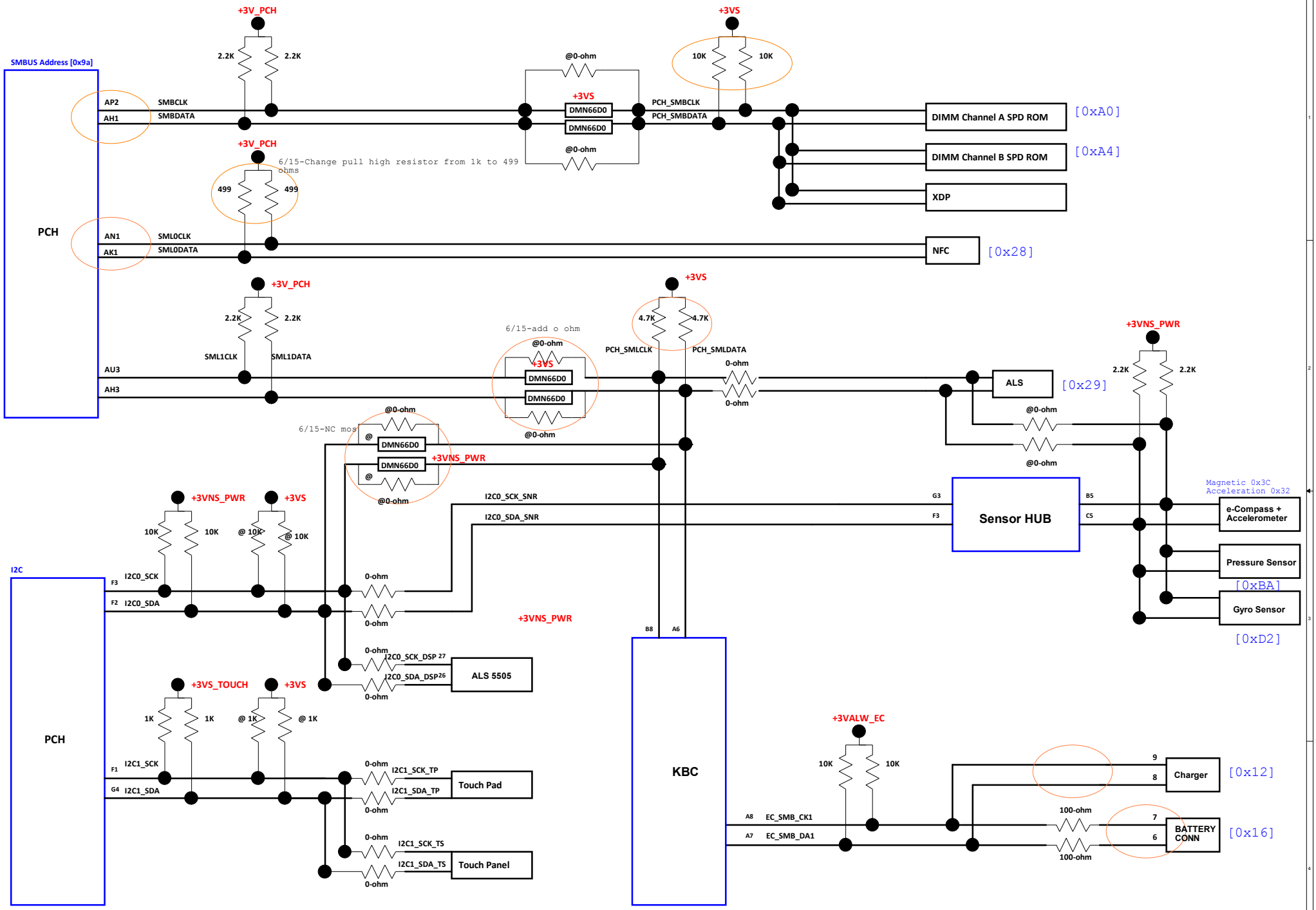


Security Classification	Compal Secret Data		
Issued Date	2011/06/02	Deciphered Date	2013/10/28

Compal Electronics, Inc.

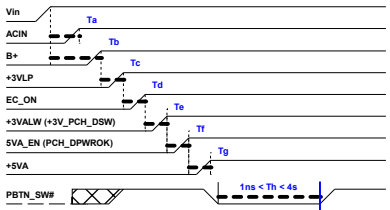
Title: **P42-SMBus Block Diagram**

Size	Document Number	Rev
		1.0

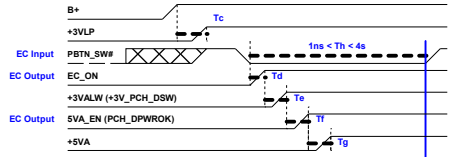
Date: Friday, April 19, 2013 Sheet 44 of 45

Discrete Power On Sequence

[AC in]



[Battery only, AC absent]



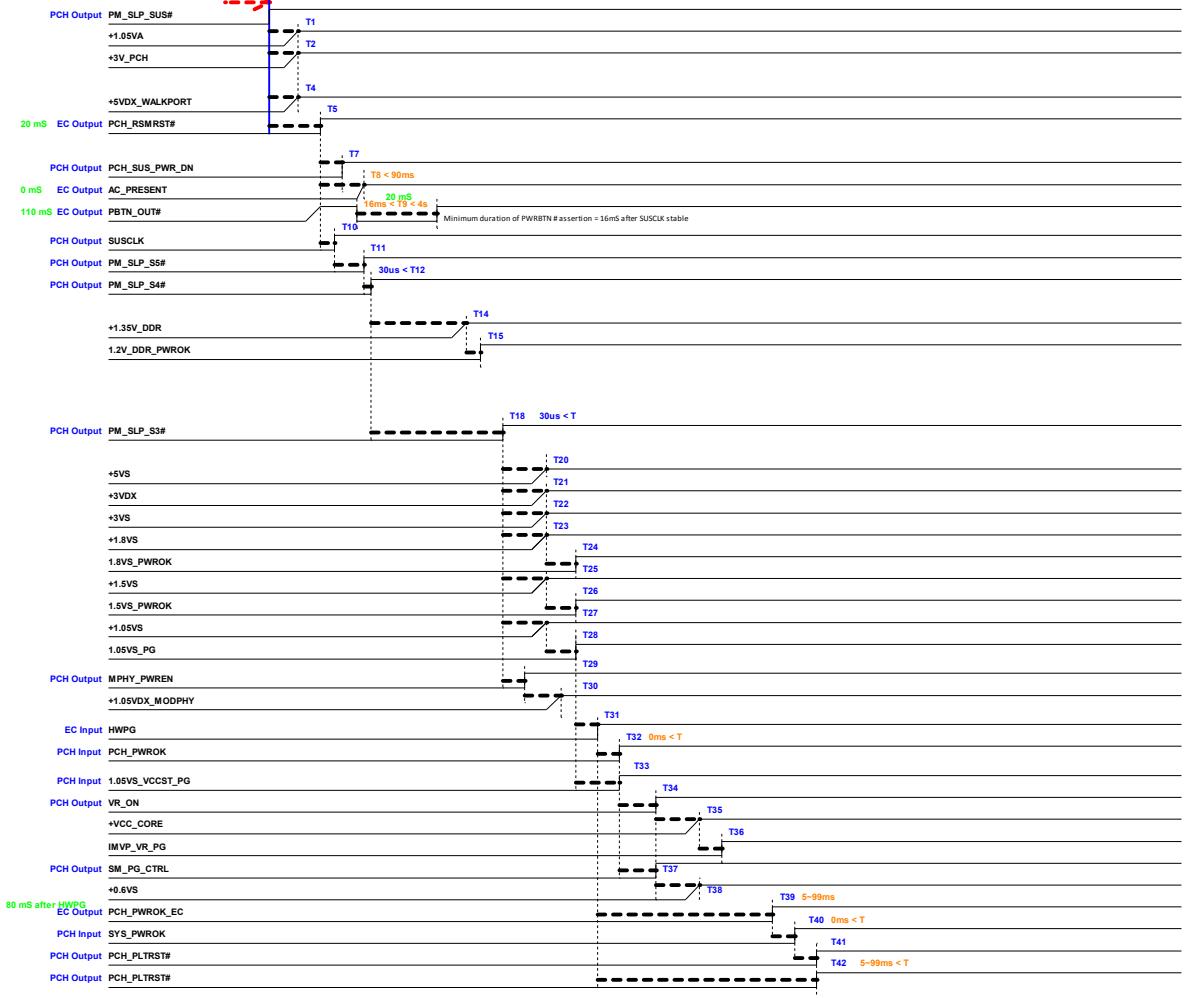
EC pay attention timing

[AC in]

ITEM	Measure Point			Time
Ta	VIN	To	ACIN	
Tb	VIN	To	B+	
Tc	B+	To	+3VLP	
Td	+3VLP	To	EC_ON	
Te	EC_ON	To	+3VALW	
Tf	+3VALW	To	PCH_DPWROK	
Tg	5VA_EN	To	+5VA	
Th	PBTN_SW#		Low pluse width	

[Battery only, AC absent]

ITEM	Measure Point			Time
		To		
		To		
Tc	B+	To	+3VLP	
Th	PBTN_SW#		Low pluse width	
Td	PBTN_SW#	To	EC_ON	
Te	EC_ON	To	+3VALW	
Tf	+3VALW	To	PCH_DPWROK	
Tg	5VA_EN	To	+5VA	



ITEM	Measure Point			Time
T1	PM_SLP_SUS#	To	+1.05VA	
T2	PM_SLP_SUS#	To	+3V_PCH	
T3		To		
T4	PM_SLP_SUS#	To	+5VDX_WALKPORT	
T5	PM_SLP_SUS#	To	PCH_RSMRST#	>10ms
T6		To		
T7	PCH_RSMRST#	To	PCH_SUS_PWR_DN	<200ms
T8	PCH_RSMRST#	To	AC_PRESENT	0~90ms
T9	PBTN_OUT#	To	Low pluse width	
T10	PCH_RSMRST#	To	SUSCLK	>100ms
T11	SUSCLK	To	PM_SLP_S5#	
T12	PM_SLP_S5#	To	PM_SLP_S4#	<30us
T13		To		
T14	PM_SLP_S4#	To	+1.35V_DDR	
T15	+1.35V_DDR	To	1.2V_DDR_PWROK	<10ms
T16		To		
T17		To		
T18	PM_SLP_S4#	To	PM_SLP_S3#	<30us
T19		To		
T20	PM_SLP_S3#	To	+5VS	
T21	PM_SLP_S3#	To	+3VDX	
T22	PM_SLP_S3#	To	+3VS	
T23	PM_SLP_S3#	To	+1.8VS	
T24	+1.8VS	To	ALL_VS_PG	
T25	PM_SLP_S3#	To	+1.5VS	
T26	+1.5VS	To	1.5VS_PWROK	
T27	PM_SLP_S3#	To	+1.05VS	
T28	+1.05VS	To	1.05VS_PG	>1ms
T29	PM_SLP_S3#	To	MPHY_PWREN	
T30	MPHY_PWREN	To	+1.05VDX_MODPHY	
T31	ALL_VS_PG	To	HWPG	
T32	HWPG	To	PCH_PWROK	>5ms
T33	1.05VS_PG	To	1.05VS_VCCST_PG	
T34	1.05VS_VCCST_PG	To	VR_ON	<0.1us
T35	VR_ON	To	+VCC_CORE	<2.5ms
T36	+VCC_CORE	To	IMVP_VR_PG	<7.5ms
T37	PCH_PWROK	To	SM_PG_CTRL	
T38	SM_PG_CTRL	To	+0.6VS	<35us
T39	HWPG	To	PCH_PWROK_EC	5~99ms
T40	PCH_PWROK_EC	To	SYS_PWROK	
T41	SYS_PWROK	To	PCH_PLTRST#	>1.06ms
T42	HWPG	To	PCH_PLTRST#	>5~99ms

Security Classification	Compal Secret Data		Compal Electronics, Inc.
Issued Date	2011/08/25	Deciphered Date	2012/07/25
Title	P44-Power Sequence		
Size	Document Number		Rev 1.0
Date: Friday, April 19, 2013		Sheet 45 of 45	