

Compal Confidential

ZBWAA Bay Trail-M Schematics Document

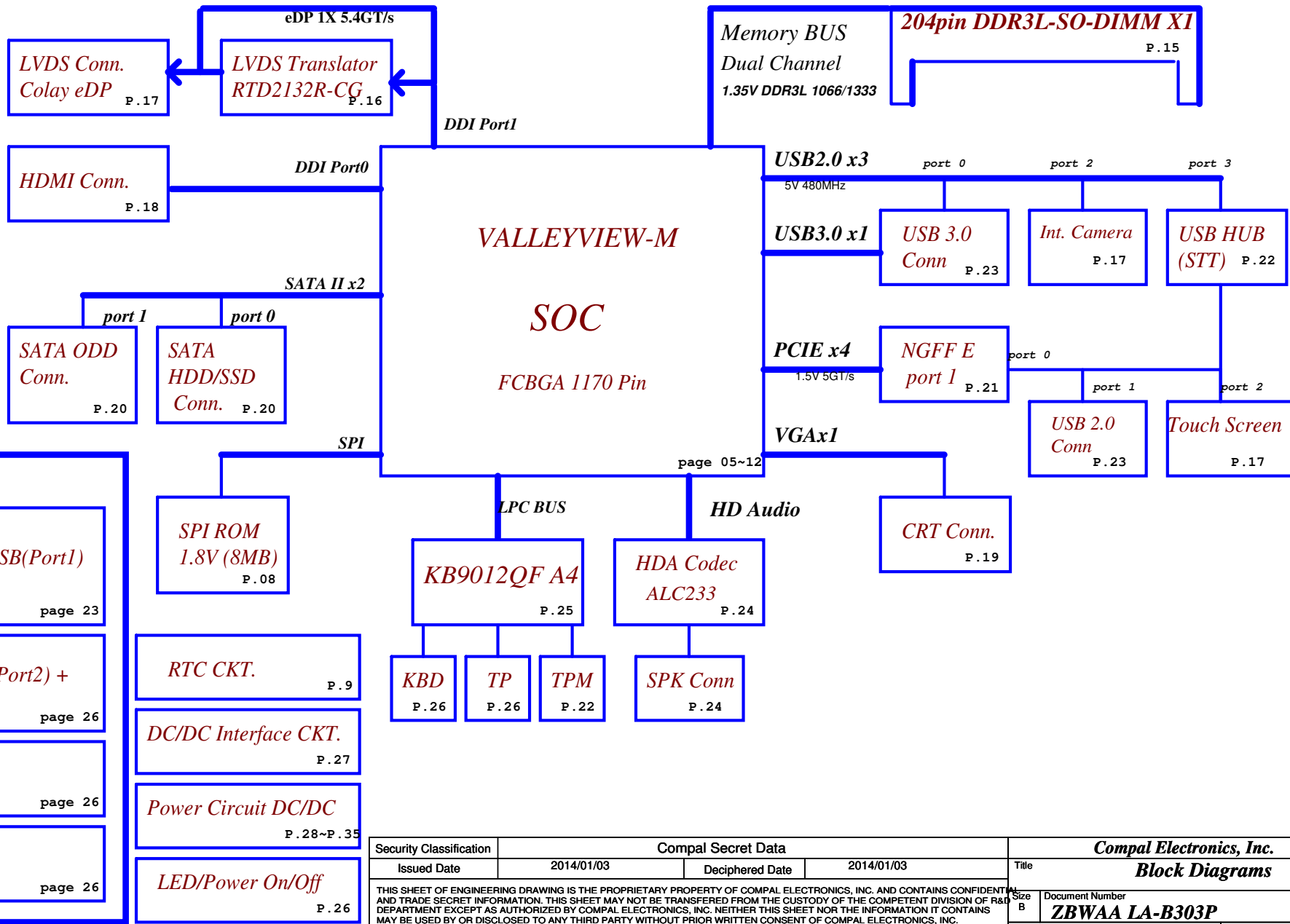
Bay Trail-M Platform with DDR3L

LA-B303P REV 1.0 Schematic

Intel BayTrail-M Platform

Date : 2014/02/22 Version 1.0

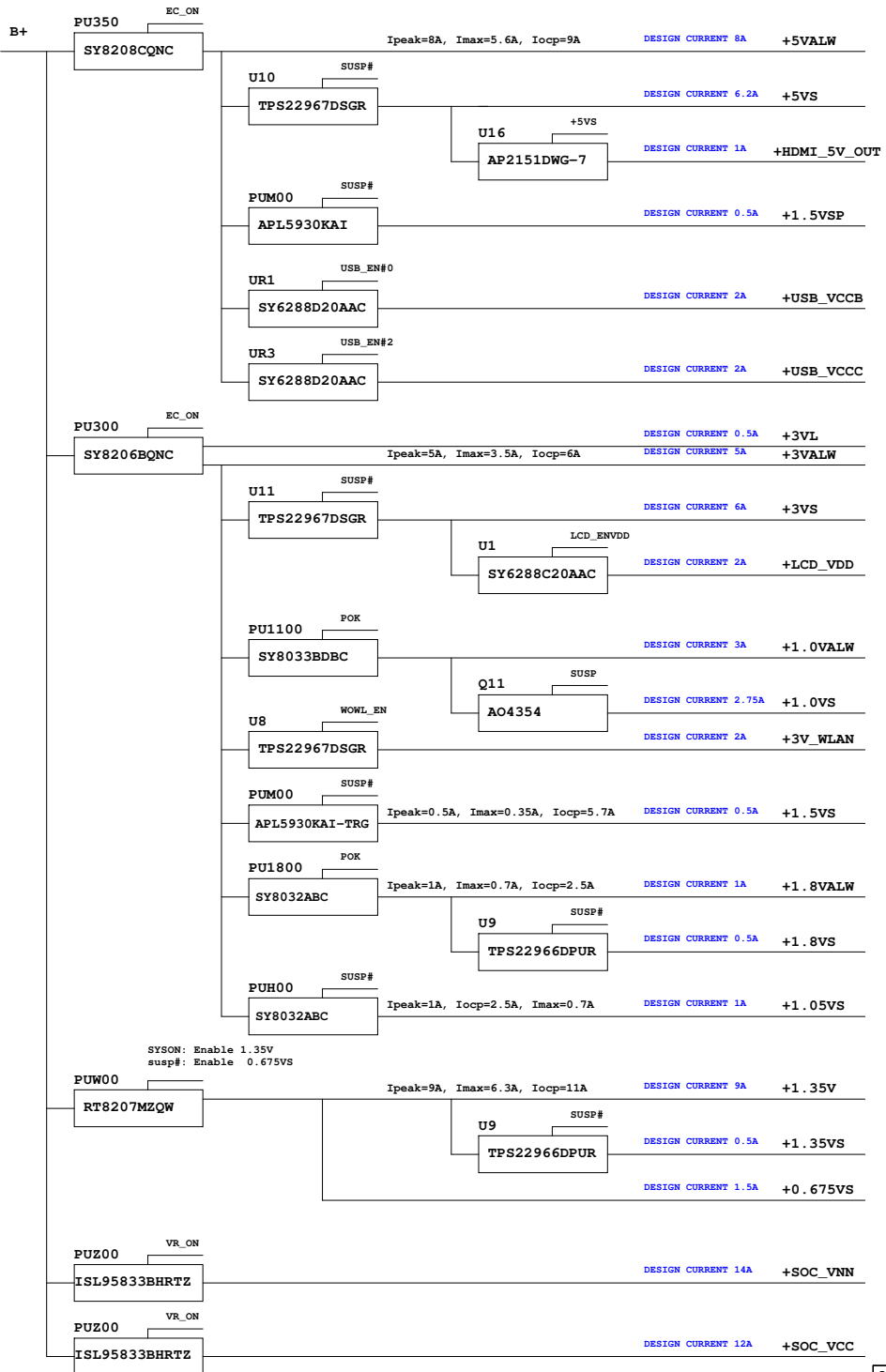
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				ZBWAA LA-B303P	1.0
				Date: Monday, March 03, 2014	Sheet 1 of 41



Sub Boards

- LS-B303P
LAN(PCIE Port0)+USB(Port1)
Audio Combo Jack
page 23
- LS-B304P
Card Reader(PCIE Port2) +
TP + Lid SW
page 26
- LS-B301P
LED B
page 26
- LS-B302P
Power Button B
page 26

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Date:	Monday, March 03, 2014	Sheet	2	of	41



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				ZBWAA LA-B303P	1.0
Date:	Monday, March 03, 2014	Sheet	3 of 41		

Voltage Rails

Power Plane	Description	S0	S3	S4/S5
VIN	19V Adapter power supply	ON	ON	ON
BATT+	12V Battery power supply	ON	ON	ON
B+	AC or battery power rail for power circuit. (19V/12V)	ON	ON	ON
+RTCVCC	Battery Power	ON	ON	ON
+1.0VALW	+1.0v Always power rail	ON	ON	ON
+1.8VALW	+1.8v Always power rail	ON	ON	ON
+3VALW	+3.3v Always power rail	ON	ON	ON
+5VALW	+5.0v Always power rail	ON	ON	ON
+1.35V	+1.35V power rail for DDR3L	ON	ON	OFF
+SOC_VCC	Core voltage for SOC	ON	OFF	OFF
+SOC_VNN	GFX voltage for SOC	ON	OFF	OFF
+0.675VS	+0.675V power rail for DDR3L Terminator	ON	OFF	OFF
+1.0VS	+1.0v system power rail	ON	OFF	OFF
+1.05VS	+1.05v system power rail	ON	OFF	OFF
+1.35VS	+1.35v system power rail	ON	OFF	OFF
+1.5VS	+1.5v system power rail	ON	OFF	OFF
+1.8VS	+1.8v system power rail	ON	OFF	OFF
+3VS	+3.3v system power rail	ON	OFF	OFF
+5VS	+5.0v system power rail	ON	OFF	OFF

Note : ON* means that this power plane is ON only with AC power available, otherwise it is OFF.

SOC SM Bus Address

Device	HEX	Address
SO-DIMM A (JDIMM1)	A0 H	1010 0000 b

EC SM Bus2 Address

Device	HEX	Address
Thermal sensor	4D H	01001101 b

EC SM Bus1 Address

Device	HEX	Address
Smart Battery	16 H	0001 0110 b
Smart Charger	12 H	0001 0010 b

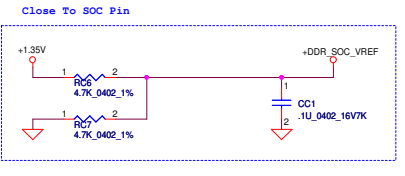
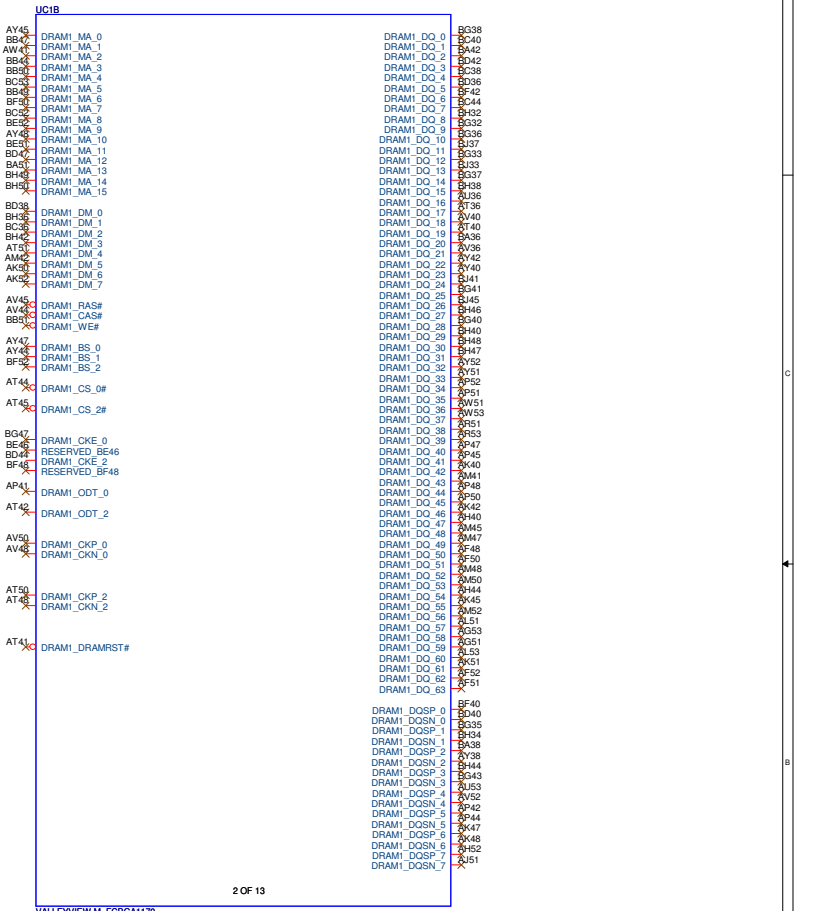
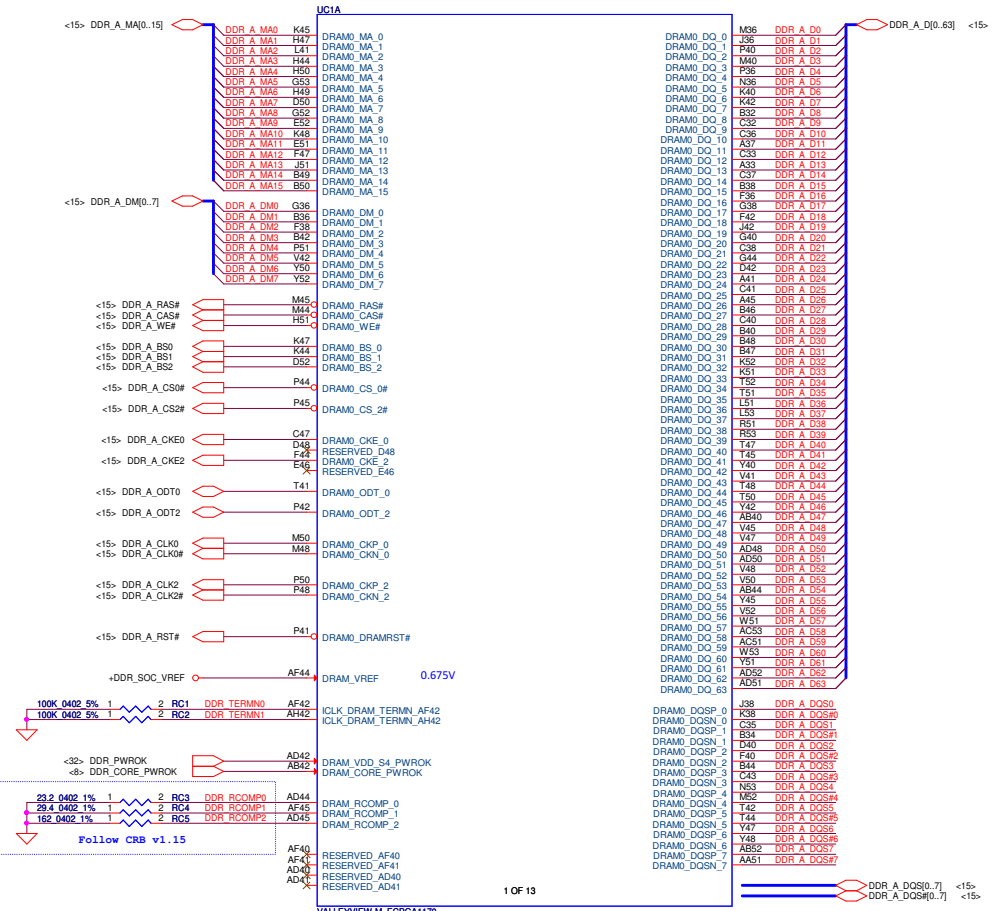
BOM Option Table

Item	BOM Structure
Unpop	@
Connector	CONN@
XDP (Debug Port)	XDP@
EMC requirement	EMC@
EMC requirement unpop	@ EMC@
EMI requirement	EMI@
EMI requirement unpop	@ EMI@
R short	RS@
Test Point	TEST@
ESD requirement	ESD@
ESD requirement unpop	@ ESD@
FAN	FAN@
HUB_24P requirement	HUB_24P@
HUB_28P requirement	HUB_28P@
LVDS requirement	LVDS@
EDP requirement	IEDP@
CRT requirement	CRT@
Thermal sensor requirement	Thermal@
ISCT requirement	ISCT@
NOISCT requirement	NOISCT@
TPM requirement	TPM@
CRT EMI requirement	CRT@ EMI@
Camera EMI requirement	CAM_EMI@
FIX code requirement	FIX@
HDMI requirement	HDMI45@
9012 requirement	9012@
9022 requirement	9022@
TPM EMC requirement	TPM@ EMC@

43 level BOM table

43 Level	Description	BOM Structure
	SMT MB LA-B303P ZBWAA BAY TRAIL M	ESD@/EMC@/FAN@/XDP@/LVDS@

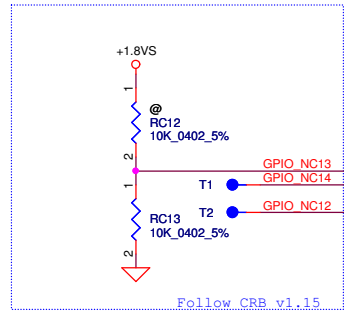
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				Document Number
				ZBWAA LA-B303P
				Date: Monday, March 03, 2014
				Sheet 4 of 41
				Rev 1.0



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Date: Monday, March 03, 2014				Rev 1.0
				Sheet 5 of 41

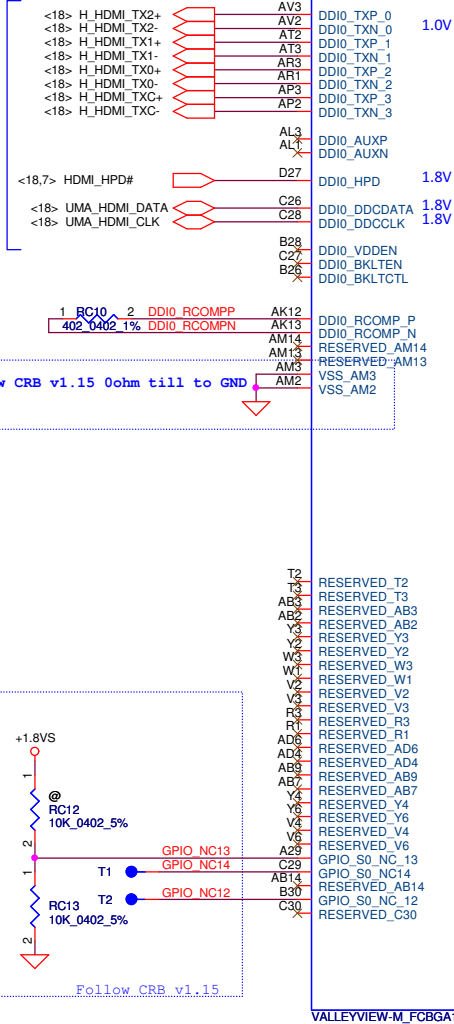
HDMI

Follow CRB v1.15 0ohm till to GND



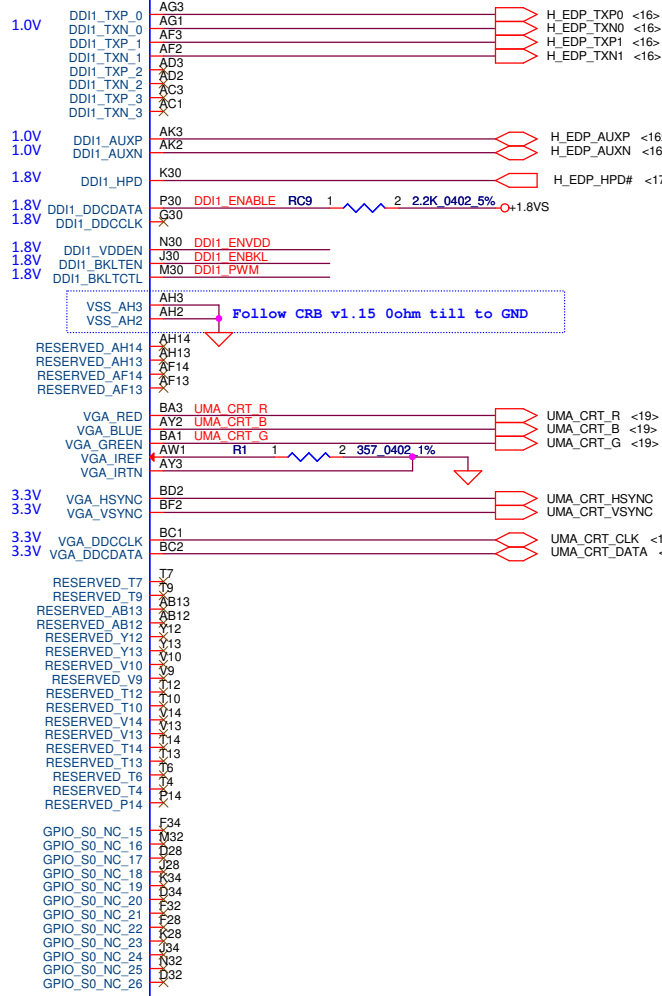
GPIO_S0_NC[13]:
Multiplexed with Hardware Straps Pin:MDSI_DDCDATA

UC1C



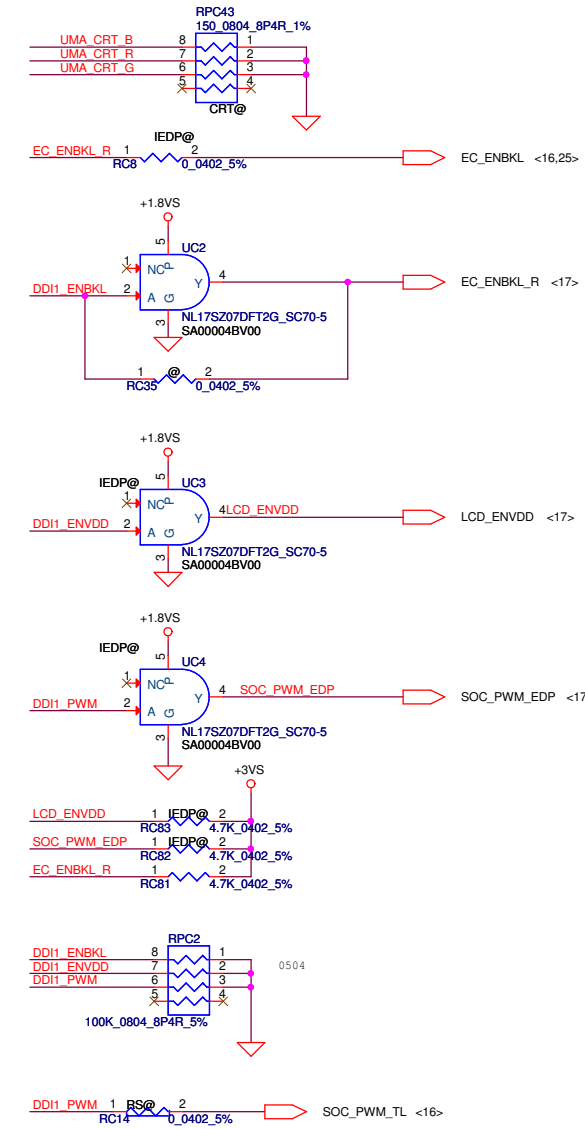
VALLEYVIEW-M_FCBGA1170

3 OF 10



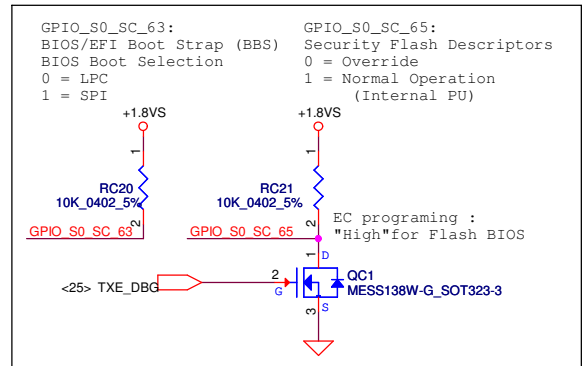
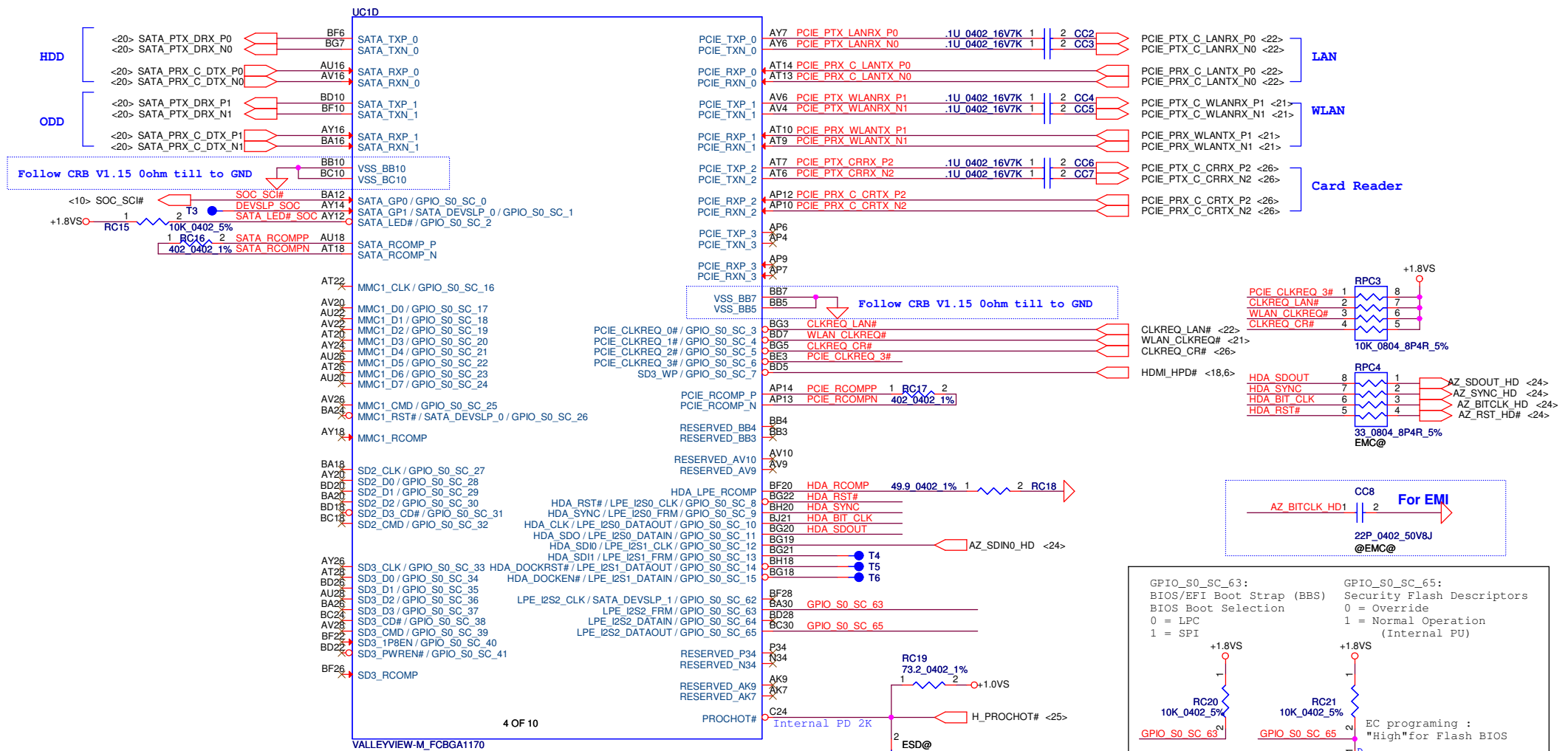
eDP

CRT

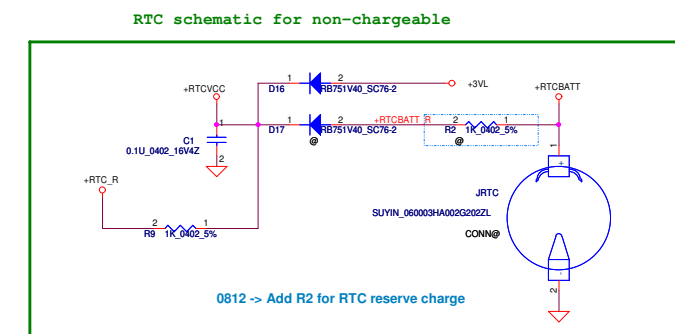
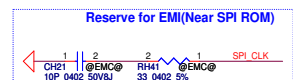
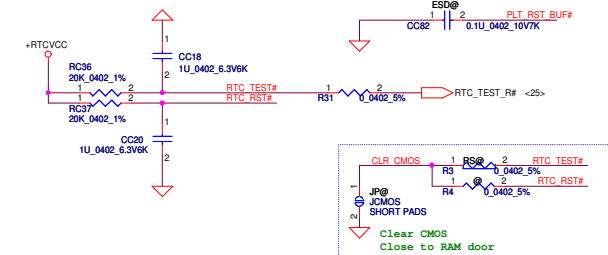
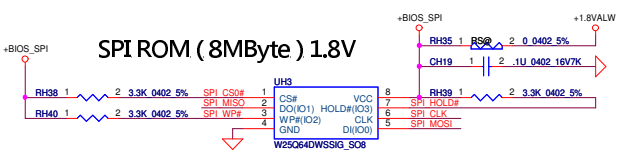
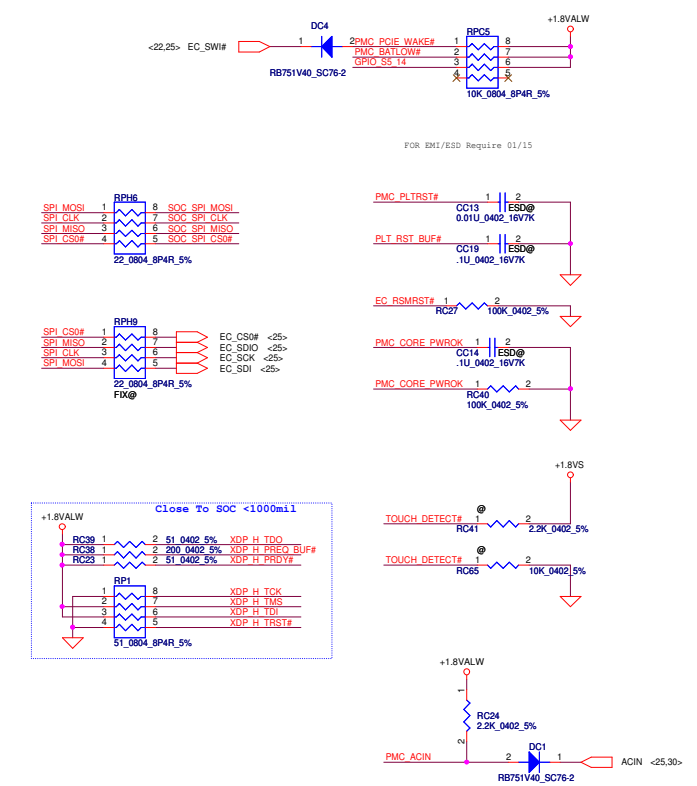
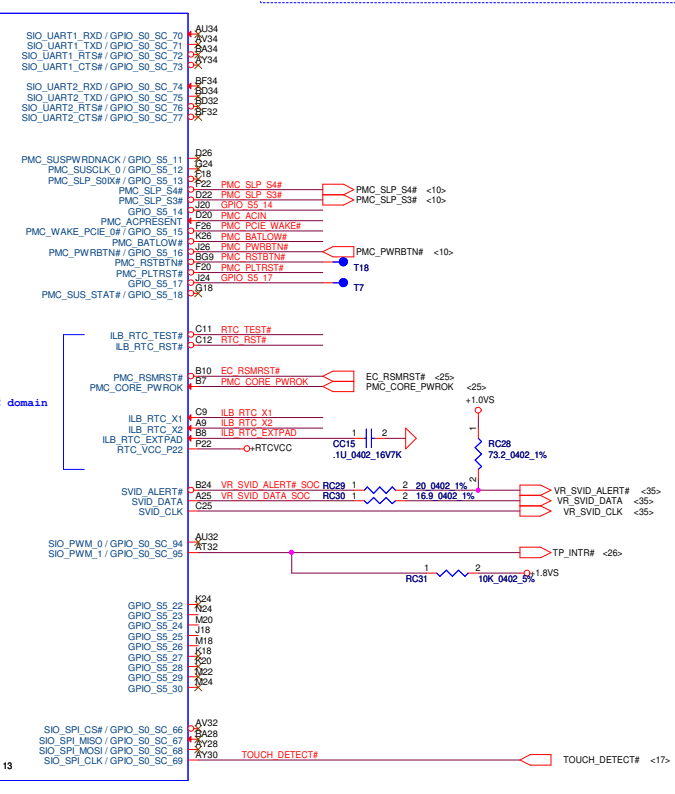
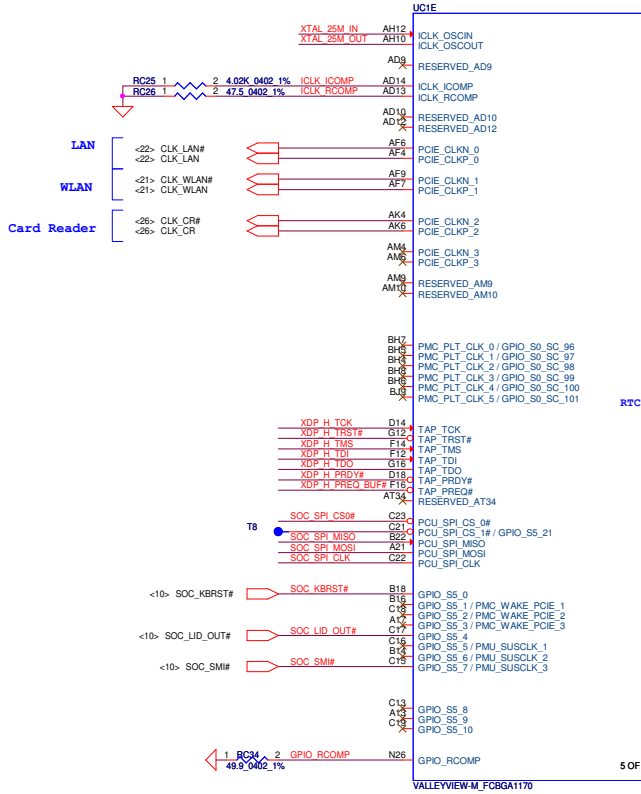
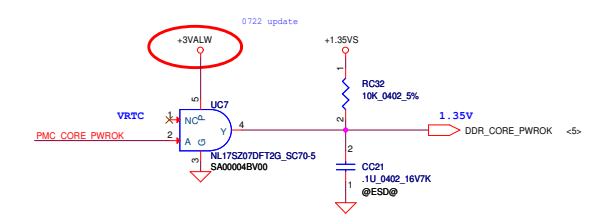
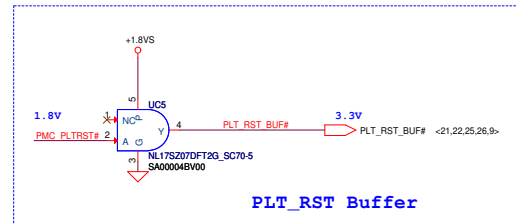
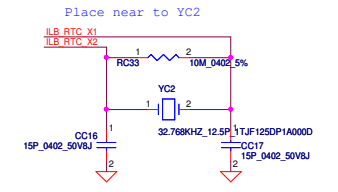
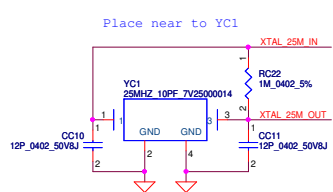


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Date: Monday, March 03, 2014			Sheet 6 of 41	

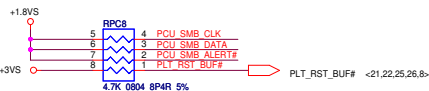
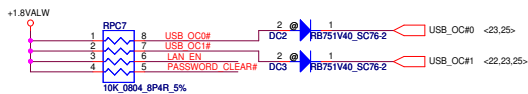
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				ZBWAA LA-B303P	1.0
				Date: Monday, March 03, 2014	Sheet 7 of 41



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Issued Date	2014/01/03	Deciphered Date	2014/01/03
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Size	C	Document Number	ZBWAA LA-B303P
Date	Monday, March 03, 2014	Sheet	8 of 41



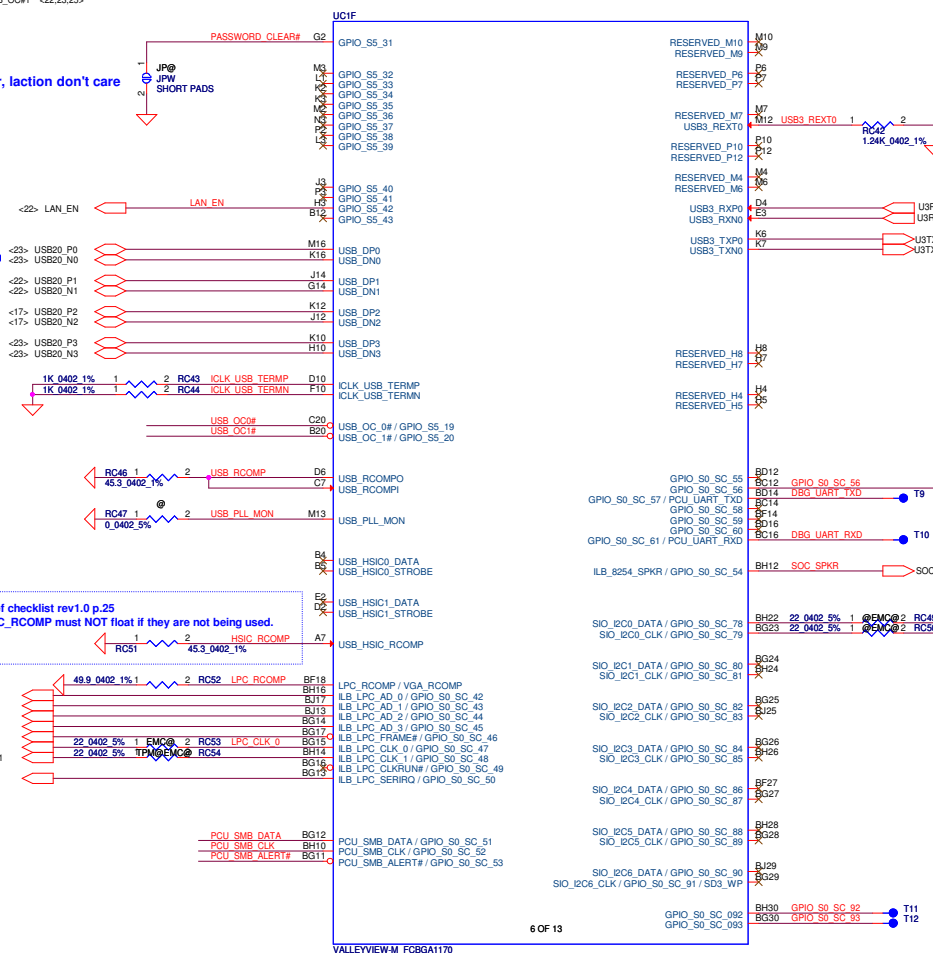
no DDR door, laction don't care

RIGHT PORT FRONT(3.0)

LEFT PORT(2.0)

Camera

USB Hub

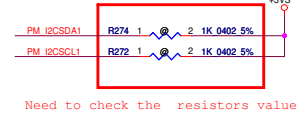
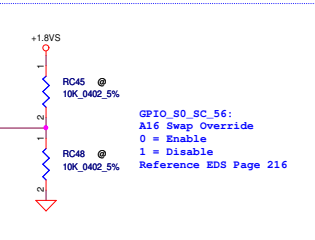


RIGHT PORT FRONT(3.0)

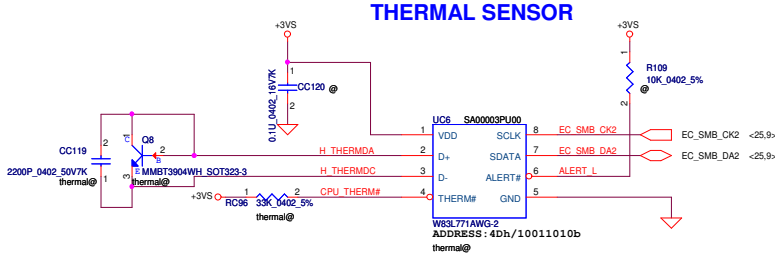
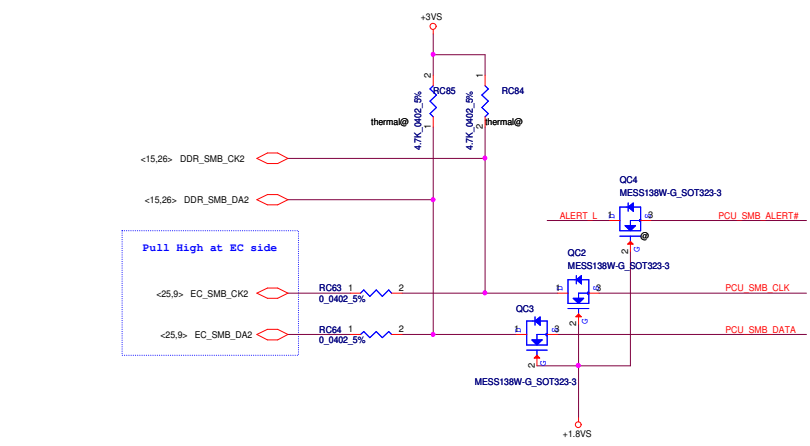
NOTE: Ref checklist rev1.0 p.25
 USB_HSIC_RCOMP must NOT float if they are not being used.

ILB_LPC_CLK_0 : Output of 25MHz,
 Need Check with EC

ILB_LPC_CLK_1 is for CLK_0 feedback. (Input)
 Set to Output for Normal Usage

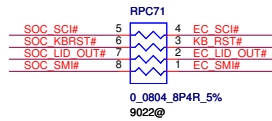
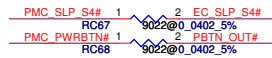
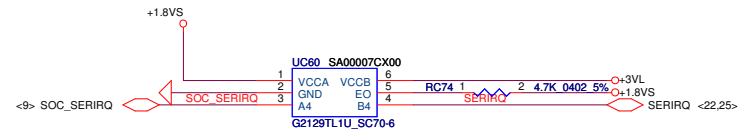
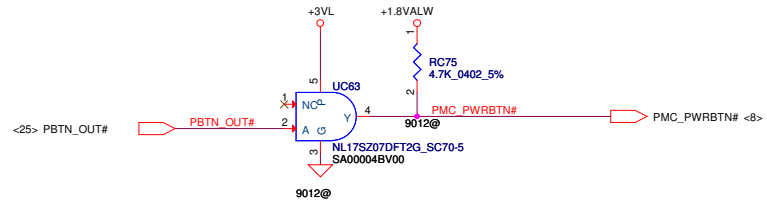
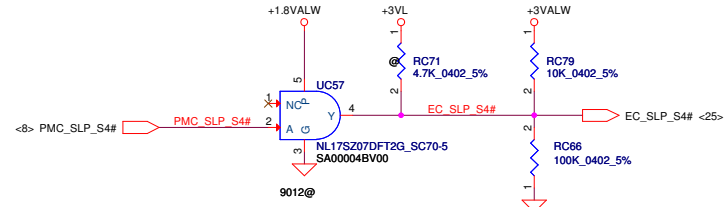
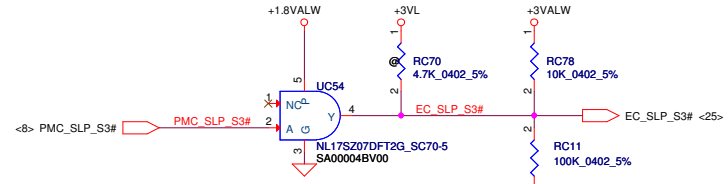
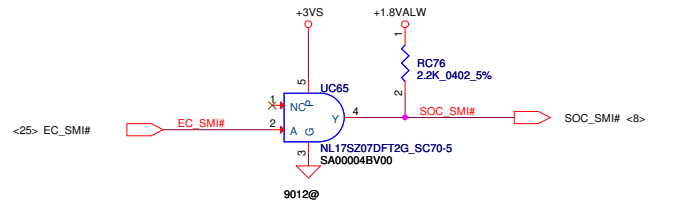
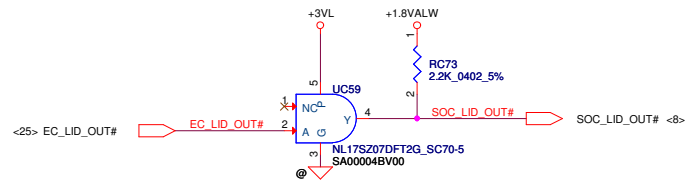
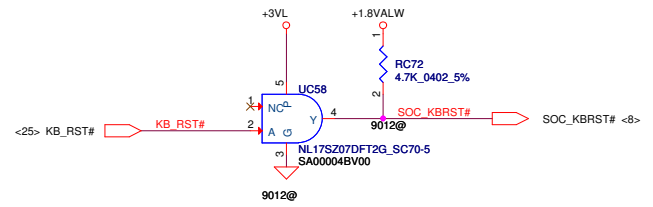
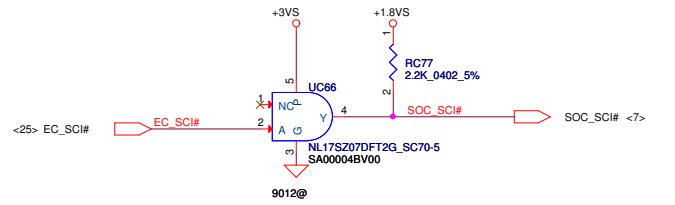


Need to check the resistors value

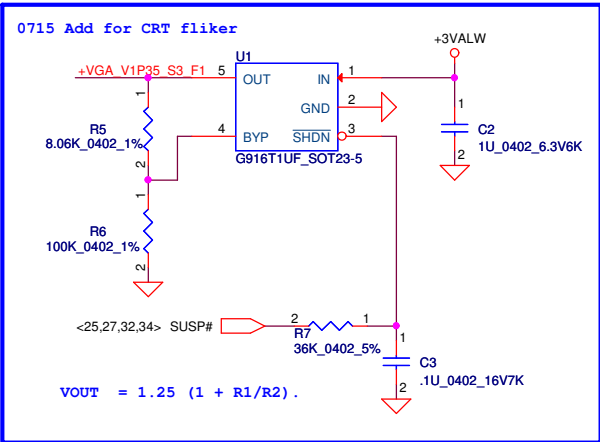
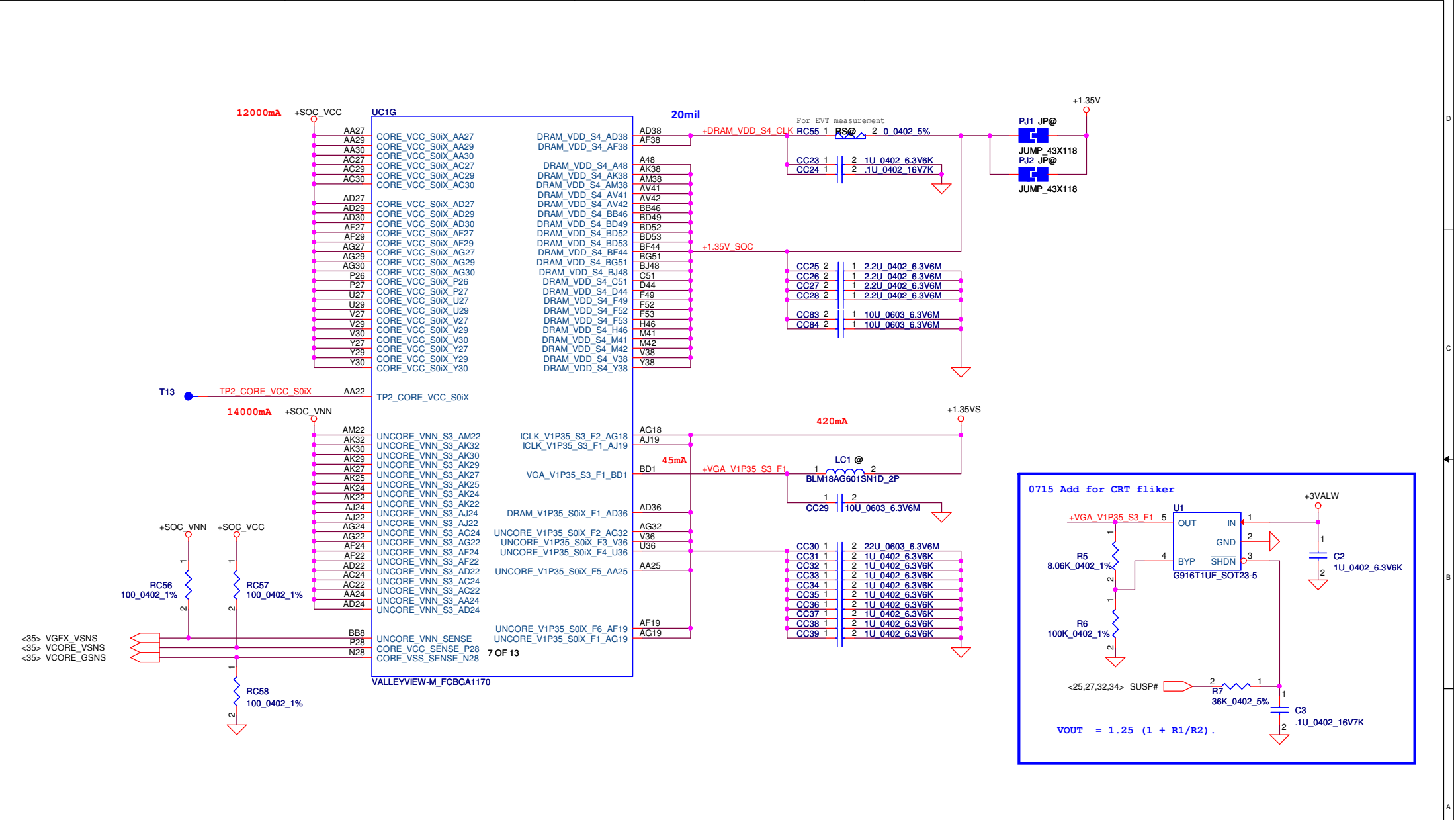


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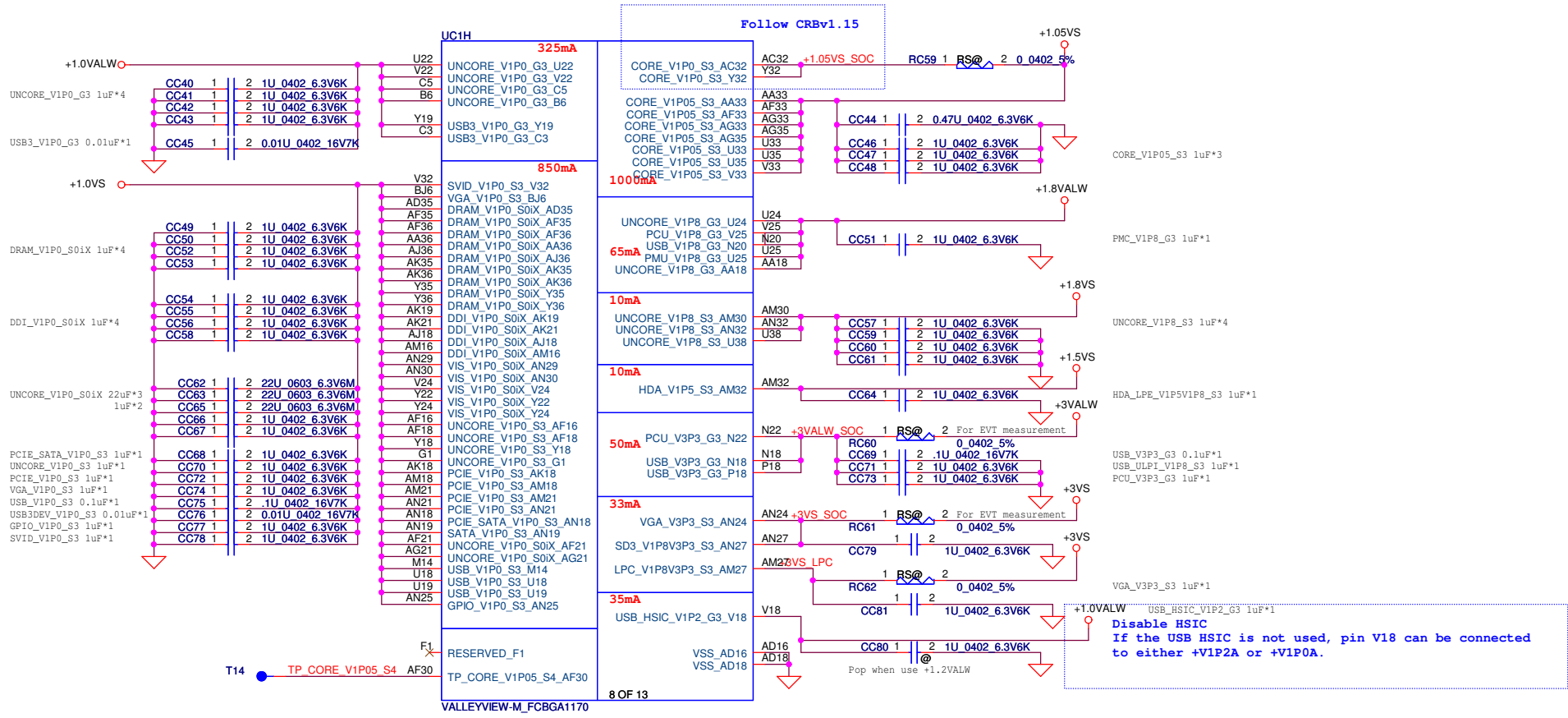
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				VLV-M SOC USB/LPC/SMBus
Size	C	Document Number	ZBWAA LA-B303P	Rev
Date	Monday, March 03, 2014	Sheet	9 of 41	1.0



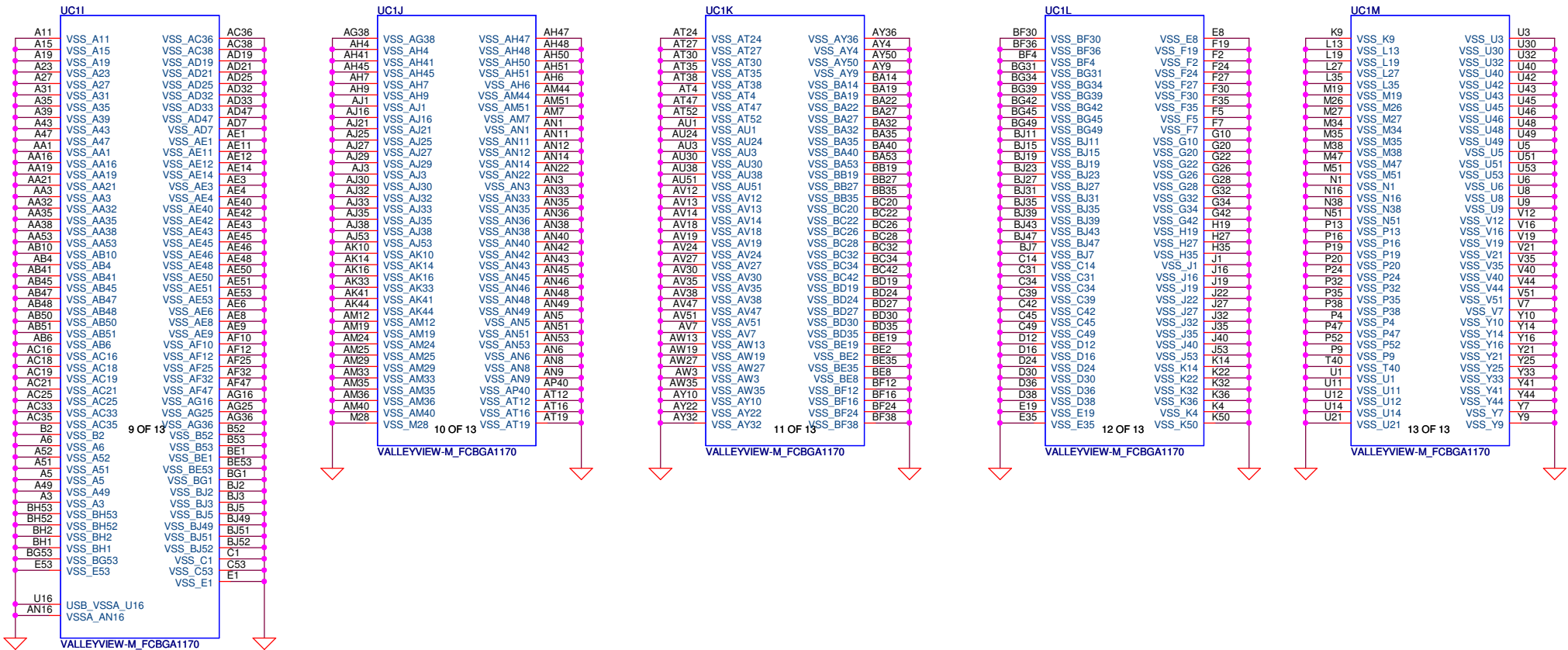
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Issued Date	2013/10/16	Deciphered Date	2014/10/16	VLV-M SOC Level Shifter	
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Date: Monday, March 03, 2014				Sheet	10 of 41



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				Date Monday, March 03, 2014	Sheet 11 of 41



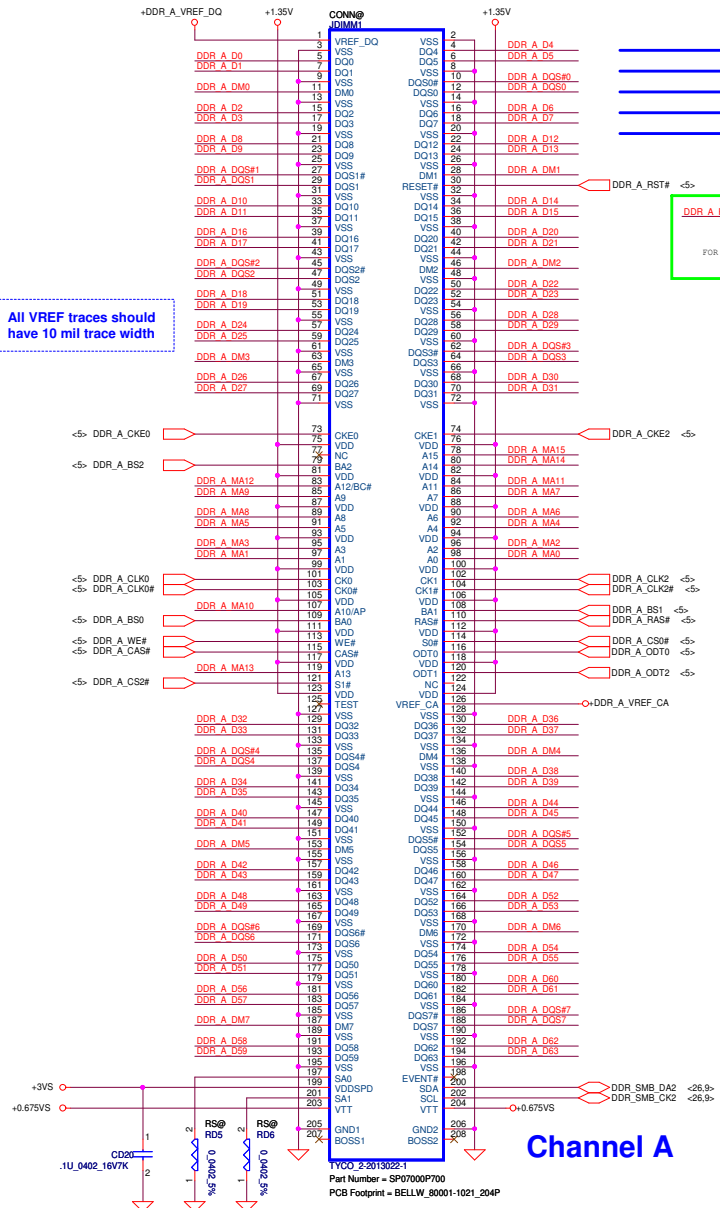
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				Date:	Monday, March 03, 2014
				Sheet	12 of 41
				Rev	1.0



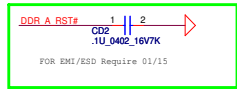
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Size	Document Number	Rev			
B	ZBWAA LA-B303P	1.0	Date:	Monday, March 03, 2014	Sheet 13 of 41

Remove debug connector

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Issued Date	2014/01/03	Deciphered Date	2014/01/03	Title VLV-M SOC Debug
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				Document Number ZBWAA LA-B303P
Date: Monday, March 03, 2014			Sheet 14 of 41	



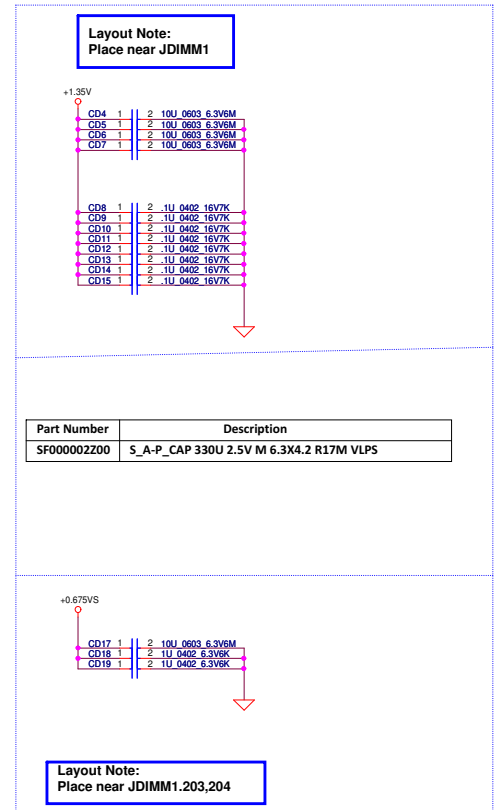
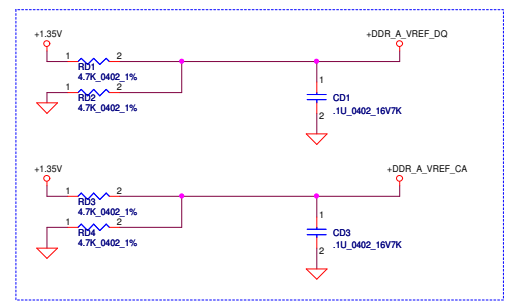
All VREF traces should have 10 mil trace width

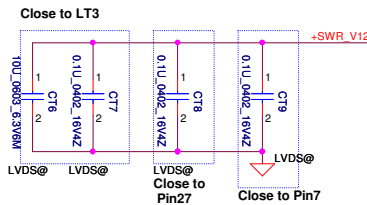
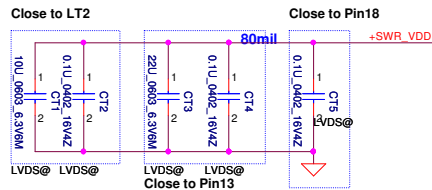
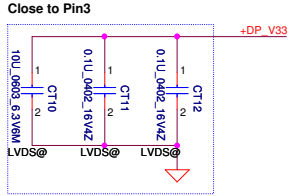
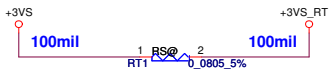


TYCO 2-2018022-1
Part Number = SP07000P700
PCB Footprint = BELLW_80001-1021_204P

<Address: SA1:SA0=00 (A0H)>
DIMM_1 STD H:4mm

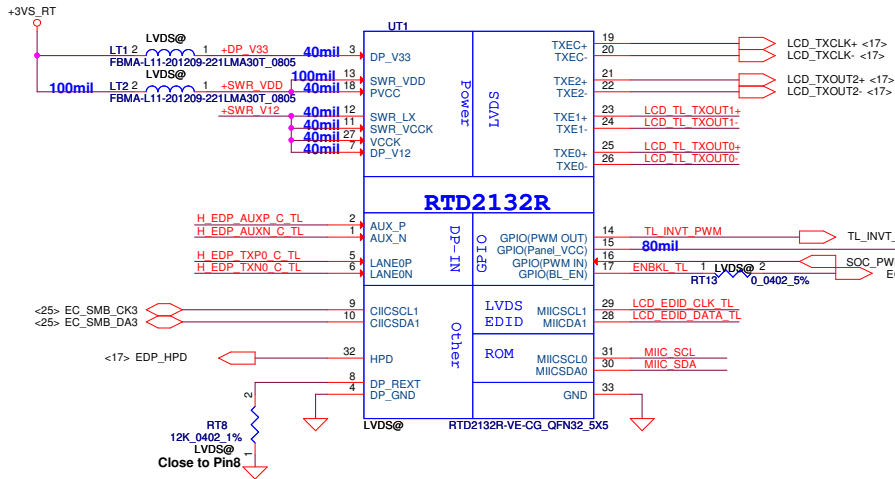
Signal voltage level = 0.675 V
PLACE TWO 4.7K RESISTORS CLOSE TO DIMMS ON DIMM_VREF_CA / DIMM_VREF_DQ
Decoupling caps are needed; one 0.1 µF placed close to VREF pins of each DDR3 SODIMM.





SWR / LDO Mode select

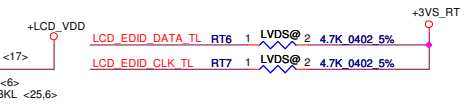
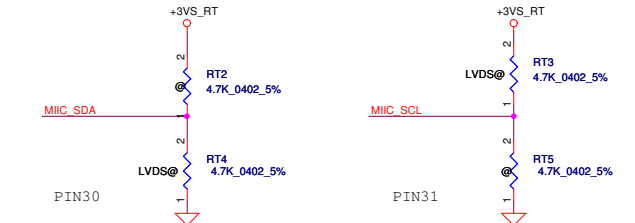
※LDO mode is adopted as default power regulator mode. Also can implement SWR mode by add inductor.



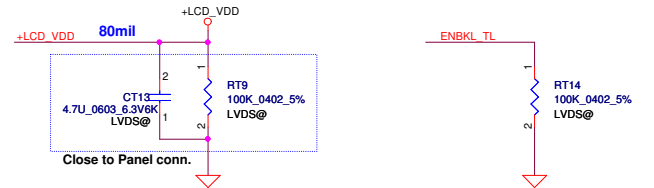
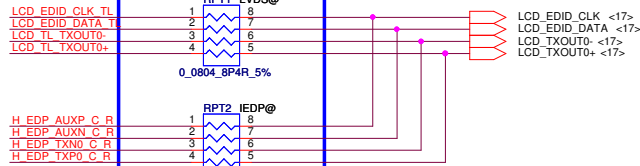
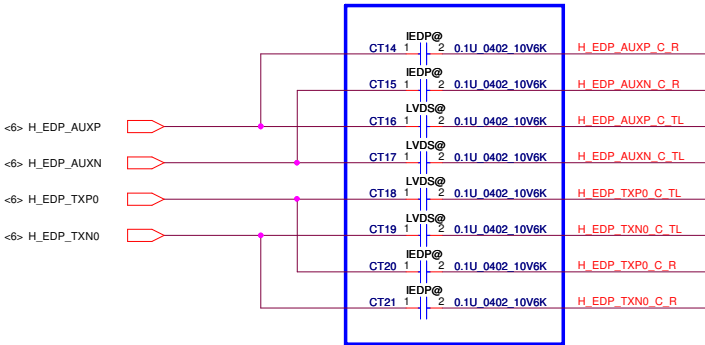
Mode Configure

※ROM only mode : PIN 30 4.7k pull low, Pin 31 4.7k pull high.
 EP mode : PIN 30 4.7k pull high, Pin 31 4.7k pull low.
 EEPROM : PIN 30 4.7k pull high, Pin 31 4.7k pull high.

< ※Default mode >



SOC_PWM_TL 100k pull down resistance close to cpu side



Place co-lay Resistor back to back on TOP and BOT

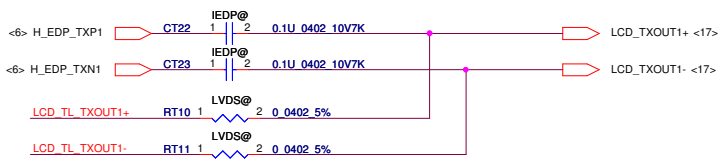
	PIN15
2132S	TL_ENVDD
2132R	+LCD_VDD *

* Version R internal Power Switch, can output 1A, Rds(on)=0.2 ohm

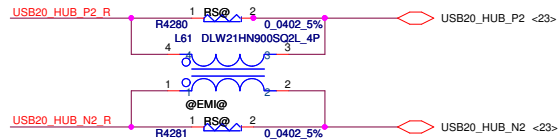
PIN16	Accept voltage input (high level)
2132S	3.3V
2132R	1.5-3.3V

* Version R has internal level shifter, remove level shifter circuit on AMD platform

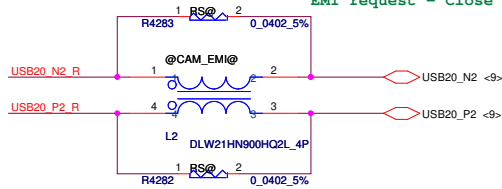
Different between 2132S and 2132R	
2132S	2132R
1. Support SWR mode	1. Support LDO mode and SWR mode 2. Internal ROM 3. Support LCD_VDD(internal Power switch) 4. Integrates Level shifter



BTO : TOUCH_EMI@

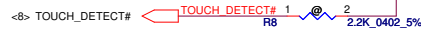
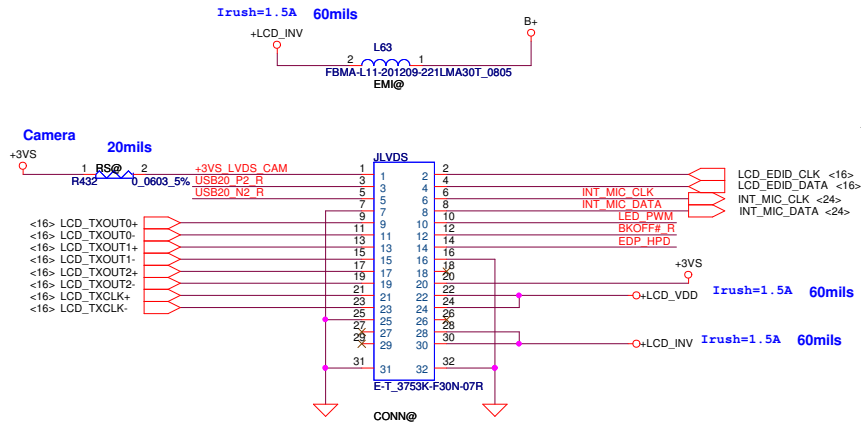


EMI request - Close to JEDP connector



LVDS colay eDP cable

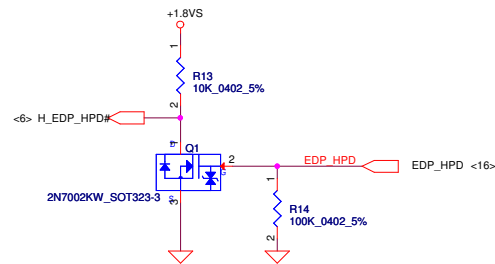
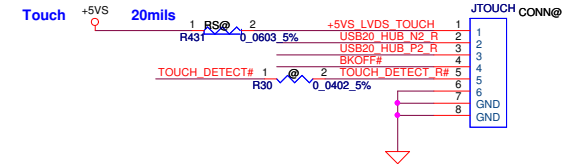
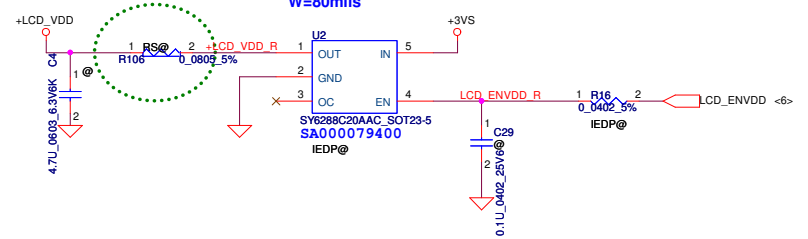
Pin define will be change after ME ready



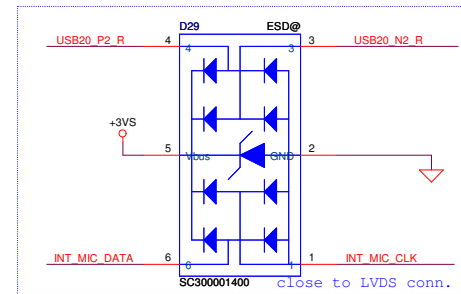
LCD POWER CIRCUIT (For EDP panel only)

Reserver for power consumption
Remove on Pre MP phase

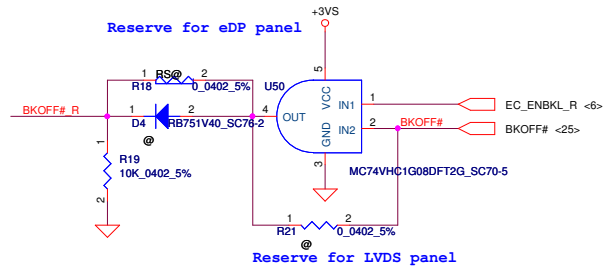
I_{rush}=2A
W=80mils



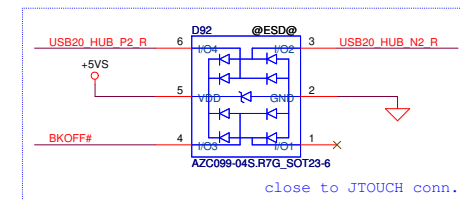
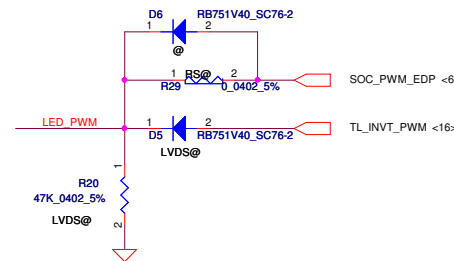
Camera & MIC



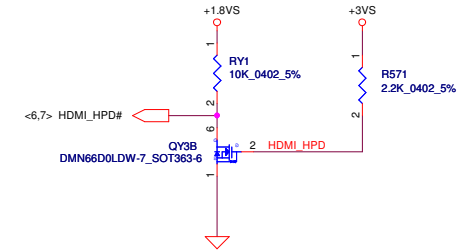
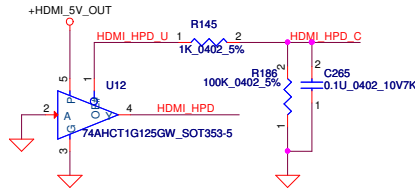
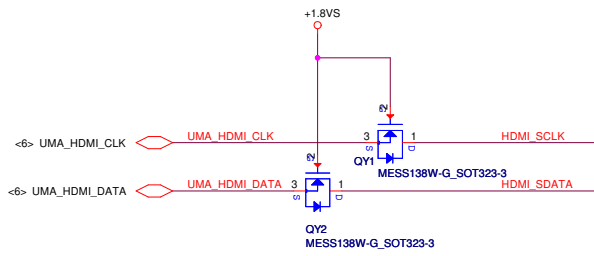
Reserve for eDP panel



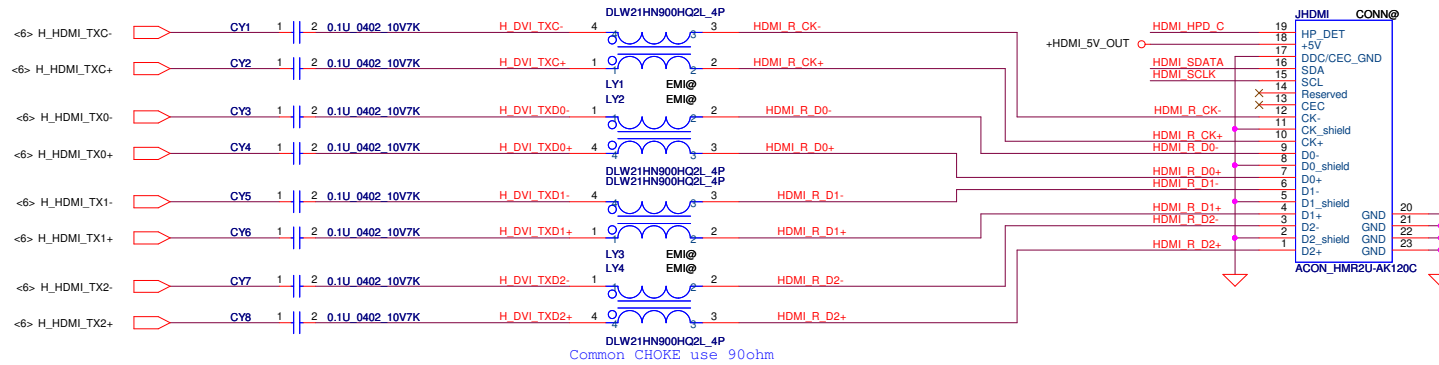
Reserve for LVDS panel



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Issued Date	2014/01/03	Deciphered Date	2014/01/03	LVDS
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				Rev 1.0 Page 17 of 41



HDMI Connector



HDMI Royalty

ZZZ1 HDMI45@

RO0000003HM

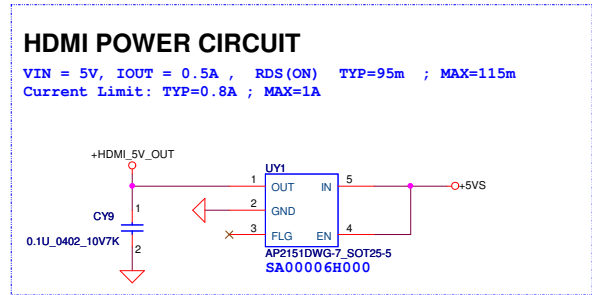
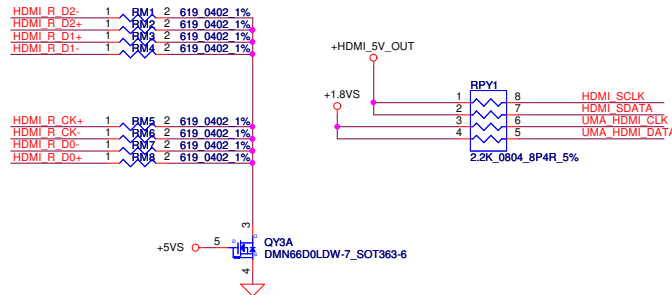
HDMI W/Logo + HDCP

HDMI W/O Logo: RO0000001HM

HDMI W/Logo: RO0000002HM

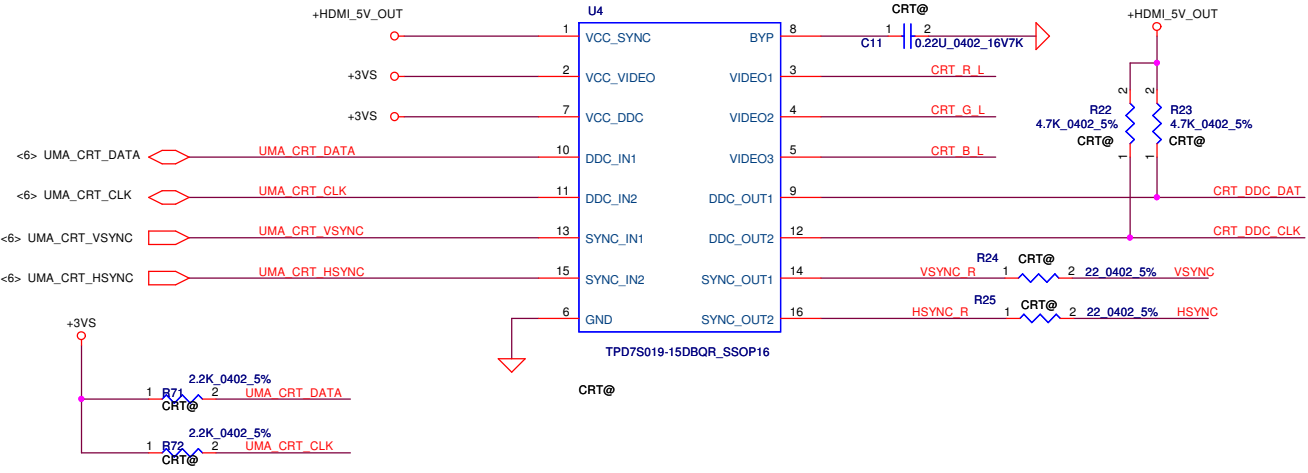
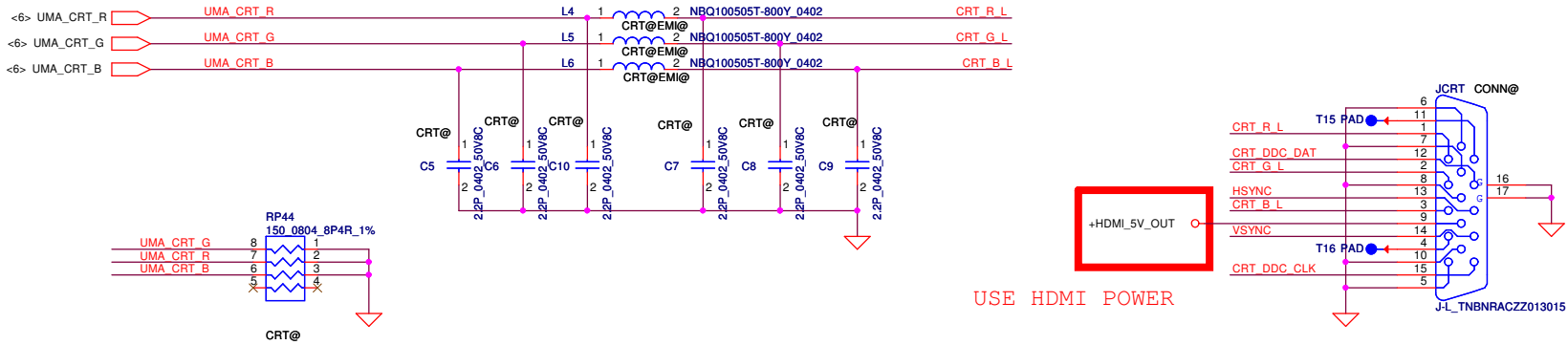
HDMI W/Logo + HDCP: RO0000003HM

please manually load
this virtual material to 45@ BOM



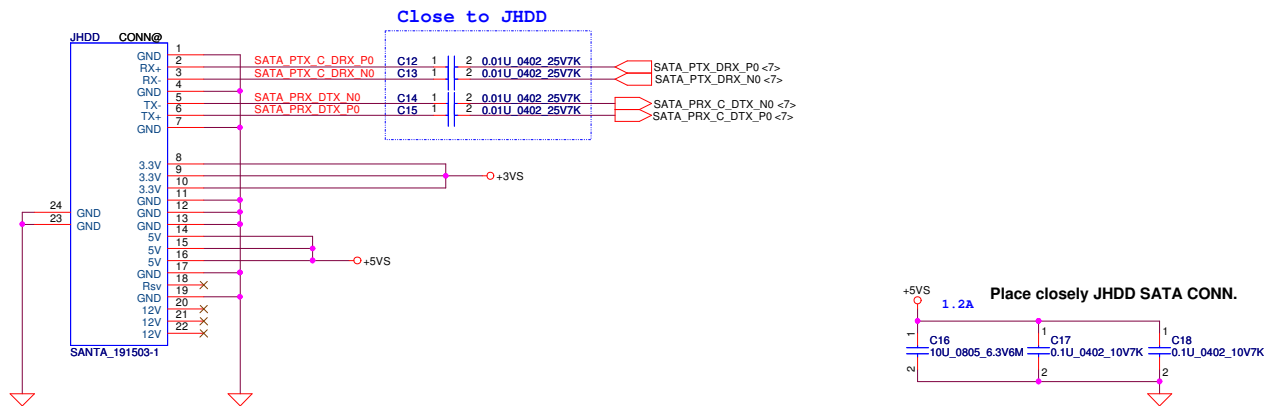
Security Classification	Compal Secret Data		Title	
Issued Date	2014/01/03	Deciphered Date	2014/01/03	HDMI Conn.
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				ZBWAA LA-B303P
				Rev 1.0
Date: Monday, March 03, 2014				Sheet 18 of 41

CRT CONNECTOR



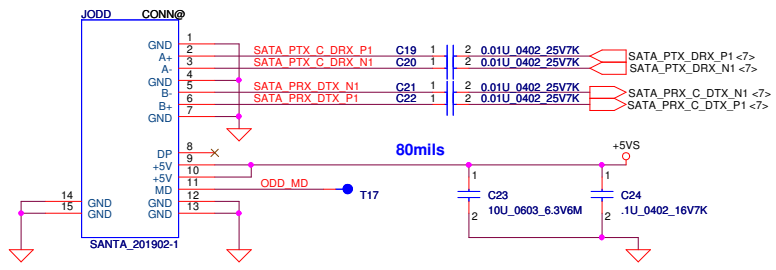
Security Classification		Compal Secret Data		Compal Electronics, Inc.	
Issued Date	2013/09/25	Deciphered Date	2016/09/25	Title	
				CRT	
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				ZBWAA LA-B303P	
				Date:	Monday, March 03, 2014
				Sheet	19 of 41
				Rev	1.0

SATA HDD/SSD Conn.

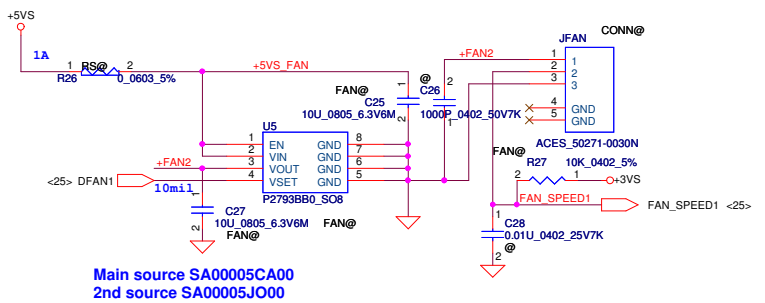


SATA ODD Conn

Power Consumption	
Peak	1800 mA
Read (CD)	1100 mA
Read (DVD)	950 mA
Write	1300 mA
Standby	20mA



FAN Control Circuit



Security Classification	Compal Secret Data		Compal Electronics, Inc.	
Issued Date	2013/09/25	Deciphered Date	2016/09/25	Title
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				Rev
				1.0
				Date: Monday, March 03, 2014
				Sheet 20 of 41

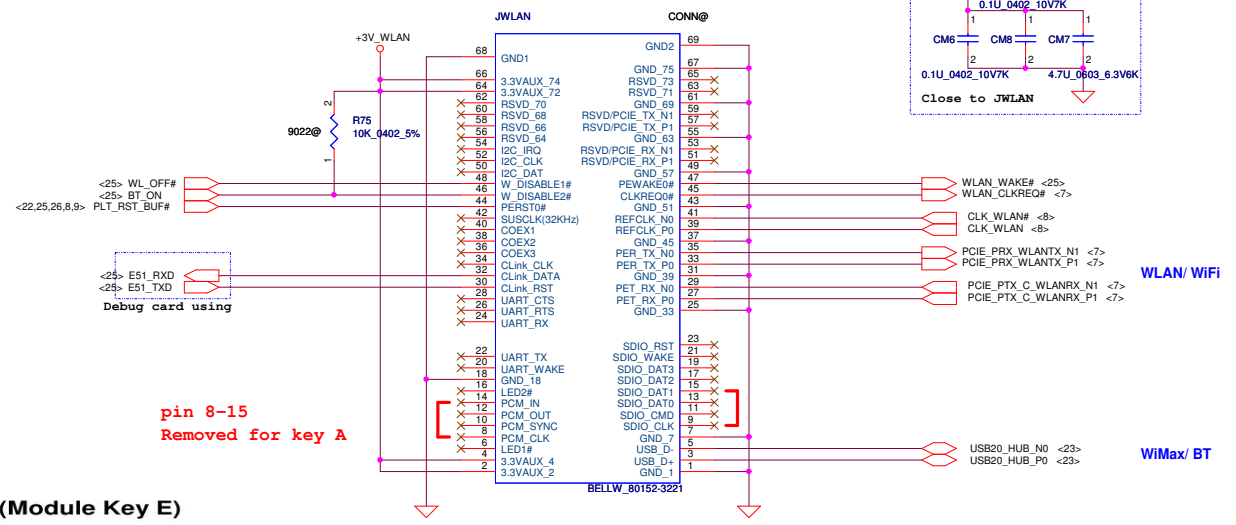
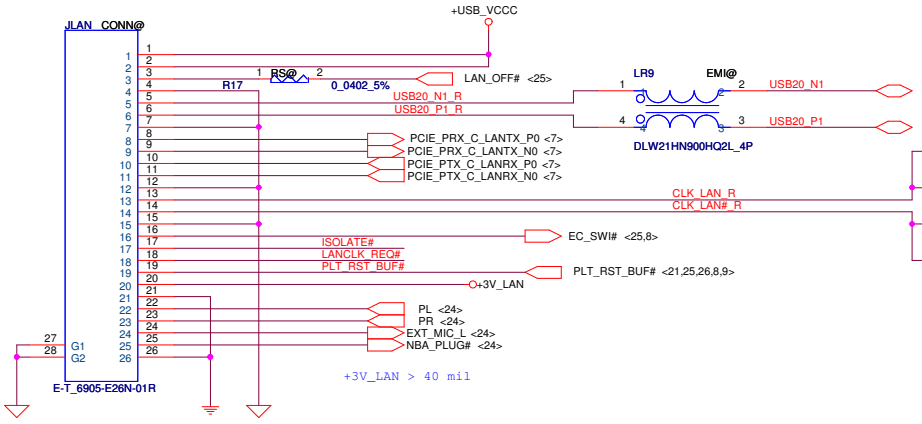


Table 23. SDIO Based Module Solution Pinout (Module Key E)

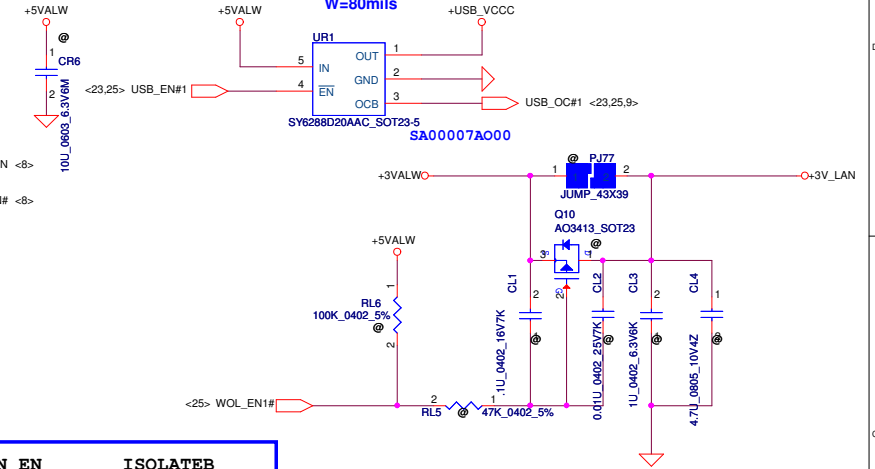
74	3.3V	GND	75
72	3.3V	RESERVED/REFCLKN1	73
70	UIM_Power_In/GPIO1/PEWake1#	RESERVED/REFCLKP1	71
68	UIM_Power_Out/CLKREQ1#	GND	69
66	UIM_SWP/PERST1#	Reserved/PETn1	67
64	RESERVED	Reserved/PETp1	65
62	ALERT# (O)(0/3.3)	GND	63
60	I2C CLK (I)(0/3.3)	Reserved/PERn1	61
58	I2C DATA (IO)(0/3.3)	Reserved/PERp1	59
56	W_DISABLE#1 (I)(0/3.3V)	GND	57
54	Reserved/W_DISABLE#2 (I)(0/3.3V)	PEWake0# (IO)(0/3.3V)	55
52	PERST0# (O)(0/3.3V)	CLKREQ0# (IO)(0/3.3V)	53
50	SUSCLK(32kHz) (I)(0/3.3V)	GND	51
48	COEX1 (I/O)(0/1.8V)	REFCLKN0	49
46	COEX2(I/O)(0/1.8V)	REFCLKP0	47
44	COEX3(I/O)(0/1.8V)	GND	45
42	VENDOR DEFINED	PETn0	43
40	VENDOR DEFINED	PETp0	41
38	VENDOR DEFINED	GND	39
36	UART CTS (I)(0/1.8V)	PERn0	37
34	UART RTS (O)(0/1.8V)	PERp0	35
32	UART Rx (I)(0/1.8V)	GND	33
	Module Key	Module Key	
	Module Key	Module Key	
	Module Key	Module Key	
	Module Key	Module Key	
22	UART Tx (O)(0/1.8V)	SDIO Reset(I)(0/1.8V)	23
20	UART Wake (O)(0/3.3V)	SDIO Wake(O)(0/1.8V)	21
18	GND	SDIO DAT3(IO)(0/1.8V)	19
16	LED#2 (O)(OD)	SDIO DAT2(IO)(0/1.8V)	17
14	PCM_IN/125 SD_IN (I)(0/1.8V)	SDIO DAT1(IO)(0/1.8V)	15
12	PCM_OUT/125 SD_OUT (O)(0/1.8V)	SDIO DAT0(IO)(0/1.8V)	13
10	PCM_SYNC/125 WS (IO)(0/1.8V)	SDIO CMD(IO)(0/1.8V)	11
8	PCM_CLK/125 SCK (IO)(0/1.8V)	SDIO CLK(I)(0/1.8V)	9
6	LED#1 (O)(OD)	GND	7
4	3.3V	USB_D-	5
2	3.3V	USB_D+	3
		GND	1

LAN/USB Small board Conn

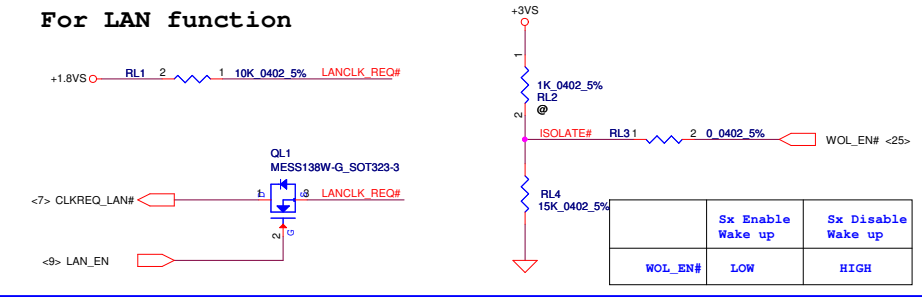


Left USB 2.0 x 1

Current Limit 2A



For LAN function



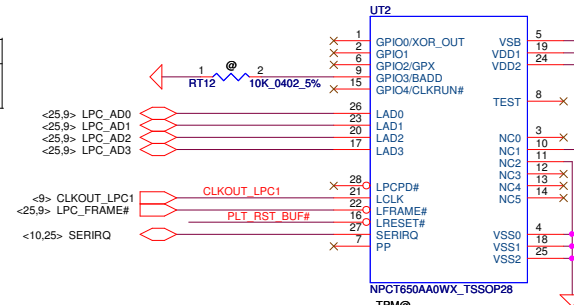
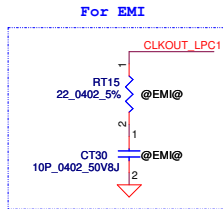
LAN	WOL	LAN_EN		ISOLATEB	
		S0	Sx	S0	Sx
0	0	0	0	1	1
0	1	0	0	1	1
1	0	1	1	1	1
1	1	1	1	1	0*

*
 S3: after SUSP# assert low over 100ms
 S4/S5: after SYSON assert low over 100ms

+3V_LAN rising time (10%-90%) need > 1ms and <100ms.

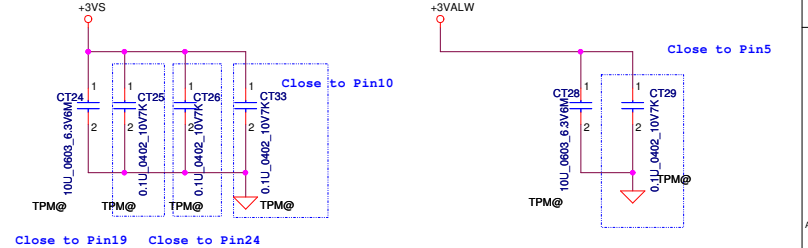
TPM

BADD	ADDRESS
0	EEh - EFh
* Floating	7Eh - 7Fh



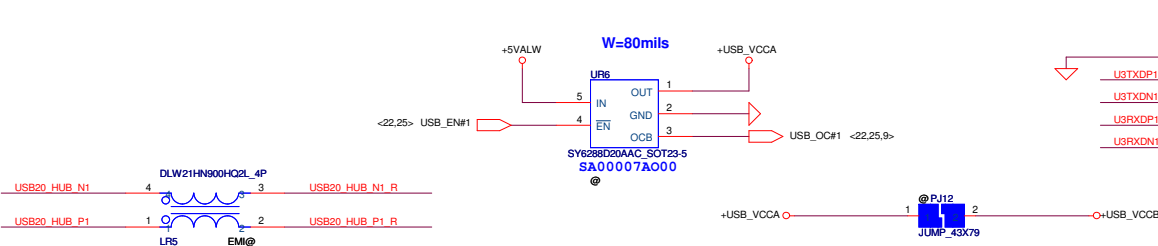
Pin10 connect to +3VS for co-lay with NTPC7620

Pin11 connect to GND for co-lay with NTPC7620

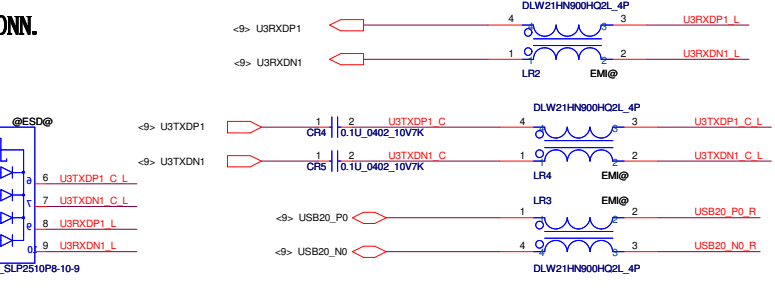


RIGHT REAR USB2.0 CONN.

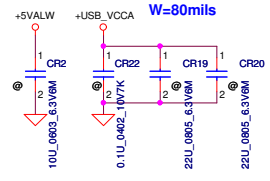
Current Limit 2A



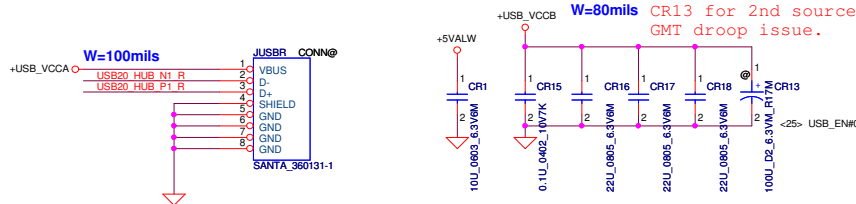
RIGHT FRONT USB3.0 CONN.



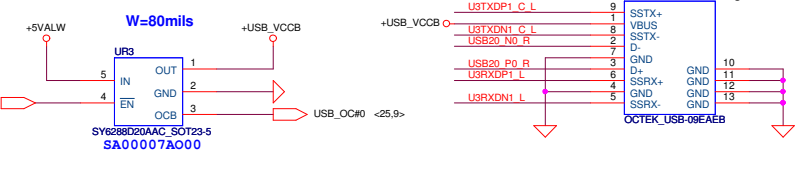
CLOSE UR6



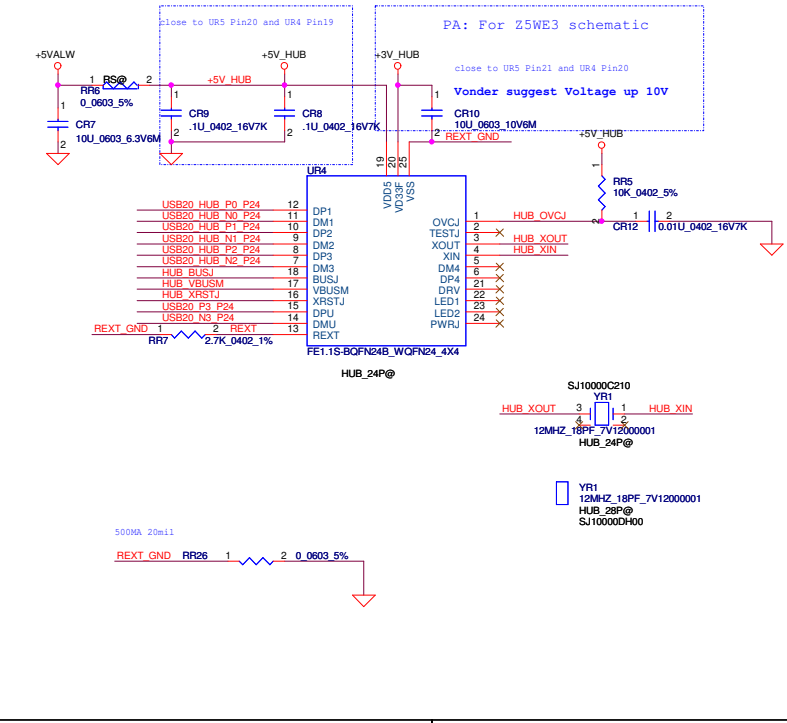
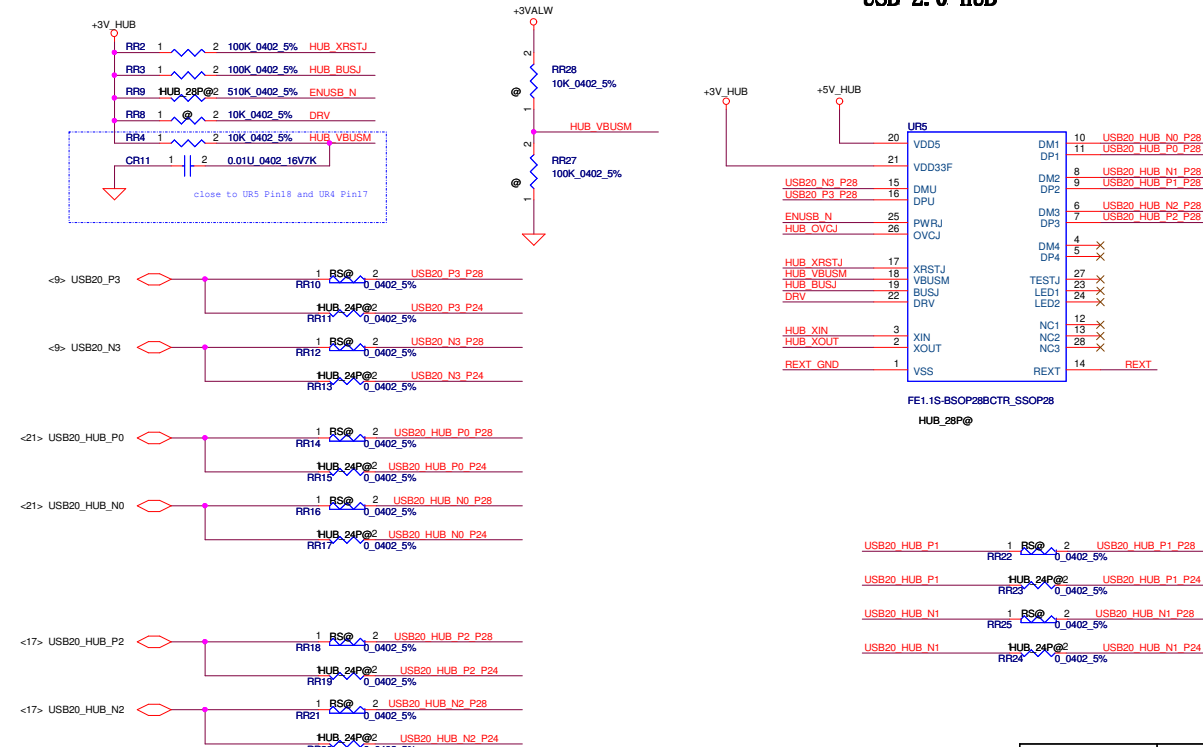
CLOSE UR3

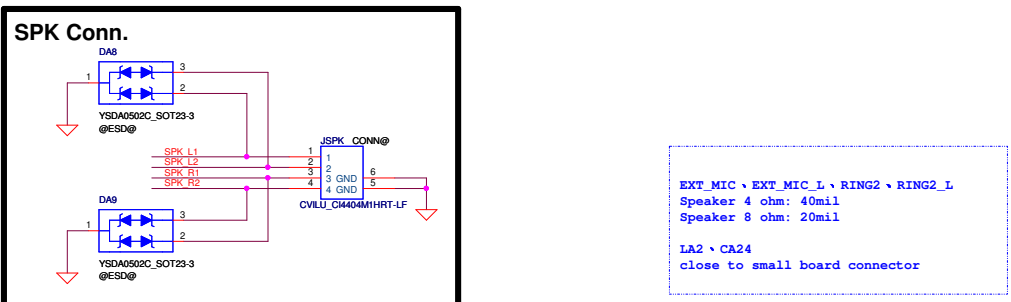
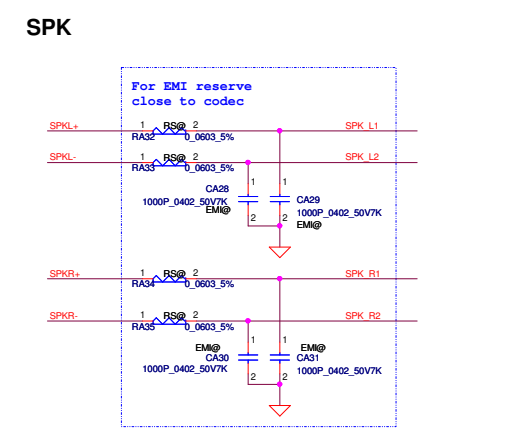
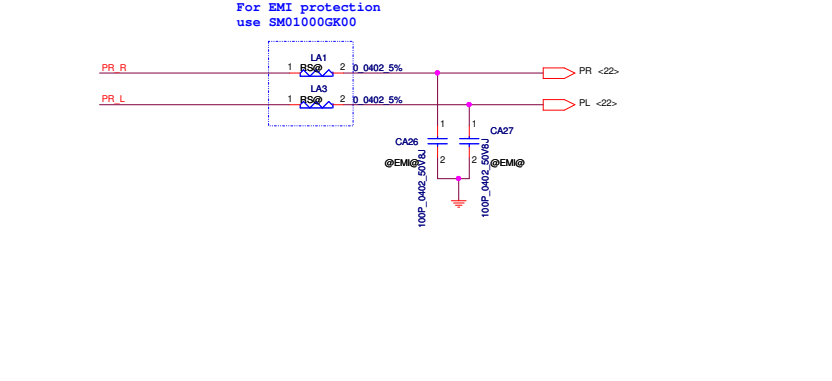
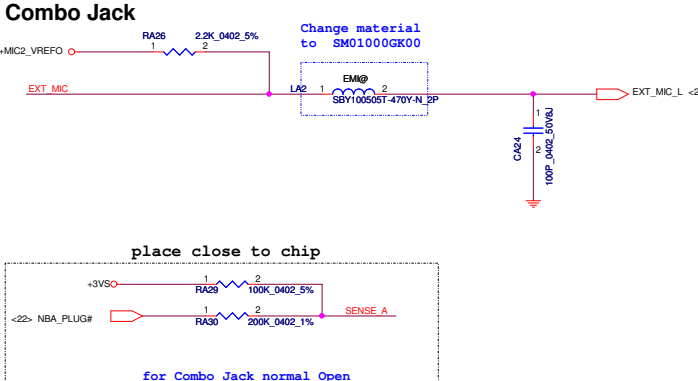
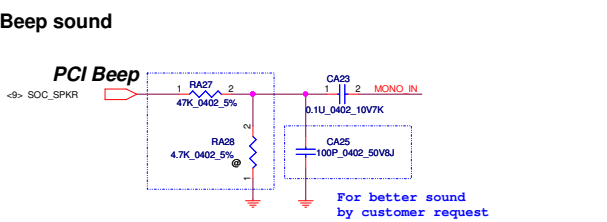
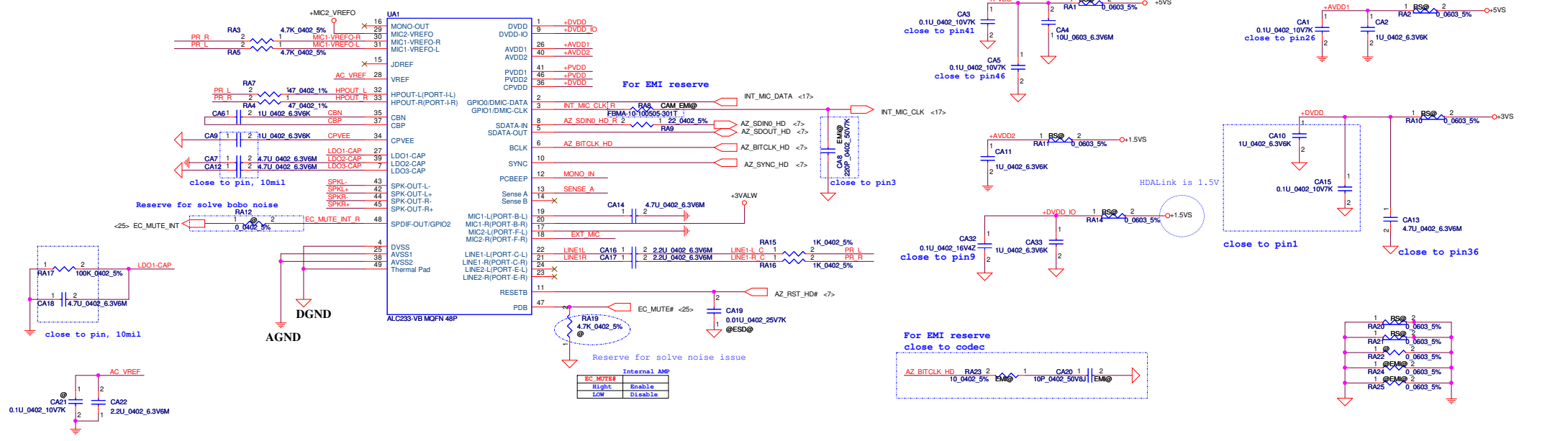


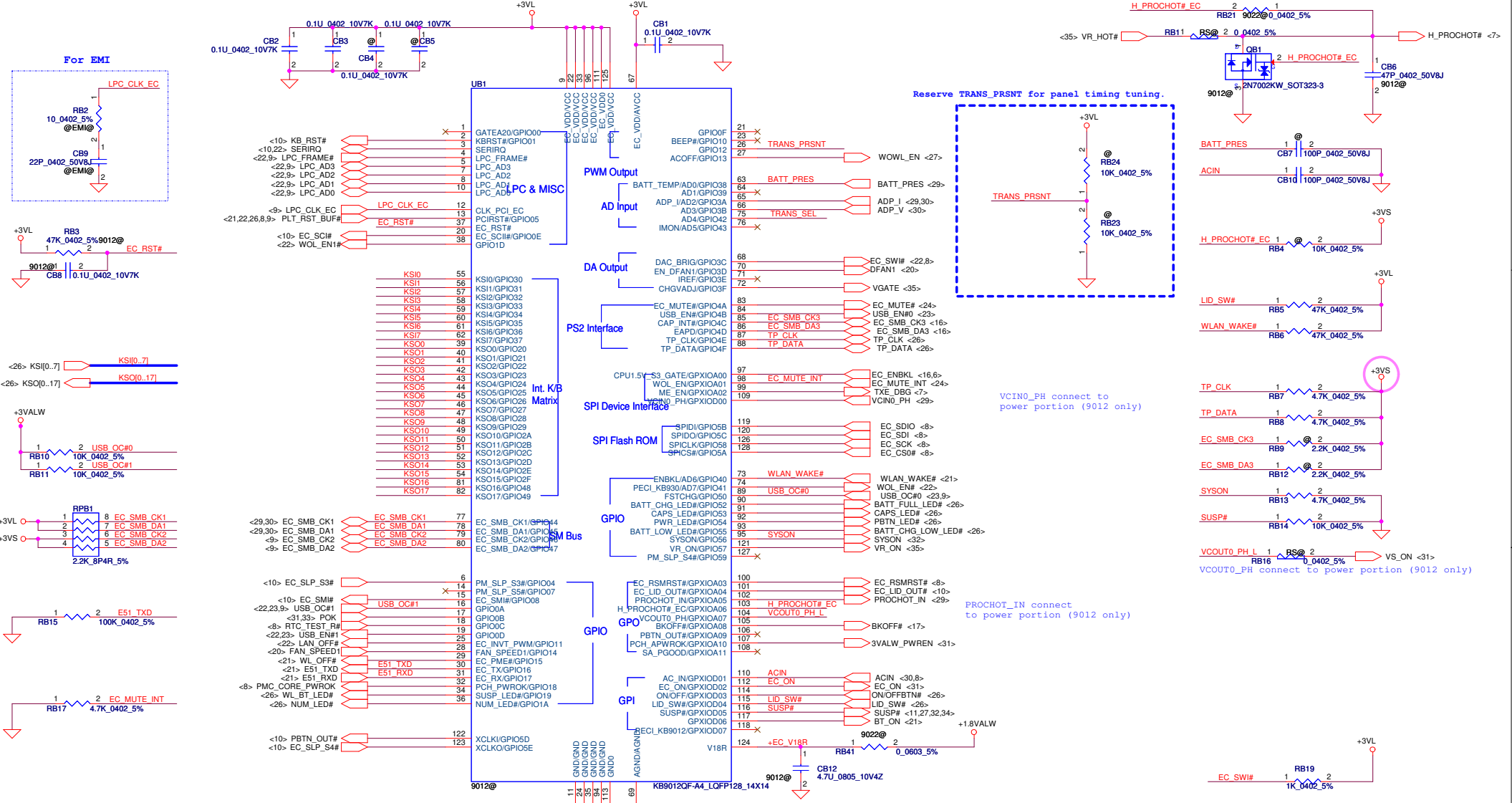
Current Limit 2A



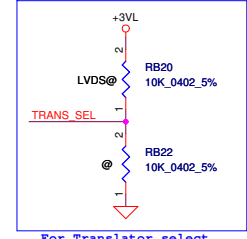
USB 2.0 HUB







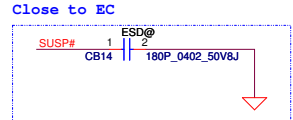
Signal pull high is default status (ROM only mode).
If signal pull low, EC will send translator code to chip.(EP mode)



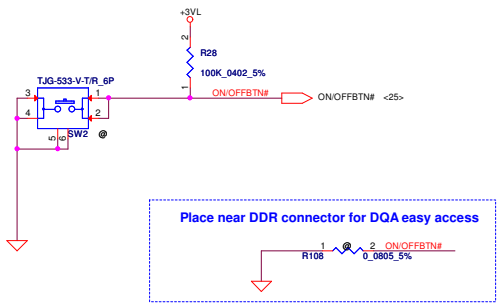
Voltage Comparator Pins FOR 9012 A3

Pin	>1.2V	<1.2V
VCIN0 pin109	HIGH	LOW
VCIN1 pin102	HIGH (default)	LOW
VCOUT0 pin104	HIGH	LOW
VCOUT1 pin103	HIGH	LOW (default)

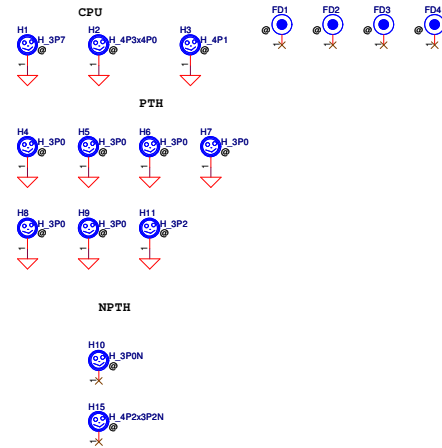
UB1
SiC KB9022QC LQFP 128P EC CONTROLLER
9022@
SA000075S20



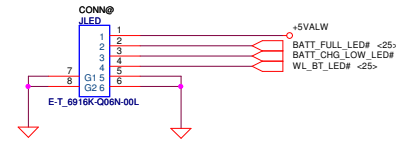
Power Button



Screw Hole PCB Fedical Mark PAD

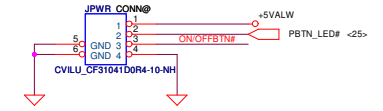


LED Small board to Conn

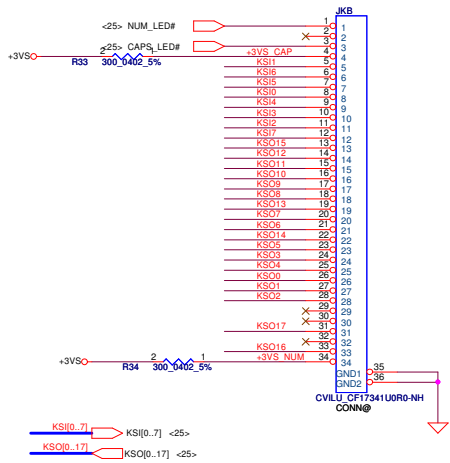


PBTN/B to M/B

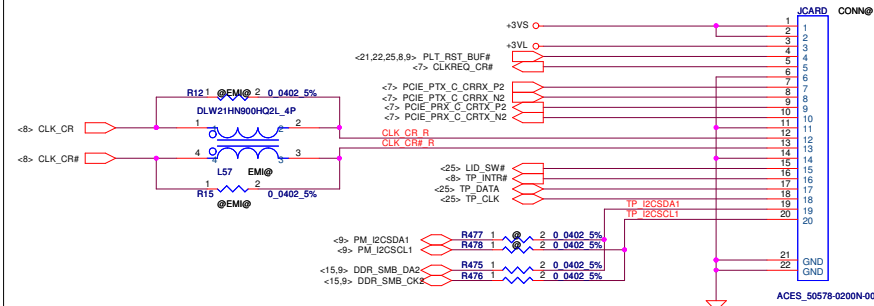
NOTICE: ON/OFFBTN# have pull-high resistance on motherboard



KEYBOARD CONN.



Card Reader + TP + Lid SW

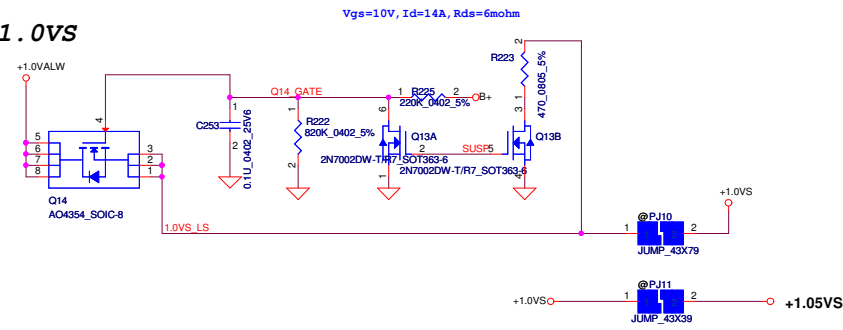


ISPD

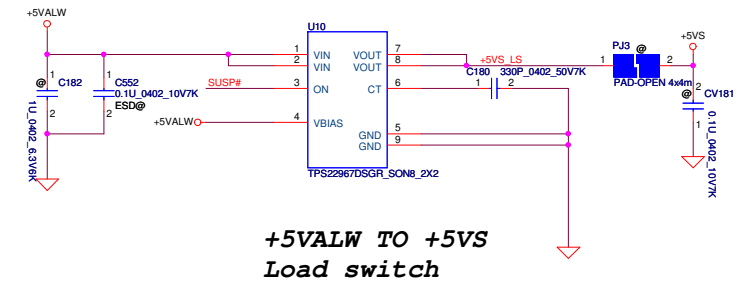


Security Classification	Compal Secret Data	Compal Secret Data	Compal Secret Data
Issued Date	2013/09/25	Deciphered Date	2016/09/25
Title		ISPD/KB/Screw	
Document Number		ZBWAA LA-B303P	
Date		Monday, March 03, 2014	
Sheet		26 of 41	
Rev		1.0	

+1.0VALW TO +1.0VS

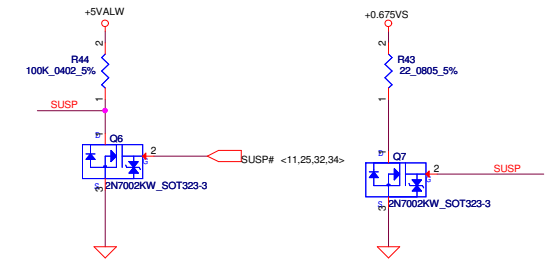
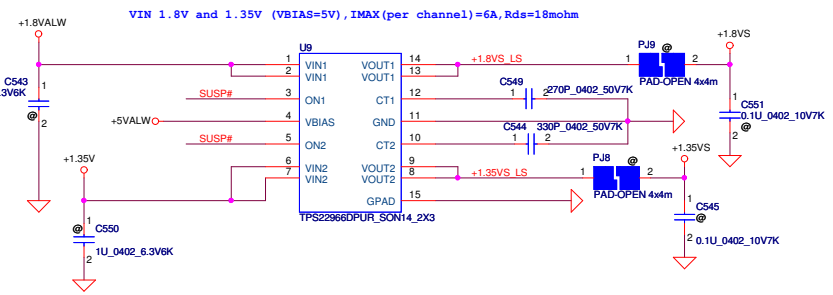


Part number is SA000070S00
VIN 5V (VBIAS=5V), IMAX=4A, Rds=22mohm

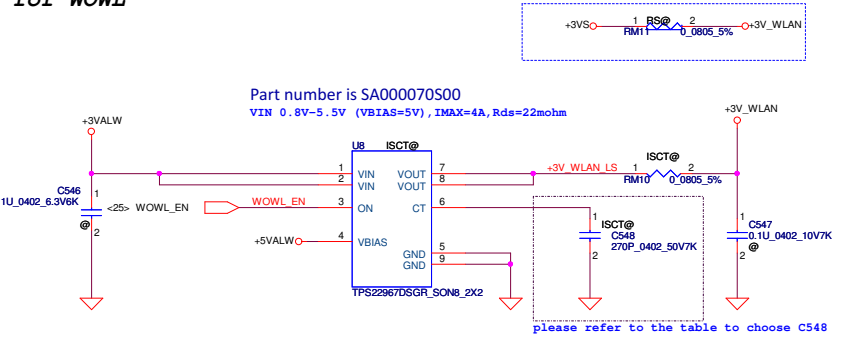


**+5VALW TO +5VS
Load switch**

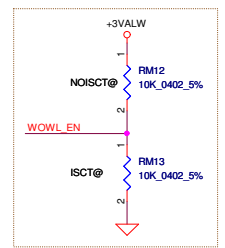
**+1.8VALW TO +1.8VS
+1.35V TO +1.35VS
Load Switch**



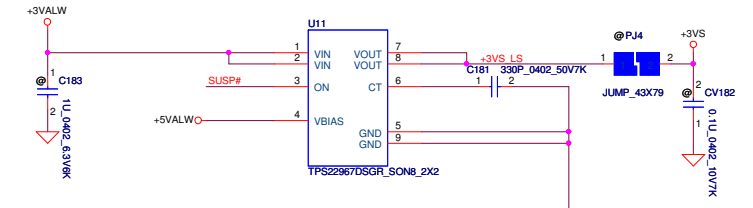
**+3VALW TO +3V_WLAN
for WOWL**



For BC detect ISCT
WOWL_EN : HIGH -> NOISCT
WOWL_EN : LOW -> ISCT



Part number is SA000070S00
VIN 3V (VBIAS=3V), IMAX=4A, Rds=22mohm



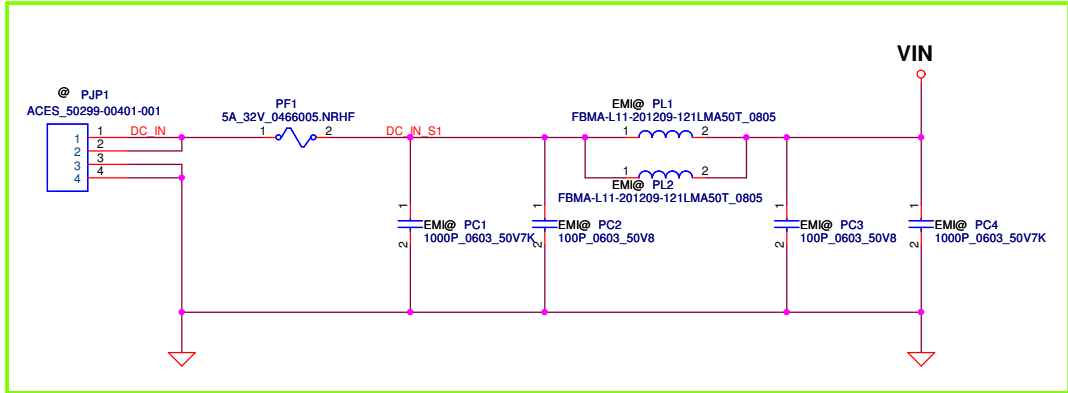
**+3VALW TO +3VS
Load switch**

Security Classification	Compal Secret Data		Compal Electronics, Inc.	
Issued Date	2013/09/25	Deciphered Date	2016/09/25	Title
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				ZBWAA LA-B303P
				Rev 1.0
Date: Monday, March 03, 2014				Sheet 27 of 41

Mark Green frame that means this part is not belong to layout module part .

Function Field :

Support 37.1
 RTC 38.2
 EMI Part 47.1

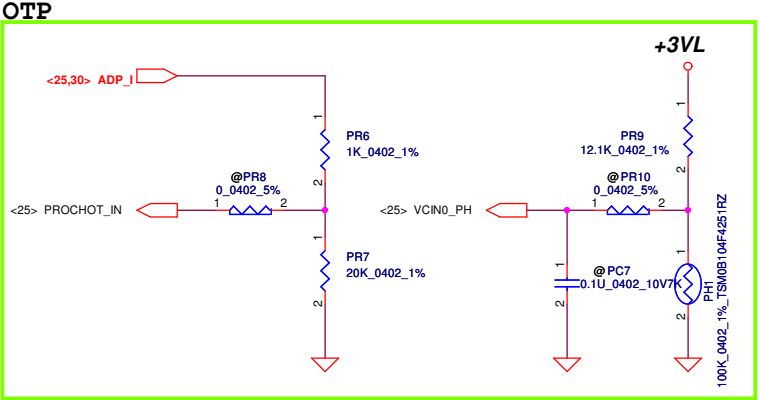
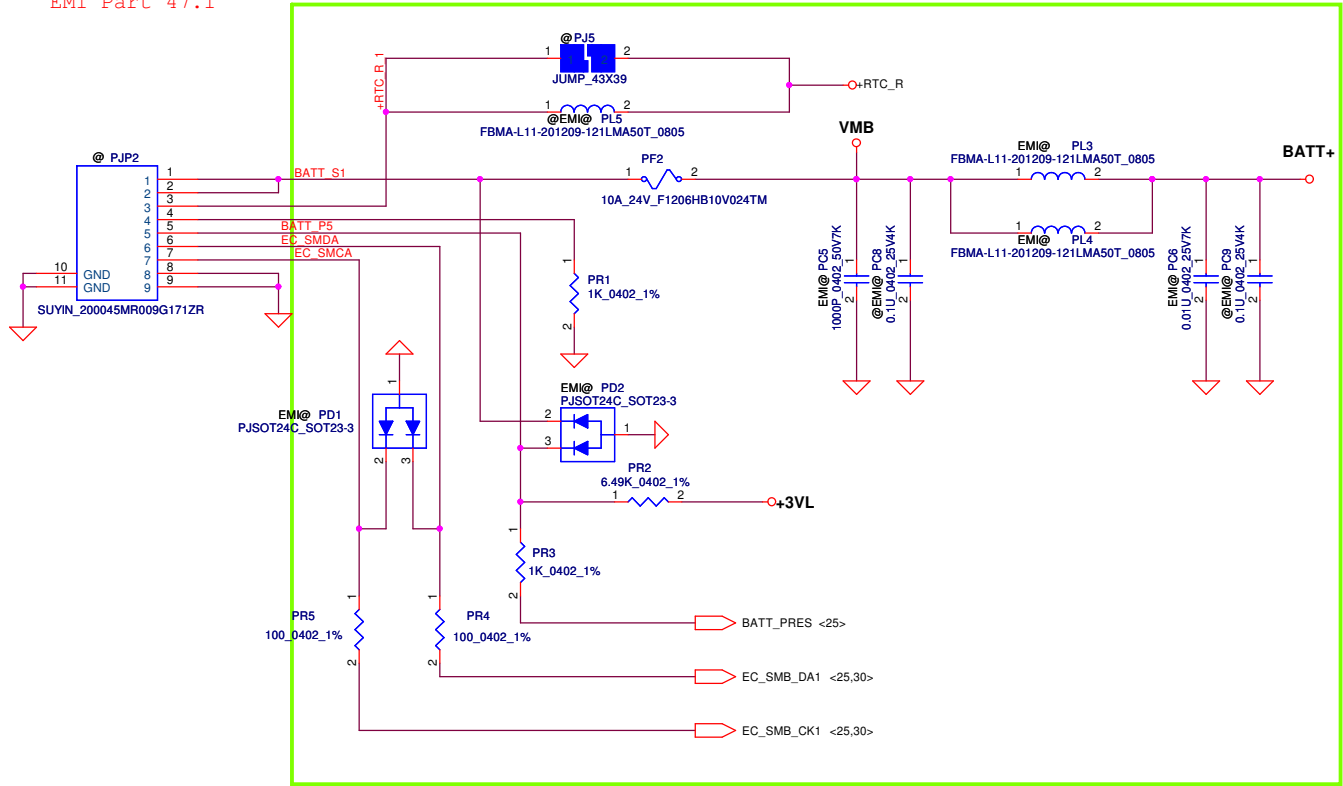


Security Classification	Compal Secret Data			<i>Compal Electronics, Inc.</i>	
Issued Date	2011/06/15	Deciphered Date	2012/07/11	DCIN / RTC Battery	
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				Date:	Monday, March 03, 2014
				Sheet	28 of 41
				Rev	1.0

Mark Green frame that means this part is not belong to layout module part .

Function Field :

Support 37.1
 OTP 39.7
 EMI Part 47.1



	Initial	Recovery
45W UMA	0.55V	0.43V

	Initial	Recovery
CPU OTP	90 C	70 C

Module model information

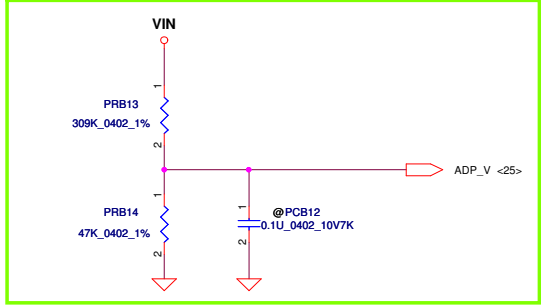
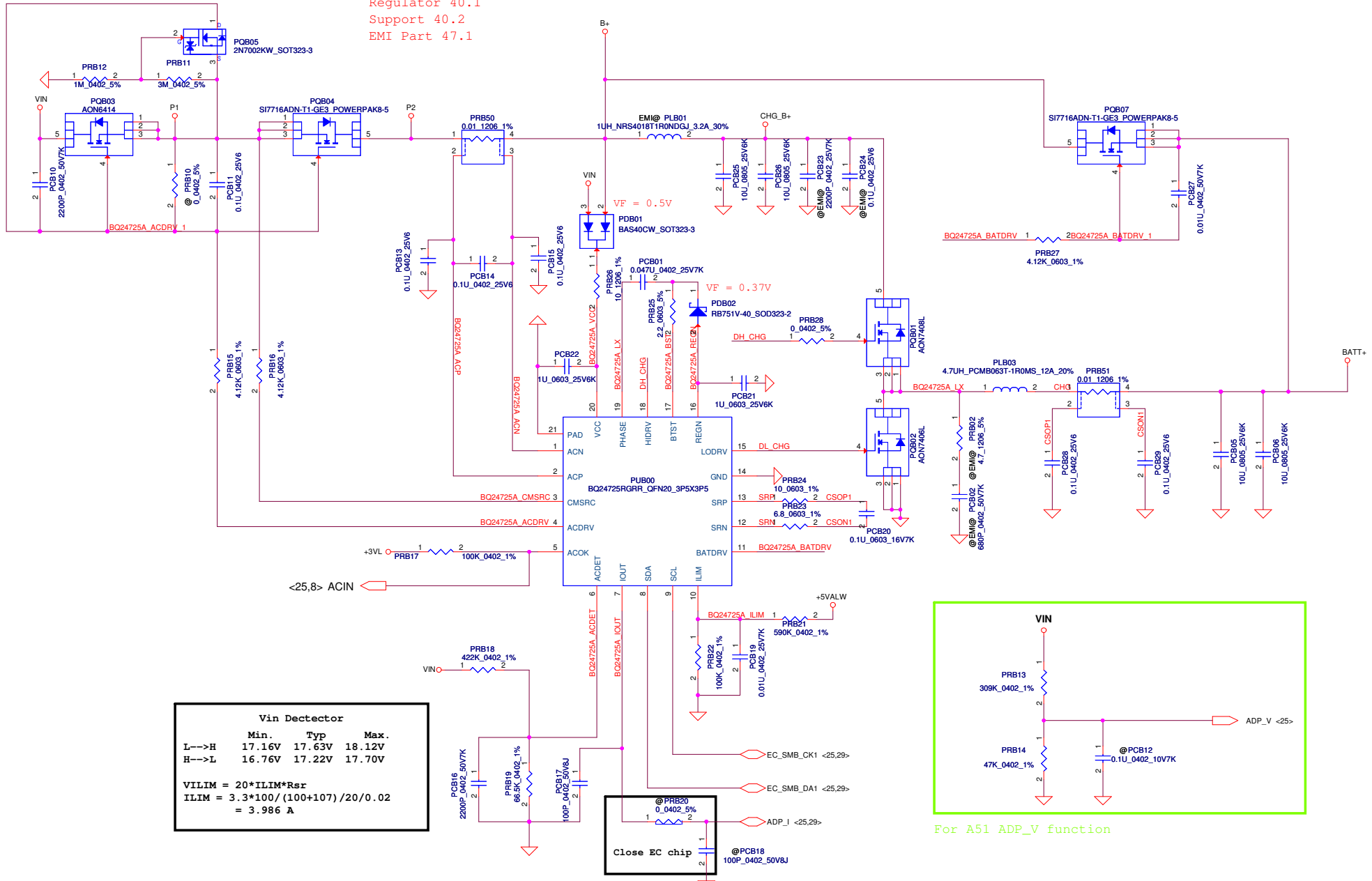
BQ24735A_V1.mdd

BQ24735A_V2.mdd

Mark Green frame that means this part is not belong to layout module part .

Function Field :

- Regulator 40.1
- Support 40.2
- EMI Part 47.1



For A51 ADP_V function

Security Classification	Compal Secret Data		Title	Compal Electronics, Inc.	
Issued Date	2014/07/02	Deciphered Date	2012/07/02	PWR-CHARGER	
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Document Number	Common Circuit		Rev	1.0	
Date	Monday, March 03, 2014	Sheet	30	of 41	

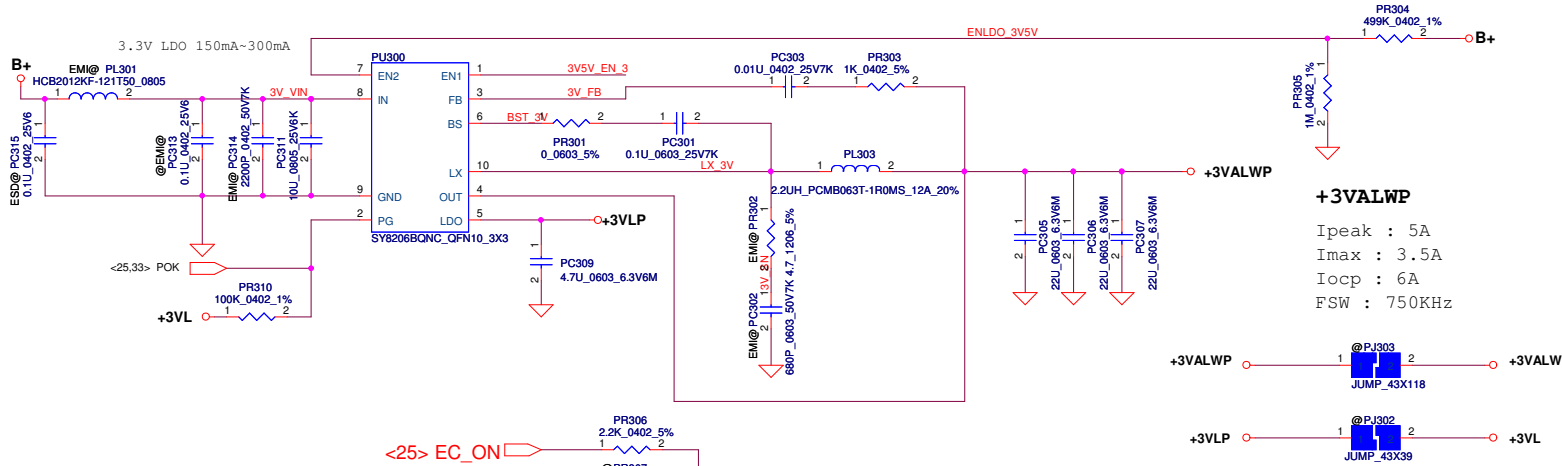
Module model information

SY8206B_V2.mdd

Mark Green frame that means this part is not belong to layout module part .

Function Field :

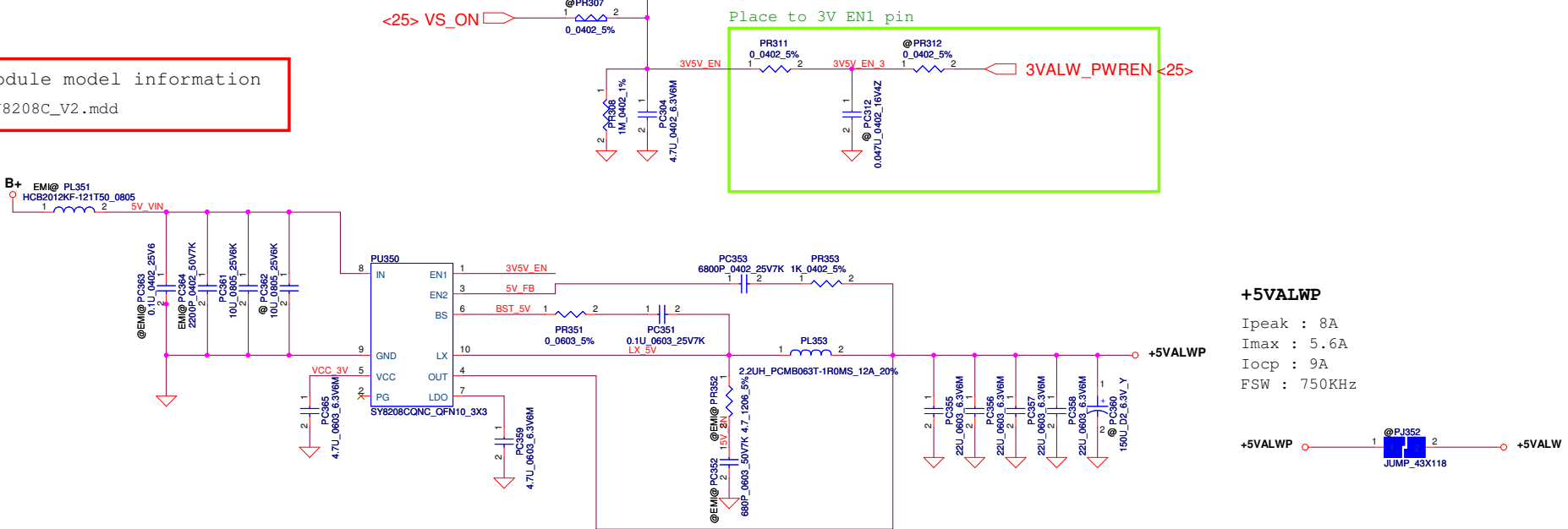
Regulator 35.1
Support 35.2
EMI Part 47.1



+3VALWP
 Ipeak : 5A
 Imax : 3.5A
 Iocp : 6A
 FSW : 750KHz

Module model information

SY8208C_V2.mdd



+5VALWP
 Ipeak : 8A
 Imax : 5.6A
 Iocp : 9A
 FSW : 750KHz

Security Classification		Compal Secret Data		Title	
Issued Date	2011/06/15	Deciphered Date	2012/07/11	Compal Electronics, Inc.	
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				JUMP_43X118	1.0
Date: Monday, March 03, 2014				Sheet	31 of 41

Module model information

RT8207M_V1.mdd For Single layer
RT8207M_V2.mdd For Dual layer

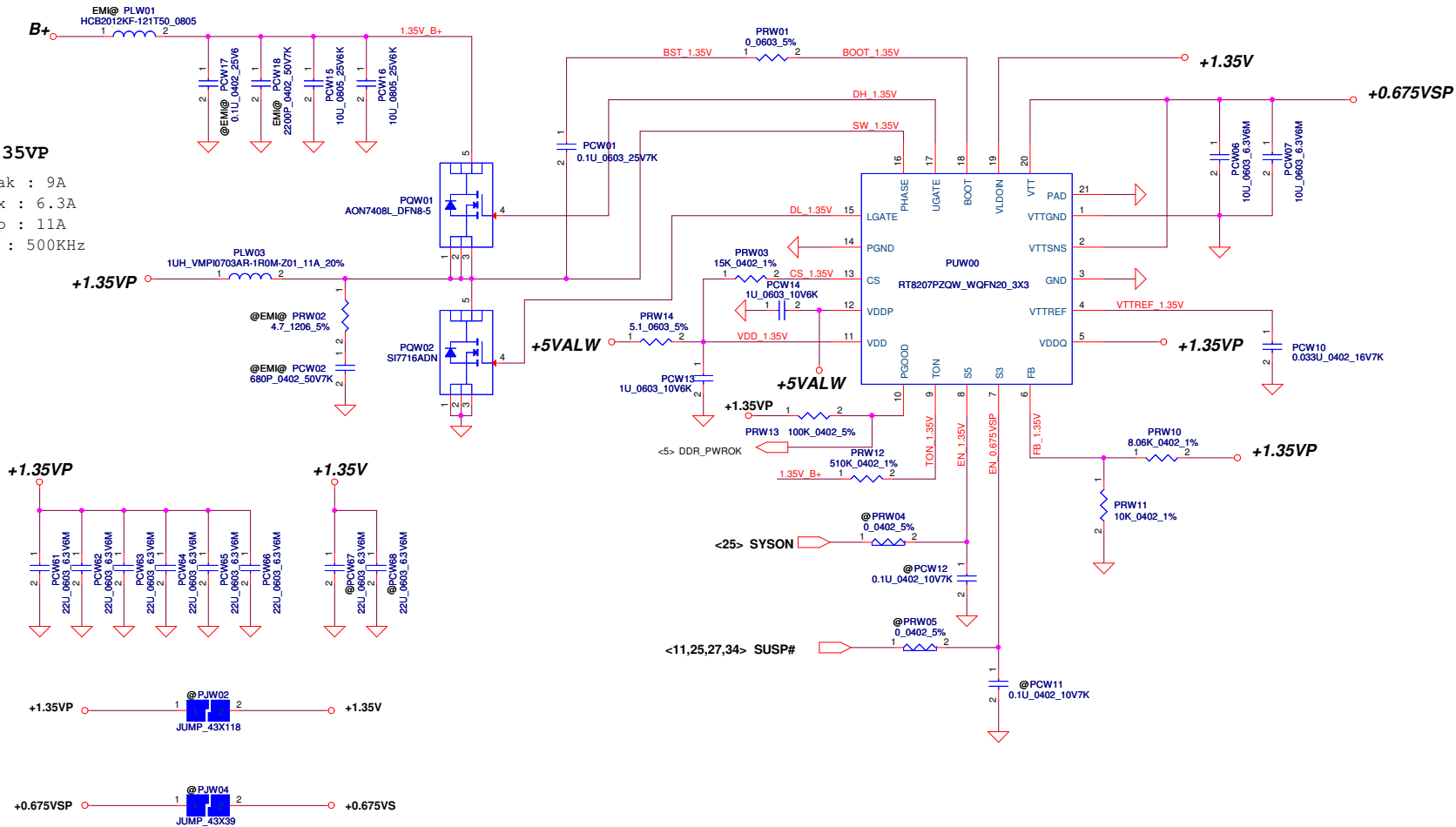
Mark Green frame that means this part is not belong to layout module part .

Function Field :

Regulator 35.3
Support 35.4
EMI Part 47.1

+1.35VP

Ipeak : 9A
Imax : 6.3A
Iocp : 11A
FSW : 500KHz



Module model information

SY8033_V1.mdd

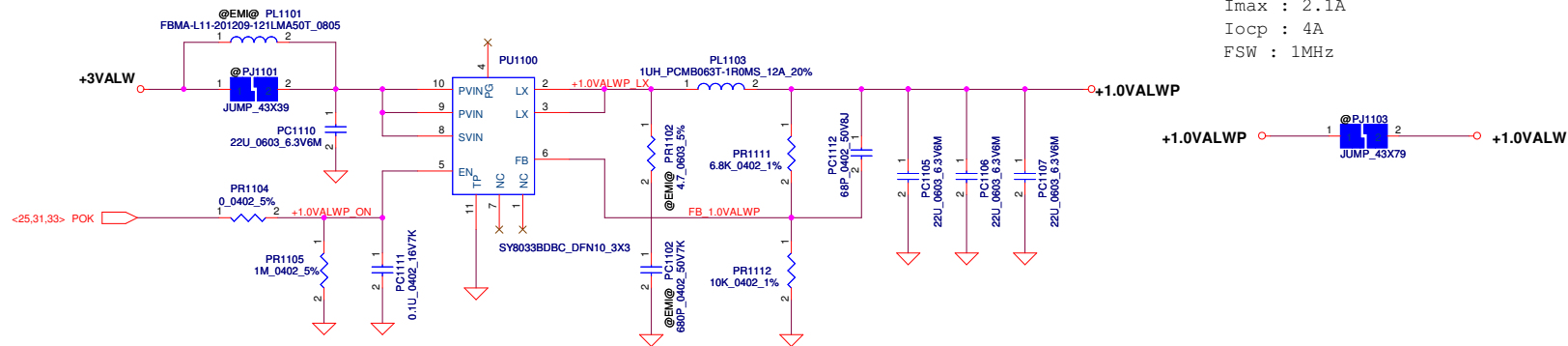
Mark Green frame that means this part is not belong to layout module part .

Function Field :

- +1.8V Regulator 35.15
- +1.8V Support 35.16
- +1.0V Regulator 35.27
- +1.0V Support 35.28
- EMI Part 47.1

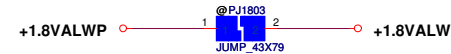
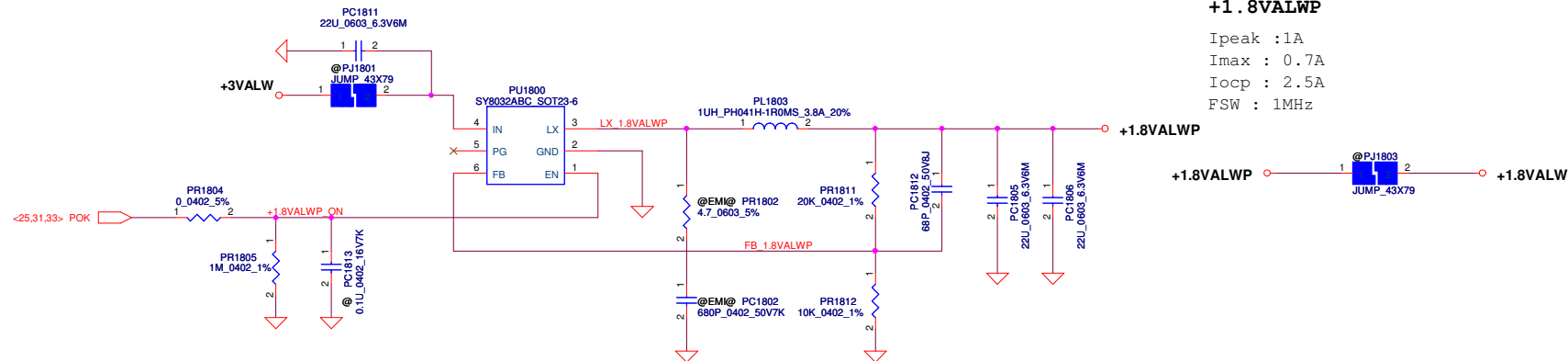
+1.0VALWP

Ipeak : 3A
 Imax : 2.1A
 Iocp : 4A
 FSW : 1MHz



+1.8VALWP

Ipeak : 1A
 Imax : 0.7A
 Iocp : 2.5A
 FSW : 1MHz



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				Rev 1.0 Sheet 33 of 41

Module model information

SY8033_V1.mdd

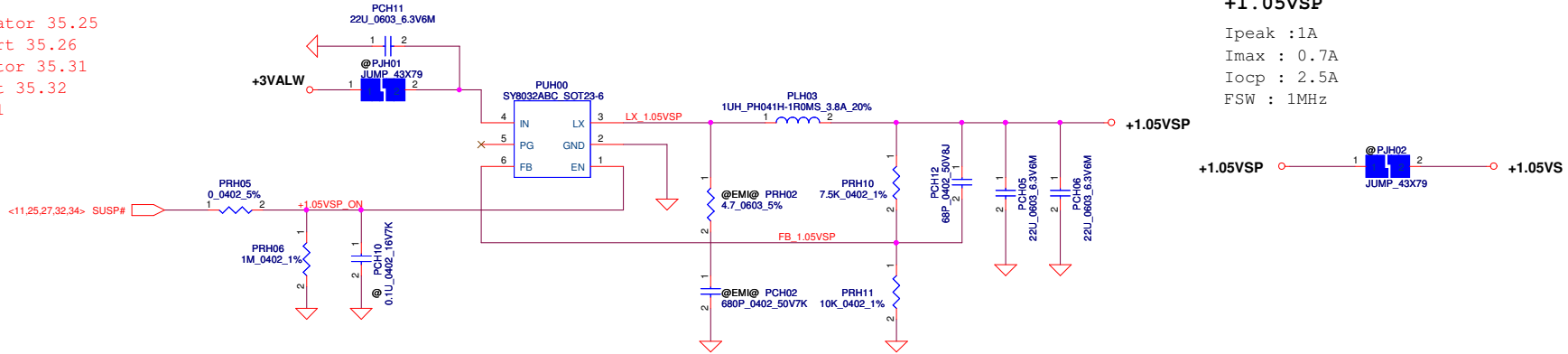
Mark Green frame that means this part is not belong to layout module part .

Function Field :

- +1.05V Regulator 35.25
- +1.05V Support 35.26
- +1.5V Regulator 35.31
- +1.5V Support 35.32
- EMI Part 47.1

+1.05VSP

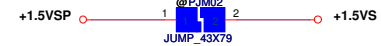
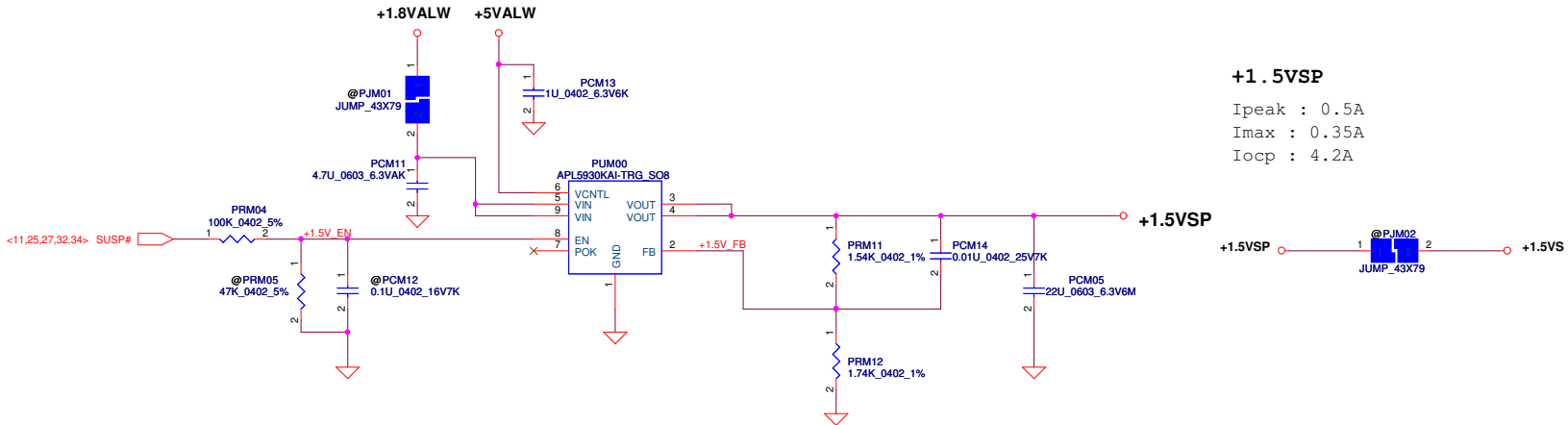
Ipeak : 1A
 Imax : 0.7A
 Iocp : 2.5A
 FSW : 1MHz



+1.8VALW +5VALW

+1.5VSP

Ipeak : 0.5A
 Imax : 0.35A
 Iocp : 4.2A



Security Classification	Compal Secret Data		Title	
Issued Date	2011/06/15	Deciphered Date	2012/07/11	Compal Electronics, Inc.
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				Rev 1.0
Date: Monday, March 03, 2014				Sheet 34 of 41

+1.05VS / +1.5VS

Module model information

ISL95833-BTM_V1A.mdd for IC portion

ISL95833-BTM_V1B.mdd for SW portion

Function Field :

- Regulator 36.1
- Driver 36.2
- Support 36.3
- Output Cap 36.4
- Acoustic Cap 37.2
- EMI Part 47.1

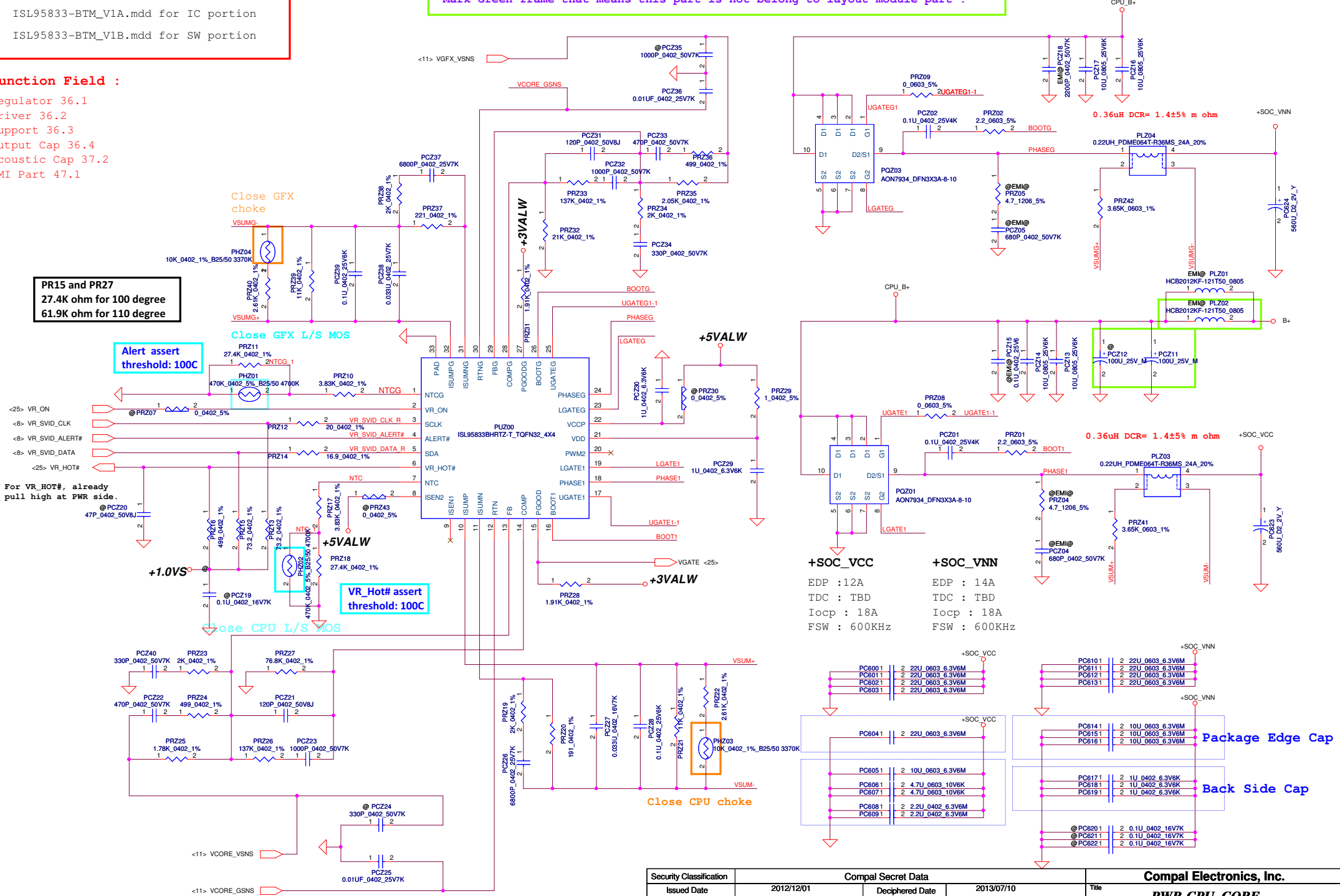
Mark Green frame that means this part is not belong to layout module part .

PR15 and PR27
27.4K ohm for 100 degree
61.9K ohm for 110 degree

Alert assert
threshold: 100C

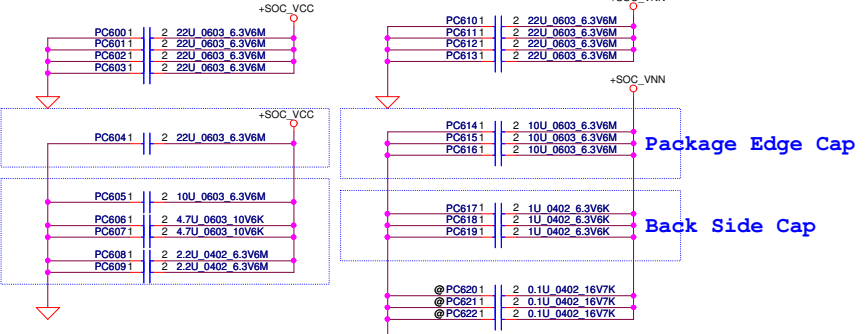
VR_Hot# assert
threshold: 100C

For VR_HOT#, already
pull high at PWR side.



+SOC_VCC
EDP : 12A
TDC : TBD
Iocp : 18A
FSW : 600KHz

+SOC_VNN
EDP : 14A
TDC : TBD
Iocp : 18A
FSW : 600KHz



Security Classification		Compal Secret Data		Compal Electronics, Inc.	
Issued Date	2012/12/01	Deciphered Date	2013/07/10	Title	PWR-CPU_CORE
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Size	Custom	Document Number		Rev	1.0
Date:		Sheet	35	of	41

PWR PIR (Product Improve Record)

ZBWAA LA-B303P SCHEMATIC CHANGE LIST

REVISION CHANGE: 0.1

GERBER-OUT DATE: 2013/10/29

NO DATE PAGE MODIFICATION LIST

PURPOSE

 Item Date Page Action Component Request

Security Classification	Compal Secret Data			Compal Electronics, Inc.	
Issued Date	2010/09/03	Deciphered Date	2012/12/31	Title	PWR-PIR
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				Date: Monday, March 03, 2014	Sheet 36 of 41

HW PIR (Product Improve Record)

ZBWAA LA-B303P SCHEMATIC CHANGE LIST

REVISION CHANGE: 0.2

GERBER-OUT DATE: 2013/11/13

NO DATE PAGE MODIFICATION LIST PURPOSE

Item	Date	Page	Action	Component	Request
1)	11/13	7, 9	Change	change QC1, QC2, QC3 PN to SB000000S700	For PJE request
2)	11/13	25	delete	RPB2 for 9022 design	For EC
3)	11/13	10	delete	RC73, RC76, RC77 bom structure 9012 requirement	For 9022 design
4)	11/13	22	change	QL1 PN from SB000009Q80 to SB000000S700	FOR common design
5)	11/13	24	delete	RA15, RA16 bom structure unpop for audio common design	FOR common design
6)	11/13	16	delete	RT16 for repeat schematic	FOR LVDS translator
7)	11/13	25	change	UB2 name to UB1	For EC
8)	11/13	22	change	NPCT420@ to TPM@ for TPM common design	FOR common design
9)	11/13	24	change	audio codec PIN9 voltage level from 3vs to 1.5vs	FOR common design
10)	11/13	22	change	LANCLK_REQ# pull high voltage from 3vs to 1.8vs	FOR common design
11)	11/13	17	change	R21, D4 bom structure to @	FOR common design
12)	11/13	17	change	change U3 to U50 delete U50, R18 bom structure	FOR common design
13)	11/15	10	change	KBRST# to KB_RST#	FOR common design
14)	11/16	16	add	RT13 for lvds translator	FOR common design
15)	11/16	17	swap	L2 signal swap for layout route kiter	FOR layout
16)	11/20	21	add	R75 pull high BT_ON for 9022@ bom struction	For 9022 design
17)	11/20	12	Delete	RC63 for LPC 3.3V when is used VGA	For bay tail m
18)	11/20	25	add	H11 for stand-off	FOR layout
19)	11/22	10	Delete	UC54, UC60, RC74, RC70 bom structure 9012@ for LPC 3.3V	For bay trail m
20)	11/22	10	change	change UC60 VCCA, EO valtage from 1.8vvalw to 1.8vs	For bay trail m EDS
21)	11/22	25	Delete	delete RB42, RB43 for LPC 3.3V when is used VGA	For LPC
22)	11/23	24	Remove	ALC233 co-layer component, now is for ALC233VB only	FOR common design
23)	11/23	24	change	Unify analog output net name to PR_L/PR_R	FOR common design
24)	11/26	23	Modify	usb hub 24 PIN and usb hub 28PIN co-layer	FOR USB HUB
25)	11/28	18	add	add U12, R145, C265, R186 for HDMI_HPD	FOR HDMI
26)	11/26	26	Add	Add H11 for stand-off	For layout
27)	11/27	25	Change	Delete RB42, RB43 for LPC 3.3V when is used VGA	For LPC
28)	11/27	18	Add	U12, R145, C265, R186 for HDMI_HPD	For HDMI
29)	11/28	23	Change	Hub usb 24 pin and 28 pin co-layer	For cost
30)	11/28	22	Change	change LAN/USB Small board connector pin	For Lan/usb small board
31)	11/28	24	Change	change CA15 material to 10V7K	For audio codec
32)	11/28	17	add	add D6	For bay tail m edp
33)	11/28	9	change	usb port assignment OK	For SW request
34)	11/29	8	delete	delete D1	For RTC
35)	11/29	8	add	add D16, D17	For RTC
36)	11/29	23	Modify	change CR16, CR17, CR18 package 0603 to 0805	For common design
37)	11/29	8	add	add CC19, CC21, D92	For ESD
38)	11/30	6	add	add RC35, RT14	For ENBKL
39)	11/30	27	add	add R106	For commom design
40)	12/02	27	add	add PJ11	For LD request
41)	12/03	17	add	add R4283, R4282 on EMI camera choke	For EMI
42)	12/03	17	change	Change L2 from CAM_EMI@ to @CAM_EMI@	For EMI
43)	12/03	18	delete	delete RY2	For common design
44)	12/03	27	change	change PJ11 from 43x79 to 43x39	For common design
45)	12/04	23	change	change GNDA to REXT_GND	For USB HUB co-layer
46)	12/04	23	add	add UR6, CR2, CR22, CR19, CR20, PJ12	FOR USB issue
47)	12/07	23	change	change UR6, CR2, CR22, CR19, CR20 bom struction to @	FOR USB issue
48)	12/07	25	change	change RB19 materail from 1k_0402_5% to 100k_0402_5%	FOR EC_SWI#
49)	12/07	22, 26	change	change part number from L56, L57 to SM070003K00	FOR X1 code
50)	12/07	23	change	change RR9 bom struction to HUB_28P	FOR USB HUB
51)	12/07	25	delete	delete CA2, CA6, CA9, CA10, CA11, CA22, UA1 bom structure	FOR Common design

Security Classification	Compal Secret Data		Compal Electronics, Inc.	
Issued Date	2010/09/03	Deciphered Date	2012/12/31	Title
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			Rev	1.0
			Sheet	37 of 41

HW PIR (Product Improve Record)

ZBWAA LA-B303P SCHEMATIC CHANGE LIST

REVISION CHANGE: 0.3

GERBER-OUT DATE: 2014/1/10

NO DATE PAGE MODIFICATION LIST PURPOSE

Item	Date	Page	Action	Component	Request
1)	12/27	23	Change	change YR1 PN to SJ10000C210	For main source request
2)	12/27	8,17	Change	change D4,D5,DC1,DC2,DC3,DC4,D6,D16,D17 PN to SCS00003500	For main source request
3)	12/27	8	delete	delete R9 bom structure @	For RTC circuit
4)	12/27	8	add	Add D17,R2 bom structure @	For RTC circuit
5)	12/27	24	change	change CA28,CA29,CA30,CA31 bom structure to EMI@	For EMI request
6)	12/27	10	change	change RC77 PN from SD028470180 to SD028220180	For SOC_SCI# issue verify
7)	12/27	9	add	Add DC2,DC3 bom structure @	FOR USB_OC# issue verify
8)	12/27	17	add	Add R431 bom structure TOUCH@	For touch screen circuit
9)	12/27	8	change	change CC10,CC11 PN to SE071120J80	For HW Design change
10)	12/27	8	change	change CC16,CC17 PN to SE071150J80	for HW Design change
11)	12/27	17,25	change	change Q1,Q6,QB1 PN to SB000009Q80	for main source request
12)	12/27	18	change	change QY1,QY2 PN to SB00000S700	for main source request
13)	12/27	14	remove	remove XDP related materail	for ESD team request
14)	12/27	8	add	add RC38,RC39 for XDP	for XDP circuit
15)	01/02	10	add	add RC78,RC79 for slp_S3&S4	for HW Design change
16)	01/02	10	add	add RC70,RC71 bom structure @	for HW Design change
17)	01/02	10	add	add RC79 bom structure 9012@	for HW Design change
18)	01/02	25	delete	delete R107	for 9022 circuit
19)	01/03	8	change	change CC19 net from PMC_PLTRST# to PLT_RST_BUF#	for ESD team request
20)	01/03	8	change	change CC19 bom structure form @ESD@ to ESD@	for ESD team request
21)	01/03	10	change	change RC73,RC76 PN from SD028470180 to SD028220180	for HW design change
22)	01/03	27	add	add C552 on +5VALW	for ESD team request
23)	01/04	8	add	add RC40 for PMC_CORE_PWROK	for RTC power consumption
24)	01/06	9	add	add thermal sensor schematic	for thermal team request
25)	01/08	20	change	change JFAN footprint to ACES_50271-0030N-001_3P	for DFX team request
26)	01/08	8	add	add RC41,RC65 for touch screen detect	for signal name rule
27)	01/08	17	change	change +LCD_ENVDD_R to LCD_ENVDD_R	for common design request
28)	01/09	17	change	change D29 bom structure @ESD@ to ESD@	for ESD team request
29)	01/09	24	change	change UA1 compal PN from SA00007BF00 to SA00007BF10	for audio codec
30)	01/09	25	add	add UB1 107 pin net 3VALW_PWREN	for commond design request
31)	01/09	25	change	change RB19 to 1k_0402_5%	for LAN wake circuit
32)	01/10	9	add	add bom structure thermal@ config	for thermal sensor circuit
33)	01/10	8	change	change RC38 value from 51_0402_5% to 200_0402_5%	for XDP circuit request

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Date:	Monday, March 03, 2014	Sheet	38	of 41

HW PIR (Product Improve Record)

ZBWAA LA-B303P SCHEMATIC CHANGE LIST

REVISION CHANGE: 0.4

GERBER-OUT DATE: 2014/01/24

NO DATE PAGE MODIFICATION LIST PURPOSE

Item	Date	Page	Action	Component	Request
1)	01/24	8	Change	change RC41 BOM Structure from Touch@ to @	For HW design change
2)	01/24	8	Change	change RC65 Bom Structure from Notouch@ to @	For HW design change
3)	01/24	17	Add	add R8 for touch screen	For HW design change
4)	01/27	22	Add	add R17 for Disable/Enable lan chip	For power consumption
5)	01/27	20	change	change JHDD footprint to LCN_ASF98-2231S10-0002_22P	For DFB request
6)	01/28	17	Add	add R30 for touch screen	For HW design change
7)	01/28	23	Add	add RR27,RR28 for usb_hub	For HW design change
8)	01/28	23	Add	add CR13 for 2nd source droop issue	For common design
9)	01/28	25	Add	add EC pin 18 net name RTC_TEST#	For common design
10)	01/28	25	Add	add EC pin 25 net name LAN_OFF#	For common design
11)	01/28	25	Add	add R31 for RTC_TEST#	For common design
12)	02/11	17	Change	change R4280,R4281 BOM structure from touch_EMI@ to EMI@	For Touch screen
13)	02/11	17	Change	change L61 BOM structure from @touch_EMI@ to @EMI@	For Touch screen
14)	02/11	17	delete	delete R431 BOM structure touch@	For Touch screen

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Date:	Friday, March 07, 2014		Sheet	39	of 41

HW PIR (Product Improve Record)

ZBWAA LA-B303P SCHEMATIC CHANGE LIST

REVISION CHANGE: 1.0

GERBER-OUT DATE: 2014/03/03

NO DATE PAGE MODIFICATION LIST PURPOSE

Item	Date	Page	Action	Component	Request
1)	02/22	10	Change	change RC78,RC79 value 4.7K_0402_5% to 10K_0402_5%	For HW design change
2)	02/22	10	Add	Add RC11,RC66	For HW design change
3)	02/22	27	Change	change C549 PN from SE074271KL0 to SE074271k80	For HW design change
4)	02/22	8	Change	change RP1 PN from SD309510A80 to SD309510A10	For HW design change
5)	02/22	24	delete	delete RA13&RA18	For audio common design
6)	02/22	24	change	change 0 ohm RA1,RA2,RA10,RA11,RA14,RA20.RA21 to short pad	For audio common design
7)	02/22	23	Add	add YR1 SJ10000DH00 for USB_HUB_28P	For vender request
8)	02/22	10	change	change UC59 BOM structure 9012@ to @	For HW design change
9)	02/24	22	Add	Add Q10,RL5,RL6,CL1,CL2,CL3,CL4 for reserve circuit	For Lan lost issue
10)	02/24	22	change	change RL3 short pad to 0 ohm	For HW design change
11)	02/25	26	change	change SW2 BOM config from mount to un-mount	For Pre-MP phase
12)	02/25	26	change	change screw hole size for H1,H2,H3.	For ME request
13)	02/26	17~	change	change 0 ohm R3,RC55,RC60,RC61,RC62,R18,R4280,R4281.R4282, R4283,R17,RR10,RR12,RR14,RR16,RR18,RR21,RR22,RR25,R29,RC14, R431,R432,R26,RR6,RT1,R106,RM11 to short pad	For 0 ohm short pad
14)	02/26	17	change	change R30,R8 mount to un-mount	For HW design change

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Date:	Monday, March 03, 2014	Sheet	40 of 41	

